## Analog Integrated Circuits

Power Management, Signal Conditioning and ASSP Devices

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#### Abstract

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## CHAPTER 1

 Family Tree and Selector GuideON Semiconductor's Analog Integrated Circuits



## Single Operational Amplifiers

| Device Name | $\mathrm{V}_{\mathrm{Cc}}$ <br> (min) <br> (V) | $\begin{gathered} \mathrm{V}_{\mathrm{Cc}} \\ (\max ) \\ (\mathrm{V}) \end{gathered}$ | $\begin{gathered} \text { GBW } \\ \text { (typ) } \\ \text { (MHz) } \end{gathered}$ | Slew <br> Rate <br> (typ) <br> (V/us) | $\begin{gathered} \mathrm{V}_{10} \\ \left(\max @ 25^{\circ} \mathrm{C},\right. \\ \mathrm{Vs}=5.0 \mathrm{~V}) \\ (\mathrm{mV}) \end{gathered}$ | $I_{\text {IB }}$ (typ) <br> (nA) | $\begin{gathered} \mathbf{I}_{\mathbf{D}} \\ (\operatorname{typ}) \\ (\mathrm{mA}) \end{gathered}$ | Temp Range $\left({ }^{\circ} \mathrm{C}\right)$ | CMR <br> (typ) <br> (dB) | $\mathbf{e n}_{n}$ (typical) $(\mathrm{nV} / \sqrt{\mathrm{Hz}})$ <br> $@ \mathrm{f}=1.0 \mathrm{kHz}$ | Number of Channels | Supply Type | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LM301A | $\pm 3.0$ | $\pm 18$ | 1.0 | 0.5 | 7.5 | 250 | 1.8 | 0 to 70 | 90 | - | 1 | Split | $\begin{gathered} \hline \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | General Purpose Precision <br> Non Compensated |
| LM201A | $\pm 3.0$ | $\pm 22$ | 1.0 | 0.5 | 2.0 | 75 | 1.8 | $\begin{gathered} -25 \text { to } \\ +150 \end{gathered}$ | 96 | - | 1 | Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | General <br> Non Compensated |
| MC34071 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | 44 | 4.5 | 13* | 5.0 | 100 | 1.6 | 0 to 70 | 97 | 32 | 1 | Single, Split | $\begin{aligned} & \text { DIP-8, } \\ & \text { SO-8 } \end{aligned}$ | High SR, Wide BW, Single Supply, *Av = -1.0 |
| MC34071A | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | 44 | 4.5 | 13* | 3.0 | 100 | 1.6 | 0 to 70 | 97 | 32 | 1 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | High SR, Wide BW, Single <br> Supply, *Av = -1.0 |
| MC33071 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | 44 | 4.5 | 13* | 5.0 | 100 | 1.6 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 97 | 32 | 1 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | High SR, Wide BW, Single <br> Supply, *Av=-1.0 |
| MC33071A | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | 44 | 4.5 | 13* | 3.0 | 100 | 1.6 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 97 | 32 | 1 | Single, Split | $\begin{aligned} & \text { DIP-8, } \\ & \text { SO-8 } \end{aligned}$ | High SR, Wide BW, Single Supply, *Av = -1.0 |
| MC33201 | $\begin{gathered} 1.8 \text { or } \\ \pm 0.9 \end{gathered}$ | 12 | 2.2 | 1.0 | 6.0 | 200 | 0.9 | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 90 | 20 | 1 | Single, Split | $\begin{aligned} & \text { DIP-8, } \\ & \text { SO-8 } \end{aligned}$ | Low Voltage, Rail-to-Rail |
| MC33201V | $\begin{aligned} & 1.8 \text { or } \\ & \pm 0.9 \end{aligned}$ | 12 | 2.2 | 1.0 | 6.0 | 200 | 0.9 | $\begin{gathered} -55 \text { to } \\ +125 \end{gathered}$ | 90 | 20 | 1 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Low Voltage, Rail-to-Rail, Extended Temp. Range |
| MC33171 | $\begin{aligned} & 3.0 \text { or } \\ & \pm 1.5 \end{aligned}$ | $\begin{aligned} & 44 \text { or } \\ & \pm 22 \end{aligned}$ | 1.8 | 2.1 | 4.5 | 20 | 0.18 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 90 | 32 | 1 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Low Power, Single Supply, Two Voltage Ranges |
| MC33501 | $\begin{aligned} & 1.0 \text { or } \\ & \pm 0.5 \end{aligned}$ | $\begin{gathered} 7.0 \text { or } \\ \pm 3.5 \end{gathered}$ | $\begin{gathered} 4 @ \\ \mathrm{Vs}=5 \end{gathered}$ | 3.0 | 5.0 | $\begin{gathered} 0.04 \\ \mathrm{pA} \end{gathered}$ | $\begin{gathered} 1.65 / \\ 1.2 @ \\ \mathrm{Vs}=1 \mathrm{~V} \end{gathered}$ | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 75 | 30 | 1 | Single, Split | TSOP-5 | One Volt SMARTMOS ${ }^{T M}$, Rail-to-Rail |

Single Operational Amplifiers (continued)

| Device Name | $\mathrm{V}_{\mathrm{cc}}$ (min) (V) | $\underset{(\max )}{\mathrm{V}_{\mathrm{CC}}}$ <br> (V) | $\begin{aligned} & \text { GBW } \\ & \text { (typ) } \\ & \text { (MHz) } \end{aligned}$ | Slew <br> Rate <br> (typ) <br> (V/us) | $\begin{gathered} \mathrm{V}_{10} \\ \left(\max @ 25^{\circ} \mathrm{C},\right. \\ \mathrm{Vs}=5.0 \mathrm{~V}) \\ (\mathrm{mV}) \end{gathered}$ | $\underset{(\mathrm{lyp})}{\mathrm{I}_{\mathrm{B}}}$ ( nA ) | $\begin{gathered} \mathbf{I}_{\mathbf{D}} \\ (\text { (typ) } \\ \text { (mA) } \end{gathered}$ | Temp Range $\left({ }^{\circ} \mathrm{C}\right)$ | CMR <br> (typ) <br> (dB) | $\begin{gathered} \mathbf{e}_{\boldsymbol{n}} \\ \text { (typical) } \\ (\mathrm{nV} / \sqrt{\mathrm{Hz}}) \\ @ \mathrm{f}=1.0 \mathrm{kHz} \end{gathered}$ | Number <br> of <br> Channels | Supply Type | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MC33503 | $\begin{gathered} 1.0 \text { or } \\ \pm 0.5 \end{gathered}$ | $\begin{gathered} 7.0 \text { or } \\ \pm 3.5 \end{gathered}$ | $\begin{gathered} 4 @ \\ \mathrm{~V}_{\mathrm{s}=5} \end{gathered}$ | 3.0 | 5.0 | $\begin{gathered} 0.04 \\ \mathrm{pA} \end{gathered}$ | $\begin{gathered} 1.65 / \\ 1.2 @ \\ \mathrm{Vs}=1 \mathrm{~V} \end{gathered}$ | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 75 | 30 | 1 | Single, Split | TSOP-5 | One Volt SMARTMOS, Rail-to-Rail |
| NCS7101 | $\begin{aligned} & 1.8 \text { or } \\ & \pm 0.9 \end{aligned}$ | $\begin{aligned} & 12 \text { or } \\ & \pm 6.0 \end{aligned}$ | 1.0 | 1.2 | 6.0 | 40 pA | 1.1 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 65 | 500 | 1 | Single, Split | TSOP-5 | Low Voltage, Rail-to-Rail |
| NCS2001 | $\begin{aligned} & 0.9 \text { or } \\ & \pm 0.45 \end{aligned}$ | $\begin{gathered} 7.0 \text { or } \\ \pm 3.5 \end{gathered}$ | 1.4 | 1.6 | 6.0 | 10 pA | 1.0 | 0 to 70 | 70 | 100 | 1 | Single, Split | TSOP-5 | One Volt, CMOS Rail-to-Rail |

## Dual Operational Amplifiers

| Device Name | $V_{C C}$ <br> (min) <br> (V) | $\begin{gathered} \mathrm{V}_{\mathrm{Cc}} \\ (\max ) \\ (\mathrm{V}) \end{gathered}$ | GBW <br> (typ) <br> (MHz) | Slew <br> Rate <br> (typ) <br> (V/us) | $\begin{gathered} \hline \mathrm{V}_{1 \mathrm{O}} \\ \left(\max @ 25^{\circ} \mathrm{C},\right. \\ \mathrm{Vs}=5.0 \mathrm{~V}) \\ (\mathrm{mV}) \end{gathered}$ | $I_{\text {IB }}$ (typ) ( nA ) | $I_{D}$ (typ) (mA) | Temp Range $\left({ }^{\circ} \mathrm{C}\right)$ | CMR <br> (typ) <br> (dB) | $\mathbf{e n}_{n}$ (typical) $(\mathrm{nV} / \sqrt{\mathrm{Hz}})$ @ $f=1.0 \mathrm{kHz}$ | Number of Channels | Supply Type | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MC34072 | $\begin{gathered} 3.0 \mathrm{or} \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | 13* | 5.0 | 500 | 3.2 | 0 to 70 | 97 | 32 | 2 | Single, Split | $\begin{gathered} \hline \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | High SR, Wide BW, Single Supply, *Av = -1.0 |
| MC34072A | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | $13^{*}$ | 3.0 | 500 | 3.2 | 0 to 70 | 97 | 32 | 2 | Single, Split | $\begin{aligned} & \text { DIP-8, } \\ & \text { SO-8 } \end{aligned}$ | High SR, Wide BW, Single Supply, *Av = -1.0 |
| MC34072V | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | 44 or $\pm 22$ | 4.5 | 13* | 3.0 | 500 | 3.2 | $\begin{gathered} -40 \text { to } \\ +125 \end{gathered}$ | 97 | 32 | 2 | Single, Split | SO-8 | High SR, Wide BW, Single Supply, *Av = -1.0 |
| MC33072 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | 13* | 5.0 | 500 | 3.2 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 97 | 32 | 2 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | High SR, Wide BW, Single Supply, *Av $=-1.0$ |
| MC33072A | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | 44 | 4.5 | $13^{*}$ | 3.0 | 500 | 3.2 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 97 | 32 | 2 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | High SR, Wide BW, Single Supply, *Av = -1.0 |
| MC33202 | $\begin{aligned} & 1.8 \text { or } \\ & \pm 0.9 \end{aligned}$ | 12 | 2.2 | 1.0 | 8.0 | 200 | 1.8 | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 90 | 20 | 2 | Single, Split | DIP-8, SO-8, Micro8 ${ }^{\text {m }}$ | Low Voltage, Rail-to-Rail |
| MC33202V | 1.8 | 12 | 2.2 | 1.0 | 8.0 | 200 | 1.8 | $\begin{gathered} -55 \text { to } \\ +125 \end{gathered}$ | 90 | 20 | 2 | Single, Split | $\begin{aligned} & \text { DIP-8, } \\ & \text { SO-8 } \end{aligned}$ | Low Voltage, Rail-to-Rail, Extended Temp. Range |
| MC33172 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 1.8 | 2.1 | 4.5 | 20 | 0.36 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 90 | 32 | 2 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Low Power, Single Supply, Two Voltage Ranges |
| MC33502 | 1.0 | 7.0 | 5.0 | 3.0 | 5.0 | $\begin{gathered} 0.04 \\ \mathrm{pA} \end{gathered}$ | 2.4 | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 75 | 30 | 2 | Single, Split | TSOP-5 | One Volt SMARTMOS, Rail-to-Rail |
| MC33078 | $\pm 5.0$ | $\pm 18$ | 16 | 7.0 | 2.0 | 300 | 4.1 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 100 | 4.5 | 2 | Split | SO-8 | Low Noise |
| MC33178 | $\pm 2.0$ | $\pm 18$ | 5.0 | 2.0 | 3.0 | 100 | - | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 110 | 7.5 | 2 | Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | High Output Current, Low Power, Low Noise |
| MC33272A | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 24 | 10 | $\begin{aligned} & 1 @ \mathrm{Vs}= \pm 15 \mathrm{~V} \\ & 2 @ \mathrm{Vs}=5.0 \mathrm{~V} \end{aligned}$ | 300 | 2.15 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 100 | 18 | 2 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Single Supply, High SR, Low Input Offset Voltage |

Dual Operational Amplifiers (continued)

| Device Name | $\mathrm{V}_{\mathrm{Cc}}$ <br> (min) <br> (V) | $\begin{gathered} \mathbf{V}_{\mathrm{Cc}} \\ (\max ) \\ (\mathrm{V}) \end{gathered}$ | GBW <br> (typ) <br> (MHz) | Slew <br> Rate <br> (typ) <br> (V/us) | $\begin{gathered} \mathrm{V}_{1 \mathrm{O}} \\ \left(\max @ 25^{\circ} \mathrm{C},\right. \\ \mathrm{Vs}=5.0 \mathrm{~V}) \\ (\mathrm{mV}) \end{gathered}$ | $I_{\text {IB }}$ (typ) <br> (nA) | $I_{D}$ <br> (typ) <br> (mA) | Temp Range ( ${ }^{\circ} \mathrm{C}$ ) | CMR <br> (typ) <br> (dB) | $\begin{gathered} \mathbf{e}_{\mathbf{n}} \\ \text { (typical) } \\ (\mathrm{nV} / \sqrt{\mathrm{Hz}}) \\ @ \mathrm{f}=1.0 \mathrm{kHz} \end{gathered}$ | $\begin{aligned} & \text { Number } \\ & \text { of } \\ & \text { Channels } \end{aligned}$ | Supply Type | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LM833 | $\pm 2.5$ | 36 | 15 | 7.0 | 5.0 | 300 | 4.0 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 100 | 4.5 | 2 | Single, Split | $\begin{gathered} \hline \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Low Noise |
| LM358 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 32 \text { or } \\ \pm 18 \end{gathered}$ | 1.0 | 0.6 | 7.0 | 45 | 0.7 | 0 to 70 | 70 | - | 2 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Low Noise |
| LM258 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 32 \text { or } \\ \pm 18 \end{gathered}$ | 1.0 | 0.6 | 5.0 | 45 | 0.7 | $\begin{gathered} -25 \text { to } \\ +85 \end{gathered}$ | 85 | - | 2 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Low Noise |
| LM2904 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 26 \text { or } \\ \pm 13 \end{gathered}$ | 1.0 | 0.6 | 7.0 | 45 | 0.7 | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 70 | - | 2 | Single, Split | $\begin{gathered} \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ | Low Power |
| LM2904V | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 26 \text { or } \\ \pm 13 \end{gathered}$ | 1.0 | 0.6 | 7.0 | 45 | 0.7 | $\begin{gathered} -40 \text { to } \\ +125 \end{gathered}$ | 70 | - | 2 | Single, Split | $\begin{aligned} & \text { DIP-8, } \\ & \text { SO-8 } \end{aligned}$ | Low Power |
| TCA0372 | $\begin{gathered} 5.0 \text { or } \\ \pm 2.5 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 1.4 | 1.4 | 15 | 100 | 5.0 | $\begin{gathered} -40 \text { to } \\ +125 \end{gathered}$ | 90 | 22 | 2 | Single, Split | $\begin{gathered} \text { SOP } \\ (12+2+2) \\ \text { DIP-8, } \\ \text { DIP-16 } \end{gathered}$ | Power, High Current |
| MC33077 | $\pm 2.5$ | $\pm 18$ | 37 | 11 | $1 @ \mathrm{Vs}= \pm 15 \mathrm{~V}$ | 280 | 3.5 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 107 | 4.4 | 2 | Split | $\begin{aligned} & \text { DIP-8, } \\ & \text { SO-8 } \end{aligned}$ | Low Noise |

## Quad Operational Amplifiers

| Device Name | $\mathrm{V}_{\mathrm{Cc}}$ <br> (min) <br> (V) | $\begin{gathered} \mathrm{V}_{\mathrm{cc}} \\ (\max ) \\ (\mathrm{V}) \end{gathered}$ | GBW <br> (typ) <br> (MHz) | Slew <br> Rate <br> (typ) <br> (V/us) | $\begin{gathered} \mathrm{V}_{10} \\ \left(\max @ 25^{\circ} \mathrm{C},\right. \\ \mathrm{Vs}=5.0 \mathrm{~V}) \\ (\mathrm{mV}) \end{gathered}$ | $I_{\text {IB }}$ (typ) (nA) | $\begin{gathered} \mathbf{I}_{\mathbf{D}} \\ (\operatorname{typ}) \\ (\mathrm{mA}) \end{gathered}$ | Temp Range $\left({ }^{\circ} \mathrm{C}\right)$ | CMR <br> (typ) <br> (dB) | $\mathbf{e n}_{n}$ (typical) $(\mathrm{nV} / \sqrt{\mathrm{Hz}})$ <br> @ f=1.0 kHz | $\begin{aligned} & \text { Number } \\ & \text { of } \\ & \text { Channels } \end{aligned}$ | Supply Type | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MC34074 | $\begin{gathered} 3.0 \\ \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | 13* | 5.0 | 100 | 6.4 | 0 to 70 | 97 | 32 | 4 | Single, Split | $\begin{gathered} \hline \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | High SR, Wide BW, Single Supply, *AV = -1.0 |
| MC34074A | $\begin{gathered} 3.0 \\ \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | 13* | 3.0 | 100 | 6.4 | 0 to 70 | 97 | 32 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | High SR, Wide BW, Single Supply, *AV = -1.0 |
| MC34074V | $\begin{gathered} 3.0 \\ \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | 13* | 3.0 | 100 | 6.4 | $\begin{gathered} -40 \text { to } \\ +125 \end{gathered}$ | 97 | 32 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | High SR, Wide BW, Single Supply, *AV = -1.0 |
| MC33074 | $\begin{gathered} 3.0 \\ \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | 13* | 5.0 | 100 | 6.4 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 97 | 32 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14, } \\ \text { TSSOP-14 } \end{gathered}$ | High SR, Wide BW, Single Supply, *AV =-1.0 |
| MC33074A | $\begin{gathered} 3.0 \\ \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 44 \text { or } \\ \pm 22 \end{gathered}$ | 4.5 | 13* | 3.0 | 100 | 6.4 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 97 | 32 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14, } \\ \text { TSSOP-14 } \end{gathered}$ | High SR, Wide BW, Single Supply, *AV = -1.0 |
| MC33204 | $\begin{gathered} 1.8 \\ \text { or } \\ \pm 0.9 \end{gathered}$ | $\begin{aligned} & 12 \text { or } \\ & \pm 6.0 \end{aligned}$ | 2.2 | 1.0 | 10 | 200 | 3.2 | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 90 | 20 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14, } \\ \text { TSSOP-14 } \end{gathered}$ | Low Voltage, Rail-to-Rail |
| MC33204V | $\begin{gathered} 1.8 \\ \text { or } \\ \pm 0.9 \end{gathered}$ | $\begin{aligned} & 12 \text { or } \\ & \pm 6.0 \end{aligned}$ | 2.2 | 1.0 | 10 | 200 | 3.2 | $\begin{gathered} -55 \text { to } \\ +125 \end{gathered}$ | 90 | 20 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | Low Voltage, Rail-to-Rail, Extended Temp. Range |
| MC33174 | $\begin{gathered} 3.0 \\ \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{aligned} & 44 \text { or } \\ & \pm 22 \end{aligned}$ | 1.8 | 2.1 | 4.5 | 20 | 0.72 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 90 | 32 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | Low Power, Single Supply, Two voltage Ranges |
| MC33079 | $\pm 5.0$ | $\pm 18$ | 16 | 7.0 | 2.5 | 300 | 8.4 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 100 | 4.5 | 4 | Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | Low Noise |
| MC33179 | $\pm 2.0$ | $\pm 18$ | 5.0 | 2.0 | 3.0 | 100 | 1.7 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 110 | 7.5 | 4 | Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | High Output Current, Low Power, Low Noise |
| MC33274A | $\begin{gathered} 3.0 \\ \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 24 | 10 | $\begin{aligned} & 1 @ \mathrm{Vs}= \pm 15 \mathrm{~V} \\ & 2 @ \mathrm{Vs}=5.0 \mathrm{~V} \end{aligned}$ | 300 | $\begin{gathered} 4.3 @ \\ \mathrm{Vs}= \pm 15 \mathrm{~V} \end{gathered}$ | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 100 | 18 | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | Single Supply, High SR, Low Input Offset Voltage |

Quad Operational Amplifiers (continued)

| Device Name | $\mathrm{V}_{\mathrm{CC}}$ <br> (min) <br> (V) | $\begin{gathered} \mathrm{V}_{\mathrm{CC}} \\ (\max ) \\ (\mathrm{V}) \end{gathered}$ | GBW <br> (typ) <br> (MHz) | Slew <br> Rate <br> (typ) <br> (V/us) | $\begin{gathered} \mathrm{V}_{1 \mathrm{O}} \\ \left(\max @ 25^{\circ} \mathrm{C},\right. \\ \mathrm{Vs}=5.0 \mathrm{~V}) \\ (\mathrm{mV}) \end{gathered}$ | IIB (typ) (nA) | ID <br> (typ) <br> (mA) | Temp Range ( ${ }^{\circ} \mathrm{C}$ ) | CMR <br> (typ) <br> (dB) | $\mathbf{e n}_{n}$ (typical) $(\mathrm{nV} / \sqrt{\mathrm{Hz}})$ <br> @ $\mathrm{f}=1.0 \mathrm{kHz}$ | $\begin{aligned} & \text { Number } \\ & \text { of } \\ & \text { Channels } \end{aligned}$ | Supply Type | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LM324 | $\begin{gathered} 3.0 \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 32 \\ \pm 16 \end{gathered}$ | 1.0 | 0.6 | 7.0 | 90 | - | 0 to 70 | 70 | - | 4 | Single, Split | $\begin{gathered} \hline \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | Low Power |
| LM324A | $\begin{gathered} 3.0 \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 32 \\ \pm 16 \end{gathered}$ | 1.0 | 0.6 | 3.0 | 45 | 0.7 | 0 to 70 | 70 | - | 4 | Single, Split | $\begin{aligned} & \text { DIP-14, } \\ & \text { SO-14 } \end{aligned}$ | Low Power |
| LM224 | $\begin{gathered} 3.0 \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 32 \\ \pm 16 \end{gathered}$ | 1.0 | 0.6 | 5.0 | 90 | - | $\begin{gathered} -25 \text { to } \\ +85 \end{gathered}$ | 85 | - | 4 | Single, Split | $\begin{aligned} & \text { DIP-14, } \\ & \text { SO-14 } \end{aligned}$ | Low Power |
| LM2902 | $\begin{gathered} 3.0 \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 26 \\ \pm 13 \end{gathered}$ | 1.0 | 0.6 | 7.0 | 90 | - | $\begin{gathered} -40 \text { to } \\ +105 \end{gathered}$ | 70 | - | 4 | Single, Split | $\begin{gathered} \text { DIP-14, } \\ \text { SO-14 } \end{gathered}$ | Low Power |
| MC3403 | $\begin{gathered} 3.0 \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \\ \pm 18 \end{gathered}$ | 1.0 | 0.6 | 10 | 200 | 2.8 | 0 to 70 | 90 | - | 4 | Single, Split | $\begin{aligned} & \text { DIP-14, } \\ & \text { SO-14 } \end{aligned}$ | Low Power |
| MC3303 | $\begin{gathered} 3.0 \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \\ \pm 18 \end{gathered}$ | 1.0 | 0.6 | 8.0 | 200 | 2.8 | $\begin{gathered} -40 \text { to } \\ +85 \end{gathered}$ | 90 | - | 4 | Single, Split | $\begin{aligned} & \text { DIP-14, } \\ & \text { SO-14 } \end{aligned}$ | Low Power |



Single Comparators

| Device <br> Name | $\mathbf{V}_{\mathbf{C C}}$ <br> $(\mathrm{min})$ | $\mathbf{V}_{\mathbf{C C}}$ <br> $(\max )$ | $\mathbf{V}_{\mathbf{I O}}$ <br> $(\max )$ <br> $(\mathrm{mV})$ | lio <br> $(\max )$ <br> $(\mathrm{nA})$ | $\mathbf{l}_{\mathbf{I B}}$ <br> $(\mathrm{typ})$ <br> $(\mathrm{nA})$ | Iq <br> $($ typ $)$ <br> $(\mathrm{nA})$ | Temp <br> Range <br> $\left({ }^{\circ} \mathrm{C}\right)$ | Response <br> Time <br> $(\mathrm{ns})$ | Supply <br> Type | Number <br> of <br> Channels | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LM211 | 5.0 or <br> $\pm 2.5$ | 36 or <br> $\pm 15$ | 3.0 | 10 | 45 | 2.4 | -25 to +85 | 200 | Single <br> Split | 1 | SO-8 | Highly Flexible Voltage |
| LM311 | 5.0 or <br> $\pm 2.5$ | 36 or <br> $\pm 15$ | 7.5 | 50 | 45 | 2.4 | 0 to 70 | 200 | Single <br> Split | 1 | SO-8 <br> DIP-8 | Highly Flexible Voltage |

## Dual Comparators

| Device Name | $\mathrm{V}_{\mathrm{Cc}}$ <br> (min) | $\begin{aligned} & \mathbf{V}_{\mathrm{Cc}} \\ & (\max ) \end{aligned}$ | $V_{10}$ (max) (mV) | lio (max) (nA) | $I_{I B}$ (typ) <br> (nA) | Iq <br> (typ) <br> (nA) | Temp Range $\left({ }^{\circ} \mathrm{C}\right)$ | Response Time (ns) | Supply <br> Type | Number of Channels | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LM293 | $\begin{gathered} 2.0 \text { or } \\ \pm 1.0 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 5.0 | 50 | 25 | 0.4 | -25 to +85 | 1300 | Single Split | 2 | SO-8 | Low Offset Voltage |
| LM393 | $\begin{gathered} 2.0 \text { or } \\ \pm 1.0 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 5.0 | 50 | 25 | 0.4 | 0 to 70 | 1300 | Single Split | 2 | $\begin{aligned} & \text { SO-8 } \\ & \text { DIP-8 } \end{aligned}$ | Low Offset Voltage |
| LM2903 | $\begin{gathered} 2.0 \text { or } \\ \pm 1.0 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 7.0 | 50 | 25 | 0.4 | -40 to +105 | 1500 | Single Split | 2 | $\begin{aligned} & \text { SO-8 } \\ & \text { DIP-8 } \end{aligned}$ | Low Offset Voltage |
| LM2903V | $\begin{gathered} 2.0 \text { or } \\ \pm 1.0 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 7.0 | 50 | 25 | 0.4 | -40 to +125 | 1500 | Single Split | 2 | $\begin{aligned} & \text { SO-8 } \\ & \text { DIP-8 } \end{aligned}$ | Low Offset Voltage |

## Quad Comparators

| Device Name | $\begin{aligned} & \mathbf{V}_{\mathbf{C C}} \\ & (\mathrm{min}) \end{aligned}$ | $\begin{aligned} & \mathbf{V}_{\mathbf{C C}} \\ & (\max ) \end{aligned}$ | $\begin{gathered} \mathrm{V}_{\mathrm{IO}} \\ (\max ) \\ (\mathrm{mV}) \end{gathered}$ | lio (max) (nA) | IIB <br> (typ) <br> (nA) | Iq <br> (typ) <br> (nA) | Temp Range $\left({ }^{\circ} \mathrm{C}\right)$ | Response Time (ns) | Supply Type | Number of Channels | Package | Description |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| LM239 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 5.0 | 50 | 25 | 0.8 | -25 to +85 | 1300 | Single Split | 4 | $\begin{aligned} & \text { SO-14 } \\ & \text { DIP-14 } \end{aligned}$ | TTL and CMOS Compatible |
| LM339 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 5.0 | 50 | 25 | 0.8 | 0 to 70 | 1300 | Single Split | 4 | $\begin{aligned} & \text { SO-14 } \\ & \text { DIP-14 } \end{aligned}$ | TTL and CMOS Compatible |
| LM2901 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 7.0 | 50 | 25 | 0.8 | -40 to +105 | 1300 | Single Split | 4 | $\begin{aligned} & \text { SO-14 } \\ & \text { DIP-14 } \end{aligned}$ | TTL and CMOS Compatible |
| LM2901V | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 36 \text { or } \\ \pm 18 \end{gathered}$ | 7.0 | 50 | 25 | 0.8 | -40 to +125 | 1300 | Single Split | 4 | $\begin{aligned} & \text { SO-14 } \\ & \text { DIP-14 } \end{aligned}$ | TTL and CMOS Compatible |
| MC3302 | $\begin{gathered} 3.0 \text { or } \\ \pm 1.5 \end{gathered}$ | $\begin{gathered} 30 \text { or } \\ \pm 15 \end{gathered}$ | 20 | 100 | 25 | 0.8 | -40 to +85 | 1300 | Single Split | 4 | $\begin{aligned} & \text { SO-14 } \\ & \text { DIP-14 } \end{aligned}$ | TTL and CMOS Compatible |



For more information on analog switches, please see the Analog Switch Brochure, BRD8007/D available online at http://www.onsemi.com, or from the Literature Distribution Center. For ordering details see back cover.




General Purpose Buck Converters (For Non-Isolated Step-Down Application)

| $\mathrm{I}_{\text {out }}$ | Part No. | $\mathrm{V}_{\text {in }}$ | $\mathrm{V}_{\text {out }}$ | Frequency | Temp. Range ( ${ }^{\circ} \mathrm{C}$ ) | Control Method | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0.5 A | LM2574DW-ADJ | 4.75 to 40 V | 1.23 V to 37 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | SO-16 |
| 0.5 A | LM2574N-3.3 | 4.75 to 40 V | Fixed 3.3 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | DIP-8 |
| 0.5 A | LM2574N-5 | 7.0 to 40 V | Fixed 5.0 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | DIP-8 |
| 0.5 A | LM2574N-12 | 15 to 40 V | Fixed 12 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | DIP-8 |
| 0.5 A | LM2574N-15 | 18 to 40 V | Fixed 15 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | DIP-8 |
| 1.0 A | LM2575D2T-ADJ | 8.0 to 40 V | 1.23 V to 37 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | $\mathrm{D}^{2} \mathrm{PAK}$ |
| 1.0 A | LM2575T-ADJ | 8.0 to 40 V | 1.23 V to 37 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575TV-ADJ | 8.0 to 40 V | 1.23 V to 37 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575D2T-3.3 | 4.75 to 40 V | Fixed 3.3 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | D2PAK |
| 1.0 A | LM2575T-3.3 | 4.75 to 40 V | Fixed 3.3 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575TV-3.3 | 4.75 to 40 V | Fixed 3.3 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575D2T-5 | 8.0 to 40 V | Fixed 5.0 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | D2PAK |
| 1.0 A | LM2575T-5 | 8.0 to 40 V | Fixed 5.0 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575TV-5 | 8.0 to 40 V | Fixed 5.0 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575D2T-12 | 15 to 40 V | Fixed 12 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | D2PAK |
| 1.0 A | LM2575T-12 | 15 to 40 V | Fixed 12 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575TV-12 | 15 to 40 V | Fixed 12 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575D2T-15 | 18 to 40 V | Fixed 15 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | $\mathrm{D}^{2} \mathrm{PAK}$ |
| 1.0 A | LM2575T-15 | 18 to 40 V | Fixed 15 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 1.0 A | LM2575TV-15 | 18 to 40 V | Fixed 15 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576D2T-ADJ | 8.0 to 40 V | 1.23 V to 37 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | $\mathrm{D}^{2} \mathrm{PAK}$ |
| 3.0 A | LM2576T-ADJ | 8.0 to 40 V | 1.23 V to 37 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576TV-ADJ | 8.0 to 40 V | 1.23 V to 37 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576D2T-3.3 | 6.0 to 40 V | Fixed 3.3 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | D2PAK |
| 3.0 A | LM2576T-3.3 | 6.0 to 40 V | Fixed 3.3 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576TV-3.3 | 6.0 to 40 V | Fixed 3.3 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576D2T-5 | 8.0 to 40 V | Fixed 5.0 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | $\mathrm{D}^{2} \mathrm{PAK}$ |
| 3.0 A | LM2576T-5 | 8.0 to 40 V | Fixed 5.0 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576TV-5 | 8.0 to 40 V | Fixed 5.0 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | MC33166D2T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | D2PAK |

General Purpose Buck Converters (For Non-Isolated Step-Down Application) (continued)

| $\mathrm{I}_{\text {out }}$ | Part No. | $\mathrm{V}_{\text {in }}$ | $\mathrm{V}_{\text {out }}$ | Frequency | Temp. Range ( ${ }^{\circ} \mathrm{C}$ ) | Control Method | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 3.0 A | MC33166T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | TO-220 |
| 3.0 A | MC33166TH | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | TO-220 |
| 3.0 A | MC33166TV | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | TO-220 |
| 3.0 A | MC34166D2T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | D2PAK |
| 3.0 A | MC34166T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | TO-220 |
| 3.0 A | MC34166TH | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | TO-220 |
| 3.0 A | MC34166TV | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | TO-220 |
| 3.0 A | LM2576D2T-12 | 15 to 40 V | Fixed 12 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | D2PAK |
| 3.0 A | LM2576T-12 | 15 to 40 V | Fixed 12 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576TV-12 | 15 to 40 V | Fixed 12 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576D2T-15 | 18 to 40 V | Fixed 15 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | D2PAK |
| 3.0 A | LM2576T-15 | 18 to 40 V | Fixed 15 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 3.0 A | LM2576TV-15 | 18 to 40 V | Fixed 15 V | Fixed 52 kHz | -40 to +125 | Voltage Mode | TO-220 |
| 5.0 A | MC33167D2T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | D2PAK |
| 5.0 A | MC33167T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | TO-220 |
| 5.0 A | MC33167TH | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | TO-220 |
| 5.0 A | MC33167TV | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | -40 to +85 | Voltage Mode | TO-220 |
| 5.0 A | MC34167D2T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | D2PAK |
| 5.0 A | MC34167T | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | TO-220 |
| 5.0 A | MC34167TH | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | TO-220 |
| 5.0 A | MC34167TV | 7.5 to 40 V | $>5.0 \mathrm{~V}$ | Fixed 72 kHz | 0 to 70 | Voltage Mode | TO-220 |

General Purpose Buck Controllers (For Non-Isolated Step-Down Application)

| Peak output to MOSFET | Part No. | $\mathrm{V}_{\text {in }}$ | $\mathrm{V}_{\text {ref }}$ | Output Current | Frequency | Temp. Range ( ${ }^{\circ} \mathrm{C}$ ) | Control Method | Package | Remark |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1.0 A | CS51031YD8 | 4.5 to 16 V | 1.25 V | by External P MOSFET | max 700 kHz | -40 to +125 | Voltage Mode | SO-8 |  |
| 1.0 A | CS51031GD8 | 4.5 to 16 V | 1.25 V | by External P <br> MOSFET | $\max 700 \mathrm{kHz}$ | -40 to +125 | Voltage Mode | SO-8 |  |
| 1.0 A | CS51033YD8 | 3.3 V | 1.25 V | by External P <br> MOSFET | $\max 700 \mathrm{kHz}$ | -40 to +125 | Voltage Mode | SO-8 |  |
| 1.0 A | CS51033GD8 | 3.3 V | 1.25 V | by External P <br> MOSFET | $\max 700 \mathrm{kHz}$ | 0 to 70 | Voltage Mode | SO-8 |  |
|  | CS5211 |  |  |  |  |  |  |  |  |
| 1.5 A | NCP1570 | 11.4 V to 12.6 V | 0.985 V | by External N MOSFET | 200 kHz | 0 to 70 | $\mathrm{V}^{2 ®}$ Control | SO-8 |  |
|  | NCP5162 |  |  |  |  |  |  |  |  |
| - | CS51411E | 4.5 V to 40 V | 1.276 V | 1.5 A | 260 kHz | -40 to +85 | $\mathrm{V}^{2}$ Control | SO-8 | Synchronization Pin |
| - | CS51411G | 4.5 V to 40 V | 1.276 V | 1.5 A | 260 kHz | 0 to 70 | $\mathrm{V}^{2}$ Control | SO-8 | Synchronization Pin |
| - | CS51412E | 4.5 V to 40 V | 1.276 V | 1.5 A | 260 kHz | -40 to +85 | $\mathrm{V}^{2}$ Control | SO-8 | Bias Pin |
| - | CS51412G | 4.5 V to 40 V | 1.276 V | 1.5 A | 260 kHz | 0 to 70 | $V^{2}$ Control | SO-8 | Bias Pin |
| - | CS51413E | 4.5 V to 40 V | 1.276 V | 1.5 A | 520 kHz | -40 to +85 | $\mathrm{V}^{2}$ Control | SO-8 | Synchronization Pin |
| - | CS51413G | 4.5 V to 40 V | 1.276 V | 1.5 A | 520 kHz | 0 to 70 | $\mathrm{V}^{2}$ Control | SO-8 | Synchronization Pin |
| - | CS51414E | 4.5 V to 40 V | 1.276 V | 1.5 A | 520 kHz | -40 to +85 | $V^{2}$ Control | SO-8 | Bias Pin |
| - | CS51414G | 4.5 V to 40 V | 1.276 V | 1.5 A | 520 kHz | 0 to 70 | V2 Control | SO-8 | Bias Pin |

General Purpose Boost Converters (For Non-Isolated Step-Up Applications) (Can also be configured for Boost, Flyback, Forward)

| Internal Switch | Part No. | $\mathrm{V}_{\text {in }}$ | $\mathrm{V}_{\text {out }}$ | Frequency | Temp. Range <br> $\left({ }^{\circ} \mathrm{C}\right)$ | Package | Remark |
| :---: | :---: | :---: | :---: | :--- | :---: | :---: | :---: |
| 1.5 A | CS5171ED8 | 2.7 V to 30 V | Programmable | Fixed 280 kHz | -40 to +85 | SO-8 |  |
| 1.5 A | CS5171GD8 | 2.7 V to 30 V | Programmable | Fixed 280 kHz | 0 to 70 | SO-8 |  |
| 1.5 A | CS5172ED8 | 2.7 V to 30 V | Programmable | Fixed 280 kHz | -40 to +85 | SO-8 | Negative Feedback of CS5171 |
| 1.5 A | CS5172GD8 | 2.7 V to 30 V | Programmable | Fixed 280 kHz | 0 to 70 | SO-8 | Negative Feedback of CS5171 |
| 1.5 A | CS5173ED8 | 2.7 V to 30 V | Programmable | Fixed 560 kHz | -40 to +85 | SO-8 |  |
| 1.5 A | CS5173GD8 | 2.7 V to 30 V | Programmable | Fixed 560 kHz | 0 to 70 | SO-8 |  |
| 1.5 A | CS5174ED8 | 2.7 V to 30 V | Programmable | Fixed 560 kHz | -40 to +85 | SO-8 | Negative Feedback of CS5173 |
| 1.5 A | CS5174GD8 | 2.7 V to 30 V | Programmable | Fixed 560 kHz | 0 to 70 | SO-8 | Negative Feedback of CS5173 |

DC-DC Boost Converters (For Non-Isolated Step-Up Applications)

| $V_{\text {in }}$ | Part No. | $\mathrm{V}_{\text {out }}$ | Switch | Frequency | Temp. Range ( ${ }^{\circ} \mathrm{C}$ ) | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0.9 to 8.0 V | MC33466H-30LT1 | Fixed 3 V | External | Fixed 100 kHz | -30 to +80 | SOT-89 |
|  | MC33463H-30LT1 |  |  | VFM around 100 kHz |  |  |
|  | MC33466H-30JT1 |  | Internal | Fixed 50 kHz |  |  |
|  | MC33463H-30KT1 |  |  | VFM around 100 kHz |  |  |
|  | MC33466H-33LT1 | Fixed 3.3 V | External | Fixed 100 kHz |  |  |
|  | MC33463H-33LT1 |  |  | VFM around 100 kHz |  |  |
|  | MC33466H-33JT1 |  | Internal | Fixed 50 kHz |  |  |
|  | MC33463H-33KT1 |  |  | VFM around 100 kHz |  |  |
|  | MC33466H-50LT1 | Fixed 5 V | External | Fixed 100 kHz |  |  |
|  | MC33463H-50LT1 |  |  | VFM around 100 kHz |  |  |
|  | MC33466H-50JT1 |  | Internal | Fixed 50 kHz |  |  |
|  | MC33463H-50KT1 |  |  | VFM around 100 kHz |  |  |



## Charge Pump Converters

| Output Current <br> $($ Typ mA$)$ | Part No. | Output Voltage | Input Voltage <br> Range $(\mathrm{V})$ | Oscillator <br> Frequency <br> $(\mathrm{kHz})$ | Quiescent Supply <br> Current ${ }^{\star}\left(\right.$ Max $\left.\mu \mathrm{A} @ 25^{\circ} \mathrm{C}\right)$ | Package | Features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 25 | MAX828 | $\mathrm{V}_{\text {out }}=-\mathrm{V}_{\text {in }}$ or $\mathrm{V}_{\text {out }}=2 \mathrm{~V}_{\text {in }}$ | $1.5 \rightarrow 5.5$ | $10 / 35$ | 90 | SOT-23-5 |  |
| 25 | MAX829 | $\mathrm{V}_{\text {out }}=-\mathrm{V}_{\text {in }}$ or $\mathrm{V}_{\text {out }}=2 \mathrm{~V}_{\text {in }}$ | $1.5 \rightarrow 5.5$ | 12 | 260 | SOT-23-5 |  |
| 25 | MAX1720 | $\mathrm{V}_{\text {out }}=-\mathrm{V}_{\text {in }}$ or $\mathrm{V}_{\text {out }}=2 \mathrm{~V}_{\text {in }}$ | $1.5 \rightarrow 5.5$ | 35 | 90 | TSOP-6 | with Enable |

*Measured at $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ at $25^{\circ} \mathrm{C}$ and no load.



Enhanced Current-Mode PWM Controller

| Part No. | Package | Features | Application |
| :---: | :---: | :---: | :---: |
| CS51021AED16 | 16L SO Narrow | - 75 uA Max. Startup Current (Comparing to $0.5 \sim 1 \mathrm{~mA}$ in UC384X) <br> - Fixed Frequency Current-Mode Control up to 1 MHz ( 500 kHz in UC384X) <br> - Input Voltage Monitor (Under/Over) <br> - Programmable Dual Threshold Current Sense for OCP (Fast and Slow) <br> - LEB (55 ns) Current Sense <br> - Programmable Slope Compensation <br> - Adjustable Soft Start <br> - Programmable Maximum Duty Cycle <br> - Sleep (CS51022/51024)/Bi-directional Sync (CS51021/51023) Options <br> - UVLO Options: (8.25/7.7 V) for CS51021/22/(13/7.7 V) for CS51023/24 <br> - Operating Junction Temperature Range $-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ <br> - 50 ns Shutdown Propagation Delay <br> - 1 A FET Driver | More Programmable and Enhanced Features to Replace the General Market of UC384X |
| CS51022AED16 |  |  |  |
| CS51023AED16 |  |  |  |
| CS51024AED16 |  |  |  |

Enhanced Voltage-Mode PWM Controller

| Part No. | Package | Features | Application |
| :---: | :---: | :---: | :---: |
| CS51227ED8 | 8L SO Narrow | - Fixed Frequency Voltage Mode Control with Feedforward <br> - Programmable Volt-Second Clamp <br> - Programmable Frequency (up to 1 MHx ) <br> - 1 A FET Driving Capability <br> - Thermal Shutdown <br> - $75 \mu \mathrm{~A}$, Maximum Startup Current <br> - 150 ns LEB for Over Current Protection <br> - Operate from 5 V Supply - 4.6 V UVLO | DC/DC Converter to have Simple Solution with Feedforward Control Function in a Small SO-8 Package |
| CS51221ED16 CS51221EN16 | 16L SO Narrow | - With Enhanced Features in Addition to CS51227 <br> - Bi-directional Synchronization <br> - 3.3 V Reference Voltage Output <br> - Programmable Under and Overvoltage Monitor <br> - Programmable Soft Start <br> - Hiccup Mode Fault Timing | When more Control Features and Flexibility are wanted |

Synchronous Rectification PWM Controller with Auxiliary Output

| Part No. | Package | Features | Application |
| :---: | :---: | :---: | :---: |
| CS5106LSW24 | 24 Lead SSOP | - Integrated Bootstrap Controller <br> - Synchronous Drivers with Programmable Non-Overlap Time for Main Output <br> - Input OVLO/UVLO <br> - Output Undervoltage Protection with Timer <br> - Under and Overvoltage Shutdown <br> - Enable Lead <br> - Master/Slave Clock Synchronous Frequency Range Detect $+25 \%,-35 \%$ <br> - 20 mA 5 V Reference Output <br> - $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ Operating Temperature Range <br> - Auxiliary Drive for Output | Full-Featured High Power Isolated DC/DC Converter with 2 Outputs |

Highly Integrated PWM Current-Mode Controller

\begin{tabular}{|c|c|c|c|}
\hline Part No. \& Package \& Features \& Application <br>
\hline CS5124XD8

CS5126XD8 \& 8L SO Narrow \& | - Input UVLO |
| :--- |
| - Direct Optocoupler Interface |
| - Soft-Start Capacitor Pin |
| - LEB (Leading Edge Blanking) for Current Sense (130 ns) |
| - $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ Operating Junction Temperature Range |
| - Thermal Shutdown |
| - Sleep Mode On/Off Pin |
| - CS5124 is 400 kHz with Bias Pin for Startup Circuitry, 195 mV First Current Sense Threshold for Resistor Current Sensing |
| - CS5126 is 200 kHz with Sync Pin, 330 mV First Current Sense Threshold for Current Sense Transformer | \& Compact Sub 50 W Isolated DC/DC Flyback <br>

\hline
\end{tabular}

PWM: Pulse Width Modulation
PFM: Pulse Frequency Modulation
VFM: Variable Frequency Modulation


Off-Line Controllers (with High Voltage Start-up Circuit)


PWM: Pulse Width Modulation
PFM: Pulse Frequency Modulation VFM: Variable Frequency Modulation


MC33363/A/B
MC33365
MC33362
NCP1000
NCP1001
NCP1002
NCP1050
NCP1051
NCP1052
NCP1053
NCP1054
NCP1055

## Very High Voltage Off-Line Switching Regulators with On-Chip Power Switch

This monolithic high voltage switching regulator is specifically designed to operate from a rectified ac line voltage source. Included are an on-chip high voltage power switch, active off-line startup circuitry and a full featured PWM controller with fault protection.

|  |  |  |  |  |  |  |  | $\begin{aligned} & \overline{0} \text { o } \\ & \text { 능 } \\ & \text { OU } \end{aligned}$ |  | $\begin{aligned} & \mathbb{O} \\ & \text { O} \\ & \text { Ö } \\ & 0 \end{aligned}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MC33362 | 120 VAC Operation | Yes | 500 V | 0.9 A | $4.4 \Omega$ | 20 W | Active On-Chip 250 V FET | - PWM, Fixed Frequency <br> Voltage Mode | $\begin{aligned} & \text { Adjustable } \\ & \text { up to } \\ & 300 \mathrm{kHz} \end{aligned}$ | $\begin{gathered} \text { DIP-16 } \\ \text { SO-16WB } \end{gathered}$ | $\begin{gathered} -25 \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  |
| MC33363A | Yes | Yes | 700 V | 0.9 A | $7.5 \Omega$ | 14 W | Active On-Chip 500 V FET | - PWM, Fixed Frequency <br> Voltage Mode | $\begin{aligned} & \text { Adjustable } \\ & \text { up to } \\ & 300 \mathrm{kHz} \end{aligned}$ | $\begin{aligned} & \text { DIP-16 } \\ & \text { SO-16WB } \end{aligned}$ | $\begin{gathered} -25 \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  |
| MC33363B | Yes | Yes | 700 V | 0.72 A | $15 \Omega$ | 8.0 W | Active On-Chip 450 V FET | - PWM, Fixed Frequency <br> Voltage Mode | Adjustable up to 300 kHz | $\begin{gathered} \text { DIP-16 } \\ \text { SO-16WB } \end{gathered}$ | $\begin{gathered} -25 \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  |
| MC33365 | Yes | Yes | 700 V | 0.72 A | $15 \Omega$ | 8.0 W | Active On-Chip 450 V FET | - PWM, Fixed Frequency <br> - Voltage Mode | Adjustable up to 300 kHz | $\begin{aligned} & \text { DIP-16 } \\ & \text { SO-16WB } \end{aligned}$ | $\begin{gathered} -25 \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ | Bulk Capacitor Voltage Sensing Capability to Sense an AC Line Brown-Out |

NOTE: Typical output power is dependent upon line voltage range, heatsinking and ambient temperature.


## Power Factor Controllers

| Device | Operating Modes | Switching Frequency | Features | Voltage Reference | Maximum <br> Input <br> Voltage | Temp Range | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MC33260 | - Voltage Mode <br> - Follower Boost or Fixed Output <br> - Critical Conduction Mode | Free to 500 kHz Fixed Clamp | - Synchronization Capability <br> - Output Current Sense <br> - Output Overvoltage Detect <br> - Input Undervoltage Lockout <br> - Maximum On time Limit | None | 16 V | $-40^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$ | $\begin{aligned} & \hline \text { PDIP-8 } \\ & \text { SOIC-8 } \end{aligned}$ |
| MC33262 | - Current Mode <br> - Fixed Output Voltage <br> - Critical Conduction Mode | Free, no Frequency Clamp | - Output Current Sense <br> - Output Overvoltage Detect <br> - Input Undervoltage Lockout <br> - Zero Current Detect | $2.5 \mathrm{~V}+/-1.4 \%$ | 30 V | $-40^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$ | $\begin{aligned} & \hline \text { PDIP-8 } \\ & \text { SOIC-8 } \end{aligned}$ |
| MC34262 | - Current Mode <br> - Fixed Output Voltage <br> - Critical Conduction Mode | Free, no Frequency Clamp | - Output Current Sense <br> - Output Overvoltage Detect <br> - Input Undervoltage Lockout <br> - Zero Current Detect | $2.5 \mathrm{~V}+/-1.4 \%$ | 30 V | $0^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | PDIP-8 <br> SOIC-8 |
| MC33368 | - Current Mode <br> - Fixed Output Voltage <br> - Critical Conduction Mode | Free, <br> Programmable Frequency Clamp | - True Off-line Start-Up <br> - Output Current Sense <br> - Output Overvoltage Detect <br> - Input Undervoltage Lockout <br> - Zero Current Detect | 5.0 V +/- 1.5\% | 500 V | $-25^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | SOIC-16 |



## Series Voltage References

| Part Number | Reference Voltage <br> (V) | Tolerance +/(\%) | Typical Temperature Coefficient (ppm/ ${ }^{\circ} \mathrm{C}$ ) | Typical Quiescent Current (mA) | Package |  | Operating Temperature Range ( ${ }^{\circ} \mathrm{C}$ ) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | $\begin{aligned} & \infty \\ & 0 \\ & \hline \end{aligned}$ | $\frac{\mathbf{1}}{\mathbf{0}}$ |  |
| MC1403 | 2.500 | 1.0 | 10 | 1.200 | $\checkmark$ | $\checkmark$ | 0 to +70 |
| MC1403B | 2.500 | 1.0 | 10 | 1.200 | $\checkmark$ | $\checkmark$ | -40 to +85 |

## Shunt Voltage References

| Part Number | Reference Voltage <br> (V) | Tolerance +/- <br> (\%) | Typical Temperature Coefficient (ppm/ ${ }^{\circ} \mathrm{C}$ ) | Minimum Operating Current (mA) | Package |  |  |  |  | Operating Temperature Range ( ${ }^{\circ} \mathrm{C}$ ) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | $\begin{aligned} & \infty \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \text { N } \\ & 1 \\ & 1 \\ & \hline 1 \end{aligned}$ |  | $\begin{aligned} & \text { Lp } \\ & 0 \\ & 0 \\ & 0 \\ & \bullet \end{aligned}$ | $\frac{\square}{\mathbf{O}}$ |  |
| LM285-1.2 | 1.235 | 1.0 | 80 | 0.010 | $\checkmark$ | $\checkmark$ |  |  |  | -40 to +85 |
| LM385-1.2 | 1.235 | 2.0 | 80 | 0.015 | $\checkmark$ | $\checkmark$ |  |  |  | 0 to +70 |
| LM285-2.5 | 2.500 | 1.5 | 80 | 0.020 | $\checkmark$ | $\checkmark$ |  |  |  | 0 to +70 |
| LM385-2.5 | 2.500 | 3.0 | 80 | 0.020 | $\checkmark$ | $\checkmark$ |  |  |  | 0 to +70 |
| LM385B-1.2 | 1.235 | 1.0 | 80 | 0.020 | $\checkmark$ | $\checkmark$ |  |  |  | 0 to +70 |
| LM385B-2.5 | 2.500 | 1.5 | 80 | 0.020 | $\checkmark$ | $\checkmark$ |  |  |  | 0 to +70 |
| CS1009 | 2.500 | 0.2 | - | - | $\checkmark$ | $\checkmark$ |  |  |  | -40 to +105 |
| NCP100 | Adjustable 0.9 to 6 V | 1.0 | 25 | 0.100 |  |  |  | $\checkmark$ |  | -40 to +85 |
| TLV431A | Adjustable 1.24 to 16 V | 1.0 | - | 0.050 |  | $\checkmark$ |  | $\checkmark$ |  | -40 to +85 |
| TL431C | Adjustable 2.495 to 36 V | 2.2 | 50 | 0.500 | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 0 to +70 |
| TL431I | Adjustable 2.495 to 36 V | 2.2 | 50 | 0.500 | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | -40 to +85 |
| TL431AC | Adjustable 2.495 to 36 V | 1.0 | 50 | 0.500 | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 0 to +70 |
| TL431AI | Adjustable 2.495 to 36 V | 1.0 | 50 | 0.500 | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | -40 to +85 |
| TL431BC | Adjustable 2.495 to 36 V | 0.4 | 50 | 0.500 | $\checkmark$ | $\sqrt{ }$ | $\checkmark$ |  | $\checkmark$ | 0 to +70 |
| TL431BI | Adjustable 2.495 to 36 V | 0.4 | 50 | 0.500 | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | -40 to +85 |



General Purpose Linear Voltage Regulators

|  |  | Nominal Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Package |  |  |  |  |  | Automotive Temperature Rating Available ( -40 to $+125^{\circ} \mathrm{C}$ ) |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number | $\begin{array}{\|l} 0 \\ \stackrel{0}{3} \\ 0 \\ 0 \\ 0 \end{array}$ |  |  | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & i \circ \end{aligned}\right.$ | $\left\|\begin{array}{c} \text { N } \\ \text { in } \end{array}\right\|$ | $$ | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & \infty \\ & \infty \end{aligned}\right.$ | $\begin{aligned} & > \\ & 0 \\ & 0 \\ & \sigma^{\prime} \end{aligned}$ | $\begin{aligned} & > \\ & \mathbf{O} \\ & \underset{\sim}{\dot{N}} \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & \\ & \end{aligned}\right.$ | $\begin{aligned} & > \\ & 0 \\ & \underset{\infty}{0} \\ & \hline \end{aligned}$ | $\begin{aligned} & > \\ & \text { O} \\ & \text { ลㅅ } \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & \text { O } \\ & \text { N } \end{aligned}\right.$ |  | Drop Out Voltage (Typical) | Maximum Input Voltage (Vdc) | $\left\lvert\, \begin{aligned} & \infty \\ & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \end{aligned}\right.$ | \|늠 | ¢ | $\underset{\substack{\underset{\sim}{N} \\ \underset{\sim}{1} \\ \hline}}{ }$ | $\left\|\begin{array}{c} \mathfrak{N} \\ \mathbf{1} \\ \mathbf{O} \\ 1 \end{array}\right\|$ | $\begin{array}{\|c} \mathbf{N} \\ \text { Ni } \\ \text { O} \end{array}$ |  | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & 0 \end{aligned}\right.$ | $\left\lvert\, \begin{gathered} \underset{~ N}{N} \\ \text { Ni } \end{gathered}\right.$ | $\begin{aligned} & > \\ & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & > \\ & 0 \\ & \infty \\ & \infty \end{aligned}$ | $\begin{aligned} & > \\ & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & > \\ & \mathbf{O} \\ & \underset{\sim}{\mathrm{N}} \end{aligned}$ | $\begin{array}{\|c} > \\ 0 \\ \stackrel{0}{n} \\ \end{array}$ | $\begin{aligned} & > \\ & \mathbf{o} \\ & \underset{\sim}{\infty} \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & \text { ò } \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & > \\ & \text { O} \\ & \text { N் } \end{aligned}\right.$ |
| 100 mA | MC78LxxA <br> Series | $\checkmark$ |  |  | $\checkmark$ |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 5.0 | $\begin{gathered} 1.7 \mathrm{~V} @ \\ 40 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} 5.0 \text { to } 18 \mathrm{~V} \text { Version }=30 \mathrm{~V} \\ 12 \text { to } 18 \mathrm{~V} \text { Version }=35 \mathrm{~V} \\ 24 \mathrm{~V} \text { Version }=40 \mathrm{~V} \end{gathered}$ | $\checkmark$ |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  | $\checkmark$ | $\begin{aligned} & \hline \sqrt{ } \\ & 1 . \end{aligned}$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ |
| 100 mA | MC79LxxA Series |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 5.0 | $\begin{gathered} 1.7 \mathrm{~V} @ \\ 40 \mathrm{~mA} \end{gathered}$ | $\begin{gathered} -5.0 \mathrm{~V} \text { Version }=-30 \mathrm{~V} \\ -12 \text { to }-18 \mathrm{~V} \text { Version }=-35 \mathrm{~V} \\ -24 \mathrm{~V} \text { Version }=-40 \mathrm{~V} \end{gathered}$ | $\checkmark$ |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  |  | $\checkmark$ | $\checkmark$ |  |  |  |
| 100 mA | LM317Lxx Series | $\checkmark$ |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  | 4.0 | $\begin{aligned} & 1.9 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}$ | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |
| 500 mA | MC78Mxx Series | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 4.0 | $\begin{aligned} & 1.9 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | 5.0 to 18 V Version $=35 \mathrm{~V}$ <br> 20 to 24 V Version $=40 \mathrm{~V}$ |  | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ |  | $\begin{aligned} & \sqrt{ } \\ & 1 . \end{aligned}$ | $\sqrt{ }$ | $\begin{aligned} & \sqrt{ } \\ & 1 . \end{aligned}$ | $\left\lvert\, \begin{aligned} & \sqrt{ } \\ & 1 \end{aligned}\right.$ | $\checkmark$ | $\begin{aligned} & \sqrt{ } \\ & 1 . \end{aligned}$ |  | V 1. |
| 500 mA | MC78MxxA Series | $\checkmark$ |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  |  | 2.0 | $\begin{aligned} & 1.9 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | 5.0 to 18 V Version $=35 \mathrm{~V}$ <br> 20 to 24 V Version $=40 \mathrm{~V}$ |  | $\checkmark$ |  |  |  | $\checkmark$ |  |  |  | $\checkmark$ | $\sqrt{ }$ | $\checkmark$ | $\sqrt{ }$ |  |  |  |  |
| 500 mA | MC79Mxx Series |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  |  | 4.0 | $\begin{aligned} & 1.1 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | -35 V |  | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  |  |
| 500 mA | LM317Mxx Series | $\checkmark$ |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  | 4.0 | $\begin{aligned} & 2.1 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}$ |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |
| 500 mA | LM317MxxA Series | $\checkmark$ |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  | 2.0 | $\begin{aligned} & 2.1 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}$ |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |
| 1.5 A | MC78xx <br> Series | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\sqrt{ }$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 4.0 | $\begin{aligned} & 2.0 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | 5.0 to 18 V Version $=35 \mathrm{~V}$ <br> 24 V Version $=40 \mathrm{~V}$ |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\sqrt{ }$ | $\begin{aligned} & \sqrt{ } \\ & 1 . \end{aligned}$ | $\sqrt{ }$ | $\checkmark$ | $\begin{aligned} & \sqrt{ } \\ & 1 . \end{aligned}$ |  | $\checkmark$ |
| 1.5 A | MC78xxA <br> Series | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 2.0 | $\begin{aligned} & 2.0 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | 5.0 to 18 V Version $=35 \mathrm{~V}$ <br> 24 V Version $=40 \mathrm{~V}$ |  |  | $\begin{aligned} & \sqrt{ } \\ & 2 . \end{aligned}$ |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |

xx' indicates nominal voltage

1. Available in select packages only; contact your local ON Semiconductor sales office for information.
2. Available for select voltage options only; contact your local ON Semiconductor sales office for information.

General Purpose Linear Voltage Regulators（continued）

|  |  | Nominal Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Pac | kage |  |  | Automotive Temperature Rating Available（ -40 to $+125^{\circ} \mathrm{C}$ ） |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part <br> Number |  |  |  | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & i 0 \end{aligned}\right.$ | $\left\|\begin{array}{c} \text { N } \\ \stackrel{N}{n} \end{array}\right\|$ | $\left\|\begin{array}{l} > \\ 0 \\ 0 \\ 0 \end{array}\right\|$ | $\left\|\begin{array}{l} > \\ 0 \\ \infty \\ \infty \end{array}\right\|$ | $\begin{aligned} & > \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\left\|\begin{array}{l} > \\ 0 \\ \stackrel{\rightharpoonup}{\mathrm{~N}} \end{array}\right\|$ | $\left\|\begin{array}{l} > \\ 0 \\ 10 \\ \hline \end{array}\right\|$ | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & \infty \\ & \infty \end{aligned}\right.$ | $\begin{aligned} & > \\ & \text { o } \\ & \text { 人̀ } \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & \text { ò } \\ & \underset{\sim}{\prime} \end{aligned}\right.$ | $\begin{aligned} & \begin{array}{l} 0 \\ 0 \\ \frac{\pi}{0} \\ \frac{0}{0} \\ \hline 0 \\ \hline- \end{array} \\ & \hline 1 \end{aligned}$ | Drop Out Voltage （Typical） | Maximum Input Voltage（Vdc） | $\left\lvert\, \begin{aligned} & \infty \\ & 1 \\ & 0 \\ & 0 \\ & 0 \end{aligned}\right.$ | 咎 | ¢ | $\underset{N}{N}$ | $\left\lvert\, \begin{aligned} & \mathrm{N} \\ & \mathbf{1} \\ & \mathbf{O} \\ & 1 \end{aligned}\right.$ | $\begin{array}{\|c} \mathbf{N} \\ \text { N } \\ \text { IO } \end{array}$ |  | $\begin{aligned} & \mathbf{c} \\ & 0 \\ & \mathbf{i} \end{aligned}$ | $\underset{\substack{\lambda \\ \stackrel{~}{n}}}{ }$ | $\begin{aligned} & > \\ & 0 \\ & 0 \\ & \hline \end{aligned}$ | $\left\|\begin{array}{l} > \\ 0 \\ \infty \\ \infty \end{array}\right\|$ | $\begin{array}{\|l} > \\ 0 \\ \sigma^{\prime} \end{array}$ | $\left\|\begin{array}{l} > \\ \mathbf{O} \\ \stackrel{\rightharpoonup}{\mathrm{N}} \end{array}\right\|$ | $\begin{array}{\|l} > \\ 0 \\ \stackrel{0}{n} \\ \stackrel{1}{2} \end{array}$ | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & \infty \\ & \infty \end{aligned}\right.$ | $\begin{aligned} & > \\ & \text { o } \\ & \text { 人̀ } \end{aligned}$ | － |
| 1.5 A | LM340－xx Series | $\checkmark$ |  |  | $\checkmark$ |  |  |  |  | $\checkmark$ | $\checkmark$ |  |  |  | 4.0 | $\begin{gathered} 1.75 \mathrm{~V} @ \\ 1.0 \mathrm{~A} \end{gathered}$ | 35 V |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |
| 1.5 A | LM340A-xx <br> Series | $\checkmark$ |  |  | $\checkmark$ |  |  |  |  | $\checkmark$ | $\sqrt{ }$ |  |  |  | 2.0 | $\begin{gathered} 1.75 \mathrm{~V} @ \\ 1.0 \mathrm{~A} \end{gathered}$ | 35 V |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |
| 1.5 A | MC79xx <br> Series |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\sqrt{ }$ |  | $\checkmark$ | $\sqrt{ }$ | $\sqrt{ }$ |  | $\checkmark$ | 4.0 | $\begin{gathered} 2.0 \text { V @ } \\ 1.0 \text { A } \end{gathered}$ | $\begin{gathered} -5.0 \text { to }-18 \mathrm{~V} \text { Version }=-35 \mathrm{~V} \\ -24 \mathrm{~V} \text { Version }=-40 \mathrm{~V} \end{gathered}$ |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\sqrt{ }$ |  |  |  |  | $3 .$ | $\checkmark$ |  |  | V 3. |
| 1.5 A | MC79xxA Series |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  | $\sqrt{ }$ | $\checkmark$ |  |  |  | 2.0 | $\begin{gathered} 2.0 \mathrm{~V} @ \\ 1.0 \mathrm{~A} \end{gathered}$ | $\begin{gathered} -5.0 \text { to }-18 \mathrm{~V} \text { Version }=-35 \mathrm{~V} \\ -24 \mathrm{~V} \text { Version }=-40 \mathrm{~V} \end{gathered}$ |  |  | $4$ |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |
| 1.5 A | LM317 | $\checkmark$ |  | $\sqrt{ }$ |  |  |  |  |  |  |  |  |  |  | 4.0 | $\begin{aligned} & 2.25 \mathrm{~V} \text { @ } \\ & 1.5 \mathrm{~A} \end{aligned}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}$ |  |  | $\checkmark$ |  |  | $\checkmark$ | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |
| 1.5 A | LM337 |  | $\checkmark$ | $\checkmark$ |  |  |  |  |  |  |  |  |  |  | 4.0 | $\begin{gathered} 2.2 \mathrm{~V} @ \\ 1.5 \mathrm{~A} \end{gathered}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}$ |  |  | $\checkmark$ |  |  | $\checkmark$ | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |
| 3．0 A | LM323 | $\checkmark$ |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  | 4.0 | $\begin{gathered} 2.0 \text { V @ } \\ 3.0 \text { A } \end{gathered}$ | 20 V |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |
| 3.0 A | LM323A | $\checkmark$ |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  | 2.0 | $\begin{gathered} 2.0 \text { V @ } \\ 3.0 \text { A } \end{gathered}$ | 20 V |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |
| 3.0 A | LM350 | $\checkmark$ |  | $\sqrt{ }$ |  |  |  |  |  |  |  |  |  |  | 4.0 | $\begin{gathered} 2.7 \text { V @ } \\ 3.0 \text { A } \end{gathered}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=35 \mathrm{~V}$ |  |  |  |  |  | $\checkmark$ | $\sqrt{ }$ |  |  |  |  |  |  |  |  |  |  |
| 3.0 A | MC78Txx <br> Series | $\checkmark$ |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ | $\sqrt{ }$ |  |  |  | 4.0 | $\begin{gathered} \text { 2.2 V @ } \\ 3.0 \text { A } \end{gathered}$ | $\begin{gathered} 5.0 \text { to } 12 \mathrm{~V} \text { Version }=35 \mathrm{~V} \\ 15 \mathrm{~V} \text { Version }=40 \mathrm{~V} \end{gathered}$ |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  | $\checkmark$ |  |  |  |  |
| 3.0 A | MC78TxxA Series | $\checkmark$ |  |  | $\checkmark$ |  |  |  |  | $\checkmark$ | $\sqrt{ }$ |  |  |  | 2.0 | $\begin{gathered} \text { 2.2 V @ } \\ 3.0 \text { A } \end{gathered}$ | $\begin{gathered} 5.0 \text { to } 12 \mathrm{~V} \text { Version }=35 \mathrm{~V} \\ 15 \mathrm{~V} \text { Version }=40 \mathrm{~V} \end{gathered}$ |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  | $\checkmark$ | $\checkmark$ |  |  |  |

＇xx＇indicates nominal voltage
3．Available in select packages only；contact your local ON Semiconductor sales office for information．
4．Available for select voltage options only；contact your local ON Semiconductor sales office for information．



Low Dropout Voltage Regulators

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  |  | $\left\|\begin{array}{l} > \\ \infty \\ \stackrel{\infty}{r} \end{array}\right\|$ | $\begin{aligned} & > \\ & \text { in } \end{aligned}$ | $\left\|\begin{array}{l} \vec{\lambda} \\ \vec{N} \end{array}\right\|$ | $\left\lvert\, \begin{aligned} & > \\ & \infty \\ & \underset{\sim}{n} \end{aligned}\right.$ | $\left\|\begin{array}{l\|} > \\ \mathscr{\infty} \\ \underset{\sim}{\infty} \\ \mid \end{array}\right\|$ | $\begin{aligned} & > \\ & \text { o } \\ & \text { ल } \end{aligned}$ | $\begin{aligned} & > \\ & \mathbf{N} \\ & \text { ले } \end{aligned}$ | $\begin{aligned} & > \\ & \infty \\ & \infty \\ & \text { c. } \end{aligned}$ | $\left.\begin{array}{l} > \\ \infty \\ \dot{\infty} \end{array}\right\rangle$ |  | $$ |  | 웅 |  |  | Drop Out Voltage | Min. | Max. |  |  |  |  |  |  |  | $0$ |  | Additional Features |
| - | MC78BCxx |  |  |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  | 5. | 2.5 | $\begin{aligned} & 0.1 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | - | 10 | $\checkmark$ |  |  |  |  |  |  |  |  | External Power Transistor |
| 80 mA | MC33761 |  |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 0.16 \mathrm{~V} @ \\ 80 \mathrm{~mA} \end{gathered}$ | - | 12 | $\checkmark$ |  |  |  |  |  |  |  |  | w/ ENABLE, Ultra Low Noise |
| 80 mA | MC78LCxx |  |  |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  | 5. | 2.5 | $\begin{gathered} 0.22 \mathrm{~V} @ \\ 10 \mathrm{~mA} \end{gathered}$ | - | 10 | $\sqrt{ }$ | $\checkmark$ |  |  |  |  |  |  |  | Very Low Quiescent Current |
| $\begin{gathered} 80 \mathrm{~mA}, \\ 80 \mathrm{~mA} \end{gathered}$ | MC33762 |  |  |  | $\begin{aligned} & \sqrt{ } \\ & \sqrt{2} \end{aligned}$ |  | $\begin{aligned} & \sqrt{ } \\ & \sqrt{2} \end{aligned}$ |  | $\begin{aligned} & \sqrt{ } \\ & \sqrt{2} \end{aligned}$ |  |  |  |  |  |  |  |  | - | $\begin{gathered} 0.16 \mathrm{~V} @ \\ 80 \mathrm{~mA}, \\ 0.16 \mathrm{~V} @ \\ 80 \mathrm{~mA} \end{gathered}$ | - | 12 |  |  |  | $\checkmark$ |  |  |  |  |  | Dual, w/ ENABLE, Ultra Low Noise |
| 80 mA | NCP512* |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 2.5 | $\begin{gathered} 250 \mathrm{mV} @ \\ 80 \mathrm{~mA} \end{gathered}$ | - | 6.0 | $\checkmark$ |  |  |  |  |  |  |  |  | w/ ENABLE |
| 80 mA | NCP552* |  | $\sqrt{ }$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 2.5 | $\begin{gathered} 100 \mathrm{mV} \text { @ } \\ 10 \mathrm{~mA} \end{gathered}$ | - | 12 | $\sqrt{ }$ |  |  |  |  |  |  |  |  | w/ ENABLE, Low $\mathrm{I}_{\mathrm{Q}}$ |
| 80 mA | NCP4561 |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 0.16 \text { V @ } \\ 80 \text { mA } \end{gathered}$ | - | 12 | $\checkmark$ |  |  |  |  |  |  |  |  | w/ ENABLE, Ultra Low Noise |
| 100 mA | MC33160 |  |  |  |  |  |  |  |  |  |  |  |  | $\sqrt{ }$ |  |  |  | - | - | - | 40 |  |  |  |  |  |  |  |  |  | Regulator and Supervisory Circuit in SOP-16L and DIP-16 Packages |
| 100 mA | CS9201 |  |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  | 2.0 | $\begin{gathered} 0.4 \mathrm{~V} @ \\ 100 \mathrm{~mA} \end{gathered}$ | 6.0 | 26 |  |  | $\checkmark$ |  |  |  |  |  |  | No Cap, 74 V Load Dump Protection |
| 100 mA | CS9202 |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  | 2.0 | - | 4.5 | 26 |  |  | $\checkmark$ |  |  |  |  |  |  | No Cap, 74 V Load Dump Protection |
| 100 mA | CS8221 |  |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  | $\sqrt{ }$ |  |  | $\sqrt{ }$ |  |  |  | - |
| 100 mA | CS8311 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  | 2.0 | $\begin{gathered} 0.4 \mathrm{~V} @ \\ 100 \mathrm{~mA} \end{gathered}$ | - | 26 |  |  | $\sqrt{ }$ |  |  |  |  |  |  | w/ RESET and ENABLE, 60 V Load Dump Protection |

5. Output voltages from 2.0 V to 6.0 V , in 0.1 V increments, are available on request.
*Q2, 2001

Low Dropout Voltage Regulators (continued)

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  |  | $\left\lvert\, \begin{aligned} & > \\ & \infty \\ & \underset{\sim}{n} \end{aligned}\right.$ | $\begin{aligned} & > \\ & \text { in } \end{aligned}$ | $\left\|\begin{array}{l} \vec{\lambda} \\ \vec{N} \end{array}\right\|$ | $\begin{aligned} & > \\ & \boldsymbol{D}_{0} \\ & \underset{\sim}{n} \end{aligned}$ | $\left\|\begin{array}{l} > \\ \underset{\sim}{\infty} \\ \underset{\sim}{\infty} \end{array}\right\|$ | $\begin{aligned} & > \\ & 0 \\ & \text { c } \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & \underset{~ N}{c} \\ & \text { ल. } \end{aligned}\right.$ | $\begin{aligned} & > \\ & \mathbf{c} \\ & \text { ci } \end{aligned}$ | $\begin{aligned} & > \\ & \infty \\ & \infty \\ & \hline \end{aligned}$ | $\left\|\begin{array}{l} > \\ 0 \\ \dot{\sigma} \end{array}\right\|$ | $\begin{aligned} & > \\ & \stackrel{n}{n} \\ & \dot{\sim} \end{aligned}$ | $\underset{\sim}{>} \mid$ | > ${ }^{>}$ |  | き |  | Drop Out Voltage | Min. | Max. |  |  |  |  |  | צ |  |  |  | $\frac{\square}{\bar{a}}$ | Additional Features |
| 100 mA | CS8151 |  |  |  |  |  |  |  |  |  |  |  |  |  | $\sqrt{ }$ |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | w/ WATCHDOG, RESET, WAKE UP \& DELAY, 74 V Load Dump Protection |
| 100 mA | CS8151C |  |  |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  | 1.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  |  |  |  |  | $\checkmark$ | w/ WATCHDOG, RESET, WAKE UP \& DELAY, 60 V Load Dump Protection |
| 100 mA | CS8101 |  |  |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} \text { @ } \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  | $\checkmark \sqrt{ } \sqrt{ }$ |  |  |  |  | $\checkmark$ |  |  | w/ RESET and ENABLE, 60 V Load Dump Protection |
| 100 mA | CS8271 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | - | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | - | 30 |  |  | $\|\sqrt{ }\|$ |  |  |  |  |  |  | $\checkmark$ | w/ ENABLE |
| 100 mA | L4949 |  |  |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  | 1.0 | $\begin{gathered} 0.2 \mathrm{~V} @ \\ 50 \mathrm{~mA} \end{gathered}$ | 5.0 | 28 |  |  | $\checkmark$ | $\checkmark$ |  |  |  |  |  |  | Power-On Reset, Input Voltage Sense |
| 100 mA | LM2931/A |  |  |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  | $\begin{aligned} & 3.8 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 0.16 \mathrm{~V} @ \\ 100 \mathrm{~mA} \end{gathered}$ | - | 40 |  |  | $\checkmark$ |  |  | $\checkmark \sqrt{ }$ |  | $\sqrt{ } \sqrt{ }$ |  |  | - |
| 100 mA | LM2931C/AC | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | $\begin{aligned} & 5.0 \\ & 2.0 \end{aligned}$ | $\begin{gathered} 0.16 \text { V @ } \\ 100 \mathrm{~mA} \end{gathered}$ | - | 40 |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark \sqrt{ }$ |  |  | - |
| 100 mA | LP2950C/AC |  |  |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  |  | $\|\sqrt{ }\|$ |  |  |  | $\begin{aligned} & 1.0 / \\ & 0.5 \end{aligned}$ | $\begin{gathered} 0.38 \text { V @ } \\ 100 \mathrm{~mA} \end{gathered}$ | - | 30 |  |  |  |  |  | $\sqrt{ }$ |  | $\sqrt{ }$ |  |  | - |
| 100 mA | LP2951C/AC | $\checkmark$ |  |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  |  | $\checkmark$ |  |  |  | $\begin{aligned} & 1.0 / \\ & 0.5 \end{aligned}$ | $\begin{gathered} 0.38 \text { V @ } \\ 100 \text { mA } \end{gathered}$ | - | 30 |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |  |  |  |  |  | - |
| 120 mA | MC78FCxx |  |  |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  | $\sqrt{ }$ |  | $\checkmark$ |  |  | 6. | 2.5 | $\begin{gathered} 0.5 \mathrm{~V} @ \\ 40 \mathrm{~mA} \end{gathered}$ | 2.0 | 10 |  | $\checkmark$ |  |  |  |  |  |  |  |  | - |
| 150 mA | MC78PCxx |  |  | $\sqrt{ }$ | $\checkmark$ |  | $\sqrt{ }$ |  | $\checkmark$ |  | $\checkmark$ |  |  |  | $\sqrt{ }$ |  |  |  | 2.0 | $\begin{aligned} & 0.2 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | - | 8.0 | $\checkmark$ |  |  |  |  |  |  |  |  |  | w/ ENABLE |
| 150 mA | MC33263 |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  |  |  | - | $\begin{gathered} 0.18 \text { V @ } \\ 150 \mathrm{~mA} \end{gathered}$ | - | 12 | $\checkmark$ |  |  |  |  |  |  |  |  |  | w/ ENABLE, Ultra Low Noise |

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Low Dropout Voltage Regulators (continued)

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  | Additional Features |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  | $\underset{\sim}{>}$ | $\begin{aligned} & > \\ & \text { in } \\ & \text { N } \end{aligned}$ | $\left\|\begin{array}{l} > \\ \underset{\sim}{\mathrm{N}} \end{array}\right\|$ | $\underset{\substack{\infty \\ \underset{\sim}{n}}}{ }$ | $\left\|\begin{array}{l} > \\ \underset{\infty}{\infty} \\ \underset{\sim}{*} \end{array}\right\|$ | $\begin{aligned} & \text { > } \\ & \text { ले } \end{aligned}$ | $\begin{aligned} & > \\ & \mathbf{N} \\ & \mathrm{N} \end{aligned}$ | $\begin{array}{\|l\|l\|} > & > \\ \mathbf{m} & \infty \\ ल & 0 \\ m \end{array}$ | $\underset{\sim}{c}$ | $\left\lvert\, \begin{gathered} > \\ N \\ \dot{r} \end{gathered}\right.$ | $\left\lvert\, \begin{aligned} & > \\ & 10 \end{aligned}\right.$ | $\left\|\begin{array}{l} > \\ \infty \end{array}\right\|$ |  |  | $\begin{aligned} & \mathscr{U} \\ & \frac{\pi}{\pi} \\ & \frac{1}{\omega} \\ & \frac{0}{0} \\ & \hline 1 \end{aligned}$ | Drop Out Voltage | Min. | Max. | $\left\|\begin{array}{l} 0 \\ 0 \\ 0 \\ 0 \end{array}\right\|$ |  |  |  | ¢ ¢ ¢ | N | No | $\mathfrak{l}$ |  |  |
| 150 mA | CS8321 |  |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  | 2.0 | $\begin{aligned} & \hline 0.3 \mathrm{~V} @ \\ & 150 \mathrm{~mA} \end{aligned}$ | - | 26 |  |  |  |  | $\checkmark$ |  | Y |  |  | 45 V Load Dump Protection |
| 150 mA | NCP500 |  | $\checkmark$ | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 2.5 | $\begin{gathered} 0.165 \mathrm{~V} @ \\ 150 \mathrm{~mA} \end{gathered}$ | - | 6.0 |  |  |  |  |  |  |  | $\checkmark$ |  | w/ Shutdown |
| 150 mA | NCP511 |  | $\sqrt{ } \sqrt{ }$ | $\sqrt{ }$ | $\sqrt{ }$ | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | - | $\begin{array}{\|c} 0.170 \mathrm{~V} @ \\ 150 \mathrm{~mA} \end{array}$ | - | 6.0 |  |  |  |  |  |  |  | $\checkmark$ |  | w/ Shutdown |
| 150 mA | NCP551 |  | $\checkmark \sqrt{ } \sqrt{ }$ | $\checkmark$ | $\sqrt{ }$ | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 2.0 | $\begin{gathered} 44 \mathrm{mV} \text { @ } \\ 10 \mathrm{~mA} \end{gathered}$ | - | 12 |  |  |  |  |  |  |  | $\checkmark$ |  | w/ Shutdown |
| 200 mA | MC33565 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  | 2.0 | - | 4.3 | 5.5 |  |  | $\checkmark$ |  |  |  |  |  |  | w/ Auxiliary Control |
| 300 mA | MC33275 |  |  | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 2.0 | $\begin{gathered} 0.26 \text { V @ } \\ 300 \mathrm{~mA} \end{gathered}$ | - | 12 |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  |  | - |
| 300 mA | MC33375 |  | $\checkmark$ | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 2.0 | $\begin{gathered} 0.26 \text { V @ } \\ 300 \mathrm{~mA} \end{gathered}$ | - | 12 |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | w/ ENABLE |
| 300 mA | CS8120 |  |  |  |  |  |  |  |  |  |  |  | $\|\sqrt{ }\|$ |  |  |  | 4.0 | $\begin{aligned} & 1.0 \mathrm{~V} @ \\ & 200 \mathrm{~mA} \end{aligned}$ | - | 26 |  |  | $\checkmark$ |  | $\sqrt{ }$ |  | $\checkmark$ |  | $\checkmark$ | w/ RESET and ENABLE, 60 V Load Dump Protection |
| 500 mA | CS8140/1 |  |  |  |  |  |  |  |  |  |  |  | $\sqrt{ }$ |  |  |  | 4.0 | $\begin{gathered} 1.25 \mathrm{~V} @ \\ 500 \mathrm{~mA} \end{gathered}$ | - | 26 |  |  | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ | w/ ENABLE, RESET and WATCHDOG, 60 <br> V Load Dump Protection |
| 500 mA | CS5231-3 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  | 2.0 | - | - | 6 |  |  | $\checkmark$ |  | $\sqrt{ }$ |  |  |  |  | w/ Auxiliary Control |
| 500 mA | CS5233-3 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  | 2.0 | - | - | 6 |  |  | $\checkmark$ |  |  |  |  |  |  | w/ Auxiliary Control and Standby Input |

[^1]Low Dropout Voltage Regulators (continued)

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  |  | $\begin{aligned} & > \\ & \mathbf{n} \\ & \mathrm{N} \end{aligned}$ | $\left\|\begin{array}{l} \lambda \\ \vec{N} \\ \mathrm{~N} \end{array}\right\|$ | $\begin{aligned} & > \\ & \infty \\ & \mathbf{N} \end{aligned}$ | $\left\|\begin{array}{l} > \\ \infty \\ \infty \\ \dot{N} \end{array}\right\|$ | $\begin{aligned} & > \\ & \hline 0 \\ & \text { ci } \end{aligned}$ | $\left\|\begin{array}{l} > \\ \underset{N}{n} \\ ल \end{array}\right\|$ | $\begin{array}{\|l\|l\|l\|l\|} > & > \\ \infty & \infty \\ ल & 0 \\ \hline \end{array}$ | $\begin{array}{l\|l} > & > \\ 0 \\ \dot{j} & 0 \\ \dot{\sim} \end{array}$ | $\left\lvert\, \begin{gathered} > \\ n_{n} \\ \underset{寸}{ } \end{gathered}\right.$ | $\underset{i n}{>}>\infty$ | $0$ |  |  | Drop Out Voltage | Min. | Max. |  |  |  | - | ¢ |  |  | $$ |  | Additional Features |
| 750 mA | CS8122 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 2.0 | $\begin{gathered} \hline 0.35 \mathrm{~V} @ \\ 500 \mathrm{~mA} \end{gathered}$ | 6.0 | 26 |  |  |  |  |  |  |  | $\checkmark$ |  | w/ Delayed RESET, 60 V Load Dump Protection |
| 750 mA | CS8126-X |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 3.0 | $\begin{gathered} 0.35 \mathrm{~V} @ \\ 500 \mathrm{~mA} \end{gathered}$ | 6.0 | 26 |  |  | $\checkmark$ |  | $\checkmark$ |  |  |  |  | w/ Delayed RESET, 60 V Load Dump Protection |
| 750 mA | CS8129 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 3.0 | $\begin{gathered} 0.35 \mathrm{~V} @ \\ 500 \mathrm{~mA} \end{gathered}$ | 6.0 | 26 |  |  | $\checkmark$ |  |  |  |  | $\checkmark$ |  | w/ Delayed RESET, 60 V Load Dump Protection |
| 750 mA | CS403 |  |  |  |  |  |  |  |  |  |  |  | $\sqrt{ }$ |  |  | 5.0 | $\begin{aligned} & 1.4 \mathrm{~V} @ \\ & 750 \mathrm{~mA} \end{aligned}$ | - | 18 |  |  |  |  |  |  |  | $\checkmark$ |  | w/ RESET |
| 800 mA | MC33269 | $\checkmark$ |  |  |  |  |  |  |  | $\checkmark$ |  |  | $\sqrt{ }$ |  | $\checkmark$ | 1.0 | $\begin{aligned} & 1.1 \mathrm{~V} @ \\ & 800 \mathrm{~mA} \end{aligned}$ | - | 20 |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | - |
| 800 mA | MC34268 |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  |  | 1.4 | $\begin{aligned} & 1.1 \mathrm{~V} @ \\ & 800 \mathrm{~mA} \end{aligned}$ | - | 15 |  |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  |  | For SCSI-2 Active Termination |
| 1.0 A | CS5201-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  | 1.0 | $\begin{gathered} 1.0 \text { V @ } \\ 1.0 \text { A } \end{gathered}$ | - | 7.0 |  |  |  |  | $\sqrt{ }$ | $\checkmark$ |  | $\checkmark$ |  | - |
| 1.0 A | CS5201-3 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  | 1.5 | $\begin{gathered} 1.0 \mathrm{~V} @ \\ 1.0 \mathrm{~A} \end{gathered}$ | - | 7.0 |  |  |  |  | $\checkmark$ | $\sqrt{ } \sqrt{ }$ |  | $\checkmark$ |  | - |
| 1.5 A | CS52015-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  | 1.0 | $\begin{aligned} & 1.05 \text { V @ } \\ & 1.5 \text { A } \end{aligned}$ | - | 7.0 |  |  |  |  | $\checkmark$ | $\sqrt{ } \sqrt{ }$ |  | $\checkmark$ |  | - |
| 1.5 A | CS52015-3 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  | 1.5 | $\begin{aligned} & 1.05 \mathrm{~V} @ \\ & 1.5 \mathrm{~A} \end{aligned}$ | - | 7.0 |  |  |  |  | $\checkmark$ | $\checkmark$ |  | $\checkmark$ |  | - |
| 1.5 A | CS5233-3 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  | 2.0 | - | - | 6.0 |  |  |  |  | $\sqrt{ }$ | ) |  |  |  | w/ Auxiliary Control and Standby Input |

8. Output voltages from 2.0 V to 6.0 V , in 0.1 V increments, are available on request.
*Q2, 2001

Low Dropout Voltage Regulators (continued)

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  |  | $\begin{aligned} & > \\ & \text { No } \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & \underset{\sim}{\mathrm{N}} \end{aligned}\right.$ | $\begin{aligned} & > \\ & \mathbf{\infty} \\ & \mathbf{N} \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & \\ & \underset{\sim}{\infty} \\ & \text { in } \end{aligned}\right.$ | $\begin{aligned} & > \\ & \text { ò } \\ & \text { in } \end{aligned}$ | $\left\|\begin{array}{l} > \\ \underset{N}{N} \\ \mathrm{~m} \end{array}\right\|$ | $\xrightarrow{\text { che }}$ |  |  |  | $>\infty$ | $\left\lvert\, \begin{aligned} & > \\ & 0 \\ & 0 \end{aligned}\right.$ |  |  | Drop Out Voltage | Min. | Max. |  | 20 | $\begin{array}{\|l\|l} \infty & \begin{array}{c} 3 \\ 0 \\ 0 \\ 0 \\ 0 \end{array} \\ 0 & 0 \\ 0 \end{array}$ |  |  |  |  | $\left\|\begin{array}{l} 10 \\ 0 \\ 0 \\ 0 \\ 0 \\ 1 \end{array}\right\|$ |  | Additional Features |
| 3.0 A | CS5203-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 1.2 \mathrm{~V} @ \\ 3.0 \mathrm{~A} \end{gathered}$ | - | 7.0 |  |  |  |  |  |  | $\checkmark$ |  |  | - |
| 3.0 A | CS5203-3 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  | 1.5 | $\begin{gathered} 1.15 \mathrm{~V} @ \\ 3.0 \mathrm{~A} \end{gathered}$ | - | 7.0 |  |  |  |  |  |  |  |  |  | - |
| 3.0 A | CS5203A-X | $\checkmark$ | $\sqrt{ }$ |  |  |  |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 1.0 | $\begin{gathered} 1.05 \text { V @ } \\ 3.0 \text { A } \end{gathered}$ | - | 17 |  |  |  |  |  |  | $\checkmark$ |  |  | - |
| 3.0 A | CS5253-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1.0 | $\begin{gathered} 0.4 \mathrm{~V} \text { @ } \\ 3.0 \text { A } \end{gathered}$ | - | 6.0 |  |  |  |  |  |  |  |  |  | w/ Control and Sense |
| 3.0 A | CS5253B-8 |  |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 0.4 \text { V @ } \\ 3.0 \text { A } \end{gathered}$ | - | 6.0 |  |  |  |  |  |  |  |  |  | - |
| 4.0 A | CS5204-X | $\checkmark$ |  |  |  |  |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 1.0 | $\begin{gathered} 1.1 \mathrm{~V} @ \\ 4.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  |  | $\checkmark$ |  |  | - |
| 4.0 A | CS5204-2 |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  | 2.0 | $\begin{gathered} 1.1 \text { V @ } \\ 4.0 \text { A } \end{gathered}$ | - | 17 |  |  |  |  |  |  | $\checkmark$ |  |  | - |
| 5.0 A | CS5205-X | $\checkmark$ |  |  |  |  |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 1.0 | $\begin{gathered} 1.2 \mathrm{~V} @ \\ 5.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  | $\checkmark$ | $\sqrt{ }$ |  |  | - |
| 5.0 A | CS5205-2 |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  | 2.0 | $\begin{gathered} 1.2 \mathrm{~V} @ \\ 5.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  | $\sqrt{ }$ | $\sqrt{ }$ |  |  | - |
| 5.0 A | CS5205A-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1.0 | $\begin{gathered} 1.15 \mathrm{~V} \text { @ } \\ 5.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  | $\sqrt{ }$ | $\sqrt{ }$ |  |  | - |
| 6.0 A | CS5206-X | $\checkmark$ |  |  |  |  |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | 1.0 | $\begin{gathered} 1.3 \mathrm{~V} @ \\ 6.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  | $\checkmark$ | $\sqrt{ }$ |  |  | - |
| 7.0 A | CS5207-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 1.4 \mathrm{~V} @ \\ 7.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  |  | $\checkmark$ |  |  | - |
| 7.0 A | CS5207-2 |  | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  | 2.0 | $\begin{gathered} 1.45 \mathrm{~V} \text { @ } \\ 7.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  |  | $\checkmark$ |  |  | - |

9. Output voltages from 2.0 V to 6.0 V , in 0.1 V increments, are available on request.
*Q2, 2001

Low Dropout Voltage Regulators (continued)

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number | \|r| |  | $\left\lvert\, \begin{aligned} & > \\ & \mathbf{n} \\ & \text { N } \end{aligned}\right.$ |  |  | B\| |  |  |  |  |  |  |  |  | Drop Out Voltage | Min. | Max. | OR |  |  | ¢ 0 |  |  | ~ |  | Additional Features |
| 7.0 A | CS5207-3 |  |  |  |  |  |  |  |  |  |  |  |  |  | 2.0 | $\begin{gathered} \hline 1.4 \mathrm{~V} \text { @ } \\ 7.0 \mathrm{~A} \end{gathered}$ | - | 17 |  |  |  |  |  |  |  |  | - |
| 7.0 A | CS5207A-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{aligned} & 0.96 \text { V @ } \\ & 7.0 \mathrm{~A} \end{aligned}$ | - | 6.0 |  |  |  |  |  |  | $\checkmark$ |  | - |
| 7.0 A | CS5257A-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 0.35 \text { V @ } \\ 7.0 \text { A } \end{gathered}$ | - | 6.0 |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  | w/ Control and Sense |
| 8.0 A | CS5208-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 0.96 \text { V @ } \\ 8.0 \text { A } \end{gathered}$ | - | 6.0 |  |  |  |  |  |  | $\checkmark$ |  | - |
| 8.0 A | CS5258-1 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  | 1.5 | $\begin{gathered} 0.4 \mathrm{~V} @ \\ 8.0 \text { A } \end{gathered}$ | - | 6.0 |  |  |  |  |  |  | $\checkmark$ |  | w/ Control and Sense |

[^2]

## Wireless Portable

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number | (1) |  | - |  |  | $\begin{aligned} & > \\ & \stackrel{\rightharpoonup}{m} \\ & \hline \end{aligned}$ | $\left\lvert\, \begin{aligned} & > \\ & \underset{\sim}{c} \\ & \text { an } \end{aligned}\right.$ | $\left\lvert\, \begin{aligned} & \stackrel{\rightharpoonup}{m} \\ & \underset{\omega}{2} \end{aligned}\right.$ |  | Drop Out Voltage | Min. | Max. | $\left\|\begin{array}{c} \tilde{0} \\ 1 \\ 1 \\ 0 \\ 0 \end{array}\right\|$ |  |  | M |  |  | (1) |  | Additional Features |
| $\begin{aligned} & 80 \mathrm{~mA}, \\ & 80 \mathrm{~mA} \end{aligned}$ | MC33762 |  |  | $\begin{array}{\|l} \hline \sqrt{ }, \\ \sqrt{2} \end{array}$ | $\begin{array}{\|l\|} \hline v, \\ V \end{array}$ |  | $\sqrt{\sqrt{v}}$ |  |  | - | $\begin{aligned} & \hline 0.16 \mathrm{~V} @ 80 \mathrm{~mA}, \\ & 0.16 \mathrm{~V} @ 80 \mathrm{~mA} \end{aligned}$ | - | 12 |  |  | $\checkmark$ |  |  |  |  |  | Dual, Ultra Low Noise, 1 V ON/OFF Control, No External Cap |
| - | MC33765 |  |  |  | $\checkmark$ |  |  |  |  | 3.0 | 0.17 V @ 150 mA | 3.0 | 5.3 |  |  |  |  |  |  | $\checkmark$ |  | 5 Outputs, Ultra Low Noise |

## NIC \& PCI Cards

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  | $\gg$ | - |  |  |  | $\left\|\begin{array}{l} > \\ \mathbf{N} \\ \text { m} \end{array}\right\|$ | $\begin{aligned} & \vec{\lambda} \\ & \mathbf{m} \\ & ल \end{aligned}$ |  | Drop Out Voltage | Min. | Max. |  | 0 0 1 1 0 0 |  |  |  |  |  | $\left\|\begin{array}{l} 0 \\ \frac{0}{2} \\ 0 \\ 0 \\ 0 \\ 0 \end{array}\right\|$ | 믐 | Additional Features |
| 200 mA | MC33565 |  |  |  |  |  |  |  | $\checkmark$ | 2.0 | - | 4.3 | 5.5 |  |  | $\checkmark$ |  |  |  |  |  |  | w/ Auxiliary Control |
| 500 mA | CS5231-3 |  |  |  |  |  |  |  | $\checkmark$ | 2.0 | - | - | 6.0 |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | w/ Auxiliary Control |
| 1.2 A | MC33566 |  |  |  |  |  |  |  | $\checkmark$ | - | - | 4.35 | 5.5 |  |  |  |  |  | $\checkmark$ |  |  |  | w/ Auxiliary Control |
| 1.5 A | CS5233-3 |  |  |  |  |  |  |  | $\checkmark$ | 2.0 | - | - | 6.0 |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  | w/ Auxiliary Control |

Computing

|  |  | Output Voltage |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  |  |  |  |  |  |  |  | Drop Out Voltage | Min. | Max. | $\left\lvert\, \begin{gathered} \substack{0 \\ 1 \\ 1 \\ 0 \\ 0} \\ \hline \end{gathered}\right.$ |  |  | - |  |  |  | Additional Features |
| 800 mA | MC34268 |  |  |  |  | $\checkmark$ |  |  | 1.4 | 1.1 V @ 800 mA | - | 15 |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ |  |  | For SCSI-2 Active Termination |
| - | MC33567-1 |  | $\checkmark$ | $\checkmark$ |  |  |  |  | 2.5 | - | - | 12.5 |  | $\checkmark$ |  |  |  |  |  | Dual, External Pass Transistor |
| - | MC33567-2 |  |  |  | $\stackrel{V}{v}$ |  |  |  | - | - | - | - |  | $\checkmark$ |  |  |  |  |  | Dual, External Pass Transistor |
| - | MC33567-3 |  | $\checkmark$ | $\checkmark$ |  |  |  |  | - | - | - | - |  | $\checkmark$ |  |  |  |  |  | Dual, External Pass Transistor |



Automotive

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  | $\xrightarrow{>0}$ | - |  | - |  | $\left\|\begin{array}{c} \stackrel{\rightharpoonup}{\infty} \\ \underset{\sim}{2} \end{array}\right\|$ |  |  | $\stackrel{>}{\infty}$ | ㅇ | $\underset{\sim}{\text { N }}$ | $\left\|\begin{array}{l} \vec{~} \\ 0 \\ \dot{f} \end{array}\right\|$ |  | Drop Out Voltage | Min. | Max. |  | $\left\|\begin{array}{c\|c} 0.0 \\ 0 \\ 1 \\ 1 & 0 \\ 0 \\ 0 & 0 \\ 0 \end{array}\right\|$ |  |  | $\frac{\infty}{\infty}$ |  |  |  | Additional Features |
| 100 mA | MC33160 |  |  |  |  |  |  |  |  | $\mid$ |  |  |  |  | - | - | - | 40 |  |  |  |  |  |  |  |  | Regulator and Supervisory Circuit in SOP-16L and DIP-16 Packages |
| 100 mA | CS9201 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  |  |  |  | No Cap |
| 100 mA | CS9202 |  |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 4.5 | 26 |  | $\checkmark$ |  |  |  |  |  |  | No Cap |
| 100 mA | CS8221 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  | $\|v\|$ |  |  |  | $\checkmark$ |  |  | - |
| 100 mA | CS8311 |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | - | 26 |  | $\|\sqrt{ }\|$ | $\checkmark$ |  |  |  |  |  | w/ RESET and ENABLE, 60 V Load Dump Protection |
| 100 mA | CS8151 |  |  |  |  |  |  |  |  | $\mid$ |  |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ v | w/ WATCHDOG, RESET, WAKE UP and DELAY, 74 V Load Dump Protection |
| 100 mA | CS8101 |  |  |  |  |  |  |  |  | $\|v\|$ |  |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  |  | $\checkmark$ |  | uPower w/ RESET and ENABLE, 60 V Load Dump Protection |
| 100 mA | CS8271 | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  | - | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | - | 30 |  | $\|\sqrt{ }\|$ | $\sqrt{ }$ |  |  |  |  | $\checkmark$ | uPower with ENABLE |
| 100 mA | L4949 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 1.0 | $\begin{gathered} 0.2 \mathrm{~V} @ \\ 50 \mathrm{~mA} \end{gathered}$ | 5.0 | 28 |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |  |  |  |  | Power-On Reset, Input Voltage Sense |

Automotive (continued)

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  | $\xrightarrow{7}$ | - |  |  |  | $\begin{aligned} & > \\ & \text { ल } \\ & \text { m } \end{aligned}$ | $\left\|\begin{array}{c} > \\ \infty \\ \infty \\ m \end{array}\right\|$ | $\begin{aligned} & > \\ & 0 \\ & -寸 \end{aligned}$ | $\begin{aligned} & > \\ & \stackrel{y}{n} \\ & \stackrel{\sigma}{*} \end{aligned}$ | $>$ | $>_{\infty}$ | > | $\underset{\sim}{\underset{\sim}{*}}$ | $$ |  | Drop Out Voltage | Min. | Max. | $\left\|\begin{array}{c} \underset{N}{N} \\ 1 \\ \underset{\sim}{0} \end{array}\right\|$ |  | $0$ |  | $\begin{aligned} & \frac{y}{x} \\ & \substack{a} \end{aligned}$ | $\left\|\begin{array}{c} \frac{x}{4} \\ \underset{Q}{\Omega} \end{array}\right\|$ | $$ | $\begin{array}{l\|l} \mathrm{N} \\ \mathrm{O} & \mathrm{~N} \\ \mathrm{~N} & 1 \\ \mathrm{O} & \mathrm{O} \end{array}$ | 0 $\vdots$ $\vdots$ 0 0 0 1 | 믐 | Additional Features |
| 100 mA | LM2931/A |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 3.8, 5.0 | $\begin{gathered} \hline 0.16 \mathrm{~V} @ \\ 100 \mathrm{~mA} \end{gathered}$ | - | 40 |  | $\checkmark$ |  |  | $\checkmark$ | $\checkmark$ |  | $\checkmark \checkmark$ |  |  | 60 V Load Dump Protection |
| 100 mA | LM2931C/AC | $\checkmark$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5.0, 2.0 | $\begin{gathered} 0.16 \text { V @ } \\ 100 \mathrm{~mA} \end{gathered}$ | - | 40 |  | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark \sqrt{ }$ |  |  | 60 V Load Dump Protection |
| 150 mA | CS8321 |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 2.0 | $\begin{aligned} & 0.3 \mathrm{~V} @ \\ & 150 \mathrm{~mA} \end{aligned}$ | - | 26 |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  | uPower w/ 45 V Load Dump Protection |
| 300 mA | CS8120 |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 4.0 | $\begin{aligned} & 1.0 \mathrm{~V} @ \\ & 200 \mathrm{~mA} \end{aligned}$ | - | 26 |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | w/ RESET and ENABLE, 60 V Load Dump Protection |
| 500 mA | CS8140/1 |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 4.0 | $\begin{gathered} 1.25 \mathrm{~V} \text { @ } \\ 500 \mathrm{~mA} \end{gathered}$ | - | 26 |  |  | $\checkmark$ |  |  |  |  | $\checkmark$ |  | $\checkmark$ | w/ ENABLE, <br> RESET and WATCHDOG, 60 V Load Dump Protection |
| 750 mA | CS8122 |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 2.0 | $\begin{aligned} & 0.35 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  |  |  | $\checkmark$ |  |  | w/ Delayed RESET, 60 V Load Dump Protection |
| 750 mA | CS8126-1 |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 3.0 | $\begin{gathered} 0.35 \mathrm{~V} @ \\ 500 \mathrm{~mA} \end{gathered}$ | 6.0 | 26 |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ |  |  | w/ Delayed RESET, 60 V Load Dump Protection |
| 750 mA | CS8129 |  |  |  |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 3.0 | $\begin{gathered} 0.35 \mathrm{~V} @ \\ 500 \mathrm{~mA} \end{gathered}$ | 6.0 | 26 |  |  | $\checkmark$ |  |  |  |  | $\checkmark$ |  |  | w/ Delayed RESET, 60 V Load Dump Protection |

Automotive（continued）

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output <br> Current | Part Number |  |  |  | cicos | $\left\lvert\, \begin{aligned} & > \\ & \underset{ल}{n} \end{aligned}\right.$ | $\underset{\substack{>\\ \underset{\sim}{n}}}{ }$ |  |  | $\ggg>$ | $\left.\right\|_{\infty}$ | io | $\underset{\sim}{\mathrm{N}}$ | $\left\|\begin{array}{l} \mathbf{M} \\ \mathbf{0} \\ \mathbf{2} \\ \mathbb{心} \\ \stackrel{心}{心} \end{array}\right\|$ |  | $\begin{aligned} & \text { Drop Out } \\ & \text { Voltage } \end{aligned}$ | Min． | Max． |  |  | $\left(\begin{array}{l\|l} \infty \\ 0 \\ 0 \\ 0 \\ & \frac{0}{0} \\ \hline \frac{2}{2} \end{array}\right.$ |  |  |  |  | Additional Features |
| $\begin{aligned} & 100 \mathrm{~mA}, \\ & 250 \mathrm{~mA} \end{aligned}$ | CS8361 | $\checkmark$ |  |  |  |  |  |  |  | $\checkmark$ |  |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \\ & 0.4 \mathrm{~V} @ \\ & 250 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  | $\checkmark$ |  |  |  |  |  | Dual，uPower w／ RESET and ENABLE |
| $\begin{aligned} & 100 \mathrm{~mA}, \\ & 250 \mathrm{~mA} \end{aligned}$ | CS8363 | $\checkmark$ |  |  |  |  | $\checkmark$ |  |  |  |  |  |  |  | 2.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA}, \\ & 0.4 \mathrm{~V} @ \\ & 250 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  | $\|v\|$ |  |  | Dual，uPower w／ RESET and ENABLE |
| $\begin{aligned} & 250 \mathrm{~mA}, \\ & 100 \mathrm{~mA} \end{aligned}$ | CS8481 |  |  |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  |  |  |  | 3.0 | - $100 \mathrm{~mA}$ | － | 30 |  |  |  |  | $\|\sqrt{ }\|$ |  |  | Dual，w／ENABLE |
| $\begin{aligned} & 250 \mathrm{~mA}, \\ & 100 \mathrm{~mA} \end{aligned}$ | CS8391 |  |  |  |  |  |  |  |  | $\begin{aligned} & \sqrt{ }, \\ & \sqrt{2} \end{aligned}$ |  |  |  |  | 3.0 |  | － | 45 |  |  |  |  | $\|\sqrt{ }\|$ |  |  | Dual，w／ENABLE |
| $\begin{gathered} 250 \mathrm{~mA}, \\ 100 \mathrm{~mA} \end{gathered}$ | CS8281 |  |  |  |  |  |  |  |  | $\begin{aligned} & \sqrt{ }, \\ & \sqrt{2} \end{aligned}$ |  |  |  |  | 3.0 | $\begin{aligned} & 0.4 \mathrm{~V} @ \\ & 250 \mathrm{~mA}, \\ & 0.4 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  | $\|v\|$ |  |  | Dual，w／ENABLE |
| $400 \mathrm{~mA} \text {, }$ $200 \mathrm{~mA}$ | CS8161 |  |  |  |  |  |  |  |  | $V$ |  |  | $\checkmark$ |  | $\begin{aligned} & 5.0, \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 0.35 \mathrm{~V} @ \\ & 400 \mathrm{~mA}, \\ & 0.35 \mathrm{~V} \text { @ } \\ & 200 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  |  |  | Dual，w／ENABLE |
| $\begin{gathered} 500 \mathrm{~mA}, \\ 70 \mathrm{~mA} \end{gathered}$ | CS8147 |  |  |  |  |  |  |  |  | $\checkmark$ |  | $\checkmark$ |  |  | $\begin{aligned} & 5.0, \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 0.5 \mathrm{~V} @ \\ & 500 \mathrm{~mA} \\ & 1.5 \mathrm{~V} \text { @ } \\ & 70 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  |  | $\checkmark$ | Dual，w／ENABLE |

Automotive (continued)

|  |  | Output Voltage |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Input Voltage |  | Package |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Current | Part Number |  | $\xrightarrow{>0}$ | $\cdots$ | $\stackrel{l}{l} \mid \vec{\infty}$ | - | $\underset{\substack{>\\ \underset{\sim}{n}}}{ }$ |  | $\left\|\begin{array}{c} > \\ n \\ \dot{d} \end{array}\right\|$ | in | $\left.\right\|_{\infty} ^{\infty}$ | ? | $\underset{\sim}{\text { N }}$ |  |  | Drop Out Voltage | Min. | Max. |  | $3 \begin{array}{ll} \infty \\ 0 & \substack{3 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0} \\ \hline 0 \end{array}$ | (1) |  |  |  |  | Additional Features |
| $\begin{aligned} & 750 \mathrm{~mA}, \\ & 100 \mathrm{~mA} \end{aligned}$ | CS8156 |  |  |  |  |  |  |  |  | $\checkmark$ |  |  | $\checkmark$ |  | $\begin{aligned} & \hline 5.0, \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 0.6 \mathrm{~V} \text { @ } \\ & 750 \mathrm{~mA}, \\ & 0.6 \mathrm{~V} @ \\ & 100 \mathrm{~mA} \end{aligned}$ | 6.0 | 26 |  |  |  |  |  |  |  | Dual, w/ ENABLE |
| $\begin{gathered} 1.0 \mathrm{~A}, \\ 250 \mathrm{~mA} \end{gathered}$ | CS8371 |  |  |  |  |  |  |  |  | $\checkmark$ | $\checkmark$ |  |  |  | $\begin{aligned} & 5.0, \\ & 5.0 \end{aligned}$ | $\begin{gathered} 1.5 \mathrm{~V} @ \\ 1.0 \mathrm{~A}, \\ 2.5 \mathrm{~V} @ \\ 250 \mathrm{~mA} \end{gathered}$ | - | 16 |  |  |  |  |  | $\checkmark$ |  | Dual, Independent ENABLEs, NO CAP |



Supervisory

| Description | Typical Threshold Voltage ( $\mathrm{V}_{\text {th }}$ (V) | Supply Voltage Range <br> (V) | Typical Supply Current ( $\mu \mathrm{A}$ ) | Maximum Supply Current ( $\mu \mathrm{A}$ ) | Threshold Hysteresis (Typ) (mV) | Operating Temp. <br> Range ( ${ }^{\circ} \mathrm{C}$ ) | Package | Description | Time Delay (Typ) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MAX809 | $\begin{gathered} \hline 4.63,4.38,4.00,3.08, \\ 2.93,2.63 \text { * } \end{gathered}$ | 1.0 to 5.5 | 24 | 60 | - | -40 to +85 | SOT23 | $\begin{gathered} \hline \text { 3-Pin } \\ \text { Microprocessor } \\ \text { Reset Monitors } \end{gathered}$ | 240 msec |
| MAX810 | $\begin{gathered} \text { 4.63, 4.38, 3.08, 2.93, } \\ 2.63^{*} \end{gathered}$ | 1.0 to 5.5 | 24 | 60 | - | -40 to +85 | SOT23 | 3-Pin <br> Microprocessor Reset Monitors | 240 msec |
| MC33064 | 4.60 | 1.0 to 6.5 | 390 | 500 | 20 | -40 to +85 | SO-8, <br> Micro8, <br> TO-92 | Undervoltage Sensing Circuit | Ext. Capacitor Dependent |
| MC34064 | 4.60 | 1.0 to 6.5 | 390 | 500 | 20 | 0 to +70 | SO-8, <br> Micro8, TO-92 | Undervoltage Sensing Circuit | Ext. Capacitor Dependent |
| MC33161 | 1.27 | 2.0 to 40 (Pos Sensing) <br> 4.0 to 40 (Neg Sensing) | 560 | 900 | 25 | -40 to +85 | $\begin{aligned} & \text { SO-8, } \\ & \text { DIP-8 } \end{aligned}$ | Universal Voltage Monitor | Ext. Capacitor Dependent |
| MC34161 | 1.27 | 2.0 to 40 (Pos Sensing) <br> 4.0 to 40 (Neg Sensing) | 560 | 900 | 25 | 0 to +70 | $\begin{aligned} & \text { SO-8, } \\ & \text { DIP-8 } \end{aligned}$ | Universal Voltage Monitor | Ext. Capacitor Dependent |
| MC33164 | 2.71 ( $\mathrm{V}_{\text {in }}$ Increasing) <br> 2.65 ( $\mathrm{V}_{\text {in }}$ Decreasing) | 1.0 to 10 | 24 | 40 | 60 | -40 to +125 | $\begin{aligned} & \text { SO-8, } \\ & \text { Micro8, } \\ & \text { TO-92 } \end{aligned}$ | Micropower Undervoltage Sensing Circuits | Ext. Capacitor Dependent |
| MC34164 | 2.71 ( $\mathrm{V}_{\text {in }}$ Increasing) 2.65 ( $\mathrm{V}_{\text {in }}$ Decreasing) | 1.0 to 10 | 24 | 40 | 60 | 0 to +70 | $\begin{aligned} & \text { SO-8, } \\ & \text { Micro8, } \\ & \text { TO-92 } \end{aligned}$ | Micropower Undervoltage Sensing Circuits | Ext. Capacitor Dependent |
| MC3423 | 2.6 | 4.5 to 40 | 6.0 mA | 10 mA | - | 0 to +70 | $\begin{aligned} & \text { SO-8, } \\ & \text { DIP-8 } \end{aligned}$ | Overvoltage Crowbar Sensing Circuit | $0.5 \mu \mathrm{sec}$ |
| NCP300/1 | $\begin{gathered} 0.9,1.8,2.0,2.7,3.0, \\ 4.5,4.7 \end{gathered}$ | 0.8 to 10 | $\begin{gathered} 0.20 \text { to } \\ 0.34^{*} \end{gathered}$ | 1.2 to 1.4* | 45 to 235 <br> Depends on Threshold Voltage | -40 to +125 | TSOP-5 | Voltage Detector Series <br> NCP300-CMOS, NCP301-Open Drain | High to Low 45-97* $\mu \mathrm{sec}$ Low to High 77-130* $\mu \mathrm{sec}$ |

*Voltages from 1.6 to 4.9 V by steps of 0.1 V are available upon request.

Supervisory (continued)

| Description | Typical Threshold Voltage ( $\mathrm{V}_{\text {th }}$ ) (V) | Supply Voltage Range (V) | Typical Supply Current ( $\mu \mathrm{A}$ ) | Maximum Supply Current ( $\mu \mathrm{A}$ ) | Threshold Hysteresis (Typ) ( mV ) | Operating Temp. <br> Range ( ${ }^{\circ} \mathrm{C}$ ) | Package | Description | Time Delay (Typ) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3 | $\begin{gathered} 0.9,1.8,2.0,2.7,3.0, \\ 4.5,4.7 \end{gathered}$ | 0.8 to 10 | $\begin{gathered} 0.20 \text { to } \\ 0.34^{*} \end{gathered}$ | 1.2 to 1.4* | 45 to 235 Depends on Threshold Voltage | -40 to +125 | TSOP-5 | Voltage Detector Series with Programmable Delay NCP302-CMOS, NCP303-Open Drain | Ext. Capacitor Dependent |
| NCP304/5 | $\begin{gathered} 0.9,1.8,2.0,2.7,3.0, \\ 4.5,4.7 \end{gathered}$ | 0.8 to 10 | 0.8 to 1.1* | 3.0 to 3.9* | 45 to 235 <br> Depends on Threshold Voltage | -40 to +125 | SC-82AB | Voltage Detector Series <br> NCP304-CMOS, NCP305-Open Drain | High to Low 10-18* $\mu \mathrm{sec}$ Low to High $6-21^{*} \mu \mathrm{sec}$ |
| NCP345 | 6.85 | 3.0 to 25 | 750 | 1000 | 100 | -40 to +85 | TSOP-5 | Overvoltage Protection IC | $10 \mu \mathrm{sec}$ |

*Depends on the voltage threshold of the part


## MOSFET/IGBT Drivers

| Part No. | Configuration | Peak Output Current (A) | Output Resistance $\begin{gathered} \left(R_{H} / R_{L}\right) \\ \left(\operatorname{Max} \Omega @ 25^{\circ} \mathrm{C}\right) \end{gathered}$ | Max Supply Voltage (V) | Input/Output Delay $\left(\mathrm{t}_{\mathrm{D} 1}, \mathrm{t}_{\mathrm{D} 2}\right)^{*}$ (nsec) | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CS4124 | High-Side PWM FET Controller | 0.300 | - | 30 | 1000/1000 | DIP-16 |
| CS7054 | Low-Side PWM FET Controller | 0.400 | - | 30 | 1000/1000 | DIP-14 |
| CS8312 | IGBT Ignition Pre-Driver with Current Regulation | 5 mA | - | 12 | 30/30 ( $\mu \mathrm{s}$ ) | DIP-8, SO-8 |
| MC33153 | Single, Inverting Protection Circuits for IGBTs | 1.0 A (source) 2.0 A (sink) | - | 20 | 300/300 | DIP-8, SO-8 |
| MC33151 | Dual, Inverting Extended Operating Temp. | 1.5 | - | 20 | 100/100 | DIP-8, SO-8 |
| MC34151 | Dual, Inverting | 1.5 | - | 20 | 100/100 | DIP-8, SO-8 |
| MC33152 | Dual, Non-Inverting Extended Operating Temp. | 1.5 | - | 20 | 120/120 | DIP-8, SO-8 |
| MC34152 | Dual, Non-Inverting | 1.5 | - | 20 | 120/120 | DIP-8, SO-8 |

${ }^{*} t_{D 1}=$ delay time from input low-to-high transition to output transition. $\mathrm{t}_{\mathrm{D} 2}=$ delay time from input high-to-low transition to output transition.


Smart Drivers (High-Side, Low-Side \& H-Bridge)

|  | Part | Output |  | Features |  |  |  |  |  |  |  | Protection |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Number | Description | Current | $\mathrm{R}_{\mathrm{DS} \text { (on) }}$ <br> @ $25^{\circ} \mathrm{C}$ |  |  |  |  |  |  |  |  |  | $\begin{aligned} & \mathscr{0} \\ & \stackrel{\pi}{0} \\ & 0 \\ & 0 \\ & 00 \end{aligned}$ |  |  |  |
| CS1107 | Low-Side Single Relay Driver | 350 mA |  | $\checkmark$ | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | 40 V |
| CS1108 | Low-Side Single Lamp Driver | 350 mA |  | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | 40 V |
| CS1112 | Low-Side Quad Power Output Driver |  | $1.0 \Omega$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 60 V |
| CS3701 | Configurable Dual H-Bridge Driver | 500 mA |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 45 V |
| CS76113/4 | Low-Side Hex Power Output Driver |  | $0.75 \Omega$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 45 V |
| CS8240 | High-Side Driver | 500 mA |  | $\checkmark$ |  |  |  |  |  |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | 60 V |

Squib Drivers

| Part Number | Output |  |  | Features |  |  |  |  |  |  |  | Protection |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Number of Outputs | Loop | $\mathbf{R}_{\mathrm{DS}(\mathrm{on})}$ <br> @ $25^{\circ} \mathrm{C}$ |  |  |  |  |  |  |  |  |  |  |  |
| CS2082 | 2 | Dual | $750 \mathrm{~m} \Omega$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 60 V |



Brushless DC Motor Controllers

| Device | Operating Voltage Range（V） |  | 00$\#$00000050 |  |  |  |  | Output Drivers |  |  |  |  | \|드글 |  | $\begin{aligned} & \stackrel{0}{⿳ 亠 丷 厂 彡} \\ & \frac{\pi}{0} \\ & \stackrel{\pi}{0} \end{aligned}$ | Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathrm{V}_{\mathrm{Cc}}$ | $\mathrm{V}_{\mathrm{C}}$ |  |  |  |  |  |  | $\begin{aligned} & \stackrel{\vdots}{\circ} \\ & \stackrel{\rightharpoonup}{0} \\ & \text { 응응응 } \\ & \text { O. } \end{aligned}$ |  |  |  |  |  |  |  |
| MC33033 | 10－30 | － | $\checkmark$ | $\checkmark$ | $\checkmark$ | $60^{\circ} / 300^{\circ}$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | Noninv． Only | $\checkmark$ | － | － | － | DIP－20，SO－20L |
| MC33035 | 10－40 | 10－30 | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\begin{gathered} \text { and } \\ 120^{\circ} / 240^{\circ} \end{gathered}$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | Noninv． and Inv． | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | DIP－24，SO－24L |

Air Core Motor Drivers／Gauge Drivers

|  | Gauges Driven |  | Input |  |  | Output |  | Features |  |  | Protection |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Part Number | Major | Minor | Freq． | PWM | SPI | Current | Method | Return to Zero | UVLO | Regulator Output | Current Limit | Over Voltage | Over Temp． | Peak Transient |
| CS4121 | 1 |  | $\checkmark$ |  |  | 33 mA | Differential |  |  | $\checkmark$ |  | $\checkmark$ |  | 60 V |
| CS4122 | 1 | 2 | $\checkmark$ |  | $\checkmark$ | 80 mA | Differential |  |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | 18 V |
| CS8190 | 1 |  | $\checkmark$ |  |  | 33 mA | Differential | $\checkmark$ | $\checkmark$ |  |  | $\checkmark$ |  | 60 V |
| CS8191 | 1 |  | $\checkmark$ |  |  | 55 mA | Differential |  |  |  | $\checkmark$ | $\checkmark$ |  | 60 V |

## Stepper Motor Drivers／Odometer Drivers

|  | Input |  | Modes |  | Output |  | Features |  |  | Protection |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Part <br> Number | Sine | Square | ＋1 | ＋2 | Current | Method | UVLO | Buffered Speed Output | On－Chip <br> Flyback Diodes | Current Limit | Over Voltage | Peak Transient |
| CS4161 | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 85 mA | Differential | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\sqrt{ }$ | 60 V |
| CS8441 | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 85 mA | Differential |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | 60 V |



## Data Transmission

## Line Receivers - EIA Standard

| $\begin{array}{ll} \hline \mathbf{S}= & \text { Single } \\ & \text { Ended } \\ \mathrm{D}= & \text { Differential } \end{array}$ | Type of Output | $\mathrm{t}_{\text {prop }}$ Delay Time Max (ns) | Party Line Operation | Strobe <br> Enable | Power Supplies (V) | Device | Suffix/ <br> Package | Receivers Per Package | Companion Drivers | Comments |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| S | R (Note 11.) | 85 | - | - | +5.0 | $\begin{gathered} \text { MC1489 } \\ \text { MC1489A } \end{gathered}$ | $\begin{aligned} & \hline \text { DIP-16, } \\ & \text { SO-16 } \end{aligned}$ | 4 | MC1488 MC14C88B | EIA-232-D |

11. R = Resistor Pull-up, TP = Totem-pole output.

## Line Drivers - EIA Standard

| Output Current Capability (mA) | ```tprop Delay Time Max (ns)``` | $\begin{array}{ll} \mathrm{S}= & \text { Single } \\ & \text { Ended } \\ \mathrm{D}= & \text { Differential } \end{array}$ | Party Line Operation | Strobe or Enable | Power Supplies (V) | Device | Suffix/ <br> Package | Receivers Per Package | Companion Drivers | Comments |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 85 | 35 | D | $\checkmark$ | $\checkmark$ | +5.0 | $\begin{aligned} & \text { MC75174B } \\ & \text { MC75172B } \end{aligned}$ | SO-20L | 4 | - | EIA-485 |
| 10 | 350 | S | - |  | $\begin{gathered} \pm 9.0 \text { to } \\ \pm 12 \end{gathered}$ | MC1488 | $\begin{gathered} \hline \text { DIP-8, } \\ \text { SO-8 } \end{gathered}$ |  | $\begin{gathered} \text { MC1489 } \\ \text { MC1489A } \end{gathered}$ | EIA-232-D |
| 60 | 300 | S/D |  | $\begin{aligned} & \text { EIA-422 V } \\ & \text { EIA-423 - } \end{aligned}$ | $\pm 5.0$ | MC26LS30 | SO-16 | $\begin{aligned} & \hline 4(423) \\ & 2(422) \end{aligned}$ | - | $\begin{gathered} \text { EIA-422 or } \\ \text { EIA-423 } \end{gathered}$ <br> Switchable |

## Peripheral Drivers

| Output Current <br> Capability <br> $(\mathrm{mA})$ | Input <br> Capability | Propagation <br> Delay Time <br> Max $(\mu \mathrm{s})$ | Output <br> Clamp <br> Diode | Off State <br> Voltage <br> Max (V) | Device | Drivers <br> Per <br> Package | Suffix/ <br> Package |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 500 | TTL, 5.0 V <br> CMOS | 1.0 | $\sqrt{2}$ | 50 | MC1413B | Function |  |






Smart Drivers (High-Side, Low-Side \& H-Bridge)

|  | Part | Output |  | Features |  |  |  |  |  |  |  | Protection |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Number | Description | Current | $\mathrm{R}_{\mathrm{DS}(\text { on) }}$ <br> @ $25^{\circ} \mathrm{C}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |
| CS1107 | Low-Side Single Relay Driver | 350 mA |  | $\checkmark$ | $\checkmark$ |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | 40 V |
| CS1108 | Low-Side Single Lamp Driver | 350 mA |  | $\checkmark$ |  |  |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | 40 V |
| CS1112 | Low-Side Quad Power Output Driver |  | $1.0 \Omega$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 60 V |
| CS3701 | Configurable Dual H-Bridge Driver | 500 mA |  | $\checkmark$ |  | $\checkmark$ |  | $\checkmark$ |  |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 45 V |
| CS76113/4 | Low-Side Hex Power Output Driver |  | $0.75 \Omega$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | $\checkmark$ | 45 V |
| CS8240 | High-Side Driver | 500 mA |  | $\checkmark$ |  |  |  |  |  |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | 60 V |

Squib Drivers

| Part Number | Output |  |  | Features |  |  |  |  |  |  |  | Protection |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Number of Outputs | Loop | $\mathbf{R}_{\mathrm{DS}(\mathrm{on})}$ <br> @ $25^{\circ} \mathrm{C}$ |  |  |  |  |  |  |  |  |  |  |  |
| CS2082 | 2 | Dual | $750 \mathrm{~m} \Omega$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 60 V |

## Vacuum Fluorescent Drivers

| Part <br> Number | Outputs |  |  |  |  |  |  | Interface |  | Features |  |  |  |  | Protection |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Anodes |  |  | Grids |  |  | Type |  |  |  |  |  | ming |  |  |
|  | Count | Current | Voltage (Typ) | Count | Current | Voltage (Typ) |  | SPI | Data Out | Power On Reset | Low Iq | PWM Input Pin | Serial Input Bits | Multiplex | Max <br> Voltage |
| CS1087/9 | $\begin{gathered} 23 \\ 6 \end{gathered}$ | $\begin{gathered} 2 \mathrm{~mA} \\ 20 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & 0.3 \mathrm{~V} \\ & 0.3 \mathrm{~V} \end{aligned}$ | 3 | 50 mA | 0.5 V | $\begin{aligned} & \text { Push-Pull } \\ & \text { Push-Pull } \end{aligned}$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | Triplex | 18 V |
| CS1088 | $\begin{gathered} 25 \\ 6 \end{gathered}$ | $\begin{gathered} 2 \mathrm{~mA} \\ 20 \mathrm{~mA} \end{gathered}$ | $\begin{aligned} & 0.3 \mathrm{~V} \\ & 0.3 \mathrm{~V} \end{aligned}$ | 3 | 50 mA | 0.5 V | Push-Pull Push-Pull | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\checkmark$ |  | Triplex | 18 V |

## Sensor Interface

|  | Part | Features |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Number | Description | Channels | Hysteresis | Programmable Trip Level | Trimming Method | Active Input Clamps | $\mathrm{V}_{\text {cc }}$ Max |
| CS1124 | Variable-Reluctance Sensor Interface IC | 2 | $\pm 160 \mathrm{mV}$ | $\checkmark$ | N/A | $\checkmark$ | 7.0 V |

Air Core Motor Drivers/Gauge Drivers

| Part <br> Number | Gauges Driven |  | Input |  |  | Output |  | Features |  |  | Protection |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Major | Minor | Freq. | PWM | SPI | Current | Method | Return to Zero | UVLO | Regulator Output | Current Limit | Over Voltage | Over Temp. | Peak Transient |
| CS4121 | 1 |  | $\checkmark$ |  |  | 33 mA | Differential |  |  | $\checkmark$ |  | $\checkmark$ |  | 60 V |
| CS4122 | 1 | 2 | $\checkmark$ |  | $\checkmark$ | 80 mA | Differential |  |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | 18 V |
| CS8190 | 1 |  | $\sqrt{ }$ |  |  | 33 mA | Differential | $\checkmark$ | $\checkmark$ |  |  | $\checkmark$ |  | 60 V |
| CS8191 | 1 |  | $\checkmark$ |  |  | 55 mA | Differential |  |  |  | $\checkmark$ | $\checkmark$ |  | 60 V |

## Stepper Motor Drivers/Odometer Drivers

|  | Input |  | Modes |  | Output |  | Features |  |  | Protection |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Part Number | Sine | Square | +1 | +2 | Current | Method | UVLO | Buffered Speed Output | On-Chip <br> Flyback Diodes | Current Limit | Over Voltage | Peak Transient |
| CS4161 | $\checkmark$ | $\checkmark$ | $\checkmark$ | $\checkmark$ | 85 mA | Differential | $\checkmark$ |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | 60 V |
| CS8441 | $\checkmark$ | $\sqrt{ }$ | $\checkmark$ | $\checkmark$ | 85 mA | Differential |  |  | $\checkmark$ | $\checkmark$ | $\checkmark$ | 60 V |






## CHAPTER 2 Data Sheets

## LM285

## Micropower Voltage Reference Diodes

The LM285/LM385 series are micropower two-terminal bandgap voltage regulator diodes. Designed to operate over a wide current range of $10 \mu \mathrm{~A}$ to 20 mA , these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on-chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

The LM285/LM385 series are packaged in a low cost TO-226AA plastic case and are available in two voltage versions of 1.235 and 2.500 V as denoted by the device suffix (see Ordering Information table). The LM285 is specified over a $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ temperature range while the LM385 is rated from $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$.

The LM385 is also available in a surface mount plastic package in voltages of 1.235 and 2.500 V .

- Operating Current from $10 \mu \mathrm{~A}$ to 20 mA
- $1.0 \%, 1.5 \%, 2.0 \%$ and $3.0 \%$ Initial Tolerance Grades
- Low Temperature Coefficient
- $1.0 \Omega$ Dynamic Impedance
- Surface Mount Package Available



## LM385, B

## MICROPOWER VOLTAGE

 REFERENCE DIODESSEMICONDUCTOR TECHNICAL DATA


## Standard Application



| ORDERING INFORMATION |  |  |  |
| :---: | :---: | :---: | :---: |
| Device | Operating Temperature Range | Reverse Breakdown Voltage | Tolerance |
| $\begin{array}{\|l\|l} \hline \text { LM285D-1.2 } \\ \text { LM285Z-1.2 } \end{array}$ | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=-40^{\circ} \text { to } \\ \\ +85^{\circ} \mathrm{C} \end{gathered}$ | 1.235 V | $\pm 1.0 \%$ |
| $\begin{array}{\|l\|} \hline \text { LM285D-2.5 } \\ \text { LM285Z-2.5 } \end{array}$ |  | 2.500 V | $\pm 1.5 \%$ |
| $\begin{array}{\|l\|} \hline \text { LM385BD-1.2 } \\ \text { LM385BZ-1.2 } \end{array}$ | $\begin{gathered} \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to } \\ +70^{\circ} \mathrm{C} \end{gathered}$ | 1.235 V | $\pm 1.0 \%$ |
| $\begin{array}{\|l\|} \hline \text { LM385D-1.2 } \\ \text { LM385Z-1.2 } \end{array}$ |  | 1.235 V | $\pm 2.0 \%$ |
| $\begin{array}{\|l\|} \hline \text { LM385BD-2.5 } \\ \text { LM385BZ-2.5 } \end{array}$ |  | 2.500 V | $\pm 1.5 \%$ |
| $\begin{array}{\|l} \hline \text { LM385D-2.5 } \\ \text { LM385Z-2.5 } \end{array}$ |  | 2.500 V | $\pm 3.0 \%$ |

## LM285 LM385, B

MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Reverse Current | $\mathrm{I}_{\mathrm{R}}$ | 30 | mA |
| Forward Current | $\mathrm{I}_{\mathrm{F}}$ | 10 | mA |
| Operating Ambient Temperature Range <br> LM285 <br> LM385 | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 <br> 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature |  | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | $\mathrm{T}_{\text {stg }}$ | -65 to +150 |
| ${ }^{\circ} \mathrm{C}$ |  |  |  |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Characteristic | Symbol | LM285-1.2 |  |  | LM385-1.2/LM385B-1.2 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| ```Reverse Breakdown Voltage (I}\mp@subsup{\textrm{I}}{\textrm{min}}{}\leqslant\mp@subsup{\textrm{I}}{\textrm{R}}{}\leqslant20\textrm{mA} LM285-1.2/LM385B-1.2 TA}=\mp@subsup{T}{\mathrm{ low }}{}\mathrm{ to Thigh (Note 1) LM385-1.2 TA}=\mp@subsup{T}{\mathrm{ low to }}{\mathrm{ thigh (Note 1)}``` | $\mathrm{V}_{\text {(BR) }} \mathrm{R}$ | $\begin{aligned} & 1.223 \\ & 1.200 \end{aligned}$ | $\begin{gathered} 1.235 \\ - \\ - \end{gathered}$ | $\begin{aligned} & 1.247 \\ & 1.270 \end{aligned}$ | $\begin{aligned} & 1.223 \\ & 1.210 \\ & 1.205 \\ & 1.192 \end{aligned}$ | $\begin{gathered} 1.235 \\ - \\ 1.235 \end{gathered}$ | $\begin{aligned} & 1.247 \\ & 1.260 \\ & 1.260 \\ & 1.273 \end{aligned}$ | V |
| Minimum Operating Current $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 1) } \end{aligned}$ | $I_{\text {Rmin }}$ | - |  | $\begin{aligned} & 10 \\ & 20 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 15 \\ & 20 \\ & \hline \end{aligned}$ | $\mu \mathrm{A}$ |
| Reverse Breakdown Voltage Change with Current $\begin{aligned} & \mathrm{I}_{\mathrm{Rmin}} \leqslant \mathrm{I}_{\mathrm{R}} \leqslant 1.0 \mathrm{~mA}, \mathrm{~T}_{A}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{A}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\text { Note } 1) \\ & 1.0 \mathrm{~mA} \leqslant \mathrm{I}_{\mathrm{R}} \leqslant 20 \mathrm{~mA}, \mathrm{~T}_{A}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{A}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\text { Note } 1) \end{aligned}$ | $\Delta \mathrm{V}_{(\mathrm{BR}) \mathrm{R}}$ | - |  | $\begin{aligned} & 1.0 \\ & 1.5 \\ & 10 \\ & 20 \end{aligned}$ | - | - - - | $\begin{aligned} & 1.0 \\ & 1.5 \\ & 20 \\ & 25 \end{aligned}$ | mV |
| Reverse Dynamic Impedance $\mathrm{I}_{\mathrm{R}}=100 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | Z |  | 0.6 | - | - | 0.6 | - | W |
| Average Temperature Coefficient $10 \mu \mathrm{~A} \leqslant \mathrm{I}_{\mathrm{R}} \leqslant 20 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\text { Note } 1)$ | $\Delta \mathrm{V}_{(\mathrm{BR})} / \Delta \mathrm{T}$ | - | 80 | - | - | 80 | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| Wideband Noise (RMS) $\mathrm{I}_{\mathrm{R}}=100 \mu \mathrm{~A}, 10 \mathrm{~Hz} \leqslant \mathrm{f} \leqslant 10 \mathrm{kHz}$ | n | - | 60 | - | - | 60 | - | $\mu \mathrm{V}$ |
| Long Term Stability $\mathrm{I}_{\mathrm{R}}=100 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \pm 0.1^{\circ} \mathrm{C}$ | S | - | 20 | - | - | 20 | - | $\begin{aligned} & \mathrm{ppm} / \\ & \mathrm{kHR} \end{aligned}$ |

## LM285 LM385, B

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Characteristic | Symbol | LM285-2.5 |  |  | LM385-2.5/LM385B-2.5 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| ```Reverse Breakdown Voltage (I IRmin }\leqslant\mp@subsup{I}{R}{}\leqslant20 mA LM285-2.5/LM385B-2.5 TA}=\mp@subsup{T}{\mathrm{ low }}{}\mathrm{ to T Thigh (Note 1) LM385-2.5 TA}=\mp@subsup{T}{\mathrm{ low }}{}\mathrm{ to T Thigh (Note 1)``` | $\mathrm{V}_{(\mathrm{BR}) \mathrm{R}}$ | $\begin{gathered} 2.462 \\ 2.415 \\ - \\ - \end{gathered}$ | $\begin{gathered} 2.5 \\ - \\ - \end{gathered}$ | $\begin{aligned} & 2.538 \\ & 2.585 \end{aligned}$ | $\begin{aligned} & 2.462 \\ & 2.436 \\ & 2.425 \\ & 2.400 \end{aligned}$ | $\begin{gathered} 2.5 \\ - \\ 2.5 \end{gathered}$ | $\begin{aligned} & 2.538 \\ & 2.564 \\ & 2.575 \\ & 2.600 \end{aligned}$ | V |
| Minimum Operating Current $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 1) } \end{aligned}$ | $\mathrm{I}_{\text {Rmin }}$ |  | 13 | $\begin{aligned} & 20 \\ & 30 \end{aligned}$ | - |  | $\begin{aligned} & 20 \\ & 30 \end{aligned}$ | $\mu \mathrm{A}$ |
| Reverse Breakdown Voltage Change with Current $\begin{aligned} & \mathrm{I}_{\mathrm{Rmin}} \leqslant \mathrm{I}_{\mathrm{R}} \leqslant 1.0 \mathrm{~mA}, \mathrm{~T}_{A}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{A}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\text { Note } 1) \\ & 1.0 \mathrm{~mA} \leqslant \mathrm{I}_{\mathrm{R}} \leqslant 20 \mathrm{~mA}, \mathrm{~T}_{A}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{A}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\text { Note } 1) \end{aligned}$ | $\Delta \mathrm{V}_{(\mathrm{BR}) \mathrm{R}}$ | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | - - - | $\begin{aligned} & 1.0 \\ & 1.5 \\ & 10 \\ & 20 \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.5 \\ & 20 \\ & 25 \end{aligned}$ | mV |
| Reverse Dynamic Impedance $\mathrm{I}_{\mathrm{R}}=100 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | Z |  | 0.6 | - | - | 0.6 | - | W |
| Average Temperature Coefficient $20 \mu \mathrm{~A} \leqslant \mathrm{I}_{\mathrm{R}} \leqslant 20 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ (Note 1) | $\Delta \mathrm{V}_{(\mathrm{BR})} / \Delta \mathrm{T}$ | - | 80 | - | - | 80 | - | ppm/ ${ }^{\circ} \mathrm{C}$ |
| Wideband Noise (RMS) $\mathrm{I}_{\mathrm{R}}=100 \mu \mathrm{~A}, 10 \mathrm{~Hz} \leqslant \mathrm{f} \leqslant 10 \mathrm{kHz}$ | n | - | 120 | - | - | 120 | - | $\mu \mathrm{V}$ |
| Long Term Stability $\mathrm{I}_{\mathrm{R}}=100 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \pm 0.1^{\circ} \mathrm{C}$ | S | - | 20 | - | - | 20 | - | $\begin{aligned} & \hline \mathrm{ppm} / \\ & \mathrm{kHR} \end{aligned}$ |

NOTES: $1 . \mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}$ for LM285-1.2, LM285-2.5
$\mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$ for LM285-1.2, LM285-2.5
$=0^{\circ} \mathrm{C}$ for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5
$=+70^{\circ} \mathrm{C}$ for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

## LM285 LM385, B

TYPICAL PERFORMANCE CURVES FOR LM285-1.2/385-1.2/385B-1.2

Figure 1. Reverse Characteristics


Figure 3. Forward Characteristics


Figure 5. Noise Voltage


Figure 2. Reverse Characteristics


Figure 4. Temperature Drift


Figure 6. Response Time


## LM285 LM385, B

Figure 7. Reverse Characteristics


Figure 9. Forward Characteristics


Figure 11. Noise Voltage


Figure 8. Reverse Characteristics


Figure 10. Temperature Drift


Figure 12. Response Time


## NCP100

## Sub 1.0 V Precision Adjustable Shunt Regulator

The NCP100 is a precision low voltage shunt regulator that is programmable over a voltage range of 0.9 V to 6.0 V . This device features a guaranteed reference accuracy of $\pm 1.7 \%$ at $25^{\circ} \mathrm{C}$ and $\pm 2.6 \%$ over the entire temperature range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$. The NCP100 exhibits a sharp low current turn-on characteristic with a low dynamic impedance of $0.20 \Omega$ over an operating current range of $100 \mu \mathrm{~A}$ to 20 mA . These characteristics make this device an ideal replacement for zener diodes in numerous application circuits that require a precise low voltage reference. When combined with an optocoupler, the NCP100 can be used as an error amplifier for controlling the feedback loop in isolated low output voltage ( 2.3 V ) switching power supplies. This device is available in an economical space saving TSOP-5 package.

## Features

- Programmable Output Voltage Range of 0.9 V to 6.0 V
- Voltage Reference Tolerance of $\pm 1.7 \%$
- Sharp Low Current Turn-ON Characteristic
- Low Dynamic Output Impedance of $0.2 \Omega$ from $100 \mu \mathrm{~A}$ to 20 mA
- Wide Operating Current Range of $80 \mu \mathrm{~A}$ to 20 mA
- Space Saving TSOP-5 Package


## Applications

- Reference for Single Cell Alkaline, NiCD and NiMH Applications
- Low Output Voltage (2.3 V) Switching Power Supply Error Amp
- Battery Powered Consumer Products
- Portable Test Equipment and Instrumentation


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TSOP-5
SN SUFFIX
CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM

$Y Y=$ Year
WW = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP100SNT1 | TSOP-5 | 3000 Units / 7" Reel |

Figure 1. Symbol
Figure 2. Representative Block Diagram

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Cathode to Anode Voltage (Note 1) | $\mathrm{V}_{\text {KA }}$ | 7.0 | V |
| Cathode Current Range, Continuous (Note 2) | $\mathrm{I}_{\mathrm{K}}$ | -20 to 25 | mA |
| Reference Input Current Range, Continuous (Note 1) | $\mathrm{I}_{\text {ref }}$ | -0.05 to 2.0 | mA |
| Thermal Resistance Junction to Air | $\mathrm{R}_{\text {өJA }}$ | 225 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |

## RECOMMENDED OPERATING CONDITIONS

| Condition | Symbol | Min | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Cathode to Anode Voltage Range | $\mathrm{V}_{\text {KA }}$ | 0.9 | 6.0 | V |
| Cathode Current Range | $\mathrm{I}_{\mathrm{K}}$ | 0.1 | 20 | mA |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 4000 V per JESD-22, Method A114B.
Machine Model Method 400 V .
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Reference Voltage }\left(l_{\mathrm{KA}}=10 \mathrm{~mA},\right. \text { Figure 3) } \\ & V_{\mathrm{KA}}=0.9 \mathrm{~V} \\ & T_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & T_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & T_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{KA}}=1.0 \mathrm{~V} \\ & T_{A}=25^{\circ} \mathrm{C} \\ & T_{A}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & T_{A}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 0.684 \\ & 0.682 \\ & 0.678 \\ & 0.686 \\ & 0.684 \\ & 0.680 \end{aligned}$ | $\begin{gathered} 0.696 \\ - \\ - \\ 0.698 \end{gathered}$ | $\begin{aligned} & 0.708 \\ & 0.710 \\ & 0.714 \\ & 0.710 \\ & 0.712 \\ & 0.716 \end{aligned}$ | V |
| Reference Input Voltage Change Over Temperature $\mathrm{V}_{\mathrm{KA}}=1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$, Figure 3 (Notes 3,4 ) | $\Delta \mathrm{V}_{\text {ref }}$ | - | 1.0 | 12 | mV |
| Reference Input Voltage Change Over Programmed Cathode Voltage $\begin{aligned} & \left(\mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \text { Figure } 3\right) \\ & \mathrm{V}_{\mathrm{KA}}=0.9 \mathrm{~V} \text { to } 1.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{KA}}=1.0 \mathrm{~V} \text { to } 6.0 \mathrm{~V} \end{aligned}$ | Regline | $\begin{gathered} -3.0 \\ 0 \end{gathered}$ | $\begin{aligned} & 0.2 \\ & 6.7 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 12 \end{aligned}$ | mV |
| Ratio of Reference Input Voltage Change to Cathode Voltage Change $\mathrm{V}_{\mathrm{KA}}=0.9 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}$, Figure 3 | $\frac{\Delta \mathrm{V}_{\text {ref }}}{\Delta \mathrm{V}_{\mathrm{KA}}}$ | - | 1.3 | 2.4 | $\mathrm{mV} / \mathrm{V}$ |
| Reference Input Current ( $\mathrm{V}_{\mathrm{KA}}=1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}$ ) | $\mathrm{I}_{\text {ref }}$ | -100 | -30 | 100 | nA |
| Minimum Cathode Current for Regulation | $\mathrm{I}_{\mathrm{K} \text { (min) }}$ | - | 80 | - | $\mu \mathrm{A}$ |
| Cathode Off-State Current ( $\left.\mathrm{V}_{\text {KA }}=6.0 \mathrm{~V}, \mathrm{~V}_{\text {ref }}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{K} \text { (off) }}$ | - | 70 | 90 | $\mu \mathrm{A}$ |
| Dynamic Output Impedance <br> $\mathrm{V}_{\mathrm{KA}}=1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{K}}=100 \mu \mathrm{~A}$ to $20 \mathrm{~mA}, \mathrm{f} \leq 1.0 \mathrm{kHz}$, Figure 3 | $\left\|Z_{K A}\right\|$ | - | 0.2 | - | $\Omega$ |

3. Low duty cycle pulse techniques are used during testing to maintain the junction temperatures as close to ambient as possible.
4. The $\Delta \mathrm{V}_{\text {ref }}$ parameter is defined as the difference between the maximum and minimum values obtained over the ambient temperature range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$.



Figure 3. General Test Circuit


Figure 4. Test Circuit for Reference Input Voltage Change vs. Cathode Voltage


Figure 6. Test Circuit for Spectral Noise Density


Figure 7. Reference Input Voltage Change vs. Ambient Temperature


Figure 8. Cathode Voltage Change vs. Ambient Temperature

NCP100


Figure 9. Cathode Current vs. Cathode Voltage


Figure 11. Reference Input Voltage Change vs. Cathode Voltage


Figure 10. Cathode Current vs. Cathode Voltage


Figure 12. Dynamic Impedance vs. Frequency


Figure 13. Small-Signal Voltage Gain and Phase vs. Frequency


Figure 14. Reference Voltage vs. Cathode Current for $V_{K A}=0.9 \mathrm{~V}$

NCP100


Figure 15. Reference Voltage vs. Cathode Current for $V_{K A}=1.0 \mathrm{~V}$


Figure 17. Reference Voltage vs. Cathode Current


Figure 19. Stability Boundary Conditions

Figure 16. Reference Voltage vs. Cathode Current for $V_{K A}=6.0 \mathrm{~V}$


Figure 18. Spectral Noise Density


Figure 20. Turn-On Time

## APPLICATIONS INFORMATION

The NCP100 is an adjustable shunt regulator similar to the industry standard 431-type regulators. Each device is laser trimmed at wafer probe to allow for tight reference accuracy and low reference voltage shift over the full operating temperature range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ (Figure 7).

The nominal value for the reference is 0.698 V . This lower voltage allows the device to be used in low voltage applications where the traditional 1.25 V and 2.5 V references are not suitable.


Figure 21. Typical Application Circuit
The typical application circuit for this device is shown in Figure 21. The cathode voltage can be programmed between 0.9 V to 6.0 V to allow for proper operation by setting the R1/R2 resistor divider network values. The following equation can be used in calculating the cathode voltage $\left(\mathrm{V}_{\mathrm{KA}}\right)$. Note, if $\mathrm{V}_{\mathrm{KA}}$ is known then the ratio of R 1 and R 2 can be determined from this equation as well.

$$
V_{K A}=V_{\text {ref }}\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right)+I_{\text {ref }} \mathrm{R} 1
$$

The table below shows the required $\mathrm{R} 1 / \mathrm{R} 2$ values using $1.0 \%$ resistors for commonly used voltages.

| $\mathbf{V}_{\mathbf{K A}}$ <br> $(\mathrm{V})$ | $\mathbf{R 1}$ <br> $(\mathbf{k} \Omega)$ | $\mathbf{R 2}$ <br> $(\mathrm{k} \boldsymbol{\Omega})$ |
| :---: | :---: | :---: |
| 0.9 | 30 | 100 |
| 1.0 | 43.2 | 100 |
| 1.8 | 158 | 100 |
| 3.3 | 374 | 100 |
| 5.0 | 619 | 100 |
| 6.0 | 750 | 100 |

Because the error amplifier is a CMOS design the value of $\mathrm{I}_{\text {ref }}$ is extremely low allowing it to be neglected for most applications. The low $\mathrm{I}_{\text {ref }}$ also allows for higher R1 and R2 values keeping current consumption very low.

The NCP100 is especially well suited for lower voltage applications, particularly at $\mathrm{V}_{\mathrm{KA}}=1.0 \mathrm{~V}$. As is seen in Figures 7 and 8, this device exhibits excellent cathode and reference voltage flatness across the $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ temperature range.
In Figure 21, the input resistor $\left(\mathrm{R}_{\text {in }}\right)$ is nominally set to $1.0 \mathrm{k} \Omega$. For proper operation, once $\mathrm{V}_{\mathrm{in}}, \mathrm{R} 1$ and R 2 are set,
the resistance and power value of $\mathrm{R}_{\text {in }}$ can be determined by the following equation.

$$
\mathrm{R}_{\text {in }}=\frac{\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{KA}}}{\mathrm{I}_{\mathrm{K}}+\mathrm{I}_{\mathrm{L}}+\left(\frac{\mathrm{V}_{\mathrm{KA}}}{\mathrm{R}_{1}+\mathrm{R}_{2}}\right)}
$$

The maximum current that will flow through $\mathrm{R}_{\text {in }}$ must be determined. This is the sum of the maximum values of cathode current, resistor divider network current, and load current. With $\mathrm{V}_{\mathrm{in}}$, set, the difference $\left(\mathrm{V}_{\mathrm{in}}-\mathrm{V}_{\mathrm{KA}}\right)$ is now constant. This value is divided by the maximum current calculated above to arrive at the value of $R_{i n}$. Once the value of $R_{\text {in }}$ is calculated, it's minimum power rating is easily derived by:

$$
P_{\text {in }}=\left(l_{\text {in }}\right)^{2} R_{\text {in }}
$$

Once these values are determined, it should be verified that the minimum and maximum values of $\mathrm{I}_{\mathrm{K}}$ are within the recommended range of 0.1 mA to 20 mA under the worst case conditions.
For stability, the NCP100 requires an output capacitor between the cathode and anode. Figure 19 shows the capacitance boundary values required for stable operation across the $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ temperature range. The goal is to remain to the right of the curve for any programmed cathode voltages. For example, if the $\mathrm{V}_{\mathrm{KA}}$ is programmed to 1.0 V , then a load capacitor value of $3.0 \mu \mathrm{~F}$ or greater would be selected. The load capacitor's equivalent series resistance, ESR, should be less than $4.0 \Omega$. Both the capacitance and ESR values should be checked across the anticipated application temperature range to insure that the values meet the requirements stated above.


Figure 22. Negative Dynamic Impedance Circuit
One unique use for the NCP100 is that it can be configured for negative dynamic impedance as shown in Figure 22. This circuit is equivalent to Figure 21 with the addition of a small value resistor $\mathrm{R}_{\text {comp }}$ in the cathode circuit. The regulated voltage output remains across the NCP100 cathode and anode leads. The voltage programming and stability requirements remain the same as in the typical application shown in Figure 21.

## NCP100

The circuit performs the same as the one in Figure 21 with the exception of the effects of $R_{\text {comp }}$. As $I_{K}$ increases, the voltage across $\mathrm{R}_{\text {comp }}$ also increases by:

$$
\mathrm{V}_{\mathrm{comp}}=\mathrm{I}_{\mathrm{KA}} \mathrm{R}_{\mathrm{comp}}
$$

$\mathrm{V}_{\text {comp }}$ effectively adjusts the NCP100 programmed $\mathrm{V}_{\text {KA }}$ voltage slightly down since the R1/R2 voltage divider will try to hold the point it is connected to at the programmed voltage. The regulator $\mathrm{V}_{\mathrm{KA}}$ will now be lowered by the value of the $\mathrm{V}_{\text {comp }}$. This effect can compensate for the NCP100's intrinsic positive impedance versus cathode current ( $\mathrm{I}_{\mathrm{K}}$ ) to allow for $0 \Omega$ or even a negative dynamic impedance.

Figure 23 shows this phenomenon for a program voltage of 1.0 V . The NCP100 intrinsic positive dynamic impedance


Figure 23. Cathode Current vs. Cathode Voltage for Programmed $\mathrm{V}_{\mathrm{KA}}=1.0 \mathrm{~V}$
response is the $\mathrm{R}_{\text {comp }}=0 \Omega$ curve. A $0 \Omega$ dynamic impedance regulator response is realized with $\mathrm{R}_{\text {comp }}=$ $0.15 \Omega$. Negative dynamic impedance responses are achieved with $\mathrm{R}_{\text {comp }}>0.15 \Omega$.

Figure 24 shows the characteristic at a programmed $\mathrm{V}_{\mathrm{KA}}$ of 6.0 V . The $0 \Omega$ dynamic impedance value corresponds to $\mathrm{R}_{\text {comp }}=2.9 \Omega$.
Figure 25 shows the dynamic impedance versus cathode compensation resistance for programmed voltages of 1.0 V , 3.3 V and 6.0 V . It can be seen that any value up to the positive intrinsic dynamic impedance of the NCP100 can be realized. The other limit is that with a high enough negative dynamic impedance, the NCP100 V may drop below the minimum operating $\mathrm{V}_{\mathrm{KA}}$ voltage of 0.9 V , which can result in unpredictable performance.


Figure 24. Cathode Current vs. Cathode Voltage for Programmed $\mathrm{V}_{\mathrm{KA}}=6.0 \mathrm{~V}$


Figure 25. Dynamic Impedance vs. Cathode Compensation Resistance


Figure 26. High Current Shunt Regulator


Figure 27. Low Dropout Series Pass Regulator


Figure 28. Offline Converter with Isolated DC Output

The circuit in Figure 28 uses the NCP100 as a compensated amplifier for controlling the feedback loop of an isolated output line powered converter. This device allows the converter to directly regulate the output voltage at a significantly lower level than obtainable with the
common TL431 device family. The output voltage is programmed by the resistors R1 and R2. The minimum regulated DC output is limited to the sum of the lowest allowable cathode to anode voltage ( 0.9 V ) and the forward drop of the optocoupler light emitting diode (1.4 V).

## INFORMATION FOR USING THE TSOP-5 SURFACE MOUNT PACKAGE <br> MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5

## TLV431A

## Low Voltage Precision Adjustable Shunt Regulator

The TLV431A series are precision low voltage shunt regulators that are programmable over a wide voltage range of 1.24 V to 16 V . These series feature a guaranteed reference accuracy of $\pm 1.0 \%$ at $25^{\circ} \mathrm{C}$ and $\pm 2.0 \%$ over the entire industrial temperature range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$. These devices exhibit a sharp low current turn-on characteristic with a low dynamic impedance of $0.20 \Omega$ over an operating current range of $100 \mu \mathrm{~A}$ to 20 mA . This combination of features makes this series an excellent replacement for zener diodes in numerous applications circuits that require a precise reference voltage. When combined with an optocoupler, the TLV431A can be used as an error amplifier for controlling the feedback loop in isolated low output voltage ( 3.0 V to 3.3 V ) switching power supplies. These devices are available in economical TSOP-5 and TO-92 packages.

## Features

- Programmable Output Voltage Range of 1.24 V to 16 V
- Voltage Reference Tolerance $\pm 1.0 \%$
- Sharp Low Current Turn-On Characteristic
- Low Dynamic Output Impedance of $0.20 \Omega$ from $100 \mu \mathrm{~A}$ to 20 mA
- Wide Operating Current Range of $50 \mu \mathrm{~A}$ to 20 mA
- Micro Miniature TSOP-5 and TO-92 Packages


## Applications

- Low Output Voltage (3.0 V to 3.3 V) Switching Power Supply Error Amplifier
- Adjustable Voltage or Current Linear and Switching Power Supplies
- Voltage Monitoring
- Current Source and Sink Circuits
- Analog and Digital Circuits Requiring Precision References
- Low Voltage Zener Diode Replacements


Figure 1. Representative Block Diagram

## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| TLV431ALP | TO-92 | $6000 /$ Box |
| TLV431ALPRA | TO-92 | $2000 /$ Tape \& Reel |
| TLV431ALPRE | TO-92 | $2000 /$ Tape \& Reel |
| TLV431ALPRM | TO-92 | $2000 /$ Ammo Pack |
| TLV431ALPRP | TO-92 | $2000 /$ Ammo Pack |
| TLV431ASNT1 | TSOP-5 | $3000 /$ Tape \& Reel |

## TLV431A



The device contains 13 active transistors.
Figure 2. Representaive Schematic Diagram

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Cathode to Anode Voltage | $\mathrm{V}_{\text {KA }}$ | 18 | V |
| Cathode Current Range, Continuous (Note 1) | $\mathrm{I}_{\mathrm{K}}$ | -20 to 25 | mA |
| Reference Input Current Range, Continuous | $\mathrm{I}_{\text {ref }}$ | -0.05 to 10 | mA |
| Thermal Characteristics |  |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| LP Suffix Package |  |  |  |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {өJA }}$ | 178 |  |
| Thermal Resistance, Junction-to-Case | $\mathrm{R}_{\theta \mathrm{\theta JC}}$ | 83 |  |
| SN Suffix Package | $\mathrm{R}_{\text {өJA }}$ | 226 |  |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range (Note 1) | $\mathrm{T}_{\text {stg }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  |  |  |

1. Maximum package power dissipation limits must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .

## RECOMMENDED OPERATING CONDITIONS

| Condition | Symbol | Min | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Cathode to Anode Voltage | $\mathrm{V}_{\mathrm{KA}}$ | $\mathrm{V}_{\text {ref }}$ | 16 | V |
| Cathode Current | $\mathrm{I}_{\mathrm{K}}$ | 0.1 | 20 | mA |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Reference Voltage (Figure 1) } \\ & \left(V_{K A}=V_{\text {ref }}, I_{K}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }},\right. \text { Note 2) } \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 1.228 \\ & 1.215 \end{aligned}$ | 1.240 | $\begin{aligned} & 1.252 \\ & 1.265 \end{aligned}$ | V |
| Reference Input Voltage Deviation Over Temperature (Figure 1) $\left(\mathrm{V}_{\mathrm{KA}}=\mathrm{V}_{\text {ref }}, \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$, Notes 2, 3) | $\Delta \mathrm{V}_{\text {ref }}$ | - | 7.2 | 20 | mV |
| Ratio of Reference Input Voltage Change to Cathode Voltage Change (Figure 2) $\left(\mathrm{V}_{\mathrm{KA}}=\mathrm{V}_{\text {ref }} \text { to } 16 \mathrm{~V}, \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}\right)$ | $\frac{\Delta \mathrm{V}_{\text {ref }}}{\Delta \mathrm{V}_{\mathrm{KA}}}$ | - | -0.6 | -1.5 | $\frac{\mathrm{mV}}{\mathrm{~V}}$ |
| Reference Terminal Current (Figure 2) ( $\mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{R} 1=10 \mathrm{k} \Omega, \mathrm{R} 2=\mathrm{open}$ ) | $\mathrm{I}_{\text {ref }}$ | - | 0.15 | 0.3 | $\mu \mathrm{A}$ |
| Reference Input Current Deviation Over Temperature (Figure 2) $\left(\mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{R} 1=10 \mathrm{k} \Omega, \mathrm{R} 2=\right.$ Open, Notes 2,3 ) | $\Delta \mathrm{I}_{\text {ref }}$ | - | 0.04 | 0.08 | $\mu \mathrm{A}$ |
| Minimum Cathode Current for Regulation (Figure 1) | $\mathrm{I}_{\mathrm{K}(\text { min })}$ | - | 55 | 80 | $\mu \mathrm{A}$ |
| Off-State Cathode Current (Figure 3) $\begin{aligned} & \left(V_{K A}=6.0 \mathrm{~V}, \mathrm{~V}_{\text {ref }}=0\right) \\ & \left(\mathrm{V}_{\mathrm{KA}}=16 \mathrm{~V}, \mathrm{~V}_{\text {ref }}=0\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{K} \text { (off) }}$ | - | $\begin{gathered} 0.01 \\ 0.012 \end{gathered}$ | $\begin{aligned} & 0.04 \\ & 0.05 \end{aligned}$ | $\mu \mathrm{A}$ |
| Dynamic Impedance (Figure 1) $\left(\mathrm{V}_{\mathrm{KA}}=\mathrm{V}_{\text {ref }}, \mathrm{I}_{\mathrm{K}}=0.1 \mathrm{~mA} \text { to } 20 \mathrm{~mA}, \mathrm{f} \leq 1.0 \mathrm{kHz} \text {, Note } 4\right)$ | $\left\|Z_{K A}\right\|$ | - | 0.25 | 0.4 | $\Omega$ |

2. Ambient temperature range: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=85^{\circ} \mathrm{C}$.
3. The deviation parameters $\Delta \mathrm{V}_{\text {ref }}$ and $\Delta \mathrm{I}_{\text {ref }}$ are defined as the difference between the maximum value and minimum value obtained over the full operating ambient temperature range that applied.


The average temperature coefficient of the reference input voltage, $\alpha \mathrm{V}_{\text {ref }}$ is defined as:

$$
\alpha \mathrm{V}_{\text {ref }}\left(\frac{\mathrm{ppm}}{{ }^{\circ} \mathrm{C}}\right)=\frac{\left(\frac{\left(\Delta \mathrm{V}_{\text {ref }}\right)}{\mathrm{V}_{\text {ref }}\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)} \times 10^{6}\right)}{\Delta \mathrm{T}_{\mathrm{A}}}
$$

$\alpha \mathrm{V}_{\text {ref }}$ can be positive or negative depending on whether $\mathrm{V}_{\text {ref }}$ Min or $\mathrm{V}_{\text {ref }}$ Max occurs at the lower ambient temperature, refer to Figure 6. Example: $\Delta \mathrm{V}_{\text {ref }}=7.2 \mathrm{mV}$ and the slope is positive,

$$
\begin{aligned}
& \mathrm{V}_{\text {ref }} @ 25^{\circ} \mathrm{C}=1.241 \mathrm{~V} \\
& \Delta \mathrm{~T}_{\mathrm{A}}=125^{\circ} \mathrm{C} \\
& \\
& \qquad \alpha \mathrm{~V}_{\text {ref }}\left(\frac{\mathrm{ppm}}{{ }^{\circ} \mathrm{C}}\right)=\frac{\frac{0.0072}{1.241} \times 10^{6}}{125}=46 \mathrm{ppm} /{ }^{\circ} \mathrm{C}
\end{aligned}
$$

4. The dynamic impedance $Z_{K A}$ is defined as:

$$
\left|Z_{K A}\right|=\frac{\Delta V_{K A}}{\Delta I_{K}}
$$

When the device is operating with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is given by:

$$
\left|Z_{K A^{\prime}}\right|=\left|Z_{K A}\right| \times\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right)
$$



Figure 3. Test Circuit for $\mathrm{V}_{\mathrm{KA}}=\mathrm{V}_{\text {ref }}$


Figure 4. Test Circuit for $V_{K A}>V_{\text {ref }}$


Figure 5. Test Circuit for $\mathbf{I}_{\mathrm{K} \text { (off) }}$


Figure 6. Cathode Current vs. Cathode Voltage


Figure 7. Cathode Current vs. Cathode Voltage


Figure 8. Reference Input Voltage versus Ambient Temperature


Figure 9. Reference Input Current versus Ambient Temperature


Figure 10. Reference Input Voltage Change versus Cathode Voltage


Figure 12. Off-State Cathode Current versus Ambient Temperature


Figure 14. Dynamic Impedance versus Ambient Temperature


Figure 11. Off-State Cathode Current versus Cathode Voltage


Figure 13. Dynamic Impedance versus Frequency


Figure 15. Open-Loop Voltage Gain versus Frequency


Figure 16. Spectral Noise Density


Figure 18. Stability Boundary Conditions

Figure 17. Pulse Response


Figure 19. Test Circuit for Figure 16

## TLV431A

## TYPICAL APPLICATIONS



Figure 20. Shunt Regulator


$$
\begin{gathered}
V_{\text {out }}=\left(1+\frac{R 1}{R 2}\right) V_{\text {ref }} \\
V_{\text {out }(\min )}=V_{\text {ref }}+5.0 \mathrm{~V}
\end{gathered}
$$

Figure 22. Output Control for a Three Terminal Fixed Regulator


Figure 21. High Current Shunt Regulator


Figure 23. Series Pass Regulator

## TLV431A



Figure 24. Constant Current Source


Figure 25. Constant Current Sink


Figure 26. TRIAC Crowbar


Figure 27. SCR Crowbar

## TLV431A


L.E.D. indicator is 'ON' when $\mathrm{V}_{\text {in }}$ is between the upper and lower limits,

$$
\begin{aligned}
& \text { Lower limit }=\left(1+\frac{R 1}{R 2}\right) V_{\text {ref }} \\
& \text { Upper limit }=\left(1+\frac{R 3}{R 4}\right) V_{\text {ref }}
\end{aligned}
$$

Figure 28. Voltage Monitor


| $\mathbf{V}_{\text {in }}$ | $\mathbf{V}_{\text {out }}$ |
| :---: | :---: |
| $<\mathrm{V}_{\text {ref }}$ | $\mathrm{V}_{+}$ |
| $>\mathrm{V}_{\text {ref }}$ | $\approx 0.74 \mathrm{~V}$ |

Figure 29. Single-Supply Comparator with Temperature-Compensated Threshold


Figure 30. Linear Ohmmeter


Figure 31. Simple 400 mW Phono Amplifier

## TLV431A



Figure 32. Isolated Output Line Powered Switching Power Supply
The above circuit shows the TLV431A as a compensated amplifier controlling the feedback loop of an isolated output line powered switching regulator. The output voltage is programmed to 3.3 V by the resistors values selected for R1 and R2. The minimum output voltage that can be programmed with this circuit is 2.64 V , and is limited by the sum of the reference voltage ( 1.24 V ) and the forward drop of the optocoupler light emitting diode ( 1.4 V ). Capacitor C 1 provides loop compensation.

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5
(Footprint Compatible with SOT-23-5)

## Programmable Precision References

The TL431, A, B integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from $\mathrm{V}_{\text {ref }}$ to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of $0.22 \Omega$. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: $\pm 0.4 \%$, Typ @ $25^{\circ} \mathrm{C}$ (TL431B)
- Low Dynamic Output Impedance, $0.22 \Omega$ Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of $50 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage

ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
| :---: | :---: | :---: |
| TL431CLP, ACLP, BCLP | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | TO-92 |
| TL431CP, ACP, BCP |  | Plastic |
| TL431CDM, ACDM, BCDM |  | MICRO-8 |
| TL431CD, ACD, BCD |  | SOP-8 |
| TL431ILP, AILP, BILP | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | TO-92 |
| TL431IP, AIP, BIP |  | Plastic |
| TL431IDM, AIDM, BIDM |  | MICRO-8 |
| TL431ID, AID, BID |  | SOP-8 | Series

## PROGRAMMABLE PRECISION REFERENCES

SEMICONDUCTOR TECHNICAL DATA


SOP-8 is an internally modified SO-8 package. Pins 2, 3,6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases power nal dimensions of the standard SO-8 package.

## TL431, A, B Series

Representative Schematic Diagram
Component values are nominal


MAXIMUM RATINGS (Full operating ambient temperature range applies, unless
otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Cathode to Anode Voltage | VKA | 37 | V |
| Cathode Current Range, Continuous | $I_{K}$ | -100 to +150 | mA |
| Reference Input Current Range, Continuous | $\mathrm{I}_{\text {ref }}$ | -0.05 to +10 | mA |
| Operating Junction Temperature | TJ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range TL431I, TL431AI, TL431BI TL431C, TL431AC, TL431BC | $\mathrm{T}_{\mathrm{A}}$ | $\begin{gathered} -40 \text { to }+85 \\ 0 \text { to }+70 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Total Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Derate above $25^{\circ} \mathrm{C}$ Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package DM Suffix Plastic Package | $P_{\text {D }}$ | $\begin{aligned} & 0.70 \\ & 1.10 \\ & 0.52 \end{aligned}$ | W |
| Total Power Dissipation @ $T_{C}=25^{\circ} \mathrm{C}$ Derate above $25^{\circ} \mathrm{C}$ Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package | $P_{\text {D }}$ | $\begin{aligned} & 1.5 \\ & 3.0 \end{aligned}$ | W |

NOTE: ESD data available upon request.
RECOMMENDED OPERATING CONDITIONS

| Condition | Symbol | Min | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Cathode to Anode Voltage | $\mathrm{V}_{\mathrm{KA}}$ | $\mathrm{V}_{\text {ref }}$ | 36 | V |
| Cathode Current | $\mathrm{I}_{\mathrm{K}}$ | 1.0 | 100 | mA |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | D, LP Suffix <br> Package | P Suffix <br> Package | DM Suffix <br> Package | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta J A}$ | 178 | 114 | 240 |  |
| Thermal Resistance, Junction-to-Case | $R_{\theta J C}$ | 83 | 41 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## TL431, A, B Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | TL4311 |  |  | TL431C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Reference Input Voltage (Figure 1) $\begin{aligned} & \mathrm{V}_{\mathrm{KA}}=\mathrm{V}_{\text {ref, },} \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 1) } \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 2.44 \\ & 2.41 \end{aligned}$ | 2.495 - | $\begin{aligned} & 2.55 \\ & 2.58 \end{aligned}$ | $\begin{gathered} 2.44 \\ 2.423 \end{gathered}$ | $2.495$ | $\begin{aligned} & 2.55 \\ & 2.567 \end{aligned}$ | V |
| Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) $V_{K A}=V_{\text {ref }}, I_{K}=10 \mathrm{~mA}$ | $\Delta \mathrm{V}_{\text {ref }}$ | - | 7.0 | 30 | - | 3.0 | 17 | mV |
| Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $\begin{gathered} \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA} \text { (Figure 2), } \\ \Delta \mathrm{V}_{\mathrm{KA}}=10 \mathrm{~V} \text { to } \mathrm{V}_{\text {ref }} \\ \Delta \mathrm{V}_{\mathrm{KA}}=36 \mathrm{~V} \text { to } 10 \mathrm{~V} \end{gathered}$ | $\frac{\Delta V_{\text {ref }}}{\Delta V_{\mathrm{KA}}}$ | - | $\begin{array}{r} -1.4 \\ -1.0 \\ \hline \end{array}$ | $\begin{aligned} & -2.7 \\ & -2.0 \end{aligned}$ | - | $\begin{aligned} & -1.4 \\ & -1.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & -2.7 \\ & -2.0 \end{aligned}$ | $\mathrm{mV} / \mathrm{V}$ |
| $\begin{aligned} & \text { Reference Input Current (Figure 2) } \\ & \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{R} 1=10 \mathrm{k}, \mathrm{R} 2=\infty \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 1) } \end{aligned}$ | $I_{\text {ref }}$ | - |  | $\begin{aligned} & 4.0 \\ & 6.5 \end{aligned}$ |  |  | $\begin{aligned} & 4.0 \\ & 5.2 \end{aligned}$ | $\mu \mathrm{A}$ |
| Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) $\mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{R} 1=10 \mathrm{k}, \mathrm{R} 2=\infty$ | $\Delta \mathrm{l}_{\text {ref }}$ | - | 0.8 | 2.5 | - | 0.4 | 1.2 | $\mu \mathrm{A}$ |
| Minimum Cathode Current For Regulation $V_{K A}=V_{\text {ref }}$ (Figure 1) | $I_{\text {min }}$ | - | 0.5 | 1.0 | - | 0.5 | 1.0 | mA |
| Off-State Cathode Current (Figure 3) $V_{K A}=36 \mathrm{~V}, \mathrm{~V}_{\text {ref }}=0 \mathrm{~V}$ | $\mathrm{I}_{\text {off }}$ | - | 260 | 1000 | - | 260 | 1000 | nA |
| $\begin{aligned} & \text { Dynamic Impedance (Figure 1, Note 3) } \\ & V_{\mathrm{KA}}=\mathrm{V}_{\text {ref },} \Delta \mathrm{l}_{\mathrm{K}}=1.0 \mathrm{~mA} \text { to } 100 \mathrm{~mA} \\ & \mathrm{f} \leq 1.0 \mathrm{kHz} \end{aligned}$ | $\left\|Z_{\text {KA }}\right\|$ | - | 0.22 | 0.5 | - | 0.22 | 0.5 | $\Omega$ |

NOTES: 1. $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}$ for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM $=0^{\circ} \mathrm{C}$ for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
$T_{\text {high }}=+85^{\circ} \mathrm{C}$ for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM $=+70^{\circ} \mathrm{C}$ for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM 2. The deviation parameter $\Delta \mathrm{V}_{\text {ref }}$ is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.


The average temperature coefficient of the reference input voltage, $\alpha \mathrm{V}_{\text {ref }}$ is defined as:

$$
\mathrm{V}_{\text {ref }} \frac{\mathrm{ppm}}{{ }^{\circ} \mathrm{C}}=\frac{\left(\frac{\Delta \mathrm{V}_{\text {ref }}}{\mathrm{V}_{\text {ref }} @ 25^{\circ} \mathrm{C}}\right) \times 10^{6}}{\Delta \mathrm{~T}_{\mathrm{A}}}=\frac{\Delta \mathrm{V}_{\text {ref }} \times 10^{6}}{\Delta \mathrm{~T}_{\mathrm{A}}\left(\mathrm{~V}_{\text {ref }} @ 25^{\circ} \mathrm{C}\right)}
$$

$\alpha \mathrm{V}_{\text {ref }}$ can be positive or negative depending on whether $\mathrm{V}_{\text {ref }}$ Min or $\mathrm{V}_{\text {ref }}$ Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : $\Delta \mathrm{V}_{\text {ref }}=8.0 \mathrm{mV}$ and slope is positive,

$$
\mathrm{V}_{\text {ref }} @ 25^{\circ} \mathrm{C}=2.495 \mathrm{~V}, \Delta \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C} \quad \alpha \mathrm{~V}_{\text {ref }}=\frac{0.008 \times 10^{6}}{70(2.495)}=45.8 \mathrm{ppm} /{ }^{\circ} \mathrm{C}
$$

3. The dynamic impedance $Z_{K A}$ is defined as $\left|Z_{K A}\right|=\frac{\Delta V_{K A}}{\Delta I_{K}}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$
\left|Z_{K A}{ }^{\prime}\right| \approx\left|Z_{K A}\right|\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right)
$$

## TL431, A, B Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | TL431AI |  |  | TL431AC |  |  | TL431BI |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Reference Input Voltage (Figure 1) $\begin{aligned} \mathrm{V}_{K A} & =\mathrm{V}_{\text {ref, }}, I_{\mathrm{K}}=10 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 2.47 \\ & 2.44 \end{aligned}$ | 2.495 | 2.52 2.55 | $\begin{gathered} 2.47 \\ 2.453 \end{gathered}$ | 2.495 | $\begin{gathered} 2.52 \\ 2.537 \end{gathered}$ | $\begin{aligned} & 2.483 \\ & 2.475 \end{aligned}$ | $\begin{aligned} & 2.495 \\ & 2.495 \end{aligned}$ | $\begin{aligned} & 2.507 \\ & 2.515 \end{aligned}$ | V |
| Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2) $V_{K A}=V_{\text {ref, },} I_{K}=10 \mathrm{~mA}$ | $\Delta \mathrm{V}_{\text {ref }}$ | - | 7.0 | 30 | - | 3.0 | 17 | - | 3.0 | 17 | mV |
| Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $\begin{gathered} \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA} \text { (Figure 2), } \\ \Delta \mathrm{V}_{\mathrm{KA}}=10 \mathrm{~V} \text { to } \mathrm{V}_{\text {ref }} \\ \Delta \mathrm{V}_{\mathrm{KA}}=36 \mathrm{~V} \text { to } 10 \mathrm{~V} \end{gathered}$ | $\frac{\Delta \mathrm{V}_{\text {ref }}}{\Delta \mathrm{V}_{\mathrm{KA}}}$ | - | $\begin{aligned} & -1.4 \\ & -1.0 \end{aligned}$ | $\begin{aligned} & -2.7 \\ & -2.0 \end{aligned}$ | - | $\begin{aligned} & -1.4 \\ & -1.0 \end{aligned}$ | $\begin{aligned} & -2.7 \\ & -2.0 \end{aligned}$ |  | $\begin{array}{r} -1.4 \\ -1.0 \end{array}$ | $\begin{aligned} & -2.7 \\ & -2.0 \end{aligned}$ | $\mathrm{mV} / \mathrm{V}$ |
| $\begin{aligned} & \text { Reference Input Current (Figure 2) } \\ & \mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{R} 1=10 \mathrm{k}, \mathrm{R} 2=\infty \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 1) } \end{aligned}$ | $\mathrm{I}_{\text {ref }}$ |  | $1.8$ |  |  |  | $\begin{aligned} & 4.0 \\ & 5.2 \end{aligned}$ |  |  | $\begin{aligned} & 2.0 \\ & 4.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) $\mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{R} 1=10 \mathrm{k}, \mathrm{R} 2=\infty$ | $\Delta \mathrm{l}_{\text {ref }}$ | - | 0.8 | 2.5 | - | 0.4 | 1.2 | - | 0.8 | 2.5 | $\mu \mathrm{A}$ |
| Minimum Cathode Current For Regulation $V_{K A}=V_{\text {ref }}(\text { Figure 1) }$ | $I_{\text {min }}$ | - | 0.5 | 1.0 | - | 0.5 | 1.0 | - | 0.5 | 1.0 | mA |
| Off-State Cathode Current (Figure 3) $V_{K A}=36 \mathrm{~V}, \mathrm{~V}_{\text {ref }}=0 \mathrm{~V}$ | $\mathrm{I}_{\text {off }}$ | - | 260 | 1000 | - | 260 | 1000 | - | 230 | 500 | nA |
| $\begin{aligned} & \text { Dynamic Impedance (Figure 1, Note 3) } \\ & V_{\mathrm{KA}}=\mathrm{V}_{\text {ref, }} \Delta_{\mathrm{K}}=1.0 \mathrm{~mA} \text { to } 100 \mathrm{~mA} \\ & \mathrm{f} \leq 1.0 \mathrm{kHz} \end{aligned}$ | $\left\|Z_{\text {KA }}\right\|$ | - | 0.22 | 0.5 | - | 0.22 | 0.5 | - | 0.14 | 0.3 | $\Omega$ |

NOTES: 1. $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}$ for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM
$=0^{\circ} \mathrm{C}$ for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
$T_{\text {high }}=+85^{\circ} \mathrm{C}$ for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
$=+70^{\circ} \mathrm{C}$ for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
2. The deviation parameter $\Delta \mathrm{V}_{\text {ref }}$ is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.


The average temperature coefficient of the reference input voltage, $\alpha \mathrm{V}_{\text {ref }}$ is defined as:

$$
\mathrm{V}_{\text {ref }} \frac{\mathrm{ppm}}{{ }^{\circ} \mathrm{C}}=\frac{\left(\frac{\Delta \mathrm{V}_{\text {ref }}}{\mathrm{V}_{\text {ref }} @ 25^{\circ} \mathrm{C}}\right) \times 10^{6}}{\Delta \mathrm{~T}_{\mathrm{A}}}=\frac{\Delta \mathrm{V}_{\text {ref }} \times 10^{6}}{\Delta \mathrm{~T}_{\mathrm{A}}\left(\mathrm{~V}_{\text {ref }} @ 25^{\circ} \mathrm{C}\right)}
$$

$\alpha \mathrm{V}_{\text {ref }}$ can be positive or negative depending on whether $\mathrm{V}_{\text {ref }}$ Min or $\mathrm{V}_{\text {ref }}$ Max occurs at the lower ambient temperature. (Refer to Figure 6.)
Example : $\Delta \mathrm{V}_{\text {ref }}=8.0 \mathrm{mV}$ and slope is positive,

$$
\mathrm{V}_{\text {ref }} @ 25^{\circ} \mathrm{C}=2.495 \mathrm{~V}, \Delta \mathrm{~T}_{\mathrm{A}}=70^{\circ} \mathrm{C} \quad \alpha \mathrm{~V}_{\text {ref }}=\frac{0.008 \times 10^{6}}{70(2.495)}=45.8 \mathrm{ppm} /{ }^{\circ} \mathrm{C}
$$

3. The dynamic impedance $Z_{K A}$ is defined as $\left|Z_{K A}\right|=\frac{\Delta V_{K A}}{\Delta I_{K}}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$
\left|Z_{K A^{\prime}}\right| \approx\left|Z_{K A}\right|\left(1+\frac{R 1}{R 2}\right)
$$

## TL431, A, B Series



Figure 1. Test Circuit for $\mathrm{V}_{\mathrm{KA}}=\mathrm{V}_{\text {ref }}$


Figure 2. Test Circuit for $\mathrm{V}_{\mathrm{KA}}>\mathrm{V}_{\text {ref }}$


Figure 3. Test Circuit for $\mathrm{I}_{\text {off }}$


Figure 4. Cathode Current versus Cathode Voltage


Figure 6. Reference Input Voltage versus Ambient Temperature


Figure 5. Cathode Current versus Cathode Voltage


Figure 7. Reference Input Current versus Ambient Temperature


Figure 8. Change in Reference Input Voltage versus Cathode Voltage


Figure 10. Dynamic Impedance versus Frequency


Figure 12. Open-Loop Voltage Gain versus Frequency


Figure 9. Off-State Cathode Current versus Ambient Temperature


Figure 11. Dynamic Impedance versus Ambient Temperature


Figure 13. Spectral Noise Density

## TL431, A, B Series



Figure 14. Pulse Response


Figure 16. Test Circuit For Curve A of Stability Boundary Conditions


Figure 15. Stability Boundary Conditions


Figure 17. Test Circuit For Curves B, C, And D of Stability Boundary Conditions

TYPICAL APPLICATIONS


Figure 18. Shunt Regulator


Figure 19. High Current Shunt Regulator

## TL431, A, B Series



Figure 20. Output Control for a Three-Terminal Fixed Regulator


Figure 22. Constant Current Source


Figure 24. TRIAC Crowbar


Figure 21. Series Pass Regulator


Figure 23. Constant Current Sink


Figure 25. SRC Crowbar

## TL431, A, B Series

 upper and lower limits.

$$
\begin{aligned}
& \text { Lower Limit }=\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right) \mathrm{V}_{\text {ref }} \\
& \text { Upper Limit }=\left(1+\frac{\mathrm{R} 3}{\mathrm{R} 4}\right) \mathrm{V}_{\mathrm{ref}}
\end{aligned}
$$

Figure 26. Voltage Monitor


Figure 28. Linear Ohmmeter


Figure 27. Single-Supply Comparator with Temperature-Compensated Threshold


Figure 29. Simple 400 mW Phono Amplifier

## TL431, A, B Series



Figure 30. High Efficiency Step-Down Switching Converter

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\mathrm{in}}=10 \mathrm{~V}$ to $20 \mathrm{~V}, \mathrm{I}_{\mathrm{o}}=1.0 \mathrm{~A}$ | $53 \mathrm{mV}(1.1 \%)$ |
| Load Regulation | $\mathrm{V}_{\mathrm{in}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{o}}=0 \mathrm{~A}$ to 1.0 A | $25 \mathrm{mV}(0.5 \%)$ |
| Output Ripple | $\mathrm{V}_{\mathrm{in}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{o}}=1.0 \mathrm{~A}$ | 50 mV Pp P.A.R.D. |
| Output Ripple | $\mathrm{V}_{\mathrm{in}}=20 \mathrm{~V}, \mathrm{I}_{\mathrm{o}}=1.0 \mathrm{~A}$ | 100 mVpp P.A.R.D. |
| Efficiency | $\mathrm{V}_{\mathrm{in}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{o}}=1.0 \mathrm{~A}$ | $82 \%$ |

## TL431, A, B Series

## APPLICATIONS INFORMATION

The TL431 is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non-standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition. Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation.

A simplified model of the TL431 is shown in Figure 31. When tested for stability boundaries, the load resistance is $150 \Omega$. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, Gm, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of Gm flows through compensation capacitance, $\mathrm{C}_{\mathrm{P} 2}$. The voltage across $\mathrm{C}_{\mathrm{P} 2}$ drives the output dependent current source, Go, which is connected across the device cathode and anode.

Model component values are:

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{ref}}=1.78 \mathrm{~V} \\
& \mathrm{Gm}=0.3+2.7 \exp \left(-\mathrm{I}_{\mathrm{C}} / 26 \mathrm{~mA}\right)
\end{aligned}
$$

where $I_{C}$ is the device cathode current and $G m$ is in mhos
$\mathrm{Go}=1.25\left(\mathrm{~V}_{\mathrm{cp}} 2\right) \mu \mathrm{mhos}$.
Resistor and capacitor typical values are shown on the model. Process tolerances are $\pm 20 \%$ for resistors, $\pm 10 \%$ for capacitors, and $\pm 40 \%$ for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$
\mathrm{P} 1=\frac{1}{2 \pi \mathrm{R}_{\mathrm{GM}} \mathrm{C}_{\mathrm{P} 1}}=\frac{1}{2 \pi * 1.0 \mathrm{M}^{*} 20 \mathrm{pF}}=7.96 \mathrm{kHz}
$$

$$
\begin{aligned}
& \mathrm{P} 2=\frac{1}{2 \pi \mathrm{R}_{\mathrm{P} 2} \mathrm{C}_{\mathrm{P} 2}}=\frac{1}{2 \pi * 10 \mathrm{M} * 0.265 \mathrm{pF}}=60 \mathrm{kHz} \\
& \mathrm{Z} 1=\frac{1}{2 \pi \mathrm{R}_{\mathrm{Z} 1} \mathrm{C}_{\mathrm{P} 1}}=\frac{1}{2 \pi * 15.9 \mathrm{k} * 20 \mathrm{pF}}=500 \mathrm{kHz}
\end{aligned}
$$

In addition, there is an external circuit pole defined by the load:

$$
P_{L}=\frac{1}{2 \pi R_{L} C_{L}}
$$

Also, the transfer dc voltage gain of the TL431 is:

$$
\mathrm{G}=\mathrm{G}_{\mathrm{M}} \mathrm{R}_{\mathrm{GM}} \mathrm{GoR}_{\mathrm{L}}
$$

Example 1:
${ }^{\mathrm{I}} \mathrm{C}=10 \mathrm{~mA}, \mathrm{R}_{\mathrm{L}}=230 \Omega, \mathrm{C}_{\mathrm{L}}=0$. Define the transfer gain.
The DC gain is:

$$
\begin{gathered}
\mathrm{G}=\mathrm{G}_{\mathrm{M}} \mathrm{R}_{\mathrm{GM}} \mathrm{GoR}_{\mathrm{L}}= \\
(2.138)(1.0 \mathrm{M})(1.25 \mu)(230)=615=56 \mathrm{~dB} \\
\text { Loop gain }=\mathrm{G} \frac{8.25 \mathrm{k}}{8.25 \mathrm{k}+15 \mathrm{k}}=218=47 \mathrm{~dB}
\end{gathered}
$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$
A v=615 \frac{\left(\frac{1+j f}{500 \mathrm{kHz}}\right)}{\left(\frac{1+\mathrm{jf}}{8.0 \mathrm{kHz}}\right)\left(\frac{1+\mathrm{jf}}{60 \mathrm{kHz}}\right)}
$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz . The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open-Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.

## TL431, A, B Series



Figure 31. Simplified TL431 Device Model


Figure 32. Example 1 Circuit Open Loop Gain Plot Example 2.
$\mathrm{I}_{\mathrm{C}}=7.5 \mathrm{~mA}, \mathrm{R}_{\mathrm{L}}=2.2 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=0.01 \mu \mathrm{~F}$. Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.

The DC gain is:

$$
\begin{gathered}
\mathrm{G}=\mathrm{G}_{\mathrm{M}} \mathrm{R}_{\mathrm{GM}} \mathrm{GoR}_{\mathrm{L}}= \\
(2.323)(1.0 \mathrm{M})(1.25 \mu)(2200)=6389=76 \mathrm{~dB}
\end{gathered}
$$

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

$$
A v=615 \frac{\left(\frac{1+\mathrm{jf}}{500 \mathrm{kHz}}\right)}{\left(\frac{1+\mathrm{jf}}{8.0 \mathrm{kHz}}\right)\left(\frac{1+\mathrm{jf}}{60 \mathrm{kHz}}\right)\left(\frac{1+\mathrm{jf}}{7.2 \mathrm{kHz}}\right)}
$$

Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.

Note that the crossover frequency in this case is about 250 kHz , having a phase margin of about -46 degrees. Therefore, instability of this circuit is likely.


Figure 33. Example 2 Circuit Open Loop Gain Plot
With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

## CS1009

### 2.5 Volt Reference

The CS1009 is a precision trimmed $2.5 \mathrm{~V} \pm 5.0 \mathrm{mV}$ shunt regulator diode. The low dynamic impedance and wide operating current range enhances its versatility. The tight reference tolerance is achieved by on-chip trimming which minimizes voltage tolerance and temperature drift.

A third terminal allows the reference voltage to be adjusted $\pm 5.0 \%$ to calibrate out system errors. In many applications, the CS1009GZ can be used as a pin-to-pin replacement of the LT1009CZ and the LM136Z-2.5 with the external trim network eliminated.

## Features

- 0.2\% Initial Tolerance Max.
- Guaranteed Temperature Stability
- Maximum $0.6 \Omega$ Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LT1009 and LM136 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient
- Meets Mil Std 883C ESD Requirements


TO-92 Z SUFFIX CASE 29

PIN CONNECTIONS AND MARKING DIAGRAM


Pin 1. ADJ. PIN
2. $\mathrm{V}_{\mathrm{REF}}$
3. GND

A = Assembly Location
WL, L = Wafer Lot
YY, $Y$ = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS1009GD8 | SO-8 | 95 Units/Rail |
| CS1009GDR8 | SO-8 | 2500 Tape \& Reel |
| CS1009GZ3 | TO-92 | 2000 Units |
| CS1009GZR3 | TO-92 | 2000 Tape \& Reel |



Figure 2. Block Diagram

MAXIMUM RATINGS*

| Rating | Value | Unit |  |
| :--- | :---: | :---: | :---: |
| Reverse Current | 20 | mA |  |
| Forward |  | 10 | mA |
| Operating Temperature Range | -40 to 105 | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature Range | Wave Solder (through hole styles only) (Note 1) |  |  |
| Lead Temperature Soldering: (SMD styles only) (Note 2) | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |  |

1. 10 second maximum
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Reverse Breakdown Voltage | $\mathrm{I}_{\mathrm{R}}=1.0 \mathrm{~mA}$ | 2.492 | 2.500 | 2.508 | V |
| Reverse Breakdown Voltage | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}$ | 2.492 | 2.500 | 2.508 | V |
| Reverse Breakdown Voltage | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq{ }^{\circ} \mathrm{C}$ | 2.480 | 2.500 | 2.508 | V |
| Reverse Breakdown Voltage Change with Current | $400 \mu \mathrm{~A} \leq \mathrm{I}_{\mathrm{R}} \leq 10 \mathrm{~mA}$ | $-$ | $\begin{aligned} & 2.6 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Reverse Dynamic Impedance | $\mathrm{I}_{\mathrm{R}}=1.0 \mathrm{~mA}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.4 \end{aligned}$ | $\begin{aligned} & \Omega \\ & \Omega \end{aligned}$ |
| Temperature Stability <br> Avgerage Temperature Coefficient | $\begin{aligned} & 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} \text {, Note } 3 \\ & 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} \text {, Note } 3 \end{aligned}$ | - | - | - | $\begin{gathered} \mathrm{mV} \\ \mathrm{ppm} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Long Term Stabilty | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \pm 0.1 \mathrm{C}, \mathrm{I}_{\mathrm{R}}=1.0 \mathrm{~mA}$ | - | 20 | - | ppm/kHr |

$\dagger$ Denotes the specifications which apply over full operating temperature range.
3. Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Reverse Current vs. Reverse Voltage


Figure 4. Change in Reverse Voltage vs. Reverse Current


Figure 5. Forward Voltage vs. Forward Current


Figure 6. Dynamic Impedance vs. Frequency


Figure 7. Zener Noise Voltage vs. Frequency


Figure 8. Response Time


Figure 9. Reference Voltage vs. Temperature

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | TO-92 | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 45 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 165 | 170 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC1403, B

## Low Voltage Reference

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with D/A converters, up to 12 bits in accuracy, or as a reference for power supply applications.

- Output Voltage: $2.5 \mathrm{~V} \pm 25 \mathrm{mV}$
- Input Voltage Range: 4.5 V to 40 V
- Quiescent Current: 1.2 mA Typical
- Output Current: 10 mA
- Temperature Coefficient: $10 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ Typical
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP, and 8-Pin SOIC Package


## Typical Applications

- Voltage Reference for 8 to 12 Bit D/A Converters
- Low $\mathrm{T}_{\mathrm{C}}$ Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\mathbf{I}}$ | 40 | V |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +175 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range <br> MC1403B <br> MC1403 | $\mathrm{T}_{\mathrm{A}}$ |  | -40 to +85 |
| 0 to +70 |  |  |  |$\stackrel{ }{\circ} \mathrm{C}_{{ }^{\circ} \mathrm{C}}$

## PRECISION LOW VOLTAGE REFERENCE

SEMICONDUCTOR TECHNICAL DATA


PIN CONNECTIONS


ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
| :---: | :---: | :---: |
| MC1403D | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | SO-8 |
| MC1403P1 |  | Plastic DIP |
| MC1403BD | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-8 |
| MC1403BP1 |  | Plastic DIP |

Figure 1. A Reference for Monolithic D/A Converters


Providing the Reference Current for ON Semiconductor Monolithic D/A Converters

The MC1403 makes an ideal reference for many monolithic D/A converters, requiring a stable current reference of nominally 2.0 mA . This can be easily obtained from the MC1403 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for fullscale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the $D / A$ reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.
A single MC1403 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}\right)$ | $V_{\text {out }}$ | 2.475 | 2.5 | 2.525 | V |
| Temperature Coefficient of Output Voltage* MC1403 | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | 10 | 40 | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Output Voltage Change }{ }^{*} \\ & \text { (Over specified temperature range) } \\ & \text { MC1403 } \quad 0 \text { to }+70^{\circ} \mathrm{C} \\ & \text { MC1403B } \\ & \hline-40 \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\Delta \mathrm{V}_{\mathrm{O}}$ | - | - | $\begin{gathered} 7.0 \\ 12.5 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Line Regulation }\left(l_{\mathrm{O}}=0 \mathrm{~mA}\right) \\ & \left(15 \mathrm{~V} \leqslant \quad \mathrm{~V}_{1} \leqslant 40 \mathrm{~V}\right) \\ & \left(4.5 \mathrm{~V} \leqslant \mathrm{~V}_{1} \leqslant 15 \mathrm{~V}\right) \end{aligned}$ | Regline | - | $\begin{aligned} & 1.2 \\ & 0.6 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 3.0 \end{aligned}$ | mV |
| Load Regulation $\left(0 \mathrm{~mA}<\mathrm{l}_{\mathrm{O}}<10 \mathrm{~mA}\right)$ | Regload | - | - | 10 | mV |
| Quiescent Current $\left(\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}\right)$ | $\mathrm{I}_{\mathrm{Q}}$ | - | 1.2 | 1.5 | mA |

*Guaranteed but not tested.
Figure 2. MC1403, B Schematic


This device contains 15 active transistors.

Figure 3. Typical Change in $\mathrm{V}_{\text {out }}$ versus $\mathrm{V}_{\text {in }}$ (Normalized to $\mathrm{V}_{\text {in }}=15 \mathrm{~V} @ \mathrm{~T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ )


Figure 5. Quiescent Current versus Temperature


Figure 4. Change in Output Voltage versus Load Current
(Normalized to $\mathrm{V}_{\text {out }} @ \mathrm{~V}_{\text {in }}=15 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}$ )


Figure 6. Change in $\mathrm{V}_{\text {out }}$ versus Temperature (Normalized to $\mathrm{V}_{\text {out }} @ \mathrm{~V}_{\text {in }}=15 \mathrm{~V}$ )


Figure 7. Change in $\mathrm{V}_{\text {out }}$ versus Temperature
(Normalized to $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\text {in }}=15 \mathrm{~V}$, $\mathrm{I}_{\text {out }}=0 \mathrm{~mA}$ )


## MC1403, B

## 3-1/2-Digit Voltmeter - Common Anode Displays, Flashing Overrange

An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V . When switching from 2.0 V to 200 mV operation, $\mathrm{R}_{\mathrm{I}}$ is also changed, as shown on the diagram.

When using $\mathrm{R}_{\mathrm{C}}$ equal to $300 \mathrm{k} \Omega$, the clock frequency for the system is about 66 kHz . The resulting conversion time is approximately 250 ms .

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This
is done by dividing the EOC pulse rate by 2 with $1 / 2$ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to $\mathrm{V}_{\mathrm{EE}}$ via Pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as $150 \Omega$ in Figure 8 .

Figure 8. 3-1/2-Digit Voltmeter


## MC78L00A Series

## 100 mA Positive Voltage Regulators

The MC78L00A Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA . Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination, as output impedance and quiescent current are substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00A Series)


Figure 1. Representative Schematic Diagram


Figure 2. Standard Application
A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

[^3]

## ON Semiconductor ${ }^{\text {w }}$

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*SOP-8 is an internally modified SO-8 package. Pins $2,3,6$, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 package.

## PIN CONNECTIONS


(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 139 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 141 of this data sheet.

## MC78L00A Series

MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage (2.6 V-8.0 V) | $\mathrm{V}_{\mathrm{I}}$ | 30 | Vdc |
| $(12 \mathrm{~V}-18 \mathrm{~V})$ |  | 35 |  |
| $(24 \mathrm{~V})$ |  | 40 |  |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | 0 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$ (for MC78LXXAB), $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$ (for MC78LXXAC), unless otherwise noted.)

| Characteristics | Symbol | MC78L05AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 4.8 | 5.0 | 5.2 | Vdc |
| Line Regulation $\begin{aligned} & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}\right) \\ & 7.0 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 20 \mathrm{Vdc} \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 20 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 55 \\ & 45 \end{aligned}$ | $\begin{aligned} & 150 \\ & 100 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \qquad \begin{array}{l} \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}\right) \\ \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{array} \end{aligned}$ | Regload | - | $\begin{aligned} & 11 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 60 \\ & 30 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(7.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 20 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{0} \leq 40 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{I}}=10 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 4.75 \\ & 4.75 \end{aligned}$ | - | $\begin{array}{r} 5.25 \\ 5.25 \\ \hline \end{array}$ | Vdc |
| $\begin{aligned} & \text { Input Bias Current } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \\ & \hline \end{aligned}$ | IB | - | 3.8 | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ | mA |
| $\begin{aligned} & \hline \text { Input Bias Current Change } \\ & \left(8.0 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 20 \mathrm{Vdc}\right) \\ & \left(1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{aligned}$ | $\Delta{ }^{\text {IB }}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(T_{A}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 40 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection }\left(\mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA},\right. \\ & \left.\quad \mathrm{f}=120 \mathrm{~Hz}, 8.0 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 18 \mathrm{~V}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 41 | 49 | - | dB |
| Dropout Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.7 | - | Vdc |

## MC78L00A Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$ (for MC78LXXAB), $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$ (for MC78LXXAC), unless otherwise noted.)

| Characteristics | Symbol | MC78L08AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 7.7 | 8.0 | 8.3 | Vdc |
| $\begin{aligned} & \text { Line Regulation } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}\right) \\ & 10.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 23 \mathrm{Vdc} \\ & 11 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 23 \mathrm{Vdc} \end{aligned}$ | Regline |  | $\begin{aligned} & 20 \\ & 12 \end{aligned}$ | $\begin{aligned} & 175 \\ & 125 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \qquad \begin{array}{l} \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}\right) \\ \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{array} \end{aligned}$ | Regload |  | $\begin{aligned} & 15 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 80 \\ & 40 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(10.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 23 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I} \leq 40 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{I}}=14 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 7.6 \\ & 7.6 \end{aligned}$ |  | $\begin{aligned} & 8.4 \\ & 8.4 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Input Bias Current } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | $I_{\text {IB }}$ |  | 3.0 | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ | mA |
| $\begin{gathered} \text { Input Bias Current Change } \\ \left(11 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 23 \mathrm{Vdc}\right) \\ \left(1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{gathered}$ | $\Delta \\|_{\text {IB }}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 60 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection }\left(\mathrm{l}_{\mathrm{O}}=40 \mathrm{~mA}\right. \\ & \left.\mathrm{f}=120 \mathrm{~Hz}, 12 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 23 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 37 | 57 | - | dB |
| Dropout Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 1.7 | - | Vdc |

ELECTRICAL CHARACTERISTICS $\left(V_{I}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$ (for MC78LXXAB), $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$ (for MC78LXXAC), unless otherwise noted.)

| Characteristics | Symbol | MC78L09AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 8.6 | 9.0 | 9.4 | Vdc |
| Line Regulation $\begin{aligned} & \left(\mathrm{T}_{\mathrm{J}=}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}\right) \\ & 11.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 24 \mathrm{Vdc} \\ & 12 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 24 \mathrm{Vdc} \end{aligned}$ | Regline |  | $\begin{aligned} & 20 \\ & 12 \end{aligned}$ | $\begin{aligned} & 175 \\ & 125 \end{aligned}$ | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 15 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 90 \\ & 40 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(11.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 24 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I} \leq 40 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{I}}=15 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 8.5 \\ & 8.5 \end{aligned}$ |  | $\begin{aligned} & 9.5 \\ & 9.5 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Input Bias Current } \\ & \qquad \begin{array}{l} \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \end{array} \end{aligned}$ | 1 IB | - | 3.0 | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ | mA |
| Input Bias Current Change ( $11 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 23 \mathrm{Vdc}$ ) $\left(1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right)$ | $\Delta l_{1 B}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 60 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection ( } \mathrm{l}_{\mathrm{O}}=40 \mathrm{~mA}, \\ & \left.\mathrm{f}=120 \mathrm{~Hz}, 13 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 24 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 37 | 57 | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.7 | - | Vdc |

## MC78L00A Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$ (for MC78LXXAB), $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$ (for MC78LXXAC), unless otherwise noted.)

| Characteristics | Symbol | MC78L12AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 11.5 | 12 | 12.5 | Vdc |
| Line Regulation $\begin{aligned} & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}\right) \\ & 14.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 27 \mathrm{Vdc} \\ & 16 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 27 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 120 \\ & 100 \end{aligned}$ | $\begin{aligned} & 250 \\ & 200 \end{aligned}$ | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 100 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{aligned}$ | Regload | - | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 100 \\ & 50 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(14.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 27 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{I}}=19 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 11.4 \\ & 11.4 \end{aligned}$ |  | $\begin{aligned} & 12.6 \\ & 12.6 \end{aligned}$ | Vdc |
| Input Bias Current $\begin{aligned} & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | $I_{\text {IB }}$ | - |  | $\begin{aligned} & 6.5 \\ & 6.0 \end{aligned}$ | mA |
| Input Bias Current Change ( $16 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 27 \mathrm{Vdc}$ ) $\left(1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right)$ | $\Delta I_{1 B}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 80 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection ( } \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \\ & \left.\mathrm{f}=120 \mathrm{~Hz}, 15 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 25 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 37 | 42 | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.7 | - | Vdc |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$ (for MC78LXXAB), $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$ (for MC78LXXAC), unless otherwise noted.)

| Characteristics | Symbol | MC78L15AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 14.4 | 15 | 15.6 | Vdc |
| Line Regulation $\begin{aligned} & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}\right) \\ & 17.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 30 \mathrm{Vdc} \\ & 20 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 30 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 130 \\ & 110 \end{aligned}$ | $\begin{aligned} & 300 \\ & 250 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \qquad \begin{array}{l} \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}\right) \\ \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{array} \end{aligned}$ | Regload | - | $\begin{aligned} & 25 \\ & 12 \end{aligned}$ | $\begin{aligned} & 150 \\ & 75 \\ & \hline \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(17.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 30 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{I}}=23 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 14.25 \\ & 14.25 \end{aligned}$ |  | $\begin{aligned} & 15.75 \\ & 15.75 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Input Bias Current } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | $I_{\text {IB }}$ | - | 4.4 | $\begin{aligned} & 6.5 \\ & 6.0 \end{aligned}$ | mA |
| Input Bias Current Change ( $20 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 30 \mathrm{Vdc}$ ) $\left(1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right)$ | $\Delta \\|_{\text {IB }}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| $\begin{aligned} & \text { Output Noise Voltage } \\ & \qquad\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 90 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection ( } \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \\ & \mathrm{f}=120 \mathrm{~Hz}, 18.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 28.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \text { ) } \end{aligned}$ | RR | 34 | 39 | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.7 | - | Vdc |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=27 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted. )

| Characteristics | Symbol | MC78L18AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | Vo | 17.3 | 18 | 18.7 | Vdc |
| $\begin{aligned} & \text { Line Regulation } \\ & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}\right) \\ & 21.4 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc} \\ & 20.7 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc} \\ & 22 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc} \\ & 21 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc} \end{aligned}$ | Regline |  | 45 35 | $\begin{aligned} & 325 \\ & 275 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \left.\qquad \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 30 \\ & 15 \\ & \hline \end{aligned}$ | $\begin{gathered} 170 \\ 85 \\ \hline \end{gathered}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(21.4 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I} \leq 40 \mathrm{~mA}\right) \\ & \left(20.7 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{I}}=27 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{I}}=27 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{0} \leq 70 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 17.1 \\ & 17.1 \end{aligned}$ | - | $\begin{aligned} & 18.9 \\ & 18.9 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Input Bias Current } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \\ & \hline \end{aligned}$ | IB | - |  | $\begin{aligned} & 6.5 \\ & 6.0 \end{aligned}$ | mA |
| $\begin{gathered} \text { Input Bias Current Change } \\ \left(22 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc}\right) \\ \left(21 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc}\right) \\ \left(1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{gathered}$ | $\Delta^{\text {I }}$ IB | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 150 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection ( } \mathrm{l}_{\mathrm{O}}=40 \mathrm{~mA}, \\ & \mathrm{f}=120 \mathrm{~Hz}, 23 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 33 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \text { ) } \end{aligned}$ | RR | 33 | 48 | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}$ | - | 1.7 | - | Vdc |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=33 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | MC78L24AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 23 | 24 | 25 | Vdc |
| Line Regulation $\begin{aligned} & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}\right) \\ & 27.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 38 \mathrm{Vdc} \\ & 28 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 80 \mathrm{Vdc} \\ & 27 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 38 \mathrm{Vdc} \end{aligned}$ | Regline |  | $\begin{aligned} & - \\ & 50 \\ & 60 \end{aligned}$ | $\begin{aligned} & 300 \\ & 350 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \qquad \begin{array}{l} \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}\right) \\ \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{array} \end{aligned}$ | Regload |  | $\begin{aligned} & 40 \\ & 20 \end{aligned}$ | $\begin{aligned} & 200 \\ & 100 \end{aligned}$ | mV |
| Output Voltage <br> $\left(28 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 38 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right)$ <br> $\left(27 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 38 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right)$ <br> $\left(28 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}}=33 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right)$ <br> $\left(27 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 33 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 70 \mathrm{~mA}\right.$ ) | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 22.8 \\ & 22.8 \end{aligned}$ | - | $\begin{aligned} & 25.2 \\ & 25.2 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Input Bias Current } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | IB |  | 3.1 | $\begin{aligned} & 6.5 \\ & 6.0 \\ & \hline \end{aligned}$ | mA |
| $\begin{gathered} \text { Input Bias Current Change } \\ \left(28 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 38 \mathrm{Vdc}\right) \\ \left(1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}\right) \end{gathered}$ | $\Delta^{\text {I }}$ IB |  | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| $\begin{aligned} & \text { Output Noise Voltage } \\ & \quad\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 200 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection }\left(\mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA},\right. \\ & \left.\mathrm{f}=120 \mathrm{~Hz}, 29 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 35 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 31 | 45 | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.7 | - | Vdc |



Figure 3. Dropout Characteristics


Figure 5. Input Bias Current versus Ambient Temperature


Figure 4. Dropout Voltage versus Junction Temperature


Figure 6. Input Bias Current versus Input Voltage


Figure 7. Maximum Average Power Dissipation versus Ambient Temperature - TO-92 Type Package

Figure 8. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC78L00A Series

## APPLICATIONS INFORMATION

## Design Considerations

The MC78L00A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The


The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$
\mathrm{I}_{0}=\frac{5.0 \mathrm{~V}}{\mathrm{R}}+\mathrm{I}_{\mathrm{B}}
$$

$I_{I B}=3.8 \mathrm{~mA}$ over line and load changes

For example, a 100 mA current source would require R to be a $50 \Omega, 1 / 2 \mathrm{~W}$ resistor and the output voltage compliance would be the input voltage less 7 V .

Figure 9. Current Regulator
input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.


Figure 10. $\pm 15$ V Tracking Voltage Regulator


Figure 11. Positive and Negative Regulator

## MC78L00A Series

ORDERING INFORMATION

| Device | Output Voltage | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| MC78L05ABD | 5.0 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L05ABDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L05ABP |  |  | TO-92 | 2000 Units/Bag |
| MC78L05ABPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L05ABPRE |  |  | TO-92 | 2000 Units/Bag |
| MC78L05ABPRM |  |  | TO-92 | 2000 Ammo Pack |
| MC78L05ACD |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L05ACDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L05ACP |  |  | TO-92 | 2000 Units/Bag |
| MC78L05ACPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L05ACPRE |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L05ACPRM |  |  | TO-92 | 2000 Ammo Pack |
| MC78L05ACPRP |  |  | TO-92 | 2000 Ammo Pack |
| MC78L08ABD | 8.0 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L08ABDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L08ABP |  |  | TO-92 | 2000 Units/Bag |
| MC78L08ABPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L08ABPRP |  |  | TO-92 | 2000 Units/Bag |
| MC78L08ACD |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L08ACDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L08ACP |  |  | TO-92 | 2000 Units/Bag |
| MC78L08ACPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L08ACPRE |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L08ACPRP |  |  | TO-92 | 2000 Ammo Pack |
| MC78L09ABD | 9.0 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L09ABDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L09ABPRA |  |  | TO-92 | 2000 Units/Bag |
| MC78L09ABPRP |  |  | TO-92 | 2000 Units/Bag |
| MC78L09ACD |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L09ACDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L09ACP |  |  | TO-92 | 2000 Units/Bag |

## MC78L00A Series

ORDERING INFORMATION (continued)

| Device | Output Voltage | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| MC78L12ABD | 12 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L12ABDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L12ABP |  |  | TO-92 | 2000 Units/Bag |
| MC78L12ABPRP |  |  | TO-92 | 2000 Units/Bag |
| MC78L12ACD |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L12ACDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L12ACP |  |  | TO-92 | 2000 Units/Bag |
| MC78L12ACPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L12ACPRE |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L12ACPRM |  |  | TO-92 | 2000 Ammo Pack |
| MC78L12ACPRP |  |  | TO-92 | 2000 Ammo Pack |
| MC78L15ABD | 15 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L15ABDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L15ABP |  |  | TO-92 | 2000 Units/Bag |
| MC78L15ABPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L15ABPRP |  |  | TO-92 | 2000 Units/Bag |
| MC78L15ACD |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 | 98 Units/Rail |
| MC78L15ACDR2 |  |  | SOP-8 | 2500 Tape \& Reel |
| MC78L15ACP |  |  | TO-92 | 2000 Units/Bag |
| MC78L15ACPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L15ACPRP |  |  | TO-92 | 2000 Ammo Pack |
| MC78L18ABP | 18 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-92 | 2000 Units/Bag |
| MC78L18ACP |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-92 | 2000 Units/Bag |
| MC78L18ACPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L18ACPRM |  |  | TO-92 | 2000 Units/Bag |
| MC78L18ACPRP |  |  | TO-92 | 2000 Ammo Pack |
| MC78L24ABP | 24 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-92 | 2000 Units/Bag |
| MC78L24ACP |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-92 | 2000 Units/Bag |
| MC78L24ACPRA |  |  | TO-92 | 2000 Tape \& Reel |
| MC78L24ACPRP |  |  | TO-92 | 2000 Ammo Pack |

## MC78L00A Series

## MARKING DIAGRAMS

SOP-8 D SUFFIX CASE 751


$$
\begin{array}{ll}
\mathrm{xx} & =05,08,09,12, \text { or } 15 \\
\mathrm{~A} & =\text { Assembly Location } \\
\mathrm{L} & =\text { Wafer Lot } \\
\mathrm{Y} & =\text { Year } \\
\mathrm{W} & =\text { Work Week } \\
\mathrm{B}, \mathrm{C} & =\text { Temperature Range }
\end{array}
$$

> TO-92
> P SUFFIX
> CASE 029


[^4]
## MC78M00, MC78M00A Series

## 500 mA Positive Voltage Regulators

The MC78M00/MC78M00A Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA .

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- MC78M00A High Accuracy ( $\pm 2 \%$ ) Available for 5.0 V, 8.0 V, 12 V and 15 V


This device contains 28 active transistors.
Figure 1. Representative Schematic Diagram


ON Semiconductor ${ }^{\text {T }}$ http://onsemi.com


|  | MARKING |
| :---: | :---: |
| DIAGRAMS |  |



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

Pin 1. Input
2. Ground
3. Output

```
xx = Voltage Option
Z = A, B, or C Option
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
```


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 151 of this data sheet.

## MC78M00, MC78M00A Series

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.) (Note 1)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage (5.0 V-18 V) | $\mathrm{V}_{\mathrm{I}}$ | 35 | Vdc |
| $(20 \mathrm{~V}-24 \mathrm{~V})$ |  | 40 |  |
| Power Dissipation (Package Limitation) |  |  |  |
| Plastic Package, T Suffix | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited |  |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\theta_{\mathrm{JA}}$ | 70 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Air | $\theta_{\mathrm{JC}}$ | 5.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case |  |  |  |
| Plastic Package, DT Suffix | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | ${ }^{\circ}$ |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\theta_{\mathrm{JA}}$ | 92 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Air | $\theta_{\mathrm{JC}}$ | 5.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  |  |  |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
MC78M05C/AC/B/AB ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}$, unless otherwise noted.) (Note 2)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) MC78M05C MC78M05AC | V | $\begin{aligned} & 4.8 \\ & 4.9 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 5.2 \\ & 5.1 \end{aligned}$ | Vdc |
| Output Voltage Variation $\begin{aligned} & \left(7.0 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 20 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right) \\ & \text { MC78M05C } \\ & \text { MC78M05AC } \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 4.75 \\ & 4.80 \end{aligned}$ |  | $\begin{aligned} & 5.25 \\ & 5.20 \end{aligned}$ | Vdc |
| Line Regulation $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 7.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 3.0 | 50 | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{gathered} 100 \\ 50 \end{gathered}$ | mV |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $I_{\text {IB }}$ | - | 3.2 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & \left(8.0 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right) \end{aligned}$ | $\Delta l_{\text {IB }}$ | - |  | $\begin{aligned} & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 40 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\begin{aligned} & \left(\mathrm{l}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 18 \mathrm{~V}\right) \\ & \left(\mathrm{l}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 8.0 \leq \mathrm{V}_{\mathrm{I}} \leq 18 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 62 \\ & 62 \\ & \hline \end{aligned}$ | 80 |  | dB |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{I}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.2$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | 10 | - | 700 | - | mA |

2. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78MxxAC, C $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78MxxAB, AC, B, C
$=-40^{\circ} \mathrm{C}$ for $\mathrm{MC} 78 \mathrm{MxxAB}, \mathrm{B}$

## MC78M00, MC78M00A Series

MC78M06C ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=11 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 5.75 | 6.0 | 6.25 | Vdc |
| Output Voltage Variation $\left(8.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 21 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | 5.7 | - | 6.3 | Vdc |
| Line Regulation $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 5.0 | 50 | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{gathered} 120 \\ 60 \end{gathered}$ | mV |
| Input Bias Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{I}_{1 B}$ | - | 3.2 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & \left(9.0 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right) \end{aligned}$ | $\Delta^{\text {I }}$ IB |  | - | $\begin{aligned} & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 45 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 19 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 19 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 59 \\ & 59 \end{aligned}$ | $80$ |  | dB |
| Dropout Voltage $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{I}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.2$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | 10 | - | 700 | - | mA |

MC78M08C/AC/B/AB ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}$, unless otherwise noted.) (Note 3)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) MC78M08C MC78M08AC | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 7.70 \\ & 7.84 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 8.30 \\ & 8.16 \end{aligned}$ | Vdc |
| Output Voltage Variation <br> ( $10.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 23 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ ) MC78M08C <br> MC78M08AC | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 7.6 \\ & 7.7 \end{aligned}$ |  | $\begin{aligned} & 8.4 \\ & 8.3 \end{aligned}$ | Vdc |
| Line Regulation $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 10.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 6.0 | 50 | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | $\begin{gathered} 160 \\ 80 \end{gathered}$ | mV |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | IB | - | 3.2 | 6.0 | mA |
| Quiescent Current Change ( $10.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ ) ( $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ ) | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 52 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \quad\left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 11.5 \mathrm{~V} \leq \mathrm{V}_{1} \leq 21.5 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 11.5 \mathrm{~V} \leq \mathrm{V}_{1} \leq 21.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 56 \\ & 56 \end{aligned}$ | $80$ |  | dB |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{I}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.2$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | 10 | - | 700 | - | mA |

3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78MxxAC, C $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78MxxAB, AC, B, C
$=-40^{\circ} \mathrm{C}$ for $\mathrm{MC} 78 \mathrm{MxxAB}, \mathrm{B}$

## MC78M00, MC78M00A Series

MC78M09C/B ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}$, unless otherwise noted. $)$ (Note 4)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 8.64 | 9.0 | 9.45 | Vdc |
| Output Voltage Variation <br> ( $11.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 23 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 8.55 | - | 9.45 | Vdc |
| Line Regulation $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 11.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 6.0 | 50 | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \qquad\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  |  | $\begin{gathered} 180 \\ 90 \end{gathered}$ | mV |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | IB | - | 3.2 | 6.0 | mA |
| Quiescent Current Change <br> ( $11.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ ) <br> ( $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ ) | $\Delta^{\text {I }}$ IB |  | - | $\begin{aligned} & 0.8 \\ & 0.5 \\ & \hline \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 52 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \quad\left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 12.5 \mathrm{~V} \leq \mathrm{V}_{1} \leq 22.5 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 12.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 22.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 56 \\ & 56 \end{aligned}$ | $80$ | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{I}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.2$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | 10 | - | 700 | - | mA |

MC78M12C/AC/B/AB ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}$, unless otherwise noted.) (Note 4)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ MC78M12C <br> MC78M12AC | Vo | $\begin{aligned} & 11.50 \\ & 11.76 \end{aligned}$ | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | $\begin{aligned} & 12.50 \\ & 12.24 \end{aligned}$ | Vdc |
| ```Output Voltage Variation ( \(14.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 27 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}\) ) MC78M12C MC78M12AC``` | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 11.4 \\ & 11.5 \end{aligned}$ |  | $\begin{aligned} & 12.6 \\ & 12.5 \end{aligned}$ | Vdc |
| Line Regulation $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 14.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 8.0 | 50 | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  |  | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ | mV |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $I_{\text {IB }}$ | - | 3.2 | 6.0 | mA |
| Quiescent Current Change <br> ( $14.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ ) <br> ( $5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ ) | $\Delta \\|_{\text {IB }}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.5 \\ & \hline \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 75 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\begin{aligned} & \left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 15 \mathrm{~V} \leq \mathrm{V}_{1} \leq 25 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 15 \mathrm{~V} \leq \mathrm{V}_{1} \leq 25 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 55 \\ & 55 \end{aligned}$ | $80$ | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{l}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.3$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | 10 | - | 700 | - | mA |

4. $\begin{aligned} \mathrm{T}_{\text {low }} & =0^{\circ} \mathrm{C} \text { for MC78MxxAC, C } \\ & =-40^{\circ} \mathrm{C} \text { for MC78MxxAB, B }\end{aligned} \quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78MxxAB, AC, B, C

## MC78M00, MC78M00A Series

MC78M15C/AC/B/AB ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}$,
unless otherwise noted.) (Note 5)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ MC78M15C MC78M15AC | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 14.4 \\ & 14.7 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \end{aligned}$ | $\begin{aligned} & 15.6 \\ & 15.3 \end{aligned}$ | Vdc |
| Output Voltage Variation $\begin{aligned} & \left(17.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 30 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right) \\ & \text { MC78M15C } \\ & \text { MC78M15AC } \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 14.25 \\ & 14.40 \end{aligned}$ |  | $\begin{aligned} & 15.75 \\ & 15.60 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Input Regulation } \\ & \qquad\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 17.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right) \end{aligned}$ | Regline | - | 10 | 50 | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload | - |  | $\begin{aligned} & 300 \\ & 150 \end{aligned}$ | mV |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $I_{B}$ | - | 3.2 | 6.0 | mA |
| Quiescent Current Change <br> ( $17.5 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ ) <br> $\left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right.$ ) | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 90 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \quad\left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 18.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 28.5 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 18.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 28.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{array}{r} 54 \\ 54 \\ \hline \end{array}$ | $\overline{70}$ | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{I}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.3$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | Io | - | 700 | - | mA |

MC78M18C ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{I}}=27 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 17.3 | 18 | 18.7 | Vdc |
| Output Voltage Variation $\left(21 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | 17.1 | - | 18.9 | Vdc |
| Line Regulation $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 21 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 33 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 10 | 50 | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 30 \\ & 10 \end{aligned}$ | $\begin{aligned} & 360 \\ & 180 \end{aligned}$ | mV |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | IB | - | 3.2 | 6.5 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & \left(21 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 33 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right) \end{aligned}$ | $\Delta^{\text {I }}$ IB |  | - | $\begin{aligned} & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 100 | - | $\mu \mathrm{V}$ |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \quad\left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 22 \mathrm{~V} \leq \mathrm{V}_{1} \leq 32 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 22 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 32 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 53 \\ & 53 \end{aligned}$ | $\overline{70}$ | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{I}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.3$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | lo | - | 700 | - | mA |

5. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78MxxAC, C $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78MxxAB, AC, B, C
$=-40^{\circ} \mathrm{C}$ for $\mathrm{MC} 78 \mathrm{MxxAB}, \mathrm{B}$

## MC78M00, MC78M00A Series

MC78M20C ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=29 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 19.2 | 20 | 20.8 | Vdc |
| Output Voltage Variation $\left(23 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 35 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | 19 | - | 21 | Vdc |
| Line Regulation $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 23 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 10 | 50 | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 30 \\ & 10 \end{aligned}$ | $\begin{aligned} & 400 \\ & 200 \end{aligned}$ | mV |
| Input Bias Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {IB }}$ | - | 3.2 | 6.5 | mA |
| Quiescent Current Change $\begin{aligned} & \left(23 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right) \end{aligned}$ | $\Delta l_{\text {IB }}$ |  |  | $\begin{aligned} & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 110 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\begin{aligned} & \left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 24 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 34 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 24 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 34 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 52 \\ & 52 \end{aligned}$ | $\overline{70}$ | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{I}}=35 \mathrm{~V}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.5$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | lo | - | 700 | - | mA |

MC78M24C ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=33 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{D}} \leq 5.0 \mathrm{~W}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 23 | 24 | 25 | Vdc |
| Output Voltage Variation $\left(27 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 38 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | 22.8 | - | 25.2 | Vdc |
| Line Regulation $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 27 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{I}} \leq 38 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right)$ | Regline | - | 10 | 50 | mV |
| Load Regulation $\begin{aligned} & \left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 200 \mathrm{~mA}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 30 \\ & 10 \end{aligned}$ | $\begin{aligned} & 480 \\ & 240 \end{aligned}$ | mV |
| Input Bias Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {IB }}$ | - | 3.2 | 7.0 | mA |
| Quiescent Current Change $\begin{aligned} & \left(27 \mathrm{Vdc} \leq \mathrm{V}_{1} \leq 38 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}\right) \end{aligned}$ | $\Delta^{\text {I }}$ IB |  |  | $\begin{aligned} & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 170 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\begin{aligned} & \left(\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 28 \mathrm{~V} \leq \mathrm{V}_{1} \leq 38 \mathrm{~V}\right) \\ & \left(\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, 28 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}} \leq 38 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | $\begin{aligned} & 50 \\ & 50 \end{aligned}$ | $\overline{70}$ | - | dB |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Short Circuit Current Limit ( $\mathrm{J}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | los | - | 50 | - | mA |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | $\pm 0.5$ | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Peak Output Current $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | lo | - | 700 | - | mA |

## MC78M00, MC78M00A Series

## DEFINITIONS

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current - That part of the input current that is not delivered to the load.

Output Noise Voltage - The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability - Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.


Figure 2. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 3. Worst Case Power Dissipation versus Ambient Temperature (TO-220)


Figure 4. Peak Output Current versus Dropout Voltage


Figure 6. Ripple Rejection versus Frequency


Figure 5. Dropout Voltage versus Junction Temperature


Figure 7. Ripple Rejection versus Output Current


Figure 9. Bias Current versus Output Current

## MC78M00, MC78M00A Series

## APPLICATIONS INFORMATION

## Design Considerations

The MC78M00/MC78M00A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the


The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$
\mathrm{I}_{0}=\frac{5.0 \mathrm{~V}}{\mathrm{R}}+\mathrm{I}_{\mathrm{IB}}
$$

$I_{I B}=1.5 \mathrm{~mA}$ over line and load changes.

For example, a 500 mA current source would require $R$ to be a $5.0 \Omega, 10 \mathrm{~W}$ resistor and the output voltage compliance would be the input voltage less 7.0 V .

Figure 10. Current Regulator

$X X=2$ digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by $V_{B E}$ of the pass transistor.

Figure 12. Current Boost Regulator
regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.


The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

Figure 11. Adjustable Output Regulator

$X X=2$ digits of type number indicating voltage.
The circuit of Figure 12 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, $\mathrm{R}_{\mathrm{sc}}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator .Therefore, a 4.0 A plastic power transistor is specified.

Figure 13. Current Boost with Short Circuit Protection

MC78M00, MC78M00A Series
ORDERING INFORMATION

| Device | Output Voltage | Temperature Range | Package | Shipping |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Rails (No Suffix) | Tape \& Reel (RK Suffix) |
| MC78M05CDT/RK | 5.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M05ACDT/RK |  |  |  |  |  |
| MC78M05CT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M05ACT |  |  |  |  |  |
| MC78M05ABDT/RK |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M05ABT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M05BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M05BT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M06CDT/RK | 6.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M06CT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M06BT |  | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |
| MC78M08CDT/RK | 8.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M08ACDT/RK |  |  |  |  |  |
| MC78M08CT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M08ACT |  |  | 10-220 | S0 Unis/Ral | - |
| MC78M08ABDT/RK |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M08ABT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M08BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M08BT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M09CDT/RK | 9.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M09CT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M09BDT/RK |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M09BT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M12CDT/RK | 12 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M12ACDT/RK |  |  |  |  |  |
| MC78M12CT |  |  | TO-220 | 50 Units/Rail |  |
| MC78M12ACT |  |  | 10-220 | 50 Unis/Rall |  |
| MC78M12ABDT/RK |  | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M12ABT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M12BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M12BT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M15CDT/RK | 15 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M15ACDT/RK |  |  |  |  |  |
| MC78M15CT |  |  | 220 | 50 Units/Rail | - |
| MC78M15ACT |  |  | 10-220 | S0 Unis/Ral | - |
| MC78M15ABDT/RK |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M15ABT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M15BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC78M15BT |  |  | TO-220 | 50 Units/Rail | - |
| MC78M18CDT | 18 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK | 75 Units/Rail |  |
| MC78M18CT |  |  | TO-220 | 50 Units/Rail |  |
| MC78M18BT |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |
| MC78M20CT | 20 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |
| MC78M20BT |  | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |
| MC78M24CT | 24 V | $\mathrm{T}_{\mathrm{J}}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |
| MC78M24BT |  | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  |  |

## MC7800, MC7800A, LM340, LM340A Series

### 1.0 A Positive Voltage Regulators

These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 A. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in $2 \%$ and $4 \%$ Tolerance
- Available in Surface Mount D²PAK, DPAK and Standard 3-Lead Transistor Packages

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage (5.0-18 V) | $\mathrm{V}_{\mathrm{I}}$ | 35 | Vdc |
| $(24 \mathrm{~V})$ |  |  |  |$)$

NOTE: ESD data available upon request.

## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


## STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.
XX , These two digits of the type number indicate nominal voltage.

* $\mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter.
${ }^{* *} \mathrm{C}_{0}$ is not needed for stability; however, it does improve transient response. Values of less than $0.1 \mu \mathrm{~F}$ could cause instability.


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 167 of this data sheet. section on page 169 of this data sheet.


Figure 1. Representative Schematic Diagram

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7805B |  |  | MC7805C/LM340T-5 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 4.8 | 5.0 | 5.2 | 4.8 | 5.0 | 5.2 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}}\right. \\ & \leq 15 \mathrm{~W}) \\ & 7.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc} \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\stackrel{-}{4.75}$ | $5.0$ | $5.25$ | $4.75$ |  | $5.25$ | Vdc |
| $\begin{aligned} & \text { Line Regulation (Note 2) } \\ & 7.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc}, 1.0 \mathrm{~A} \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 12 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 5.0 \\ & 1.3 \\ & \hline \end{aligned}$ | $\begin{gathered} 100 \\ 50 \end{gathered}$ |  | $\begin{aligned} & 0.5 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & 20 \\ & 10 \\ & \hline \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | Regload | - | $\begin{gathered} 1.3 \\ 0.15 \end{gathered}$ | $\begin{gathered} 100 \\ 50 \end{gathered}$ | - | $\begin{aligned} & 1.3 \\ & 1.3 \end{aligned}$ | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.2 | 8.0 | - | 3.2 | 6.5 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 7.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | $\Delta_{B}$ | - |  | $\begin{gathered} - \\ 0.5 \end{gathered}$ | - | $\begin{gathered} 0.3 \\ 0.08 \end{gathered}$ | $\begin{aligned} & 1.0 \\ & 0.8 \end{aligned}$ | mA |
| Ripple Rejection <br> $8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 18 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | - | 68 | - | 62 | 83 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 0.9 | - | - | 0.9 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $\mathrm{V}_{\mathrm{in}}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.6 | - | A |
| Peak Output Current ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {O }}$ | - | -0.3 | - | - | -0.3 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7805AB/MC7805AC/LM340AT-5 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 4.9 | 5.0 | 5.1 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right) \\ & 7.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 20 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{0}$ | 4.8 | 5.0 | 5.2 | Vdc |
| Line Regulation (Note 2) $\begin{aligned} & 7.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 12 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 12 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 7.3 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \end{aligned}$ | Regline | - | $\begin{aligned} & 0.5 \\ & 0.8 \\ & 1.3 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 10 \\ & 12 \\ & 4.0 \\ & 10 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Reg ${ }_{\text {load }}$ | - | $\begin{gathered} 1.3 \\ 0.8 \\ 0.53 \end{gathered}$ | $\begin{aligned} & 25 \\ & 25 \\ & 15 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.2 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 7.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta_{B}$ |  | $\begin{gathered} 0.3 \\ - \\ 0.08 \end{gathered}$ | $\begin{aligned} & 0.8 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\text {in }}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=\mathrm{T}_{\text {low }}\right.$ to $T_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7805AB/MC7805AC/LM340AT-5 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Ripple Rejection <br> $8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 18 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | RR | 68 | 83 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \qquad 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | ro | - | 0.9 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $\mathrm{V}_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {}}$ | - | -0.3 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=11 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7806B |  |  | MC7806C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 5.75 | 6.0 | 6.25 | 5.75 | 6.0 | 6.25 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right) \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 21 \mathrm{Vdc} \\ & 9.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 21 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{0}$ | $5.7$ | $\overline{-}$ | $6.3$ | $\begin{gathered} 5.7 \\ - \end{gathered}$ |  | $6.3$ | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \left.\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note } 2\right) \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc} \\ & 9.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 13 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 5.5 \\ & 1.4 \end{aligned}$ | $\begin{gathered} 120 \\ 60 \end{gathered}$ |  | $\begin{aligned} & 0.5 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & 24 \\ & 12 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}(\text { Note } 2) \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | Regload | - | 1.3 | 120 | - | 1.3 | 30 | mV |
| Quiescent Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{I}_{\mathrm{B}}$ | - | 3.3 | 8.0 | - | 3.3 | 8.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta_{B}$ | - | - | $\overline{-}$ |  | $\begin{gathered} 0.3 \\ 0.08 \end{gathered}$ | $\begin{aligned} & 1.3 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $9.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 19 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | - | 65 | - | 58 | 65 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 0.9 | - | - | 0.9 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $V_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV | - | -0.3 | - | - | -0.3 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC7800, MC7800A, LM340, LM340A Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=11 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7806AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 5.88 | 6.0 | 6.12 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right) \\ & 8.6 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 21 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | 5.76 | 6.0 | 6.24 | Vdc |
| Line Regulation (Note 2) $8.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ $9.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 13 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | Regline |  | $\begin{aligned} & 5.0 \\ & 1.4 \end{aligned}$ | $\begin{aligned} & 12 \\ & 15 \end{aligned}$ | mV |
| Load Regulation (Note 2) $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload |  | $\begin{aligned} & 1.3 \\ & 0.9 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & 25 \\ & 25 \\ & 15 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.3 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 9.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 9.0 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 21 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta_{B}$ |  | - | $\begin{aligned} & 0.8 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $9.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 19 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{l}_{\mathrm{O}}=500 \mathrm{~mA}$ | RR | 58 | 65 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | ro | - | 0.9 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $V_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV | - | -0.3 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. )

| Characteristic | Symbol | MC7808B |  |  | MC7808C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 7.7 | 8.0 | 8.3 | 7.7 | 8.0 | 8.3 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right) \\ & 10.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc} \\ & 11.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\overline{-}$ | $\overline{-}$ | $8.4$ | $7.6$ | $8.0$ | 8.4 - | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text {, (Note 2) } \\ & 10.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc} \\ & 11 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 17 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 6.0 \\ & 1.7 \end{aligned}$ | $\begin{aligned} & 160 \\ & 80 \end{aligned}$ | - | $\begin{aligned} & 6.0 \\ & 1.7 \end{aligned}$ | $\begin{aligned} & 32 \\ & 16 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}(\text { Note } 2) \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | Regload | - | 1.4 | 160 | - | 1.4 | 35 | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.3 | 8.0 | - | 3.3 | 8.0 | mA |
| $\begin{gathered} \text { Quiescent Current Change } \\ 10.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc} \\ 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{gathered}$ | $\Delta_{\text {B }}$ | - | - | - | - | - | $\begin{aligned} & 1.0 \\ & 0.5 \\ & \hline \end{aligned}$ | mA |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX
$\mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\text {in }}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{J}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7808B |  |  | MC7808C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Ripple Rejection $11.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 18 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | - | 62 | - | 56 | 62 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $V_{1}-V_{0}$ | - | 2.0 | - | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \qquad 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 0.9 | - | - | 0.9 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ $\mathrm{V}_{\mathrm{in}}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {O}}$ | - | -0.4 | - | - | -0.4 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7808AB/MC7808AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 7.84 | 8.0 | 8.16 | Vdc |
| Output Voltage ( $5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}$ ) $10.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc}$ | $\mathrm{V}_{\mathrm{O}}$ | 7.7 | 8.0 | 8.3 | Vdc |
| Line Regulation (Note 2) <br> $10.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ <br> $11 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 17 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ <br> $10.4 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | Regline |  | $\begin{aligned} & 6.0 \\ & 1.7 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 15 \\ & 18 \\ & 15 \end{aligned}$ | mV |
| Load Regulation (Note 2) $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload |  | $\begin{gathered} 1.4 \\ 1.0 \\ 0.22 \end{gathered}$ | $\begin{aligned} & 25 \\ & 25 \\ & 15 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.3 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 11 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 10.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta_{B}$ |  | - | $\begin{aligned} & 0.8 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $11.5 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 21.5 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | RR | 56 | 62 | - | dB |
| Dropout Voltage ( $\left.\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance f $=1.0 \mathrm{kHz}$ | ro | - | 0.9 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $\mathrm{V}_{\mathrm{in}}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {O }}$ | - | -0.4 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{J}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7809B |  |  | MC7809C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 8.65 | 9.0 | 9.35 | 8.65 | 9.0 | 9.35 | Vdc |
| Output Voltage ( $\left.5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right)$ $11.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 24 \mathrm{Vdc}$ | $\mathrm{V}_{\mathrm{O}}$ | 8.55 | 9.0 | 9.45 | 8.55 | 9.0 | 9.45 | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note 2) } \\ & 11 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 26 \mathrm{Vdc} \\ & 11.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 17 \mathrm{Vdc} \end{aligned}$ | Regline |  | $\begin{aligned} & 6.2 \\ & 1.8 \end{aligned}$ | $\begin{aligned} & 32 \\ & 16 \end{aligned}$ | - | $\begin{aligned} & 6.2 \\ & 1.8 \end{aligned}$ | $\begin{aligned} & 32 \\ & 16 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}(\text { Note } 2) \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | Regload | - | 1.5 | 35 | - | 1.5 | 35 | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.4 | 8.0 | - | 3.4 | 8.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 11.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 26 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta l_{B}$ | - | - | $\begin{aligned} & 1.0 \\ & 0.5 \\ & \hline \end{aligned}$ | - | - | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $11.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 21.5 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | 56 | 61 | - | 56 | 61 | - | dB |
| Dropout Voltage ( $\left.\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $V_{n}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 1.0 | - | - | 1.0 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $\mathrm{V}_{\mathrm{in}}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {}}$ | - | -0.5 | - | - | -0.5 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7812B |  |  | MC7812C/LM340T-12 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 11.5 | 12 | 12.5 | 11.5 | 12 | 12.5 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right) \\ & 14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc} \\ & 15.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\stackrel{-}{11.4}$ | $12$ | $\stackrel{-}{12.6}$ | 11.4 - | 12 - | $12.6$ | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note 2) } \\ & 14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc} \\ & 16 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 22 \mathrm{Vdc} \\ & 14.8 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \end{aligned}$ | Regline |  | $\begin{aligned} & 7.5 \\ & 2.2 \end{aligned}$ | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ |  | $\begin{gathered} 3.8 \\ 0.3 \\ - \end{gathered}$ | $\begin{aligned} & 24 \\ & 24 \\ & 48 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | Regload | - | 1.6 | 240 | - | 8.1 | 60 | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.4 | 8.0 | - | 3.4 | 6.5 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 15 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta l_{B}$ | - | - | $\begin{gathered} - \\ 1.0 \\ 0.5 \end{gathered}$ |  | - | $\begin{aligned} & 0.7 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $15 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | - | 60 | - | 55 | 60 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | - | 2.0 | - | Vdc |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX
$\mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC7800, MC7800A, LM340, LM340A Series

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\text {in }}=19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7812B |  |  | MC7812C/LM340T-12 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance f $=1.0 \mathrm{kHz}$ | ro | - | 1.1 | - | - | 1.1 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $V_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }^{\text {}}$ | - | -0.8 | - | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7812AB/MC7812AC/LM340AT-12 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 11.75 | 12 | 12.25 | Vdc |
| Output Voltage ( $5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}$ ) $14.8 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc}$ | $\mathrm{V}_{\mathrm{O}}$ | 11.5 | 12 | 12.5 | Vdc |
| Line Regulation (Note 2) $\begin{aligned} & 14.8 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 16 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 22 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \\ & 14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \end{aligned}$ | Regline |  | $\begin{aligned} & 3.8 \\ & 2.2 \\ & 6.0 \end{aligned}$ | $\begin{gathered} 18 \\ 20 \\ 120 \end{gathered}$ | mV |
| Load Regulation (Note 2) $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | Regload | - |  | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.4 | 6.0 | mA |
| Quiescent Current Change $\begin{aligned} & 15 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 14.8 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \end{aligned}$ | $\Delta_{B}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $15 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | RR | 55 | 60 | - | dB |
| Dropout Voltage ( $\left.\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | ro | - | 1.1 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ $\mathrm{V}_{\mathrm{in}}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {}}$ | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| $\text { 1. } \begin{aligned} \mathrm{T}_{\text {low }} & =0^{\circ} \mathrm{C} \text { for MC78XXAC, C, LM340AT-XX, LM340T-XX } \\ & =-40^{\circ} \mathrm{C} \text { for MC78XXB, MC78XXAB } \end{aligned}$ | 2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into accou separately. Pulse testing with low duty cycle is used. |  |  |  |  |

## MC7800, MC7800A, LM340, LM340A Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{J}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7815B |  |  | MC7815C/LM340T-15 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 14.4 | 15 | 15.6 | 14.4 | 15 | 15.6 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right) \\ & 17.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc} \\ & 18.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\stackrel{-}{14.25}$ | $15$ | $\stackrel{-}{15.75}$ | $14.25$ |  | $15.75$ | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note } 2 \text { ) } \\ & 17.9 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc} \\ & 20 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 26 \mathrm{Vdc} \end{aligned}$ | $\mathrm{Reg}_{\text {line }}$ | - | $\begin{aligned} & 8.5 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 300 \\ & 150 \end{aligned}$ | - | $\begin{aligned} & 8.5 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 30 \\ & 28 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | Regload | - | 1.8 | 300 | - | 1.8 | 55 | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.5 | 8.0 | - | 3.5 | 6.5 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 17.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc} \\ & 17.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta l_{B}$ |  | - | $\begin{gathered} - \\ 1.0 \\ 0.5 \end{gathered}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.7 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $\text { 18.5 } \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 28.5 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | - | 58 | - | 54 | 58 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \qquad 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 1.2 | - | - | 1.2 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $V_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {}}$ | - | -1.0 | - | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7815AB/MC7815AC/LM340AT-15 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 14.7 | 15 | 15.3 | Vdc |
| Output Voltage ( $\left.5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right)$ $17.9 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}$ | $\mathrm{V}_{\mathrm{O}}$ | 14.4 | 15 | 15.6 | Vdc |
| $\begin{aligned} & \text { Line Regulation (Note 2) } \\ & 17.9 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 20 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 26 \mathrm{Vdc} \\ & 17.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \end{aligned}$ | Regline | - | $\begin{aligned} & 8.5 \\ & 3.0 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & 20 \\ & 22 \\ & 20 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload | - | $\begin{aligned} & 1.8 \\ & 1.5 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & 25 \\ & 25 \\ & 15 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.5 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 17.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 17.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta_{B}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC7800, MC7800A, LM340, LM340A Series

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\text {in }}=23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7815AB/MC7815AC/LM340AT-15 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Ripple Rejection $18.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 28.5 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{l}_{\mathrm{O}}=500 \mathrm{~mA}$ | RR | 60 | 80 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \qquad 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 1.2 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $\mathrm{V}_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {}}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=27 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7818B |  |  | MC7818C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | 17.3 | 18 | 18.7 | 17.3 | 18 | 18.7 | Vdc |
| ```Output Voltage ( \(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\) ) \(21 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc}\) \(22 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc}\)``` | $\mathrm{V}_{\mathrm{O}}$ | - | 18 | $18.9$ | $17.1$ | $18$ | $18.9$ | Vdc |
| $\begin{gathered} \text { Line Regulation, (Note 2) } \\ 21 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc} \\ 24 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc} \end{gathered}$ | Regline | - | $\begin{aligned} & 9.5 \\ & 3.2 \end{aligned}$ | $\begin{aligned} & 360 \\ & 180 \end{aligned}$ | - | $\begin{aligned} & 9.5 \\ & 3.2 \end{aligned}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | mV |
| Load Regulation, (Note 2) $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.5 \mathrm{~A}$ | Regload | - | 2.0 | 360 | - | 2.0 | 55 | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.5 | 8.0 | - | 3.5 | 6.5 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 21 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta l_{B}$ | - | - | $\overline{-}$ | - | - | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection $22 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 33 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | - | 57 | - | 53 | 57 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{il}}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 1.3 | - | - | 1.3 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit $\left(T_{A}=25^{\circ} \mathrm{C}\right)$ $\mathrm{V}_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {}}$ | - | -1.5 | - | - | -1.5 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC7800, MC7800A, LM340, LM340A Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=27 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7818AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 17.64 | 18 | 18.36 | Vdc |
| $\begin{aligned} & \text { Output Voltage }\left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right) \\ & 21 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | 17.3 | 18 | 18.7 | Vdc |
| $\begin{aligned} & \text { Line Regulation (Note 2) } \\ & 21 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 24 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \\ & 24 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 20.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \end{aligned}$ | Regline | - | $\begin{aligned} & 9.5 \\ & 3.2 \\ & 3.2 \\ & 8.0 \end{aligned}$ | $\begin{gathered} 22 \\ 25 \\ 10.5 \\ 22 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload |  | $\begin{aligned} & 2.0 \\ & 1.8 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 25 \\ & 25 \\ & 15 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.5 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 21 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 33 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 21.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta_{B}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection <br> $22 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 32 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | RR | 53 | 57 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance f $=1.0 \mathrm{kHz}$ | ro | - | 1.3 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $\mathrm{V}_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }^{\text {O}}$ | - | -1.5 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=33 \mathrm{~V}, \mathrm{I}_{\mathrm{o}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7824B |  |  | MC7824C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 23 | 24 | 25 | 23 | 24 | 25 | Vdc |
| ```Output Voltage ( \(\left.5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right)\) \(27 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}\) \(28 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}\)``` | $\mathrm{V}_{\mathrm{O}}$ | $\text { - } 22.8$ | $24$ | $25.2$ |  | $24$ | $\begin{gathered} 25.2 \\ - \end{gathered}$ | Vdc |
| $\begin{gathered} \text { Line Regulation, (Note 2) } \\ 27 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc} \\ 30 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 36 \mathrm{Vdc} \end{gathered}$ | Regline |  | $\begin{gathered} 11.5 \\ 3.8 \\ \hline \end{gathered}$ | $\begin{aligned} & 480 \\ & 240 \end{aligned}$ |  |  | $\begin{aligned} & 60 \\ & 48 \end{aligned}$ | mV |
| Load Regulation, (Note 2) $5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}$ | Regload | - | 2.1 | 480 | - | 4.4 | 65 | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.6 | 8.0 | - | 3.6 | 6.5 | mA |
| $\begin{gathered} \text { Quiescent Current Change } \\ 27 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc} \\ 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{gathered}$ | $\Delta_{B}$ | - |  | $\overline{-}$ |  | - | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC7800, MC7800A, LM340, LM340A Series

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\text {in }}=33 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | MC7824B |  |  | MC7824C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Ripple Rejection $28 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 38 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}$ | RR | - | 54 | - | 50 | 54 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(T_{A}=25^{\circ} \mathrm{C}\right) \\ & \qquad 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance $\mathrm{f}=1.0 \mathrm{kHz}$ | ro | - | 1.4 | - | - | 1.4 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $\mathrm{V}_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }_{\text {O }}$ | - | -2.0 | - | - | -2.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=33 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | MC7824AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | 23.5 | 24 | 24.5 | Vdc |
| Output Voltage ( $\left.5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq 15 \mathrm{~W}\right)$ $27.3 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}$ | $\mathrm{V}_{\mathrm{O}}$ | 23.2 | 24 | 25.8 | Vdc |
| Line Regulation (Note 2) $\begin{aligned} & 27 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 30 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 36 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \\ & 30 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 36 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 26.7 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \end{aligned}$ | Regline |  | $\begin{gathered} 11.5 \\ 3.8 \\ 3.8 \\ 10 \end{gathered}$ | $\begin{aligned} & 25 \\ & 28 \\ & 12 \\ & 25 \end{aligned}$ | mV |
| Load Regulation (Note 2) $\begin{aligned} & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload |  | $\begin{aligned} & 2.1 \\ & 2.0 \\ & 1.8 \end{aligned}$ | $\begin{aligned} & 15 \\ & 25 \\ & 15 \end{aligned}$ | mV |
| Quiescent Current | $\mathrm{I}_{\mathrm{B}}$ | - | 3.6 | 6.0 | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & 27.3 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & 27 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta_{B}$ |  | - | $\begin{aligned} & 0.8 \\ & 0.8 \\ & 0.5 \end{aligned}$ | mA |
| Ripple Rejection <br> $28 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 38 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | RR | 45 | 54 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{0}$ | - | 2.0 | - | Vdc |
| $\begin{aligned} & \text { Output Noise Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | ro | - | 1.4 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) $V_{\text {in }}=35 \mathrm{Vdc}$ | Isc | - | 0.2 | - | A |
| Peak Output Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 2.2 | - | A |
| Average Temperature Coefficient of Output Voltage | TCV ${ }^{\text {O}}$ | - | -2.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $\quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$ for MC78XXAC, C, LM340AT-XX, LM340T-XX $=-40^{\circ} \mathrm{C}$ for MC78XXB, MC78XXAB
2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7800, MC7800A, LM340, LM340A Series


Figure 2. Peak Output Current as a Function of Input/Output Differential Voltage (MC78XXC, AC, B)


Figure 3. Ripple Rejection as a Function of Output Voltages (MC78XXC, AC, B)


Figure 4. Ripple Rejection as a Function of Frequency (MC78XXC, AC, B)


Figure 5. Output Voltage as a Function of Junction Temperature (MC7805C, AC, B)


Figure 7. Quiescent Current as a Function of Temperature (MC78XXC, AC, B)

## MC7800, MC7800A, LM340, LM340A Series

## APPLICATIONS INFORMATION

## Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long

The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$
\begin{gathered}
\mathrm{I}_{\mathrm{O}}=\frac{5.0 \mathrm{~V}}{\mathrm{R}}+\mathrm{I}_{\mathrm{B}} \\
\mathrm{I}_{\mathrm{B}} \cong 3.2 \mathrm{~mA} \text { over line and load changes. }
\end{gathered}
$$

For example, a 1.0 A current source would require R to be a $5.0 \Omega$, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V .

Figure 8. Current Regulator

$X X=2$ digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor $R$ in conjunction with the $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/output differential voltage minimum is increased by $\mathrm{V}_{\mathrm{BE}}$ of the pass transistor.
wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.


The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

Figure 9. Adjustable Output Regulator


The circuit of Figure 10 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, $\mathrm{R}_{\mathrm{SC}}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

Figure 10. Current Boost Regulator
Figure 11. Short Circuit Protection


Figure 12. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)


Figure 13. Input Output Differential as a Function of Junction Temperature (MC78XXC, AC, B)


Figure 14. D2PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 15. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC7800, MC7800A, LM340, LM340A Series

## DEFINITIONS

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current - That part of the input current that is not delivered to the load.

Output Noise Voltage - The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.
Long Term Stability - Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

| Device | Output Voltage | Temperature Range | Package | Shipping |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Rails (No Suffix) | Tape \& Reel (R4 Suffix) |
| MC7805.2CT | 5.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-220 | 50 Units/Rail | - |
| MC7805ACD2T/R4 |  |  | D2PAK |  | 800 Units/Reel |
| MC7805ACT |  |  | TO-220 |  | - |
| MC7805CD2T/R4 |  |  | D2PAK |  | 800 Units/Reel |
| MC7805CT |  |  | TO-220 |  | - |
| MC7805CDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| LM340T-5 |  |  | TO-220 | 50 Units/Rail | - |
| LM340AT-5 |  |  |  |  |  |
| MC7805BD2T/R4 |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK |  | 800 Units/Reel |
| MC7805BT |  |  | TO-220 |  | - |
| MC7805BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC7805ABD2T/R4 |  |  | D2PAK | 50 Units/Rail | 800 Units/Reel |
| MC7805ABT |  |  | TO-220 |  | - |
| MC7806ACT | 6.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-220 |  | - |
| MC7806CT |  |  |  |  | - |
| MC7806BD2T/R4 |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK |  | 800 Units/Reel |
| MC7806BT |  |  | TO-220 |  | - |
| MC7808ACT | 8.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  | - |
| MC7808CD2T/R4 |  |  | D2PAK |  | 800 Units/Reel |
| MC7808CT |  |  | TO-220 |  | - |
| MC7808CDT/RK/T5 |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC7808BD2T/R4 |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK | 50 Units/Rail | 800 Units/Reel |
| MC7808BT |  |  | TO-220 |  | - |
| MC7808BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC7808ABD2T/R4 |  |  | D2PAK | 50 Units/Rail | 800 Units/Reel |
| MC7808ABT |  |  | TO-220 |  | - |

ORDERING INFORMATION (continued)

| Device | Output Voltage | Temperature Range | Package | Shipping |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Rails <br> (No Suffix) | Tape \& Reel (R4 Suffix) |
| MC7809ACT | 9.0 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-220 | 50 Units/Rail | - |
| MC7809CD2T/R4 |  |  | D2PAK |  | 800 Units/Reel |
| MC7809CT |  |  | TO-220 |  | - |
| MC7809BT |  | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  | - |
| MC7812ACD2T/R4 | 12 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK |  | 800 Units/Reel |
| MC7812ACT |  |  | TO-220 |  | - |
| MC7812CD2T/R4 |  |  | D2PAK |  | 800 Units/Reel |
| MC7812CT |  |  | TO-220 |  | - |
| MC7812CDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| LM340T-12 |  |  | TO-220 | 50 Units/Rail | - |
| LM340AT-12 |  |  | TO-220 |  |  |
| MC7812BD2T/R4 |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK |  | 800 Units/Reel |
| MC7812BT |  |  | TO-220 |  | - |
| MC7812BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC7812ABD2T/R4 |  |  | D2PAK | 50 Units/Rail | 800 Units/Reel |
| MC7812ABT |  |  | TO-220 |  | - |
| MC7815ACD2T/R4 | 15 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK |  | 800 Units/Reel |
| MC7815ACT |  |  | TO-220 |  | - |
| MC7815CD2T/R4 |  |  | D2PAK |  | 800 Units/Reel |
| MC7815CT |  |  |  |  |  |
| LM340T-15 |  |  | TO-220 |  | - |
| LM340AT-15 |  |  |  |  |  |
| MC7815CDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC7815BD2T/R4 |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK | 50 Units/Rail | 800 Units/Reel |
| MC7815BT |  |  | TO-220 |  | - |
| MC7815BDT/RK |  |  | DPAK | 75 Units/Rail | 2500 Units/Reel |
| MC7815ABD2T/R4 |  |  | D2PAK | 50 Units/Rail | 800 Units/Reel |
| MC7815ABT |  |  | TO-220 |  | - |
| MC7818ACT | 18 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-220 |  | - |
| MC7818CD2T/R4 |  |  | D2PAK |  | 800 Units/Reel |
| MC7818CT |  |  | TO-220 |  | - |
| MC7818BT |  | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  | - |
| MC7824ACT | 24 V | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ |  |  | - |
| MC7824CD2T |  |  | D2PAK |  |  |
| MC7824CT |  |  | TO-220 |  | - |
| MC7824BD2T/R4 |  | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | D2PAK |  | 800 Units/Reel |
| MC7824BT |  |  | TO-220 |  | - |

## MC7800, MC7800A, LM340, LM340A Series

MARKING DIAGRAMS

TO-220
T SUFFIX
CASE 221A

## MC7800, MC7800A Series LM340, LM340A Series



D2PAK
D2T SUFFIX CASE 936


| XX | $=$ Voltage Option |
| :--- | :--- |
| XX | $=$ Appropriate Suffix Options |
| A | $=$ Assembly Location |
| WL, L | $=$ Wafer Lot |
| Y | $=$ Year |
| WW | $=$ Work Week |

### 3.0 A Positive Voltage Regulators

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 A. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a $2 \%$ output voltage tolerance, on AC-suffix 5.0, 12 and 15 V device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to supply up to 15 A at the nominal output voltage.

- Output Current in Excess of 3.0 A
- Power Dissipation: 25 W
- No External Components Required
- Output Voltage Offered in $2 \%$ and $4 \%$ Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation


## MC78T00 Series

## THREE-AMPERE POSITIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

T SUFFIX
PLASTIC PACKAGE CASE 221A

Pin 1. Input
2. Ground
3. Output


Heatsink surface is connected to Pin 2.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

| MC78T05 | 5.0 V | MC78T12 | 12 V |
| :--- | :--- | :--- | :--- |
| MC78T08 | 8.0 V | MC78T15 | 15 V |

ORDERING INFORMATION

| Device | $\begin{aligned} & \mathrm{V}_{\mathrm{o}} \\ & \mathrm{Tol} . \end{aligned}$ | Operating Temperature Range | Package |
| :---: | :---: | :---: | :---: |
| MC78TXXCT | 4\% | $\mathrm{T}_{\mathrm{J}}=0^{\circ}$ to | Plastic |
| MC78TXXACT | 2\%* | $+125^{\circ} \mathrm{C}$ | Power |
| MC78TXXBT\# | 4\% | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to | Plastic |
| MC78TXXABT\# | 2\%* | $+125^{\circ} \mathrm{C}$ | Power |

XX Indicates nominal voltage.

* $2 \%$ regulators available in 5,12 and 15 V devices.
\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local ON Semiconductor sales office for information.

A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.
XX these two digits of the type number indicate voltage.

* $\mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)
${ }^{* *} \mathrm{C}_{0}$ is not needed for stability; however, it does improve transient response.

MAXIMUM RATINGS $\left(T_{A}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Voltage } \begin{array}{c} (5.0 \mathrm{~V}-12 \mathrm{~V}) \\ (15 \mathrm{~V}) \end{array} \end{aligned}$ | $V_{1}$ | $\begin{aligned} & 35 \\ & 40 \end{aligned}$ | Vdc |
| Power Dissipation and Thermal Characteristics Plastic Package (Note 1) $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Case | $P_{D}$ <br> $\mathrm{R}_{\text {ӨJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJC }}$ | Internally Limited 65 Internally Limited 2.5 | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Storage Junction Temperature | $\mathrm{T}_{\text {stg }}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range (MC78T00C, AC) | TJ | 0 to +125 | ${ }^{\circ} \mathrm{C}$ |

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_{\mathrm{O}} \leq \mathrm{P}_{\max }, \mathrm{P}_{\max }=25 \mathrm{~W}$.
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{O}} \leq \mathrm{P}_{\max }\right.$ [Note 1], unless otherwise noted.)

| Characteristics | Symbol | MC78T05AC |  |  | MC78T05C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A} ;\right. \\ & \left.5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 2.0 \mathrm{~A}, 7.3 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 4.9 \\ & 4.8 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 5.1 \\ & 5.2 \end{aligned}$ | $\begin{gathered} 4.8 \\ 4.75 \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 5.2 \\ 5.25 \end{gathered}$ | Vdc |
| $\begin{aligned} & \text { Line Regulation (Note 2) } \\ & \text { (7.2 Vdc } \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} ; \\ & 7.2 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} ; \\ & 8.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 12 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} ; \\ & 7.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \text { ) } \end{aligned}$ | Regline | - | 3.0 | 25 | - | 3.0 | 25 | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | Regload | - | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & 30 \\ & 80 \end{aligned}$ | - | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & 30 \\ & 80 \end{aligned}$ | mV |
| Thermal Regulation <br> (Pulse $=10 \mathrm{~ms}, \mathrm{P}=20 \mathrm{~W}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) | Regtherm | - | 0.001 | 0.01 | - | 0.002 | 0.03 | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| $\begin{aligned} & \text { Quiescent Current } \\ & \qquad\left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{B}}$ | - | $\begin{aligned} & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | - | $\begin{aligned} & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & \text { (7.2 Vdc } \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} ; \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} ; \\ & 7.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 20 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \text { ) } \end{aligned}$ | $\Delta \mathrm{l}_{\mathrm{B}}$ | - | 0.3 | 1.0 | - | 0.3 | 1.0 | mA |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \quad\left(8.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{in}} \leq 18 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz},\right. \\ & \left.\mathrm{I}_{\mathrm{O}}=2.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 62 | 75 | - | 62 | 75 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{0}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - | 2.2 | 2.5 | - | 2.2 | 2.5 | Vdc |
| Output Noise Voltage $\left(10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $\mathrm{R}_{\mathrm{O}}$ | - | 2.0 | - | - | 20 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit $\left(\mathrm{V}_{\text {in }}=35 \mathrm{Vdc}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | Isc | - | 1.5 | - | - | 1.5 | - | A |
| Peak Output Current ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 5.0 | - | - | 5.0 | - | A |
| Average Temperature Coefficient of Output Voltage $(\mathrm{lo}=5.0 \mathrm{~mA})$ | TCV | - | 0.2 | - | - | 0.2 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_{0} \leq P_{\max }, P_{\max }=25 \mathrm{~W}$.
2. Line and load regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T00 Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=13 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{O}} \leq \mathrm{P}_{\max }\right.$ [Note 1], unless otherwise noted.)

| Characteristics | Symbol | MC78T08C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A} ;\right. \\ & \left.5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 2.0 \mathrm{~A}, 10.4 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 7.7 \\ & 7.6 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 8.3 \\ & 8.4 \end{aligned}$ | Vdc |
| Line Regulation (Note 2) <br> ( $10.3 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ <br> $10.3 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ <br> $11 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 17 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ <br> $10.7 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ ) | Regline | - | 4.0 | 35 | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | Regload | - | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & 30 \\ & 80 \end{aligned}$ | mV |
| Thermal Regulation $\left(\text { Pulse }=10 \mathrm{~ms}, \mathrm{P}=20 \mathrm{~W}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{Reg}_{\text {therm }}$ | - | 0.002 | 0.03 | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| $\begin{aligned} & \text { Quiescent Current } \\ & \qquad\left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{B}}$ | - | $\begin{aligned} & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & \left(10.3 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right. \text {; } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} ; \\ & 10.7 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 23 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \text { ) } \end{aligned}$ | $\Delta l_{B}$ | - | 0.3 | 1.0 | mA |
| Ripple Rejection <br> ( $11 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 21 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\mathrm{O}}=2.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | RR | 60 | 71 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - | 2.2 | 2.5 | Vdc |
| Output Noise Voltage $\left(10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $\mathrm{R}_{\mathrm{O}}$ | - | 2.0 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit $\left(\mathrm{V}_{\mathrm{in}}=35 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | Isc | - | 1.5 | - | A |
| Peak Output Current ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 5.0 | - | A |
| Average Temperature Coefficient of Output Voltage ( $\mathrm{l}_{\mathrm{O}}=5.0 \mathrm{~mA}$ ) | TCV ${ }_{\text {}}$ | - | 0.3 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $\mathrm{P}_{\mathrm{O}} \leq \mathrm{P}_{\max }, \mathrm{P}_{\max }=25 \mathrm{~W}$.
2. Line and load regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T00 Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=17 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{O}} \leq \mathrm{P}_{\max }\right.$ [Note 1], unless otherwise noted. $)$

| Characteristics | Symbol | MC78T12AC |  |  | MC78T12C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A},\right. \\ & \left.5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 2.0 \mathrm{~A}, 14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{gathered} 11.75 \\ 11.5 \end{gathered}$ | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | $\begin{gathered} 12.25 \\ 12.5 \end{gathered}$ | $\begin{aligned} & 11.5 \\ & 11.4 \end{aligned}$ | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | $\begin{aligned} & 12.5 \\ & 12.6 \end{aligned}$ | Vdc |
| Line Regulation (Note 2) <br> ( $14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$; <br> $14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$; <br> $16 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 22 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$; <br> $14.9 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc}, \mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~A}$ ) | Regline | - | 6.0 | 45 | - | 6.0 | 45 | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | Regload | - | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & 30 \\ & 80 \end{aligned}$ | - | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & 30 \\ & 80 \end{aligned}$ | mV |
| Thermal Regulation <br> (Pulse $=10 \mathrm{~ms}, \mathrm{P}=20 \mathrm{~W}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{Reg}_{\text {therm }}$ | - | 0.001 | 0.01 | - | 0.002 | 0.03 | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| $\begin{aligned} & \text { Quiescent Current } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{B}}$ | - | $\begin{aligned} & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | - | $\begin{aligned} & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & \quad\left(14.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 35 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right. \text {; } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} ; \\ & 14.9 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 27 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \text { ) } \end{aligned}$ | $\Delta_{B}$ | - | 0.3 | 1.0 | - | 0.3 | 1.0 | mA |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \left(15 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 25 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz},\right. \\ & \left.\mathrm{I}_{\mathrm{O}}=2.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 57 | 67 | - | 57 | 67 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{0}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $V_{\text {in }}-V_{0}$ | - | 2.2 | 2.5 | - | 2.2 | 2.5 | Vdc |
| Output Noise Voltage <br> ( $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $\mathrm{R}_{\mathrm{O}}$ | - | 2.0 | - | - | 20 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit $\left(\mathrm{V}_{\text {in }}=35 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | Isc | - | 1.5 | - | - | 1.5 | - | A |
| Peak Output Current ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 5.0 | - | - | 5.0 | - | A |
| Average Temperature Coefficient of Output Voltage ( $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}$ ) | TCV | - | 0.5 | - | - | 0.5 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $\mathrm{P}_{\mathrm{O}} \leq \mathrm{P}_{\max }, \mathrm{P}_{\max }=25 \mathrm{~W}$.
2. Line and load regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## MC78T00 Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=20 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}, \mathrm{P}_{\mathrm{O}} \leq \mathrm{P}_{\max }\right.$ [Note 1], unless otherwise noted.)

| Characteristics | Symbol | MC78T15AC |  |  | MC78T15C |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A} ;\right. \\ & \left.5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 2.0 \mathrm{~A}, 17.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 14.7 \\ & 14.4 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \end{aligned}$ | $\begin{aligned} & 15.3 \\ & 15.6 \end{aligned}$ | $\begin{gathered} 14.4 \\ 14.25 \end{gathered}$ | $\begin{aligned} & 15 \\ & 15 \end{aligned}$ | $\begin{gathered} 15.6 \\ 15.75 \end{gathered}$ | Vdc |
| Line Regulation (Note 2) $\begin{aligned} & \left(17.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} ;\right. \\ & 17.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}+225^{\circ} \mathrm{C} ; \\ & 20 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 26 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} ; \\ & \left.18 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}\right) \end{aligned}$ | Regline | - | 7.5 | 55 | - | 7.5 | 55 | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | Regload | - | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & 30 \\ & 80 \end{aligned}$ | - | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & 30 \\ & 80 \end{aligned}$ | mV |
| Thermal Regulation <br> (Pulse $=10 \mathrm{~ms}, \mathrm{P}=20 \mathrm{~W}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) | Regtherm | - | 0.001 | 0.01 | - | 0.002 | 0.03 | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| $\begin{aligned} & \text { Quiescent Current } \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \\ & \left(5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{B}}$ | - | $\begin{aligned} & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | - | $\begin{aligned} & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 6.0 \end{aligned}$ | mA |
| $\begin{aligned} & \text { Quiescent Current Change } \\ & \quad\left(17.6 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} ;\right. \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} ; \\ & \left.18 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}\right) \end{aligned}$ | $\Delta_{B}$ | - | 0.3 | 1.0 | - | 0.3 | 1.0 | mA |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \quad\left(18.5 \mathrm{Vdc} \leq \mathrm{V}_{\text {in }} \leq 28.5 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}\right. \text {, } \\ & \left.\mathrm{I}_{\mathrm{O}}=2.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 55 | 65 | - | 55 | 65 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{0}=3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - | 2.2 | 2.5 | - | 2.2 | 2.5 | Vdc |
| Output Noise Voltage <br> ( $10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} / \mathrm{V}_{\mathrm{O}}$ |
| Output Resistance ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $\mathrm{R}_{\mathrm{O}}$ | - | 2.0 | - | - | 20 | - | $\mathrm{m} \Omega$ |
| Short Circuit Current Limit $\left(\mathrm{V}_{\text {in }}=40 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | Isc | - | 1.0 | - | - | 1.0 | - | A |
| Peak Output Current ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $I_{\text {max }}$ | - | 5.0 | - | - | 5.0 | - | A |
| Average Temperature Coefficient of Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}\right)$ | TCV | - | 0.6 | - | - | 0.6 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $\mathrm{P}_{\mathrm{O}} \leq \mathrm{P}_{\max }, \mathrm{P}_{\max }=25 \mathrm{~W}$.
2. Line and load regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

## VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration $(<100 \mu \mathrm{~s})$ and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms ) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power

t , TIME ( $2.0 \mathrm{~ms} / \mathrm{DIV}$ )

$$
\begin{array}{ll}
\mathrm{V}_{\text {out }}=5.0 \mathrm{~V} & \text { (1) }=\text { Reg }_{\text {line }}=2.4 \mathrm{mV} \\
\mathrm{~V}_{\text {in }}=8.0 \mathrm{~V} \rightarrow 18 \mathrm{~V} \rightarrow 8.0 \mathrm{~V} & \text { (2) }=\text { Reg }_{\text {therm }}=0.0015 \% \mathrm{~V} / \mathrm{W}
\end{array}
$$

Figure 1. MC78T05AC Line and Thermal Regulation
can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms , additional changes in the output voltage are due to the temperature coefficient of the device.
Figure 1 shows the line and thermal regulation response of a typical MC78T05AC to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled (1) and the thermal regulation component is labeled (2). Figure 2 shows the load and thermal regulation response of a typical MC78T05AC to a 20 W load pulse. The output voltage variation due to load regulation is labeled (1) and the thermal regulation component is labeled (2).


Figure 2. MC78T05AC Load and Thermal Regulation


Representative Schematic Diagram

## MC78T00 Series



Figure 3. Temperature Stability


Figure 5. Ripple Rejection versus Frequency


Figure 7. Quiescent Current versus Input Voltage


Figure 4. Output Impedance


Figure 6. Ripple Rejection versus Output Current


Figure 8. Quiescent Current versus Output Current


Figure 9. Dropout Voltage


Figure 10. Peak Output Current


Figure 11. Line Transient Response


Figure 12. Load Transient Response


Figure 13. Maximum Average Power
Dissipation for MC78T00CT, ACT

## MC78T00 Series

## APPLICATIONS INFORMATION

## Design Considerations

The MC78T00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the
regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.


The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation the MC78T05 is chosen in this application. Resistor R determines the current as follows:

$$
\mathrm{I}_{0}=\frac{5.0 \mathrm{~V}}{\mathrm{R}}+\mathrm{I}_{\mathrm{B}}
$$

$\Delta \mathrm{l}_{\mathrm{B}} \cong 0.7 \mathrm{~mA}$ over line, load and Temperature changes $I_{B} \cong 3.5 \mathrm{~mA}$
For example, a 2.0 A current source would require R to be a $2.5 \Omega$, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V .

Figure 14. Current Regulator

$X X=2$ digits of type number indicating voltage.
The MC78T00 series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A . Resistor $R$ in conjunction with the $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by the $\mathrm{V}_{\mathrm{BE}}$ of the pass transistor.


The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

Figure 15. Adjustable Output Regulator

$X X=2$ digits of type number indicating voltage.
The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, $\mathrm{R}_{\mathrm{SC}}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

Figure 16. Current Boost Regulator
Figure 17. Current Boost With Short Circuit Protection

### 3.0 A Positive Voltage Regulators

The LM323,A are monolithic integrated circuits which supply a fixed positive 5.0 V output with a load driving capability in excess of 3.0 A. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. The A-suffix is an improved device with superior electrical characteristics and a $2 \%$ output voltage tolerance. These regulators are offered with a $0^{\circ}$ to $+125^{\circ} \mathrm{C}$ temperature range in a low cost plastic power package.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. These devices can be used with a series pass transistor to supply up to 15 A at 5.0 V .

- Output Current in Excess of 3.0 A
- Available with $2 \%$ Output Voltage Tolerance
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits


## LM323, LM323A

## 3-AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATORS

## SEMICONDUCTOR TECHNICAL DATA

## TSUFFIX

PLASTIC PACKAGE
CASE 221A

Pin 1. Input
2. Ground
3. Output


Heatsink surface is connected to Pin 2.

| ORDERING INFORMATION |  |  |  |
| :--- | :---: | :---: | :---: |
| Device Output <br> Voltage <br> Tolerance Operating <br> Temperature <br> Range Package |  |  |  |
| LM323T | $4 \%$ | $T_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | Plastic <br> Power |
| LM323AT | $2 \%$ |  |  |

## Simplified Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

[^5]MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {in }}$ | 20 | Vdc |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | W |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | 0 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 s) | $\mathrm{T}_{\text {solder }}$ | 300 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(T_{J}=T_{\text {low }}\right.$ to $T_{\text {high }}$ [Note 1], unless otherwise noted.)

| Characteristics | Symbol | LM323A |  |  | LM323 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage $\left(\mathrm{V}_{\text {in }}=7.5 \mathrm{~V}, 0 \leq \mathrm{I}_{\text {out }} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | 4.9 | 5.0 | 5.1 | 4.8 | 5.0 | 5.2 | V |
| $\begin{aligned} & \text { Output Voltage } \\ & \left(7.5 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 15 \mathrm{~V}, 0 \leq \mathrm{I}_{\text {out }} \leq 3.0 \mathrm{~A},\right. \\ & \left.\mathrm{P} \leq \mathrm{P}_{\max }\right)(\text { Note } 2) \end{aligned}$ | Vo | 4.8 | 5.0 | 5.2 | 4.75 | 5.0 | 5.25 | V |
| Line Regulation $\left(7.5 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 15 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)(\text { Note } 3)$ | Regline | - | 1.0 | 15 | - | 1.0 | 25 | mV |
| Load Regulation $\left(\mathrm{V}_{\text {in }}=7.5 \mathrm{~V}, 0 \leq \mathrm{I}_{\text {out }} \leq 3.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ <br> (Note 3) | Regload | - | 10 | 50 | - | 10 | 100 | mV |
| Thermal Regulation $\left(\text { Pulse }=10 \mathrm{~ms}, \mathrm{P}=20 \mathrm{~W}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | Regtherm | - | 0.001 | 0.01 | - | 0.002 | 0.03 | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| Quiescent Current $\left(7.5 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 15 \mathrm{~V}, 0 \leq \mathrm{l}_{\text {out }} \leq 3.0 \mathrm{~A}\right)$ | $\mathrm{I}_{\mathrm{B}}$ | - | 3.5 | 10 | - | 3.5 | 20 | mA |
| Output Noise Voltage <br> $\left(10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ ) | $\mathrm{V}_{\mathrm{N}}$ | - | 40 | - | - | 40 | - | $\mu \mathrm{V}_{\text {rms }}$ |
| $\begin{aligned} & \text { Ripple Rejection } \\ & \quad\left(8.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 18 \mathrm{~V}, \mathrm{I}_{\text {out }}=2.0 \mathrm{~A},\right. \\ & \left.\mathrm{f}=120 \mathrm{~Hz}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | RR | 66 | 75 | - | 62 | 75 | - | dB |
| Short Circuit Current Limit $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=15 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\text {in }}=7.5 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right) \end{aligned}$ | Isc | - | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | - | - | $\begin{aligned} & 4.5 \\ & 5.5 \end{aligned}$ | - | A |
| Long Term Stability | S | - | - | 35 | - | - | 35 | mV |
| Thermal Resistance, Junction-to-Case (Note 4) | $\mathrm{R}_{\text {®JC }}$ | - | 2.0 | - | - | 2.0 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

NOTES: 1 . $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$
2. Although power dissipation is internally limited, specifications apply only for $\mathrm{P} \leq \mathrm{P}_{\max }=25 \mathrm{~W}$.
3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width $\leq 1.0 \mathrm{~ms}$ and a duty cycle $\leq 5 \%$.
4. Without a heatsink, the thermal resistance $\left(\mathrm{R}_{\theta \mathrm{JA}}\right.$ is $\left.65^{\circ} \mathrm{C} / \mathrm{W}\right)$. With a heatsink, the effective thermal resistance can approach the specified values of $2.0^{\circ} \mathrm{C} / \mathrm{W}$, depending on the efficiency of the heatsink.

Representative Schematic Diagram


## VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration $(<100 \mu \mathrm{~s})$ and are strictly a function of electrical gain. However, pulse widths of longer duration ( $>1.0 \mathrm{~ms}$ ) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output
voltage change per watt. The change in dissipated power can be caused by a change in either input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms , additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM323A to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled $\AA$ and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical LM323A to a 20 W load pulse. The output voltage variation due to load regulation is labeled $A$ and the thermal regulation component is labeled Á.

$$
\begin{array}{ll}
\mathrm{V}_{\text {out }}=5.0 \mathrm{~V} & \text { (1) }=\text { Reg }_{\text {line }}=2.4 \mathrm{mV} \\
\mathrm{~V}_{\text {in }}=8.0 \mathrm{~V} \rightarrow 18 \mathrm{~V} \rightarrow 8.0 \mathrm{~V} & \text { (2) }=\text { Reg }_{\text {therm }}=0.0015 \% \mathrm{~V}_{0} / \mathrm{W} \\
\mathrm{I}_{\text {out }}=2.0 \mathrm{~A} &
\end{array}
$$


t , TIME ( $2.0 \mathrm{~ms} /$ DIV)

$$
\begin{array}{ll}
\mathrm{V}_{\text {out }}=5.0 \mathrm{~V} & \text { (1) }=\text { Reg }_{\text {line }}=5.4 \mathrm{mV} \\
\mathrm{~V}_{\text {in }}=15 \mathrm{~V} & \\
\mathrm{I}_{\text {out }}=0 \mathrm{~A} \rightarrow 2.0 \mathrm{~A} \rightarrow 0 \mathrm{~A} & \text { (2) }=\text { Reg }_{\text {therm }}=0.0015 \% \mathrm{~V}_{0} / \mathrm{W}
\end{array}
$$

Figure 2. Load and Thermal Regulation


Figure 3. Temperature Stability


Figure 5. Ripple Rejection versus Frequency


Figure 4. Output Impedance


Figure 6. Ripple Rejection versus Output Current


Figure 7. Quiescent Current versus Input Voltage


Figure 8. Quiescent Current versus Output Current


Figure 9. Dropout Voltage


Figure 11. Line Transient Response


Figure 10. Short Circuit Current


Figure 12. Load Transient Response

## APPLICATIONS INFORMATION

## Design Considerations

The LM323,A series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the
regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.


The LM323,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$
\mathrm{I}_{0}=\frac{5.0 \mathrm{~V}}{\mathrm{R}}+\mathrm{I}_{\mathrm{B}}
$$

$\Delta \mathrm{l}_{\mathrm{B}} \cong 0.7 \mathrm{~mA}$ over line, load and temperature changes $\mathrm{I}_{\mathrm{B}} \cong 3.5 \mathrm{~mA}$

For example, a 2.0 A current source would require R to be a $2.5 \Omega$, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 V .

Figure 13. Current Regulator


The LM323, A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A . Resistor R in conjunction with the $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by the $\mathrm{V}_{\mathrm{BE}}$ of the pass transistor.

Figure 15. Current Boost Regulator


The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

Figure 14. Adjustable Output Regulator


The circuit of Figure 16 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, $\mathrm{R}_{\mathrm{SC}}$, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, an 8.0 A power transistor is specified.

Figure 16. Current Boost with Short Circuit Protection

## 100 mA Negative Voltage Regulators

The MC79L00, A Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA . Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either $\pm 5 \%$ (AC) or $\pm 10 \%$ (C) Selections

* Automotive temperature range selections are available with special test conditions and additional tests in 5,12 and 15 V devices. Contact your local ON Semiconductor sales office for information.


## MC79L00, MC79L00A Series

## THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

*SOP-8 is an internally modified SO-8 package. Pins $2,3,6$, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 package.

| Device No. <br> $\pm \mathbf{1 0 \%}$ | Device No. <br> $\mathbf{5 \%}$ | Nominal <br> Voltage |
| :---: | :---: | :---: |
| MC79L05C | MC79L05AC | -5.0 |
| MC79L12C | MC79L12AC | -12 |
| MC79L15C | MC79L15AC | -15 |
| MC79L18C | MC79L18AC | -18 |
| MC79L24C | MC79L24AC | -24 |

ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
| :---: | :---: | :---: |
| MC79LXXACD* | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 |
| MC79LXXACP |  | Plastic Power |
| MC79LXXCP |  | Plastic Power |
| MC79LXXABD* | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 |
| MC79LXXABP* |  | Plastic Power |

$X X$ indicates nominal voltage

MAXIMUM RATINGS $\left(T_{A}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage ( -5 V ) |  |  |  |
| $(-12,-15,-18 \mathrm{~V})$ |  |  |  |
| $(-24 \mathrm{~V})$ | $\mathrm{V}_{\mathrm{I}}$ | -30 | Vdc |
|  |  | -35 |  |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}+125^{\circ} \mathrm{C}\right.$ (for MC79LXXAB), $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$ (for MC79LXXAC)).

| Characteristics | Symbol | MC79L05C, AB |  |  | MC79L05AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | -4.6 | -5.0 | -5.4 | -4.8 | -5.0 | -5.2 | Vdc |
| $\begin{aligned} & \text { Input Regulation }\left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right) \\ & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-20 \mathrm{Vdc} \\ & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-20 \mathrm{Vdc} \\ & \hline \end{aligned}$ | Regline | - | - | $\begin{aligned} & 200 \\ & 150 \end{aligned}$ | - | - | $\begin{aligned} & 150 \\ & 100 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA} \\ & 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \end{aligned}$ | Regload | - | - | $\begin{aligned} & 60 \\ & 30 \end{aligned}$ | - | - | $\begin{aligned} & 60 \\ & 30 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-20 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{0} \leq 40 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{I}}=-10 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & -4.5 \\ & -4.5 \end{aligned}$ |  | $\begin{aligned} & -5.5 \\ & -5.5 \end{aligned}$ | $\begin{aligned} & -4.75 \\ & -4.75 \end{aligned}$ | - | $\begin{aligned} & -5.25 \\ & -5.25 \end{aligned}$ | Vdc |
| Input Bias Current $\begin{aligned} & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | $I_{\text {IB }}$ | - |  | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ | - | - | $\begin{aligned} & 6.0 \\ & 5.5 \end{aligned}$ | mA |
| $\begin{gathered} \text { Input Bias Current Change } \\ -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-20 \mathrm{Vdc} \\ 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \\ \hline \end{gathered}$ | $I_{\text {IB }}$ | - |  | $\begin{aligned} & 1.5 \\ & 0.2 \end{aligned}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 40 | - | - | 40 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\left(-8.0 \geq \mathrm{V}_{\mathrm{l}} \geq-18 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | RR | 40 | 49 | - | 41 | 49 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{0}=40 \mathrm{~mA}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\|$ | - | 1.7 | - | - | 1.7 | - | Vdc |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}+125^{\circ} \mathrm{C}\right.$ (for MC79LXXAC), $0^{\circ} \mathrm{C}<\mathrm{T}_{J}<+125^{\circ} \mathrm{C}$ (for MC79LXXAB)).

| Characteristics | Symbol | MC79L12C, AB |  |  | MC79L12AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | -11.1 | -12 | -12.9 | -11.5 | -12 | -12.5 | Vdc |
| $\begin{aligned} & \text { Input Regulation } \\ & \text { ( } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { ) } \\ & -14.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-27 \mathrm{Vdc} \\ & -16 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-27 \mathrm{Vdc} \end{aligned}$ | Regline | - |  | $\begin{aligned} & 250 \\ & 200 \end{aligned}$ | - | - | $\begin{aligned} & 250 \\ & 200 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I} \leq 100 \mathrm{~mA} \\ & 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \end{aligned}$ | Regload | - | - | $\begin{gathered} 100 \\ 50 \end{gathered}$ | - | - | $\begin{aligned} & 100 \\ & 50 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & -14.5 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-27 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{I}}=-19 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & -10.8 \\ & -10.8 \end{aligned}$ | - | $\begin{aligned} & -13.2 \\ & -13.2 \end{aligned}$ | $\begin{array}{r} -11.4 \\ -11.4 \end{array}$ |  | $\begin{aligned} & -12.6 \\ & -12.6 \end{aligned}$ | Vdc |
| Input Bias Current $\begin{aligned} & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | 1 IB | - |  | $\begin{aligned} & 6.5 \\ & 6.0 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 6.5 \\ & 6.0 \\ & \hline \end{aligned}$ | mA |
| $\begin{gathered} \text { Input Bias Current Change } \\ -16 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-27 \mathrm{Vdc} \\ 1.0 \mathrm{~mA} \leq \mathrm{I}_{0} \leq 40 \mathrm{~mA} \end{gathered}$ | 1 IB | - |  | $\begin{aligned} & 1.5 \\ & 0.2 \end{aligned}$ |  |  | $\begin{aligned} & 1.5 \\ & 0.2 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 80 | - | - | 80 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\left(-15 \leq \mathrm{V}_{I} \leq-25 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | RR | 36 | 42 | - | 37 | 42 | - | dB |
| Dropout Voltage ( $\mathrm{l}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\left\|\mathrm{V}_{1}-\mathrm{V}_{0}\right\|$ | - | 1.7 | - | - | 1.7 | - | Vdc |

## MC79L00, MC79L00A Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}+125^{\circ} \mathrm{C}\right.$ (for MC79LXXAB), $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$ (for MC79LXXAC)).

| Characteristics | Symbol | MC79L15C |  |  | MC79L15AC, AB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | -13.8 | -15 | -16.2 | -14.4 | -15 | -15.6 | Vdc |
| $\begin{aligned} & \text { Input Regulation } \\ & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right. \text { ) } \\ & -17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ & -20 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \end{aligned}$ | Regline | - |  | $\begin{aligned} & 300 \\ & 250 \end{aligned}$ | - | - | $\begin{aligned} & 300 \\ & 250 \end{aligned}$ | mV |
| Load Regulation $\begin{aligned} & \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA} \\ & 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \end{aligned}$ | Regload | - |  | $\begin{gathered} 150 \\ 75 \end{gathered}$ | - |  | $\begin{gathered} 150 \\ 75 \end{gathered}$ | mV |
| Output Voltage $-17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-\mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA}$ $\mathrm{V}_{\mathrm{I}}=-23 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & -13.5 \\ & -13.5 \end{aligned}$ |  | $\begin{aligned} & -16.5 \\ & -16.5 \end{aligned}$ | $\begin{aligned} & -14.25 \\ & -14.25 \end{aligned}$ |  | $\begin{aligned} & -15.75 \\ & -15.75 \end{aligned}$ | Vdc |
| Input Bias Current $\begin{aligned} & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | $I_{\text {IB }}$ | - |  | $\begin{aligned} & 6.5 \\ & 6.0 \end{aligned}$ | - | - | $\begin{aligned} & 6.5 \\ & 6.0 \end{aligned}$ | mA |
| Input Bias Current Change $-20 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}$ $1.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 40 \mathrm{~mA}$ | $\Delta_{1 B}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.2 \end{aligned}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{N}}$ | - | 90 | - | - | 90 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\left(-18.5 \leq \mathrm{V}_{\mathrm{I}} \leq-28.5 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}\right)$ | RR | 33 | 39 | - | 34 | 39 | - | dB |
| Dropout Voltage $\mathrm{I}=40 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ | $\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\|$ | - | 1.7 | - | - | 1.7 | - | Vdc |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-27 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C}<\mathrm{T}_{J}>+125^{\circ} \mathrm{C}\right.$, unless otherwise noted).

| Characteristics | Symbol | MC79L18C |  |  | MC79L18AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | -16.6 | -18 | -19.4 | -17.3 | -18 | -18.7 | Vdc |
| $\begin{aligned} & \text { Input Regulation } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & -20.7 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc} \\ & -21.4 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc} \\ & -22 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc} \\ & -21 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc} \end{aligned}$ | Regline |  | $\begin{aligned} & - \\ & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 325 \\ & 275 \end{aligned}$ | - | - | $\begin{gathered} 325 \\ - \\ - \\ 275 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA} \\ & 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \end{aligned}$ | Regload | - |  | $\begin{gathered} 170 \\ 85 \end{gathered}$ | - | - | $\begin{gathered} 170 \\ 85 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & -20.7 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \\ & -21.4 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{I}}=-27 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{gathered} -\overline{6} .2 \\ -16.2 \end{gathered}$ | - | $\begin{gathered} - \\ -19.8 \\ -19.8 \end{gathered}$ | $\begin{gathered} -17.1 \\ - \\ -17.1 \end{gathered}$ | - | $\begin{gathered} -18.9 \\ - \\ -18.9 \end{gathered}$ | Vdc |
| Input Bias Current $\begin{aligned} & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{\mathrm{J}}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | $I_{\text {IB }}$ | - |  | $\begin{aligned} & 6.5 \\ & 6.0 \\ & \hline \end{aligned}$ | - |  | $\begin{aligned} & 6.5 \\ & 6.0 \end{aligned}$ | mA |
| $\begin{gathered} \text { Input Bias Current Change } \\ -21 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc} \\ -27 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc} \\ 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \\ \hline \end{gathered}$ | $I_{\text {IB }}$ |  | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{gathered} - \\ 1.5 \\ 0.2 \end{gathered}$ | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 1.5 \\ & - \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 150 | - | - | 150 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\left(-23 \leq \mathrm{V}_{1} \leq-33 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | RR | 32 | 46 | - | 33 | 48 | - | dB |
| Dropout Voltage $\mathrm{I}=40 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ | $\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\|$ | - | 1.7 | - | - | 1.7 | - | Vdc |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-33 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{C}_{\mathrm{I}}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}}=0.1 \mu \mathrm{~F}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted).

| Characteristics | Symbol | MC79L24C |  |  | MC79L24AC |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Output Voltage ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | -22.1 | -24 | -25.9 | -23 | -24 | -25 | Vdc |
| $\begin{aligned} & \text { Input Regulation } \\ & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right. \text { ) } \\ & -27 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc} \\ & -27.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc} \\ & -28 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & -\overline{4} \\ & 350 \\ & 300 \end{aligned}$ | - | - | $\begin{gathered} 350 \\ - \\ 300 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation } \\ & \mathrm{T}_{J}=+25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA} \\ & 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \end{aligned}$ | Regload |  |  | $\begin{aligned} & 200 \\ & 100 \end{aligned}$ |  | - | $\begin{aligned} & 200 \\ & 100 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Voltage } \\ & -27 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \\ & -28 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{I}}=-33 \mathrm{Vdc}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 70 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{gathered} - \\ -21.4 \\ -21.4 \end{gathered}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{gathered} - \\ -26.4 \\ -26.4 \end{gathered}$ | $\begin{gathered} -22.8 \\ - \\ -22.8 \end{gathered}$ | - | $\begin{gathered} -25.2 \\ - \\ -25.2 \end{gathered}$ | Vdc |
| Input Bias Current $\begin{aligned} & \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{J}=+125^{\circ} \mathrm{C}\right) \end{aligned}$ | $I_{\text {IB }}$ | - |  | $\begin{aligned} & 6.5 \\ & 6.0 \end{aligned}$ |  | - | $\begin{aligned} & 6.5 \\ & 6.0 \\ & \hline \end{aligned}$ | mA |
| $\begin{gathered} \text { Input Bias Current Change } \\ -28 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc} \\ 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 40 \mathrm{~mA} \end{gathered}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 1.5 \\ & 0.2 \end{aligned}$ |  | - | $\begin{aligned} & 1.5 \\ & 0.1 \end{aligned}$ | mA |
| Output Noise Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 200 | - | - | 200 | - | $\mu \mathrm{V}$ |
| Ripple Rejection $\left(-29 \leq \mathrm{V}_{1} \leq-35 \mathrm{Vdc}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | RR | 30 | 43 | - | 31 | 47 | - | dB |
| Dropout Voltage $\mathrm{I}=40 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ | $\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\|$ | - | 1.7 | - | - | 1.7 | - | Vdc |

## APPLICATIONS INFORMATION

## Design Considerations

The MC79L00, A Series of fixed voltage regulators are designed with Thermal Overload Protections that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire length, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good


Figure 1. Positive and Negative Regulator
high-frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.


A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the ripple voltage.
${ }^{*} \mathrm{C}_{\text {I }}$ is required if regulator is located an appreciable distance from the power supply filter
${ }^{* *} \mathrm{C}_{0}$ improves stability and transient response.
Figure 2. Standard Application

## MC79L00, MC79L00A Series

TYPICAL CHARACTERISTICS
( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)


Figure 3. Dropout Characteristics


Figure 5. Input Bias Current versus Ambient Temperature


Figure 7. Maximum Average Power Dissipation versus Ambient Temperature (TO-92)


Figure 4. Dropout Voltage versus Junction Temperature


Figure 6. Input Bias Current versus Input Voltage


Figure 8. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## 500 mA Negative Voltage Regulators

The MC79M00 series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 series devices.

Available in fixed output voltage options of $-5.0,-8.0,-12$ and -15 V , these regulators employ current limiting, thermal shutdown, and safe-area compensation - making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 0.5 A .

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Also Available in Surface Mount DPAK (DT) Package

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

| MC79M05 MC79M08 | $\begin{aligned} & -5.0 \mathrm{~V} \\ & -8.0 \mathrm{~V} \end{aligned}$ | MC79M12 <br> MC79M15 | $\begin{aligned} & -12 \mathrm{~V} \\ & -15 \mathrm{~V} \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| ORDERING INFORMATION |  |  |  |
| Device | Output <br> Voltage Tolerance | Operating Temperature Range | Package |
| MC79MXXBDT, BDT-1 | 4.0\% | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK |
| MC79MXXBT |  |  | Plastic Power |
| MC79MXXCDT, CDT-1 |  | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | DPAK |
| MC79MXXCT |  |  | Plastic Power |

XX indicates nominal voltage.
Representative Schematic Diagram


## THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

T SUFFIX PLASTIC PACKAGE

CASE 221A

Heatsink surface connected to Pin 2.

Pin 1. Ground

2. Input
3. Output


DT SUFFIX
PLASTIC PACKAGE
CASE 369A (DPAK)


DT-1 SUFFIX PLASTIC PACKAGE CASE 369 (DPAK)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

## STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point of the input ripple voltage.
$X X$, These two digits of the type number indicate nominal voltage.
${ }^{*} \mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter.
** $\mathrm{C}_{\mathrm{O}}$ improve stability and transient response.

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $V_{1}$ | -35 | Vdc |
| Power Dissipation <br> Case 221A $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 369 and 369A (DPAK) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $\begin{aligned} & \mathrm{P}_{\mathrm{D}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \\ & \mathrm{P}_{\mathrm{D}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \end{aligned}$ | Internally Limited 65 5.0 Internally Limited 92 6.0 | $\begin{gathered} W \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ W \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Storage Junction Temperature | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature | TJ | 150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta J A}$ |  | 65 |
| Thermal Resistance, Junction-to-Case | $R_{\theta J C}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

MC79M05B, C
ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{I}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ [Note 2], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{0}$ | -4.8 | -5.0 | -5.2 | Vdc |
| Line Regulation, $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ (Note 1) $\begin{aligned} & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-18 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 7.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 50 \\ & 30 \end{aligned}$ | mV |
| Load Regulation, $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ (Note 1) $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 500 \mathrm{~mA}$ | Regload | - | 30 | 100 | mV |
| Output Voltage $-7.0 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-25 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{O}}$ | -4.75 | - | $-5.25$ | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{I}_{\mathrm{B}}$ | - | 4.3 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=-10 \mathrm{~V} \end{aligned}$ | $\Delta \mathrm{l}_{\mathrm{IB}}$ | - | - | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | mA |
| Output Noise Voltage, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 40 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{f}=120 \mathrm{~Hz}$ ) | RR | 54 | 66 | - | dB |
| Dropout Voltage $\mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.1 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | 0.2 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES: 1. Load and line regulation are specified at constant temperature. Change in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used
2. $\mathrm{B}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$
$\mathrm{C}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$

MC79M08B, C
ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{I}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ [Note 2], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -7.7 | -8.0 | -8.3 | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note 1) } \\ & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-18 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 5.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 80 \\ & 50 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=25^{\circ} \mathrm{C} \text { (Note 1) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA} \end{aligned}$ | Regload | - | 30 | 100 | mV |
| Output Voltage $-7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{O}}$ | -7.6 | -8.0 | -8.4 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {IB }}$ | - | - | 8.0 | mA |
| Input Bias Current Change $-8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}$ $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=-10 \mathrm{~V}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | mA |
| Output Noise Voltage, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 60 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{f}=120 \mathrm{~Hz}$ ) | RR | 54 | 63 | - | dB |
| Dropout Voltage $\mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.1 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | 0.4 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

MC79M12B, C
ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{I}}=-19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ [Note 2], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\left.\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | -11.5 | -12 | -12.5 | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note 1) } \\ & -14.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ & -15 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 5.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 80 \\ & 50 \end{aligned}$ | mV |
| Load Regulation, $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ (Note 1) $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 500 \mathrm{~mA}$ | Regload | - | 30 | 240 | mV |
| Output Voltage <br> $-14.5 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-30 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{O}}$ | -11.4 | - | -12.6 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $I_{\text {IB }}$ | - | 4.4 | 8.0 | mA |
| Input Bias Current Change $\begin{aligned} & -14.5 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=-19 \mathrm{~V} \end{aligned}$ | $\Delta \mathrm{l}_{\mathrm{IB}}$ | - | - | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | mA |
| Output Noise Voltage, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 75 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{f}=120 \mathrm{~Hz}$ ) | RR | 54 | 60 | - | dB |
| Dropout Voltage $\mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.1 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -0.8 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES: 1. Load and line regulation are specified at constant temperature. Change in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used
2. $B=T_{\text {low }}$ to $T_{\text {high }},-40^{\circ} \mathrm{C}<T_{J}<125^{\circ} \mathrm{C}$
$\mathrm{C}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$

MC79M15B, C
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}, \mathrm{~T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 2], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -14.4 | -15 | -15.6 | Vdc |
| $\begin{aligned} & \text { Line Regulation, } \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \text { (Note 1) } \\ & -17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ & -18 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-28 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 5.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 80 \\ & 50 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=25^{\circ} \mathrm{C} \text { (Note 1) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 500 \mathrm{~mA} \end{aligned}$ | Regload | - | 30 | 240 | mV |
| Output Voltage $-17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 350 \mathrm{~mA}$ | $\mathrm{V}_{\mathrm{O}}$ | -14.25 | - | -15.75 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{IIB}^{\text {a }}$ | - | 4.4 | 8.0 | mA |
| Input Bias Current Change <br> $-17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=350 \mathrm{~mA}$ <br> $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 350 \mathrm{~mA}, \mathrm{~V}_{\mathrm{I}}=-23 \mathrm{~V}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | mA |
| Output Noise Voltage, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 90 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{f}=120 \mathrm{~Hz}$ ) | RR | 54 | 60 | - | dB |
| Dropout Voltage $\mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 1.1 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

NOTES: 1. Load and line regulation are specified at constant temperature. Change in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
2. $B=T_{\text {low }}$ to $T_{\text {high }},-40^{\circ} \mathrm{C}<T_{J}<125^{\circ} \mathrm{C}$
$\mathrm{C}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$


Figure 1. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC7900 Series

### 1.0 A Negative Voltage Regulators

The MC7900 series of fixed output negative voltage regulators are intended as complements to the popular MC7800 series devices. These negative regulators are available in the same seven-voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 series.

Available in fixed output voltage options from -5.0 V to -24 V , these regulators employ current limiting, thermal shutdown, and safe-area compensation - making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 1.0 A .

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Available in 2\% Voltage Tolerance (See Ordering Information)

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com

TO-220
T SUFFIX
CASE 221A

Heatsink surface connected to Pin 2.


Pin 1. Ground
2. Input
3. Output
$D^{2}$ PAK D2T SUFFIX CASE 936


Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

## STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above more negative even during the high point of the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.

* $\mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter.
${ }^{* *} \mathrm{C}_{\mathrm{O}}$ improve stability and transient response.


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 204 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 205 of this data sheet.

MAXIMUM RATINGS $\left(T_{A}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { Input Voltage }\left(-5.0 \mathrm{~V} \geq \mathrm{V}_{\mathrm{O}} \geq-18 \mathrm{~V}\right) \\ (24 \mathrm{~V}) \end{gathered}$ | $V_{1}$ | $\begin{aligned} & -35 \\ & -40 \end{aligned}$ | Vdc |
| Power Dissipation <br> Case 221A $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 936 ( $D^{2}$ PAK) $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $\begin{aligned} & \mathrm{P}_{\mathrm{D}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \\ & \\ & \mathrm{P}_{\mathrm{D}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \end{aligned}$ | Internally Limited 65 <br> 5.0 <br> Internally Limited <br> 70 <br> 5.0 | W <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> W <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Junction Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |

THERMAL CHARACTERISTICS

| Characteristics | Symbol | Max | Unit |
| :--- | :---: | :---: | :---: |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta J A}$ | 65 |  |
| Thermal Resistance, Junction-to-Case | $R_{\theta J C}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |

## MC7905C

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -4.8 | -5.0 | -5.2 | Vdc |
| $\begin{aligned} & \text { Line Regulation (Note 1) } \\ & \left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}\right) \\ & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-12 \mathrm{Vdc} \\ & \left(\mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}\right) \\ & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-12 \mathrm{Vdc} \end{aligned}$ | Regline | - | $\begin{aligned} & 7.0 \\ & 2.0 \\ & \\ & 35 \\ & 8.0 \end{aligned}$ | $\begin{gathered} 50 \\ 25 \\ \\ 100 \\ 50 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { (Note 1) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload | - | $\begin{aligned} & 11 \\ & 4.0 \end{aligned}$ | $\begin{gathered} 100 \\ 50 \end{gathered}$ | mV |
| Output Voltage $-7.0 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-20 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -4.75 | - | -5.25 | Vdc |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | IB | - | 4.3 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{0} \leq 1.5 \mathrm{~A} \end{aligned}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 1.3 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 40 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{l}_{\mathrm{O}}=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 70 | - | dB |
| Dropout Voltage $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

1. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7905AC
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -4.9 | -5.0 | -5.1 | Vdc |
| Line Regulation (Note 2) $\begin{aligned} & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-12 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \\ & -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-12 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \\ & -7.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & -7.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-20 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \end{aligned}$ | Regline | - | $\begin{aligned} & 2.0 \\ & 7.0 \\ & 7.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 25 \\ & 50 \\ & 50 \\ & 50 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | Regload | - | $\begin{aligned} & 11 \\ & 4.0 \\ & 9.0 \end{aligned}$ | $\begin{gathered} 100 \\ 50 \\ 100 \end{gathered}$ | mV |
| Output Voltage $-7.5 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-20 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -4.80 | - | -5.20 | Vdc |
| Input Bias Current | $I_{\text {IB }}$ | - | 4.4 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -7.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \end{aligned}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 1.3 \\ & 0.5 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 40 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{I}_{0}=\mathrm{mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 70 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{0}=1.0 \mathrm{~A} . \mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

MC7905.2C
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -5.0 | -5.2 | -5.4 | Vdc |
| Line Regulation (Note 2) $\begin{array}{r} \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}\right) \\ -7.2 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-12 \mathrm{Vdc} \\ \left(\mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}\right) \\ -7.2 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ -8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-12 \mathrm{Vdc} \end{array}$ | Regline | - - - - | $\begin{aligned} & 8.0 \\ & 2.2 \\ & \\ & 37 \\ & 8.5 \end{aligned}$ | $\begin{gathered} 52 \\ 27 \\ \\ 105 \\ 52 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } T_{J}=+25^{\circ} \mathrm{C} \text { (Note 2) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload | - | $\begin{aligned} & 12 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 105 \\ & 52 \end{aligned}$ | mV |
| Output Voltage $-7.2 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-20 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -4.95 | - | -5.45 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | IB | - | 4.3 | 8.0 | mA |
| Input Bias Current Change $-7.2 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}$ $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.5 \mathrm{~A}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 1.3 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 42 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{l}=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 68 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

2. Load and line regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7906C
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-11 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -5.75 | -6.0 | -6.25 | Vdc |
| Line Regulation (Note 3) $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{0}=100 \mathrm{~mA}\right)$ $-8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}$ $-9.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-13 \mathrm{Vdc}$ $\left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}\right)$ $-8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}$ $-9.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-13 \mathrm{Vdc}$ | $\mathrm{Reg}_{\text {line }}$ |  | $\begin{aligned} & 9.0 \\ & 3.0 \\ & 43 \\ & 10 \end{aligned}$ | $\begin{gathered} 60 \\ 30 \\ \\ 120 \\ 60 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { (Note 3) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload | - | $\begin{aligned} & 13 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 120 \\ & 60 \end{aligned}$ | mV |
| Output Voltage $-8.0 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-21 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -5.7 | - | -6.3 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | 1 IB | - | 4.3 | 8.0 | mA |
| Input Bias Current Change $-8.0 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}$ $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.5 \mathrm{~A}$ | $\left.\Delta\right\|_{1 B}$ | - |  | $\begin{aligned} & 1.3 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 45 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{l}_{\mathrm{O}}=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 65 | - | dB |
| Dropout Voltage ( $\left.\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

## MC7908C

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -7.7 | -8.0 | -8.3 | Vdc |
| Line Regulation (Note 3) $\left(T_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}\right)$ $-10.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}$ $-11 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-17 \mathrm{Vdc}$ $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}\right)$ $-10.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc}$ $-11 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-17 \mathrm{Vdc}$ | Regline | - - - - | $\begin{aligned} & 12 \\ & 5.0 \\ & 50 \\ & 22 \end{aligned}$ | $\begin{gathered} 80 \\ 40 \\ \\ 160 \\ 80 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { (Note 3) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload |  | $\begin{aligned} & 26 \\ & 9.0 \end{aligned}$ | $\begin{gathered} 160 \\ 80 \end{gathered}$ | mV |
| Output Voltage $-10.5 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-23 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -7.6 | - | -8.4 | Vdc |
| Input Bias Current ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | IB | - | 4.3 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -10.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-25 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 52 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( l O $=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 62 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

3. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7912C
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -11.5 | -12 | -12.5 | Vdc |
| Line Regulation (Note 4) $\begin{gathered} \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}\right) \\ -14.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ -16 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-22 \mathrm{Vdc} \\ \left(\mathrm{~T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}\right) \\ -14.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ -16 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-22 \mathrm{Vdc} \end{gathered}$ | Regline | - - - - | $\begin{aligned} & 13 \\ & 6.0 \\ & \\ & 55 \\ & 24 \end{aligned}$ | $\begin{gathered} 120 \\ 60 \\ 240 \\ 120 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { (Note 4) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload |  | $\begin{aligned} & 46 \\ & 17 \end{aligned}$ | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ | mV |
| Output Voltage $-14.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-27 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -11.4 | - | -12.6 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $I_{\text {IB }}$ | - | 4.4 | 8.0 | mA |
| Input Bias Current Change $-14.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}$ $5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 1.5 \mathrm{~A}$ | $\Delta l_{\text {IB }}$ |  |  | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 75 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{l}_{\mathrm{O}}=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 61 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

MC7912AC
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-19 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -11.75 | -12 | -12.25 | Vdc |
| $\begin{aligned} & \text { Line Regulation (Note 4) } \\ & -16 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-22 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} \\ & -16 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-22 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A} \\ & -14.8 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & -14.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-27 \mathrm{Vdc} ; \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} \end{aligned}$ | Regline | - | $\begin{aligned} & 6.0 \\ & 24 \\ & 24 \\ & 13 \end{aligned}$ | $\begin{gathered} 60 \\ 120 \\ 120 \\ 120 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation (Note 4) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | Regload | - | $\begin{aligned} & 46 \\ & 17 \\ & 35 \end{aligned}$ | $\begin{gathered} 150 \\ 75 \\ 150 \end{gathered}$ | mV |
| Output Voltage $-14.8 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{l}} \geq-27 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -11.5 | - | -12.5 | Vdc |
| Input Bias Current | $I_{\text {IB }}$ | - | 4.4 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -15 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \end{aligned}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.5 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 75 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( l O $=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 61 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

4. Load and line regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7915C
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -14.4 | -15 | -15.6 | Vdc |
| Line Regulation (Note 5) $\begin{gathered} \left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{0}=100 \mathrm{~mA}\right) \\ -17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ -20 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-26 \mathrm{Vdc} \\ \left(\mathrm{~T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}\right) \\ -17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ -20 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-26 \mathrm{Vdc} \end{gathered}$ | $\mathrm{Reg}_{\text {line }}$ |  | $\begin{aligned} & 14 \\ & 6.0 \\ & 57 \\ & 27 \end{aligned}$ | $\begin{gathered} 150 \\ 75 \\ \\ 300 \\ 150 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { (Note 5) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload | - | $\begin{aligned} & 68 \\ & 25 \end{aligned}$ | $\begin{aligned} & 300 \\ & 150 \end{aligned}$ | mV |
| Output Voltage $-17.5 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-30 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -14.25 | - | -15.75 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | 1 IB | - | 4.4 | 8.0 | mA |
| Input Bias Current Change <br> $-17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}$ <br> $5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}$ | $\left.\Delta\right\|_{1 B}$ | - |  | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 90 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{l}_{\mathrm{O}}=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 60 | - | dB |
| Dropout Voltage ( $\left.\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~A}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

MC7915AC
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-23 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -14.7 | -15 | -15.3 | Vdc |
| $\begin{aligned} & \text { Line Regulation (Note 5) } \\ & -20 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-26 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} \\ & -20 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-26 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \\ & -17.9 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA} \\ & -17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} \end{aligned}$ | Regline | - | $\begin{aligned} & 27 \\ & 57 \\ & 57 \\ & 57 \end{aligned}$ | $\begin{gathered} 75 \\ 150 \\ 150 \\ 150 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation (Note 5) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \end{aligned}$ | Regload | - | $\begin{aligned} & 68 \\ & 25 \\ & 40 \end{aligned}$ | $\begin{gathered} 150 \\ 75 \\ 150 \end{gathered}$ | mV |
| Output Voltage $-17.9 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{l}} \geq-30 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -14.4 | - | -15.6 | Vdc |
| Input Bias Current | $I_{\text {IB }}$ | - | 4.4 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -17.5 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} \end{aligned}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 0.8 \\ & 0.5 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 90 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( l O $=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 60 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

5. Load and line regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7918C
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-27 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -17.3 | -18 | -18.7 | Vdc |
| Line Regulation (Note 6) $\left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}\right)$ $-21 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc}$ $-24 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}$ $\left(\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{0}=500 \mathrm{~mA}\right)$ $-21 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc}$ $-24 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-30 \mathrm{Vdc}$ | $\mathrm{Reg}_{\text {line }}$ |  | $\begin{aligned} & 25 \\ & 10 \\ & 90 \\ & 50 \end{aligned}$ | $\begin{gathered} 180 \\ 90 \\ \\ 360 \\ 180 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { (Note 6) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload | - | $\begin{gathered} 110 \\ 55 \end{gathered}$ | $\begin{aligned} & 360 \\ & 180 \end{aligned}$ | mV |
| Output Voltage $-21 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -17.1 | - | -18.9 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | 1 IB | - | 4.5 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -21 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-33 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | $\left.\Delta\right\|_{1 B}$ | - |  | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 110 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( $\mathrm{l}_{\mathrm{O}}=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 59 | - | dB |
| Dropout Voltage ( $\left.\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

## MC7924C

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}=-33 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{O}}$ | -23 | -24 | -25 | Vdc |
| Line Regulation (Note 6) $\left(\mathrm{T}_{J}=+25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}\right)$ $-27 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc}$ $-30 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-36 \mathrm{Vdc}$ ( $\left.\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}, \mathrm{I}_{0}=500 \mathrm{~mA}\right)$ $-27 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc}$ $-30 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-36 \mathrm{Vdc}$ | Regline | - - - - | $\begin{gathered} 31 \\ 14 \\ \\ 118 \\ 70 \end{gathered}$ | $\begin{aligned} & 240 \\ & 120 \\ & \\ & 470 \\ & 240 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Load Regulation, } \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \text { (Note 6) } \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \\ & 250 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 750 \mathrm{~mA} \end{aligned}$ | Regload | - | $\begin{aligned} & 150 \\ & 85 \end{aligned}$ | $\begin{aligned} & 480 \\ & 240 \end{aligned}$ | mV |
| Output Voltage $-27 \mathrm{Vdc} \geq \mathrm{V}_{\mathrm{I}} \geq-38 \mathrm{Vdc}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.0 \mathrm{~A}, \mathrm{P} \leq 15 \mathrm{~W}$ | $\mathrm{V}_{\mathrm{O}}$ | -22.8 | - | -25.2 | Vdc |
| Input Bias Current ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | IB | - | 4.6 | 8.0 | mA |
| $\begin{aligned} & \text { Input Bias Current Change } \\ & -27 \mathrm{Vdc} \geq \mathrm{V}_{1} \geq-38 \mathrm{Vdc} \\ & 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 1.5 \mathrm{~A} \end{aligned}$ | $\Delta l_{\text {IB }}$ | - | - | $\begin{aligned} & 1.0 \\ & 0.5 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 100 \mathrm{kHz}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 170 | - | $\mu \mathrm{V}$ |
| Ripple Rejection ( l O $=20 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ ) | RR | - | 56 | - | dB |
| Dropout Voltage ( $\mathrm{I}_{0}=1.0 \mathrm{~A}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | 2.0 | - | Vdc |
| Average Temperature Coefficient of Output Voltage $\mathrm{I}_{\mathrm{O}}=5.0 \mathrm{~mA}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{O}} / \Delta \mathrm{T}$ | - | -1.0 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |

6. Load and line regulation are specified at constant junction temperature. Changes in $V_{O}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.


Figure 2. Worst Case Power Dissipation as a Function of Ambient Temperature


Figure 4. Ripple Rejection as a Function of Frequency


Figure 6. Output Voltage as a Function of Junction Temperature


Figure 3. Peak Output Current as a Function of Input-Output Differential Voltage


Figure 5. Ripple Rejection as a Function of Output Voltage


Figure 7. Quiescent Current as a Function of Temperature

## APPLICATIONS INFORMATION

## Design Considerations

The MC7900 Series of fixed voltage regulators are designed with Thermal overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The capacitor chosen should have an equivalent series resistance of less than $0.7 \Omega$. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be

*Mounted on heatsink.
When a boost transistor is used, short circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to $0.6 \mathrm{~V} / \mathrm{R}_{\mathrm{Sc}}$. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heatsink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.
used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.


The MC7905, -5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows.

$$
\mathrm{I}_{\mathrm{O}}=\frac{5.0 \mathrm{~V}}{\mathrm{R}}+\mathrm{I}_{\mathrm{B}}
$$

The quiescent current for this regulator is typically 4.3 mA . The 5.0 V regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

Figure 8. Current Regulator


The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA .

Figure 10. Operational Amplifier Supply
( $\pm 15$ @ 1.0 A)

Figure 9. Current Boost Regulator
(-5.0 V @ 4.0 A, with 5.0 A Current Limiting)


Figure 11. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## DEFINITIONS

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current - That part of the input current that is not delivered to the load.

Output Noise Voltage - The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability - Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

ORDERING INFORMATION

| Device | Nominal Output Voltage | Output Voltage Tolerance | Package | Operating Temperature Range | Shipping |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MC7905ACD2T | 5.0 V | 2\% | D²PAK | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |
| MC7905ACD2TR4 |  | 2\% | D2PAK |  | 800 Tape \& Reel |
| MC7905CD2T |  | 4\% | D2PAK |  | 50 Units/Rail |
| MC7905CD2TR4 |  | 4\% | D2PAK |  | 800 Tape \& Reel |
| MC7905ACT |  | 2\% | TO-220 |  | 50 Units/Rail |
| MC7905CT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7905BD2T |  | 4\% | D2PAK | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |
| MC7905BD2TR4 |  | 4\% | D²PAK |  | 800 Tape \& Reel |
| MC7905BT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7905.2CT | 5.2 V | 4\% | TO-220 | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |
| MC7906CD2T | 6.0 V | 4\% | D²PAK |  | 50 Units/Rail |
| MC7906CT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7908CD2T | 8.0 V | 4\% | D2PAK |  | 50 Units/Rail |
| MC7908CD2TR4 |  | 4\% | D2PAK |  | 800 Tape \& Reel |
| MC7908ACT |  | 2\% | TO-220 |  | 50 Units/Rail |
| MC7908CT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7912ACD2T | 12 V | 2\% | D2PAK |  | 50 Units/Rail |
| MC7912ACD2TR4 |  | 2\% | D2PAK |  | 800 Tape \& Reel |
| MC7912CD2T |  | 4\% | D2PAK |  | 50 Units/Rail |
| MC7912CD2TR4 |  | 4\% | D²PAK |  | 800 Tape \& Reel |
| MC7912ACT |  | 2\% | TO-220 |  | 50 Units/Rail |
| MC7912CT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7912BD2T |  | 4\% | D2PAK | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |
| MC7912BD2TR4 |  | 4\% | D2PAK |  | 800 Tape \& Reel |
| MC7912BT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7915ACD2T | 15 V | 2\% | D2PAK | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |
| MC7915CD2T |  | 4\% | D2PAK |  | 50 Units/Rail |
| MC7915CD2TR4 |  | 4\% | D²PAK |  | 800 Tape \& Reel |
| MC7915ACT |  | 2\% | TO-220 |  | 50 Units/Rail |
| MC7915CT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7915BD2T |  | 4\% | $\mathrm{D}^{2} \mathrm{PAK}$ | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |
| MC7915BT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7918CT | 18 V | 4\% | TO-220 | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |
| MC7924CD2T | 24 V | 4\% | D2PAK |  | 50 Units/Rail |
| MC7924CT |  | 4\% | TO-220 |  | 50 Units/Rail |
| MC7924BT |  | 4\% | TO-220 | $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 50 Units/Rail |

## MC7900 Series

## MARKING DIAGRAMS

```
TO-220
T SUFFIX
CASE 221A
```



[^6]
## 100 mA Adjustable Output, Positive Voltage Regulator

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V . This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM317L serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages


## Simplified Application


${ }^{*} \mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter.
${ }^{* *} C_{0}$ is not needed for stability, however, it does improve transient response.

$$
V_{\text {out }}=1.25 \mathrm{~V}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2}
$$

Since $I_{\text {Adj }}$ is controlled to less than $100 \mu \mathrm{~A}$, the error associated with this term is negligible in most applications.

LOW CURRENT
THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA
*SOP-8 is an internally modified SO-8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 package.

| Device | Operating Temperature Range | Package |
| :---: | :---: | :---: |
| LM317LD | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 |
| LM317LZ |  | Plastic |
| LM317LBD | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SOP-8 |
| LM317LBZ |  | Plastic |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input-Output Voltage Differential | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | 40 | Vdc |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | W |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V} ; \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA} ; \mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 1]; $\mathrm{I}_{\max }$ and $\mathrm{P}_{\max }$ [Note 2]; unless otherwise noted.)

| Characteristics | Figure | Symbol | LM317L, LB |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Line Regulation (Note 3) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}$ | 1 | Regline | - | 0.01 | 0.04 | \%/V |
| $\begin{gathered} \text { Load Regulation (Note 3), } \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max }-\mathrm{LM} 317 \mathrm{~L} \\ \mathrm{~V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{gathered}$ | 2 | Regload | - | $\begin{aligned} & 5.0 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 25 \\ & 0.5 \end{aligned}$ | $\stackrel{m V}{\% V_{O}}$ |
| Adjustment Pin Current | 3 | $I_{\text {Adj }}$ | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjustment Pin Current Change $\begin{gathered} 2.5 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max } \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max }-\mathrm{LM} 317 \mathrm{~L} \end{gathered}$ | 1, 2 | $\Delta^{\text {Adj }}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Reference Voltage } \\ & 3.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max } \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max }-\mathrm{LM} 317 \mathrm{~L} \end{aligned}$ | 3 | $\mathrm{V}_{\text {ref }}$ | 1.20 | 1.25 | 1.30 | V |
| Line Regulation (Note 3) $3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}$ | 1 | Regline | - | 0.02 | 0.07 | \%/V |
| $\begin{aligned} & \text { Load Regulation (Note 3) } \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max }-\mathrm{LM} 317 \mathrm{~L} \\ & \mathrm{~V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{aligned}$ | 2 | Regload | - | $\begin{aligned} & 20 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 70 \\ & 1.5 \end{aligned}$ | $\stackrel{m V}{\% V_{O}}$ |
| Temperature Stability ( $\mathrm{T}_{\text {low }} \leq \mathrm{T}_{J} \leq \mathrm{T}_{\text {high }}$ ) | 3 | $\mathrm{T}_{\mathrm{S}}$ | - | 0.7 | - | \% $\mathrm{V}_{\mathrm{O}}$ |
| Minimum Load Current to Maintain Regulation ( $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}$ ) | 3 | $I_{\text {Lmin }}$ | - | 3.5 | 10 | mA |
| Maximum Output Current <br> $\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}} \leq 6.25 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\text {max }}, Z$ Package <br> $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{Z}$ Package | 3 | $I_{\text {max }}$ | 100 - | $\begin{gathered} 200 \\ 20 \end{gathered}$ | - | mA |
| $\begin{aligned} & \text { RMS Noise, \% of } \mathrm{V}_{\mathrm{O}} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} \end{aligned}$ |  | N | - | 0.003 | - | \% $\mathrm{V}_{\mathrm{O}}$ |
| $\begin{gathered} \text { Ripple Rejection (Note 4) } \\ \mathrm{V}_{\mathrm{O}}=1.2 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz} \\ \mathrm{C}_{\text {Adj }}=10 \mu \mathrm{~F}, \mathrm{~V}_{\mathrm{O}}=10.0 \mathrm{~V} \end{gathered}$ | 4 | RR | 60 | $\begin{aligned} & 80 \\ & 80 \end{aligned}$ | - | dB |
| Long Term Stability, $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {high }}$ (Note 5) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for Endpoint Measurements | 3 | S | - | 0.3 | 1.0 | \%/1.0 k Hrs. |
| Thermal Resistance, Junction-to-Case Z Package |  | $\mathrm{R}_{\text {өJC }}$ | - | 83 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Air Z Package |  | $\mathrm{R}_{\text {өJA }}$ | - | 160 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

NOTES: 1. $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ for LM317L $\quad-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ for LM317LB
2. $I_{\max }=100 \mathrm{~mA} \quad P_{\max }=625 \mathrm{~mW}$
3. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. $\mathrm{C}_{\text {Adj }}$, when used, is connected between the adjustment pin and ground.
5. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

## LM317L

## Representative Schematic Diagram



Figure 1. Line Regulation and $\Delta \mathbf{I}_{\text {Adj }}$ Line Test Circuit

## LM317L



Figure 2. Load Regulation and $\Delta \mathbf{I}_{\text {Adj }}$ /Load Test Circuit


Figure 3. Standard Test Circuit


Figure 4. Ripple Rejection Test Circuit


Figure 5. Load Regulation


Figure 7. Current Limit


Figure 9. Minimum Operating Current


Figure 6. Ripple Rejection


Figure 8. Dropout Voltage


Figure 10. Ripple Rejection versus Frequency


Figure 11. Temperature Stability


Figure 13. Line Regulation


Figure 12. Adjustment Pin Current


Figure 14. Output Noise


Figure 15. Line Transient Response


Figure 16. Load Transient Response

## APPLICATIONS INFORMATION

## Basic Circuit Operation

The LM317L is a 3-terminal floating regulator. In operation, the LM317L develops and maintains a nominal 1.25 V reference ( $\mathrm{V}_{\text {ref }}$ ) between its output and adjustment terminals. This reference voltage is converted to a programming current ( $\mathrm{I}_{\mathrm{PROG}}$ ) by $\mathrm{R}_{1}$ (see Figure 13), and this constant current flows through $\mathrm{R}_{2}$ to ground. The regulated output voltage is given by:

$$
V_{\text {out }}=V_{\text {ref }}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2}
$$

Since the current from the adjustment terminal ( $\mathrm{I}_{\mathrm{Adj}}$ ) represents an error term in the equation, the LM317L was designed to control $\mathrm{I}_{\text {Adj }}$ to less than $100 \mu \mathrm{~A}$ and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.


Figure 17. Basic Circuit Configuration

## Load Regulation

The LM317L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

## External Capacitors

A $0.1 \mu \mathrm{~F}$ disc or $1.0 \mu \mathrm{~F}$ tantalum input bypass capacitor $\left(\mathrm{C}_{\mathrm{in}}\right)$ is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ( $\mathrm{C}_{\mathrm{Adj}}$ ) prevents ripple from being amplified as the output voltage is increased. A $10 \mu \mathrm{~F}$ capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance $\left(\mathrm{C}_{\mathrm{O}}\right)$ in the form of a $1.0 \mu \mathrm{~F}$ tantalum or $25 \mu \mathrm{~F}$ aluminum electrolytic capacitor on the output swamps this effect and insures stability.

## Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM317L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ( $\mathrm{C}_{\mathrm{O}}>10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{Adj}}>5.0 \mu \mathrm{~F}$ ). Diode $\mathrm{D}_{1}$ prevents $\mathrm{C}_{\mathrm{O}}$ from discharging thru the IC during an input short circuit. Diode $\mathrm{D}_{2}$ protects against capacitor $\mathrm{C}_{\text {Adj }}$ discharging through the IC during an output short circuit. The combination of diodes $D_{1}$ and $D_{2}$ prevents $C_{\text {Adj }}$ from discharging through the IC during an input short circuit.


Figure 18. Voltage Regulator with Protection Diodes


Figure 19. Adjustable Current Limiter


Figure 21. Slow Turn-On Regulator

$D_{1}$ protects the device during an input short circuit.
Figure 20. 5 V Electronic Shutdown Regulator


Figure 22. Current Regulator

## LM317M

## 500 mA Adjustable Output, Positive Voltage Regulator

The LM317M is an adjustable three-terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V . This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317M serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking Many Fixed Voltages

* $=\mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter. ${ }^{* *}=C_{0}$ is not needed for stability, however, it does improve transient response.

$$
V_{\text {out }}=1.25 \mathrm{~V}\left(1+\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}\right)+\mathrm{I}_{\mathrm{Adj}} \mathrm{R}_{2}
$$

Since $\mathrm{I}_{\text {Adj }}$ is controlled to less than $100 \mu \mathrm{~A}$, the error associated with this term is negligible in most applications.

Figure 1. Simplified Application

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


DPAK DT SUFFIX CASE 369A


Heatsink Surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

| PIN ASSIGNMENT |  |
| :---: | :---: |
| 1 | Adjust |
| 2 | $\mathrm{~V}_{\text {out }}$ |
| 3 | $\mathrm{~V}_{\text {in }}$ |

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 223 of this data sheet

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input-Output Voltage Differential | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | 40 | Vdc |
| Power Dissipation (Package Limitation) (Note 1) Plastic Package, T Suffix, Case 221A $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> Plastic Package, DT Suffix, Case 369A $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> Plastic Package, ST Suffix, Case 318E $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \theta_{\mathrm{JA}} \\ \theta_{\mathrm{JC}} \\ \\ \mathrm{P}_{\mathrm{D}} \\ \theta_{\mathrm{JA}} \\ \theta_{\mathrm{JC}} \\ \mathrm{P}_{\mathrm{D}} \\ \theta_{\mathrm{JA}} \\ \theta_{\mathrm{JC}} \end{gathered}$ | Internally Limited 70 5.0 Internally Limited 92 5.0 Internally Limited 245 15 | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{l}}-\mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V} ; \mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 2], unless otherwise noted.)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation (Note 3) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}$ | 3 | Regline | - | 0.01 | 0.04 | \%/V |
| Load Regulation (Note 3) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 0.5 \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{aligned}$ | 4 | Regload |  | $\begin{aligned} & 5.0 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 25 \\ & 0.5 \end{aligned}$ | $\stackrel{\mathrm{mV}}{\%} \mathrm{~V}$ |
| Adjustment Pin Current | 5 | $1_{\text {Adj }}$ | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjustment Pin Current Change $2.5 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}, 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{L}} \leq 0.5 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }$ | 3,4 | $\Delta^{\text {Adj }}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| Reference Voltage $3.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}, 10 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{O}} \leq 0.5 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }:$ | 5 | $\mathrm{V}_{\text {ref }}$ | 1.200 | 1.250 | 1.300 | V |
| Line Regulation (Note 3) $3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}$ | 3 | Regline | - | 0.02 | 0.07 | \%/V |
| $\begin{gathered} \text { Load Regulation (Note 3) } \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 0.5 \mathrm{~A} \\ \mathrm{~V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{gathered}$ | 4 | Regload | - | $\begin{aligned} & 20 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 70 \\ & 1.5 \end{aligned}$ | $\stackrel{\mathrm{mV}}{\% \mathrm{~V}_{\mathrm{O}}}$ |
| Temperature Stability ( $\mathrm{l}_{\text {low }} \leq \mathrm{T}_{J} \leq \mathrm{T}_{\text {high }}$ ) | 5 | Ts | - | 0.7 | - | \% $\mathrm{V}_{\mathrm{O}}$ |
| Minimum Load Current to Maintain Regulation $\left(\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}\right)$ | 5 | $I_{\text {Lmin }}$ | - | 3.5 | 10 | mA |
| $\begin{aligned} & \text { Maximum Output Current } \\ & \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 15 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max } \\ & \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ | 5 | $I_{\text {max }}$ | $\begin{gathered} 0.5 \\ 0.15 \end{gathered}$ | $\begin{gathered} 0.9 \\ 0.25 \end{gathered}$ | - | A |
| $\begin{aligned} & \text { RMS Noise, } \% \text { of } V_{O} \\ & T_{A}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq f \leq 10 \mathrm{kHz} \end{aligned}$ | - | N | - | 0.003 | - | \% $\mathrm{V}_{\mathrm{O}}$ |
| ```Ripple Rejection, \(\mathrm{V}_{\mathrm{O}}=10 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz}\) (Note 4) Without \(\mathrm{C}_{\text {Adj }}\) \(\mathrm{C}_{\text {Adj }}=10 \mu \mathrm{~F}\)``` | 6 | RR | $66$ | $\begin{aligned} & 65 \\ & 80 \end{aligned}$ | - | dB |
| Long-Term Stability, $\mathrm{T}_{J}=\mathrm{T}_{\text {high }}$ (Note 5) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for Endpoint Measurements | 5 | S | - | 0.3 | 1.0 | $\begin{gathered} \% / 1.0 \mathrm{k} \\ \text { Hrs. } \end{gathered}$ |

1. Figure 25 provides thermal resistance versus pc board pad size.
2. $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ for LM317M $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ for LM317MB
3. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. $\mathrm{C}_{\text {Adj; }}$, when used, is connected between the adjustment pin and ground.
5. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.


Figure 2. Representative Schematic Diagram

## LM317M



Figure 3. Line Regulation and $\Delta \mathbf{I}_{\text {Adj }}$ /Line Test Circuit


Figure 4. Load Regulation and $\Delta \mathrm{I}_{\text {Adj }}$ Load Test Circuit

## LM317M



Figure 5. Standard Test Circuit


Figure 6. Ripple Rejection Test Circuit


Figure 7. Load Regulation


Figure 8. Ripple Rejection


Figure 9. Current Limit


Figure 11. Minimum Operating Current


Figure 10. Dropout Voltage


Figure 12. Ripple Rejection versus Frequency


Figure 13. Temperature Stability


Figure 15. Line Regulation


Figure 14. Adjustment Pin Current


Figure 16. Output Noise


Figure 17. Line Transient Response


Figure 18. Load Transient Response

## APPLICATIONS INFORMATION

## Basic Circuit Operation

The LM317M is a three-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 V reference ( $\mathrm{V}_{\mathrm{ref}}$ ) between its output and adjustment terminals. This reference voltage is converted to a programming current ( $\mathrm{I}_{\mathrm{PROG}}$ ) by $\mathrm{R}_{1}$ (see Figure 19), and this constant current flows through $\mathrm{R}_{2}$ to ground. The regulated output voltage is given by:

$$
V_{\text {out }}=V_{\text {ref }}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2}
$$

Since the current from the terminal ( $\mathrm{I}_{\text {Adj }}$ ) represents an error term in the equation, the LM317M was designed to control $\mathrm{I}_{\text {Adj }}$ to less than $100 \mu \mathrm{~A}$ and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.


Figure 19. Basic Circuit Configuration

## Load Regulation

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor $\left(\mathrm{R}_{1}\right)$ should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of $\mathrm{R}_{2}$ can be returned near the load ground to provide remote ground sensing and improve load regulation.

## External Capacitors

A $0.1 \mu \mathrm{~F}$ disc or $1.0 \mu \mathrm{~F}$ tantalum input bypass capacitor $\left(\mathrm{C}_{\mathrm{in}}\right)$ is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ( $\mathrm{C}_{\mathrm{Adj}}$ ) prevents ripple from being amplified as the output voltage is increased. A $10 \mu \mathrm{~F}$ capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.
Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance $\left(\mathrm{C}_{\mathrm{O}}\right)$ in the form of a $1.0 \mu \mathrm{~F}$ tantalum or $25 \mu \mathrm{~F}$ aluminum electrolytic capacitor on the output swamps this effect and insures stability.

## Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 20 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ( $\mathrm{C}_{\mathrm{O}}>25 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{Adj}}>5.0 \mu \mathrm{~F}$ ). Diode $\mathrm{D}_{1}$ prevents $\mathrm{C}_{\mathrm{O}}$ from discharging thru the IC during an input short circuit. Diode $\mathrm{D}_{2}$ protects against capacitor $\mathrm{C}_{\text {Adj }}$ discharging through the IC during an output short circuit. The combination of diodes $D_{1}$ and $D_{2}$ prevents $C_{\text {Adj }}$ from discharging through the IC during an input short circuit.


Figure 20. Voltage Regulator with Protection Diodes


Figure 21. Adjustable Current Limiter


Figure 23. Slow Turn-On Regulator


Figure 25. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

$D_{1}$ protects the device during an input short circuit.
Figure 22. 5 V Electronic Shutdown Regulator

$$
\begin{aligned}
I_{\text {outmax }}= & \left(\frac{V_{\text {ref }}}{R_{1}+R_{2}}\right)+I_{\text {Adj }} \cong \frac{1.25 \mathrm{~V}}{R_{1}+R_{2}} \\
& 5.0 \mathrm{~mA}<I_{\text {out }}<100 \mathrm{~mA}
\end{aligned}
$$

Figure 24. Current Regulator


Figure 26. SOT-223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## LM317M

## ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping |
| :--- | :---: | :---: | :---: |
| LM317MT | $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | TO-220 | 50 units/rail |
| LM317MDT | $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | DPAK | 75 units/rail |
| LM317MDTRK | $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | DPAK | 2500 units/Tape \& Reel |
| LM317MSTT3 | $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | SOT-223 | 4000 units/Tape \& Reel |
| LM317MBT | $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | TO-220 | 50 units/rail |
| LM317MBDT | $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | DPAK | 75 units/rail |
| LM317MBDTRK | $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | DPAK | 2500 units/Tape \& Reel |
| LM317MBSTT3 | $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ | SOT-223 | 4000 units/Tape \& Reel |

### 1.5 A Adjustable Output, Positive Voltage Regulator

The LM317 is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V . This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Available in Surface Mount D²PAK, and Standard 3-Lead Transistor Package
- Eliminates Stocking many Fixed Voltages


## Standard Application


${ }^{*} \mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter. ${ }^{* *} \mathrm{C}_{0}$ is not needed for stability, however, it does improve transient response.

$$
\mathrm{V}_{\text {out }}=1.25 \mathrm{~V}\left(1+\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}\right)+\mathrm{I}_{\mathrm{Adj}} \mathrm{R}_{2}
$$

Since $I_{\text {Adj }}$ is controlled to less than $100 \mu \mathrm{~A}$, the error associated with this term is negligible in most applications.

## LM317

## THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

## SEMICONDUCTOR TECHNICAL DATA

T SUFFIX
PLASTIC PACKAGE CASE 221A

Heatsink surface connected to Pin 2.


Pin 1. Adjust
2. $V_{\text {out }}$
3. $V_{\text {in }}$

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
( $\mathrm{D}^{2}$ PAK)


Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2 .


## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input-Output Voltage Differential | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | 40 | Vdc |
| Power Dissipation <br> Case 221A $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 936 ( $D^{2}$ PAK) $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $\begin{aligned} & \mathrm{P}_{\mathrm{D}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \\ & \\ & \mathrm{P}_{\mathrm{D}} \\ & \theta_{\mathrm{JA}} \\ & \theta_{\mathrm{JC}} \end{aligned}$ | Internally Limited <br> 65 <br> 5.0 <br> Internally Limited <br> 70 <br> 5.0 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V} ; \mathrm{I}_{\mathrm{O}}=0.5 \mathrm{~A}\right.$ for D2T and T packages; $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}[$ Note 1$] ; \mathrm{I}_{\text {max }}$ and $\mathrm{P}_{\max }$ [Note 2]; unless otherwise noted.)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation (Note 3), $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}$ | 1 | Regline | - | 0.01 | 0.04 | \%/V |
| $\begin{aligned} & \text { Load Regulation (Note 3), } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max } \\ & \mathrm{V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{aligned}$ | 2 | Regload | - | $\begin{aligned} & 5.0 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 25 \\ & 0.5 \end{aligned}$ | $\stackrel{\mathrm{mV}}{\% \mathrm{~V}_{\mathrm{O}}}$ |
| Thermal Regulation, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ( Note 6), 20 ms Pulse |  | Regtherm | - | 0.03 | 0.07 | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| Adjustment Pin Current | 3 | $I_{\text {Adj }}$ | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjustment Pin Current Change, $2.5 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}$, $10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{L}} \leq \mathrm{I}_{\text {max }}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\text {max }}$ | 1, 2 | $\Delta^{\text {Adj }}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Reference Voltage, } 3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}, \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max }, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max } \end{aligned}$ | 3 | $\mathrm{V}_{\text {ref }}$ | 1.2 | 1.25 | 1.3 | V |
| Line Regulation (Note 3), 3.0 V $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 40 \mathrm{~V}$ | 1 | Regline | - | 0.02 | 0.07 | \% V |
| $\begin{aligned} & \text { Load Regulation (Note 3), } 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max } \\ & \mathrm{V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{aligned}$ | 2 | Regload | - | $\begin{aligned} & 20 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 70 \\ & 1.5 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \% \mathrm{~V}_{\mathrm{O}} \end{gathered}$ |
| Temperature Stability ( $\mathrm{T}_{\text {low }} \leq \mathrm{T}_{J} \leq \mathrm{T}_{\text {high }}$ ) | 3 | Ts | - | 0.7 | - | \% $\mathrm{V}_{0}$ |
| Minimum Load Current to Maintain Regulation ( $\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}$ ) | 3 | $I_{L \text { min }}$ | - | 3.5 | 10 | mA |
| Maximum Output Current $\begin{aligned} & \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 15 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }, \text { T Package } \\ & \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=40 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{~T} \text { Package } \end{aligned}$ | 3 | $I_{\text {max }}$ | $\begin{gathered} 1.5 \\ 0.15 \end{gathered}$ | $\begin{aligned} & 2.2 \\ & 0.4 \end{aligned}$ | - | A |
| RMS Noise, \% of $\mathrm{V}_{\mathrm{O}}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ |  | N | - | 0.003 | - | \% $\mathrm{V}_{\mathrm{O}}$ |
| Ripple Rejection, $\mathrm{V}_{\mathrm{O}}=10 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz}$ (Note 4) Without $\mathrm{C}_{\text {Adj }}$ $\mathrm{C}_{\mathrm{Adj}}=10 \mu \mathrm{~F}$ | 4 | RR | $66$ | $\begin{aligned} & 65 \\ & 80 \end{aligned}$ | - | dB |
| Long-Term Stability, $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {high }}$ (Note 5), $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ for Endpoint Measurements | 3 | S | - | 0.3 | 1.0 | $\% / 1.0 \text { k }$ Hrs. |
| Thermal Resistance Junction to Case, T Package |  | $\mathrm{R}_{\text {өJC }}$ | - | 5.0 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

NOTES: 1. $T_{\text {low }}$ to $T_{\text {high }}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$, for LM317T, D2T. $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$, for LM317BT, BD2T.
2. $I_{\max }=1.5 \mathrm{~A}, \mathrm{P}_{\max }=20 \mathrm{~W}$
3. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. $\mathrm{C}_{\mathrm{Adj}}$, when used, is connected between the adjustment pin and ground.
5. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

## LM317

Representative Schematic Diagram


This device contains 29 active transistors.


Figure 1. Line Regulation and $\Delta \mathbf{I}_{\text {Adj }}$ /Line Test Circuit

## LM317



Figure 2. Load Regulation and $\Delta \mathbf{I}_{\text {Adj }}$ /Load Test Circuit


Figure 3. Standard Test Circuit


Figure 4. Ripple Rejection Test Circuit


Figure 5. Load Regulation


Figure 7. Adjustment Pin Current


Figure 9. Temperature Stability


Figure 6. Current Limit


Figure 8. Dropout Voltage


Figure 10. Minimum Operating Current


Figure 11. Ripple Rejection versus Output Voltage


Figure 13. Ripple Rejection versus Frequency


Figure 15. Line Transient Response

Figure 12. Ripple Rejection versus Output Current


Figure 14. Output Impedance


Figure 16. Load Transient Response

## APPLICATIONS INFORMATION

## Basic Circuit Operation

The LM317 is a 3-terminal floating regulator. In operation, the LM317 develops and maintains a nominal 1.25 V reference ( $\mathrm{V}_{\mathrm{ref}}$ ) between its output and adjustment terminals. This reference voltage is converted to a programming current ( $\mathrm{I}_{\mathrm{PROG}}$ ) by $\mathrm{R}_{1}$ (see Figure 17), and this constant current flows through $\mathrm{R}_{2}$ to ground.

The regulated output voltage is given by:

$$
v_{\text {out }}=V_{\text {ref }}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2}
$$

Since the current from the adjustment terminal ( $\mathrm{I}_{\text {Adj }}$ ) represents an error term in the equation, the LM317 was designed to control $\mathrm{I}_{\text {Adj }}$ to less than $100 \mu \mathrm{~A}$ and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.


Figure 17. Basic Circuit Configuration

## Load Regulation

The LM317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor $\left(\mathrm{R}_{1}\right)$ should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of $R_{2}$ can be returned near the load ground to provide remote ground sensing and improve load regulation.

## External Capacitors

A $0.1 \mu \mathrm{~F}$ disc or $1.0 \mu \mathrm{~F}$ tantalum input bypass capacitor $\left(\mathrm{C}_{\mathrm{in}}\right)$ is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ( $\mathrm{C}_{\mathrm{Adj}}$ ) prevents ripple from being amplified as the output voltage is increased. A $10 \mu \mathrm{~F}$ capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.
Although the LM317 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance $\left(\mathrm{C}_{\mathrm{O}}\right)$ in the form of a $1.0 \mu \mathrm{~F}$ tantalum or $25 \mu \mathrm{~F}$ aluminum electrolytic capacitor on the output swamps this effect and insures stability.

## Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ( $\mathrm{C}_{\mathrm{O}}>25 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{Adj}}>10 \mu \mathrm{~F}$ ). Diode $\mathrm{D}_{1}$ prevents $\mathrm{C}_{\mathrm{O}}$ from discharging thru the IC during an input short circuit. Diode $\mathrm{D}_{2}$ protects against capacitor $\mathrm{C}_{\text {Adj }}$ discharging through the IC during an output short circuit. The combination of diodes $D_{1}$ and $D_{2}$ prevents $C_{\text {Adj }}$ from discharging through the IC during an input short circuit.


Figure 18. Voltage Regulator with Protection Diodes

## LM317



Figure 19. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 20. "Laboratory" Power Supply with Adjustable Current Limit and Output Voltage

$\mathrm{V}_{\mathrm{O}}<\mathrm{BV}_{\mathrm{DSS}}+1.25 \mathrm{~V}+\mathrm{V}_{\mathrm{SS}}$, $I_{\text {Lmin }}-I_{D S S}<I_{0}<1.5 \mathrm{~A}$.
As shown $0<\mathrm{I}_{0}<1.0 \mathrm{~A}$.

Figure 21. Adjustable Current Limiter


Figure 23. Slow Turn-On Regulator


* $D_{1}$ protects the device during an input short circuit.

Figure 22. 5.0 V Electronic Shutdown Regulator


Figure 24. Current Regulator

### 3.0 A, Adjustable Output, Positive Voltage Regulator

The LM350 is an adjustable three-terminal positive voltage regulator capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V . This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM350 serves a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM350 can be used as a precision current regulator.

- Guaranteed 3.0 A Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically $0.1 \%$
- Line Regulation Typically 0.005\%/V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

${ }^{*}=\mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter. ${ }^{* *}=\mathrm{C}_{0}$ is not needed for stability, however, it does improve transient response.

$$
V_{\text {out }}=1.25 \mathrm{~V}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2}
$$

Since $\mathrm{I}_{\text {Adj }}$ is controlled to less than $100 \mu \mathrm{~A}$, the error associated with this term is negligible in most applications.

## THREE-TERMINAL

 ADJUSTABLE POSITIVE VOLTAGE REGULATOR
## SEMICONDUCTOR TECHNICAL DATA

T SUFFIX<br>PLASTIC PACKAGE CASE 221A



Pin 1. Adjust
2. $V_{\text {out }}$
3. $\mathrm{V}_{\text {in }}$

Heatsink surface is connected to Pin 2.
ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| LM350T | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | Plastic Power |
| LM350BT\# | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | Plastic Power |

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local ON Semiconductor sales office for information.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input-Output Voltage Differential | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | 35 | Vdc |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | W |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Soldering Lead Temperature (10 seconds) | $\mathrm{T}_{\text {solder }}$ | 300 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V} ; \mathrm{I}_{\mathrm{L}}=1.5 \mathrm{~A} ; \mathrm{T}_{J}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }} ; \mathrm{P}_{\text {max }}$ [Note 1], unless otherwise noted.)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation (Note 2) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 35 \mathrm{~V}$ | 1 | Regline | - | 0.0005 | 0.03 | \%/V |
| Load Regulation (Note 2) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 10 \mathrm{~mA} \leq \mathrm{I}_{1} \leq 3.0 \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{aligned}$ | 2 | Regload | - | $\begin{aligned} & 5.0 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 25 \\ & 0.5 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \% \mathrm{~V}_{\mathrm{O}} \end{gathered}$ |
| $\begin{aligned} & \text { Thermal Regulation, Pulse }=20 \mathrm{~ms}, \\ & \left(\mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right) \end{aligned}$ |  | $\mathrm{Reg}_{\text {therm }}$ | - | 0.002 | - | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| Adjustment Pin Current | 3 | $1_{\text {Adj }}$ | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjustment Pin Current Change $\begin{aligned} & 3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 35 \mathrm{~V} \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{L}} \leq 3.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max } \end{aligned}$ | 1,2 | $\Delta^{\text {Adj }}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Reference Voltage } \\ & 3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 35 \mathrm{~V} \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 3.0 \mathrm{~A}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max } \end{aligned}$ | 3 | $\mathrm{V}_{\text {ref }}$ | 1.20 | 1.25 | 1.30 | V |
| Line Regulation (Note 2) $3.0 \mathrm{~V} \leq \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}} \leq 35 \mathrm{~V}$ | 1 | Regline | - | 0.02 | 0.07 | \%/V |
| $\begin{gathered} \text { Load Regulation (Note 2) } \\ 10 \mathrm{~mA} \leq \mathrm{I} \leq 3.0 \mathrm{~A} \\ \mathrm{~V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{O}} \geq 5.0 \mathrm{~V} \end{gathered}$ | 2 | Regload | - | $\begin{aligned} & 20 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 70 \\ & 1.5 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \% \mathrm{~V}_{\mathrm{O}} \end{gathered}$ |
| Temperature Stability ( $\mathrm{T}_{\text {low }} \leq \mathrm{T}_{\mathrm{J}} \leq \mathrm{T}_{\text {high }}$ ) | 3 | Ts | - | 1.0 | - | \% $\mathrm{V}_{0}$ |
| Minimum Load Current to <br> Maintain Regulation $\left(\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=35 \mathrm{~V}\right)$ | 3 | $I_{\text {Lmin }}$ | - | 3.5 | 10 | mA |
| $\begin{aligned} & \text { Maximum Output Current } \\ & V_{1}-\mathrm{V}_{\mathrm{O}} \leq 10 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max } \\ & \mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}=30 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ | 3 | $I_{\text {max }}$ | $\begin{gathered} 3.0 \\ 0.25 \end{gathered}$ | $\begin{aligned} & 4.5 \\ & 1.0 \end{aligned}$ |  | A |
| $\begin{aligned} & \text { RMS Noise, \% of } V_{O} \\ & T_{A}=25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} \end{aligned}$ |  | N | - | 0.003 | - | \% $\mathrm{V}_{\mathrm{O}}$ |
| $\begin{aligned} & \text { Ripple Rejection, } \mathrm{V}_{\mathrm{O}}=10 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz} \text { (Note 3) } \\ & \text { Without }^{\mathrm{C}_{\text {Adj }}} \\ & \mathrm{C}_{\text {Adj }}=10 \mu \mathrm{~F} \end{aligned}$ | 4 | RR | $66$ | $\begin{aligned} & 65 \\ & 80 \end{aligned}$ | - | dB |
| Long Term Stability, $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {high }}$ (Note 4) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for Endpoint Measurements | 3 | S | - | 0.3 | 1.0 | \%/1.0 k Hrs. |
| Thermal Resistance, Junction-to-Case Peak (Note 5) Average (Note 6) |  | $\mathrm{R}_{\text {өJC }}$ | - | $2.3$ | $\begin{gathered} - \\ 1.5 \end{gathered}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

NOTES: 1. $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=0^{\circ}$ to $+125^{\circ} \mathrm{C} ; \mathrm{P}_{\max }=25 \mathrm{~W}$ for LM350T; $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=-40^{\circ}$ to $+125^{\circ} \mathrm{C} ; \mathrm{P}_{\max }=25 \mathrm{~W}$ for LM350BT
2. Load and line regulation are specified at constant junction temperature. Changes in $\mathrm{V}_{\mathrm{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
3. $\mathrm{C}_{\text {Adj }}$, when used, is connected between the adjustment pin and ground.
4. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
5. Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to the other measurement techniques.
6. The average die temperature is used to derive the value of thermal resistance junction to case (average).

## LM350

Representative Schematic Diagram


Figure 1. Line Regulation and $\Delta \mathbf{I}_{\text {Adj }} /$ Line Test Circuit

## LM350



Figure 2. Load Regulation and $\Delta^{\text {Adj }}$ ILoad Test Circuit


Figure 3. Standard Test Circuit


Figure 4. Ripple Rejection Test Circuit


Figure 5. Load Regulation


Figure 7. Adjustment Pin Current


Figure 6. Current Limit


Figure 8. Dropout Voltage


Figure 9. Temperature Stability


Figure 10. Minimum Operating Current


Figure 11. Ripple Rejection versus Output Voltage


Figure 12. Ripple Rejection versus Output Current


Figure 13. Ripple Rejection versus Frequency


Figure 15. Line Transient Response


Figure 16. Load Transient Response

## APPLICATIONS INFORMATION

## Basic Circuit Operation

The LM350 is a three-terminal floating regulator. In operation, the LM350 develops and maintains a nominal 1.25 V reference ( $\mathrm{V}_{\mathrm{ref}}$ ) between its output and adjustment terminals. This reference voltage is converted to a programming current (IPROG) by $\mathrm{R}_{1}$ (see Figure 17), and this constant current flows through $\mathrm{R}_{2}$ to ground. The regulated output voltage is given by:

$$
V_{\text {out }}=V_{\text {ref }}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2}
$$

Since the current from the terminal ( $\mathrm{I}_{\mathrm{Adj}}$ ) represents an error term in the equation, the LM350 was designed to control $\mathrm{I}_{\text {Adj }}$ to less than $100 \mu \mathrm{~A}$ and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM350 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.


Figure 17. Basic Circuit Configuration

## Load Regulation

The LM350 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor $\left(\mathrm{R}_{1}\right)$ should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of $\mathrm{R}_{2}$ can be returned near the load ground to provide remote ground sensing and improve load regulation.

## External Capacitors

A $0.1 \mu \mathrm{~F}$ disc or $1 \mu \mathrm{~F}$ tantalum input bypass capacitor $\left(\mathrm{C}_{\mathrm{in}}\right)$ is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ( $\mathrm{C}_{\mathrm{Adj}}$ ) prevents ripple from being amplified as the output voltage is increased. A $10 \mu \mathrm{~F}$ capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM350 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance $\left(\mathrm{C}_{\mathrm{O}}\right)$ in the form of a $1 \mu \mathrm{~F}$ tantalum or $25 \mu \mathrm{~F}$ aluminum electrolytic capacitor on the output swamps this effect and insures stability.

## Protection Diodes

When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM350 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values $\left(\mathrm{C}_{\mathrm{O}}>25 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{Adj}}>10 \mu \mathrm{~F}\right)$. Diode $\mathrm{D}_{1}$ prevents $\mathrm{C}_{\mathrm{O}}$ from discharging thru the IC during an input short circuit. Diode $\mathrm{D}_{2}$ protects against capacitor $\mathrm{C}_{\text {Adj }}$ discharging through the IC during an output short circuit. The combination of diodes $D_{1}$ and $D_{2}$ prevents $C_{\text {Adj }}$ from discharging through the IC during an input short circuit.


Figure 18. Voltage Regulator with Protection Diodes

## LM350



Figure 19. "Laboratory" Power Supply with Adjustable Current Limit and Output Voltage


Figure 20. Adjustable Current Limiter


Figure 22. Slow Turn-On Regulator

$D_{1}$ protects the device during an input short circuit.
Figure 21. 5.0 V Electronic Shutdown Regulator


Figure 23. Current Regulator

### 1.5 A, Adjustable Output, Negative Voltage Regulator

The LM337 is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of -1.2 V to -37 V . This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM337 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable between -1.2 V and -37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking many Fixed Voltages
- Available in Surface Mount D²PAK and Standard 3-Lead Transistor Package


## Standard Application



D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D2PAK)
 PLASTIC PACKAGE CASE 221A

Heatsink surface connected to Pin 2.

Pin 1. Adjust
2. $V_{\text {in }}$
3. $V_{\text {out }}$

## SEMICONDUCTOR

 TECHNICAL DATA
## THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SUFFIX

Heatsink surface

Heasink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
| :---: | :---: | :---: |
| LM337BD2T | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | Surface Mount |
| LM337BT |  | Insertion Mount |
| LM337D2T | $\mathrm{T}_{J}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$ | Surface Mount |
| LM337T |  | Insertion Mount |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input-Output Voltage Differential | $\mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}}$ | 40 | Vdc |
| Power Dissipation |  |  |  |
| Case 221 A |  |  |  |
| $\mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | W |
| Thermal Resistance, Junction-to-Ambient | $\theta_{\mathrm{JA}}$ | 65 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case | $\theta_{\mathrm{JC}}$ | 5.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Case $936\left(\mathrm{D}^{2} \mathrm{PAK}\right)$ |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | W |
| Thermal Resistance, Junction-to-Ambient | $\theta_{\mathrm{JA}}$ | 70 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case | $\theta_{\mathrm{JC}}$ | 5.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mid \mathrm{V}_{\mathrm{l}} \mathrm{V} \mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V} ; \mathrm{I}_{\mathrm{O}}=0.5 \mathrm{~A}$ for T package; $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ [Note 1]; $\mathrm{I}_{\max }$ and $\mathrm{P}_{\max }$ [Note 2].)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation (Note 3), $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 3.0 \mathrm{~V} \leq \mid \mathrm{V}_{\mathrm{I}}-\mathrm{V}_{\mathrm{O}} \mathrm{l} \leq 40 \mathrm{~V}$ | 1 | Regline | - | 0.01 | 0.04 | \%/V |
| $\begin{aligned} & \text { Load Regulation (Note 3), } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max } \\ & \left\|\mathrm{V}_{\mathrm{O}}\right\| \leq 5.0 \mathrm{~V} \\ & \left\|\mathrm{~V}_{\mathrm{O}}\right\| \geq 5.0 \mathrm{~V} \end{aligned}$ | 2 | Regload | - | $\begin{aligned} & 15 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 50 \\ & 1.0 \end{aligned}$ | $\stackrel{m V}{\% V_{O}}$ |
| Thermal Regulation, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Note 6), 10 ms Pulse |  | $\mathrm{Reg}_{\text {therm }}$ | - | 0.003 | 0.04 | \% $\mathrm{V}_{\mathrm{O}} / \mathrm{W}$ |
| Adjustment Pin Current | 3 | $\mathrm{I}_{\text {Adj }}$ | - | 65 | 100 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Adjustment Pin Current Change, } 2.5 \mathrm{~V} \leq\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\| \leq 40 \mathrm{~V} \text {, } \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{L}} \leq \mathrm{I}_{\max }, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ | 1, 2 | $\Delta^{\text {Adj }}$ | - | 2.0 | 5.0 | $\mu \mathrm{A}$ |
| Reference Voltage, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 3.0 \mathrm{~V} \leq\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\| \leq 40 \mathrm{~V}$, $10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\text {max }}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\text {max }}, \mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ | 3 | $\mathrm{V}_{\text {ref }}$ | $\begin{gathered} \hline-1.213 \\ -1.20 \end{gathered}$ | $\begin{gathered} -1.250 \\ -1.25 \end{gathered}$ | $\begin{gathered} -1.287 \\ -1.30 \end{gathered}$ | V |
| Line Regulation (Note 3), 3.0 $\mathrm{V} \leq\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\| \leq 40 \mathrm{~V}$ | 1 | Regline | - | 0.02 | 0.07 | \%/V |
| $\begin{aligned} & \text { Load Regulation (Note 3), } 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq \mathrm{I}_{\max } \\ & \mid \mathrm{V}_{\mathrm{O}} \leq 5.0 \mathrm{~V} \\ & \left\|\mathrm{~V}_{\mathrm{O}}\right\| \geq 5.0 \mathrm{~V} \end{aligned}$ | 2 | Regload | - | $\begin{aligned} & 20 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 70 \\ & 1.5 \end{aligned}$ | $\begin{gathered} \mathrm{mV} \\ \% \mathrm{~V}_{\mathrm{O}} \\ \hline \end{gathered}$ |
| Temperature Stability ( $\mathrm{T}_{\text {low }} \leq \mathrm{T}_{\mathrm{J}} \leq \mathrm{T}_{\text {high }}$ ) | 3 | $\mathrm{T}_{\text {S }}$ | - | 0.6 | - | \% $\mathrm{V}_{0}$ |
| Minimum Load Current to Maintain Regulation $\begin{aligned} & \left(\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\| \leq 10 \mathrm{~V}\right) \\ & \left(\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\| \leq 40 \mathrm{~V}\right) \end{aligned}$ | 3 | $I_{\text {Lmin }}$ | - | $\begin{aligned} & 1.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 10 \end{aligned}$ | mA |
| Maximum Output Current $\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\| \leq 15 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\text {max }}$, T Package $\left\|\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}\right\| \leq 40 \mathrm{~V}, \mathrm{P}_{\mathrm{D}} \leq \mathrm{P}_{\max }, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$, T Package | 3 | $I_{\text {max }}$ | - | $\begin{gathered} 1.5 \\ 0.15 \\ \hline \end{gathered}$ | $\begin{aligned} & 2.2 \\ & 0.4 \end{aligned}$ | A |
| RMS Noise, \% of $\mathrm{V}_{\mathrm{O}}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, 10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ |  | N | - | 0.003 | - | \% $\mathrm{V}_{\mathrm{O}}$ |
| Ripple Rejection, $\mathrm{V}_{\mathrm{O}}=-10 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz}$ (Note 4) Without $\mathrm{C}_{\text {Adj }}$ $\mathrm{C}_{\mathrm{Adj}}=10 \mu \mathrm{~F}$ | 4 | RR | $\overline{66}$ | $\begin{aligned} & 60 \\ & 77 \end{aligned}$ | - | dB |
| Long-Term Stability, $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {high }}$ (Note 5), $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ for Endpoint Measurements | 3 | S | - | 0.3 | 1.0 | \%/1.0 k Hrs. |
| Thermal Resistance Junction-to-Case, T Package |  | $\mathrm{R}_{\text {өJC }}$ | - | 4.0 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

NOTES: 1. $T_{\text {low }}$ to $T_{\text {high }}=0^{\circ}$ to $+125^{\circ} \mathrm{C}$, for LM337T, D2T. $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$, for LM337BT, BD2T.
2. $I_{\max }=1.5 \mathrm{~A}, \mathrm{P}_{\max }=20 \mathrm{~W}$
3. Load and line regulation are specified at constant junction temperature. Change in $\mathrm{V}_{\mathrm{O}}$ because of heating effects is covered under the Thermal Regulation specification. Pulse testing with a low duty cycle is used.
4. C $_{\text {Adj, }}$, when used, is connected between the adjustment pin and ground.
5. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

Representative Schematic Diagram


This device contains 39 active transistors.


Figure 1. Line Regulation and $\Delta \mathbf{I}_{\text {Adj }}$ /Line Test Circuit

## LM337



Figure 2. Load Regulation and $\Delta \mathbf{I}_{\text {Adj }}$ /Load Test Circuit


To Calculate $R_{2}: \quad R_{2}=\left(\frac{V_{0}}{V_{\text {ref }}}-1\right) R_{1}$
This assumes $\mathrm{I}_{\mathrm{Adj}}$ is negligible.

* Pulse testing required.
$1 \%$ Duty Cycle is suggested.
Figure 3. Standard Test Circuit

* $D_{1}$ Discharges $C_{\text {Adj }}$ if output is shorted to Ground.

Figure 4. Ripple Rejection Test Circuit


Figure 5. Load Regulation


Figure 7. Adjustment Pin Current


Figure 9. Temperature Stability


Figure 6. Current Limit


Figure 8. Dropout Voltage


Figure 10. Minimum Operating Current


Figure 11. Ripple Rejection versus Output Voltage


Figure 12. Ripple Rejection versus Output Current


Figure 13. Ripple Rejection versus Frequency


Figure 14. Output Impedance


Figure 15. Line Transient Response


Figure 16. Load Transient Response

## APPLICATIONS INFORMATION

## Basic Circuit Operation

The LM337 is a 3-terminal floating regulator. In operation, the LM337 develops and maintains a nominal -1.25 V reference ( $\mathrm{V}_{\text {reff }}$ ) between its output and adjustment terminals. This reference voltage is converted to a programming current ( $\mathrm{I}_{\mathrm{PROG}}$ ) by $\mathrm{R}_{1}$ (see Figure 17), and this constant current flows through $\mathrm{R}_{2}$ from ground.

The regulated output voltage is given by:

$$
v_{\text {out }}=V_{\text {ref }}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2}
$$

Since the current into the adjustment terminal ( $\mathrm{I}_{\text {Adj }}$ ) represents an error term in the equation, the LM337 was designed to control $\mathrm{I}_{\text {Adj }}$ to less than $100 \mu \mathrm{~A}$ and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.


Figure 17. Basic Circuit Configuration

## Load Regulation

The LM337 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor $\left(\mathrm{R}_{1}\right)$ should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby
degrading regulation. The ground end of $\mathrm{R}_{2}$ can be returned near the load ground to provide remote ground sensing and improve load regulation.

## External Capacitors

A $1.0 \mu \mathrm{~F}$ tantalum input bypass capacitor $\left(\mathrm{C}_{\mathrm{in}}\right)$ is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor ( $\mathrm{C}_{\mathrm{Adj}}$ ) prevents ripple from being amplified as the output voltage is increased. A $10 \mu \mathrm{~F}$ capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

An output capacitance $\left(\mathrm{C}_{\mathrm{O}}\right)$ in the form of a $1.0 \mu \mathrm{~F}$ tantalum or $10 \mu \mathrm{~F}$ aluminum electrolytic capacitor is required for stability.

## Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337 with the recommended protection diodes for output voltages in excess of -25 V or high capacitance values ( $\mathrm{C}_{\mathrm{O}}>25 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{Adj}}>10 \mu \mathrm{~F}$ ). Diode $\mathrm{D}_{1}$ prevents $\mathrm{C}_{\mathrm{O}}$ from discharging thru the IC during an input short circuit. Diode $\mathrm{D}_{2}$ protects against capacitor $\mathrm{C}_{\text {Adj }}$ discharging through the IC during an output short circuit. The combination of diodes $D_{1}$ and $D_{2}$ prevents $C_{\text {Adj }}$ from the discharging through the IC during an input short circuit.


Figure 18. Voltage Regulator with Protection Diodes


Figure 19. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC78LC00 Series

## Micropower Voltage Regulator

The MC78LC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78LC00 series features an ultra-low quiescent current of $1.1 \mu \mathrm{~A}$ and a high accuracy output voltage. Each device contains a voltage reference, an error amplifier, a driver transistor and resistors for setting the output voltage. These devices are available in either SOT-89, 3 pin, or SOT-23, 5 pin, surface mount packages.

## Features

- Low Quiescent Current of $1.1 \mu \mathrm{~A}$ Typical
- Low Dropout Voltage ( 220 mV at 10 mA )
- Excellent Line Regulation (0.1\%)
- High Accuracy Output Voltage ( $\pm 2.5 \%$ )
- Output Current for Low Power (up to 80 mA )
- Two Surface Mount Packages (SOT-89, 3 Pin, or SOT-23, 5 Pin)


Figure 1. Representative Block Diagram

## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com

PIN CONNECTIONS AND MARKING DIAGRAMS

(Tab is connected to Pin 2)

$$
\begin{aligned}
& \mathrm{xx}=\text { Version } \\
& \mathrm{YY}=\text { Lot }
\end{aligned}
$$

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 253 of this data sheet.

## MC78LC00 Series

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 12 | Vdc |
| Power Dissipation and Thermal Characteristics |  |  |  |
| Maximum Power Dissipation |  |  |  |
| Case 1213 (SOT-89) H Suffix | $\mathrm{P}_{\mathrm{D}}$ | 300 | mW |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {OJA }}$ | 333 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Case 1212 (SOT-23) N Suffix | $\mathrm{P}_{\mathrm{D}}$ | 150 | mW |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {日JA }}$ | 667 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 to +80 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O}}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ (Note 2) unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage <br> 30 HT 1 and 30 NTR Suffixes $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> 33 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> 40 HT 1 Suffix $\left(\mathrm{V}_{\mathrm{in}}=6.0 \mathrm{~V}\right)$ <br> 50 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 2.950 \\ & 3.218 \\ & 3.900 \\ & 4.875 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.3 \\ & 4.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.075 \\ & 3.382 \\ & 4.100 \\ & 5.125 \end{aligned}$ | V |
| Line Regulation $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1.0\right] \mathrm{V} \text { to } 10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ | Regline | - | 0.05 | 0.2 | \%/V |
| $\begin{aligned} & \text { Load Regulation }\left(\mathrm{I}_{\mathrm{o}}=1.0 \text { to } 10 \mathrm{~mA}\right) \\ & 30 \mathrm{HT} 1 \text { and 30NTR Suffixes }\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right) \\ & 33 \mathrm{HT} 1 \text { Suffix }\left(\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}\right) \\ & 40 \mathrm{HT} 1 \text { Suffix }\left(\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}\right) \\ & 50 \mathrm{HT} 1 \text { Suffix }\left(\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}\right) \end{aligned}$ | Regload |  | $\begin{aligned} & 40 \\ & 40 \\ & 50 \\ & 60 \end{aligned}$ | $\begin{aligned} & 60 \\ & 60 \\ & 70 \\ & 90 \end{aligned}$ | mV |
| Output Current <br> 30 HT 1 and 30 NTR Suffixes $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> 33 HT 1 Suffix $\left(\mathrm{V}_{\mathrm{in}}=6.0 \mathrm{~V}\right)$ <br> 40 HT 1 Suffix $\left(\mathrm{V}_{\mathrm{in}}=7.0 \mathrm{~V}\right)$ <br> 50 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | 10 | $\begin{aligned} & 35 \\ & 35 \\ & 45 \\ & 55 \end{aligned}$ | $\begin{aligned} & 50 \\ & 50 \\ & 65 \\ & 80 \\ & \hline \end{aligned}$ | - | mA |
| $\begin{aligned} & \text { Dropout Voltage } \\ & 30 \mathrm{HT} 1 \text { and } 30 \mathrm{NTR} \text { Suffixes }\left(\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}\right) \\ & 33 \mathrm{HT1} \text { Suffix }\left(I_{0}=1.0 \mathrm{~mA}\right) \\ & 40 \mathrm{HT} 1 \text { Suffix }\left(\mathrm{I}_{0}=1.0 \mathrm{~mA}\right) \\ & 50 \mathrm{HT} 1 \text { Suffix }\left(\mathrm{I}_{0}=1.0 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - - - | $\begin{aligned} & 40 \\ & 35 \\ & 25 \\ & 25 \end{aligned}$ | $\begin{aligned} & 60 \\ & 53 \\ & 38 \\ & 38 \\ & \hline \end{aligned}$ | mV |
| Quiescent Current <br> 30 HT 1 and 30 NTR Suffixes $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right.$ ) <br> 33 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> 40 HT 1 Suffix ( $\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}$ ) <br> 50 HT 1 Suffix ( $\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}$ ) | Icc |  | $\begin{aligned} & 1.1 \\ & 1.1 \\ & 1.2 \\ & 1.3 \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 3.3 \\ & 3.6 \\ & 3.9 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm/ ${ }^{\circ} \mathrm{C}$ |

2. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

## MC78LC00 Series

## DEFINITIONS

Dropout Voltage - The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.
Line Regulation - The change in output voltage for a change in input voltage. The measurement is made under conditions


Figure 2. Output Voltage versus Input Voltage


Figure 4. Dropout Voltage versus Output Current
of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.
Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.
Quiescent Bias Current - Current which is used to operate the regulator chip and is not delivered to the load.


Figure 3. Output Voltage versus Output Current


Figure 5. Output Voltage versus Temperature


Figure 6. Quiescent Current versus Input Voltage


Figure 7. Quiescent Current versus Temperature


Figure 9. Line Transient Response

## MC78LC00 Series

## APPLICATIONS INFORMATION

## Introduction

The MC78LC00 micropower voltage regulators are specifically designed with high accuracy output voltage and ultra low quiescent current by CMOS process making them ideal for battery powered applications and hand-held communication equipment. An input bypass capacitor is recommended if the regulator is located an appreciable distance ( $\geq 4$ inches) from the input voltage source. These regulators require $\geq 0.1 \mu \mathrm{~F}$ capacitance between the output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or other appropriate capacitors are recommended for operation below $25^{\circ} \mathrm{C}$. The bypass capacitors should be mounted with the shortest possible leads or track lengths directly across the regulator input and output terminals.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the
electrolyte freezes, around $-30^{\circ} \mathrm{C}$, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ are readily available. Solid tantalum capacitors may be the better choice if small size is a requirement. However, a maximum ESR limit of $3.0 \Omega$ must be observed over temperature to maintain stability.

In the Current Boost Circuit, shown in Figures 11 and 13, an output current of up to 600 mA can be delivered by the circuit. The circuit of Figure 11 has no current limit. In each case, the external transistor must be rated for the expected power dissipation. Figure 12 shows how a fixed output may be programmed, using R1 and R2, to provide a higher output voltage.


Figure 11. Current Boost Circuit


Figure 13. Current Boost Circuit with Overcurrent Limit Circuit

## MC78LC00 Series

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| MC78LC30NTR | 3.0 | 0C | SOT-23 | 3000 Units/7" Tape \& Reel |
| MC78LC30HT1 | 3.0 | OC |  |  |
| MC78LC33HT1 | 3.3 | SC | SOT-89 | 1000 Units Tape \& Reel |
| MC78LC40HT1 | 4.0 | OD |  |  |
| MC78LC50HT1 | 5.0 | $0 E$ |  |  |

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## MC33761

## Ultra Low-Noise Low Dropout Voltage Regulator with 1.0 V ON/OFF Control

The MC33761 is an Low DropOut (LDO) regulator featuring excellent noise performances. Thanks to its innovative design, the circuit reaches an impressive $40 \mu \mathrm{VRMS}$ noise level without an external bypass capacitor. Housed in a small SOT-23 5 leads-like package, it represents the ideal designer's choice when space and noise are at premium.

The absence of external bandgap capacitor accelerates the response time to a wake-up signal and keeps it within $40 \mu$ s (in repetitive mode), making the MC33761 as a natural candidate for portable applications.

The MC33761 also hosts a novel architecture which prevents excessive undershoots in the presence of fast transient bursts, as in any bursting systems.

Finally, with a static line regulation better than -75 dB , it naturally shields the downstream electronics against choppy lines.

## Features

- Ultra-Low Noise: $150 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$ @ $100 \mathrm{~Hz}, 40 \mu \mathrm{VRMS}$ $100 \mathrm{~Hz}-100 \mathrm{kHz}$ Typical, $\mathrm{I}_{\text {out }}=60 \mathrm{~mA}, \mathrm{Co}=1.0 \mu \mathrm{~F}$
- Fast Response Time from OFF to ON: $40 \mu$ s Typical at a 200 Hz Repetition Rate
- Ready for 1.0 V Platforms: ON with a 900 mV High Level
- Nominal Output Current of 80 mA with a 100 mA Peak Capability
- Typical Dropout of 90 mV @ $30 \mathrm{~mA}, 160 \mathrm{mV}$ @ 80 mA
- Ripple Rejection: 70 dB @ 1.0 kHz
- $1.5 \%$ Output Precision @ $25^{\circ} \mathrm{C}$
- Thermal Shutdown
- $\mathrm{V}_{\text {out }}$ Available at $2.5 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}$
- Operating Range from -40 to $+85^{\circ} \mathrm{C}$
- Dual Version is Available as MC33762


## Applications

- Noise Sensitive Circuits: VCOs RF Stages, etc.
- Bursting Systems (TDMA Phones)
- All Battery Operated Devices


Figure 1. Simplified Block Diagram

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


THIN SOT-23-5
SN SUFFIX CASE 483

PIN CONNECTIONS AND MARKING DIAGRAM

$\mathrm{xx}=$ Version
$Y=$ Year
W = Work Week

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 266 of this data sheet.

## PIN FUNCTION DESCRIPTIONS

| Pin \# | Pin Name | Function | Description |
| :---: | :---: | :--- | :--- |
| 1 | $V_{\text {in }}$ | Powers the IC | A positive voltage up to 12 V can be applied upon this pin. |
| 2 | GND | The IC's ground |  |
| 3 | ON/OFF | Shuts or wakes-up <br> the IC | A 900 mV level on this pin is sufficient to start the IC. A 150 mV shuts it down. |
| 4 | NC | None | It makes no arm to connect the pin to a known potential, like in a pin-to-pin <br> replacement case. |
| 5 | V $_{\text {out }}$ | Delivers the output <br> voltage | This pin requires a $1.0 \mu \mathrm{~F}$ output capacitor to be stable. |

## MAXIMUM RATINGS

| Rating | Pin \# | Symbol | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |
| Power Supply Voltage | 1 | $V_{\text {in }}$ | - | 12 | V |
| ESD Capability, HBM Model | All Pins | - | - | 1.0 | kV |
| ESD Capability, Machine Model | All Pins | - | - | 200 | V |
| Maximum Power Dissipation NW Suffix, Plastic Package Thermal Resistance Junction-to-Air | - | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ |  | Internally Limited $210$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{w} \end{gathered}$ |
| Operating Ambient Temperature <br> Maximum Junction Temperature (Note 1) <br> Maximum Operating Junction Temperature (Note 2) | - | $\begin{gathered} \mathrm{T}_{\mathrm{A}} \\ \mathrm{~T}_{\mathrm{max}} \\ \mathrm{~T}_{\mathrm{J}} \end{gathered}$ | - | $\begin{gathered} -40 \text { to }+85 \\ 150 \\ 125 \end{gathered}$ | $\circ$ <br>  <br>  <br>  <br>  <br>  <br>  <br>  <br> C <br> C |
| Storage Temperature Range | - | $\mathrm{T}_{\text {stg }}$ | - | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |

## ELECTRICAL CHARACTERISTICS

(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, max $\mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristics | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

Logic Control Specifications

| Input Voltage Range | 3 | $\mathrm{~V}_{\text {ON/ }} \overline{\overline{F F}}$ | 0 | - | $\mathrm{V}_{\text {in }}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| ON/OFF Input Resistance (all versions) | 3 | $\mathrm{R}_{\text {ON/OFF }}$ | - | 250 | - | $\mathrm{k} \Omega$ |
| ON/OFF Control Voltages (Note 3) | 3 | $\mathrm{~V}_{\text {ON/OFF }}$ |  |  |  | mV |
| Logic Zero, OFF State, IO $=50 \mathrm{~mA}$ |  |  | - | - | 150 |  |
| Logic One, ON State, IO $=50 \mathrm{~mA}$ |  |  | 900 | - | - |  |

## Currents Parameters

| Current Consumption in OFF State (all versions) OFF Mode Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0, \mathrm{~V}_{\text {OFF }}=150 \mathrm{mV}$ | - | $\mathrm{IQ}_{\text {OFF }}$ | - | 0.1 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Current Consumption in ON State (all versions) ON Mode Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0, \mathrm{~V}_{\mathrm{ON}}=3.5 \mathrm{~V}$ | - | $\mathrm{IQ}_{\mathrm{ON}}$ | - | 180 | - | $\mu \mathrm{A}$ |
| Current Consumption in ON State (all versions), ON Mode Saturation Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}-0.5 \mathrm{~V}$, No Output Load | - | $\mathrm{IQ}_{\text {SAT }}$ | - | 800 | - | $\mu \mathrm{A}$ |
| Current Limit $\mathrm{V}_{\text {in }}=$ Vout $_{\text {nom }}+1.0 \mathrm{~V}$, <br> Output is brought to Vout $_{\text {nom }}-0.3 \mathrm{~V}$ (all versions) | - | $I_{\text {MAX }}$ | 100 | 180 | - | mA |

1. Internally limited by shutdown.
2. Specifications are guaranteed below this value.
3. Voltage slope should be greater than $2.0 \mathrm{mV} / \mathrm{us}$.

ELECTRICAL CHARACTERISTICS (continued)
(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, max $\mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristics | Pin \# | Symbol | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

## Output Voltages

| $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<80 \mathrm{~mA}$ <br> 2.5 V | 5 | $\mathrm{~V}_{\text {out }}$ | 2.462 | 2.5 | 2.537 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| 2.8 V | 5 | $\mathrm{~V}_{\text {out }}$ | 2.758 | 2.8 | 2.842 | V |
| 3.0 V | 5 | $\mathrm{~V}_{\text {out }}$ | 2.955 | 3.0 | 3.045 | V |
| 5.0 V | 5 | $\mathrm{~V}_{\text {out }}$ | 4.925 | 5.0 | 5.075 | V |
| Other Voltages up to 5.0 V Available in 50 mV Increment Steps | 5 | $\mathrm{~V}_{\text {out }}$ | -1.5 | X | +1.5 | $\%$ |
| $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<80 \mathrm{~mA}$ <br> 2.5 V | 5 | $\mathrm{~V}_{\text {out }}$ | 2.425 | 2.5 | 2.575 | V |
| 2.8 V | 5 | $\mathrm{~V}_{\text {out }}$ | 2.716 | 2.8 | 2.884 | V |
| 3.0 V | 5 | $\mathrm{~V}_{\text {out }}$ | 2.91 | 3.0 | 3.090 | V |
| 5.0 V | 5 | $\mathrm{~V}_{\text {out }}$ | 4.850 | 5.0 | 5.150 | V |
| Other Voltages up to 5.0 V Available in 50 mV Increment Steps | 5 | $\mathrm{~V}_{\text {out }}$ | -3.0 | X | +3.0 | $\%$ |

## Line and Load Regulation, Dropout Voltages

| Line Regulation (all versions) $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<12 \mathrm{~V}, \mathrm{I}_{\text {out }}=80 \mathrm{~mA}$ | 5/1 | Regline | - | - | 20 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Load Regulation (all versions) $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=1.0 \text { to } 80 \mathrm{~mA}$ | 5 | Reg ${ }_{\text {Ioad }}$ | - | - | 40 | mV |
| $\begin{aligned} & \text { Dropout Voltage (all versions) (Note 4) } \\ & \mathrm{I}_{\text {out }}=30 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=60 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=80 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 5 \\ & 5 \end{aligned}$ | $\begin{aligned} & V_{\text {in }}-V_{\text {out }} \\ & V_{\text {in }}-V_{\text {out }} \\ & V_{\text {in }}-V_{\text {out }} \end{aligned}$ | - | $\begin{gathered} 90 \\ 140 \\ 160 \end{gathered}$ | $\begin{aligned} & 150 \\ & 200 \\ & 250 \end{aligned}$ | mV |

## Dynamic Parameters

| Ripple Rejection (all versions) <br> $V_{\text {in }}=V_{\text {out }}+1.0 \mathrm{~V}+1.0 \mathrm{kHz} 100 \mathrm{mVpp}$ Sinusoidal Signal | $5 / 1$ | Ripple | - | -70 | - | dB |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Noise Density @ 1.0 kHz | 5 | - | - | 150 | - | $\mathrm{nV} /$ |
| VHz |  |  |  |  |  |  |$|$

## Thermal Shutdown

| Thermal Shutdown (all versions) | - | - | - | - | 125 | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |

4. $\mathrm{V}_{\text {out }}$ is brought to $\mathrm{V}_{\text {out }}-100 \mathrm{mV}$.

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant chip temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential value). The dropout level is affected by the chip temperature, load current and minimum input supply requirements.

## Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output current are kept constant during the measurement. Results are expressed in $\mu$ VRMS.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specs.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected. One usually distinguishes static line regulation or DC line regulation (a DC step in the input voltage generates a corresponding step in the output voltage) from ripple rejection or audio susceptibility where the input is combined with a frequency generator to sweep from a few hertz up to a defined boundary while the output amplitude is monitored.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $125^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package power dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient temperature, it is possible to calculate the maximum power dissipation and thus the maximum available output current.

## Characterization Curves

All curves taken with $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {out }}=2.8 \mathrm{~V}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}$


Figure 2. Ground Current versus Output Current

Figure 4. Dropout versus Output Current


Figure 3. Quiescent Current versus Temperature

Figure 5. Output Voltage versus Output Current


Figure 6. Dropout versus Temperature

## APPLICATION HINTS

## Input Decoupling

As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the MC33761 package. Higher values will correspondingly improve the overall line transient response.

## Output Decoupling

Thanks to a novel concept, the MC33761 is a stable component and does not require any specific Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

## Noise Decoupling

Unlike other LDOs, the MC33761 is a true low-noise regulator. Without the need of an external bypass capacitor, it typically reaches the incredible level of $40 \mu \mathrm{VRMS}$ overall noise between 100 Hz and 100 kHz . To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics. The classical bypass capacitor impacts the start-up phase of standard LDOs. However, thanks to its low-noise architecture, the MC33761 operates without a bypass element and thus offers a typical $40 \mu$ s start-up phase.

## Protections

The MC33761 hosts several protections, giving natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a maximum value of 180 mA typical while temperature shutdown occurs if the die heats up beyond $125^{\circ} \mathrm{C}$. These values let you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$
P_{\max }=\frac{T_{J \max }-T_{A}}{R_{\theta J A}}
$$

If $\mathrm{T}_{\text {Jmax }}$ is limited to $125^{\circ} \mathrm{C}$, then the MC33761 can dissipate up to $470 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$. The power dissipated by the MC33761 can be calculated from the following formula:

$$
\text { Ptot }=\left(\mathrm{v}_{\text {in }} \times \mathrm{I}_{\text {gnd }}\left(\mathrm{I}_{\text {out }}\right)\right)+\left(\mathrm{v}_{\text {in }}-\mathrm{v}_{\text {out }}\right) \times \mathrm{I}_{\text {out }}
$$

or

$$
\mathrm{Vin}_{\max }=\frac{\text { Ptot }+\mathrm{V}_{\text {out }} \times \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 80 mA output current is needed, the ground current is extracted from the data-sheet curves: $4.0 \mathrm{~mA} @ 80 \mathrm{~mA}$. For a MC33761SNT1-28 (2.8 V) delivering 80 mA and operating at $25^{\circ} \mathrm{C}$, the maximum input voltage will then be 8.3 V .

## Typical Applications

The following picture portrays the typical application of the MC33761.


Figure 7. A Typical Application Schematic

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. The figure below gives an example of a layout where stray inductances/capacitances are minimized. This layout is the

basis for the MC33761 performance evaluation board. The BNC connectors give the user an easy and quick evaluation mean.

## Understanding the Load Transient Improvement

The MC33761 features a novel architecture which allows the user to easily implement the regulator in burst systems where the time between two current shots is kept very small.

The quality of the transient response time is related to many parameters, among which the closed-loop bandwidth with the corresponding phase margin plays an important role. However, other characteristics also come into play like the series pass transistor saturation. When a current perturbation suddenly appears on the output, e.g. a load increase, the error amplifier reacts and actively biases the PNP transistor. During this reaction time, the LDO is in open-loop and the output impedance is rather high. As a result, the voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place with a positive overshoot. The problem appears when this overshoot decays down to the LDO steady-state value.


Figure 8. A Standard LDO Behavior when the Load Current Disappears


Figure 10. Without Load Transient Improvement

During this decreasing phase, the LDO stops the PNP bias and one can consider the LDO asleep (Figure 8). If by misfortune a current shot appears, the reaction time is incredibly lengthened and a strong undershoot takes place. This reaction is clearly not acceptable for line sensitive devices, such as VCOs or other Radio-Frequency parts. This problem is dramatically exacerbated when the output current drops to zero rather than a few mA. In this later case, the internal feedback network is the only discharge path, accordingly lengthening the output voltage decay period (Figure 9).
The MC33761 cures this problem by implementing a clever design where the LDO detects the presence of the overshoot and forces the system to go back to steady-state as soon as possible, ready for the next shot. Figure 10 and 11 show how it positively improves the response time and decreases the negative peak voltage.


Figure 9. A Standard LDO Behavior when the Load Current Appears in the Decay Zone


Figure 11. MC33761 with Load Transient Improvement

## MC33761

## MC33761 Has a Fast Start-Up Phase

Thanks to the lack of bypass capacitor the MC33761 is able to supply its downstream circuitry as soon as the OFF to ON signal appears. In a standard LDO, the charging time of the external bypass capacitor hampers the response time. A simple solution consists in suppressing this bypass element but, unfortunately, the noise rises to an
unacceptable level. MC33761 offers the best of both worlds since it no longer includes a bypass capacitor and starts in less than $40 \mu$ s typically (Repetitive at 200 Hz ). It also ensures a low-noise level of $40 \mu$ VRMS $100 \mathrm{~Hz}-100 \mathrm{kHz}$. The following picture details the typical 33761 start-up phase.


Figure 12. Repetitive Start-Up Waveforms

TYPICAL TRANSIENT RESPONSES


Figure 13. Output is Pulsed from 2.0 mA to 80 mA


Figure 14. Discharge Effects from 0 to 40 mA


Figure 16. Load Transient Improvement Effect

## MC33761

TYPICAL TRANSIENT RESPONSES


Figure 17. MC33761 Typical Noise Density Performance


Figure 18. MC33761 Typical Ripple Rejection Performance


Figure 19. Typical Output Impedance plot $\mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {out }}+\mathbf{1 . 0}$

## MC33761

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


THIN SOT-23-5

## MC33761

ORDERING INFORMATION

| Device | Voltage Output | Package | Shipping |
| :---: | :---: | :---: | :---: |
| MC33761SNT1-25 | 2.5 V | Thin SOT-23-5 | 3000 Units / Tape \& Reel |
| MC33761SNT1-28 | 2.8 V | Thin SOT-23-5 | 3000 Units / Tape \& Reel |
| MC33761SNT1-30 | 3.0 V | Thin SOT-23-5 | 3000 Units / Tape \& Reel |
| MC33761SNT1-50 | 5.0 V | Thin SOT-23-5 | 3000 Units / Tape \& Reel |

## NCP4561

## Ultra Low-Noise Low Dropout Voltage Regulator with 1.0 V ON/OFF Control

The NCP4561 is a Low DropOut (LDO) regulator featuring excellent noise performances. Thanks to its innovative concept, the circuit reaches an incredible $40 \mu$ VRMS noise level without an external bypass capacitor. Housed in a small SOT-23 5 leads-like package, it represents the ideal designer's choice when space and noise are at premium.

The absence of external bandgap capacitor unleashes the response time to a wake-up signal and makes it stay within $40 \mu$ s (in repetitive mode), pushing the NCP4561 as a natural candidate in portable applications.

The NCP4561 also hosts a novel architecture which prevents excessive undershoots when the regulator is the seat of fast transient bursts, as in any bursting systems.

Finally, with a static line regulation better than -75 dB , it naturally shields the downstream electronics against choppy lines.

## Features

- Ultra Low-Noise: $150 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$ @ $100 \mathrm{~Hz}, 40 \mu$ VRMS $100 \mathrm{~Hz}-$ 100 kHz Typical, Iout $=60 \mathrm{~mA}, \mathrm{C}_{\mathrm{o}}=1.0 \mu \mathrm{~F}$
- Fast Response Time from OFF to ON: $40 \mu \mathrm{~s}$ Typical at a 200 Hz Repetition Rate
- Ready for 1.0 V Platforms: ON with a 900 mV High Level
- Nominal Output Current of 80 mA with a 100 mA Peak Capability
- Typical Dropout of 90 mV @ $30 \mathrm{~mA}, 160 \mathrm{mV}$ @ 80 mA
- Ripple Rejection: 70 dB @ 1.0 kHz
- $1.5 \%$ Output Precision @ $25^{\circ} \mathrm{C}$
- Thermal Shutdown


## Applications

- Noise Sensitive Circuits: VCOs RF Stages, etc.
- Bursting Systems (TDMA Phones)
- All Battery Operated Devices


Figure 1. Simplified Block Diagram


ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


TSOP-5
SN SUFFIX
CASE 483


ORDERING INFORMATION

| Device | Voltge <br> Output $^{\star}$ | Shipping |
| :---: | :---: | :---: |
| NCP4561SNT1-28 | 2.8 V | $3000 /$ Tape \& Reel |

* Contact your ON Semiconductor sales representative for other output voltage values.


## PIN FUNCTION DESCRIPTIONS

| Pin \# | Pin Name | Function | Description |
| :---: | :---: | :--- | :--- |
| 1 | ON/OFF | Shuts or <br> wakes-up the IC | A 900 mV level on this pin is sufficient to start the IC. A 150 mV shuts it down. |
| 2 | GND | The IC's ground |  |
| 3 | NC | None | It makes no arm to connect the pin to a known potential, like in a pin-to-pin <br> replacement case. |
| 4 | $\mathrm{~V}_{\text {out }}$ | Delivers the <br> output voltage | This pin requires a $1.0 \mu \mathrm{~F}$ output capacitor to be stable. |
| 5 | $\mathrm{~V}_{\text {in }}$ | Powers the IC | A positive voltage up to 12 V can be applied upon this pin. |

## MAXIMUM RATINGS

| Rating | Pin \# | Symbol | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |
| Power Supply Voltage | 5 | $V_{\text {in }}$ | - | 12 | V |
| ESD Capability, HBM Model | All Pins |  | - | 1.0 | kV |
| ESD Capability, Machine Model | All Pins |  | - | 200 | V |
| Maximum Power Dissipation NW Suffix, Plastic Package Thermal Resistance Junction-to-Air |  | $\mathrm{P}_{\mathrm{D}}$ <br> $\mathrm{R}_{\theta \mathrm{J}-\mathrm{A}}$ | - | Internally Limited 210 | $\begin{gathered} \mathrm{w} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Ambient Temperature <br> Maximum Junction Temperature (Note 1) <br> Maximum Operating Junction Temperature (Note 2) |  | $\begin{gathered} \hline \mathrm{T}_{\mathrm{A}} \\ \mathrm{~T}_{\mathrm{maxx}^{2}} \mathrm{~T}_{\mathrm{J}} \end{gathered}$ | - | $\begin{gathered} \hline-40 \text { to }+85 \\ 150 \\ 125 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | $\mathrm{T}_{\text {stg }}$ | - | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |

## ELECTRICAL CHARACTERISTICS

(For Typical Values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for Min $/$ Max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, Max $\mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristics | Pin \# | Symbol | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Logic Control Specifications

| Input Voltage Range | 1 | $V_{\text {ON/OFF }}$ | 0 | - | $V_{\text {in }}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| ON/OFF Input Resistance | 1 | $\mathrm{R}_{\text {ON/OFF }}$ | - | 250 | - | $\mathrm{k} \Omega$ |
| ON/OFF Control Voltages (Note 3) | 1 | $\mathrm{~V}_{\text {ON/OFF }}$ |  |  |  | mV |
| Logic Zero, OFF State, $\mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}$ <br> Logic One, ON State, $\mathrm{IO}=50 \mathrm{~mA}$ |  |  | - | - | 150 |  |

## Currents Parameters

| Current Consumption in OFF State <br> OFF Mode Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0, \mathrm{~V}_{\text {OFF }}=150 \mathrm{mV}$ | $\mathrm{IQ}_{\text {OFF }}$ | - | 0.1 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Consumption in ON State ON Mode Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0, \mathrm{~V}_{\mathrm{ON}}=3.5 \mathrm{~V}$ | $\mathrm{IQ}_{\mathrm{ON}}$ | - | 180 | - | $\mu \mathrm{A}$ |
| Current Consumption in ON State, ON Mode Saturation Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}-0.5 \mathrm{~V}$, No Output Load | $\mathrm{IQ}_{\text {SAT }}$ | - | 800 | - | $\mu \mathrm{A}$ |
| Current Limit $\mathrm{V}_{\text {in }}=$ Vout $_{\text {nom }}+1.0 \mathrm{~V}$, <br> Output is brought to Voutnom -0.3 V | $\mathrm{I}_{\text {max }}$ | 100 | 180 | - | mA |

1. Internally Limited by Shutdown.
2. Specifications are guaranteed below this value.
3. Voltage Slope should be Greater than $2.0 \mathrm{mV} / \mu \mathrm{s}$.

## ELECTRICAL CHARACTERISTICS (continued)

(For Typical Values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for Min/Max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, Max $\mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristics | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## Output Voltages

| $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<80 \mathrm{~mA}$ | 4 | $\mathrm{~V}_{\text {out }}$ | 2.758 | 2.8 | 2.842 | V |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<80 \mathrm{~mA}$ | 4 | $\mathrm{~V}_{\text {out }}$ | 2.716 | 2.8 | 2.884 | V |

Line and Load Regulation, Dropout Voltages

| Line Regulation $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<12 \mathrm{~V}, \mathrm{I}_{\text {out }}=80 \mathrm{~mA}$ | 4/5 | Regline | - | - | 20 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Load Regulation $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, C_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=1.0 \text { to } 80 \mathrm{~mA}$ | 4 | Regload | - | - | 40 | mV |
| $\begin{aligned} & \text { Dropout Voltage (Note 4) } \\ & I_{\text {out }}=30 \mathrm{~mA} \\ & I_{\text {out }}=60 \mathrm{~mA} \\ & I_{\text {out }}=80 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4 \\ & 4 \\ & 4 \end{aligned}$ | $\begin{aligned} & V_{\text {in }}-V_{\text {out }} \\ & V_{\text {in }}-V_{\text {out }} \\ & V_{\text {in }}-V_{\text {out }} \end{aligned}$ | - | $\begin{gathered} 90 \\ 140 \\ 160 \end{gathered}$ | $\begin{aligned} & 150 \\ & 200 \\ & 250 \end{aligned}$ | mV |

## Dynamic Parameters

| Ripple Rejection <br> $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}+1.0 \mathrm{kHz} 100 \mathrm{mVpp}$ Sinusoidal Signal | 4/5 | Ripple | - | -70 | - | dB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Noise Density @ 1.0 kHz | 4 |  | - | 150 | - | $\begin{aligned} & \mathrm{nV} / \\ & \sqrt{\mathrm{Hz}} \end{aligned}$ |
| RMS Output Noise Voltage $C_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=50 \mathrm{~mA}, \mathrm{~F}=100 \mathrm{~Hz} \text { to } 1.0 \mathrm{MHz}$ | 4 | Noise | - | 35 | - | $\mu \mathrm{V}$ |
| Output Rise Time <br> $C_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=50 \mathrm{~mA}, 10 \%$ of Rising ON Signal to $90 \%$ of Nominal $\mathrm{V}_{\text {out }}$ | 4 | $\mathrm{t}_{\text {rise }}$ | - | 40 | - | $\mu \mathrm{S}$ |

Thermal Shutdown

| Thermal Shutdown |  |  | - | - | 125 |
| :--- | :--- | :--- | :--- | :--- | :--- |

4. $\mathrm{V}_{\text {out }}$ is brought to $\mathrm{V}_{\text {out }}-100 \mathrm{mV}$.

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant chip temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential value). The dropout level is affected by the chip temperature, load current and minimum input supply requirements.

## Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output current are kept constant during the measurement. Results are expressed in $\mu$ VRMS.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specs.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected. One usually distinguishes static line regulation or DC line regulation (a DC step in the input voltage generates a corresponding step in the output voltage) from ripple rejection or audio susceptibility where the input is combined with a frequency generator to sweep from a few hertz up to a defined boundary while the output amplitude is monitored.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $125^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package power dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient temperature, it is possible to calculate the maximum power dissipation and thus the maximum available output current.

TYPICAL CHARACTERISTICS


Figure 2. Ground Current vs. Output Current


Figure 3. Quiescent Current vs. Temperature


Figure 4. Dropout vs. Output Current


Figure 6. Dropout Voltage vs. Temperature


Figure 5. Output Voltage vs. Output Current


Figure 7. Typical Noise Density Performance

POWER SUPPLY REJECTION RATIO


Figure 8. Typical Ripple Rejection Performance ( $\mathrm{I}_{\text {load }}=10 \mathrm{~mA}$ )


Figure 9. Typical Ripple Rejection Performance ( $\mathrm{I}_{\text {load }}=60 \mathrm{~mA}$ )

## APPLICATION HINTS

## Input Decoupling

As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP4561 package. Higher values will correspondingly improve the overall line transient response.

## Output Decoupling

Thanks to a novel concept, the NCP4561 is a stable component and does not require any specific Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

## Noise Decoupling

Unlike other LDOs, the NCP4561 is a true low-noise regulator. Without the need of an external bypass capacitor, it typically reaches the incredible level of $40 \mu$ VRMS overall noise between 100 Hz and 100 kHz . To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics. The classical bypass capacitor impacts the start-up phase of standard LDOs. However, thanks to its low-noise architecture, the NCP4561 operates without a bypass element and thus offers a typical $40 \mu \mathrm{~s}$ start-up phase.

## Protections

The NCP4561 hosts several protections, giving natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a maximum value of 180 mA typical while temperature shutdown occurs if the die heats up beyond $125^{\circ} \mathrm{C}$. These values let you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.
The maximum dissipation the package can handle is given by:

$$
P_{\max }=\frac{T_{J \max }-T_{A}}{R_{\theta J A}}
$$

If $\mathrm{T}_{\mathrm{Jmax}}$ is limited to $125^{\circ} \mathrm{C}$, then the NCP4561 can dissipate up to $470 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$. The power dissipated by the NCP4561 can be calculated from the following formula:

$$
\text { Ptot }=\left(v_{\text {in }} \times I_{\text {gnd }}\left(I_{\text {out }}\right)\right)+\left(v_{\text {in }}-v_{\text {out }}\right) \times I_{\text {out }}
$$

or

$$
\operatorname{Vin}_{\max }=\frac{\text { Ptot }+\mathrm{V}_{\text {out }} \times I_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 80 mA output current is needed, the ground current is extracted from the data-sheet curves: $4.0 \mathrm{~mA} @ 80 \mathrm{~mA}$. For a NCP4561SNT1-28 (2.8 V) delivering 80 mA and operating at $25^{\circ} \mathrm{C}$, the maximum input voltage will then be 8.3 V .

## Typical Applications

The following figure portrays the typical application of the NCP4561.


Figure 10. A Typical Application Schematic

## PCB Layout Considerations

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. The figure below gives an example of a layout where stray

inductances/capacitances are minimized. This layout is the basis for the NCP4561 performance evaluation board. The BNC connectors give the user an easy and quick evaluation mean.


Figure 11. PCB Layout

## Understanding the Load Transient Improvement

The NCP4561 features a novel architecture which allows the user to easily implement the regulator in burst systems where the time between two current shots is kept very small.

The quality of the transient response time is related to many parameters, among which the closed-loop bandwidth with the corresponding phase margin plays an important role. However, other characteristics also come into play like the series pass transistor saturation. When a current perturbation suddenly appears on the output, e.g. a load increase, the error amplifier reacts and actively biases the PNP transistor. During this reaction time, the LDO is in open-loop and the output impedance is rather high. As a result, the voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place with a positive overshoot. The problem appears when this overshoot decays down to the LDO steady-state value.

During this decreasing phase, the LDO stops the PNP bias and one can consider the LDO asleep. If by misfortune a current shot appears, the reaction time is incredibly lengthened and a strong undershoot takes place. This reaction is clearly not acceptable for line sensitive devices, such as VCOs or other Radio-Frequency parts. This problem is dramatically exacerbated when the output current drops to zero rather than a few mA. In this later case, the internal feedback network is the only discharge path, accordingly lengthening the output voltage decay period.
The NCP4561 cures this problem by implementing a clever design where the LDO detects the presence of the overshoot and forces the system to go back to steady-state as soon as possible, ready for the next shot, which positively improves the response time and decreases the negative peak voltage.

## NCP4561 has a fast start-up phase

Thanks to the lack of bypass capacitor the NCP4561 is able to supply its downstream circuitry as soon as the OFF to ON signal appears. In a standard LDO, the charging time of the external bypass capacitor hampers the response time. A simple solution consists in suppressing this bypass element but, unfortunately, the noise rises to an
unacceptable level. NCP4561 offers the best of both worlds since it no longer includes a bypass capacitor and starts in less than $40 \mu$ s typically (Repetitive at 200 Hz ). It also ensures a low-noise level of $40 \mu \mathrm{VRMS} 100 \mathrm{~Hz}-100 \mathrm{kHz}$. The following picture details the typical NCP4561 startup phase.


Figure 12. Start-Up Waveform

TYPICAL TRANSIENT RESPONSES


Figure 13. Load Current is Pulsed from 0 to 40 mA


Figure 14. Load Current is Pulsed from 0 to 80 mA

## TYPICAL TRANSIENT RESPONSES



Figure 15. Load Current is Switched from 40 to 0 mA


Figure 16. Load Current is Switched from 80 to 0 mA

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

(TSOP-5 is footprint compatible with SOT23-5)

ORDERING INFORMATION

| Device | Voltage Output* | Package | Shipping |
| :---: | :---: | :---: | :---: |
| NCP4561SNT1-28 | 2.8 V | TSOP-5 | 3000 Units /Tape \& Reel |

[^7]
## NCP502

## 80 mA CMOS Low Iq Voltage Regulator in an SC70-5

The NCP502 series of fixed output linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP502 series features an ultra-low quiescent current of $40 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP502 has been designed to be used with low cost ceramic capacitors. The device is housed in the micro-miniature SC70-5 surface mount package. Standard voltage versions are $1.5,1.8,2.5$, $2.7,2.8,3.0,3.3$, and 5.0 V . Other voltages are available in 100 mV steps.

## Features

- Low Quiescent Current of $40 \mu \mathrm{~A}$ Typical
- Excellent Line and Load Regulation
- Low Output Voltage Option
- Output Voltage Accuracy of $2.0 \%$
- Industrial Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Cellular Phones
- Battery Powered Consumer Products
- Hand-Held Instruments
- Camcorders and Cameras


ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com
MARKING
DIAGRAM

| SC-88A/SOT-353/SC70-5 |
| :--- |
| DF SUFFIX |
| CASE 419A |


| XXX |
| :--- |
| = Specific Device Code |
| $=$ |

$=$ Date Code

## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 287 of this data sheet.

NCP502

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | Gnd | Power supply ground. |
| 2 | Vin | Positive power supply input voltage. |
| 3 | Vout | Regulated output voltage. |
| 4 | N/C | No internal connection. |
| 5 | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the device is <br> disabled. If this function is not used, Enable should be connected to Vin. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $V_{\text {in }}$ | 12 | V |
| Enable Voltage | Enable | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Voltage | $V_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Power Dissipation and Thermal Characteristics <br> Power Dissipation <br> Thermal Resistance, Junction to Ambient | $P_{D}$ $\mathrm{R}_{\theta \mathrm{JA}}$ | Internally Limited 400 | $\begin{gathered} \text { W } \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\text {A }}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ | $\mathrm{T}_{\text {solder }}$ | 10 | sec |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{~mA} \mathrm{DC}$ with trigger voltage.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom. })}+2.0 \mathrm{~V}, \mathrm{~V}_{\text {enable }}=\mathrm{V}_{\text {in }}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right) \mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}($ nom. $)+1.0 \mathrm{~V}$ 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.646 \\ & 2.744 \\ & 2.94 \\ & 3.234 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.754 \\ & 2.856 \\ & 3.06 \\ & 3.366 \\ & 5.100 \end{aligned}$ | V |
| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right) \mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }} \text { (nom.) } \\ & +1.0 \mathrm{~V} \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.619 \\ & 2.716 \\ & 2.910 \\ & 3.201 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.781 \\ & 2.884 \\ & 3.09 \\ & 3.399 \\ & 5.100 \end{aligned}$ | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$ to $12 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ ) | Regline | - | 0.4 | 3.0 | $\mathrm{mV} / \mathrm{V}$ |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 80 mA ) | Regload | - | 0.2 | 0.8 | $\mathrm{mV} / \mathrm{mA}$ |
| Output Current | $\mathrm{I}_{0 \text { (nom.) }}$ | 80 | - | - | mA |
| ```Dropout Voltage \(\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.\) to \(85^{\circ} \mathrm{C}\), \(\mathrm{I}_{\text {out }}=80 \mathrm{~mA}\), Measured at \(V_{\text {out }}-3.0 \%\) ) \(1.5 \mathrm{~V}-1.7 \mathrm{~V}\) \(1.8 \mathrm{~V}-2.4 \mathrm{~V}\) \(2.5 \mathrm{~V}-2.6 \mathrm{~V}\) \(2.7 \mathrm{~V}-2.9 \mathrm{~V}\) \(3.0 \mathrm{~V}-4.9 \mathrm{~V}\) 5.0 V``` | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{aligned} & 1500 \\ & 1300 \\ & 1000 \\ & 850 \\ & 850 \\ & 600 \end{aligned}$ | $\begin{gathered} 1900 \\ 1700 \\ 1400 \\ 1300 \\ 1200 \\ 900 \end{gathered}$ | mV |
| Quiescent Current <br> (Enable Input $=0 \mathrm{~V}$ ) <br> (Enable Input $=\mathrm{V}_{\text {in }}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to $\left.\mathrm{I}_{\mathrm{o}(\text { nom. } .)}\right)$ | ${ }^{\text {Q }}$ | - | $\begin{aligned} & 0.1 \\ & 40 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 90 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 90 | 200 | 500 | mA |
| Ripple Rejection ( $\mathrm{f}=1.0 \mathrm{kHz}, 15 \mathrm{~mA}$ ) | RR | - | 55 | - | dB |
| Output Voltage Noise ( $\mathrm{f}=100 \mathrm{~Hz}$ to 100 kHz ) | $\mathrm{V}_{\mathrm{n}}$ | - | 180 | - | $\mu \mathrm{Vrms}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(en) }}$ | $1.3$ | - | $\overline{0.3}$ | V |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | 100 | - | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\Theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

NCP502


Figure 2. Quiescent Current versus Input Voltage


Figure 3. Quiescent Current versus Temperature


Figure 4. Line Transient Response


Figure 6. Load Transient Response


Figure 7. Ripple Rejection/Frequency

NCP502


Figure 8. Output Voltage versus Temperature


Figure 9. Output Voltage versus Input Voltage


Figure 10. Dropout Voltage versus Temperature

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.

## APPLICATIONS INFORMATION

A typical application circuit for the NCP502 series is shown in Figure 1, front page.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP502 package. Higher values and lower ESR will improve the overall line transient response. If large line or load transients are not expected, then it is possible to operate the regulator without the use of a capaitor.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

## Output Decoupling (C2)

The NCP502 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. If load transients are not to be expected, then it is possible for the regulator to operate with no output capacitor. Otherwise, capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $5.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

## Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to $\mathrm{V}_{\mathrm{in}}$.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Thermal

As power across the NCP502 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP502 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP502 can dissipate up to $250 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$.

The power dissipated by the NCP502 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} l_{\text {gnd }}\left(I_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right] * l_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If an 80 mA output current is needed then the ground current from the data sheet is $40 \mu \mathrm{~A}$. For an NCP502 (3.0 V), the maximum input voltage will then be 6.12 V .

## NCP502

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


SC70-5
(SC-88A/SOT-353)

## NCP502

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP502SQ15T1 | 1.5 | LCC |  |  |
| NCP502SQ18T1 | 1.8 | LCD |  |  |
| NCP502SQ25T1 | 2.5 | LCE |  | 3000 Units/ |
| NCP502SQ27T1 | 2.7 | LCF | SC70-5 | (" Tape \& Reel |
| NCP502SQ28T1 | 2.8 | LCG |  |  |
| NCP502SQ30T1 | 3.0 | LCH |  |  |
| NCP502SQ33T1 | 3.3 | LCI |  |  |
| NCP502SQ50T1 | 5.0 | LCJ |  |  |

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## NCP512

## Product Preview 80 mA CMOS Low Iq Voltage Regulator in an SC70-5

The NCP512 series of fixed output linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP512 series features an ultra-low quiescent current of $40 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP512 has been designed to be used with low cost ceramic capacitors. The device is housed in the micro-miniature SC70-5 surface mount package. Standard voltage versions are $1.5,1.8,2.5$, $2.7,2.8,3.0,3.3$, and 5.0 V . Other voltages are available in 100 mV steps.

## Features

- Low Quiescent Current of $40 \mu \mathrm{~A}$ Typical
- Low Dropout Voltage of 250 mV at 80 mA
- Excellent Line and Load Regulation
- Low Output Voltage Option
- Output Voltage Accuracy of $2.0 \%$
- Industrial Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Cellular Phones
- Battery Powered Consumer Products
- Hand-Held Instruments
- Camcorders and Cameras


This device contains \# active transistors
Figure 1. Typical Application Diagram

NCP512

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | Gnd | Power supply ground. |
| 2 | Vin | Positive power supply input voltage. |
| 3 | Vout | Regulated output voltage. |
| 4 | N/C | No internal connection. |
| 5 | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the device is <br> disabled. If this function is not used, Enable should be connected to Vin. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $V_{\text {in }}$ | 0 to 6.0 | V |
| Enable Voltage | Enable | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Voltage | $V_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Power Dissipation and Thermal Characteristics <br> Power Dissipation <br> Thermal Resistance, Junction to Ambient | $P_{D}$ $\mathrm{R}_{\theta \mathrm{JA}}$ | Internally Limited - | $\begin{gathered} \text { W } \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\text {A }}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ | $\mathrm{T}_{\text {solder }}$ | 10 | sec |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{~mA} \mathrm{DC}$ with trigger voltage.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom. })}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {enable }}=\mathrm{V}_{\text {in }}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.646 \\ & 2.744 \\ & 2.94 \\ & 3.234 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.754 \\ & 2.856 \\ & 3.06 \\ & 3.366 \\ & 5.100 \end{aligned}$ | V |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $\left.85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.619 \\ & 2.716 \\ & 2.910 \\ & 3.201 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.781 \\ & 2.884 \\ & 3.09 \\ & 3.399 \\ & 5.100 \end{aligned}$ | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$ to 6.0 V , $\left.\mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ | Regline | - | 1.0 | 3.0 | $\mathrm{mV} / \mathrm{V}$ |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 80 mA ) | Regload | - | 0.3 | 0.8 | $\mathrm{mV} / \mathrm{mA}$ |
| Output Current $\begin{aligned} & 1.5 \mathrm{~V}, 1.8 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=4.0 \mathrm{~V}\right) \\ & 2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right) \\ & 3.3 \mathrm{~V},\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \\ & 5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{0 \text { (nom.) }}$ | $\begin{aligned} & 80 \\ & 80 \\ & 80 \\ & 80 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \\ & 200 \\ & 200 \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | mA |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $85^{\circ} \mathrm{C}$, $\mathrm{I}_{\text {out }}=80 \mathrm{~mA}$, Measured at $V_{\text {out }}-3.0 \%$ ) <br> 1.5 V <br> 1.8 V <br> 2.5 V <br> 2.7 V <br> 2.8 V <br> 3.0 V <br> 3.3 V <br> 5.0 V | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{aligned} & 450 \\ & 350 \\ & 220 \\ & 200 \\ & 200 \\ & 180 \\ & 160 \\ & 120 \end{aligned}$ | $\begin{aligned} & 550 \\ & 450 \\ & 300 \\ & 300 \\ & 300 \\ & 300 \\ & 300 \\ & 300 \end{aligned}$ | mV |
| Quiescent Current <br> (Enable Input = 0 V) <br> (Enable Input $=\mathrm{V}_{\text {in }}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to $\left.\mathrm{I}_{\mathrm{o}(\text { nom. })}\right)$ | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.1 \\ & 40 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 90 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Short Circuit Current $\begin{aligned} & 1.5 \mathrm{~V}, 1.8 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=4.0 \mathrm{~V}\right) \\ & 2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right) \\ & 3.3 \mathrm{~V},\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \\ & 5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {out(max) }}$ | $\begin{aligned} & \text { TBD } \\ & \text { TBD } \\ & \text { TBD } \\ & \text { TBD } \end{aligned}$ | $\begin{aligned} & 150 \\ & 150 \\ & 150 \\ & 150 \end{aligned}$ | $\begin{aligned} & 400 \\ & 400 \\ & 400 \\ & 400 \end{aligned}$ | mA |
| Output Voltage Noise ( $\mathrm{f}=100 \mathrm{~Hz}$ to 100 kHz ) | $\mathrm{V}_{\mathrm{n}}$ | - | 180 | - | $\mu \mathrm{Vrms}$ |
| Ripple Rejection ( $\mathrm{f}=1.0 \mathrm{kHz}, 60 \mathrm{~mA}$ ) | RR | - | 50 | - | dB |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(en) }}$ | $1.3$ | - | $\begin{gathered} - \\ 0.3 \end{gathered}$ | V |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm/ ${ }^{\circ} \mathrm{C}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\Theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.

## APPLICATIONS INFORMATION

A typical application circuit for the NCP512 series is shown in Figure 1, front page.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP512 package. Higher values and lower ESR will improve the overall line transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

## Output Decoupling (C2)

The NCP512 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

## Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to $\mathrm{V}_{\mathrm{in}}$.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Thermal

As power across the NCP512 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP512 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP512 can dissipate up to xxx mW @ $25^{\circ} \mathrm{C}$.

The power dissipated by the NCP512 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} I_{\text {gnd }}\left(I_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right]^{*} l_{\text {out }}
$$

or

$$
V_{\text {inMAX }}=\frac{P_{\text {tot }}+V_{\text {out }}{ }^{*} I_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If an 80 mA output current is needed then the ground current from the data sheet is $40 \mu \mathrm{~A}$. For an NCP512 (3.0 V), the maximum input voltage will then be $x x \mathrm{~V}$.

## NCP512

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

## NCP512

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP512 | 1.5 | $x x x$ |  |  |
| NCP512 | 1.8 | $x x x$ |  |  |
| NCP512 | 2.5 | $x x x$ |  |  |
| NCP512 | 2.7 | $x x x$ | SC70-5 | xxxx Units/ |
| NCP512 | 2.8 | xxx |  |  |
| NCP512 | 3.0 | Rxx |  |  |
| NCP512 | 3.3 | xxx |  |  |
| NCP512 | 5.0 |  |  |  |

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## NCP552

## 80 mA CMOS Low Iq NOCAP ${ }^{T M}$ Voltage Regulator

The NCP552 series of fixed output NOCAP linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP552 series features an ultra-low quiescent current of $2.8 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP552 has been designed to be used with low cost ceramic capacitors. This device has the ability to operate without an output capacitor. The device is housed in the micro-miniature SC82-AB surface mount package. Standard voltage versions are $1.5,1.8,2.5$, $2.7,2.8,3.0,3.3$, and 5.0 V . Other voltages are available in 100 mV steps.

## Features

- Low Quiescent Current of $2.8 \mu \mathrm{~A}$ Typical
- Low Output Voltage Option
- Output Voltage Accuracy of $2.0 \%$
- Industrial Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Battery Powered Consumer Products
- Hand-Held Instruments
- Camcorders and Cameras


This device contains 32 active transistors

Figure 1. Typical Application Diagram

## (a)

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SC82-AB (SC70-4)
SQ SUFFIX
CASE 419C

PIN CONNECTIONS AND
MARKING DIAGRAM

(Top View)

$$
\begin{array}{ll}
\text { xxx } & =\text { Device Code } \\
\text { M } & =\text { Date Code }
\end{array}
$$

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 303 of this data sheet.

NCP552

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | Gnd | Power supply ground. |
| 2 | Vin | Positive power supply input voltage. |
| 3 | Vout | Regulated output voltage. |
| 4 | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the device is <br> disabled. If this function is not used, Enable should be connected to Vin. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {in }}$ | 12 | V |
| Enable Voltage | Enable | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Voltage | $\mathrm{V}_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| $\begin{array}{l}\text { Power Dissipation and Thermal Characteristics } \\ \text { Power Dissipation } \\ \text { Thermal Resistance, Junction to Ambient }\end{array}$ | $\mathrm{P}_{\mathrm{D}}$ |  | Internally Limited |
| 400 |  |  |  |$]$| W |
| :---: |
| Operating Junction Temperature |
| Operating Ambient Temperature |
| Storage Temperature |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 200 \mathrm{~mA} \mathrm{DC}$ with trigger voltage.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom. })}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {enable }}=\mathrm{V}_{\text {in }}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.646 \\ & 2.744 \\ & 2.94 \\ & 3.234 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.754 \\ & 2.856 \\ & 3.06 \\ & 3.366 \\ & 5.100 \end{aligned}$ | V |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $\left.85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.619 \\ & 2.716 \\ & 2.910 \\ & 3.201 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.781 \\ & 2.884 \\ & 3.09 \\ & 3.399 \\ & 5.100 \end{aligned}$ | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$ to $\left.12 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ | Regline | - | 2.0 | 4.5 | $\mathrm{mV} / \mathrm{V}$ |
| Load Regulation ( $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to $80 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}$ ) | Regload | - | 0.3 | 0.8 | $\mathrm{mV} / \mathrm{mA}$ |
| $\begin{aligned} & \text { Output Current }\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}\right) \\ & 1.5 \mathrm{~V}, 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V}, \\ & 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{I}_{0}$ (nom.) | $\begin{aligned} & 80 \\ & 80 \\ & 80 \\ & 80 \end{aligned}$ | $\begin{aligned} & 180 \\ & 180 \\ & 180 \\ & 180 \end{aligned}$ | - | mA |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $85^{\circ} \mathrm{C}$, $\mathrm{I}_{\text {out }}=80 \mathrm{~mA}$, Measured at $\begin{aligned} & \left.V_{\text {out }}-3.0 \%\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{aligned} & 1300 \\ & 1100 \\ & 800 \\ & 750 \\ & 730 \\ & 680 \\ & 650 \\ & 470 \end{aligned}$ | $\begin{aligned} & 1800 \\ & 1600 \\ & 1400 \\ & 1200 \\ & 1200 \\ & 1000 \\ & 1000 \\ & 1000 \end{aligned}$ | mV |
| Quiescent Current <br> (Enable Input $=0 \mathrm{~V}$ ) <br> (Enable Input $=\mathrm{V}_{\text {in }}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to $\mathrm{I}_{\mathrm{o} \text { (nom.) }}, \mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.1 \\ & 2.8 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 6.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| ```Output Short Circuit Current ( \(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}\) ) \(1.5 \mathrm{~V}, 1.8 \mathrm{~V}\) \(2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}\) 3.3 V , 5.0 V``` | $\mathrm{I}_{\text {out(max) }}$ | $\begin{aligned} & 100 \\ & 100 \\ & 100 \\ & 100 \end{aligned}$ | $\begin{aligned} & 230 \\ & 300 \\ & 300 \\ & 300 \end{aligned}$ | $\begin{aligned} & 450 \\ & 450 \\ & 450 \\ & 450 \end{aligned}$ | mA |
| Output Voltage Noise ( $\mathrm{f}=20 \mathrm{~Hz}$ to 100 kHz , $\mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ ) ( $\mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 90 | - | $\mu \mathrm{Vrms}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(en) }}$ | $1.3$ | - | $\overline{0.3}$ | V |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | $\mathrm{ppm} /{ }^{\circ} \mathrm{C}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.


Figure 2. Dropout Voltage versus Temperature


Figure 3. Output Voltage versus Temperature


Figure 4. Quiescent Current versus Temperature


Figure 5. Quiescent Current versus Input Voltage


Figure 6. Output Noise Density


Figure 7. Line Transient Response

## NCP552



Figure 8. Load Transient Response


Figure 10. Turn-On Response


Figure 11. Output Voltage versus Input Voltage

## APPLICATIONS INFORMATION

A typical application circuit for the NCP552 series is shown in Figure 1, front page.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP552 package. Higher values and lower ESR will improve the overall line transient response. If large line or load transients are not expected, then it is possible to operate the regulator without the use of a capacitor.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

## Output Decoupling (C2)

The NCP552 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. If load transients are not to be expected, then it is possible for the regulator to operate with no output capacitor. Otherwise, capacitors exhibiting ESRs ranging from a few $m \Omega$ up to $10 \Omega$ can thus safely be used. The minimum decoupling value is $0.1 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

## Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to $\mathrm{V}_{\mathrm{in}}$.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Thermal

As power across the NCP552 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP552 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP552 can dissipate up to $250 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$.

The power dissipated by the NCP552 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }} * I_{\text {gnd }}\left(l_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right]^{*} l_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If an 80 mA output current is needed then the ground current from the data sheet is $2.8 \mu \mathrm{~A}$. For an NCP552 (3.0 V), the maximum input voltage will then be 6.12 V .

## INFORMATION FOR USING THE SC-82AB SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


NCP552

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP552SQ15T1 | 1.5 | LAW |  |  |
| NCP552SQ18T1 | 1.8 | LAX |  |  |
| NCP552SQ25T1 | 2.5 | LAY |  |  |
| NCP552SQ27T1 | 2.7 | LAZ | SC82-AB | 3000 Units/ |
| NCP552SQ28T1 | 2.8 | LBA | (SC70-4) | Rape Reel |
| NCP552SQ30T1 | 3.0 | LBB |  |  |
| NCP552SQ33T1 | 3.3 | LBD |  |  |
| NCP552SQ50T1 | 5.0 |  |  |  |

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## NCP553

## 80 mA CMOS Low Iq NOCAP ${ }^{\text {TM }}$ Voltage Regulator

The NCP553 series of fixed output NOCAP linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP553 series features an ultra-low quiescent current of $2.8 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP553 has been designed to be used with low cost ceramic capacitors. This device has the ability to operate without an output capacitor. The device is housed in the micro-miniature SC82-AB surface mount package. Standard voltage versions are $1.5,1.8,2.5$, $2.7,2.8,3.0,3.3$, and 5.0 V . Other voltages are available in 100 mV steps.

## Features

- Low Quiescent Current of $2.8 \mu \mathrm{~A}$ Typical
- Low Output Voltage Option
- Output Voltage Accuracy of $2.0 \%$
- Industrial Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Battery Powered Consumer Products
- Hand-Held Instruments
- Camcorders and Cameras


This device contains 32 active transistors

Figure 1. Typical Application Diagram


ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SC82-AB (SC70-4)
SQ SUFFIX
CASE 419C

PIN CONNECTIONS AND
MARKING DIAGRAM

(Top View)

$$
\begin{array}{ll}
\text { xxx } & =\text { Device Code } \\
\text { M } & =\text { Date Code }
\end{array}
$$

See detailed ordering and shipping information in the package dimensions section on page 312 of this data sheet.

NCP553

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name |  |
| :---: | :---: | :--- |
| 1 | Gnd | Power supply ground. |
| 2 | Vin | Positive power supply input voltage. |
| 3 | Vout | Regulated output voltage. |
| 4 | N/C | No internal connection. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {in }}$ | 12 | V |
| Output Voltage | $\mathrm{V}_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Power Dissipation and Thermal Characteristics <br> Power Dissipation <br> Thermal Resistance, Junction to Ambient | $\mathrm{P}_{\mathrm{D}}$ |  |  |
| Operating Junction Temperature | $\mathrm{R}_{\theta \mathrm{JA}}$ | Internally Limited |  |
| 400 |  |  |  |$\quad$| W |
| :---: |
| ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Ambient Temperature |
| Storage Temperature |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per MIL-STD-883, Method 3015 Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 200 \mathrm{~mA} D \mathrm{DC}$ with trigger voltage.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom.) }}+1.0 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.646 \\ & 2.744 \\ & 2.94 \\ & 3.234 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.754 \\ & 2.856 \\ & 3.06 \\ & 3.366 \\ & 5.100 \end{aligned}$ | V |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $\left.85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.619 \\ & 2.716 \\ & 2.910 \\ & 3.201 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.781 \\ & 2.884 \\ & 3.09 \\ & 3.399 \\ & 5.100 \end{aligned}$ | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$ to $\left.12 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ | Regline | - | 2.0 | 4.5 | $\mathrm{mV} / \mathrm{V}$ |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to $80 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}$ ) | Regload | - | 0.3 | 0.8 | $\mathrm{mV} / \mathrm{mA}$ |
| $\begin{aligned} & \text { Output Current }\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}\right) \\ & 1.5 \mathrm{~V}, 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V}, \\ & 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{I}_{0}$ (nom.) | $\begin{aligned} & 80 \\ & 80 \\ & 80 \\ & 80 \end{aligned}$ | $\begin{aligned} & 180 \\ & 180 \\ & 180 \\ & 180 \end{aligned}$ | - | mA |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $85^{\circ} \mathrm{C}$, $\mathrm{I}_{\text {out }}=80 \mathrm{~mA}$, Measured at $\begin{aligned} & \left.V_{\text {out }}-3.0 \%\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | - - - - - - - - | $\begin{aligned} & 1300 \\ & 1100 \\ & 800 \\ & 750 \\ & 730 \\ & 680 \\ & 650 \\ & 470 \end{aligned}$ | $\begin{aligned} & 1800 \\ & 1600 \\ & 1400 \\ & 1200 \\ & 1200 \\ & 1000 \\ & 1000 \\ & 1000 \end{aligned}$ | mV |
| Quiescent Current ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to $\mathrm{I}_{\text {(nom.) }}, \mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{Q}}$ | - | 2.8 | 6.0 | $\mu \mathrm{A}$ |
| ```Output Short Circuit Current ( \(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+2.0 \mathrm{~V}\) ) \(1.5 \mathrm{~V}, 1.8 \mathrm{~V}\) \(2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}\) 3.3 V , 5.0 V``` | $\mathrm{I}_{\text {out(max) }}$ | $\begin{aligned} & 100 \\ & 100 \\ & 100 \\ & 100 \end{aligned}$ | $\begin{aligned} & 230 \\ & 300 \\ & 300 \\ & 300 \end{aligned}$ | $\begin{aligned} & 450 \\ & 450 \\ & 450 \\ & 450 \end{aligned}$ | mA |
| Output Voltage Noise ( $\mathrm{f}=100 \mathrm{~Hz}$ to $100 \mathrm{kHz}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ ) $C_{\text {out }}=1 \mu \mathrm{~F}$ | $\mathrm{V}_{\mathrm{n}}$ | - | 90 | - | $\mu \mathrm{Vrms}$ |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm $/{ }^{\circ} \mathrm{C}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.


Figure 2. Dropout Voltage vs. Temperature


Figure 4. Quiescent Current vs. Temperature


Figure 3. Output Voltage vs. Temperature


Figure 5. Quiescent Current vs. Input Voltage


Figure 6. Output Noise Density


Figure 7. Line Transient Response

## NCP553



Figure 8. Load Transient Response


Figure 9. Load Transient Response


Figure 10. Output Voltage vs. Input Voltage

## APPLICATIONS INFORMATION

A typical application circuit for the NCP553 series is shown in Figure 1, front page.

## Input Decoupling (C1)

A $0.1 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP553 package. Higher values and lower ESR will improve the overall line transient response. If large line or load transients are not expected, then it is possible to operate the regulator without the use of a capacitor.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

## Output Decoupling (C2)

The NCP553 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. If load transients are not to be expected, then it is possible for the regulator to operate with no output capacitor. Otherwise, capacitors exhibiting ESRs ranging from a few $m \Omega$ up to $10 \Omega$ can thus safely be used. The minimum decoupling value is $0.1 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Thermal

As power across the NCP553 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP553 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP553 can dissipate up to $250 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$.

The power dissipated by the NCP553 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} l_{\text {gnd }}\left(I_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right] * l_{\text {out }}
$$

or

$$
V_{\text {inMAX }}=\frac{P_{\text {tot }}+V_{\text {out }}{ }^{*} I_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If an 80 mA output current is needed then the ground current from the data sheet is $2.8 \mu \mathrm{~A}$. For an NCP553 $(3.0 \mathrm{~V})$, the maximum input voltage will then be 6.12 V .

## INFORMATION FOR USING THE SC-82AB SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


NCP553

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP553SQ15T1 | 1.5 | LBE |  |  |
| NCP553SQ18T1 | 1.8 | LBF |  |  |
| NCP553SQ25T1 | 2.5 | LBG |  |  |
| NCP553SQ27T1 | 2.7 | LBH | SC82-AB | 3000 Units/ |
| NCP53SSQ28T1 | 2.8 | LBI | (SC70-4) | $8^{\prime \prime}$ Tape \& Reel |
| NCP553SQ30T1 | 3.0 | LBJ |  |  |
| NCP553SQ33T1 | 3.3 | LBK |  |  |
| NCP553SQ50T1 | 5.0 | LBL |  |  |

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## NCP562

## 80 mA CMOS Low Iq Low-Dropout Voltage Regulator

The NCP562 series of fixed output low-dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP562 series features an ultra-low quiescent current of $2.5 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP562 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of $0.1 \mu \mathrm{~F}$. The device is housed in the micro-miniature $\mathrm{SC} 82-\mathrm{AB}$ surface mount package. Standard voltage versions are $1.5,1.8,2.5,2.7,2.8,3.0,3.3$, and 5.0 V .

## Features

- Low Quiescent Current of $2.5 \mu \mathrm{~A}$ Typical
- Low Output Voltage Option
- Output Voltage Accuracy of $2.0 \%$
- Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Battery Powered Instruments
- Hand-Held Instruments
- Camcorders and Cameras


This device contains 28 active transistors

Figure 1. Representative Block Diagram


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 320 of this data sheet.

NCP562

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | Gnd | Power supply ground. |
| 2 | Vin | Positive power supply input voltage. |
| 3 | Vout | Regulated output voltage. |
| 4 | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the device is <br> disabled. If this function is not used, Enable should be connected to Vin. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {in }}$ | 6.0 | V |
| Enable Voltage | Enable | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Voltage | $\mathrm{V}_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| $\begin{array}{l}\text { Power Dissipation and Thermal Characteristics } \\ \text { Power Dissipation } \\ \text { Thermal Resistance, Junction to Ambient }\end{array}$ | $\mathrm{P}_{\mathrm{D}}$ |  | Internally Limited |
| 400 |  |  |  |$]$| W |
| :---: |
| Operating Junction Temperature |
| Operating Ambient Temperature |
| Storage Temperature |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{~mA} \mathrm{DC}$ with trigger voltage.

## ELECTRICAL CHARACTERISTICS

$\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom.) }}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {enable }}=\mathrm{V}_{\text {in }}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted. $)$

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $V_{\text {out }}$ | $\begin{gathered} 1.455 \\ 1.746 \\ 2.425 \\ 2.646 \\ 2.744 \\ 2.940 \\ 3.234 \\ 4.9 \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 1.545 \\ 1.854 \\ 2.575 \\ 2.754 \\ 2.856 \\ 3.060 \\ 3.366 \\ 5.1 \end{gathered}$ | V |
| Line Regulation $\begin{aligned} & 1.5 \mathrm{~V}-4.4 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {o(nom.) }}+1.0 \mathrm{~V} \text { to } 6.0 \mathrm{~V}\right. \\ & 4.5 \mathrm{~V}-5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=5.5 \mathrm{~V} \text { to } 6.0 \mathrm{~V}\right) \end{aligned}$ | Regline |  | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=10 \mathrm{~mA}$ to 80 mA ) | Regload | - | 20 | 40 | mV |
| $\begin{aligned} & \text { Output Current }\left(\mathrm{V}_{\text {out }}=\left(\mathrm{V}_{\text {out }} \text { at } \mathrm{I}_{\text {out }}=80 \mathrm{~mA}\right)-3.0 \%\right) \\ & \left.1.5 \mathrm{~V} \text { to } 3.9 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {out }} \text { (nom. }\right)+2.0 \mathrm{~V}\right) \\ & 4.0 \mathrm{~V}-5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{o} \text { (nom.) }}$ | $\begin{aligned} & 80 \\ & 80 \end{aligned}$ | $\begin{aligned} & 280 \\ & 280 \end{aligned}$ | - | mA |
| Dropout Voltage ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$, $\mathrm{I}_{\text {out }}=80 \mathrm{~mA}$, Measured at $\begin{aligned} & \mathrm{V} \text { out }-3.0 \%) \\ & 1.5 \mathrm{~V}-1.7 \mathrm{~V} \\ & 1.8 \mathrm{~V}-2.4 \mathrm{~V} \\ & 2.5 \mathrm{~V}-2.6 \mathrm{~V} \\ & 2.7 \mathrm{~V}-2.9 \mathrm{~V} \\ & 3.0 \mathrm{~V}-3.2 \mathrm{~V} \\ & 3.3 \mathrm{~V}-4.9 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | - | $\begin{aligned} & 550 \\ & 400 \\ & 250 \\ & 230 \\ & 200 \\ & 190 \\ & 140 \end{aligned}$ | $\begin{aligned} & 800 \\ & 550 \\ & 400 \\ & 400 \\ & 350 \\ & 350 \\ & 250 \end{aligned}$ | mV |
| Quiescent Current <br> (Enable Input $=0 \mathrm{~V}$ ) <br> (Enable Input $=\mathrm{V}_{\text {in }}$, $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to $\left.\mathrm{I}_{\mathrm{o}(\text { nom. }}\right)$ | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.1 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 6.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Short Circuit Current $\begin{aligned} & 1.5 \mathrm{~V} \text { to } 3.9 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {nom }}+2.0 \mathrm{~V}\right) \\ & 4.0 \mathrm{~V}-5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\text {out(max) }}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | $\begin{aligned} & 600 \\ & 600 \end{aligned}$ | mA |
| Output Voltage Noise ( $\mathrm{f}=100 \mathrm{~Hz}$ to $100 \mathrm{kHz}, \mathrm{V}_{\text {out }}=3.0 \mathrm{~V}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 100 | - | $\mu \mathrm{Vrms}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(en) }}$ | $1.3$ | - | $\overline{0.3}$ | V |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm $/{ }^{\circ} \mathrm{C}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\Theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

NCP562


Figure 2. Quiescent Current versus Temperature


Figure 4. Output Voltage versus Temperature


Figure 3. Quiescent Current versus Input Voltage


Figure 5. Output Voltage versus Input Voltage


Figure 6. Dropout Voltage versus Temperature


Figure 7. Turn-On Response



Figure 10. Output Voltage Noise

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.

## APPLICATIONS INFORMATION

A typical application circuit for the NCP562 series is shown in Figure 1.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP562 package. Higher values and lower ESR will improve the overall line transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

## Output Decoupling (C2)

The NCP562 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $10 \Omega$ can thus safely be used. The minimum decoupling value is $0.1 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

## Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used, then the pin should be connected to $\mathrm{V}_{\mathrm{in}}$.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Thermal

As power across the NCP562 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP562 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP562 can dissipate up to 250 mW @ $25^{\circ} \mathrm{C}$.
The power dissipated by the NCP562 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} l_{\text {gnd }}\left(I_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right] * l_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If an 80 mA output current is needed then the ground current from the data sheet is $2.5 \mu \mathrm{~A}$. For an NCP562SQ30T1 (3.0 V), the maximum input voltage will then be 6.0 V .

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


NCP562

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP562SQ15T1 | 1.5 | LDI |  |  |
| NCP562SQ18T1 | 1.8 | LEY |  |  |
| NCP562SQ25T1 | 2.5 | LDK |  |  |
| NCP562SQ27T1 | 2.7 | LEZ | SC82-AB | 3000 Units/ |
| NCP562SQ28T1 | 2.8 | LDL |  |  |
| NCP562SQ30T1 | 3.0 | LDM |  |  |
| NCP562SQ33T1 | 3.3 | LDN |  |  |
| NCP562SQ50T1 | 5.0 | LDP |  |  |

Additional voltages are available upon request by contacting your ON Semiconductor representative.

## NCP563

## 80 mA CMOS Low Iq Low-Dropout Voltage Regulator

The NCP563 series of fixed output low-dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP563 series features an ultra-low quiescent current of $2.5 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP563 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of $0.1 \mu \mathrm{~F}$. The device is housed in the micro-miniature SC82-AB surface mount package. Standard voltage versions are $1.5,1.8,2.5,2.7,2.8,3.0,3.3$, and 5.0 V .

## Features

- Low Quiescent Current of $2.5 \mu \mathrm{~A}$ Typical
- Low Output Voltage Option
- Output Voltage Accuracy of $2.0 \%$
- Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Battery Powered Instruments
- Hand-Held Instruments
- Camcorders and Cameras


This device contains 28 active transistors

Figure 1. Representative Block Diagram


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 328 of this data sheet.

NCP563

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name |  |
| :---: | :---: | :--- |
| 1 | Gnd | Power supply ground. |
| 2 | Vin | Positive power supply input voltage. |
| 3 | Vout | Regulated output voltage. |
| 4 | N/C | No internal connection. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {in }}$ | 6.0 | V |
| Output Voltage | $\mathrm{V}_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Power Dissipation and Thermal Characteristics <br> Power Dissipation <br> Thermal Resistance, Junction to Ambient | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited |  |
| Operating Junction Temperature | $\mathrm{R}_{\theta \mathrm{JA}}$ |  | W |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{J}}$ | W |  |
| ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |  |  |
| Storage Temperature | $\mathrm{T}_{\mathrm{A}}$ | +125 | ${ }^{\circ} \mathrm{C}$ |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ | $\mathrm{T}_{\text {stg }}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{~mA} \mathrm{DC}$ with trigger voltage.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom.) }}+1.0 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $V_{\text {out }}$ | $\begin{gathered} 1.455 \\ 1.746 \\ 2.425 \\ 2.646 \\ 2.744 \\ 2.940 \\ 3.234 \\ 4.9 \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 1.545 \\ 1.854 \\ 2.575 \\ 2.754 \\ 2.856 \\ 3.060 \\ 3.366 \\ 5.1 \end{gathered}$ | V |
| Line Regulation $\begin{aligned} & 1.5 \mathrm{~V}-4.4 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {o(nom. }}+1.0 \mathrm{~V} \text { to } 6.0 \mathrm{~V}\right) \\ & 4.5 \mathrm{~V}-5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=5.5 \mathrm{~V} \text { to } 6.0 \mathrm{~V}\right) \end{aligned}$ | Regline |  | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=10 \mathrm{~mA}$ to 80 mA ) | Regload | - | 20 | 40 | mV |
| $\begin{aligned} & \text { Output Current }\left(\mathrm{V}_{\text {out }}=\left(\mathrm{V}_{\text {out }} \text { at } \mathrm{I}_{\text {out }}=80 \mathrm{~mA}\right)-3.0 \%\right) \\ & \left.1.5 \mathrm{~V} \text { to } 3.9 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {out(not }}\right)+2.0 \mathrm{~V}\right) \\ & 4.0 \mathrm{~V}-5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{0 \text { (nom.) }}$ | $\begin{aligned} & 80 \\ & 80 \end{aligned}$ | $\begin{aligned} & 280 \\ & 280 \end{aligned}$ | - | mA |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $85^{\circ} \mathrm{C}$, $\mathrm{I}_{\text {out }}=80 \mathrm{~mA}$, Measured at $V_{\text {out }}-3.0 \% \text { ) }$ <br> $1.5 \mathrm{~V}-1.7 \mathrm{~V}$ <br> $1.8 \mathrm{~V}-2.4 \mathrm{~V}$ <br> 2.5 V-2.6 V <br> 2.7 V-2.9 V <br> 3.0 V-3.2 V <br> $3.3 \mathrm{~V}-4.9 \mathrm{~V}$ <br> 5.0 V | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{aligned} & 550 \\ & 400 \\ & 250 \\ & 230 \\ & 200 \\ & 190 \\ & 140 \end{aligned}$ | $\begin{aligned} & 800 \\ & 550 \\ & 400 \\ & 400 \\ & 350 \\ & 350 \\ & 250 \end{aligned}$ | mV |
| Quiescent Current ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to $\mathrm{I}_{\text {out(nom) }}$ ) | $\mathrm{I}_{\mathrm{Q}}$ | - | 2.5 | 6.0 | $\mu \mathrm{A}$ |
| Output Short Circuit Current $\begin{aligned} & 1.5 \mathrm{~V} \text { to } 3.9 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {nom }}+2.0 \mathrm{~V}\right) \\ & 4.0 \mathrm{~V}-5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\text {out(max) }}$ | $\begin{aligned} & 100 \\ & 150 \end{aligned}$ | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | $\begin{aligned} & 600 \\ & 600 \end{aligned}$ | mA |
| Output Voltage Noise ( $\mathrm{f}=100 \mathrm{~Hz}$ to $100 \mathrm{kHz}, \mathrm{V}_{\text {out }}=3.0 \mathrm{~V}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 100 | - | $\mu \mathrm{Vrms}$ |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm $/{ }^{\circ} \mathrm{C}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.


Figure 2. Quiescent Current versus Temperature


Figure 4. Output Voltage versus Temperature


Figure 3. Quiescent Current versus Input Voltage


Figure 5. Output Voltage versus Input Voltage


Figure 6. Dropout Voltage versus Temperature


Figure 7. Line Transient Response


Figure 9. Output Voltage Noise

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.

## APPLICATIONS INFORMATION

A typical application circuit for the NCP563 series is shown in Figure 1.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP563 package. Higher values and lower ESR will improve the overall line transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

## Output Decoupling (C2)

The NCP563 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $10 \Omega$ can thus safely be used. The minimum decoupling value is $0.1 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Thermal

As power across the NCP563 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP563 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP563 can dissipate up to 250 mW @ $25^{\circ} \mathrm{C}$.

The power dissipated by the NCP563 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} \operatorname{lgnd}\left(l_{\text {out }}\right)\right]+\left.\left[V_{\text {in }}-V_{\text {out }}\right]^{*}\right|_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If an 80 mA output current is needed then the ground current from the data sheet is $2.5 \mu \mathrm{~A}$. For an NCP563SQ30T1 ( 3.0 V ), the maximum input voltage will then be 6.0 V .

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


## NCP563

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP563SQ15T1 | 1.5 | LDQ |  |  |
| NCP563SQ18T1 | 1.8 | LFA |  |  |
| NCP563SQ25T1 | 2.5 | LDS |  |  |
| NCP563SQ27T1 | 2.7 | LFB | SC82-AB | 3000 Units/ |
| NCP563SQ28T1 | 2.8 | LDT |  |  |
| NCP563SQ30T1 | 3.0 | LDU |  |  |
| NCP563SQ33T1 | 3.3 | LDV |  |  |
| NCP563SQ50T1 | 5.0 | LDX |  |  |

Additional voltages are available upon request by contacting your ON Semiconductor representative.

## LM2931 Series

## 100 mA, Adjustable Output, LDO Voltage Regulator with 60 V Load Dump Protection

The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power-up with mirror-image insertion.

Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The ' C ' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor-based systems.

- Input-to-Output Voltage Differential of < 0.6 V @ 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- -50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror-Image Protection
- Ideally Suited for Battery Powered Equipment
- Economical 5-Lead TO-220 Package with Two Optional Leadforms
- Available in Surface Mount SOP-8, D²PAK and DPAK Packages
- High Accuracy ( $\pm 2 \%$ ) Reference (LM2931AC) Available


## SOIC-8 D SUFFIX CASE 751



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ADJUSTABLE OUTPUT VOLTAGE


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 340 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking and heatsink information in the device marking section on page 341 of this data sheet.

## LM2931 Series

Representative Schematic Diagram


This device contains 26 active transistors.

## LM2931 Series

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage Continuous | $V_{1}$ | 40 | Vdc |
| Transient Input Voltage（ $\tau \leq 100 \mathrm{~ms}$ ） | $\mathrm{V}_{\mathbf{l}}(\tau)$ | 60 | Vpk |
| Transient Reverse Polarity Input Voltage $1.0 \%$ Duty Cycle，$\tau \leq 100 \mathrm{~ms}$ | $-\mathrm{V}_{\mathrm{I}}(\tau)$ | －50 | Vpk |
| Power Dissipation <br> Case 29 （TO－92 Type） $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance，Junction－to－Ambient <br> Thermal Resistance，Junction－to－Case <br> Case 221A，314A，314B and 314D（TO－220 Type） $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance，Junction－to－Ambient <br> Thermal Resistance，Junction－to－Case <br> Case 369A（DPAK）（Note 1） $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance，Junction－to－Ambient <br> Thermal Resistance，Junction－to－Case <br> Case 751 （SOP－8）（Note 2） $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance，Junction－to－Ambient <br> Thermal Resistance，Junction－to－Case <br> Case 936 and 936A（D2PAK）（Note 3） $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance，Junction－to－Ambient Thermal Resistance，Junction－to－Case | $\mathrm{P}_{\mathrm{D}}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> PD <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJc }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | Internally Limited 178 83 Internally Limited 65 5.0 Internally Limited 92 6.0 Internally Limited 160 25 Internally Limited 70 5.0 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Tested Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to＋150 | ${ }^{\circ} \mathrm{C}$ |

1．DPAK Junction－to－Ambient Thermal Resistance is for vertical mounting．Refer to Figure 24 for board mounted Thermal Resistance．
2．SOP－8 Junction－to－Ambient Thermal Resistance is for minimum recommended pad size．Refer to Figure 23 for Thermal Resistance variation versus pad size．
3．$D^{2}$ PAK Junction－to－Ambient Thermal Resistance is for vertical mounting．Refer to Figure 25 for board mounted Thermal Resistance．
4．ESD data available upon request．

## LM2931 Series

## ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{C}_{\mathrm{O}}=100 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}(\mathrm{ESR})}=0.3 \Omega, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ [Note 5])

| Characteristic | LM2931-5.0 | LM2931A-5.0 |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Unit |

## FIXED OUTPUT

| Output Voltage $\begin{aligned} \mathrm{V}_{\text {in }} & =14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {in }} & =6.0 \mathrm{~V} \text { to } 26 \mathrm{~V}, \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}, \\ \mathrm{~T}_{J} & =-40^{\circ} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 4.75 \\ & 4.50 \end{aligned}$ | $5.0$ | $\begin{aligned} & 5.25 \\ & 5.50 \end{aligned}$ | $\begin{aligned} & 4.81 \\ & 4.75 \end{aligned}$ |  | $\begin{aligned} & 5.19 \\ & 5.25 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\begin{aligned} & \mathrm{V}_{\text {in }}=9.0 \mathrm{~V} \text { to } 16 \mathrm{~V} \\ & \mathrm{~V}_{\text {in }}=6.0 \mathrm{~V} \text { to } 26 \mathrm{~V} \end{aligned}$ | $\mathrm{Reg}_{\text {line }}$ |  | $\begin{aligned} & 2.0 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 30 \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 30 \end{aligned}$ | mV |
| Load Regulation ( l = $=5.0 \mathrm{~mA}$ to 100 mA ) | Regload | - | 14 | 50 | - | 14 | 50 | mV |
| Output Impedance $\mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \Delta \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{f}=100 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}$ | $\mathrm{Z}_{0}$ | - | 200 | - | - | 200 | - | $\mathrm{m} \Omega$ |
| Bias Current $\begin{aligned} & V_{\text {in }}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {in }}=6.0 \mathrm{~V} \text { to } 26 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{~T}_{J}=-40^{\circ} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\mathrm{B}}$ |  | $\begin{aligned} & 5.8 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 30 \\ & 1.0 \end{aligned}$ |  | $\begin{aligned} & 5.8 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & 30 \\ & 1.0 \end{aligned}$ | mA |
| Output Noise Voltage ( $\mathrm{f}=10 \mathrm{~Hz}$ to 100 kHz ) | $\mathrm{V}_{\mathrm{n}}$ | - | 700 | - | - | 700 | - | $\mu \mathrm{Vrms}$ |
| Long Term Stability | S | - | 20 | - | - | 20 | - | mV/kHR |
| Ripple Rejection ( $\mathrm{f}=120 \mathrm{~Hz}$ ) | RR | 60 | 90 | - | 60 | 90 | - | dB |
| $\begin{gathered} \text { Dropout Voltage } \\ \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA} \end{gathered}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | $\begin{gathered} 0.015 \\ 0.16 \\ \hline \end{gathered}$ | $\begin{aligned} & 0.2 \\ & 0.6 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 0.015 \\ 0.16 \\ \hline \end{gathered}$ | $\begin{aligned} & 0.2 \\ & 0.6 \\ & \hline \end{aligned}$ | V |
| Over-Voltage Shutdown Threshold | $\mathrm{V}_{\mathrm{th}(\mathrm{OV})}$ | 26 | 29.5 | 40 | 26 | 29.5 | 40 | V |
| Output Voltage with Reverse Polarity Input $\left(\mathrm{V}_{\text {in }}=-15 \mathrm{~V}\right)$ | - $\mathrm{V}_{\mathrm{O}}$ | -0.3 | 0 | - | -0.3 | 0 | - | V |

5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

## LM2931 Series

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{C}_{\mathrm{O}}=100 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{O}(\mathrm{ESR})}=0.3 \Omega, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ [Note 5])

| Characteristic | LM2931C | LM2931AC |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Typ | Unit |

ADJUSTABLE OUTPUT

| Reference Voltage (Note 6., Figure 18) $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA}, \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 1.14 \\ & 1.08 \end{aligned}$ |  | $\begin{aligned} & 1.26 \\ & 1.32 \end{aligned}$ | $\begin{aligned} & 1.17 \\ & 1.15 \end{aligned}$ |  | $\begin{aligned} & 1.23 \\ & 1.25 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage Range | $\mathrm{V}_{\text {O range }}$ | $\begin{gathered} 3.0 \text { to } \\ 24 \end{gathered}$ | $\begin{gathered} 2.7 \text { to } \\ 29.5 \end{gathered}$ | - | $\begin{gathered} 3.0 \text { to } \\ 24 \end{gathered}$ | $\begin{gathered} 2.7 \text { to } \\ 29.5 \end{gathered}$ | - | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O}}+0.6 \mathrm{~V}$ to 26 V$)$ | Regline | - | 0.2 | 1.5 | - | 0.2 | 1.5 | $\mathrm{mV} / \mathrm{V}$ |
| Load Regulation ( l = $=5.0 \mathrm{~mA}$ to 100 mA ) | Regload | - | 0.3 | 1.0 | - | 0.3 | 1.0 | \%/V |
| Output Impedance $\mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \Delta \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{f}=10 \mathrm{~Hz} \text { to } 10 \mathrm{kHz}$ | $\mathrm{Z}_{0}$ | - | 40 | - | - | 40 | - | $\mathrm{m} \Omega / \mathrm{V}$ |
| Bias Current $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA} \end{aligned}$ <br> Output Inhibited $\left(\mathrm{V}_{\mathrm{th}(\mathrm{O})}=2.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{B}}$ |  | $\begin{aligned} & 6.0 \\ & 0.4 \\ & 0.2 \end{aligned}$ | $\begin{gathered} - \\ 1.0 \\ 1.0 \end{gathered}$ | - | $\begin{aligned} & 6.0 \\ & 0.4 \\ & 0.2 \end{aligned}$ | $\begin{gathered} - \\ 1.0 \\ 1.0 \end{gathered}$ | mA |
| Adjustment Pin Current | $I_{\text {Adj }}$ | - | 0.2 | - | - | 0.2 | - | $\mu \mathrm{A}$ |
| Output Noise Voltage ( $\mathrm{f}=10 \mathrm{~Hz}$ to 100 kHz ) | $\mathrm{V}_{\mathrm{n}}$ | - | 140 | - | - | 140 | - | $\mu \mathrm{Vrms} / \mathrm{V}$ |
| Long-Term Stability | S | - | 0.4 | - | - | 0.4 | - | \%/kHR |
| Ripple Rejection ( $\mathrm{f}=120 \mathrm{~Hz}$ ) | RR | 0.10 | 0.003 | - | 0.10 | 0.003 | - | \%/V |
| $\begin{gathered} \text { Dropout Voltage } \\ \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA} \\ \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA} \\ \hline \end{gathered}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | $\begin{gathered} 0.015 \\ 0.16 \\ \hline \end{gathered}$ | $\begin{aligned} & 0.2 \\ & 0.6 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 0.015 \\ 0.16 \\ \hline \end{gathered}$ | $\begin{aligned} & 0.2 \\ & 0.6 \\ & \hline \end{aligned}$ | V |
| Over-Voltage Shutdown Threshold | $\mathrm{V}_{\mathrm{th}(\mathrm{OV})}$ | 26 | 29.5 | 40 | 26 | 29.5 | 40 | V |
| Output Voltage with Reverse Polarity Input $\left(\mathrm{V}_{\text {in }}=-15 \mathrm{~V}\right)$ | - $\mathrm{V}_{\mathrm{O}}$ | -0.3 | 0 | - | -0.3 | 0 | - | V |
| $\begin{array}{ll} \text { Output Inhibit Threshold Voltages } \\ \text { Output "On": } & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40^{\circ} \text { to }+125^{\circ} \mathrm{C} \\ \text { Output "Off": } & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40^{\circ} \text { to }+125^{\circ} \mathrm{C} \end{array}$ | $\mathrm{V}_{\text {th(OI) }}$ | $\begin{gathered} - \\ 2.50 \\ 3.25 \end{gathered}$ | $\begin{gathered} 2.15 \\ - \\ 2.26 \end{gathered}$ | $\begin{aligned} & 1.90 \\ & 1.20 \end{aligned}$ | $\begin{gathered} - \\ - \\ 2.50 \\ 3.25 \end{gathered}$ | $\begin{gathered} 2.15 \\ - \\ 2.26 \end{gathered}$ | $\begin{gathered} 1.90 \\ 1.20 \\ - \end{gathered}$ | V |
| Output Inhibit Threshold Current ( $\mathrm{V}_{\text {th( }}(\mathrm{II})=2.5 \mathrm{~V}$ ) | $\mathrm{Ith}_{\text {(OI) }}$ | - | 30 | 50 | - | 30 | 50 | $\mu \mathrm{A}$ |

5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. The reference voltage on the adjustable device is measured from the output to the adjust pin across $R_{1}$.

## LM2931 Series



Figure 1. Dropout Voltage versus Output Current


Figure 3. Peak Output Current versus Input Voltage


Figure 5. Output Voltage versus Input Voltage


Figure 2. Dropout Voltage versus Junction Temperature


Figure 4. Output Voltage versus Input Voltage


Figure 6. Load Dump Characteristics


Figure 7. Bias Current versus Input Voltage


Figure 9. Bias Current versus Junction Temperature


Figure 11. Ripple Rejection versus Frequency


Figure 8. Bias Current versus Output Current


Figure 10. Output Impedance versus Frequency


Figure 12. Ripple Rejection versus Output Current


## APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow-out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power-up with mirror-image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor $\mathrm{C}_{\mathrm{in}}$ is recommended if the regulator is located an appreciable distance ( $\geq 4^{\prime \prime}$ ) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $\left|\mathrm{Z}_{\mathrm{O}}\right|$ must not exceed $0.4 \Omega$. This
limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around $-30^{\circ} \mathrm{C}$, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ and $-55^{\circ}$ to $+105^{\circ} \mathrm{C}$ are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $\left|Z_{O}\right|$ limit over temperature must be observed.
Note that in the stable region, the output noise voltage is linearly proportional to $\left|\mathrm{Z}_{\mathrm{O}}\right|$. In effect, $\mathrm{C}_{\mathrm{O}}$ dictates the high frequency roll-off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under-damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable". It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.


Figure 17. Fixed Output Regulator


The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V . Resistor R in conjunction with the $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting. This circuit is not short circuit proof.

Figure 19. (5.0 A) Low Differential Voltage Regulator


Figure 21. Constant Intensity Lamp Flasher


Switch Position $1=$ Output "On", $2=$ Output "Off"

$$
V_{\text {out }}=V_{\text {ref }}\left(1+\frac{R_{2}}{R_{1}}\right)+I_{\text {Adj }} R_{2} \quad 22.5 k \geq \frac{R_{1} R_{2}}{R_{1}+R_{2}}
$$

Figure 18. Adjustable Output Regulator


The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor $\mathrm{R}_{\mathrm{Sc}}$ and an additional PNP transistor. The current sensing PNP must be capable of handling the short circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

Figure 20. Current Boost Regulator with Short Circuit Projection


Figure 22. Output Noise Voltage versus Output Capacitor Impedance


Figure 23. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 24. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 25. 3-Pin and 5-Pin D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## LM2931 Series

## DEFINITIONS

Dropout Voltage - The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current - That part of the input current that is not delivered to the load.

Output Noise Voltage - The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long-Term Stability - Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

## LM2931 Series

ORDERING INFORMATION

| Device | Output |  | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
|  | Voltage | Tolerance |  |  |
| LM2931AD-5.0 | 5.0 V | $\pm 3.8 \%$ | SOIC-8 | 98 Units/Rail |
| LM2931AD-5.0R2 |  |  | SOIC-8 | 2500 Tape \& Reel |
| LM2931ADT-5.0 |  |  | DPAK | 75 Units/Rail |
| LM2931ADT-5.0RK |  |  | DPAK | 2500 VacPk Reel |
| LM2931AD2T-5.0 |  |  | D2PAK | 50 Units/Rail |
| LM2931AD2T-5.0R4 |  |  | D2PAK | 800 VacPk Reel |
| LM2931AT-5.0 |  |  | TO-220 | 50 Units/Rail |
| LM2931AZ-5.0 |  |  | TO-92 | 2000/Inner Bag |
| LM2931AZ-5.0RA |  |  | TO-92 | 2000 Tape \& Reel |
| LM2931AZ-5.0RP |  |  | TO-92 | 2000/Ammo Pack |
| LM2931D-5.0 |  | $\pm 5.0 \%$ | SOIC-8 | 98 Units/Rail |
| LM2931D-5.0R2 |  |  | SOIC-8 | 2500 Tape \& Reel |
| LM2931D2T-5.0 |  |  | D2PAK | 50 Units/Rail |
| LM2931D2T-5.0R4 |  |  | D2PAK | 800 VacPk Reel |
| LM2931DT-5.0 |  |  | DPAK | 75 Units/Rail |
| LM2931T-5.0 |  |  | TO-220 | 50 Units/Rail |
| LM2931Z-5.0 |  |  | TO-92 | 2000/Inner Bag |
| LM29312-5.0RA |  |  | TO-92 | 2000 Tape \& Reel |
| LM29312-5.0RP |  |  | TO-92 | 2000/Ammo Pack |
| LM2931CD | Adjustable |  | SOIC-8 | 98 Units/Rail |
| LM2931CDR2 |  |  | SOIC-8 | 2500 Tape \& Reel |
| LM2931CD2T |  |  | D2PAK | 50 Units/Rail |
| LM2931CD2TR4 |  |  | D2PAK | 800 VacPk Reel |
| LM2931CT |  |  | TO-220 | 50 Units/Rail |
| LM2931ACD |  | $\pm 2.0 \%$ | SOIC-8 | 98 Units/Rail |
| LM2931ACDR2 |  |  | SOIC-8 | 2500 Tape \& Reel |
| LM2931ACD2TR4 |  |  | D2PAK | 800 VacPk Reel |
| LM2931ACTV |  |  | TO-220 | 50 Units/Rail |

## LM2931 Series

MARKING DIAGRAMS


Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.


Heatsink surface connected to Pin 2.


Heatsink surface connected to Pin 3.


Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

| $\begin{aligned} & \text { SO-8 } \\ & \text { D SUFFIX } \\ & \text { CASE } 751 \end{aligned}$ |
| :---: |
|  |
| 2931A |
| ALYW |
| \# \\| \| |


$\begin{array}{ll}\text { A } & =\text { Assembly Location } \\ \text { WL, L } & =\text { Wafer Lot } \\ \text { YY, Y } & =\text { Year } \\ \text { WW, W } & =\text { Work Week }\end{array}$

## LP2950, LP2951

## 100 mA, 3.0 V, Low Power Low Dropout Voltage Regulator

The LP2950 and LP2951 are micropower voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-output voltage differential. These devices feature a very low quiescent bias current of $75 \mu \mathrm{~A}$ and are capable of supplying output currents in excess of 100 mA . Internal current and thermal limiting protection is provided.

The LP2951 has three additional features. The first is the $\overline{\text { Error }}$ Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power-on reset. The second feature allows the output voltage to be preset to $5.0 \mathrm{~V}, 3.3 \mathrm{~V}$ or 3.0 V output (depending on the version) or programmed from 1.25 V to 29 V . It consists of a pinned out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn-off or turn-on the regulator output.

Due to the low input-to-output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The LP2950 is available in the three pin case 29 and DPAK packages, and the LP2951 is available in the eight pin dual-in-line, SO-8 and Micro-8 surface mount packages. The ' $A$ ' suffix devices feature an initial output voltage tolerance $\pm 0.5 \%$.

## LP2950 and LP2951 Features:

- Low Quiescent Bias Current of $75 \mu \mathrm{~A}$
- Low Input-to-Output Voltage Differential of 50 mV at $100 \mu \mathrm{~A}$ and 380 mV at 100 mA
- 5.0 V, 3.3 V or $3.0 \mathrm{~V} \pm 0.5 \%$ Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a $1.0 \mu \mathrm{~F}$ Output Capacitor for Stability
- Internal Current and Thermal Limiting


## LP2951 Additional Features:

- Error Output Signals an Out of Regulation Condition
- Output Programmable from 1.25 V to 29 V
- Logic Level Shutdown Input
(See Following Page for Device Information.)

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ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on pages 354 and 355 of this data sheet.

DEVICE INFORMATION

| Package | Output Voltage |  |  |  | Operating Junction Temperature Range |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 3.0 V | 3.3 V | 5.0 V | Adjustable |  |
| TO-92 Suffix Z | $\begin{aligned} & \hline \text { LP2950CZ-3.0 } \\ & \text { LP2950ACZ-3.0 } \end{aligned}$ | $\begin{aligned} & \hline \text { LP2950CZ-3.3 } \\ & \text { LP2950ACZ-3.3 } \end{aligned}$ | $\begin{aligned} & \hline \text { LP2950CZ-5.0 } \\ & \text { LP2950ACZ-5.0 } \end{aligned}$ | Not <br> Available | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| DPAK <br> Suffix DT | $\begin{aligned} & \text { LP2950CDT-3.0 } \\ & \text { LP2950ACDT-3.0 } \end{aligned}$ | $\begin{aligned} & \text { LP2950CDT-3.3 } \\ & \text { LP2950ACDT-3.3 } \end{aligned}$ | $\begin{aligned} & \hline \text { LP2950CDT-5.0 } \\ & \text { LP2950ACDT-5.0 } \end{aligned}$ | Not <br> Available | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \hline \text { SO-8 } \\ & \text { Suffix D } \end{aligned}$ | $\begin{aligned} & \text { LP2951CD-3.0 } \\ & \text { LP2951ACD-3.0 } \end{aligned}$ | $\begin{aligned} & \text { LP2951CD-3.3 } \\ & \text { LP2951ACD-3.3 } \end{aligned}$ | $\begin{aligned} & \text { LP2951CD } \\ & \text { LP2951ACD } \end{aligned}$ | $\begin{aligned} & \text { LP2951CD } \\ & \text { LP2951ACD } \end{aligned}$ | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| Micro-8 Suffix DM | LP2951CDM-3.0 LP2951ACDM-3.0 | $\begin{aligned} & \text { LP2951CDM-3.3 } \\ & \hline \end{aligned}$ | LP2951CDM <br> LP2951ACDM | $\begin{aligned} & \hline \text { LP2951CDM } \\ & \text { LP2951ACDM } \end{aligned}$ | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| DIP-8 Suffix N | $\begin{aligned} & \hline \text { LP2951CN-3.0 } \\ & \text { LP2951ACN-3.0 } \end{aligned}$ | $\begin{aligned} & \hline \text { LP2951CN-3.3 } \\ & \text { LP2951ACN-3.3 } \end{aligned}$ | $\begin{aligned} & \hline \text { LP2951CN } \\ & \text { LP2951ACN } \end{aligned}$ | $\begin{aligned} & \text { LP2951CN } \\ & \text { LP2951ACN } \end{aligned}$ | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ |
| LP2950Cx-xx / LP2951Cxx-xx <br> LP2950ACx-xx / LP2951ACxx-xx |  | $1 \%$ Output Voltage Precision at $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ <br> $0.5 \%$ Output Voltage Precision at $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  |  |  |



Figure 1. Representative Block Diagrams

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 30 | Vdc |
| Power Dissipation and Thermal Characteristics Maximum Power Dissipation Case 751(SO-8) D Suffix <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case Case 369A (DPAK) DT Suffix (Note 1) <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case Case 29 (TO-226AA/TO-92) Z Suffix Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case <br> Case 626 N Suffix <br> Thermal Resistance, Junction-to-Ambient Case 846A (Micro-8) DM Suffix <br> Thermal Resistance, Junction-to-Ambient | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJA }}$ | Internally Limited <br> 180 <br> 45 <br> 92 <br> 6.0 <br> 160 <br> 83 <br> 105 <br> 240 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Feedback Input Voltage | $\mathrm{V}_{\mathrm{fb}}$ | -1.5 to +30 | Vdc |
| Shutdown Input Voltage | $\mathrm{V}_{\text {sd }}$ | -0.3 to +30 | Vdc |
| Error Comparator Output Voltage | $\mathrm{V}_{\text {err }}$ | -0.3 to +30 | Vdc |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=\mathrm{V}_{\mathrm{O}}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}, \mathrm{C}_{\mathrm{O}}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ [Note 3], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage, 5.0 V Versions | $\mathrm{V}_{\mathrm{O}}$ |  |  |  | V |
| $\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}, \mathrm{I}_{0}=100 \mu \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-5.0/LP2951C |  | 4.950 | 5.000 | 5.050 |  |
| LP2950AC-5.0/LP2951AC |  | 4.975 | 5.000 | 5.025 |  |
| $\mathrm{T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-5.0/LP2951C |  | 4.900 | - | 5.100 |  |
| LP2950AC-5.0/LP2951AC |  | 4.940 | - | 5.060 |  |
| $\mathrm{V}_{\text {in }}=6.0$ to $30 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}$ to $100 \mathrm{~mA}, \mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-5.0/LP2951C |  | 4.880 | - | 5.120 |  |
| LP2950AC-5.0/LP2951AC |  | 4.925 | - | 5.075 |  |
| Output Voltage, 3.3 V Versions | $\mathrm{V}_{\mathrm{O}}$ |  |  |  | V |
| $\mathrm{V}_{\text {in }}=4.3 \mathrm{~V}, \mathrm{I}_{0}=100 \mu \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-3.3/LP2951C-3.3 |  | 3.267 | 3.300 | 3.333 |  |
| LP2950AC-3.3/LP2951AC-3.3 |  | 3.284 | 3.300 | 3.317 |  |
| $\mathrm{T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-3.3/LP2951C-3.3 |  | 3.234 | - | 3.366 |  |
| LP2950AC-3.3/LP2951AC-3.3 |  | 3.260 | - | 3.340 |  |
| $\mathrm{V}_{\text {in }}=4.3$ to $30 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}$ to $100 \mathrm{~mA}, \mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-3.3/LP2951C-3.3 |  | 3.221 | - | 3.379 |  |
| LP2950AC-3.3/LP2951AC-3.3 |  | 3.254 | - | 3.346 |  |
| Output Voltage, 3.0 V Versions | $\mathrm{V}_{\mathrm{O}}$ |  |  |  | V |
| $\mathrm{V}_{\text {in }}=4.0 \mathrm{~V}, \mathrm{I}_{0}=100 \mu \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-3.0/LP2951C-3.0 |  | 2.970 | 3.000 | 3.030 |  |
| LP2950AC-3.0/LP2951AC-3.0 |  | 2.985 | 3.000 | 3.015 |  |
| $\mathrm{T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-3.0/LP2951C-3.0 |  | 2.940 | - | 3.060 |  |
| LP2950AC-3.0/LP2951AC-3.0 |  | 2.964 | - | 3.036 |  |
| $\mathrm{V}_{\text {in }}=4.0$ to $30 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}$ to $100 \mathrm{~mA}, \mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  |  |  |  |  |
| LP2950C-3.0/LP2951C-3.0 |  | 2.928 | - | 3.072 |  |
| LP2950AC-3.0/LP2951AC-3.0 |  | 2.958 | - | 3.042 |  |

1. The Junction-to-Ambient Thermal Resistance is determined by PC board copper area per Figure 27.
2. ESD data available upon request.
3. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. $\mathrm{V}_{\mathrm{O}(\mathrm{nom})}$ is the part number voltage option.
5. Noise tests on the LP2951 are made with a $0.01 \mu \mathrm{~F}$ capacitor connected across Pins 7 and 1 .

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{in}}=\mathrm{V}_{\mathrm{O}}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}, \mathrm{C}_{\mathrm{O}}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ [Note 8], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O} \text { (nom) }}+1.0 \mathrm{~V}$ to 30 V ) (Note 9) LP2950C-XX/LP2951C/LP2951C-XX LP2950AC-XX/LP2951AC/LP2951AC-XX | Regline |  | $\begin{aligned} & 0.08 \\ & 0.04 \end{aligned}$ | $\begin{aligned} & 0.20 \\ & 0.10 \end{aligned}$ | \% |
| Load Regulation ( $\mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}$ to 100 mA ) LP2950C-XX/LP2951C/LP2951C-XX LP2950AC-XX/LP2951AC/LP2951AC-XX | Regload |  | $\begin{aligned} & 0.13 \\ & 0.05 \end{aligned}$ | $\begin{aligned} & 0.20 \\ & 0.10 \end{aligned}$ | \% |
| $\begin{gathered} \text { Dropout Voltage } \\ \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A} \\ \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA} \\ \hline \end{gathered}$ | $\mathrm{V}_{1}-\mathrm{V}_{\mathrm{O}}$ | - | $\begin{gathered} 30 \\ 350 \end{gathered}$ | $\begin{gathered} 80 \\ 450 \end{gathered}$ | mV |
| $\begin{aligned} & \text { Supply Bias Current } \\ & \mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A} \\ & \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA} \\ & \hline \end{aligned}$ | $I_{\text {cc }}$ |  | $\begin{aligned} & 93 \\ & 4.0 \end{aligned}$ | $\begin{gathered} 120 \\ 12 \end{gathered}$ | $\begin{gathered} \mu \mathrm{A} \\ \mathrm{~mA} \end{gathered}$ |
| Dropout Supply Bias Current $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O} \text { (nom) }}-0.5 \mathrm{~V}\right.$, $\left.\mathrm{I}_{\mathrm{O}}=100 \mu \mathrm{~A}\right)($ Note 9$)$ | ICCdropout | - | 110 | 170 | $\mu \mathrm{A}$ |
| Current Limit ( $\mathrm{V}_{\mathrm{O}}$ Shorted to Ground) | $\mathrm{I}_{\text {Limit }}$ | - | 220 | 300 | mA |
| Thermal Regulation | $\mathrm{Reg}_{\text {thermal }}$ | - | 0.05 | 0.20 | \%/W |
| Output Noise Voltage ( 10 Hz to 100 kHz ) (Note 10) $\begin{aligned} & C_{L}=1.0 \mu \mathrm{~F} \\ & C_{L}=100 \mu \mathrm{~F} \end{aligned}$ | $\mathrm{V}_{\mathrm{n}}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{gathered} 126 \\ 56 \end{gathered}$ | - | $\mu \mathrm{Vrms}$ |

LP2951A/LP2951AC ONLY

| Reference Voltage ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) <br> LP2951C/LP2951C-XX <br> LP2951AC/LP2951AC-XX | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 1.210 \\ & 1.220 \end{aligned}$ | $\begin{aligned} & 1.235 \\ & 1.235 \end{aligned}$ | $\begin{aligned} & 1.260 \\ & 1.250 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Reference Voltage }\left(T_{J}=-40 \text { to }+125^{\circ} \mathrm{C}\right) \\ & \text { LP2951C/LP2951C-XX } \\ & \text { LP2951AC/LP2951AC-XX } \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 1.200 \\ & 1.200 \end{aligned}$ |  | $\begin{aligned} & 1.270 \\ & 1.260 \end{aligned}$ | V |
| ```Reference Voltage ( }\mp@subsup{T}{J}{}=-40\mathrm{ to +125 ' C) IO}=100\mu\textrm{A}\mathrm{ to }100\textrm{mA},\mp@subsup{\textrm{V}}{\mathrm{ in }}{=23 to 30 V LP2951C/LP2951C-XX LP2951AC/LP2951AC-XX``` | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 1.185 \\ & 1.190 \end{aligned}$ |  | $\begin{aligned} & 1.285 \\ & 1.270 \end{aligned}$ | V |
| Feedback Pin Bias Current | $\mathrm{I}_{\text {FB }}$ | - | 15 | 40 | nA |

ERROR COMPARATOR

| Output Leakage Current $\left(\mathrm{V}_{\mathrm{OH}}=30 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{kg}}$ | - | 0.01 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Low Voltage $\left(\mathrm{V}_{\text {in }}=4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{OL}}=400 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 150 | 250 | mV |
| Upper Threshold Voltage $\left(\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {thu }}$ | 40 | 45 | - | mV |
| Lower Threshold Voltage $\left(\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {thl }}$ | - | 60 | 95 | mV |
| Hysteresis $\left(\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {hy }}$ | - | 15 | - | mV |

## SHUTDOWN INPUT

| Input Logic Voltage <br> Logic "0" (Regulator "On") <br> Logic "1" (Regulator "Off") | $\mathrm{V}_{\text {shtdn }}$ |  |  | $\begin{aligned} & 0.7 \\ & 30 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Shutdown Pin Input Current $\begin{aligned} & \mathrm{V}_{\text {shtdd }}=2.4 \mathrm{~V} \\ & \mathrm{~V}_{\text {shtdn }}=30 \mathrm{~V} \end{aligned}$ | $I_{\text {shtdn }}$ | - | $\begin{gathered} 35 \\ 450 \end{gathered}$ | $\begin{gathered} 50 \\ 600 \end{gathered}$ | $\mu \mathrm{A}$ |
| Regulator Output Current in Shutdown Mode $\left(\mathrm{V}_{\text {in }}=30 \mathrm{~V}, \mathrm{~V}_{\text {shtdn }}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0\right.$, Pin 6 Connected to Pin 7) | $\mathrm{l}_{\text {off }}$ | - | 3.0 | 10 | $\mu \mathrm{A}$ |

6. The Junction-to-Ambient Thermal Resistance is determined by PC board copper area per Figure 27.
7. ESD data available upon request.
8. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
9. $V_{O(n o m)}$ is the part number voltage option.
10. Noise tests on the LP2951 are made with a $0.01 \mu \mathrm{~F}$ capacitor connected across Pins 7 and 1.

## DEFINITIONS

Dropout Voltage - The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation - The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current - Current which is used to operate the regulator chip and is not delivered to the load.


Figure 2. Quiescent Current


Figure 4. Input Current

Output Noise Voltage - The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Leakage Current - Current drawn through a bipolar transistor collector-base junction, under a specified collector voltage, when the transistor is "off".
Upper Threshold Voltage - Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic " 0 " to " 1 ".
Lower Threshold Voltage - Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic " 1 " to " 0 ".
Hysteresis - The difference between Lower Threshold voltage and Upper Threshold voltage.


Figure 3. Dropout Characteristics


Figure 5. Output Voltage versus Temperature


Figure 6. Dropout Voltage versus Output Current


Figure 7. Dropout Voltage versus Temperature


Figure 8. Error Comparator Output


Figure 9. Line Transient Response


Figure 10. LP2951 Enable Transient


Figure 11. Load Transient Response


Figure 12. Ripple Rejection


Figure 14. Shutdown Threshold Voltage versus Temperature


Figure 13. Output Noise


Figure 15. Maximum Rated Output Current

## APPLICATIONS INFORMATION

## Introduction

The LP2950/LP2951 regulators are designed with internal current limiting and thermal shutdown making them user-friendly. Typical application circuits for the LP2950 and LP2951 are shown in Figures 18 through 26.

These regulators are not internally compensated and thus require a $1.0 \mu \mathrm{~F}$ (or greater) capacitance between the LP2950/LP2951 output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below $25^{\circ} \mathrm{C}$.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to $0.33 \mu \mathrm{~F}$ for currents less than 10 mA , or $0.1 \mu \mathrm{~F}$ for currents below 1.0 mA . Using the 8 -pin versions at voltages less than 5.0 V operates the error amplifier at lower values of gain, so that more output capacitance is needed for stability. For the worst case operating condition of a 100 mA load at 1.23 V output (Output Pin 1 connected to the feedback Pin 7) a minimum capacitance of $3.3 \mu \mathrm{~F}$ is recommended.

The LP2950 will remain stable and in regulation when operated with no output load. When setting the output voltage of the LP2951 with external resistors, the resistance values should be chosen to draw a minimum of $1.0 \mu \mathrm{~A}$.

A bypass capacitor is recommended across the LP2950/LP2951 input to ground if more than 4 inches of wire connects the input to either a battery or power supply filter capacitor

Input capacitance at the LP2951 Feedback Pin 7 can create a pole, causing instability if high value external resistors are used to set the output voltage. Adding a 100 pF capacitor between the Output Pin 1 and the Feedback Pin 7 and increasing the output filter capacitor to at least $3.3 \mu \mathrm{~F}$ will stabilize the feedback loop.

## Error Detection Comparator

The comparator switches to a positive logic low whenever the LP2951 output voltage falls more than approximately $5.0 \%$ out of regulation. This value is the comparator's designed-in offset voltage of 60 mV divided by the 1.235 V internal reference. As shown in the representative block diagram. This trip level remains $5.0 \%$ below normal regardless of the value of regulated output voltage. For example, the error flag trip level is 4.75 V for a normal 5.0 V regulated output, or 9.50 V for a 10 V output voltage.

Figure 2 is a timing diagram which shows the ERROR signal and the regulated output voltage as the input voltage
to the LP2951 is ramped up and down. The $\overline{\mathrm{ERROR}}$ signal becomes valid (low) at about 1.3 V input. It goes high when the input reaches about 5.0 V ( $\mathrm{V}_{\text {out }}$ exceeds about 4.75 V ). Since the LP2951's dropout voltage is dependent upon the load current (refer to the curve in the Typical Performance Characteristics), the input voltage trip point will vary with load current. The output voltage trip point does not vary with load.
The error comparator output is an open collector which requires an external pull-up resistor. This resistor may be returned to the output or some other voltage within the system. The resistance value should be chosen to be consistent with the $400 \mu \mathrm{~A}$ sink capability of the error comparator. A value between 100 k and $1.0 \mathrm{M} \Omega$ is suggested. No pull-up resistance is required if this output is unused.
When operated in the shutdown mode, the error comparator output will go high if it has been pulled up to an external supply. To avoid this invalid response, the error comparator output should be pulled up to $\mathrm{V}_{\text {out }}$ (see Figure 16).


Figure 16. ERROR Output Timing

## Programming the Output Voltage (LP2951)

The LP2951CX may be pin-strapped for the nominal fixed output voltage using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5.0 V tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference voltage and its 30 V maximum rating. An external pair of resistors is required, as shown in Figure 17.


Figure 17. Adjustable Regulator
The complete equation for the output voltage is:

$$
v_{\text {out }}=v_{\text {ref }}(1+R 1 / R 2)+I_{F B} R 1
$$

where $\mathrm{V}_{\text {ref }}$ is the nominal 1.235 V reference voltage and $\mathrm{I}_{\mathrm{FB}}$ is the feedback pin bias current, nominally -20 nA . The minimum recommended load current of $1.0 \mu \mathrm{~A}$ forces an upper limit of $1.2 \mathrm{M} \Omega$ on the value of R 2 , if the regulator must work with no load. $\mathrm{I}_{\mathrm{FB}}$ will produce a $2 \%$ typical error in $\mathrm{V}_{\text {out }}$ which may be eliminated at room temperature by adjusting R1. For better accuracy, choosing R2 $=100 \mathrm{k}$ reduces this error to $0.17 \%$ while increasing the resistor program current to $12 \mu \mathrm{~A}$. Since the LP2951 typically draws $75 \mu \mathrm{~A}$ at no load with Pin 2 open circuited, the extra $12 \mu \mathrm{~A}$ of current drawn is often a worthwhile tradeoff for eliminating the need to set output voltage in test.

## Output Noise

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method
for reducing noise on the 3 lead LP2950. However, increasing the capacitor from $1.0 \mu \mathrm{~F}$ to $220 \mu \mathrm{~F}$ only decreases the noise from $430 \mu \mathrm{~V}$ to $160 \mu \mathrm{Vrms}$ for a 100 kHz bandwidth at the 5.0 V output.
Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity. Pick

$$
C_{\text {Bypass }} \approx \frac{1}{2 \pi R 1 \times 200 \mathrm{~Hz}}
$$

or about $0.01 \mu \mathrm{~F}$. When doing this, the output capacitor must be increased to $3.3 \mu \mathrm{~F}$ to maintain stability. These changes reduce the output noise from $430 \mu \mathrm{~V}$ to $126 \mu \mathrm{Vrms}$ for a 100 kHz bandwidth at 5.0 V output. With bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.


Figure 18. 1.0 A Regulator with 1.2 V Dropout

## TYPICAL APPLICATIONS



Figure 19. Lithium Ion Battery Cell Charger


Figure 20. Low Drift Current Sink


Error flag occurs when $\mathrm{V}_{\text {in }}$ is too low to maintain $\mathrm{V}_{\text {out }}$, or if $\mathrm{V}_{\text {out }}$ is reduced by excessive load current.

Figure 21. Latch Off When Error Flag Occurs


Figure 22. 5.0 V Regulator with 2.5 V Sleep Function


All diodes are 1N4148.
Early Warning flag on low input voltage.
Main output latches off at lower input voltages.
Battery backup on auxiliary output.
Operation: Regulator \#1's $\mathrm{V}_{\text {out }}$ is programmed one diode drop above 5.0 V . Its error flag becomes active when $\mathrm{V}_{\text {in }} \leq 5.7 \mathrm{~V}$. When $\mathrm{V}_{\text {in }}$ drops below 5.3 V , the error flag of regulator \#2 becomes active and via Q1 latches the main output "off". When $\mathrm{V}_{\text {in }}$ again exceeds 5.7 V , regulator \#1 is back in regulation and the early warning signal rises, unlatching regulator \#2 via D3.

Figure 23. Regulator with Early Warning and Auxiliary Output

$\mathrm{V}_{\text {out }}=1.25 \mathrm{~V}(1.0+\mathrm{R} 1 / \mathrm{R} 2)$
For 5.0 V output, use internal resistors. Wire Pin 6 to 7 , and wire Pin 2 to $+V_{\text {out }}$ Bus.

Figure 24. 2.0 A Low Dropout Regulator


Figure 25. Open Circuit Detector for 4.0 to 20 mA Current Loop


Figure 26. Low Battery Disconnect


Figure 27. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

ORDERING INFORMATION (LP2950)

| Part Number | Output Voltage <br> (Volts) | Tolerance (\%) | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| LP2950CZ-3.0 | 3.0 | 1.0 | TO-92 | 2000 Units / Bag |
| LP2950ACZ-3.0 | 3.0 | 0.5 | TO-92 | 2000 Units / Bag |
| LP2950CZ-3.3 | 3.3 | 1.0 | TO-92 | 2000 Units / Bag |
| LP2950ACZ-3.3 | 3.3 | 0.5 | TO-92 | 2000 Units / Bag |
| LP2950CZ-3.3RA | 3.3 | 1.0 | TO-92 | 2000 Units / Tape \& Reel |
| LP2950ACZ-3.3RA | 3.3 | 0.5 | TO-92 | 2000 Units / Tape \& Reel |
| LP2950CZ-5.0 | 5.0 | 1.0 | TO-92 | 2000 Units / Bag |
| LP2950ACZ-5.0 | 5.0 | 0.5 | TO-92 | 2000 Units / Bag |
| LP2950CZ-5.0RA | 5.0 | 1.0 | TO-92 | 2000 Units / Tape \& Reel |
| LP2950CZ-5.0RP | 5.0 | 1.0 | TO-92 | 2000 Units / Ammo Pack |
| LP2950ACZ-5.0RA | 5.0 | 0.5 | TO-92 | 2000 Units / Tape \& Reel |
| LP2950CDT-3.0 | 3.0 | 1.0 | DPAK | 75 Units / Rail |
| LP2950CDT-3.0RK | 3.0 | 1.0 | DPAK | 2500 Units / Tape \& Reel |
| LP2950ACDT-3.0 | 3.0 | 0.5 | DPAK | 75 Units / Rail |
| LP2950CDT-3.3 | 3.3 | 1.0 | DPAK | 75 Units / Rail |
| LP2950CDT-3.3RK | 3.3 | 1.0 | DPAK | 2500 Units / Tape \& Reel |
| LP2950ACDT-3.3 | 3.3 | 0.5 | DPAK | 75 Units / Rail |
| LP2950CDT-5.0 | 5.0 | 1.0 | DPAK | 75 Units / Rail |
| LP2950CDT-5.0RK | 5.0 | 1.0 | DPAK | 2500 Units / Tape \& Reel |
| LP2950ACDT-5.0 | 5.0 | 0.5 | DPAK | 75 Units / Rail |
| LP2950ACDT-5.0RK | 5.0 | 0.5 | DPAK | 2500 Units / Tape \& Reel |

ORDERING INFORMATION (LP2951)

| Part Number | Output Voltage <br> (Volts) | Tolerance (\%) | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| LP2951CD-3.0 | 3.0 or Adj. | 1.0 | SO-8 | 98 Units / Rail |
| LP2951CD-3.0R2 | 3.0 or Adj. | 1.0 | SO-8 | 2500 Units / Tape \& Reel |
| LP2951ACD-3.0 | 3.0 or Adj. | 0.5 | SO-8 | 98 Units / Rail |
| LP2951ACD-3.0R2 | 3.0 or Adj. | 0.5 | SO-8 | 2500 Units / Tape \& Reel |
| LP2951CD-3.3 | 3.3 or Adj. | 1.0 | SO-8 | 98 Units / Rail |
| LP2951CD-3.3R2 | 3.3 or Adj. | 1.0 | SO-8 | 2500 Units / Tape \& Reel |
| LP2951ACD-3.3 | 3.3 or Adj. | 0.5 | SO-8 | 98 Units / Rail |
| LP2951ACD-3.3R2 | 3.3 or Adj. | 0.5 | SO-8 | 2500 Units / Tape \& Reel |
| LP2951CD | 5.0 or Adj. | 2.0 | SO-8 | 98 Units / Rail |
| LP2951CDR2 | 5.0 or Adj. | 2.0 | SO-8 | 2500 Units / Tape \& Reel |
| LP2951ACD | 5.0 or Adj. | 1.2 | SO-8 | 98 Units / Rail |
| LP2951ACDR2 | 5.0 or Adj. | 1.2 | SO-8 | 2500 Units / Tape \& Reel |
| LP2951CDM-3.0R2 | 3.0 or Adj. | 1.0 | Micro-8 | 2500 Units / Tape \& Reel |
| LP2951ACDM-3.0R2 | 3.0 or Adj. | 0.5 | Micro-8 | 2500 Units / Tape \& Reel |
| LP2951CDM-3.3R2 | 3.3 or Adj. | 1.0 | Micro-8 | 2500 Units / Tape \& Reel |
| LP2951ACDM-3.3R2 | 3.3 or Adj. | 0.5 | Micro-8 | 2500 Units / Tape \& Reel |
| LP2951CDMR2 | 5.0 or Adj. | 2.0 | Micro-8 | 2500 Units / Tape \& Reel |
| LP2951ACDMR2 | 5.0 or Adj. | 1.2 | Micro-8 | 2500 Units / Tape \& Reel |
| LP2951CN-3.0 | 3.0 or Adj. | 1.0 | DIP-8 | 50 Units / Rail |
| LP2951ACN-3.0 | 3.0 or Adj. | 0.5 | DIP-8 | 50 Units / Rail |
| LP2951CN-3.3 | 3.3 or Adj. | 1.0 | DIP-8 | 50 Units / Rail |
| LP2951ACN-3.3 | 3.3 or Adj. | 0.5 | DIP-8 | 50 Units / Rail |
| LP2951CN | 5.0 or Adj. | 2.0 | DIP-8 | 50 Units / Rail |
| LP2951ACN | 5.0 or Adj. | 1.2 | DIP-8 | 50 Units / Rail |

## CS8221

## Micropower 5.0 V, 100 mA Low Dropout Linear Regulator

The CS8221 is a precision $5.0 \mathrm{~V}, 100 \mathrm{~mA}$ micropower voltage regulator with very low quiescent current ( $60 \mu \mathrm{~A}$ typical at $100 \mu \mathrm{~A}$ load). The 5.0 V output is accurate within $\pm 2.0 \%$ and supplies 100 mA of load current with a maximum dropout voltage of only 600 mV .

The regulator is protected against reverse battery, short circuit, overvoltage, and over temperature conditions. The device can withstand 74 V peak transients making it suitable for use in automotive environments. The CS8221 is pin for pin compatible with the LM2931.

## Features

- Low Quiescent Current ( $60 \mu \mathrm{~A}$ @ $100 \mu \mathrm{~A}$ Load)
- $5.0 \mathrm{~V} \pm 2.0 \%$ Output
- 100 mA Output Current Capability
- Internally Fused Leads in SO-8 Package
- Fault Protection
- +74 V Peak Transient Voltage
-     - 15 V Reverse Voltage
- Short Circuit
- Thermal Shutdown

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com
SO-8
DFSUFFIX
CASE 751

PIN CONNECTIONS AND MARKING INDIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8221YDF8 | SO-8 | 95 Units/Rail |
| CS8221YDFR8 | SO-8 | 2500 Tape \& Reel |
| CS8221YDP3 | D$^{2}$ PAK, 3-PIN | 50 Units/Rail |
| CS8221YDPR3 | D$^{2}$ PAK, 3-PIN | 750 Tape \& Reel |

*Contact your local sales representative for TO-92 package option.


Figure 1. Block Diagram
ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Junction Temperature Range, $\mathrm{T}_{J}$ | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\text {STORAGE }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation | Internally Limited | - |
| Peak Transient Voltage (60 V Load Dump @ $\mathrm{VIN}_{\text {IN }}=14 \mathrm{~V}$ ) | $-15,74$ | V |
| Input Operating Range | Reflow (Note 1) | 230 peak |
| Output Current | -0.5 to 26 | V |
| Electrostatic Discharge (Human Body Model) | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering: | Internally Limited | - |

1. 60 seconds maximum above $183^{\circ}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(6.0 \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, I $\mathrm{l}_{\mathrm{OUT}}=1.0 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Output Voltage, V ${ }_{\text {OUT }}$ | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA} \\ & 6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{IOUT} \leq 100 \mathrm{~mA} \end{aligned}$ | $\begin{gathered} 4.9 \\ 4.85 \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 5.1 \\ 5.15 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Dropout Voltage ( $\left.\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right)$ | $\begin{aligned} & \text { lout }=100 \mathrm{~mA} \\ & \text { lout }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 100 \mathrm{~mA}$, | - | 5.0 | 50 | mV |
| Line Regulation | $6.0 \mathrm{~V}<\mathrm{V}<26 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) | $\begin{aligned} & \text { lout }=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{IN}}=6.0 \mathrm{~V} \\ & \text { IOUT }=50 \mathrm{~mA} \\ & \text { IOUT }=100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 60 \\ & 4.0 \\ & 12 \end{aligned}$ | $\begin{aligned} & 120 \\ & 6.0 \\ & 20 \end{aligned}$ | $\mu \mathrm{A}$ <br> mA <br> mA |
| Ripple Rejection | $7.0 \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$, $\mathrm{l}_{\text {OUT }}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ | 60 | 75 | - | dB |
| Current Limit | - | 125 | 200 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 40 | 125 | - | $\mu \mathrm{A}$ |
| Thermal Shutdown (Note 2) | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT }} \leq 1.0 \mathrm{~V}$ | 30 | 34 | 38 | V |

2. This parameter is guaranteed by design, but not parametrically tested in production.

PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  |  | FUNCTION |
| :---: | :---: | :---: | :--- | :--- |
| SO-8 | D$^{2}$ PAK | LEAD SYMBOL |  |  |
| 1 | 3 | V $_{\text {OUT }}$ | $5.0 \mathrm{~V}, \pm 2.0 \%, 100 \mathrm{~mA}$ Output. |  |
| $2,3,6,7$ | 2 | GND | Ground. |  |
| 4 | - | NC | No Connection. |  |
| 5 | - | NC | No Connection. |  |
| 8 | 1 | $\mathrm{~V}_{\mathrm{IN}}$ | Input Voltage. |  |

## CIRCUIT DESCRIPTION

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 2).


Figure 2. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 30 V , the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.


Figure 3. Application and Test Diagram

## STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor CouT shown in Figure 3 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for Cout for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.
Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.
Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Increase the temperature to your highest operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 4) is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT }(\mathrm{min})}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta J A}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like
$R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

Figure 4. Single Output Regulator With Key Performance Parameters Labeled

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | D $^{2}$ PAK, <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 25 | 4.2 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {OJA }}$ | Typical | 110 | $10-50^{\star}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\theta \mathrm{JA}}=\mathrm{R}_{\theta \mathrm{JC}}=\mathrm{R}_{\theta \mathrm{CA}}$


## CS9201

## Micropower 5.0 V, 100 mA <br> Low Dropout Linear Regulator with NOCAPTM

The CS9201 is a precision $5.0 \mathrm{~V}, 100 \mathrm{~mA}$ voltage regulator with low quiescent current ( $450 \mu \mathrm{~A}$ typ. @ $100 \mu \mathrm{~A}$ load). The 5.0 V output is accurate within $\pm 2 \%$ and supplies 100 mA of load current with a maximum dropout voltage of only 600 mV .

The regulator is protected against reverse battery, short circuit, over voltage, and over temperature conditions. The device can withstand 74 V peak transients making it suitable for use in automotive environments. ON's proprietary NOCAP solution is the first technology which allows the output to be stable without the use of an external capacitor. NOCAP is suitable for slow switching or steady loads.

## Features

- NOCAP
- Low Quiescent Current ( $450 \mu \mathrm{~A}$ typ. @ $100 \mu \mathrm{~A}$ load)
- $5.0 \mathrm{~V}, \pm 2 \%$ Output
- 100 mA Output Current Capability
- Fault Protection
- 74 V Peak Transient Voltage
-     - 15 V Reverse Voltage
- Short Circuit
- Thermal Shutdown
- Overvoltage Shutdown
- Internally Fused Leads

(1) Contact factory for optional Sense lead.



## ON Semiconductor ${ }^{\text {T }}$

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PIN CONNECTIONS AND MARKING DIAGRAM

$\begin{array}{ll}\text { A } & =\text { Assembly Location } \\ \text { WL, L } & =\text { Wafer Lot } \\ \text { YY, Y } & =\text { Year } \\ \text { WW, W } & =\text { Work Week }\end{array}$

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS9201YDF8 | SO-8 | 95 Units/Rail |
| CS9201YDFR8 | SO-8 | 2500 Tape \& Reel |

Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Dissipation |  | Internally Limited | - |
| Input Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ): <br> DC <br> Peak Transient Voltage ( 60 V Load Dump @ $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$ ) |  | $\begin{gathered} -15 \text { to } 36 \\ 74 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Output Current |  | Internally Limited | - |
| ESD Susceptibility (Human Body Model) |  | 4.0 | kV |
| Package Thermal Resistance: <br> Junction-to-Case, R $\mathrm{R}_{\text {日J }}$ Junction-to-Ambient, R $\mathrm{R}_{\text {JA }}$ |  | $\begin{gathered} 25 \\ 110 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Junction Temperature |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow (SMD styles only) Note 1 | 230 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, I $\mathrm{I}_{\mathrm{OUT}}=1.0 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Output Voltage, V ${ }_{\text {OUT }}$ | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mathrm{uA} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA} \\ & 6.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}, 100 \mathrm{uA} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.90 \\ & 4.85 \end{aligned}$ | $\begin{aligned} & 5.00 \\ & 5.00 \end{aligned}$ | $\begin{aligned} & 5.10 \\ & 5.15 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\begin{aligned} & \text { IOUT }=100 \mathrm{~mA} \\ & \text { IOUT }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 100 \mathrm{~mA}$ | - | 5 | 50 | mV |
| Line Regulation | $6.0 \mathrm{~V}<\mathrm{V}<26 \mathrm{~V}$, I I OUT $=1.0 \mathrm{~mA}$ | - | 5 | 50 | mV |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) | $\begin{aligned} & \mathrm{l}_{\text {OUT }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {IN }}=12 \mathrm{~V} \\ & \mathrm{l}_{\text {OUT }} \leq 50 \mathrm{~mA} \\ & \mathrm{l}_{\text {OUT }} \leq 100 \mathrm{~mA} \end{aligned}$ | - | $\begin{gathered} 450 \\ 4 \\ 12 \end{gathered}$ | $\begin{gathered} 750 \\ 6 \\ 20 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple Rejection | $7.0 \mathrm{~V} \leq \mathrm{VI}_{\mathrm{N}} \leq 17 \mathrm{~V}$, Iout $=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ | 60 | 75 | - | dB |
| Current Limit | - | 105 | 200 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 25 | 125 | - | mA |
| Thermal Shutdown (Note 2) | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT }} \leq 1.0 \mathrm{~V}$ | 28 | 32 | 36 | V |

2. This parameter is guaranteed by design, but not parametrically tested in production.

## PACKAGE LEAD DESCRIPTION

| Package Lead Number |  |  |
| :---: | :---: | :--- |
| SO-8 | Lead Symbol |  |
| 1 | $\mathrm{~V}_{\text {OUT }}$ | $5.0 \mathrm{~V}, \pm 2 \%, 100 \mathrm{~mA}$ output. |
| 4,5 | NC | No connection. |
| $2,3,6,7$ | GND | Ground. |
| 8 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Load Regulation vs. Output Current $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$


Figure 4. Line Regulation vs. Input Voltage lout $=100 \mu \mathrm{~A}$


Figure 6. Quiescent Current vs. Output Current $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$


Figure 3. Output Voltage vs. Temperature $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$


Figure 5. Quiescent Current vs. Output Current (Lightly Loaded) $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$


Figure 7. Quiescent Current vs. Input Voltage $I_{\text {OUt }}=100 \mu \mathrm{~A}$

## CIRCUIT DESCRIPTION

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 8).

If the input voltage rises above 32 V (typ), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.


Figure 8. Typical Circuit Waveforms for Output Stage Protection


* C 1 is required if regulator is distant from power source filter.

Figure 9. Application and Test Diagram

## APPLICATION NOTES

## STABILITY CONSIDERATIONS / NOCAP

Normally a low dropout or quasi-low dropout regulator (or any type requiring a slow lateral PNP in the control loop) necessitates a large external compensation capacitor at the output of the IC. The external capacitor is also used to curtail overshoot, determine startup delay time and load transient response.

Traditional LDO regulators typically have low unity gain bandwidth, display overshoot and poor ripple rejection. Compensation is also an issue and depends on the external capacitor value, ESR (Equivalent Series Resistance) and board layout parasitics that all can create oscillations if not properly accounted for.

NOCAP is an ON Semiconductor exclusive output stage which internally compensates the LDO regulator over temperature, load and line variations without the need for an expensive external capacitor
NOCAP is ideally suited for slow switching or steady loads. If the load is characterized by transient current events, an output storage capacitor may be needed. If this is the case, the capacitor should be no larger than 100 nF . With loads that require greater transient suppression, a regulator with a traditional output stage (such as the CS8221) may be better suited for proper operation.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 10) is:

$$
\begin{align*}
P_{D(\max )}= & \left\{V_{\operatorname{IN}(\max )}-\mathrm{V}_{\text {OUT }}(\min )\right\} \operatorname{IOUT}(\max ) \\
& +\mathrm{V}_{\operatorname{IN}(\max )} \mathrm{I} \mathrm{Q} \tag{1}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{A}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$



Figure 10. Single output regulator with key performance parameters labeled.

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \mathrm{JA}}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $\mathrm{R}_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## CS9202

## Micropower 3.3 V, 100 mA <br> Low Dropout Linear Regulator with NOCAPTM

The CS9202 is a precision $3.3 \mathrm{~V}, 100 \mathrm{~mA}$ voltage regulator with low quiescent current ( $450 \mu \mathrm{~A}$ typ. @ $100 \mu \mathrm{~A}$ load). The 3.3 V output is accurate within $\pm 2 \%$ and supplies 100 mA of load current.

The regulator is protected against reverse battery, short circuit, over voltage, and over temperature conditions. The device can withstand 74 V peak transients making it suitable for use in automotive environments. ON's proprietary NOCAP solution is the first technology which allows the output to be stable without the use of an external capacitor. NOCAP is suitable for slow switching or steady loads.

## Features

- NOCAP
- Low Quiescent Current ( $450 \mu \mathrm{~A}$ typ. @ $100 \mu \mathrm{~A}$ load)
- $3.3 \mathrm{~V}, \pm 2 \%$ Output
- 100 mA Output Current Capability
- Fault Protection
- 74 V Peak Transient Voltage
- -15 V Reverse Voltage
- Short Circuit
- Thermal Shutdown
- Overvoltage Shutdown
- Internally Fused Leads

(1) Contact factory for optional Sense lead.


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS9202YDF8 | SO-8 | 95 Units/Rail |
| CS9202YDFR8 | SO-8 | 2500 Tape \& Reel |

Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Dissipation |  | Internally Limited | - |
| Input Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ): <br> DC <br> Peak Transient Voltage ( 60 V Load Dump @ $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$ ) |  | $\begin{gathered} -15 \text { to } 36 \\ 74 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Output Current |  | Internally Limited | - |
| ESD Susceptibility (Human Body Model) |  | 4.0 | kV |
| Package Thermal Resistance: <br> Junction-to-Case, R $\mathrm{R}_{\text {日J }}$ Junction-to-Ambient, R $\mathrm{R}_{\text {JA }}$ |  | $\begin{gathered} 25 \\ 110 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Junction Temperature |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow (SMD styles only) Note 1 | 230 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS $\left(4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, I $\mathrm{I}_{\mathrm{OUT}}=1.0 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Output Voltage, $\mathrm{V}_{\text {OUT }}$ | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mathrm{uA} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA} \\ & 4.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}, 100 \mathrm{uA} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 3.234 \\ & 3.201 \end{aligned}$ | $\begin{aligned} & 3.300 \\ & 3.300 \end{aligned}$ | $\begin{aligned} & 3.366 \\ & 3.399 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA}$ | - | 5 | 50 | mV |
| Line Regulation | $4.5 \mathrm{~V}<\mathrm{V}<26 \mathrm{~V}$, I IOUT $=1.0 \mathrm{~mA}$ | - | 5 | 50 | mV |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) | $\begin{aligned} & \text { loUt }=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{IN}}=12 \mathrm{~V} \\ & \text { lout } \leq 50 \mathrm{~mA} \\ & \text { lout } \leq 100 \mathrm{~mA} \end{aligned}$ | - | $\begin{gathered} 450 \\ 4 \\ 12 \end{gathered}$ | $\begin{gathered} 750 \\ 6 \\ 20 \end{gathered}$ | $\mu \mathrm{A}$ <br> mA <br> mA |
| Ripple Rejection | 7.0 V $\leq \mathrm{VI}_{\mathrm{N}} \leq 17 \mathrm{~V}, \mathrm{l}_{\text {OUT }}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ | 60 | 75 | - | dB |
| Current Limit | - | 105 | 200 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 25 | 125 | - | mA |
| Thermal Shutdown (Note 2) | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT }} \leq 1.0 \mathrm{~V}$ | 28 | 32 | 36 | V |

2. This parameter is guaranteed by design, but not parametrically tested in production.

## PACKAGE LEAD DESCRIPTION

| Package Lead Number |  |  |
| :---: | :---: | :--- |
| SO-8 | Lead Symbol |  |
| 1 | $\mathrm{~V}_{\text {OUT }}$ | Function |
| $2,3,6,7$ | GND | Ground. |
| 4,5 | NC | No connection. |
| 8 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 2. Load Regulation vs. Output Current $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$


Figure 4. Line Regulation vs. Input Voltage lout $=100 \mu \mathrm{~A}$


Figure 6. Quiescent Current vs. Output
Current $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$


Figure 3. Output Voltage vs. Temperature

$$
\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}
$$



Figure 5. Quiescent Current vs. Output Current (Lightly Loaded) $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$


Figure 7. Quiescent Current vs. Input Voltage lout $=100 \mu \mathrm{~A}$

## CIRCUIT DESCRIPTION

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 8).

If the input voltage rises above 32 V (typ), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.


Figure 8. Typical Circuit Waveforms for Output Stage Protection


* C 1 is required if regulator is distant from power source filter.

Figure 9. Application and Test Diagram

## APPLICATION NOTES

## STABILITY CONSIDERATIONS / NOCAP

Normally a low dropout or quasi-low dropout regulator (or any type requiring a slow lateral PNP in the control loop) necessitates a large external compensation capacitor at the output of the IC. The external capacitor is also used to curtail offshoot, determine startup delay time and load transient response.

Traditional LDO regulators typically have low unity gain bandwidth, display overshoot and poor ripple rejection. Compensation is also an issue and depends on the external capacitor value, ESR (Equivalent Series Resistance) and board layout parasitics that all can create oscillations if not properly accounted for.

NOCAP is an ON Semiconductor exclusive output stage which internally compensates the LDO regulator over temperature, load and line variations without the need for an expensive external capacitor
NOCAP is ideally suited for slow switching or steady loads. If the load is characterized by transient current events, an output storage capacitor may be needed. If this is the case, the capacitor should be no larger than 100 nF . With loads that require greater transient suppression, a regulator with a traditional output stage (such as the CS8221) may be better suited for proper operation.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 10) is:

$$
\begin{align*}
P_{D(\max )}= & \left\{V_{\operatorname{IN}(\max )}-\mathrm{V}_{\text {OUT }}(\min )\right\} \operatorname{IOUT}(\max ) \\
& +\mathrm{V}_{\operatorname{IN}(\max )} \mathrm{I} \mathrm{Q} \tag{1}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \text { JA }}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{A}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$



Figure 10. Single output regulator with key performance parameters labeled.

The value of $\mathrm{R}_{\Theta J A}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta J A}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $\mathrm{R}_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## 100 mA, 5.0 V, Low Dropout Voltage Regulator with Power-On Reset

The L4949 is a monolithic integrated 5.0 V voltage regulator with a very low dropout and additional functions such as power-on reset and input voltage sense.

It is designed for supplying the micro-computer controlled systems especially in automotive applications.

- Operating DC Supply Voltage Range 5.0 V to 28 V
- Transient Supply Voltage Up to 40 V
- Extremely Low Quiescent Current in Standby Mode
- High Precision Standby Output Voltage $5.0 \mathrm{~V} \pm 1 \%$
- Output Current Capability Up to 100 mA
- Very Low Dropout Voltage Less Than 0.4 V
- Reset Circuit Sensing The Output Voltage
- Programmable Reset Pulse Delay With External Capacitor
- Voltage Sense Comparator
- Thermal Shutdown and Short Circuit Protections


## MULTIFUNCTION VERY LOW DROPOUT VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT


N SUFFIX PLASTIC PACKAGE

CASE 626


D SUFFIX PLASTIC PACKAGE CASE 751

Representative Block Diagram


PIN CONNECTIONS

(Top View)


ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| DC Operating Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 28 | V |
| Transient Supply Voltage ( t < 1.0 s ) | $V_{C C T}$ TR | 40 | V |
| Output Current | $\mathrm{I}_{\text {out }}$ | Internally Limited | - |
| Output Voltage | $V_{\text {out }}$ | 20 | V |
| Sense Input Current | $\mathrm{I}_{\mathrm{S}}$ | $\pm 1.0$ | mA |
| Sense Input Voltage | $\mathrm{V}_{\text {SI }}$ | $\mathrm{V}_{\mathrm{CC}}$ | - |
| Output Voltages Reset Output Sense Output | $V_{\text {Reset }}$ <br> $\mathrm{V}_{\mathrm{SO}}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ | V |
| Output Currents Reset Output Sense Output | $\begin{aligned} & I_{\text {Reset }} \\ & I_{\text {So }} \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | mA |
| Preregulator Output Voltage | $\mathrm{V}_{\mathrm{Z}}$ | 7.0 | V |
| Preregulator Output Current | Iz | 5.0 | mA |
| ESD Protection at any pin Human Body Model Machine Model | - | $\begin{gathered} 2000 \\ 400 \end{gathered}$ | V |
| Thermal Resistance, Junction-to-Air P Suffix, DIP-8 Plastic Package, Case 626 D Suffix, SO-8 Plastic Package, Case 751 | $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 100 \\ & 200 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Maximum Junction Temperature | TJ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$, unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\left.\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}\right)$ | $V_{\text {out }}$ | 4.95 | 5.0 | 5.05 | V |
| Output Voltage ( $6.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<28 \mathrm{~V}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<50 \mathrm{~mA}$ ) | $V_{\text {out }}$ | 4.9 | 5.0 | 5.1 | V |
| Output Voltage ( $\left.\mathrm{V}_{\mathrm{CC}}=35 \mathrm{~V}, \mathrm{t}<1.0 \mathrm{~s}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<50 \mathrm{~mA}\right)$ | $V_{\text {out }}$ | 4.9 | 5.0 | 5.1 | V |
| Dropout Voltage $\begin{aligned} & \mathrm{I}_{\text {out }}=10 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=50 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=100 \mathrm{~mA} \end{aligned}$ | $V_{\text {drop }}$ |  | $\begin{aligned} & 0.1 \\ & 0.2 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 0.40 \\ & 0.50 \end{aligned}$ | V |
| Input to Output Voltage Difference in Undervoltage Condition $\left(\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=35 \mathrm{~mA}\right)$ | $\mathrm{V}_{10}$ | - | 0.2 | 0.4 | V |
| Line Regulation ( $6.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<28 \mathrm{~V}$, $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 20 | mV |
| Load Regulation ( $1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<100 \mathrm{~mA}$ ) | Regload | - | 8.0 | 30 | mV |
| $\begin{gathered} \text { Current Limit } \\ V_{\text {out }}=4.5 \mathrm{~V} \\ \mathrm{~V}_{\text {out }}=0 \mathrm{~V} \end{gathered}$ | Lim | $105$ | $\begin{aligned} & 200 \\ & 100 \end{aligned}$ | $400$ | mA |
| Quiescent Current ( $\mathrm{l}_{\text {out }}=0.3 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}<100^{\circ} \mathrm{C}$ ) | IQSE | - | 150 | 260 | $\mu \mathrm{A}$ |
| Quiescent Current ( $\mathrm{l}_{\text {out }}=100 \mathrm{~mA}$ ) | $\mathrm{I}_{\mathrm{Q}}$ | - | - | 5.0 | mA |

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{J}<125^{\circ} \mathrm{C}\right.$, unless otherwise specified.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESET |  |  |  |  |  |
| Reset Threshold Voltage | $V_{\text {Resth }}$ | - | $\mathrm{V}_{\text {out }}-0.5$ | - | V |
| Reset Threshold Hysteresis <br> @ $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ <br> @ $\mathrm{T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ | $\mathrm{V}_{\text {Resth,hys }}$ | $\begin{aligned} & 50 \\ & 50 \end{aligned}$ | 100 - | $\begin{aligned} & 200 \\ & 300 \end{aligned}$ | mV |
| Reset Pulse Delay ( $\mathrm{C}_{\mathrm{T}}=100 \mathrm{nF}, \mathrm{t}_{\mathrm{R}} \geq 100 \mu \mathrm{~s}$ ) | $t_{\text {ResD }}$ | 55 | 100 | 180 | ms |
| Reset Reaction Time ( $\mathrm{C}_{\mathrm{T}}=100 \mathrm{nF}$ ) | $t_{\text {ResR }}$ | - | 5.0 | 30 | $\mu \mathrm{s}$ |
| Reset Output Low Voltage ( $\mathrm{R}_{\text {Reset }}=10 \mathrm{k} \Omega$ to $\mathrm{V}_{\text {out }}, \mathrm{V}_{\mathrm{CC}} \geq 3.0 \mathrm{~V}$ ) | $V_{\text {ResL }}$ | - | - | 0.4 | V |
| Reset Output High Leakage Current ( $\mathrm{V}_{\text {Reset }}=5.0 \mathrm{~V}$ ) | $\mathrm{I}_{\text {ResH }}$ | - | - | 1.0 | $\mu \mathrm{A}$ |
| Delay Comparator Threshold | $\mathrm{V}_{\text {cTth }}$ | - | 2.0 | - | V |
| Delay Comparator Threshold Hysteresis | $\mathrm{V}_{\text {CTth, hys }}$ | - | 100 | - | mV |

SENSE

| Sense Low Threshold $\left(\mathrm{V}_{\mathrm{SI}}\right.$ Decreasing $=1.5 \mathrm{~V}$ to 1.0 V$)$ | $\mathrm{V}_{\text {SOth }}$ | 1.16 | 1.23 | 1.35 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Sense Threshold Hysteresis | $\mathrm{V}_{\text {SOth,hys }}$ | 20 | 100 | 200 | mV |
| Sense Output Low Voltage $\left(\mathrm{V}_{\mathrm{SI}} \leq 1.16 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}} \geq 3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{SO}}=10 \mathrm{k} \Omega\right.$ to $\left.\mathrm{V}_{\text {out }}\right)$ | $\mathrm{V}_{\text {SOL }}$ | - | - | 0.4 | V |
| Sense Output Leakage $\left(\mathrm{V}_{\mathrm{SO}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{SI}} \geq 1.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{SOH}}$ | - | - | 1.0 | $\mu \mathrm{~A}$ |
| Sense Input Current | $\mathrm{I}_{\mathrm{SI}}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{~A}$ |

PREREGULATOR

| Preregulator Output Voltage $\left(I_{Z}=10 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{Z}}$ | - | 6.3 | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |

## PIN FUNCTION DESCRIPTION

| Pin | Symbol |  |
| :---: | :--- | :--- |
| 1 | $\mathrm{~V}_{\mathrm{CC}}$ | Supply Voltage |
| 2 | $\mathrm{~S}_{\mathrm{i}}$ | Input of Sense Comparator |
| 3 | $\mathrm{~V}_{\mathrm{Z}}$ | Output of Preregulator |
| 4 | $\mathrm{C}_{\mathrm{T}}$ | Reset Delay Capacitor |
| 5 | Gnd | Ground |
| 6 | Reset | Output of Reset Comparator |
| 7 | $\mathrm{~S}_{\mathrm{O}}$ | Output of Sense Comparator |
| 8 | $\mathrm{~V}_{\text {out }}$ | Main Regulator Output |

TYPICAL CHARACTERIZATION CURVES


Figure 1. Output Voltage versus Junction Temperature


Figure 2. Output Voltage versus Supply Voltage

## TYPICAL CHARACTERIZATION CURVES (continued)



Figure 3. Dropout Voltage versus Output Current


Figure 5. Quiescent Current versus Output Current


Figure 7. Reset Output versus Regulator Output Voltage


Figure 4. Dropout Voltage versus Junction Temperature


Figure 6. Quiescent Current versus Supply Voltage


Figure 8. Reset Thresholds versus Junction Temperature

TYPICAL CHARACTERIZATION CURVES (continued)


Figure 9. Sense Output versus Sense Input Voltage


Figure 10. Sense Thresholds versus Junction Temperature

## APPLICATION INFORMATION

## Supply Voltage Transient

High supply voltage transients can cause a reset output signal perturbation. For supply voltages greater than 8.0 V the circuit shows a high immunity of the reset output against supply transients of more than $100 \mathrm{~V} / \mu \mathrm{s}$. For supply voltages
less than 8.0 V supply transients of more than $0.4 \mathrm{~V} / \mu \mathrm{s}$ can cause a reset signal perturbation. To improve the transient behavior for supply voltages less than 8.0 V a capacitor at Pin 3 can be used. A capacitor at Pin $3(\mathrm{C} 3 \leq 1.0 \mu \mathrm{~F})$ reduces also the output noise.


Figure 11. Application Schematic

## OPERATING DESCRIPTION

The L4949 is a monolithic integrated low dropout voltage regulator. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows the use of other features and functions independently when required.

## Voltage Regulator

The voltage regulator uses an isolated Collector Vertical PNP transistor as a regulating element. With this structure, very low dropout voltage at currents up to 100 mA is obtained. The dropout operation of the standby regulator is maintained down to 3.0 V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 35 V . With this feature no functional interruption due to overvoltage pulses is generated.

The typical curve showing the standby output voltage as a function of the input supply voltage is shown in Figure 13.

The current consumption of the device (quiescent current) is less than $200 \mu \mathrm{~A}$.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled. The quiescent current as a function of the supply input voltage is shown in Figure 14.

## Short Circuit Protection:

The maximum output current is internally limited. In case of short circuit, the output current is foldback current limited as described in Figure 12.


Figure 12. Foldback Characteristic of $\mathrm{V}_{\text {out }}$


Figure 13. Output Voltage versus Supply Voltage


Figure 14. Quiescent Current versus Supply Voltage

## Preregulator

To improve the transient immunity a preregulator stabilizes the internal supply voltage to 6.0 V . This internal voltage is present at Pin $3\left(\mathrm{~V}_{\mathrm{Z}}\right)$. This voltage should not be used as an output because the output capability is very small $(\leq 100 \mu \mathrm{~A})$.

This output may be used as an option when better transient behavior for supply voltages less than 8.0 V is required. In this case a capacitor $(100 \mathrm{nF}-1.0 \mu \mathrm{~F})$ must be connected between Pin 3 and Gnd. If this feature is not used Pin 3 must be left open.

## Reset Circuit

The block circuit diagram of the reset circuit is shown in Figure 15.

The reset circuit supervises the output voltage. The reset threshold of 4.5 V is defined with the internal reference voltage and standby output divider.

The reset pulse delay time $\mathrm{t}_{\mathrm{RD}}$, is defined with the charge time of an external capacitor $\mathrm{C}_{\mathrm{T}}$ :

$$
\mathrm{t}_{\mathrm{RD}}=\frac{\mathrm{C}_{\mathrm{T}} \times 2.0 \mathrm{~V}}{2.0 \mu \mathrm{~A}}
$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor $\mathrm{C}_{\mathrm{T}}$ and is proportional to the value of $\mathrm{C}_{\mathrm{T}}$. The reaction time of the reset circuit increases the noise immunity.


Figure 15. Reset Circuit

Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for standby output voltage drops longer than approximately $50 \mu \mathrm{~s}$. The typical reset output waveforms are shown in Figure 16.


Figure 16. Typical Reset Output Waveforms

## Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23 V . The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after the protection diode and to give additional information to the microprocessor like low voltage warnings.

## CS8311

## Micropower 10 V, 100 mA <br> Low Dropout Linear Regulator with RESET and ENABLE

The CS8311 is a precision 10 V micropower voltage regulator with very low quiescent current ( $100 \mu \mathrm{~A}$ typ at $100 \mu \mathrm{~A}$ load). The 10 V output is accurate within $\pm 4.0 \%$ and supplies 100 mA of load current with a typical dropout voltage of only 400 mV . Microprocessor control logic includes an $\overline{\text { ENABLE }}$ input and an active $\overline{\text { RESET. }}$

The active $\overline{\text { RESET }}$ circuit includes hysteresis, and operates correctly at an output voltage as low as 1.0 V . The $\overline{\text { RESET }}$ function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits by more than 1.0 V typ. The logic level compatible ENABLE input allows the user to put the regulator into a shutdown mode where it draws only $20 \mu \mathrm{~A}$ typical of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

## Features

- $10 \mathrm{~V} \pm 4.0 \%$ Output
- Low $100 \mu \mathrm{~A}$ Quiescent Current
- Active RESET
- ENABLE Input for ON/OFF and Active/Sleep Mode Control
- 100 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage
-     - 15 V Reverse Voltage Short Circuit Thermal Overload
- Low Reverse Current (Output to Input)
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|  | SO-8 |
| :---: | :---: |
| , | D SUFFIX |
| 8 | CASE 751 |

PIN CONNECTIONS AND MARKING DIAGRAM

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8311YD8 | SO-8 | 95 Units/Rail |
| CS8311YDR8 | SO-8 | 2500 Tape \& Reel |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| $\mathrm{V}_{\mathrm{IN}}$ |  | 38 |
| Peak Transient Voltage (46 V Load Dump @ $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$ ) | 60 | V |
| ENABLE, RESET | -0.3 to +10.4 | V |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| Junction Temperature Range | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | Reflow (SMD styles only) (Note 1$)$ | 230 peak |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $11 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$; $\mathrm{I}_{\mathrm{OUT}}=1.0 \mathrm{~mA} ;-40 \leq \mathrm{T}_{\mathrm{A}} \leq 125,-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$;
unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Output Voltage, $\mathrm{V}_{\text {OUT }}$ | $11 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 100 \mathrm{~mA}$ | 9.60 | 10.00 | 10.40 | V |
| Dropout Voltage ( $\left.\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right)$ | $\begin{aligned} & \text { IOUT }=100 \mathrm{~mA} \\ & \text { IOUT }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA}$ | - | 5.0 | 100 | mV |
| Line Regulation | $11 \mathrm{~V}<\mathrm{V}<26 \mathrm{~V}$, lout $=1.0 \mathrm{~mA}$ | - | 5.0 | 100 | mV |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) Active Mode | $\begin{aligned} & \text { lout }=100 \mu \mathrm{~A} \\ & \text { lout }=50 \mathrm{~mA} \\ & \text { lout }=100 \mathrm{~mA} \end{aligned}$ |  | $\begin{gathered} 100 \\ 4.0 \\ 12 \end{gathered}$ | $\begin{aligned} & 250 \\ & 6.0 \\ & 20 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Quiescent Current, (1Q) Sleep Mode | $\mathrm{V}_{\text {OUT }}=\mathrm{OFF}, \mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {ENABLE }}=2.0 \mathrm{~V}$ | - | 20 | 50 | $\mu \mathrm{A}$ |
| Ripple Rejection | $14 \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, \mathrm{l}_{\text {OUT }}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ | 60 | 75 | - | dB |
| Current Limit | - | 105 | 200 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 25 | 125 | - | mA |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT }} \leq 1.0 \mathrm{~V}$ | 30 | 34 | 38 | V |
| Reverse Current | $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 250 | $\mu \mathrm{A}$ |

ENABLE Input (ENABLE)

| Threshold High | $\left(\mathrm{V}_{\text {OUT }}\right.$ OFF $)$ | - | 1.4 | 2.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Threshold Low | $\left(\mathrm{V}_{\text {OUT }}\right.$ ON $)$ | 0.6 | 1.4 | - | V |
| Input Current | $\mathrm{V}_{\overline{\text { ENABLE }}}=2.4 \mathrm{~V}$ | - | 30 | 100 | $\mu \mathrm{~A}$ |

## Reset Function (RESET)

| RESET Threshold High ( $\mathrm{V}_{\mathrm{RH}}$ ) | V OUT Increasing | 8.50 | 9.00 | $\mathrm{V}_{\text {OUT }}-0.50$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESET Threshold Low ( $\mathrm{V}_{\mathrm{RL}}$ ) | $V_{\text {Out }}$ Decreasing | 8.30 | 8.90 | $\mathrm{V}_{\text {OUT }}-0.45$ | V |
| RESET Hysteresis | (High - Low) | 50 | 100 | 200 | mV |
| Reset Output Leakage RESET $=$ High | $\mathrm{V}_{\text {OUT }} \geq \mathrm{V}_{\text {RH }}$ | - | - | 25 | $\mu \mathrm{A}$ |
| Output Voltage Low (V $\mathrm{V}_{\text {RLO }}$ ) | $\mathrm{R}_{\text {RESET }}=10 \mathrm{k}, 1.0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq \mathrm{V}_{\text {RL }}$ | - | 0.1 | 0.4 | V |
| Output Voltage Low (VR PEAK) | $\overline{R_{\text {RESET }}}=10 \mathrm{k}, \mathrm{~V}_{\text {OUT }},$ <br> Power up, Power down | - | 0.6 | 1.0 | V |

PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :--- |
| SO-8 | LEAD SYMBOL |  |
| 1 | V $_{\text {OUT }}$ | $10 \mathrm{~V}, \pm 4.0 \%, 100 \mathrm{~mA}$ output. |
| 2 | V $_{\text {OUT }}$ Sense | Kelvin connection which allows remote sensing of output voltage for improved <br> regulation. If remote sensing is not required, connect to $\mathrm{V}_{\text {OUT. }}$ |
| 3 | ENABLE | Logic level switches output off when toggled HIGH. |
| 4 | GND | Ground. All GND leads must be connected to Ground. |
| 5 | RESET | Active reset (accurate to $\mathrm{V}_{\text {OUT }} \geq 1.0 \mathrm{~V}$ ). |
| 6,7 | NC | No connection. |
| 8 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |

## CIRCUIT DESCRIPTION

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 2).


Figure 2. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients

Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the load current capability is reduced thereby preventing thermal overload. This thermal management function is an effective means to prevent die overheating since the load current is the principle heat source in the IC.

REGULATOR CONTROL FUNCTIONS
The CS8311 contains two microprocessor compatible control functions: $\overline{\mathrm{ENABLE}}$ and $\overline{\mathrm{RESET}}$ (Figure 3).

(1) $=$ No Reset Delay Capacitor
(2) = With Reset Delay Capacitor

## ENABLE Function

The ENABLE function switches the output transistor ON and OFF. When the voltage on the $\overline{\text { ENABLE }}$ lead exceeds 1.4 V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only $50 \mu \mathrm{~A}$ (max), until the voltage on this input drops below the $\overline{\mathrm{ENABLE}}$ threshold.

## RESET Function

A $\overline{\mathrm{RESET}}$ signal (low voltage) is generated as the IC powers up until $\mathrm{V}_{\text {OUT }}$ is within 1.0 V of the regulated output voltage, or when $V_{\text {OUT }}$ drops out of regulation, and is lower than 1.1 V below the regulated output voltage. A hysteresis of 50 mV is included in the function to minimize oscillations.
The RESET output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text { RESET }}$ signal is valid for $\mathrm{V}_{\text {OUT }}$ as low as 1.0 V .


Figure 4. RC Network for RESET Delay
An external RC network on the lead (Figure 4) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$
\text { RTOTCRST }=\left[\frac{t_{\text {Delay }}}{\ln \left(\frac{V_{T}-V_{\text {OUT }}}{V_{\text {RST }}-V_{\text {OUT }}}\right)}\right]
$$

where:
$\mathrm{R}_{\mathrm{RST}}=\overline{\mathrm{RESET}}$ Delay resistor
$\mathrm{R}_{\mathrm{IN}}=\mu \mathrm{P}$ port impedance
$\mathrm{R}_{\mathrm{TOT}}=\mathrm{R}_{\mathrm{RST}}$ in parallel with $\mathrm{R}_{\mathrm{IN}}$
$\mathrm{C}_{\mathrm{RST}}=\overline{\mathrm{RESET}}$ Delay capacitor
$t_{\text {Delay }}=$ desired delay time
$\mathrm{V}_{\mathrm{RST}}=\mathrm{V}_{\mathrm{SAT}}$ of $\overline{\mathrm{RESET}}$ lead ( 0.7 V @ turn -ON )
$\mathrm{V}_{\mathrm{T}}=\overline{\mathrm{RESET}}$ threshold.

Figure 3. Circuit Waveform

## APPLICATION NOTES



Figure 5. Microprocessor Control of CS8311 Using External Switching Transistor Q1

The circuit depicted in Figure 5 lets the system control its power source, the CS8311 regulator. A SWITCH (potentially an I/O port on microprocessor) is used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the $\overline{\text { ENABLE }}$ lead falls below its lower threshold. The regulator's output is enabled. When the drive current is removed, the voltage on the $\overline{\text { ENABLE }}$ lead rises, the output is switched off and the IC moves into Sleep mode where it draws $50 \mu \mathrm{~A}$ (max).

By coupling these two controls with the ENABLE lead, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The microprocessor can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port allows the microprocessor to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1.
Table 1. Logic Control of CS8311 Output

| Microprocessor <br> I/O Drive | Switch | ENABLE | Output |
| :---: | :---: | :---: | :---: |
| ON | Closed | LOW | ON |
|  | Open | LOW | ON |
| OFF | Closed | LOW | ON |
|  | Open | HIGH | OFF |

The I/O port of the microprocessor typically provides $50 \mu \mathrm{~A}$ to Q1. In automotive applications the SWITCH is connected to the ignition switch.

STABILITY CONSIDERATIONS
The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

${ }^{*} \mathrm{C}_{\mathrm{IN}}$ required if regulator is located far from the power supply filter.
*COUT required for stability. Capacitor must operate at minimum temperature expected.

Figure 6. Test and Application Circuit Showing Output Compensation
The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.
The value for the output capacitor Cout shown in Figure 6 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for Cout for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 7) is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
$\mathrm{I}_{\mathrm{OUT}(\max )}$ is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
R_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta J A}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 7. Single Output Regulator With Key Performance Parameters Labeled

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## CS8311

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 45 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 165 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8101

## Micropower 5.0 V, 100 mA Low Dropout Linear Regulator with RESET and ENABLE

The CS8101 is a precision 5.0 V micropower voltage regulator with very low quiescent current ( $70 \mu \mathrm{~A}$ typ at $100 \mu \mathrm{~A}$ load). The 5.0 V output is accurate within $\pm 2.0 \%$ and supplies 100 mA of load current with a typical dropout voltage of only 400 mV . Microprocessor control logic includes an $\overline{\text { ENABLE }}$ input and an active $\overline{\text { RESET. This }}$ combination of low quiescent current, outstanding regulator performance and control logic makes the CS8101 ideal for any battery operated, microprocessor controlled equipment.

The active $\overline{\text { RESET }}$ circuit includes hysteresis, and operates correctly at an output voltage as low as 1.0 V . The RESET function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits by more than 200 mV typ. The logic level compatible ENABLE input allows the user to put the regulator into a shutdown mode where it draws only $20 \mu \mathrm{~A}$ typical of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

The CS8101 is functionally equivalent to the National Semiconductor LP2951 series low current regulators.

## Features

- $5.0 \mathrm{~V} \pm 2.0 \%$ Output
- Low $70 \mu \mathrm{~A}$ Quiescent Current
- Active RESET
- ENABLE Input for ON/OFF and Active/Sleep Mode Control
- 100 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage
-     - 15 V Reverse Voltage Short Circuit Thermal Overload
- Low Reverse Current (Output to Input)
- Internally Fused Leads Available in SO-20L Package


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## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 393 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 393 of this data sheet.


Figure 1. Block Diagram

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Dissipation |  | Internally Limited | - |
| Peak Transient Voltage (46 V Load Dump @ V ${ }_{\text {IN }}=14 \mathrm{~V}$ ) |  | -15, 60 | V |
| Output Current |  | Internally Limited | - |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Operating Temperature |  | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2) | 260 peak <br> 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (6.0 V $\leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V} ; \mathrm{l}_{\mathrm{OUT}}=1.0 \mathrm{~mA} ;-40 \leq \mathrm{T}_{\mathrm{A}} \leq 125,-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$,
unless otherwise noted.)

| Characteristic | Test Conditions | Min | Typ | Max |
| :---: | :---: | :---: | :---: | :---: |

## Output Stage

| Output Voltage, V $\mathrm{V}_{\text {OUT }}$ | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA} \\ & 6.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.90 \\ & 4.85 \end{aligned}$ | $\begin{aligned} & 5.00 \\ & 5.00 \end{aligned}$ | $\begin{aligned} & 5.10 \\ & 5.15 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\begin{aligned} & \text { lout }=100 \mathrm{~mA} \\ & \text { lout }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Line Regulation | $6.0<\mathrm{V}<26 \mathrm{~V}$, $\mathrm{l}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) Active Mode | $\begin{aligned} & \text { IOUT }=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {IN }}=6.0 \mathrm{~V} \\ & \text { IOUT }=50 \mathrm{~mA} \\ & \text { IOUT }=100 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 70 \\ & 4.0 \\ & 12 \end{aligned}$ | $\begin{aligned} & 140 \\ & 6.0 \\ & 20 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) Sleep Mode | $\mathrm{V}_{\text {OUT }}=O F F, \mathrm{~V}_{\text {IN }}=6.0 \mathrm{~V}, \mathrm{~V}_{\text {ENABLE }}=2.0 \mathrm{~V}$ | - | 20 | 50 | $\mu \mathrm{A}$ |
| Ripple Rejection | $7.0 \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=100 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ | 60 | 75 | - | dB |
| Current Limit | - | 105 | 200 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 25 | 125 | - | mA |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT }} \leq 1.0 \mathrm{~V}$ | 30 | 34 | 38 | V |
| Reverse Current | $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 200 | $\mu \mathrm{A}$ |

ENABLE Input (ENABLE)

| Threshold HIGH LOW | (V Vut OFF) <br> (VOUT ON) | $\overline{-}$ | $\begin{aligned} & 1.4 \\ & 1.4 \end{aligned}$ | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Current | $V_{\text {ENABLE }}=2.4 \mathrm{~V}$ | - | 30 | 100 | $\mu \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS (continued) $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I}} \leq 26 \mathrm{~V}\right.$; $\mathrm{l}_{\text {OUT }}=1.0 \mathrm{~mA} ;-40 \leq \mathrm{T}_{\mathrm{A}} \leq 125,-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Reset Functions (RESET)

| $\begin{aligned} & \text { RESET Threshold } \\ & \text { HIGH }\left(\mathrm{V}_{\mathrm{RH}}\right) \\ & \text { LOW }\left(\mathrm{V}_{\mathrm{RL}}\right) \end{aligned}$ | $V_{\text {OUT }}$ Increasing <br> $V_{\text {OUT }}$ Decreasing | $\begin{aligned} & 4.525 \\ & 4.500 \end{aligned}$ | $\begin{aligned} & 4.75 \\ & 4.70 \end{aligned}$ | $\begin{gathered} \mathrm{V}_{\text {OUT }}-0.05 \\ \text { VOUT }-0.075 \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESET Hysteresis | (HIGH - LOW) | 25 | 50 | 100 | mV |
| Reset Output Leakage RESET $=$ HIGH | $\mathrm{V}_{\text {OUT }} \geq \mathrm{V}_{\text {RH }}$ | - | - | 25 | $\mu \mathrm{A}$ |
| Output Voltage Low (VRLO) Low (VRPEAK) | $\begin{aligned} & 1.0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq \mathrm{V}_{\text {RL, }} \overline{R_{\text {RESET }}}=10 \mathrm{k} \\ & \text { V Out, Power up, Power down, }_{\text {R }}^{\text {RESET }}=10 \mathrm{k} \end{aligned}$ | - | $\begin{aligned} & 0.1 \\ & 0.6 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 1.0 \end{aligned}$ | V |

PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  |  | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { TO-220 } \\ & 5 \text { LEAD } \end{aligned}$ | SO-20L | SO-8 | LEAD SYMBOL |  |
| 1 | 20 | 1 | $V_{\text {OUT }}$ | $5.0 \mathrm{~V}, \pm 2.0 \%, 100 \mathrm{~mA}$ output. |
| - | - | 2 | $\mathrm{V}_{\text {OUT }}$ SENSE | Kelvin connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not required, connect to $\mathrm{V}_{\text {OUT }}$. |
| 2 | 1 | 3 | ENABLE | Logic level switches output off when toggled HIGH. |
| 3 | $\begin{gathered} 4,5,6,7 \\ 14,15,16,17 \end{gathered}$ | 4 | GND | Ground. All GND leads must be connected to Ground. |
| 4 | 10 | 5 | RESET | Active reset (accurate to $\mathrm{V}_{\text {OUT }} \geq 1.0 \mathrm{~V}$ ) |
| - | $\begin{gathered} 2,3,8,9,11 \\ 12,13,18 \end{gathered}$ | 6,7 | NC | No Connection. |
| 5 | 19 | 8 | $\mathrm{V}_{\text {IN }}$ | Input voltage. |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 2. CS8101 Dropout Voltage vs. Load Over Temperature

## CIRCUIT DESCRIPTION

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 3).


Figure 3. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the load current capability is reduced thereby preventing thermal overload. This thermal management function is an effective means to prevent die overheating since the load current is the principle heat source in the IC.

## REGULATOR CONTROL FUNCTIONS

The CS8101 contains two microprocessor compatible control functions: $\overline{\mathrm{ENABLE}}$ and $\overline{\mathrm{RESET}}$ (Figure 4).

(1) = No Reset Delay Capacitor
(2) $=$ With Reset Delay Capacitor

Figure 4. Circuit Waveform

## ENABLE Function

The $\overline{\text { ENABLE }}$ function switches the output transistor ON and OFF. When the voltage on the ENABLE lead exceeds 1.4 V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only $50 \mu \mathrm{~A}$, until the voltage on this input drops below the ENABLE threshold.

## RESET Function

A $\overline{\text { RESET }}$ signal (low voltage) is generated as the IC powers up until $\mathrm{V}_{\text {OUT }}$ is within 250 mV of the regulated output voltage, or when $\mathrm{V}_{\text {OUT }}$ drops out of regulation, and is lower than 300 mV below the regulated output voltage. A hysteresis of 50 mV is included in the function to minimize oscillations.

The $\overline{\text { RESET }}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text { RESET }}$ signal is valid for V VUT as low as 1.0 V .


Figure 5. RC Network for RESET Delay
An external RC network on the lead (Figure 5) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$
\text { RTOTCRST }=\left[\frac{- \text { tDelay }}{\ln \left(\frac{\mathrm{V}_{T}-\mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\text {RST }}-\mathrm{V}_{\text {OUT }}}\right)}\right]
$$

where:
$\mathrm{R}_{\text {RST }}=\overline{\mathrm{RESET}}$ Delay resistor
$\mathrm{R}_{\mathrm{IN}}=\mu \mathrm{P}$ port impedance
$\mathrm{R}_{\mathrm{TOT}}=\mathrm{R}_{\mathrm{RST}}$ in parallel with $\mathrm{R}_{\mathrm{IN}}$
$\mathrm{C}_{\mathrm{RST}}=\overline{\mathrm{RESET}}$ Delay capacitor
$t_{\text {Delay }}=$ desired delay time
$\mathrm{V}_{\mathrm{RST}}=\mathrm{V}_{\mathrm{SAT}}$ of $\overline{\mathrm{RESET}}$ lead ( 0.7 V @ turn -ON )
$\mathrm{V}_{\mathrm{T}}=\overline{\mathrm{RESET}}$ threshold.
The circuit depicted in Figure 6 lets the microprocessor control its power source, the CS8101 regulator. An I/O port on the $\mu \mathrm{P}$ and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the ENABLE lead falls below its lower threshold. The regulator's output is enabled. When the drive current is removed, the voltage on the ENABLE lead rises, the output is switched off and the IC moves into Sleep mode where it draws $50 \mu \mathrm{~A}$ (max).
By coupling these two controls with the ENABLE lead, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The microprocessor can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port allows the microprocessor to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1.
Table 1. Logic Control of CS8101 Output

| Microprocessor <br> I/O Drive | Switch | ENABLE | Output |
| :---: | :---: | :---: | :---: |
| ON | Closed | LOW | ON |
|  | Open | LOW | ON |
| OFF | Closed | LOW | ON |
|  | Open | HIGH | OFF |

The I/O port of the microprocessor typically provides $50 \mu \mathrm{~A}$ to Q1. In automotive applications the SWITCH is connected to the ignition switch.

## APPLICATION NOTES



Figure 6. Microprocessor Control of CS8101 Using External Switching Transistor Q1

## STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

${ }^{*} \mathrm{C}_{\mathrm{IN}}$ required if regulator is located far from the power supply filter.
*Cout required for stability. Capacitor must operate at minimum temperature expected.

Figure 7. Test and Application Circuit Showing Output Compensation

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor Cout shown in Figure 7 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for $\mathrm{C}_{\text {OUT }}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause
the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.
Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.
Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.
Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 8) is:
$P_{D}($ max $)=\left\{\mathrm{V}_{\mathrm{IN}(\text { max })}-\mathrm{V}_{\mathrm{OUT}(\text { min })} \mathrm{I}^{\mathrm{IOUT}(\text { max })}+\mathrm{V}_{\mathrm{IN}(\text { max })} \mathrm{I}_{\mathrm{Q}}\right.$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 8. Single Output Regulator With Key Performance Parameters Labeled

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \text { JA. }}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JJC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it is a function of package type. $\mathrm{R}_{\Theta C S}$ and $\mathrm{R}_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

ORDERING INFORMATION ${ }^{\dagger}$

| Device | Description | Shipping |
| :--- | :---: | :---: |
| CS8101YD8 | SO-8 | 95 Units/Rail |
| CS8101YDR8 | SO-8 | 2500 Tape \& Reel |
| CS8101YDWF20 | SO-20L | 37 Units/Rail |
| CS8101YDWFR20 | SO-20L | 1000 Tape \& Reel |
| CS8101YT5 | TO-220 FIVE LEAD STRAIGHT | 50 Units/Rail |
| CS8101YTVA5 | TO-220 FIVE LEAD VERTICAL | 50 Units/Rail |
| CS8101YTHA5 | TO-220 FIVE LEAD HORIZONTAL | 50 Units/Rail |

$\dagger$ Contact your local sales representative for D²PAK package option.


PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> FIVE LEAD | SO-8 | SO-20L | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 3.3 | 45 | 9.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | 165 | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8151

### 5.0 V, 100 mA Low Dropout Linear Regulator with Watchdog, RESET, and Wake Up

The CS8151 is a precision $5.0 \mathrm{~V}, 100 \mathrm{~mA}$ micro-power voltage regulator with very low quiescent current ( $400 \mu \mathrm{~A}$ typical at $200 \mu \mathrm{~A}$ load). The 5.0 V output is accurate within $\pm 2 \%$ and supplies 100 mA of load current with a typical dropout voltage of 400 mV . Microprocessor control logic includes Watchdog, Wake Up and RESET. This unique combination of low quiescent current and full microprocessor control makes the CS8151 ideal for use in battery operated, microprocessor controlled equipment.

The CS8151 Wake Up function brings the microprocessor out of Sleep mode. The microprocessor in turn, signals its Wake Up status back to the CS8151 by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The CS8151 responds to the falling edge of the Watchdog signal which it expects at least once during each wake-up period. When the correct Watchdog signal is received, a falling edge is issued on the wake-up signal line.
$\overline{\text { RESET }}$ is independent of $\mathrm{V}_{\text {IN }}$ and operates correctly to an output voltage as low as 1.0 V . A $\overline{\mathrm{RESET}}$ signal is issued in any of three situations. During power up the RESET is held low until the output voltage is in regulation. During operation if the output voltage shifts below the regulation limits, the RESET toggles low and remains low until proper output voltage regulation is restored. And finally, a $\overline{\text { RESET }}$ signal is issued if the regulator does not receive a Watchdog signal within the Wake Up period.

The RESET pulse width, Wake Up signal frequency, and Wake Up delay time are all set by one external capacitor $C_{\text {Delay }}$.

The regulator is protected against short circuit, over voltage, and thermal runaway conditions. The device can withstand 74 volt peak transients, making it suitable for use in automotive environments.

## Features

- $5.0 \mathrm{~V} \pm 2 \% / 100 \mathrm{~mA}$ Output Voltage
- Micropower Compatible Control Functions
- Wake Up
- Watchdog
- $\overline{\text { RESET }}$
- Low Dropout Voltage: 400 mV @ 100 mA
- Low Sleep Mode Quiescent Current ( $400 \mu \mathrm{~A}$ Typ)
- Protection Features
- Thermal Shutdown
- Short Circuit
- 74 V Peak Transient Capability
- Reverse Transient (-50 V)
- Internally Fused Leads in DIP-16 and SO-16L Packages



## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8151YT7 | TO-220* <br> STRAIGHT | 50 Units/Rail |
| CS8151YTVA7 | TO-220* <br> VERTICAL | 50 Units/Rail |
| CS8151YDPS7 | D²PAK $^{*}$ | 50 Units/Rail |
| CS8151YDPSR7 | D²PAK $^{*}$ | 750 Tape \& Reel |
| CS8151YNF16 | DIP-16 | 25 Units/Rail |
| CS8151YDWF16 | SO-16L | 46 Units/Rail |
| CS8151YDWFR16 | SO-16L | 1000 Tape \& Reel |
| *7 Lead/Pin. |  |  |$.$|  |
| :--- |

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 402 of this data sheet.

## PIN CONNECTIONS

TO-220 SEVEN LEAD



Figure 1. Block Diagram

MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| Power Dissipation | Internally Limited | - |
| Output Current (V ${ }_{\text {OUT }}$, RESET, Wake Up) | Internally Limited | - |
| Reverse Battery | -15 | V |
| Peak Transient Voltage ( 60 V Load Dump @ $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$ ) | +74 | V |
| Maximum Negative Transient ( $\mathrm{<} 2.0 \mathrm{~ms}$ ) | -50 | V |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| ESD Susceptibility (Machine Model) | 200 | V |
| Logic Inputs/Outputs | -0.3 to +6.0 | V |
| Storage Temperature Range | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering <br> Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 peak 230 peak | ${ }^{\circ} \mathrm{C} \mathrm{C}$ |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}\right.$,
$100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA}, \mathrm{C}_{2}=47 \mu \mathrm{~F}(\mathrm{ESR}<8.0 \Omega), \mathrm{C}_{\text {Delay }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Output Section

| Output Voltage, V $\mathrm{V}_{\text {OUT }}$ | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V} \\ & 6.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}, 0<\mathrm{I}_{\text {OUT }}<100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.90 \\ & 4.85 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 5.10 \\ & 5.15 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\begin{aligned} & \text { lout }=100 \mathrm{~mA} \\ & \text { lout }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A}<\mathrm{l}_{\text {OUT }}<100 \mathrm{~mA}$ | - | 10 | 50 | mV |
| Line Regulation | IOUT $=1.0 \mathrm{~mA}, 6.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}$ | - | 10 | 50 | mV |
| Ripple Rejection | $\begin{aligned} & 7.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<17 \mathrm{~V} @ \mathrm{f}=120 \mathrm{~Hz}, \\ & \text { IOUT }=100 \mathrm{~mA} \end{aligned}$ | 60 | 75 | - | dB |
| Current Limit | $\mathrm{V}_{\text {OUT }}=4.5 \mathrm{~V}$ | 100 | 250 | - | mA |
| Thermal Shutdown | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT }}<1.0 \mathrm{~V}$ | 50 | 56 | 62 | V |
| Quiescent Current | $\begin{aligned} & \text { lout }=200 \mu \mathrm{~A} \text { (Sleep) } \\ & \text { lout }=50 \mathrm{~mA} \\ & \text { lout }=100 \mathrm{~mA} \text { (Wake Up) } \end{aligned}$ |  | $\begin{gathered} 0.4 \\ 4.0 \\ 12 \end{gathered}$ | $\begin{gathered} 0.75 \\ - \\ 20 \end{gathered}$ | mA <br> mA <br> mA |
| Reverse Current | $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 1.0 | 1.5 | mA |

RESET

| Threshold High (RTH) | RTH V ${ }_{\text {OUT }}$ Increasing | $\mathrm{V}_{\text {OUT }}-0.3$ | - | V ${ }_{\text {OUT }}-0.04$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Threshold Low (RTL) | RTL V ${ }_{\text {OUT }}$ Decreasing | 4.5 | 4.7 | 4.91 | V |
| Hysteresis | RTH - RTL | 150 | 200 | 250 | mV |
| Output Low | 1.0 V < $\mathrm{V}_{\text {OUT }} \mathrm{RTL}$, I IOUT $=25 \mu \mathrm{~A}$ | - | 0.2 | 0.8 | V |
| Output High | $\mathrm{I}_{\text {OUT }}=25 \mu \mathrm{~A}, \mathrm{~V}_{\text {OUT }}>$ RTH | 3.8 | 4.2 | 5.1 | V |
| Current Limit | $\begin{aligned} & \overline{\text { RESET }}=0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}>\mathrm{V}_{\text {RTH }} \text { (Sourcing) } \\ & \text { RESET }=5.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}>1.0 \mathrm{~V} \text { (Sinking) } \end{aligned}$ | $\begin{gathered} 0.025 \\ 0.1 \end{gathered}$ | $\begin{aligned} & 0.5 \\ & 12 \end{aligned}$ | $\begin{gathered} 1.30 \\ 80 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Delay Time | POR Mode | 3.0 | 5.0 | 7.0 | ms |

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 100 \mathrm{~mA}, \mathrm{C}_{2}=47 \mu \mathrm{~F}($ ESR $<8.0 \Omega), \mathrm{C}_{\text {Delay }}=0.1 \mu \mathrm{~F}$; unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Watchdog Input |  |  |  |  |  |
| Threshold High | - | - | 1.4 | 2.0 | V |
| Threshold Low | - | 0.8 | 1.3 | - | V |
| Hysteresis | - | 25 | 100 | - | mV |
| Input Current | $0<$ WDI <6.0 V | -10 | 0 | +10 | $\mu \mathrm{~A}$ |
| Pulse Width | $50 \%$ WDI Falling Edge to <br> $50 \%$ WDI Rising Edge and <br> $50 \%$ WDI Rising Edge to <br> $50 \%$ WDI Falling Edge <br> (see Figures 2, 3, and 4) | 5.0 | - | - | $\mu \mathrm{s}$ |

## Wake Up Output

| Wake Up Period | See Figure 2. | 30 | 40 | 50 | ms |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Wake Up Duty Cycle Nominal | See Figure 4. | 40 | 50 | 60 | \% |
| RESET High to Wake Up Rising Delay Time | 50\% RESET Rising Edge to 50\% Wake Up Edge (see Figures 2, 3, and 4 ) | 15 | 20 | 25 | ms |
| Wake Up Response to Watchdog Input | 50\% WDI Falling Edge to $50 \%$ Wake Up Falling Edge | - | 2.0 | 10 | $\mu \mathrm{s}$ |
| Wake Up Response to RESET | 50\% RESET Falling Edge to 50\% Wake Up Falling Edge, $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V} \rightarrow 4.5 \mathrm{~V}$ | - | 2.0 | 10 | $\mu \mathrm{s}$ |
| Output Low | IOUT $=25 \mu \mathrm{~A}$ (Sinking) | - | 0.2 | 0.8 | V |
| Output High | IOUT $=25 \mu \mathrm{~A}$ (Sourcing) | 3.8 | 4.2 | 5.1 | V |
| Current Limit | Wake Up $=5.0 \mathrm{~V}$ <br> Wake Up $=0 \mathrm{~V}$ | $\begin{gathered} 0.025 \\ 0.5 \end{gathered}$ | 1.0 | $\begin{aligned} & 7.0 \\ & 3.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| TO-220 \& D2PAK | DIP-16 | SO-16L |  |  |
| 1 | 8 | 8 | $V_{\text {OUT }}$ | Regulated output voltage $5.0 \mathrm{~V} \pm 2 \%$. |
| 2 | 9 | 9 | $\mathrm{V}_{\text {IN }}$ | Supply voltage to the IC. |
| 3 | 11 | 11 | WDI | CMOS/TTL compatible input lead. The Watchdog function monitors the falling edge of the incoming signal. |
| 4 | 4, 5, 12, 13 | 4, 5, 6, 12, 13* | GND | Ground connection. |
| 5 | 14 | 14 | Wake Up | CMOS/TTL compatible output consisting of a continuously generated signal used to Wake Up the microprocessor from sleep mode. |
| 6 | 15 | 15 | RESET | CMOS/TTL compatible output lead RESET goes low whenever $V_{\text {OUT }}$ drops by more than $6.0 \%$ from nominal, or during the absence of a correct watchdog signal. |
| 7 | 16 | 16 | Delay | Input lead from timing capacitor for RESET and Wake Up signal. |
| - | 7 | 7 | Sense | Kelvin connection which allows remote sensing of the output voltage for improved regulation. If remote sensing is not required, connect to $\mathrm{V}_{\text {OUT }}$. |

[^8]

Figure 2. Power Up, Sleep Mode and Normal Operation


Figure 3. Error Condition: Watchdog Remains Low and a RESET Is Issued


Figure 4. Power Down and Restart Sequence

## DEFINITION OF TERMS

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse
techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.
Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
Current Limit: Peak current that can be delivered to the output.

## CIRCUIT DESCRIPTION

## Functional Description

To reduce the drain on the battery a system can go into a low current consumption mode when ever its not performing a main routine. The Wake Up signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 volt square wave with a duty cycle of $50 \%$ at a frequency that is determined by a timing capacitor, $\mathrm{C}_{\text {Delay }}$.

When the microprocessor receives a rising edge from the Wake Up output, it must issue a watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.


Figure 5. Wake Up Response to WDI


Figure 6. Wake Up Response to RESET (Low Voltage)

The first falling edge of the watchdog signal causes the Wake Up to go low within $2.0 \mu \mathrm{~s}$ (typ) and remain low until the next Wake Up cycle (see Figure 5). Other watchdog pulses received within the same cycle are ignored (Figures 2,3 , and 4).

During power up, $\overline{\text { RESET }}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the RESET toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text { RESET }}$ delay, $\overline{\mathrm{RESET}}$ returns high.
The Watchdog circuitry continuously monitors the input watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wake Up cycle will cause a $\overline{\text { RESET }}$ pulse to occur at the end of the Wake Up cycle (see Figure 3).
The Wake Up output is pulled low during a RESET regardless of the cause of the $\overline{\mathrm{RESET}}$. After the $\overline{\mathrm{RESET}}$ returns high, the Wake Up cycle begins again (see Figure 3).
The $\overline{\text { RESET }}$ pulse width, Wake Up signal frequency and RESET high to Wake Up delay time are all set by one external capacitor $C_{\text {Delay. }}$

Wake Up Period $=\left(4 \times 10^{5}\right) \mathrm{C}_{\text {Delay }}$
$\overline{\text { RESET }}$ Delay Time $=\left(5 \times 10^{4}\right) C_{\text {Delay }}$
$\overline{\text { RESET High to Wake Up Delay Time }}=\left(2 \times 10^{5}\right) \mathrm{C}_{\text {Delay }}$
Capacitor temperature coefficient and tolerance as well as the tolerance of the CS8151 must be taken into account in order to get the correct system tolerance for each parameter.

## APPLICATION NOTES

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (see Figure 7).

If the input voltage rises above the overvoltage shutdown threshold (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.


Figure 7. Typical Circuit Waveforms for Output Stage Protection

## Stability Considerations

The output or compensation capacitor C 2 (see Figure 8) helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

*C1 required if regulator is located far from the power supply filter.
${ }^{* *} \mathrm{C} 2$ required for stability.
Figure 8. Test and Application Circuit Showing Output Compensation

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or
ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.
The value for the output capacitor C 2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C 2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.
Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low
temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## Calculating Power Dissipation

 In a Single Output Linear RegulatorThe maximum power dissipation for a single output regulator (Figure 9) is:

$$
\begin{align*}
\mathrm{PD}_{\mathrm{D}}(\max )= & \left(\mathrm{V}_{\mathrm{IN}}(\max )-\mathrm{V}_{\mathrm{OUT}}(\min )\right) \mathrm{IOUT}(\max )  \tag{1}\\
& +\mathrm{VIN}_{\mathrm{IN}(\max ) \mathrm{Q}}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

## Heat Sinks

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.


Figure 9. Single Output Regulator with Key Performance Parameters Labeled


Figure 10. Application Diagram

## MARKING DIAGRAMS

| TO-220 <br> SEVEN LEAD <br> T SUFFIX | TO-220 <br> CASE 821E |
| :---: | :---: |
| SEVEN LEAD |  |
| TVA SUFFIX |  |
| CASE 821J |  |



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> 7 LEAD | D $^{2}$ PAK <br> 7-Pin | DIP-16 | SO-16L | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 1.8 | 1.8 | 15 | 18 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{*}$ | 50 | 75 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$.

## Micropower Voltage Regulator

The MC78FC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78FC00 series voltage regulator ICs feature a high accuracy output voltage and ultra-low quiescent current. Each device contains a voltage reference unit, an error amplifier, a driver transistor, and resistors for setting output voltage, and a current limit circuit. These devices are available in SOT-89 surface mount packages, and allow construction of an efficient, constant voltage power supply circuit.

MC78FC00 Series Features:

- Ultra-Low Quiescent Current of $1.1 \mu \mathrm{~A}$ Typical
- Ultra-Low Dropout Voltage ( 100 mV at 10 mA )
- Large Output Current (up to 120 mA )
- Excellent Line Regulation (0.1\%)
- Wide Operating Voltage Range (2.0 V to 10 V )
- High Accuracy Output Voltage ( $\pm 2.5 \%$ )
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Surface Mount Package (SOT-89)


## ORDERING INFORMATION

| Device | Output <br> Voltage | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: | :---: |
| MC78FC30HT1 | 3.0 |  |  |
| MC78FC33HT1 | 3.3 | $T_{A}=-30^{\circ}$ to $+80^{\circ} \mathrm{C}$ | SOT-89 |
| MC78FC40HT1 | 4.0 |  |  |
| MC78FC50HT1 | 5.0 |  |  |

Other voltages from 2.0 to 6.0 V , in 0.1 V increments, are available upon request. Consult factory for information.

Representative Block Diagram


This device contains 11 active transistors.

## MICROPOWER ULTRA-LOW QUIESCENT CURRENT VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA


H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT-89)

PIN CONNECTIONS


Standard Application


MAXIMUM RATINGS $\left(T_{C}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 10 | Vdc |
| Power Dissipation and Thermal Characteristics |  |  |  |
| Maximum Power Dissipation |  |  |  |
| Case 1213 (SOT-89) H Suffix | $\mathrm{P}_{\mathrm{D}}$ | 300 | mW |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {өJA }}$ | 333 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -30 to +80 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=\mathrm{V}_{\mathrm{O}}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ [Note 1], unless otherwise noted. $)$

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage <br> 30 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> 33 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}\right)$ <br> 40HT1 Suffix ( $\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}$ ) <br> 50 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 2.925 \\ & 3.218 \\ & 3.900 \\ & 4.875 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.3 \\ & 4.0 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.075 \\ & 3.382 \\ & 4.100 \\ & 5.125 \end{aligned}$ | V |
| Line Regulation $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1.0\right] \mathrm{V} \text { to } 10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$ | Regline | - | 0.1 | - | mV |
| Load Regulation $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1.0\right], \mathrm{I}_{\mathrm{O}}=1.0 \text { to } 10 \mathrm{~mA}$ | Regload | - | 40 | 80 | mV |
| Output Current <br> 30 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> 33 HT 1 Suffix $\left(\mathrm{V}_{\mathrm{in}}=6.0 \mathrm{~V}\right)$ <br> 40 HT 1 Suffix $\left(\mathrm{V}_{\mathrm{in}}=7.0 \mathrm{~V}\right)$ <br> 50 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | 10 | $\begin{aligned} & 50 \\ & 65 \\ & 65 \\ & 80 \end{aligned}$ | $\begin{gathered} 80 \\ 100 \\ 100 \\ 120 \end{gathered}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \end{aligned}$ | mA |
| Dropout Voltage $\mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - | 0.5 | 0.7 | V |
| Quiescent Current <br> 30 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> 33 HT 1 Suffix $\left(\mathrm{V}_{\mathrm{in}}=5.0 \mathrm{~V}\right)$ <br> 40 HT 1 Suffix $\left(\mathrm{V}_{\text {in }}=6.0 \mathrm{~V}\right)$ <br> 50 HT 1 Suffix ( $\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}$ ) | Icc | - | $\begin{aligned} & 1.1 \\ & 1.1 \\ & 1.2 \\ & 1.3 \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 3.3 \\ & 3.6 \\ & 3.9 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm $/{ }^{\circ} \mathrm{C}$ |

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

## DEFINITIONS

Dropout Voltage - The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.
Line Regulation - The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques
such that average chip temperature is not significantly affected.
Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.
Quiescent Bias Current - Current which is used to operate the regulator chip and is not delivered to the load.

## MC78FC00 Series



Figure 1. Output Voltage versus Output Current


Figure 3. Quiescent Current versus Temperature


Figure 2. Dropout versus Set Output Voltage


Figure 4. Dropout Voltage versus Output Current


Figure 5. Line Transient Response

## MC78FC00 Series

## APPLICATIONS INFORMATION

## Introduction

The MC78FC00 micropower voltage regulators are specifically designed with internal current limiting and low quiescent current making them ideal for battery powered applications. An input bypass capacitor is recommended if the regulator is located an appreciable distance ( $\geq 4$ inches) from the input voltage source. These regulators require $0.1 \mu \mathrm{~F}$ capacitance between the output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or other appropriate capacitors are recommended for operation below $25^{\circ} \mathrm{C}$. The bypass capacitors should be mounted with the shortest possible leads or track lengths directly across the regulator input and output terminals.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around $-30^{\circ} \mathrm{C}$, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ are readily available. Solid tantalum capacitors may be the better choice if small size is a requirement. However, a maximum ESR limit of $3.0 \Omega$ must be observed over temperature to maintain stability.

Figure 6 is a typical circuit application. Figure 7 is a current boost circuit which can deliver more than 600 mA . The circuit has no current limiting and the external transistor must be rated for the expected power dissipation.


Figure 6. Typical Application


Figure 7. Current Boost Circuit

## CS8321

## Micropower 5.0 V, 150 mA Low Dropout Linear Regulator

The CS8321 is a precision 5.0 V micropower voltage regulator with very low quiescent current ( $140 \mu \mathrm{~A}$ typ at 1.0 mA load). The 5.0 V output is accurate within $\pm 2 \%$ and supplies 150 mA of load current with a typical dropout voltage of only 300 mV .

This combination of low quiescent current and outstanding regulator performance makes the CS8321 ideal for any battery operated equipment.

The regulator is protected against reverse battery and short circuit conditions. The device can withstand 45 V load dump transients making it suitable for use in automotive environments.

## Features

- $5.0 \mathrm{~V} \pm 2 \%$ Output
- Low $140 \mu \mathrm{~A}$ (typ) Quiescent Current
- 150 mA Output Current Capability
- Fault Protection
-     - 15 V Reverse Voltage Output Current Limit
- Low Reverse Current (Output to Input)

*Lead Shorted to $\mathrm{V}_{\text {OUT }}$ in 3-Pin Applications
Figure 1. Block Diagram


MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8321YT3 | TO-220 <br> THREE LEAD | 50 Units/Rail |
| CS8321YDP3 | D$^{2}$ PAK, 3-PIN | 50 Units/Rail |
| CS8321YDPR3 | D2PAK, 3-PIN | 750 Tape \& Reel |

*Contact your local sales representative for SO-16, DIP-16, SO-8, and DIP-8 package options.

## ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Transient Input Voltage | $-15,45$ |  |
| Output Current | Internally Limited |  |
| ESD Susceptibility (Human Body Model) | - |  |
| Junction Temperature | 2.0 |  |
| Storage Temperature | Wave Solder (through hole styles only) Note 1 | kV |
| Lead Temperature Soldering | Reflow (SMD styles only) Note 2 | -40 to 150 |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(6.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<26 \mathrm{~V}\right.$, $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- |

Output Stage

| Output Voltage, V ${ }_{\text {OUT }}$ | $9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }} 16 \mathrm{~V}, 100 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 150 \mathrm{~mA}$ | 4.9 | 5.0 | 5.1 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\begin{aligned} & \text { lout }=150 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C} \\ & \text { IOUT }=150 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=125^{\circ} \mathrm{C} \end{aligned}$ | - | $0.3$ | $\begin{aligned} & 0.5 \\ & 0.6 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Quiescent Current, ( $\mathrm{I}_{\mathrm{Q}}$ ) | $\begin{aligned} & \text { lout }=1.0 \mathrm{~mA} @ \mathrm{~V}_{\text {IN }}=13 \mathrm{~V} \\ & \text { lout }^{2} 50 \mathrm{~mA} @ \mathrm{IIN}=13 \mathrm{~V} \\ & \mathrm{l}_{\text {OUT }}<150 \mathrm{~mA} @ \mathrm{~V}_{\text {IN }}=13 \mathrm{~V} \end{aligned}$ | - | $\begin{gathered} - \\ 4.0 \\ 15 \end{gathered}$ | $\begin{aligned} & 200 \\ & 6.0 \\ & 25 \end{aligned}$ | $\mu \mathrm{A}$ <br> mA <br> mA |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A}<\mathrm{I}_{\text {OUT }}<150 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V} \leq 26 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Ripple Rejection | $7.0 \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}, \mathrm{l}_{\text {OUT }}=150 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}$ | 60 | 75 | - | dB |
| Current Limit | - | 175 | 250 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 60 | 200 | - | mA |
| Reverse Current | $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 140 | 200 | $\mu \mathrm{A}$ |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |  |
| :---: | :---: | :---: | :--- |
| TO-220 | D $^{2}$ PAK |  |  |
| 1 | 1 |  | Input voltage. |
| 2 | 2 | GND | Ground. All GND leads must be connected to ground. |
| 3 | 3 | V OUT | $5.0 \mathrm{~V}, \pm 2 \%, 150 \mathrm{~mA}$ Output. |

## CIRCUIT DESCRIPTION AND APPLICATION NOTES

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

The CS8321 is a series pass voltage regulator. It consists of an error amplifier, bandgap voltage reference, PNP pass transistor with antisaturation control, and current limit.

As the voltage at the input, $\mathrm{V}_{\mathrm{IN}}$, is increased (Figure 1), $\mathrm{Q}_{\mathrm{N}}$ is forward biased via $R$. $\mathrm{Q}_{\mathrm{N}}$ provides base drive for $\mathrm{Q}_{\mathrm{P}}$. As $Q_{P}$ becomes forward biased, the output voltage, $V_{\text {OUT }}$, begins to rise as Qp 's output current charges the output capacitor. Once V OUT rises to a certain level, the error amplifier becomes biased and provides the appropriate amount of base current to $Q_{p}$. The error amplifier monitors the scaled output voltage via an internal voltage divider, R1 and R2, and compares it to the bandgap voltage reference. The error amplifier's output is a current which is equal to the error amplifier's differential input voltage times its transconductance. Therefore, the error amplifier varies the base drive current to $\mathrm{Q}_{\mathrm{N}}$, which provides bias to $\mathrm{Q}_{\mathrm{P}}$, based on the difference between the reference voltage and the scaled output voltage, V VUT.

## Antisaturation Protection

An antisaturation control circuit has also been added to prevent the pass transistor from going into deep saturation, which would cause excessive power dissipation due to large bias currents lost to the substrate via a parasitic PNP transistor, as shown in Figure 2.


Figure 2. The Parasitic PNP Transistor Which Is Part of the Pass Transistor ( $\mathbf{Q}_{\mathrm{P}}$ ) Structure

## Current Limit Limit

The output stage is protected against short circuit conditions. As shown in Figure 3, the output current will fold back when the faulted load is continually increased. This technique has been incorporated to limit the total power dissipation across the device during a short circuit condition, since the device does not contain overtemperature shutdown.

## STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.


Figure 3. Typical Current Limit and Fold Back Waveform

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.
The value for the output capacitor $\mathrm{C}_{\text {OUT }}$ shown in Figure 4 should work for most applications, however it is not necessarily the best solution.

${ }^{*} \mathrm{C}_{\mathrm{IN}}$ required if regulator is located far from the power supply filter.
${ }^{* *}$ Cout required for stability. Capacitor must operate at $^{\text {ren }}$ minimum temperature expected.
$\dagger$ Pin internally shorted to $\mathrm{V}_{\text {OUT }}$ in 3-pin applications.

Figure 4. Test and Application Circuit Showing Output Compensation

To determine an acceptable value for Cout for a particular application, start with a tantalum capacitor of the
recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 5) is:

$$
\begin{align*}
\mathrm{PD}_{\mathrm{D}}(\max )= & \left(\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{V}_{\mathrm{OUT}}(\min )\right) \mathrm{IOUT}(\max )  \tag{1}\\
& +\mathrm{V}_{\mathrm{IN}(\max ) \mathrm{I}_{\mathrm{Q}}}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{A}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\text {©JA }}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 5. Single Output Regulator with Key Performance Parameters Labeled

## HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like
$R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

## CS8321

## PACKAGE THERMAL DATA

| Parameter |  | TO-220 | D$^{2}$ PAK | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 3.5 | $1.0^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50 \dagger$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on die area.
$\dagger$ Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$.

## MC33263

# Ultra Low Noise 150 mA Low Dropout Voltage Regulator with ON/OFF Control 

Housed in a SOT23-L package, the MC33263 delivers up to 150 mA where it exhibits a typical 180 mV dropout. With an incredible noise level of $25 \mu$ VRMS (over 100 Hz to 100 kHz , with a 10 nF bypass capacitor), the MC33263 represents the ideal choice for sensitive circuits, especially in portable applications where noise performance and space are premium. The MC33263 also excels in response time and reacts in less than $25 \mu \mathrm{~s}$ when receiving an OFF to ON signal (with no bypass capacitor).

Thanks to a novel concept, the MC33263 accepts output capacitors without any restrictions regarding their Equivalent Series Resistance (ESR) thus offering an obvious versatility for immediate implementation.

With a typical DC ripple rejection better than $-90 \mathrm{~dB}(-70 \mathrm{~dB}$ @ 1.0 kHz ), it naturally shields the downstream electronics against choppy power lines.

Additionally, thermal shutdown and short-circuit protection provide the final product with a high degree of ruggedness.

## Features:

- Very Low Quiescent Current $170 \mu \mathrm{~A}$ (ON, no load), 100 nA (OFF, no load)
- Very Low Dropout Voltage, Typical Value is 137 mV at an Output Current of 100 mA
- Very Low Noise with External Bypass Capacitor (10 nF),

Typically $25 \mu \mathrm{Vrms}$ over 100 Hz to 100 kHz

- Internal Thermal Shutdown
- Extremely Tight Line Regulation Typically -90 dB
- Ripple Rejection -70 dB @ 1.0 kHz
- Line Transient Response: 1.0 mV for $\Delta \mathrm{V}_{\mathrm{in}}=3.0 \mathrm{~V}$
- Extremely Tight Load Regulation, Typically 20 mV at $\Delta \mathrm{I}_{\mathrm{out}}=150 \mathrm{~mA}$
- Multiple Output Voltages Available
- Logic Level ON/OFF Control (TTL-CMOS Compatible)
- ESR can vary from 0 to $3.0 \Omega$
- Functionally and Pin Compatible with TK112xxA/B Series


## Applications:

- All Portable Systems, Battery Powered Systems, Cellular Telephones, Radio Control Systems, Toys and Low Voltage Systems

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## ORDERING INFORMATION

See detailed ordering and shipping information on page 423 of this data sheet


Figure 1. MC33263 Block Diagram

## MAXIMUM RATINGS

| Rating | Symbol | Pin \# | Value | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\text {in }}$ | 6 | 12 | V |
| Power Dissipation and Thermal Resistance <br> Maximum Power Dissipation <br> Thermal Resistance, Junction-to-Air |  |  |  |  |
| Operating Ambient Temperature <br> Maximum Junction Temperature | $\mathrm{P}_{\mathrm{D}}$ |  | Internally Limited | W |
| Storage Temperature Range | $\mathrm{R}_{\text {ӨJA }}$ |  | 210 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Max}_{\mathrm{J}}=150^{\circ} \mathrm{C}$ )

| Characteristics | Symbol | Pin \# | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CONTROL ELECTRICAL CHARACTERISTICS |  |  |  |  |  |  |
| Input Voltage Range | V ON/OFF | 1 | 0 | - | $\mathrm{V}_{\text {in }}$ | V |
| ON/OFF Input Current (All versions) $\mathrm{V}_{\text {ON/OFF }}=2.4 \mathrm{~V}$ | Ion/OFF | 1 | - | 2.5 | - | $\mu \mathrm{A}$ |
| ON/OFF Input Voltages (All versions) Logic "0", i.e. OFF State Logic "1", i.e. ON State | $\mathrm{V}_{\text {ON/OFF }}$ | 1 | $\begin{gathered} - \\ 2.2 \end{gathered}$ | - | $0.3$ | V |

## CURRENTS PARAMETERS

| Current Consumption in OFF State (All versions) OFF Mode Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}$ | $\mathrm{IQ}_{\text {OFF }}$ | - | 0.1 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Consumption in ON State (All versions) ON Mode Sat Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}$ | $\mathrm{IQ}_{\mathrm{ON}}$ | - | 170 | 200 | $\mu \mathrm{A}$ |
| Current Consumption in Saturation ON State (All versions) ON Mode Sat Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}-0.5 \mathrm{~V}$, $\mathrm{I}_{\text {out }}=0 \mathrm{~mA}$ | $\mathrm{IQ}_{\text {SAT }}$ | - | 900 | 1400 | $\mu \mathrm{A}$ |
| Current Limit $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$, (All versions) Output Short-circuited (Note 1) | $\mathrm{I}_{\text {MAX }}$ | 175 | 210 | - | mA |

[^9]ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Max}_{\mathrm{T}}=150^{\circ} \mathrm{C}$ )

| Characteristics | Symbol | Pin \# | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<150 \mathrm{~mA} \\ & \text { 2.8 Suffix } \\ & \text { 3.0 Suffix } \\ & \text { 3.2 Suffix } \\ & \text { 3.3 Suffix } \\ & \text { 3.8 Suffix } \\ & \text { 4.0 Suffix } \\ & \text { 4.75 Suffix } \\ & \text { 5.0 Suffix } \end{aligned}$ | $V_{\text {out }}$ | 4 | $\begin{aligned} & 2.74 \\ & 2.94 \\ & 3.13 \\ & 3.23 \\ & 3.72 \\ & 3.92 \\ & 4.66 \\ & 4.90 \end{aligned}$ | $\begin{gathered} 2.8 \\ 3.0 \\ 3.2 \\ 3.3 \\ 3.8 \\ 4.0 \\ 4.75 \\ 5.0 \end{gathered}$ | $\begin{gathered} 2.86 \\ 3.06 \\ 3.27 \\ 3.37 \\ 3.88 \\ 4.08 \\ 4.85 \\ 5.1 \end{gathered}$ | V |
| $\begin{aligned} & \text { Vin }=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<80^{\circ} \mathrm{C} \text {, } \\ & 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<150 \mathrm{~mA} \\ & \text { 2.8 Suffix } \\ & \text { 3.0 Suffix } \\ & \text { 3.2 Suffix } \\ & \text { 3.3 Suffix } \\ & \text { 3.8 Suffix } \\ & \text { 4.0 Suffix } \\ & \text { 4.75 Suffix } \\ & \text { 5.0 Suffix } \end{aligned}$ | $V_{\text {out }}$ | 4 | $\begin{gathered} 2.7 \\ 2.9 \\ 3.09 \\ 3.18 \\ 3.67 \\ 3.86 \\ 4.58 \\ 4.83 \end{gathered}$ | $\begin{gathered} 2.8 \\ 3.0 \\ 3.2 \\ 3.3 \\ 3.8 \\ 4.0 \\ 4.75 \\ 5.0 \end{gathered}$ | $\begin{gathered} 2.9 \\ 3.1 \\ 3.31 \\ 3.42 \\ 3.93 \\ 4.14 \\ 4.92 \\ 5.17 \end{gathered}$ | V |

LINE AND LOAD REGULATION, DROPOUT VOLTAGES

| Line Regulation (All versions) $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<12 \mathrm{~V}, \mathrm{I}_{\text {out }}=60 \mathrm{~mA}$ | Regline | 4/6 | - | 2.0 | 10 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Load Regulation (All versions) $\begin{aligned} & V_{\text {in }}=V_{\text {out }}+1.0 \mathrm{~V} \\ & \mathrm{I}_{\text {out }}=1.0 \text { to } 60 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=1.0 \text { to } 100 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=1.0 \text { to } 150 \mathrm{~mA} \\ & \hline \end{aligned}$ | Regload | 1 | - | $\begin{aligned} & 8.0 \\ & 15 \\ & 20 \end{aligned}$ | $\begin{aligned} & 25 \\ & 35 \\ & 45 \end{aligned}$ | mV |
| Dropout Voltage (All versions) $\begin{aligned} & \mathrm{I}_{\text {out }}=10 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=100 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=150 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | 4, 6 | - | $\begin{gathered} 30 \\ 137 \\ 180 \end{gathered}$ | $\begin{gathered} 90 \\ 230 \\ 260 \end{gathered}$ | mV |

## DYNAMIC PARAMETERS

| Ripple Rejection (All versions) $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{pp}}=1.0 \mathrm{~V}, \mathrm{f}=1.0 \mathrm{kHz}, \mathrm{l}_{\text {out }}=60 \mathrm{~mA}$ |  | 4, 6 | 60 | 70 | - | dB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Transient Response $\begin{aligned} & \mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V} \text { to } \mathrm{V}_{\text {out }}+4.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=60 \mathrm{~mA}, \\ & \mathrm{~d}\left(\mathrm{~V}_{\text {in }}\right) / \mathrm{dt}=15 \mathrm{mV} / \mathrm{us} \end{aligned}$ |  | 4, 6 | - | 1.0 | - | mV |
| Output Noise Voltage (All versions) $\begin{aligned} \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=60 \mathrm{~mA}, \mathrm{f}= & 100 \mathrm{~Hz} \text { to } 100 \mathrm{kHz} \\ & \mathrm{C}_{\text {bypass }}=10 \mathrm{nF} \\ & \mathrm{C}_{\text {bypass }}=1.0 \mathrm{nF} \\ & \mathrm{C}_{\text {bypass }}=0 \mathrm{nF} \end{aligned}$ | $\mathrm{V}_{\text {RMS }}$ | 4, 6 |  | $\begin{aligned} & 25 \\ & 40 \\ & 65 \end{aligned}$ | - | $\mu \mathrm{Vrms}$ |
| Output Noise Density $\mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=60 \mathrm{~mA}, \mathrm{f}=1.0 \mathrm{kHz}$ | $\mathrm{V}_{\mathrm{N}}$ | 4 | - | 230 | - | $\mathrm{nV} / \sqrt{\text { Hz }}$ |
| Output Rise Time (All versions) $\mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=30 \mathrm{~mA}, \mathrm{~V}_{\text {ON/OFF }}=0 \text { to } 2.4 \mathrm{~V}$ <br> $1 \%$ of ON/OFF Signal to $99 \%$ of Nominal Output Voltage <br> Without Bypass Capacitor <br> With $\mathrm{C}_{\text {bypass }}=10 \mathrm{nF}$ | $\mathrm{t}_{\mathrm{r}}$ | 4 | - | $\begin{aligned} & 40 \\ & 1.1 \end{aligned}$ | - | $\begin{aligned} & \mu \mathrm{s} \\ & \mathrm{~ms} \end{aligned}$ |

THERMAL SHUTDOWN

| Thermal Shutdown (All versions) |  |  | - | 150 | - |
| :--- | :--- | :--- | :--- | :--- | :--- |

## DEFINITIONS

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage - The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage - The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.

Maximum Power Dissipation - The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current - Current which is used to operate the regulator chip and is not delivered to the load.

Line Regulation - The change in input voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Line Transient Response - Typical over- and undershoot response when input voltage is excited with a given slope.

Thermal Protection - Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically $150^{\circ} \mathrm{C}$, the regulator turns off.

This feature is provided to prevent catastrophic failures from accidental overheating.

Maximum Package Power Dissipation - The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. $125^{\circ} \mathrm{C}$. The junction temperature is rising while the difference between the input power ( $\mathrm{V}_{\mathrm{CC}} \mathrm{X} \mathrm{I}_{\mathrm{CC}}$ ) and the output power $\left(V_{\text {out }} X_{I_{\text {out }}}\right)$ is increasing.

Depending on ambient temperature, it is possible to calculate the maximum power dissipation, maximum load current or maximum input voltage (see Application Hints: Protection).

The maximum power dissipation supported by the device is a lot increased when using appropriate application design. Mounting pad configuration on the PCB, the board material and also the ambient temperature are affected the rate of temperature rise. It means that when the $\mathrm{I}_{\mathrm{C}}$ has good thermal conductivity through PCB, the junction temperature will be "low" even if the power dissipation is great.

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature $\left(150^{\circ} \mathrm{C}\right.$ for MC 33263$)$ and ambient temperature.

## APPLICATION HINTS

Input Decoupling - As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the MC33263 package. Higher values will correspondingly improve the overall line transient response.

Output Decoupling - Thanks to a novel concept, the MC33263 is a stable component and does not require any Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

Noise Performances - Unlike other LDOs, the MC33263 is a true low-noise regulator. With a 10 nF bypass capacitor, it typically reaches the incredible level of $25 \mu \mathrm{VRMS}$ overall noise between 100 Hz and 100 kHz . To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics as well as noise dependency versus bypass capacitor.

The bypass capacitor impacts the start-up phase of the MC33263 as depicted by the data-sheet curves. A typical 1.0 ms settling time is achieved with a 10 nF bypass capacitor. However, thanks to its low-noise architecture, the MC33263 can operate without bypass and thus offers a typical $20 \mu \mathrm{~s}$ start-up phase. In that case, the typical output noise stays lower than $65 \mu \mathrm{VRMS}$ between $100 \mathrm{~Hz}-$ 100 kHz .

Protections - The MC33263 hosts several protections, conferring natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a minimum of 175 mA while temperature shutdown occurs if the die heats up beyond $150^{\circ} \mathrm{C}$. These value lets you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$
P_{\max }=\frac{T_{J \max }-T_{A}}{R_{\theta J A}}
$$

If $\mathrm{T}_{\text {Jmax }}$ is internally limited to $150^{\circ} \mathrm{C}$, then the MC33263 can dissipate up to 595 mW @ $25^{\circ} \mathrm{C}$.

The power dissipated by the MC33263 can be calculated from the following formula:

$$
\text { Ptot }=\left\langle\mathrm{V}_{\text {in }} \cdot I_{\text {gnd }}\left(I_{\text {out }}\right)\right\rangle+\left\langle\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right\rangle \cdot I_{\text {out }}
$$

or

$$
\operatorname{Vin}_{\max }=\frac{\text { Ptot }+\mathrm{V}_{\text {out }} \cdot I_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 150 mA output current is needed, the ground current is extracted from the data-sheet curves: $6.5 \mathrm{~mA} @ 150 \mathrm{~mA}$. For a MC33263NW28R2 ( 2.8 V ), the maximum input voltage will then be 6.48 V , a rather comfortable margin.

Typical Application - The following figure portraits the typical application for the MC33263 where both input/output decoupling capacitors appear.


Figure 2. A Typical MC33263 Application with Recommended Capacitor Values

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. The following figure gives an example of a layout where stray inductances/capacitances are minimized.


Figure 3. Printed Circuit Board


Figure 4. Copper Side Component Layout
This layout is the basis for an MC33263 performance evaluation board where the BNC connectors give the user an easy and quick evaluation mean.

MC33263 Wake-up Improvement - In portable applications, an immediate response to an enable signal is vital. If noise is not of concern, the MC33263 without a bypass capacitor settles in nearly $20 \mu$ s and typically delivers $65 \mu \mathrm{VRMS}$ between 100 Hz and 100 kHz .

In ultra low-noise systems, the designer needs a 10 nF bypass capacitor to decrease the noise down to $25 \mu$ VRMS between 100 Hz and 100 kHz . With the adjunction of the 10 nF capacitor, the wake-up time expands up to 1.0 ms as shown on the data-sheet curves. If an immediate response is wanted, following figure's circuit gives a solution to
charge the bypass capacitor with the enable signal without degrading the noise response of the MC33263.

At power-on, C 4 is discharged. When the control logic sends its wake-up signal by going to a high level, the PNP base is momentarily tight to ground. The PNP switch closes and immediately charges the bypass capacitor C 1 toward its operating value. After a few $\mu \mathrm{s}$, the PNP opens and becomes totally transparent to the regulator.

This circuit improves the response time of the regulator which drops from 1.0 ms down to $30 \mu \mathrm{~s}$. The value of C 4 needs to be tweaked in order to avoid any bypass capacitor overload during the wake-up transient.


Figure 5. A PNP Transistor Drives the Bypass Pin when Enable Goes High


Figure 6. MC33263 Wake-up Improvement with Small PNP Transistor

The PNP being wired upon the bypass pin, it shall not degrade the noise response of the MC33263. Figure 7 confirms the good behavior of the integrated circuit in this
area which reaches a typical noise level of $26 \mu \mathrm{VRMS}$ $(100 \mathrm{~Hz}$ to 100 kHz$)$ at $\mathrm{I}_{\text {out }}=60 \mathrm{~mA}$.


Figure 7. Noise Density of the MC33263 with a 10 nF Bypass Capacitor and a Wake-up Improvement Network

TYPICAL PERFORMANCE CHARACTERISTICS
Ground Current Performances


Figure 8. Ground Current versus Output Current


Figure 9. Ground Current versus Ambient Temperature

Line Transient Response and Output Voltage


Figure 10. Quiescent Current versus Temperature


Figure 11. Line Transient Response

## TYPICAL PERFORMANCE CHARACTERISTICS

Load Transient Response versus Load Current Slope


Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE
Figure 12. $\mathrm{I}_{\text {out }}=3.0 \mathrm{~mA}$ to 150 mA


Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE
Figure 14. ISlope $=6.0 \mathrm{~mA} / \mu \mathrm{s}$ (Large Scale) $\mathrm{I}_{\text {out }}=3.0 \mathrm{~mA}$ to 150 mA


Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE
Figure 13. $I_{\text {Slope }}=100 \mathrm{~mA} / \mu \mathrm{s}$ (Large Scale) $\mathrm{I}_{\text {out }}=3.0 \mathrm{~mA}$ to 150 mA


Y1: OUTPUT CURRENT, Y2: OUTPUT VOLTAGE
Figure 15. Islope $=2.0 \mathrm{~mA} / \boldsymbol{\mu s}$ (Large Scale) $I_{\text {out }}=3.0 \mathrm{~mA}$ to 150 mA

## TYPICAL PERFORMANCE CHARACTERISTICS

## Noise Performances



Figure 16. Noise Density versus Bypass Capacitor


Figure 17. RMS Noise versus Bypass Capacitor ( 100 Hz - 100 kHz )

Settling Time Performances


Figure 18. Output Voltage Settling Time versus Bypass Capacitor


Figure 20. Output Voltage Settling Shape
$C_{\text {bypass }}=3.3 \mathrm{nF}$


Figure 19. Output Voltage Settling Shape $C_{\text {bypass }}=10 \mathrm{nF}$


Figure 21. Output Voltage Settling Shape without Bypass Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS
Dropout Voltage


Figure 22. Dropout Voltage versus $\mathrm{I}_{\text {out }}$


Figure 23. Dropout Voltage versus Temperature

Output Voltage


Figure 24. Output Voltage versus Temperature


Figure 25. Output Voltage versus $\mathrm{I}_{\text {out }}$

Ripple Rejection Performances


Figure 26. Ripple Rejection versus Frequency with 10 nF Bypass Capacitor


Figure 27. Ripple Rejection versus Frequency without Bypass Capacitor

## MC33263

ORDERING AND DEVICE MARKING INFORMATION

| Device | Marking | Version | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| MC33263NW-28R2 | A | 2.8 V |  |  |
| MC33263NW-30R2 | B | 3.0 V |  |  |
| MC33263NW-32R2 | C |  |  |  |
| MC33263NW-33R2 | D | 3.2 V |  | SOT-23L |

## MC78PC00 Series

## Low Noise 150 mA <br> Low Drop Out (LDO) Linear Voltage Regulator

The MC78PC00 are a series of CMOS linear voltage regulators with high output voltage accuracy, low supply current, low dropout voltage, and high Ripple Rejection. Each of these voltage regulators consists of an internal voltage reference, an error amplifier, resistors, a current limiting circuit and a chip enable circuit.

The dynamic Response to line and load is fast, which makes these products ideally suited for use in hand-held communication equipment.

The MC78PC00 series are housed in the SOT-23 5 lead package, for maximum board space saving.

## MC78PC00 Features:

- Ultra-Low Supply Current: typical $35 \mu \mathrm{~A}$ in ON mode with no load.
- Standby Mode: typical $0.1 \mu \mathrm{~A}$.
- Low Dropout Voltage: typical 0.2 V @ $\mathrm{I}_{\mathrm{OUT}}=100 \mathrm{~mA}$.
- High Ripple Rejection: typical 70 dB @ $\mathrm{f}=1 \mathrm{kHz}$.
- Low Temperature-Drift Coefficient of Output Voltage: typical $\pm 100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$.
- Excellent Line Regulation: typical 0.05\%/V.
- High Accuracy Output Voltage: $\pm 2.0 \%$.
- Fast Dynamic Response to Line and Load.
- Small Package: SOT-23 5 leads.
- Built-in Chip Enable circuit (CE input pin).
- Identical Pinout to the LP2980/1/2.


## MC78PC00 Applications:

- Power source for cellular phones (GSM, CDMA, TDMA), Cordless Phones (PHS, DECT) and 2-way radios.
- Power source for domestic appliances such as cameras, VCRs and camcorders.
- Power source for battery-powered equipment.




## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


SOT-23-5
N SUFFIX
CASE 1212

## PIN CONNECTIONS



DEVICE MARKING
(4 digits are available for device marking)

| Marking |  |  |
| :---: | :---: | :---: |
| (1) (2) | K8 | 1.8 V |
|  | F 5 | 2.5 V |
|  | F 8 | 2.8 V |
|  | $\mathrm{G0}$ | 3.0 V |
|  | G 3 | 3.3 V |
|  | $\mathrm{J0}$ | 5.0 V |
| (3) (4) |  | Lot Number |

PIN DESCRIPTION

| Pin \# | Symbol | Description |
| :---: | :---: | :--- |
| 1 | $\mathrm{~V}_{\text {IN }}$ | Input Pin |
| 2 | GND | Ground Pin |
| 3 | CE | Chip Enable Pin |
| 4 | N/C | No Connection |
| 5 | $\mathrm{~V}_{\text {OUT }}$ | Output Pin |

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 437 of this data sheet.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {IN }}$ | 9.0 | V |
| Input Voltage | $\mathrm{V}_{\mathrm{CE}}$ | $-0.3 \sim \mathrm{~V}_{\text {IN }}+0.3$ | V |
| Output Voltage | $\mathrm{V}_{\mathrm{OUT}}$ | $-0.3 \sim \mathrm{~V}_{\text {IN }}+0.3$ | V |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | 250 | mW |
| Operating Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +125 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{Jmax}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}\right)$

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V}$, I IOUT $\left.=30 \mathrm{~mA}\right)$ MC78PC18 <br> MC78PC25 <br> MC78PC28 <br> MC78PC30 <br> MC78PC33 <br> MC78PC50 | $V_{\text {OUT }}$ | $\begin{gathered} 1.764 \\ 2.450 \\ 2.744 \\ 2.94 \\ 3.234 \\ 4.9 \end{gathered}$ | $\begin{gathered} 1.80 \\ 2.50 \\ 2.80 \\ 3.00 \\ 3.3 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 1.836 \\ 2.550 \\ 2.856 \\ 3.06 \\ 3.366 \\ 5.1 \end{gathered}$ | V |
| Nominal Output Current $\left(\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\text {OUT (nom) }}-0.1 \mathrm{~V}\right)$ | Iout | 150 | - | - | mA |
| Load Regulation ( $\left.\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 80 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\text {OUT }} / \Delta \mathrm{l}_{\text {OUT }}$ | - | 12 | 40 | mV |
| Supply Current in ON mode ( $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V}$, I $\mathrm{OUT}=0 \mathrm{~mA}$ ) | Iss | - | 35 | 70 | $\mu \mathrm{A}$ |
| Supply Current in OFF mode, i.e. $\mathrm{V}_{\mathrm{CE}}=\mathrm{GND}$ $\left(\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{OUT}}=0 \mathrm{~mA}\right)$ | $\mathrm{I}_{\text {standby }}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Ripple Rejection ( $\mathrm{f}=1.0 \mathrm{kHz}$, Ripple $0.5 \mathrm{~V}_{\mathrm{p}-\mathrm{p}}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V}$ ) | RR | - | 70 | - | dB |
| Input Voltage | $\mathrm{V}_{\text {IN }}$ | - | - | 8.0 | V |
| Output Voltage Temperature Coefficient $\text { (IOUT }=30 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C} \text { ) }$ | $\Delta \mathrm{V}_{\text {OUT }} / \Delta \mathrm{T}$ | - | $\pm 100$ | - | ppm/ ${ }^{\circ} \mathrm{C}$ |
| Short Circuit Current Limit ( $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ ) | 1 lim | - | 50 | - | mA |
| CE Pull-down Resistance | $\mathrm{R}_{\mathrm{PD}}$ | 2.5 | 5.0 | 10 | $\mathrm{M} \Omega$ |
| CE Input Voltage "H" (ON Mode) | $\mathrm{V}_{\mathrm{IH}}$ | 1.5 | - | $\mathrm{V}_{\text {IN }}$ | V |
| CE Input Voltage "L" (OFF Mode) | $\mathrm{V}_{\mathrm{IL}}$ | 0 | - | 0.25 | V |
| Output Noise Voltage ( $\mathrm{f}=10 \mathrm{~Hz}$ to 100 kHz ) | $\mathrm{e}_{\mathrm{n}}$ | - | 30 | - | $\mu \mathrm{V}_{\text {rms }}$ |

## ELECTRICAL CHARACTERISTICS by OUTPUT VOLTAGE $\mathrm{V}_{\text {OUT }}\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { Dropout Voltage (lout }=100 \mathrm{~mA}) \\ 1.8 \leq \mathrm{V}_{\text {OUT }} \leq 1.9 \\ 2.0 \leq \mathrm{V}_{\text {OUT }} \leq 2.4 \\ 2.5 \leq \mathrm{V}_{\text {OUT }} \leq 2.7 \\ 2.8 \leq \text { V OUT } \leq 3.3 \\ 3.4 \leq \text { V }_{\text {OUT }} \leq 6.0 \\ \hline \end{gathered}$ | $\mathrm{V}_{\text {DIF }}$ |  | $\begin{aligned} & 0.60 \\ & 0.35 \\ & 0.24 \\ & 0.20 \\ & 0.17 \end{aligned}$ | $\begin{aligned} & 1.40 \\ & 0.70 \\ & 0.35 \\ & 0.30 \\ & 0.26 \end{aligned}$ | V |
| Line Regulation $\left(\mathrm{V}_{\text {OUT }}+0.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 8.0 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=30 \mathrm{~mA}\right)$ | $\Delta \mathrm{V}_{\text {OUT }} / \Delta \mathrm{V}_{\text {IN }}$ | - | 0.05 | 0.20 | \%/V |

## MC78PC00 Series

OPERATION


In the MC78PC00, the output voltage $\mathrm{V}_{\text {OUT }}$ is detected by $\mathrm{R} 1, \mathrm{R} 2$. The detected output voltage is then compared to the internal voltage reference by the error amplifier. Both a current limiting circuit for short circuit protection, and a chip enable circuit are included.

## MC78PC00 Series

## TEST CIRCUITS



Figure 1. Standard Test Circuits


Figure 3. Ripple Rejection, Line Transient Response Test Circuit


Figure 2. Supply Current Test Circuit


Figure 4. Load Transient Response Test Circuit


Figure 5. MC78PC18 Output Voltage versus Output Current


Figure 7. MC78PC40 (4.0 V) Output Voltage versus Output Current


Figure 9. MC78PC18 Output Voltage versus Input Voltage


Figure 6. MC78PC30 Output Voltage versus Output Current


Figure 8. MC78PC50 Output Voltage versus Output Current


Figure 10. MC78PC30 Output Voltage versus Input Voltage


Figure 11. MC78PC40 (4.0 V) Output Voltage versus Input Voltage


Figure 13. MC78PC18 Dropout Voltage versus Output Current


Figure 15. MC78PC40 (4.0 V) Dropout Voltage versus Output Current


Figure 12. MC78PC50 Output Voltage versus Input Voltage


Figure 14. MC78PC30 Dropout Voltage versus Output Current


Figure 16. MC78PC50 Dropout Voltage versus Output Current


Figure 17. MPC78PC18 Output Voltage versus Temperature


Figure 19. MC78PC40 (4.0 V) Output Voltage versus Temperature


Figure 21. MC78PC18 Supply Current versus Input Voltage


Figure 18. MC78PC30 Output Voltage versus Temperature


Figure 20. MC78PC50 Output Voltage versus Temperature


Figure 22. MC78PC30 Supply Current versus Input Voltage


Figure 23. MC78PC40 (4.0 V) Supply Current versus Input Voltage


Figure 25. MC78PC30 Supply Current versus Temperature


Figure 27. MC78PC50 Supply Current versus Temperature


Figure 24. MC78PC50 Supply Current versus Input Voltage


Figure 26. MC78PC40 (4.0 V) Supply
Current versus Temperature


Figure 28. Dropout Voltage versus Output Voltage


Figure 29. MC78PC18 Ripple Rejection versus Frequency


Figure 31. MC78PC30 Ripple Rejection versus Frequency


Figure 33. MC78PC40 (4.0 V) Ripple Rejection versus Frequency


Figure 30. MC78PC18 Ripple Rejection versus Frequency


Figure 32. MC78PC30 Ripple Rejection versus Frequency


Figure 34. MC78PC40 (4.0 V) Ripple Rejection versus Frequency

## MC78PC00 Series



Figure 35. MC78PC50 Ripple Rejection versus Frequency


Figure 36. MC78PC50 Ripple Rejection versus Frequency


Figure 38. MC78PC30 Ripple Rejection versus Input Voltage (DC Bias)


Figure 37. MC78PC30 Ripple Rejection versus Input Voltage (DC Bias)


Figure 39. MC78PC30 Ripple Rejection versus Input Voltage (DC Bias)


Figure 40. MC78PC30 Line Transient Response

Figure 41. MC78PC30 Line Transient Response


Figure 42. MC78PC30 Line Transient Response


Figure 43. MC78PC30 Load Transient Response


Figure 45. MC78PC30 Load Transient Response

## MC78PC00 Series

## APPLICATION HINTS

When using these circuits, please be sure to observe the following points:

- Phase compensation is made for securing stable operation even if the load current varies. For this reason, be sure to use a capacitor Cout with good frequency characteristics and ESR (Equivalent Series Resistance) as described in the graphs on page 434.
On page 434, the relations between IOUT (Output

Current) and ESR of Output Capacitor are shown. The conditions where the white noise level is under $40 \mu \mathrm{~V}$ (Avg.) are marked by the shaded area in the graph. (note: When additional ceramic capacitors are connected to the Output Pin with Output capacitor for phase compensation, there is a possibility that the operation will be unstable. Because of this, test these circuits with as same external components as ones to be used on the PCB).


Figure 46. Measuring Circuit for White Noise: MC78PC30

- Please be sure the $\mathrm{V}_{\mathrm{in}}$ and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or to malfunction.
- Connect the capacitor with a capacitance of $1.0 \mu \mathrm{~F}$ or more between $\mathrm{V}_{\text {in }}$ and GND as close as possible to $\mathrm{V}_{\text {in }}$ or GND.
- Set external components, especially the Output Capacitor, as close as possible to the circuit, and make the wiring as short as possible.


Figure 47. Typical Application

## MC78PC00 Series



Figure 48. Ceramic Capacitor $4.7 \mu \mathrm{~F}$


Figure 49. Ceramic Capacitor $6.8 \mu \mathrm{~F}$


Figure 50. Ceramic Capacitor $10 \mu \mathrm{~F}$

## MC78PC00 Series

## TAPE AND REEL INFORMATION

Component Taping Orientation for 5L SOT-23 Devices


Tape \& Reel Specifications Table

| Package | Tape Width (W) | Pitch (P) | Part Per Full Reel | Reel Diameter |
| :---: | :---: | :---: | :---: | :---: |
| $5 \mathrm{~L} \mathrm{SOT-23}$ | 8 mm | 4 mm | 3000 | 7 inches |

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC78PC18NTR |  |  |
| MC78PC25NTR |  |  |
| MC78PC28NTR | SOT-23 |  |
| MC78PC30NTR | 5 Leads | 3000 Units/Tape \& Reel |
| MC78PC33NTR |  |  |
| MC78PC50NTR |  |  |

Other voltages are available. Consult your ON Semiconductor representative.

## MC78PC00 Series

Recommended Footprint for SOT-23-5 Surface Mount Applications


## NCP551

## 150 mA CMOS Low Iq Low-Dropout Voltage Regulator

The NCP551 series of fixed output low dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP551 series features an ultra-low quiescent current of $4.0 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP551 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of $0.1 \mu \mathrm{~F}$. The device is housed in the micro-miniature TSOP-5 surface mount package. Standard voltage versions are $1.5,1.8,2.5,2.7,2.8,3.0,3.3$, and 5.0 V . Other voltages are available in 100 mV steps.

## Features

- Low Quiescent Current of $4.0 \mu \mathrm{~A}$ Typical
- Maximum Operating Voltage of 12 V
- Minimum Output Capacitance of $1.0 \mu \mathrm{~F}$
- Low Output Voltage Option
- High Accuracy Output Voltage of $2.0 \%$
- Industrial Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Battery Powered Instruments
- Hand-Held Instruments
- Camcorders and Cameras


Figure 1. Representative Block Diagram


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 448 of this data sheet.

NCP551

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | $\mathrm{~V}_{\text {in }}$ | Positive power supply input voltage |
| 2 | Gnd | Power supply ground |
| 3 | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the <br> device is disabled. If this function is not used, Enable should be connected to $V_{\text {in }}$. |
| 4 | N/C | No Internal Connection |
| 5 | $V_{\text {out }}$ | Regulated output voltage |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {in }}$ | 0 to 12 | V |
| Enable Voltage | $\mathrm{V}_{\mathrm{EN}}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Voltage | $\mathrm{V}_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| $\begin{array}{l}\text { Power Dissipation and Thermal Characteristics } \\ \text { Power Dissipation } \\ \text { Thermal Resistance, Junction-to-Ambient }\end{array}$ | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited |  |
| $\mathrm{R}_{\theta \mathrm{JA}}$ |  |  |  |$]$| W |
| :---: |
| Operating Junction Temperature |
| Operating Ambient Temperature |
| Storage Temperature |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{mADC}$ with trigger voltage.

NCP551

ELECTRICAL CHARACTERISTICS
( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom.) }}+1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EN}}=\mathrm{V}_{\text {in }}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, unless otherwise noted. )

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $V_{\text {out }}$ | $\begin{gathered} 1.455 \\ 1.746 \\ 2.425 \\ 2.646 \\ 2.744 \\ 2.94 \\ 3.234 \\ 4.90 \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 1.545 \\ 1.854 \\ 2.575 \\ 2.754 \\ 2.856 \\ 3.06 \\ 3.366 \\ 5.10 \end{gathered}$ | V |
| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \text {, } \mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $V_{\text {out }}$ | $\begin{aligned} & 1.440 \\ & 1.728 \\ & 2.400 \\ & 2.619 \\ & 2.716 \\ & 2.910 \\ & 3.201 \\ & 4.850 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.560 \\ & 1.872 \\ & 2.600 \\ & 2.781 \\ & 2.884 \\ & 3.09 \\ & 3.399 \\ & 5.150 \end{aligned}$ | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$ to $12 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ ) | Regline | - | 10 | 30 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=10 \mathrm{~mA}$ to 150 mA ) | Regload | - | 40 | 65 | mV |
| $\begin{aligned} & \text { Output Current } \\ & 1.5 \mathrm{~V}, 1.8 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=4.0 \mathrm{~V}\right) \\ & 2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right) \\ & 3.3 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \\ & 5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{0 \text { (nom.) }}$ | $\begin{aligned} & 150 \\ & 150 \\ & 150 \\ & 150 \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | mA |
| $\begin{aligned} & \text { Dropout Voltage ( } \left.\mathrm{l}_{\text {out }}=10 \mathrm{~mA} \text {, Measured at } \mathrm{V}_{\text {out }}-3.0 \%\right) \\ & 1.5 \mathrm{~V}, 1.8 \mathrm{~V}, 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}, 3.3 \mathrm{~V}, 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | - | $\begin{gathered} 130 \\ 40 \end{gathered}$ | $\begin{aligned} & 220 \\ & 150 \end{aligned}$ | mV |
| Quiescent Current <br> (Enable Input = 0 V ) <br> (Enable Input $=\mathrm{V}_{\text {in }}$, $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to $\mathrm{I}_{\mathrm{o} \text { (nom.) }}$ ) | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.1 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 8.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{c}}$ | - | $\pm 100$ | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(en) }}$ | 1.3 | - | $\overline{0.3}$ | V |
| Output Short Circuit Current $\begin{aligned} & 1.5 \mathrm{~V}, 1.8 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=4.0 \mathrm{~V}\right) \\ & 2.5 \mathrm{~V}, 2.7 \mathrm{~V}, 2.8 \mathrm{~V}, 3.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right) \\ & 3.3 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}\right) \\ & 5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\text {out(max) }}$ | $\begin{aligned} & 160 \\ & 160 \\ & 160 \\ & 160 \end{aligned}$ | $\begin{aligned} & 350 \\ & 350 \\ & 350 \\ & 350 \end{aligned}$ | $\begin{aligned} & 600 \\ & 600 \\ & 600 \\ & 600 \end{aligned}$ | mA |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.

NCP551


Figure 2. Ground Pin Current versus Output Current


Figure 4. Ground Pin Current versus Input Voltage


Figure 3. Ground Pin Current versus Output Current


Figure 5. Ground Pin Current versus Input Voltage


Figure 6. Line Transient Response


Figure 7. Line Transient Response


Figure 8. Line Transient Response


Figure 9. Line Transient Response


Figure 10. Line Transient Response


Figure 11. Line Transient Response


Figure 12. Load Transient Response ON


Figure 13. Load Transient Response OFF


Figure 14. Load Transient Response OFF


Figure 15. Load Transient Response ON


Figure 16. Turn-On Response


Figure 18. Output Voltage versus Input Voltage


Figure 19. Output Voltage versus Input Voltage

## APPLICATIONS INFORMATION

A typical application circuit for the NCP551 series is shown in Figure 20.

## Input Decoupling (C1)

A $0.1 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP551 package. Higher values and lower ESR will improve the overall line transient response.

## Output Decoupling (C2)

The NCP551 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $0.1 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

## Enable Operation

The enable pin will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to $\mathrm{V}_{\text {in }}$.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Thermal

As power across the NCP551 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP551 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP551 can dissipate up to $400 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$.

The power dissipated by the NCP551 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} l_{\text {gnd }}\left(l_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right]^{*} l_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \text { I out }}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 150 mA output current is needed then the ground current from the data sheet is $4.0 \mu \mathrm{~A}$. For an NCP551SN30T1 (3.0 V), the maximum input voltage will then be 5.6 V .


Figure 20. Typical Application Circuit


Figure 21. Current Boost Regulator
The NCP551 series can be current boosted with a PNP transistor. Resistor R in conjunction with $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by $\mathrm{V}_{\mathrm{BE}}$ of the pass resistor.


Figure 23. Delayed Turn-on
If a delayed turn-on is needed during power up of several voltages then the above schematic can be used. Resistor R, and capacitor C , will delay the turn-on of the bottom regulator.


Figure 22. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the $\mathrm{V}_{\mathrm{BE}}$ of Q 2 and $R 1$. $\mathrm{I}_{\mathrm{SC}}=\left(\left(\mathrm{V}_{\mathrm{BEQ} 2}-\mathrm{ib}{ }^{*} \mathrm{R} 2\right) / \mathrm{R} 1\right)+\mathrm{I}_{\mathrm{O}(\max )}$ Regulator


Figure 24. Input Voltages Greater than 12 V
A regulated output can be achieved with input voltages that exceed the 12 V maximum rating of the NCP551 series with the addition of a simple pre-regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output ( $\mathrm{V}_{\text {out }}$ ) is shorted to $\mathrm{G}_{\text {nd }}$.

## NCP551

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5
(Footprint Compatible with SOT23-5)

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP551SN15T1 | 1.5 | LAO |  |  |
| NCP551SN18T1 | 1.8 | LAP |  |  |
| NCP551SN25T1 | 2.5 | LAQ |  |  |
| NCP551SN27T1 | 2.7 | LAR | TSOP-5 | 3000 Units/7" Tape \& Reel |
| NCP551SN28T1 | 2.8 | LAS |  |  |
| NCP551SN30T1 | 3.0 | LAT |  |  |
| NCP551SN33T1 | 3.3 | LAU |  |  |
| NCP551SN50T1 | 5.0 | LAV |  |  |

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## NCP561

## 150 mA CMOS Low Iq Low-Dropout Voltage Regulator

The NCP561 series of fixed output low dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP561 series features an ultra-low quiescent current of $3.0 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP561 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of $1.0 \mu \mathrm{~F}$. The device is housed in the micro-miniature TSOP-5 surface mount package. Standard voltage versions are 1.5, 1.8, 2.5, 2.7, 2.8, 3.0, 3.3 and 5.0 V .

## Features

- Low Quiescent Current of $3.0 \mu \mathrm{~A}$ Typical
- Low Dropout Voltage of 170 mV at 150 mA
- Low Output Voltage Option
- Output Voltage Accuracy of $2.0 \%$
- Industrial Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Battery Powered Instruments
- Hand-Held Instruments
- Camcorders and Cameras


This device contains 28 active transistors

Figure 1. Representative Block Diagram
ON Semiconductor ${ }^{\text {T }}$ http://onsemi.com

TSOP-5 (SOT23-5, SC59-5) SN SUFFIX CASE 483
PIN CONNECTIONS AND
MARKING DIAGRAM


$$
\begin{aligned}
& \mathrm{xxx}=\text { Version } \\
& \mathrm{Y}=\text { Year } \\
& \mathrm{W}=\text { Work Week }
\end{aligned}
$$

(Top View)

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 458 of this data sheet.

## NCP561

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | Vin | Positive power supply input voltage. |
| 2 | Gnd | Power supply ground. |
| 3 | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the device is <br> disabled. If this function is not used, Enable should be connected to Vin. |
| 4 | N/C | No internal connection. |
| 5 | V OUT | Regulated output voltage. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {IN }}$ | 6.0 | V |
| Enable Voltage | Enable | -0.3 to $\mathrm{V}_{\text {IN }}+0.3$ | V |
| Output Voltage | $\mathrm{V}_{\text {OUT }}$ | -0.3 to $\mathrm{V}_{\mathrm{IN}}+0.3$ | V |
| Power Dissipation and Thermal Characteristics Power Dissipation Thermal Resistance, Junction to Ambient | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{JJA}} \end{gathered}$ | Internally Limited 250 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{w} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ | $\mathrm{T}_{\text {solder }}$ | 10 | sec |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{~mA} \mathrm{DC}$ with trigger voltage.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathbb{I N}}=\mathrm{V}_{\text {OUT(nom. }}\right)+1.0 \mathrm{~V}, \mathrm{~V}_{\text {enable }}=\mathrm{V}_{\mathbb{I N}}, \mathrm{C}_{\mathbb{I N}}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \text { I IOUT }=1.0 \mathrm{~mA}\right) \\ & 1.5 \mathrm{~V} \\ & 1.8 \mathrm{~V} \\ & 2.5 \mathrm{~V} \\ & 2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V} \\ & 3.0 \mathrm{~V} \\ & 3.3 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {OUT }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.646 \\ & 2.744 \\ & 2.940 \\ & 2.234 \\ & 4.90 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.754 \\ & 2.856 \\ & 3.060 \\ & 3.366 \\ & 5.10 \end{aligned}$ | V |
| Line Regulation $\begin{aligned} & \left.1.5 \mathrm{~V}-4.4 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {o(nom. }}\right)+1.0 \mathrm{~V} \text { to } 6.0 \mathrm{~V}\right) \\ & 4.5 \mathrm{~V}-5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=5.5 \mathrm{~V} \text { to } 6.0 \mathrm{~V}\right) \end{aligned}$ | Regline | - | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ | mV |
| Load Regulation (lout $=10 \mathrm{~mA}$ to 150 mA ) | Regload | - | 30 | 60 | mV |
| $\begin{aligned} & \text { Output Current }\left(\mathrm{V}_{\text {out }}=\left(\mathrm{V}_{\text {out }} \text { at } \mathrm{I}_{\text {out }}=150 \mathrm{~mA}\right)-3.0 \%\right) \\ & \left.1.5 \mathrm{~V} \text { to } 3.9 \mathrm{~V}\left(\mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {o(nom. }}\right)+2.0 \mathrm{~V}\right) \\ & 4.0 \mathrm{~V} \text { to } 5.0 \mathrm{~V}\left(\mathrm{~V}_{\text {IN }}=6.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{0 \text { (nom.) }}$ | $\begin{aligned} & 150 \\ & 150 \end{aligned}$ | - | - | mA |
| Dropout Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $85^{\circ} \mathrm{C}$, I IOUT $=150 \mathrm{~mA}$, Measured at $\mathrm{V}_{\text {OUT }}-3.0 \%$ ) $\begin{aligned} & 1.5 \mathrm{~V}-1.7 \mathrm{~V} \\ & 1.8 \mathrm{~V}-2.4 \mathrm{~V} \\ & 2.5 \mathrm{~V}-2.7 \mathrm{~V} \\ & 2.8 \mathrm{~V}-3.2 \mathrm{~V} \\ & 3.3 \mathrm{~V}-4.9 \mathrm{~V} \\ & 5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & 330 \\ & 240 \\ & 150 \\ & 140 \\ & 130 \\ & 120 \end{aligned}$ | $\begin{aligned} & 500 \\ & 360 \\ & 250 \\ & 230 \\ & 200 \\ & 190 \end{aligned}$ | mV |
| Quiescent Current <br> (Enable Input = 0 V) <br> $\left(\right.$ Enable Input $=\mathrm{V}_{\text {IN }}, \mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ to $\left.\mathrm{I}_{\text {o(nom. } .)}\right)$ | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.1 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 8.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Short Circuit Current $\begin{aligned} & 1.5 \mathrm{~V} \text { to } 3.9 \mathrm{~V}\left(\mathrm{~V}_{\mathbb{I N}}=\mathrm{V}_{\mathrm{o}(\text { nom. })}+2.0 \mathrm{~V}\right) \\ & 4.0 \mathrm{~V} \text { to } 5.0 \mathrm{~V}\left(\mathrm{~V}_{\mathrm{IN}}=6.0 \mathrm{~V}\right) \end{aligned}$ | IOUT(max) | $\begin{aligned} & 160 \\ & 160 \end{aligned}$ | $\begin{aligned} & 400 \\ & 400 \end{aligned}$ | $800$ | mA |
| Output Voltage Noise $\text { (f = } 20 \mathrm{~Hz} \text { to } 100 \mathrm{kHz}, \mathrm{~V}_{\text {OUT }}=3.0, \mathrm{~V} \mathrm{I}_{\text {OUT }}=1.0 \mathrm{~V} \text { ) }$ | $\mathrm{V}_{\mathrm{n}}$ | - | 60 | - | $\mu \mathrm{Vrms}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(en) }}$ | $1.3$ | - | $\overline{0.2}$ | V |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm/ ${ }^{\circ} \mathrm{C}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\Theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

TYPICAL CHARACTERISTICS


Figure 2. Dropout Voltage vs. Temperature


Figure 4. Quiescent Current vs. Temperature


Figure 6. Ground Current vs. Input Voltage


Figure 3. Output Voltages vs. Temperature

Figure 5. Quiescent Current vs. Input Voltage


Figure 7. Output Noise Voltage

## NCP561

TYPICAL CHARACTERISTICS


Figure 8. Line Transient Response


Figure 10. Load Transient Response


Figure 9. Load Transient Response


Figure 11. Turn-On Response


Figure 12. Output Voltage vs. Input Voltage

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.

## APPLICATIONS INFORMATION

A typical application circuit for the NCP561 series is shown in Figure 13.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP561 package. Higher values and lower ESR will improve the overall line transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

## Output Decoupling (C2)

The NCP561 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K, or C3216X7R1C105K

## Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to $\mathrm{V}_{\mathrm{IN}}$.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads a short as possible.

## Thermal

As power across the NCP561 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP561 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP561 can dissipate up to 400 mW @ $25^{\circ} \mathrm{C}$.
The power dissipated by the NCP561 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} \operatorname{lgnd}\left(I_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right]^{*} l_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {INMAX }}=\frac{\mathrm{P}_{\mathrm{TOT}}+\mathrm{V}_{\mathrm{OUT}}{ }^{*} \text { IOUT }}{\mathrm{I}_{\mathrm{GND}}+\mathrm{I}_{\mathrm{OUT}}}
$$

If a 150 mA output current is needed then the ground current from the data sheet is $4.0 \mu \mathrm{~A}$. For an NCP561SN30T1 ( 3.0 V ), the maximum input voltage will then be 5.6 V .


Figure 13. Typical Application Circuit

## APPLICATION CIRCUITS



Figure 14. Current Boost Regulator
The NCP561 series can be current boosted with a PNP transistor. Resistor R in conjunction with $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by $\mathrm{V}_{\mathrm{BE}}$ of the pass resistor.


Figure 16. Delayed Turn-on
If a delayed turn-on is needed during power up of several voltages then the above schematic can be used. Resistor R, and capacitor C , will delay the turn-on of the bottom regulator.


Figure 15. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the $\mathrm{V}_{\mathrm{BE}}$ of Q 2 and R1. $I_{S C}=\left(\left(V_{B E Q 2}-i b * R 2\right) / R 1\right)+I_{(\text {max })}$ Regulator


Figure 17. Input Voltages Greater than 6.0 V
A regulated output can be achieved with input voltages that exceed the 6.0 V maximum rating of the NCP561 series with the addition of a simple pre-regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output ( $\mathrm{V}_{\text {OUT }}$ ) is shorted to $\mathrm{G}_{\text {nd }}$.

## NCP561

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5
(Footprint Compatible with SOT23-5)

## NCP561

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP561SN15T1 | 1.5 | LDA |  |  |
| NCP561SN18T1 | 1.8 | LEV |  |  |
| NCP561SN25T1 | 2.5 | LDC |  |  |
| NCP561SN2711 | 2.7 | LEX | TSOP-5 | 3000 Units/ |
| NCP561SN28T1 | 2.8 | LDD |  |  |
| NCP561SN30T1 | 3.0 | LDE |  |  |
| NCP561SN33T1 | 3.3 | LDF |  |  |
| NCP561SN50T1 | 5.0 | LDH |  |  |

Additional voltages are available upon request by contacting your ON Semiconductor representative.

## NCP500

## 150 mA CMOS Low Noise Low-Dropout Voltage Regulator

The NCP500 series of fixed output low dropout linear regulators are designed for portable battery powered applications which require low noise operation, fast enable response time, and low dropout. The device achieves its low noise performance without the need of an external noise bypass capacitor. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, and resistors for setting output voltage, and current limit and temperature limit protection circuits.

The NCP500 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of $1.0 \mu \mathrm{~F}$. Standard voltage versions are $1.8,2.5,2.7,2.8,3.0,3.3$, and 5.0 V .

## Features

- Ultra-Low Dropout Voltage of 170 mV at 150 mA
- Fast Enable Turn-On Time of $20 \mu \mathrm{sec}$
- Wide Operating Voltage Range of 1.8 V to 6.0 V
- Excellent Line and Load Regulation
- High Accuracy Output Voltage of 2.5\%
- Enable Can Be Driven Directly by 1.0 V Logic
- Very Small QFN 2x2 Package


## Typical Applications

- Noise Sensitive Circuits - VCO's, RF Stages, etc.
- SMPS Post-Regulation
- Hand-Held Instrumentation
- Camcorders and Cameras


NOTE: Pin numbers in parenthesis indicate QFN package.

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAMS


QFN 2x2


| xxx | $=$ Version |
| :--- | :--- |
| Y | $=$ Year |
| W | $=$ Work Week |
| M | $=$ Date Code |

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 475 of this data sheet.

Figure 1. Simplified Block Diagram

NCP500

PIN FUNCTION DESCRIPTION

| TSOP-5 <br> Pin No. | QFN 2x2 <br> Pin No. | Pin Name |  |
| :---: | :---: | :---: | :--- |
| 1 | 3 | Vin | Positive power supply input voltage. |
| 2 | 2,5 | Gnd | Power supply ground. |
| 3 | 1 | Enable | This input is used to place the device into low-power standby. When this input is pulled to a logic <br> low, the device is disabled. If this function is not used, Enable should be connected to Vin. |
| 4 | 6 | N/C | No internal connection. |
| 5 | 4 | Vout | Regulated output voltage. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\text {in }}$ | 0 to 6.0 | V |
| Enable Voltage | $\mathrm{V}_{\text {on/off }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Voltage | $\mathrm{V}_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Short Circuit Duration | - | Infinite | - |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {өJA }}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| TSOP-5 |  | 250 |  |
| QFN | $\mathrm{T}_{\mathrm{J}}$ | 225 | +125 |
| Operating Junction Temperature | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {solder }}$ | 10 | sec |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ |  |  |  |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method $200 \mathrm{~V} \quad$ Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{~mA}$.
2. Device is internally limited to $160^{\circ} \mathrm{C}$ by thermal shutdown.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=2.3 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{jmax}}=125^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -1.8 V |  |  |  |  |  |
| Output Voltage ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | $V_{\text {out }}$ | 1.755 | 1.8 | 1.845 | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=2.3 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regload | - | 15 | 45 | mV |
| ```Dropout Voltage (Measured at Vout -2.0%, TA}=-4\mp@subsup{0}{}{\circ}\textrm{C}\mathrm{ to }8\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ ) (lout = 1.0 mA) (lout = 75 mA) (lout = 150 mA)``` | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 140 \\ & 270 \end{aligned}$ | $\begin{gathered} 10 \\ 200 \\ 350 \end{gathered}$ | mV |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 200 | 540 | 700 | mA |
| Ripple Rejection $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }(\text { nom. })}+1.0 \mathrm{~V}+0.5 \mathrm{~V}_{\text {pp }}, f=1.0 \mathrm{kHz}, \mathrm{I}_{\mathrm{o}}=60 \mathrm{~mA}\right)$ | RR | - | 62 | - | dB |
| ```Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I Iout = 1.0 mA) (Enable Input = 0.9 V, I Iout = 150 mA)``` | $\mathrm{I}_{\mathrm{Q}}$ |  | $\begin{aligned} & 0.01 \\ & 175 \\ & 175 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{A}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(EN }}$ | $0.9$ | - | $0.15$ | V |
| Enable Input Bias Current | $\mathrm{I}_{\mathrm{BB}(\mathrm{EN})}$ | - | 3.0 | 100 | nA |
| Output Turn On Time (Enable Input = 0 V to $\mathrm{V}_{\text {in }}$ ) | - | - | 20 | 100 | $\mu \mathrm{s}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=3.0 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{T}_{\text {jmax }}=125^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -2.5 V |  |  |  |  |  |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA} \text { to } 150 \mathrm{~mA}\right)$ | $V_{\text {out }}$ | 2.438 | 2.5 | 2.563 | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=3.0 \mathrm{~V}$ to 6.0 V , $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regioad | - | 15 | 45 | mV |
| $\begin{aligned} & \text { Dropout Voltage (Measured at } V_{\text {out }}-2.0 \%, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \text { ) } \\ & \text { (lout }=1.0 \mathrm{~mA}) \\ & \text { (lout }=75 \mathrm{~mA} \text { ) } \\ & \text { (lout }=150 \mathrm{~mA} \text { ) } \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{aligned} & 2.0 \\ & 100 \\ & 190 \end{aligned}$ | $\begin{gathered} 10 \\ 170 \\ 270 \end{gathered}$ | mV |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 200 | 540 | 700 | mA |
| Ripple Rejection $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }(\text { nom. })}+1.0 \mathrm{~V}+0.5 \mathrm{~V}_{\text {pp }}, f=1.0 \mathrm{kHz}, \mathrm{I}_{0}=60 \mathrm{~mA}\right)$ | RR | - | 62 | - | dB |
| ```Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I Iout = 1.0 mA) (Enable Input = 0.9 V, I Iout = 150 mA)``` | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.01 \\ & 180 \\ & 180 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{A}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(EN }}$ | $0.9$ | - | $\overline{0.15}$ | V |
| Enable Input Bias Current | $\mathrm{I}_{\mathrm{IB}(\mathrm{EN})}$ | - | 3.0 | 100 | nA |
| Output Turn On Time (Enable Input = 0 V to $\mathrm{V}_{\text {in }}$ ) | - | - | 20 | 100 | $\mu \mathrm{s}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=3.2 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{T}_{\text {jmax }}=125^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -2.7 V |  |  |  |  |  |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA} \text { to } 150 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {out }}$ | 2.633 | 2.7 | 2.768 | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=3.2 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regload | - | 15 | 45 | mV |
| ```Dropout Voltage (Measured at Vout -2.0%,}\mp@subsup{\textrm{T}}{\textrm{A}}{}=-4\mp@subsup{0}{}{\circ}\textrm{C}\mathrm{ to }8\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ ) (lout = 1.0 mA) (lout = 75 mA) (lout = 150 mA)``` | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{gathered} 2.0 \\ 90 \\ 180 \end{gathered}$ | $\begin{gathered} 10 \\ 160 \\ 260 \end{gathered}$ | mV |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 200 | 540 | 700 | mA |
| Ripple Rejection $\left.\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }} \text { (nom. }\right)+1.0 \mathrm{~V}+0.5 \mathrm{~V}_{\text {pp }}, \mathrm{f}=1.0 \mathrm{kHz}, \mathrm{I}_{0}=60 \mathrm{~mA}\right)$ | RR | - | 62 | - | dB |
| ```Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I Iout = 1.0 mA) (Enable Input = 0.9 V, I Iout = 150 mA)``` | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.01 \\ & 185 \\ & 185 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{A}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(EN) }}$ | $0.9$ | - | $\overline{0.15}$ | V |
| Enable Input Bias Current | $\mathrm{IIB}_{\text {(EN })}$ | - | 3.0 | 100 | nA |
| Output Turn On Time (Enable Input = 0 V to $\mathrm{V}_{\text {in }}$ ) | - | - | 20 | 100 | $\mu \mathrm{s}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=3.3 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{T}_{\text {jmax }}=125^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -2.8 V |  |  |  |  |  |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA} \text { to } 150 \mathrm{~mA}\right)$ | $V_{\text {out }}$ | 2.730 | 2.8 | 2.870 | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=3.3 \mathrm{~V}$ to 6.0 V , $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regioad | - | 15 | 45 | mV |
| $\begin{aligned} & \text { Dropout Voltage (Measured at } V_{\text {out }}-2.0 \%, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \text { ) } \\ & \text { (lout }=1.0 \mathrm{~mA}) \\ & \text { (lout }=75 \mathrm{~mA} \text { ) } \\ & \text { (lout }=150 \mathrm{~mA} \text { ) } \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{gathered} 2.0 \\ 90 \\ 170 \end{gathered}$ | $\begin{gathered} 10 \\ 150 \\ 250 \end{gathered}$ | mV |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 200 | 540 | 700 | mA |
| Ripple Rejection $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }(\text { nom. })}+1.0 \mathrm{~V}+0.5 \mathrm{~V}_{\text {pp }}, f=1.0 \mathrm{kHz}, \mathrm{I}_{0}=60 \mathrm{~mA}\right)$ | RR | - | 62 | - | dB |
| ```Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I Iout = 1.0 mA) (Enable Input = 0.9 V, I Iout = 150 mA)``` | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.01 \\ & 185 \\ & 185 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{A}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(EN }}$ | $0.9$ | - | $\overline{0.15}$ | V |
| Enable Input Bias Current | $\mathrm{I}_{\mathrm{IB}(\mathrm{EN})}$ | - | 3.0 | 100 | nA |
| Output Turn On Time (Enable Input = 0 V to $\mathrm{V}_{\text {in }}$ ) | - | - | 20 | 100 | $\mu \mathrm{s}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=3.5 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{T}_{\text {jmax }}=125^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -3.0 V |  |  |  |  |  |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA} \text { to } 150 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {out }}$ | 2.925 | 3.0 | 3.075 | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=3.5 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regload | - | 15 | 45 | mV |
| ```Dropout Voltage (Measured at Vout -2.0%, TA}=-4\mp@subsup{0}{}{\circ}\textrm{C}\mathrm{ to }8\mp@subsup{5}{}{\circ}\textrm{C}\mathrm{ ) (lout = 1.0 mA) (lout = 75 mA) (lout = 150 mA)``` | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{gathered} 2.0 \\ 85 \\ 165 \end{gathered}$ | $\begin{gathered} 10 \\ 130 \\ 240 \end{gathered}$ | mV |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 200 | 540 | 700 | mA |
| Ripple Rejection $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out (nom. })}+1.0 \mathrm{~V}+0.5 \mathrm{~V}_{\mathrm{pp}}, f=1.0 \mathrm{kHz}, \mathrm{I}_{\mathrm{o}}=60 \mathrm{~mA}\right)$ | RR | - | 62 | - | dB |
| ```Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I Iout = 1.0 mA) (Enable Input = 0.9 V, I Iout = 150 mA)``` | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.01 \\ & 190 \\ & 190 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{A}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(EN) }}$ | $0.9$ | - | $0.15$ | V |
| Enable Input Bias Current | $\mathrm{IIB}_{\text {(EN })}$ | - | 3.0 | 100 | nA |
| Output Turn On Time (Enable Input = 0 V to $\mathrm{V}_{\text {in }}$ ) | - | - | 20 | 100 | $\mu \mathrm{s}$ |

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ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=3.8 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{T}_{\text {jmax }}=125^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -3.3 V |  |  |  |  |  |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA} \text { to } 150 \mathrm{~mA}\right)$ | $V_{\text {out }}$ | 3.218 | 3.3 | 3.383 | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=3.8 \mathrm{~V}$ to 6.0 V , $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regload | - | 15 | 45 | mV |
| $\begin{aligned} & \text { Dropout Voltage (Measured at } V_{\text {out }}-2.0 \%, T_{A}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \text { ) } \\ & \text { (lout }=1.0 \mathrm{~mA}) \\ & \text { (lout }=75 \mathrm{~mA}) \\ & \text { (lout }=150 \mathrm{~mA}) \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{gathered} 2.0 \\ 80 \\ 150 \end{gathered}$ | $\begin{gathered} 10 \\ 110 \\ 230 \end{gathered}$ | mV |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 200 | 540 | 700 | mA |
| Ripple Rejection $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out (nom. })}+1.0 \mathrm{~V}+0.5 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=1.0 \mathrm{kHz}, \mathrm{I}_{\mathrm{o}}=60 \mathrm{~mA}\right)$ | RR | - | 62 | - | dB |
| ```Quiescent Current (Enable Input = 0 V) (Enable Input =0.9 V, I Iout = 1.0 mA) (Enable Input = 0.9 V, I Iout = 150 mA)``` | $\mathrm{I}_{\mathrm{Q}}$ |  | $\begin{aligned} & 0.01 \\ & 195 \\ & 195 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{A}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(EN }}$ | $0.9$ | - | $0.15$ | V |
| Enable Input Bias Current | $\mathrm{IIB}_{\text {(EN })}$ | - | 3.0 | 100 | nA |
| Output Turn On Time (Enable Input = 0 V to $\mathrm{V}_{\text {in }}$ ) | - | - | 20 | 100 | $\mu \mathrm{S}$ |

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ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=5.5 \mathrm{~V}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}, \mathrm{T}_{\text {jmax }}=125^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| -5.0 V |  |  |  |  |  |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA} \text { to } 150 \mathrm{~mA}\right)$ | $V_{\text {out }}$ | 4.875 | 5.0 | 5.125 | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=5.5 \mathrm{~V}$ to 6.0 V , $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regioad | - | 15 | 45 | mV |
| $\begin{aligned} & \text { Dropout Voltage (Measured at } \mathrm{V}_{\text {out }}-2.0 \%, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \text { ) } \\ & \text { (lout }=1.0 \mathrm{~mA} \text { ) } \\ & \text { (lout }=75 \mathrm{~mA} \text { ) } \\ & \text { (lout }=150 \mathrm{~mA} \text { ) } \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | - | $\begin{gathered} 2.0 \\ 60 \\ 120 \end{gathered}$ | $\begin{gathered} 10 \\ 100 \\ 180 \end{gathered}$ | mV |
| Output Short Circuit Current | $\mathrm{I}_{\text {out(max) }}$ | 200 | 540 | 700 | mA |
| Ripple Rejection $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out (nom. })}+1.0 \mathrm{~V}+0.5 \mathrm{~V}_{\text {pp }}, f=1.0 \mathrm{kHz}, \mathrm{I}_{\mathrm{o}}=60 \mathrm{~mA}\right)$ | RR | - | 62 | - | dB |
| ```Quiescent Current (Enable Input = 0 V) (Enable Input = 0.9 V, I Iout = 1.0 mA) (Enable Input = 0.9 V, I Iout = 150 mA)``` | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 0.01 \\ & 210 \\ & 210 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{A}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(EN) }}$ | $0.9$ | - | $\begin{gathered} - \\ 0.15 \end{gathered}$ | V |
| Enable Input Bias Current | $\mathrm{IIB}_{\text {(EN })}$ | - | 3.0 | 100 | nA |
| Output Turn On Time (Enable Input = 0 V to $\mathrm{V}_{\text {in }}$ ) | - | - | 20 | 100 | $\mu \mathrm{s}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

NCP500


Figure 2. Dropout Voltage vs. Temperature


Figure 4. Dropout Voltage vs. Temperature


Figure 6. Dropout Voltage vs. Temperature


Figure 3. Dropout Voltage vs. Temperature


Figure 5. Dropout Voltage vs. Temperature


Figure 7. Dropout Voltage vs. Temperature

NCP500


Figure 8. Output Voltage vs. Temperature


Figure 10. Output Voltage vs. Temperature


Figure 12. Quiescent Current vs. Input Voltage


Figure 11. Quiescent Current vs. Temperature


Figure 13. Quiescent Current vs. Input Voltage

NCP500


Figure 14. Ground Pin Current vs. Input Voltage


Figure 16. Current Limit vs. Input Voltage


Figure 15. Ground Pin Current vs. Input Voltage


Figure 17. Ripple Rejection vs. Frequency


Figure 18. Output Noise Density


Figure 19. Line Transient Response


Figure 20. Line Transient Response

Figure 21. Load Transient Response


Figure 22. Load Transient Response


Figure 23. Turn-off Response

NCP500


Figure 24. Output Voltage vs. Input Voltage


Figure 25. Output Voltage vs. Input Voltage


Figure 26. Output Voltage vs. Input Voltage

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output load current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $2 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output load current are kept constant during the measurement. Results are expressed in $\mu \mathrm{VRMS}$ or $\mathrm{n} V \sqrt{\mathrm{~Hz}}$.

## Quiescent Current

The current which flows through the ground pin when the regulator operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$.

## APPLICATIONS INFORMATION

The NCP500 series regulators are protected with internal thermal shutdown and internal current limit. A typical application circuit is shown in Figure 27.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP500 package. Higher values and lower ESR will improve the overall line transient response.

## Output Decoupling (C2)

The NCP500 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) or a minimum output current. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response. Figure 29 shows the stability region for a range of operating conditions and ESR values.

## Noise Decoupling

The NCP500 is a low noise regulator without the need of an external bypass capacitor. It typically reaches a noise level of $50 \mu \mathrm{VRMS}$ overall noise between 10 Hz and 100 kHz . The classical bypass capacitor impacts the start up phase of standard LDOs. However, thanks to its low noise architecture, the NCP500 operates without a bypass element and thus offers a typical $20 \mu$ start up phase.

## Enable Operation

The enable pin will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. The turn-on/turn-off transient voltage being supplied to the enable pin should exceed a slew rate of $10 \mathrm{mV} / \mu \mathrm{s}$ to ensure correct operation. If the enable is not to be used then the pin should be connected to Vin.

## Thermal

As power across the NCP500 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature effect the rate of junction temperature rise for the part. This is stating that when the NCP500 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\Theta J A}}
$$

If $\mathrm{T}_{\mathrm{J}}$ is not recommended to exceed $125^{\circ} \mathrm{C}$, then the NCP500 can dissipate up to $400 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$.

The power dissipated by the NCP500 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} I_{\text {gnd }}\left(l_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right]^{*} l_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 150 mA output current is needed the ground current is extracted from the data sheet curves: $200 \mu \mathrm{~A} @ 150 \mathrm{~mA}$. For a NCP500SN18T1 $(1.8 \mathrm{~V})$, the maximum input voltage will then be 4.4 V , good for a 1 Cell Li -ion battery.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.
Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

## Package Placement

QFN packages can be placed using standard pick and place equipment with an accuracy of $\pm 0.05 \mathrm{~mm}$. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system which physically performs the pick and place operation. Two commonly used types of vision systems are: (1) a vision system that locates a package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. The latter type renders more accurate place but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering feature of the QFN solder joint during solder re-flow.

## Solder Paste

Type 3 or Type 4 solder paste is acceptable.

## Re-flow and Cleaning

The QFN may be assembled using standard IR/IR convection SMT re-flow processes without any special considerations. As with other packages, the thermal profile for specific board locations must be determined. Nitrogen purge is recommended during solder for no-clean fluxes. The QFN is qualified for up to three re-flow cycles at $235^{\circ} \mathrm{C}$ peak (J-STD-020). The actual temperature of the QFN is a function of:

- Component density
- Component location on the board
- Size of surrounding components


Figure 27. Typical Application Circuit


Figure 28. Typical Application Circuit


Figure 29. Stability


Figure 30. Current Boost Regulator

The NCP500 series can be current boosted with a PNP transistor. Resistor R in conjunction with $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by $\mathrm{V}_{\mathrm{BE}}$ of the pass resistor.


Figure 31. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the $V_{B E}$ of $Q 2$ and R1. $I_{S C}=\left(\left(V_{B E Q 2}-i b * R 2\right) / R 1\right)+I_{O(\max )}$ Regulator


Figure 32. Delayed Turn-on
If a delayed turn-on is needed during power up of several voltages then the above schematic can be used. Resistor R, and capacitor C , will delay the turn-on of the bottom regulator. A few values were chosen and the resulting delay can be seen in Figure 33.


Figure 33. Delayed Turn-on
The graph shows the delay between the enable signal and output turn-on for various resistor and capacitor values.


Figure 34. Input Voltages Greater than 6.0 V
A regulated output can be achieved with input voltages that exceed the 6.0 V maximum rating of the NCP500 series with the addition of a simple pre-regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output $\left(V_{\text {out }}\right)$ is shorted to $G_{\text {nd }}$.

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5
(Footprint Compatible with SOT23-5)


QFN 2x2

NCP500

ORDERING INFORMATION

| Device | Nominal Output Voltage | Marking | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| NCP500SN18T1 | 1.8 | LCS | TSOP-5 | 3000 Units/ 7" Tape \& Reel |
| NCP500SN25T1 | 2.5 | LCT |  |  |
| NCP500SN27T1 | 2.7 | LCU |  |  |
| NCP500SN28T1 | 2.8 | LCV |  |  |
| NCP500SN30T1 | 3.0 | LCW |  |  |
| NCP500SN33T1 | 3.3 | LCX |  |  |
| NCP500SN50T1 | 5.0 | LCY |  |  |
| NCP500SQL18T1 | 1.8 | LED | QFN $2 \times 2$ |  |
| NCP500SQL25T1 | 2.5 | LEE |  |  |
| NCP500SQL27T1 | 2.7 | LEF |  |  |
| NCP500SQL28T1 | 2.8 | LEG |  |  |
| NCP500SQL30T1 | 3.0 | LEH |  |  |
| NCP500SQL33T1 | 3.3 | LEJ |  |  |
| NCP500SQL50T1 | 5.0 | LEK |  |  |

For availability of other output voltages, please contact your local ON Semiconductor Sales Representative.

## NCP511

## 150 mA CMOS Low Iq Low-Dropout Voltage Regulator

The NCP511 series of fixed output low dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent current. The NCP511 series features an ultra-low quiescent current of $40 \mu \mathrm{~A}$. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP511 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of $1.0 \mu \mathrm{~F}$. The device is housed in the micro-miniature TSOP-5 surface mount package. Standard voltage versions are $1.5,1.8,2.5,2.7,2.8,3.0,3.3$, and 5.0 V . Other voltages are available in 100 mV steps.

## Features

- Low Quiescent Current of $40 \mu \mathrm{~A}$ Typical
- Low Dropout Voltage of 100 mV at 100 mA
- Excellent Line and Load Regulation
- Maximum Operating Voltage of 6.0 V
- Low Output Voltage Option
- High Accuracy Output Voltage of $2.0 \%$
- Industrial Temperature Range of $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$


## Typical Applications

- Cellular Phones
- Battery Powered Instruments
- Hand-Held Instruments
- Camcorders and Cameras

Figure 1. Representative Block Diagram

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TSOP-5 SN SUFFIX CASE 483
PIN CONNECTIONS AND MARKING DIAGRAM


$$
\begin{aligned}
\mathrm{xxx} & =\text { Version } \\
\mathrm{Y} & =\text { Year } \\
\mathrm{W} & =\text { Work Week } \\
& \\
& \text { (Top View) }
\end{aligned}
$$

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 486 of this data sheet.

NCP511

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
| :---: | :---: | :--- |
| 1 | Vin | Positive power supply input voltage. |
| 2 | Gnd | Power supply ground. |
| 3 | Enable | This input is used to place the device into low-power standby. When this input is pulled low, the device is <br> disabled. If this function is not used, Enable should be connected to Vin. |
| 4 | N/C | No internal connection. |
| 5 | Vout | Regulated output voltage. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $V_{\text {in }}$ | 0 to 6.0 | V |
| Enable Voltage | Enable | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Output Voltage | $V_{\text {out }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| Power Dissipation and Thermal Characteristics <br> Power Dissipation <br> Thermal Resistance, Junction to Ambient | $P_{D}$ $\mathrm{R}_{\text {өJA }}$ | Internally Limited 250 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\text {A }}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Soldering Temperature @ $260^{\circ} \mathrm{C}$ | $\mathrm{T}_{\text {solder }}$ | 10 | sec |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015
Machine Model Method 200 V
2. Latch up capability $\left(85^{\circ} \mathrm{C}\right) \pm 100 \mathrm{~mA} \mathrm{DC}$ with trigger voltage.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out(nom.) }}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {enable }}=\mathrm{V}_{\text {in }}, \mathrm{C}_{\text {in }}=1.0 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.646 \\ & 2.744 \\ & 2.94 \\ & 3.234 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.754 \\ & 2.856 \\ & 3.06 \\ & 3.366 \\ & 5.100 \end{aligned}$ | V |
| Output Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $\left.85^{\circ} \mathrm{C}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}\right)$ 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V | $V_{\text {out }}$ | $\begin{aligned} & 1.455 \\ & 1.746 \\ & 2.425 \\ & 2.619 \\ & 2.716 \\ & 2.910 \\ & 3.201 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 1.8 \\ & 2.5 \\ & 2.7 \\ & 2.8 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.545 \\ & 1.854 \\ & 2.575 \\ & 2.781 \\ & 2.884 \\ & 3.09 \\ & 3.399 \\ & 5.100 \end{aligned}$ | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$ to 6.0 V , $\left.\mathrm{I}_{\text {out }}=10 \mathrm{~mA}\right)$ | Regline | - | 1.0 | 3.5 | mV/V |
| Load Regulation ( $\mathrm{l}_{\text {out }}=1.0 \mathrm{~mA}$ to 150 mA ) | Regload | - | 0.3 | 0.8 | $\mathrm{mV} / \mathrm{mA}$ |
| Output Current ( $\left.\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {out }}=\mathrm{V}_{\text {out(nom) }}-0.1 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{o} \text { (nom.) }}$ | 150 | - | - | mA |
| Dropout Voltage ( $\mathrm{l}_{\text {out }}=100 \mathrm{~mA}$, Measured at $\mathrm{V}_{\text {out }}-3.0 \%$ ) 1.5 V 1.8 V 2.5 V 2.7 V 2.8 V 3.0 V 3.3 V 5.0 V | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | - - - - - - - | $\begin{gathered} 245 \\ 160 \\ 110 \\ 100 \\ 100 \\ 100 \\ 90 \\ 75 \end{gathered}$ | $\begin{aligned} & 350 \\ & 200 \\ & 200 \\ & 200 \\ & 200 \\ & 200 \\ & 200 \\ & 200 \end{aligned}$ | mV |
| Quiescent Current <br> (Enable Input $=0 \mathrm{~V}$ ) <br> (Enable Input $=\mathrm{V}_{\text {in }}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ to $\left.\mathrm{I}_{\mathrm{o}(\text { nom. } .)}\right)$ | ${ }^{1} \mathrm{Q}$ | - | $\begin{aligned} & 0.1 \\ & 40 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 100 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm/ ${ }^{\circ} \mathrm{C}$ |
| Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low) | $\mathrm{V}_{\text {th(en) }}$ | $1.3$ | - | $\overline{0.3}$ | V |
| Output Short Circuit Current $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out (nom) }}+1.0 \mathrm{~V}, \mathrm{~V}_{\text {out }}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {out(max) }}$ | 200 | 400 | 800 | mA |
| Ripple Rejection ( $\mathrm{f}=1.0 \mathrm{kHz}, \mathrm{I}_{0}=60 \mathrm{~mA}$ ) | RR | - | 50 | - | dB |
| Output Noise Voltage ( $\mathrm{f}=20 \mathrm{~Hz}$ to 100 kHz , $\mathrm{I}_{\text {out }}=60 \mathrm{~mA}$ ) | $\mathrm{V}_{n}$ | - | 110 | - | $\mu \mathrm{Vrms}$ |

3. Maximum package power dissipation limits must be observed.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.


Figure 2. Dropout Voltage vs. Temperature


Figure 6. Ground Pin Current vs. Input Voltage


Figure 4. Quiescent Current vs. Temperature


Figure 3. Output Voltage vs. Input Voltage


Figure 5. Ground Pin Current vs. Output Current


Figure 7. Current Limit vs. Input Voltage


Figure 8. Line Transient Response


Figure 9. Line Transient Response


Figure 10. Line Transient Response


Figure 11. Load Transient Response


Figure 12. Load Transient Response

## NCP511



Figure 13. Turn-On Response


Figure 14. Output Noise Density


Figure 15. Ripple Rejection vs. Frequency

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $3.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient power dissipation and thus the maximum available output current.

## APPLICATIONS INFORMATION

A typical application circuit for the NCP511 series is shown in Figure 16.

## Input Decoupling (C1)

A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the NCP511 package. Higher values and lower ESR will improve the overall line transient response.

## Output Decoupling (C2)

The NCP511 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

## Enable Operation

The enable pin will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to $\mathrm{V}_{\mathrm{in}}$.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads a short as possible.


Figure 16. Typical Application Circuit

## Thermal

As power across the NCP511 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP511 has good thermal conductivity through the PCB , the junction temperature will be relatively low with high power dissipation applications.
The maximum dissipation the package can handle is given by:

$$
\mathrm{PD}=\frac{\mathrm{T}_{\mathrm{J}(\max )}-\mathrm{T}_{A}}{R_{\Theta J A}}
$$

If junction temperature is not allowed above the maximum $125^{\circ} \mathrm{C}$, then the NCP511 can dissipate up to 400 mW @ $25^{\circ} \mathrm{C}$.

The power dissipated by the NCP511 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} \operatorname{lgnd}\left(l_{\text {out }}\right)\right]+\left.\left[V_{\text {in }}-V_{\text {out }}\right]^{*}\right|_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 150 mA output current is needed then the ground current from the data sheet is $40 \mu \mathrm{~A}$. For an NCP511SN30T1 (3.0 V), the maximum input voltage will then be 5.6 V .


Figure 17. Output Capacitor vs. Output Current

## APPLICATION CIRCUITS



Figure 18. Current Boost Regulator
The NCP511 series can be current boosted with a PNP transistor. Resistor R in conjunction with $\mathrm{V}_{\mathrm{BE}}$ of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by $\mathrm{V}_{\mathrm{BE}}$ of the pass resistor.


Figure 19. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the $V_{B E}$ of $Q 2$ and R1. $I_{S C}=\left(\left(V_{B E Q 2}-i b * R 2\right) / R 1\right)+I_{(\text {max })}$ Regulator


Figure 21. Delayed Turn-on
The graph shows the delay between the enable signal and output turn-on for various resistor and capacitor values. ages then the above schematic can be used. Resistor R, and capacitor C , will delay the turn-on of the bottom regulator. A few values were chosen and the resulting delay can be seen in Figure 21.


Figure 22. Input Voltages Greater than 6.0 V
A regulated output can be achieved with input voltages that exceed the 6.0 V maximum rating of the NCP511 series with the addition of a simple pre-regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output ( $\mathrm{V}_{\text {out }}$ ) is shorted to $\mathrm{G}_{\text {nd. }}$.

## NCP511

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5
(Footprint Compatible with SOT-23-5)

## NCP511

ORDERING INFORMATION

| Device | Nominal <br> Output Voltage | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP511SN15T1 | 1.5 | LBU |  |  |
| NCP511SN18T1 | 1.8 | LBV |  |  |
| NCP511SN25T1 | 2.5 | LBW |  |  |
| NCP511SN27T1 | 2.7 | LBX | TSOP-5 | 3000 Units/ |
| NCP511SN28T1 | 2.8 | LBY |  |  |
| NCP511SN30T1 | 3.0 | LBZ |  |  |
| NCP511SN33T1 | 3.3 | LCA |  |  |
| NCP511SN50T1 | 5.0 | LCB |  |  |

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## NCP5426

## LDO Regulator/Vibration Motor Driver

The NCP5426 series of fixed output, 150 mA low dropout linear regulators are designed to be an economical solution for a variety of applications. Each device contains a voltage reference unit, an error amplifier, a PNP power transistor, resistors for setting output voltage, an under voltage lockout on the input, an enable pin, and current limit and temperature limit protection circuits.

The NCP5426 is designed for driving a vibration motor using ceramic capacitors on the output. The device is housed in the micro-miniature TSOP-5 surface mount package. The NCP5426 is available in output voltages of 1.2 to 2.0 volts in 0.1 volt increments.

## Features

- Wide Operating Voltage Range to 12 Volts
- Internally Set Output Voltages
- Enable Pin for On/Off Control
- UVLO on the Input Voltage with Hysteresis
- Current and Thermal Protection
- Compatible with Ceramic, Tantalum or Aluminum Electrolytic Capacitors


## Typical Applications

- Vibration Motor Driver


This device contains 47 active transistors.

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TSOP-5
(SOT23-5, SC59-5)
SN SUFFIX
CASE 483

PIN CONNECTIONS AND
MARKING DIAGRAM

$\mathrm{xxx}=$ Version
$Y=$ Year
W = Work Week
(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 494 of this data sheet.

Figure 1. Internal Schematic

DETAILED PIN DESCRIPTION

| Pin | Name | Description |
| :---: | :---: | :--- |
| 1 | Enable | The enable pin allows the user to control the output. A low signal disables the output and places the device <br> into a low current standby mode. |
| 2 | GND | Ground pin. |
| 3 | N/C | This pin is not connected to the device. |
| 4 | Vout | Regulated output voltage. |
| 5 | Vin | Input voltage. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Max Voltage, All Pins | $\mathrm{V}_{\mathrm{MAX}}$ | 12 | V |
| Power Dissipation to Air | $\mathrm{P}_{\mathrm{A}}$ | 150 | mW |
| Power Dissipation, Board Mounted | P | 600 | mW |
| Operating and Storage Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Resistance | $\mathrm{T}_{\mathrm{JA}}$ | 300 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 125 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, for min/max values $T_{A}$ is the operating junction temperature that applies, $\mathrm{V}_{\mathrm{CC}}=3.5 \mathrm{~V}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Voltage | $\mathrm{V}_{\mathrm{CC}}$ | - | - | 12 | V |
| Operating Voltage Turn On, $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}$, Increasing $\mathrm{V}_{\text {CC }}$ | $\mathrm{V}_{\text {CCON }}$ | - | 2.6 | 2.8 | V |
| Operating Voltage Turn Off, $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}$, Decreasing $\mathrm{V}_{\text {CC }}$ | $\mathrm{V}_{\text {CCoff }}$ | 2.0 | 2.1 | 2.2 | V |
| Operating Voltage Hysteresis, $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}$ | $\mathrm{V}_{\text {CC(hyst) }}$ | 400 | 500 | 600 | mV |
| Operating Current No Load | ICC | - | 120 | 240 | $\mu \mathrm{A}$ |
| Operating Current, $\mathrm{V}_{\mathrm{CC}}=1.8 \mathrm{~V}$, Enable High | ICC(uvlo) | - | 80 | 160 | $\mu \mathrm{A}$ |
| Operating Current, Enable Low | $\mathrm{I}_{\mathrm{CC} \text { (off) }}$ | - | - | 0.1 | $\mu \mathrm{A}$ |
| Maximum Output Current, $\mathrm{V}_{\text {out }}=0.95{ }^{*} \mathrm{~V}_{\text {nom }}$ | $\mathrm{l}_{\text {out(max) }}$ | 150 | - | - | mA |
| Over Current Protection, $\mathrm{V}_{\text {out }}=0 \mathrm{~V}$ | $\mathrm{I}_{\text {out(limit) }}$ | - | 270 | - | mA |
| Load Regulation, $\mathrm{V}_{\text {in }}=3.5 \mathrm{~V}$, $\mathrm{I}_{\text {out }} 1.0$ to 100 mA | Regload | - | 30 | 60 | mV |
| Line Regulation, $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}, \mathrm{~V}_{\text {in }} 3.0$ to 5.0 V | Regline | - | 10 | 20 | mV |
| Ripple Rejection, $\mathrm{V}_{\text {in }} 3.5 \mathrm{~V}, \mathrm{f} 120 \mathrm{~Hz}, \mathrm{~V}_{\mathrm{pp}} 1.0 \mathrm{~V}$, $\mathrm{I}_{\text {out }} 30 \mathrm{~mA}$ | RR | 55 | 70 | - | dB |
| Temperature Shutdown | $\mathrm{T}_{\text {std }}$ | - | 150 | - | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{CC}}$ Low Detector Temperature Coefficient, $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}$, $\mathrm{T}=-40 \text { to } 85^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{\mathrm{CC}} \mathrm{H}$ to L/ $/ \Delta \mathrm{T}$ | - | 200 | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {out }}$ Temperature Coefficient | $\Delta \mathrm{V}_{0} / \Delta \mathrm{T}$ | - | 100 | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| Enable Pin High Threshold | $\mathrm{V}_{\text {eh }}$ | 1.6 | - | - | V |
| Enable Pin Low Threshold | $\mathrm{V}_{\text {el }}$ | - | - | 0.4 | V |
| Enable Pin Current, $\mathrm{V}_{\mathrm{e}}=1.6 \mathrm{~V}$ | $\mathrm{l}_{\mathrm{e}}$ | - | 5.0 | 10 | $\mu \mathrm{A}$ |
| -1.3 Volt |  |  |  |  |  |
| Output Voltage, $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}$ | $V_{\text {out }}$ | 1.261 | 1.3 | 1.339 | V |



Figure 2. Load Regulation NCP5426


Figure 4. Quiescent Current vs. Temperature


Figure 3. Current Limit NCP5426


Figure 5. Undervoltage Lockout vs. Temperature


Figure 6. Ripple Rejection vs. Frequency


Figure 7. Load Transient Response


Figure 8. Enable Current vs. Temperature


Figure 10. Line Regulation


Figure 9. Enable Current vs. Temperature


Figure 11. Resistive Transient Response for Switching the Enable Pin, R out $^{\mathbf{- 1}} \mathbf{1 3}$ Ohms


$$
\mathrm{C}_{\text {in }}=\mathrm{C}_{\text {out }}=4.7 \mu \mathrm{~F}
$$

Figure 12. Transient Response for Switching the Enable Pin, Vibration Motor Load

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output load current at a constant temperature and input voltage.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops $2.0 \%$ below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

## Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output load current are kept constant during the measurement. Results are expressed in $\mu \mathrm{VRMS}$ or $\mathrm{nV} \sqrt{\mathrm{Hz}}$.

## Quiescent Current

The current which flows through the ground pin when the regulator operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

## Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $150^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

## Maximum Package Power Dissipation

The power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$.

## APPLICATIONS INFORMATION

The following description will assist the system designer to correctly use the NCP5426 in an application. The NCP5426 is designed specifically for use with inductive loads, typically Vibration Motors. The LDO is capable of using ceramic and tantalum capacitors. Please refer to Figure 13 for a typical system schematic.

## Input Decoupling

A capacitor, C 1 , is necessary on the input for normal operation. A ceramic or tantalum capacitor with a minimum value of $1.0 \mu \mathrm{~F}$ is required. Higher values of capacitance and lower ESR will improve the overall line and load transient response.

## Output Decoupling

A capacitor, C2, is required for the NCP5426 to operate normally. A ceramic or tantalum capacitor will suffice. The selection of the output capacitor is dependant upon several factors: output current, power up and down delays, inductive kickback during power up and down. It is recommended the output capacitor be as close to the output pin and ground pin for the best system response.

## Enable Pin

The enable pin will turn on or off the regulator. The enable pin is active high. The internal input resistance of the enable pin is high which will keep the current very low when the pin is pulled high. A low threshold voltage permits the NCP5426 to operate directly from microprocessors or controllers.

## Thermal

As power across the NCP5426 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and the ambient temperature effect the rate of junction temperature rise for the part. This is stating that when the NCP5426 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$
P D=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

$\mathrm{T}_{\mathrm{J}}$ is not recommended to exceed $125^{\circ} \mathrm{C}$. The NCP5426 can dissipate up to $400 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$. The power dissipated by the NCP5426 can be calculated from the following equation:

$$
P_{\text {tot }}=\left[V_{\text {in }}{ }^{*} \operatorname{lgnd}\left(I_{\text {out }}\right)\right]+\left[V_{\text {in }}-V_{\text {out }}\right] * l_{\text {out }}
$$

or

$$
\mathrm{V}_{\text {inMAX }}=\frac{\mathrm{P}_{\text {tot }}+\mathrm{V}_{\text {out }}{ }^{*} \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 150 mA output current is needed then the ground current is extracted from the data sheet curves: $200 \mu \mathrm{~A}$ @ 150 mA . For an NCP5426SN18T1 (1.8 V), the maximum input voltage will then be 4.4 V , good for a 1 Cell Li -ion battery.

## Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction. Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.


Figure 13. Typical Applications Circuit for Driving a Vibration Motor


Figure 14. Timing Diagram

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5
(Footprint Compatible with SOT23-5)

NCP5426

ORDERING INFORMATION

| Device | Nominal Output Voltage* | Marking | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| NCP5426SN13T1 | 1.3 | LDZ | TSOP-5 | 3000 Units/ 7" Tape \& Ree |
| NCP5426SN13T2 | 1.3 | LDZ | TSOP-5 |  |

*Contact your ON Semiconductor sales representative for other Output Voltage options.


Figure 15. T1 Reel Configuration/Orientation


Figure 16. T2 Reel Configuration/Orientation

## CS8182

## Micropower 200 mA Low Dropout Tracking Regulator/Line Driver

The CS8182 is a monolithic integrated low dropout tracking regulator designed to provide adjustable buffered output voltage that closely tracks ( $\pm 10 \mathrm{mV}$ ) the reference input. The output delivers up to 200 mA while being able to be configured higher, lower or equal to the reference voltages.

The output has been designed to operate over a wide range ( 2.8 V to 45 V ) while still maintaining excellent DC characteristics. The CS8182 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45 V load dump transients and -50 V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The $\mathrm{V}_{\mathrm{REF}} /$ ENABLE lead serves two purposes. It is used to provide the input voltage as a reference for the output and it also can be pulled low to place the device in sleep mode where it nominally draws less than $30 \mu \mathrm{~A}$ from the supply.

## Features

- 200 mA Source Capability
- Output Tracks within $\pm 10 \mathrm{mV}$ Worst Case
- Low Dropout (0.35 V typ. @ 200 mA )
- Low Quiescent Current
- Thermal Shutdown
- Short Circuit Protection
- Wide Operating Range
- Internally Fused Leads in SO-8 Package


Figure 1. Block Diagram

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DF SUFFIX
CASE 751


D2PAK 5-PIN
DPS SUFFIX
CASE 936A

## PIN CONNECTIONS AND MARKING DIAGRAMS


$\begin{array}{ll}\text { A } & =\text { Assembly Location } \\ \text { WL, L } & =\text { Wafer Lot } \\ \text { YY, Y } & =\text { Year } \\ \text { WW, W } & =\text { Work Week }\end{array}$

ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8182YDF8 | SO-8 | 95 Units/Rail |
| CS8182YDFR8 | SO-8 | 2500 Tape \& Reel |
| CS8182YDPS5 | D2PAK 5-PIN | 50 Units/Rail |
| CS8182YDPSR5 | D$^{2}$ PAK 5-PIN | 750 Tape \& Reel |

* Consult your local sales representative for

SO-8 with exposed pads package option.

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Storage Temperature |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Supply Voltage Range (continuous) |  | -15 to 45 | V |
| Supply Voltage Range (normal, continuous) |  | 3.4 to 45 | V |
| Peak Transient Voltage ( $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$, Load Dump Transient $=31 \mathrm{~V}$ ) |  | 45 | V |
| Voltage Range (Adj, $\mathrm{V}_{\text {OUT }}$, $\mathrm{V}_{\text {REF }} /$ ENABLE) |  | -10 to 45 | V |
| Maximum Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| ```Package Thermal Resistance, SO-8: Junction-to-Case, \(\mathrm{R}_{\text {өJc }}\) Junction-to-Ambient, R ®JA``` |  | $\begin{gathered} 45 \\ 165 \end{gathered}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, D²PAK, 5-Pin: Junction-to-Case, R өJc Junction-to-Ambient, $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{gathered} 4.0 \\ 10-50^{* *} \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ESD Capability (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
${ }^{* *}$ Depending on thermal properties of substrate. $R_{\theta J A}=R_{\theta J C}+R_{\theta C A}$

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$; $\mathrm{V}_{\text {REF }} /$ ENABLE $>2.75 \mathrm{~V} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{OUT}} \geq 10 \mu \mathrm{~F}$;
$0.1 \Omega<$ Cout-ESR $<1.0 \Omega @ 10 \mathrm{kHz}$, unless otherwise specified.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Regular Output

| $V_{\text {REF }}$ - Vout <br> $V_{\text {OUT }}$ Tracking Error | $4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 200 \mathrm{~mA}$, Note 2 $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=30 \mathrm{~mA}, \mathrm{~V}_{\text {REF }}=5.0 \mathrm{~V}$, Note 2 | $\begin{aligned} & -10 \\ & -5.0 \end{aligned}$ | _ | $\begin{gathered} 10 \\ 5 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\begin{aligned} & \text { lout }=100 \mu \mathrm{~A} \\ & \text { IOUT }=30 \mathrm{~mA} \\ & \text { lout }=200 \mathrm{~mA} \end{aligned}$ |  | $\begin{gathered} 100 \\ - \\ 350 \end{gathered}$ | $\begin{aligned} & 150 \\ & 500 \\ & 600 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Line Regulation | $4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, Note 2 | - | - | 10 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 200 \mathrm{~mA}$, Note 2 | - | - | 10 | mV |
| Adj Lead Current | Loop in Regulation | - | 0.2 | 1.0 | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, \mathrm{~V}_{\text {REF }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=90 \%$ of $\mathrm{V}_{\text {REF }}$, Note 2 | 225 | - | 700 | mA |
| Quiescent Current (lin $-\mathrm{l}_{\text {OUT }}$ ) | $\begin{aligned} & \mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=200 \mathrm{~mA} \\ & \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {REF }} \text { ENABLE }=0 \mathrm{~V} \end{aligned}$ | - | $\begin{aligned} & 15 \\ & 75 \\ & 30 \end{aligned}$ | $\begin{gathered} 25 \\ 150 \\ 55 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Reverse Current | $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 0.2 | 1.5 | mA |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$, $\mathrm{l}_{\text {OUT }}=200 \mathrm{~mA}, 4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | 60 | - | - | dB |
| Thermal Shutdown | GBD | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |

$\mathrm{V}_{\mathrm{REF}} / \mathrm{ENABLE}$

| Enable Voltage | - | 0.80 | 2.00 | 2.75 | V |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | $V_{\text {REF/ENABLE }}$ | - | 0.2 | 1.0 | $\mu \mathrm{~A}$ |

2. V OUT connected to Adj lead.

## PACKAGE PIN DESCRIPTION

| Package Lead Number |  |  |  |
| :---: | :---: | :---: | :--- |
| SO-8 | D²PAK 5-PIN | Lead Symbol |  |
| 8 | 1 |  | Function |
| 1 | 2 | $\mathrm{~V}_{\text {OUT }}$ | Regulated output. |
| $2,3,6,7$ | 3 | GND | Ground. |
| 4 | 4 | Adj | Adjust lead. |
| 5 | 5 | $\mathrm{~V}_{\text {REF }} /$ ENABLE | Reference voltage and ENABLE input. |

## CIRCUIT DESCRIPTION

## ENABLE Function

By pulling the $\mathrm{V}_{\mathrm{REF}} / \mathrm{ENABLE}$ lead below 2.0 V typically, (see Figure 5 or Figure 6), the IC is disabled and enters a sleep state where the device draws less than $55 \mu \mathrm{~A}$ from supply. When the $\mathrm{V}_{\mathrm{REF}} / E N A B L E$ lead is greater than 2.75 V , $\mathrm{V}_{\text {OUT }}$ tracks the $\mathrm{V}_{\text {REF }} /$ ENABLE lead normally.


Figure 2. Tracking Regulator at the Same Voltage


Figure 4. Tracking Regulator at Lower Voltages


Figure 6. Alternative ENABLE Circuit

[^10]
## Output Voltage

The output is capable of supplying 200 mA to the load while configured as a similiar (Figure 2), lower (Figure 4), or higher (Figure 3) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the $\mathrm{V}_{\text {REF }}$ lead as the non-inverting.

The device can also be configured as a high-side driver as displayed in Figure 7


Figure 3. Tracking Regulator at Higher Voltages


Figure 5. Tracking Regulator with ENABLE Circuit


Figure 7. High-Side Driver

## APPLICATION NOTES

## Switched Application

The CS8182 has been designed for use in systems where the reference voltage on the $\mathrm{V}_{\mathrm{REF}} / E N A B L E$ pin is continuously on. Typically, the current into the $\mathrm{V}_{\mathrm{REF}} / \mathrm{ENABLE}$ pin will be less than $1.0 \mu \mathrm{~A}$ when the voltage on the $\mathrm{V}_{\text {IN }}$ pin (usually the ignition line) has been switched out ( $\mathrm{V}_{\text {IN }}$ can be at high impedance or at ground.) Reference Figure 8.


Figure 8.

## External Capacitors

The output capacitor for the CS8182 is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to $-40^{\circ} \mathrm{C}$, a capacitor rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators," document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 9) is:

$$
\begin{align*}
\operatorname{PD}(\max )= & \left\{\mathrm{V}_{\operatorname{IN}}(\max )-\mathrm{V}_{\text {OUT }}(\min )\right\} \operatorname{IOUT}(\max ) \\
& +\mathrm{V}_{\operatorname{IN}}(\max ) \mathrm{I}_{\mathrm{Q}} \tag{1}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of PD (max) is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta J A}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.


Figure 9. Single Output Regulator with Key Performance Parameters Labeled

## Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J \mathrm{~J}}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it is a function of package type. $\mathrm{R}_{\Theta C S}$ and $\mathrm{R}_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## MC33565

## Smart Voltage Regulator for Peripheral Card Applications

The MC33565 Low Drop Out Voltage Regulator is designed for computer peripheral card applications, allowing glitch-free transitions from "sleep" to "active" system modes. It has internal logic circuitry to detect whether there is a 5 V supply ("active" system mode) or an auxiliary 3.3 V supply ("sleep" system mode). A guaranteed 3.3 V regulated output voltage at 200 mA is always available even if the main 5 V supply drops out.

The regulated 3.3 V output voltage is provided by either an internal dropout 5.0 V-to-3.3 V voltage regulator or an external P-channel MOSFET, depending on the system being in the "active" or "sleep" mode.

## Features

- Glitch-Free Transition from "Sleep" to "Active" Mode
- Compatible with Instantly Available PC Systems
- Output Current up to 200 mA
- Output Regulated to $2 \%$ over Temperature
- Excellent Line and Load Regulation (0.4\%)
- Prevents Reverse Current Flow during Sleep Mode


## Applications

- Computer
- Ethernet
- PCI/NIC Cards


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## 200 mA INTELLIGENT LDO REGULATOR WITH SMART BYPASS CONTROL

(2) | MARKING |
| :---: |
| DIAGRAM |

A = Assembly Location
L Wafer Lot
Y = Year
W = Work Week


## MC33565

MAXIMUM RATINGS $\left(T_{\mathrm{C}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted) (Note 1)

| Parameter | Symbol | Max Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage, $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\max }$ | 7.0 | Vdc |
|  | $\mathrm{V}_{\min }$ | -0.5 | Vdc |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{a}}$ | -5 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | -5 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 seconds) | $\mathrm{T}_{\mathrm{L}}$ | 300 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance, Junction to Ambient | $\mathrm{R}_{\theta \mathrm{JJA}}($ Note 2$)$ | 171 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction to Case | $\mathrm{R}_{\text {日JC }}$ | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

1. Minimum pad test board with 5 mil wide and 2.8 mil thick copper traces 1 inch long.

AC ELECTRICAL SPECIFICATIONS (Notes 2, 3, 4, and 5)

| Parameter | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive High Delay $\left(V_{\text {in }}\right.$ ramping up $)$ <br> $C_{\text {Drive }}=1.2 \mathrm{nF}$, measured from $+5 \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {thresHi }}$ to $\mathrm{V}_{\text {Drive }}=2 \mathrm{~V}$ | $\mathrm{t}_{\mathrm{DH}}$ | - | 1.3 | 3.5 | $\mu \mathrm{~S}$ |
| Drive Low Delay <br> $\mathrm{C}_{\text {Drive }}=1.2 \mathrm{nF}$, measured from $+5 \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {thresLo }}$ to $\mathrm{V}_{\text {Drive }}=2 \mathrm{~V}$ | $\mathrm{t}_{\mathrm{DL}}$ | - | 1.2 | 3.5 | $\mu \mathrm{~S}$ |

2. See 5 V Detect Thresholds Diagram.
3. Recommended source impedance for 5 V supply: $\leq 0.25 \Omega$. This will ensure that $\mathrm{I}_{0} \times \mathrm{R}_{\text {source }}<\mathrm{V}_{\text {hyst }}$, thus avoiding drive out toggling during 5 V detect threshold transitions.
4. See Figure 2. Application Block Diagram.
5. See Timing Diagram.

## DC ELECTRICAL CHARACTERISTICS (Note 6)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $+5 \mathrm{~V}_{\text {in }}$ Supply Voltage Range | $+5 \mathrm{~V}_{\text {in }}$ | 4.3 | 5.0 | 5.5 | Vdc |
| Reverse Leakage Current from Output | $\mathrm{I}_{\text {reverse }}$ | - | - | 25 | $\mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {Aux }}$ quiescent current | - | - | - | 3.0 | mA |
| $+5 \mathrm{~V}_{\text {in }}$ quiescent current, operating | - | - | - | 10 | mA |
| Load Capacitance (Note 7) | $\mathrm{C}_{\text {load }}$ | 4.7 | 22 | - | $\mu \mathrm{F}$ |

REGULATOR OUTPUT

| Output Voltage $\begin{aligned} & \left(4.3 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 5.5 \mathrm{~V}, 0 \mathrm{~mA} \leq \mathrm{I}_{0} \leq 200 \mathrm{~mA}\right) \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \left(\mathrm{~T}_{\mathrm{J}}=-5^{\circ} \mathrm{C} \text { to } 150^{\circ} \mathrm{C}\right) \end{aligned}$ | +3.3 $\mathrm{V}_{\text {out }}$ | $\begin{aligned} & 3.267 \\ & 3.234 \end{aligned}$ | $\begin{aligned} & 3.30 \\ & 3.30 \end{aligned}$ | $\begin{aligned} & 3.333 \\ & 3.366 \end{aligned}$ | Vdc |
| :---: | :---: | :---: | :---: | :---: | :---: |
| In-to-Out Voltage $\left(3.9 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 4.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{aux}}=3.3 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{d}}$ | 3.0 | - | - | Vdc |
| Voltage Out at Max Voltage In $\left(\mathrm{V}_{\mathrm{in}}=7 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {outmax }}$ | 3.1 | 3.3 | 3.5 | Vdc |
| Line Regulation $\left(\mathrm{I}_{\mathrm{o}}=200 \mathrm{~mA}\right)$ | - | - | - | 0.4 | \% |
| Load Regulation $\left(\mathrm{I}_{0}=0 \text { to } 200 \mathrm{~mA}\right)$ | - | - | - | 0.4 | \% |
| Short Circuit Current | $I_{\text {sc }}$ | 230 | 435 | - | mA |

## 5 V DETECT

| Low Threshold Voltage <br> $\left(+5 \mathrm{~V}_{\text {in }}\right.$ falling $)$ | $\mathrm{V}_{\text {thresLo }}$ | 3.9 | 4.02 | 4.3 | Vdc |
| :--- | :---: | :---: | :---: | :---: | :---: |
| High Threshold Voltage <br> $\left(+5 \mathrm{~V}_{\text {in }}\right.$ rising $)$ | $\mathrm{V}_{\text {thresHi }}$ | - | 4.17 | 4.3 | Vdc |
| Hysteresis | $\mathrm{V}_{\text {Hyst }}$ | 0.12 | 0.15 | 0.18 | Vdc |

6. $-5^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{a}}<70^{\circ} \mathrm{C}, 4.3 \mathrm{~V}<\mathrm{V}_{\text {in }}<5.5 \mathrm{~V}, \mathrm{C}_{\text {load }}=4.7 \mu \mathrm{~F}$ unless otherwise noted
7. $4.7 \mu \mathrm{~F}$ minimum over temperature; $22 \mu \mathrm{~F}$ recommended; $500 \mathrm{~m} \Omega$ ESR maximum.

## MC33565

DC ELECTRICAL CHARACTERISTICS (continued) (Note 8)
DRIVE OUTPUT

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output peak source Current $\left(+5 \mathrm{~V}_{\text {in }}>\mathrm{V}_{\text {thres }} \mathrm{Hi}\right.$, Pin 8 current into 1.2 nF ) | $I_{\text {peak }}$ | 15 | - | - | mA |
| Output peak sink Current $\left(+5 \mathrm{~V}_{\text {in }}<\mathrm{V}_{\text {thresLo }} \text {, Pin } 8 \text { current into } 1.2 \mathrm{nF}\right. \text { ) }$ | $I_{\text {peak }}$ | 15 | - | - | mA |
| Low Output Voltage $\left(\mathrm{I}_{\mathrm{oL}}=200 \mu \mathrm{~A}, \mathrm{~V}_{\text {in }}<\mathrm{V}_{\text {thresLo }}\right)$ | VoL | - | 145 | 200 | mVdc |
| High Output Voltage $\left(\mathrm{I}_{\mathrm{OH}}=200 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{oH}}$ | 3.4 | $\mathrm{V}_{\text {in }}-0.85$ | - | Vdc |

8. $-5^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{a}}<70^{\circ} \mathrm{C}, 4.3 \mathrm{~V}<\mathrm{V}_{\text {in }}<5.5 \mathrm{~V}, \mathrm{C}_{\text {load }}=4.7 \mu \mathrm{~F}$ unless otherwise noted

DEVICE MARKING

| Device | Type | Sub-type | Marking (1st Line) |
| :---: | :---: | :---: | :---: |
| MC33565D | 3.3 V | - | MC565 |



Figure 1. Functional Block Diagram

## PIN ASSIGNMENTS AND FUNCTIONS

| PIN \# | PIN NAME | PIN DESCRIPTION |
| :---: | :---: | :--- |
| 1 | $+5 \mathrm{~V}_{\text {in }}$ | This is the input supply for the IC. Typical voltage 5 V. |
| 2,5 | N/C | Reserved |
| 3 | $+3.3 \mathrm{~V}_{\text {in }}$ | Auxiliary input. Typical voltage 3.3 V. |
| 4 | Gnd | Logic and Power Gnd. |
| 6 | Sense in | Load-sense voltage input to internal regulator. |
| 7 | $+3.3 \mathrm{~V}_{\text {out }}$ | 3.3 V output provided to the application circuit (output current is sourced to this pin from the 5 V input.) |
| 8 | Drive out | This output drives a P-channel MOSFET with up to 1.2 nF of "effective" gate capacitance. <br> Recommended device is MGSF1P02ELT MOSFET. Drive out has active internal pull-up and <br> pull-down circuitry to guarantee fast transitions. |

## OPERATING DESCRIPTION

The MC33565 is designed for power managed computer applications such as peripheral card interface (PCI) and network interface cards (NIC) where glitch-free transition between +3.3 V and +5 V is necessary. In this type of application, the presence of a +5 V supply represents the "active" system mode, while the presence of +3.3 V represents the "sleep" system mode. The MC33565 complies with the instantly available requirements as specified by the Advanced Configuration and Power Interface (ACPI) standards set by Intel, Microsoft, and Toshiba. A regulated output voltage of +3.3 V is available even when the +5 V supply has been shut down and only the +3.3 V auxiliary supply is available.

The MC33565 has dual inputs, $+5 \mathrm{~V}_{\text {in }}$ and $+3.3 \mathrm{~V}_{\text {in }}$. It functions as a linear regulator when $\mathrm{V}_{\text {in }}$ is greater than 4.02 V. Below this threshold value, the linear regulator turns off and the auxiliary DRIVE OUT feature allows the use of an external P -channel MOSFET to supply power to the output. The MC33565 connects the $+3.3 \mathrm{~V}_{\text {in }}$ auxiliary power supply directly to the output P -channel MOSFET.

## 5 V Detect

Internal circuitry detects if the system is being powered from a +5 V supply or a 3.3 V auxiliary supply. During normal operating conditions, the MC33565 is powered by the +5 V supply. A regulated output voltage of +3.3 V is provided by an internal low drop out 5.0 V -to- 3.3 V voltage regulator. The gate of the P -channel MOSFET is driven high and therefore disabled.

If the +5 V supply is not available or the supply voltage drops below a typical threshold value of 4.02 V , the DRIVE OUT goes low. This enables the external P -channel MOSFET, connecting the +3.3 V auxiliary supply to the load and allowing the load to remain powered even though the +5 V supply is not available.

As the supply voltage begins to rise, the linear regulator output will be disabled until $\mathrm{V}_{\text {in }}$ reaches a typical threshold voltage of 4.17 V . The load continues to be powered by the auxiliary DRIVE OUT while $\mathrm{V}_{\text {in }}$ reaches the threshold voltage. When $V_{\text {in }}$ reaches the threshold voltage, the gate of the external P-channel MOSFET is driven high and turns off.

The 5 V detect logic is active throughout the entire range of the +5 V supply ramp-up. The DRIVE OUT signal is never turned ON or OFF inappropriately during ramp-up of the $+5 \mathrm{~V}_{\text {in }}$ supply. The +3.3 V output voltage never drops below 3.0 V while the +5 V supply is above the 5 V DETECT minimum threshold of 3.9 V .

## Input Blocking

The internal NPN pass transistor of the low drop out regulator (LDO) ensure that no significant reverse current will flow from $\mathrm{V}_{\text {out }}$ to $\mathrm{V}_{\text {in }}$ or GND when the $+5 \mathrm{~V}_{\text {in }}$ input is not powered and the $+3.3 \mathrm{~V}_{\text {in }}$ supply is present.

## P-Channel MOSFET Polarity

It is imperative that the polarity of the P -channel MOSFET be observed because the P -channel MOSFET body diode will be connected between the auxiliary power supply and the load. The P-channel MOSFET drain is connected to the $+3.3 \mathrm{~V}_{\text {in }}$ auxiliary power supply; source is connected to load; gate is connected to DRIVE OUT. If the polarity is reversed with the drain connected to the load and the source connected to the auxiliary supply, the body diode could be forward biased if the auxiliary supply is not present. Consequently the linear regulator would not turn off and it would supply current to everything on the auxiliary supply rail.

## Hysteresis

The internal 5 V DETECT has a typical high threshold voltage of 4.17 V and a typical low threshold voltage of 4.02 V . This results in a typical hysteresis of 150 mV for noise immunity. The input supply voltage, $\mathrm{V}_{\mathrm{in}}$, must drop 150 mV while the linear regulator is supplying power to the load before the auxiliary DRIVE OUT is enabled.

## External Compensation

An external compensation capacitor with a minimum value of $4.7 \mu \mathrm{~F}$ is required for the linear regulator to be stable. Increasing the capacitance will improve the overall transient response. The equivalent series resistance (ESR) of the capacitor should be less than $1 \Omega$ in order for the output voltage to be maintained within tight tolerance.

## Sense

The SENSE IN pin provides tight regulation of the load voltage while the 5 V supply is present even with varying load current. To take advantage of the SENSE PIN, connect pin 6 as close to the load as possible. Use a separate trace to connect the source of the MOSFET to the load. Refer to Figure 2.


Figure 2.

## Board Layout

The PCB component layout shown in Figure 27 is designed for an input range of 4.3 V to 5.5 V ; an output voltage range of 3.267 V to 3.333 V ; and an output current of 200 mA .

## Current Limit and Thermal Shutdown

Full protection with both current limit and thermal shutdown is provided. Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at $170^{\circ} \mathrm{C}$, the output is disabled. There
is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.


Figure 3. Application Block Diagram


Figure 4. Typical Application Schematic


Figure 5. Alternative Application: 5 V or 3.3 V Card Input with Hot Swap Circuitry

TYPICAL CHARACTERISTICS


NOTE:
(1) VIN rise and fall times ( $10 \%$ to $90 \%$ ) to be $\geq 100 \mu \mathrm{~s}$.

Figure 6. 5V Detect Thresholds Diagram


NOTE: $\mathrm{V}_{\text {out }}$ capacitor $\geq 4.7 \mu \mathrm{~F}$ over operating temperature range. Maximum ESR permissible $=500 \mathrm{~m} \Omega$ over operating temperature range.

Figure 8. Predicted Gain and Phase at Zero Load Current


Figure 9. Predicted Gain and Phase at Full Load Current


Figure 10. Drive Out High Voltage (external P-channel MOSFET turned off) versus Ambient Temperature


Figure 11. Drive Out Low Voltage (external P-channel MOSFET turned on) versus Ambient Temperature


Figure 12. Drive Out Peak Sink Current versus Ambient Temperature


Figure 14. Output Voltage versus Ambient Temperature


Figure 15. Line Regulation versus Ambient Temperature


Figure 16. Load Regulation versus Ambient Temperature


Figure 18. Quiescent Current versus Ambient Temperature (3.3 V aux only)


Figure 20. Reverse Leakage Current from Output versus Ambient Temperature


Figure 17. Quiescent Current versus Ambient Temperature ( 5 V only)


Figure 19. Short Circuit Current versus Ambient Temperature


Figure 21. Lower Comparator Threshold versus Ambient Temperature


Figure 22. Upper Comparator Threshold versus Ambient Temperature

$\mathrm{T}_{\mathrm{A}}$, TEMPERATURE ( ${ }^{\circ} \mathrm{C}$ )
Figure 24. Drive Out Fall Delay (after $\mathrm{V}_{\text {in }}$ crosses threshold) versus Ambient Temperature


Figure 23. Drive Out Rise Delay (after $\mathrm{V}_{\text {in }}$ crosses threshold) versus Ambient Temperature


TRACE 1: $\mathrm{V}_{\text {in }}$ stepping from 5 V to $\mathrm{V}_{\text {thresLo }}$
TRACE 2: $\mathrm{V}_{\text {out }}$ switching from regulator output to $\mathrm{V}_{\text {aux }}$
Figure 25. Bypass Mode Transition


Figure 26. Load Transient Response


Figure 27. PCB Component Layout


Figure 28. PCB Copper Layout

PARTS LIST

| Qty | Reference | Part/Description | Vendor | Notes |
| :---: | :---: | :---: | :---: | :---: |
| 3 | C1, C3, C5 | $0.1 \mu$ F Ceramic Capacitor | Various | - |
| 2 | C2, C4 | $10 \mu$ F Tantalum Capacitor | Various | - |
| 1 | U1 | MC33565 | ON Semiconductor | - |
| 1 | Q1 | MGSF1P02ELT | ON Semiconductor | P-Channel MOSFET |

## MC33275

## 300 mA, 2.5 V, Low Dropout Voltage Regulator

The MC33275 series are micropower low dropout voltage regulators available in a wide variety of output voltages as well as packages, DPAK, SOT-223, and SOP-8 surface mount packages. These devices feature a very low quiescent current and are capable of supplying output currents up to 300 mA . Internal current and thermal limiting protection are provided by the presence of a short circuit at the output and an internal thermal shutdown circuit.

The MC33275 is available as a MC33375 which includes an On/Off control.

Due to the low input-to-output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

## Features:

- Low Quiescent Current ( $125 \mu \mathrm{~A}$ )
- Low Input-to-Output Voltage Differential of 25 mV at $\mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$, and 260 mV at $\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}$
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of only $0.33 \mu \mathrm{~F}$ for 2.5 V Output Voltage
- Internal Current and Thermal Limiting

Simplified Block Diagram


This device contains 41 active transistors

## ON Semiconductor ${ }^{\text {T }}$

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## LOW DROPOUT MICROPOWER VOLTAGE REGULATOR



ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 519 of this data sheet.

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, for min $/$ max values $\mathrm{T}_{\mathrm{J}}=-40^{\circ} \mathrm{C}$ to $\left.+125^{\circ} \mathrm{C}\right)$

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 13 | Vdc |
| Power Dissipation and Thermal Characteristics $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Maximum Power Dissipation Case 751 (SOP-8) D Suffix <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 369A (DPAK) DT Suffix <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> Case 318E (SOT-223) ST Suffix <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case | $\mathrm{P}_{\mathrm{D}}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJc }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\theta \mathrm{JA}}$ <br> $\mathrm{R}_{\text {өJC }}$ | Internally Limited <br> 160 25 <br> 92 <br> 6.0 <br> 245 <br> 15 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Output Current | 10 | 300 | mA |
| Maximum Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{L}}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, for min $/$ max values $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, Note 1)


CURRENT PARAMETERS

| Characteristic |  | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Quiescent Current ON Mode | $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ | $\mathrm{I}_{\mathrm{Q}}$ | - | 125 | 200 | $\mu \mathrm{A}$ |
| Quiescent Current ON Mode SAT <br> 2.5 V Suffix <br> 3.0 V Suffix <br> 3.3 V Suffix <br> 5.0 V Suffix | $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}-0.5\right] \mathrm{V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}, \text { Note } 2$ | $\mathrm{I}_{\mathrm{Q}}$ | — | $\begin{aligned} & 1100 \\ & 1500 \\ & 1500 \\ & 1500 \end{aligned}$ | $\begin{aligned} & 1500 \\ & 2000 \\ & 2000 \\ & 2000 \end{aligned}$ | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}, \mathrm{V}_{\mathrm{O}}$ Shorted | l LIMIT | - | 450 | - | mA |

THERMAL SHUTDOWN

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Thermal Shutdown | - | - | 150 | - | ${ }^{\circ} \mathrm{C}$ |

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent Current is measured where the PNP pass transistor is in saturation. $\mathrm{V}_{\mathrm{in}}=\left[\mathrm{V}_{\mathrm{O}}-0.5\right] \mathrm{V}$ guarantees this condition.

## DEFINITIONS

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage - The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage - The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.

Maximum Power Dissipation - The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current - Current which is used to operate the regulator chip and is not delivered to the load.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Maximum Package Power Dissipation - The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. $150^{\circ} \mathrm{C}$. The junction temperature is rising while the
difference between the input power $\left(\mathrm{V}_{\mathrm{CC}} \mathrm{X} \mathrm{I}_{\mathrm{CC}}\right)$ and the output power $\left(V_{\text {out }} X \mathrm{I}_{\text {out }}\right)$ is increasing.

Depending on ambient temperature, it is possible to calculate the maximum power dissipation and so the maximum current as following:

$$
P d=\frac{T_{J}-T_{A}}{R_{\theta J A}}
$$

The maximum operating junction temperature $\mathrm{T}_{\mathrm{J}}$ is specified at $150^{\circ} \mathrm{C}$, if $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, then $\mathrm{P}_{\mathrm{D}}$ can be found. By neglecting the quiescent current, the maximum power dissipation can be expressed as:

$$
I_{\text {out }}=\frac{P_{D}}{V_{C C}-V_{o u t}}
$$

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature $\left(150^{\circ} \mathrm{C}\right.$ for MC 33275$)$ and ambient temperature.

$$
R_{\theta J A}=\frac{T_{J}-T_{A}}{P_{D}}
$$



Figure 1. Line Transient Response


Figure 2. Line Transient Response


Figure 3. Load Transient Response


Figure 4. Load Transient Response


Figure 5. Output Voltage versus Input Voltage


Figure 6. Dropout Voltage versus Output Current


Figure 7. Dropout Voltage versus Temperature


Figure 9. Ground Pin Current versus Ambient Temperature


Figure 8. Ground Pin Current versus Input Voltage


Figure 10. Output Voltage versus Ambient Temperature $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out1 }}+1 \mathrm{~V}\right)$


Figure 11. Output Voltage versus Ambient Temperature ( $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}$ )


Figure 12. Ripple Rejection


Figure 13. Ripple Rejection

## APPLICATIONS INFORMATION



Figure 14. Typical Application Circuit

The MC33275 regulators are designed with internal current limiting and thermal shutdown making them user-friendly. Figure 14 is a typical application circuit. The output capability of the regulator is in excess of 300 mA , with a typical dropout voltage of less than 260 mV . Internal protective features include current and thermal limiting.

## EXTERNAL CAPACITORS

These regulators require only a $0.33 \mu \mathrm{~F}$ (or greater) capacitance between the output and ground for stability for $2.5 \mathrm{~V}, 3.0 \mathrm{~V}$, and 3.3 V output voltage options. Output voltage options of 5.0 V require only $0.22 \mu \mathrm{~F}$ for stability. The output capacitor must be mounted as close as possible to the MC33275. If the output capacitor must be mounted further than two centimeters away from the MC33275, then a larger value of output capacitor may be required for stability. A value of $0.68 \mu \mathrm{~F}$ or larger is recommended. Most type of aluminum, tantalum, or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below $25^{\circ} \mathrm{C}$. An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths, more than 4 inches. This will reduce the circuit's sensitivity to the input line impedance at high frequencies. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. Figure 15 shows the ESR that allows the LDO to remain stable for various load currents.


Figure 15. ESR for $\mathrm{V}_{\text {out }}=3.0 \mathrm{~V}$
Applications should be tested over all operating conditions to insure stability.

## THERMAL PROTECTION

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at $150^{\circ} \mathrm{C}$, the output is disabled. There is no hysteresis built into the thermal protection. As a result the output will appear to be oscillating during thermal limit. The output will turn off until the temperature drops below the $150^{\circ} \mathrm{C}$ then the output turns on again. The process will repeat if the junction increases above the threshold. This will continue until the existing conditions allow the junction to operate below the temperature threshold.

Thermal limit is not a substitute for proper heatsinking.
The internal current limit will typically limit current to 450 mA . If during current limit the junction exceeds $150^{\circ} \mathrm{C}$, the thermal protection will protect the device also. Current limit is not a substitute for proper heatsinking. OUTPUT NOISE
In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor will reduce the noise on the MC33275.


Figure 16. SOT-223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 17. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 18. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC33275

## ORDERING INFORMATION

| Device | Type | Operating Temperature Range, Tolerance | Case | Package |
| :---: | :---: | :---: | :---: | :---: |
| MC33275DT-2.5RK | $\begin{gathered} 2.5 \mathrm{~V} \\ \text { (Fixed Voltage) } \end{gathered}$ | 1\% Tolerance <br> at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 369A | DPAK |
| MC33275ST-2.5T3 |  |  | 318 E | SOT-223 |
| MC33275D-2.5R2 |  |  | 751-5 | SOP-8 |
| MC33275DT-3.0RK | $\begin{gathered} 3.0 \mathrm{~V} \\ \text { (Fixed Voltage) } \end{gathered}$ |  | 369A | DPAK |
| MC33275ST-3.0T3 |  |  | 318E | SOT-223 |
| MC33275D-3.0R2 |  |  | 751-5 | SOP-8 |
| MC33275DT-3.3RK | $3.3 \mathrm{~V}$ <br> (Fixed Voltage) |  | 369A | DPAK |
| MC33275ST-3.3T3 |  | 2\% Tolerance at <br> $\mathrm{T}_{\mathrm{J}}$ from -40 to $+125^{\circ} \mathrm{C}$ | 318E | SOT-223 |
| MC33275D-3.3R2 |  |  | 751-5 | SOP-8 |
| MC33275DT-5.0RK | $\begin{gathered} 5.0 \mathrm{~V} \\ \text { (Fixed Voltage) } \end{gathered}$ |  | 369A | DPAK |
| MC33275ST-5.0T3 |  |  | 318E | SOT-223 |
| MC33275D-5.0R2 |  |  | 751-5 | SOP-8 |

DEVICE MARKING

| Device | Version | Marking (1st line) |
| :---: | :---: | :---: |
| MC33275 | 2.5 V | 27525 |
| MC33275 | 3.0 V | 27530 |
| MC33275 | 3.3 V | 27533 |
| MC33275 | 5.0 V | 27550 |

TAPE AND REEL SPECIFICATIONS

| Device | Reel Size | Tape Width | Quantity |
| :---: | :---: | :---: | :---: |
| MC33275DT | $13^{\prime \prime}$ | 16 mm embossed tape | 2500 units |
| MC33275D | $13^{\prime \prime}$ | 12 mm embossed tape | 2500 units |
| MC33275S | $13^{\prime \prime}$ | $8 m m$ embossed tape | 4000 units |

## MC33375

## Advance Information 300 mA, 2.5 V, Low Dropout Voltage Regulator with On/Off Control

The MC33375 series are micropower low dropout voltage regulators available in a wide variety of output voltages as well as packages, SOT-223, and SOP-8 surface mount packages. These devices feature a very low quiescent current and are capable of supplying output currents up to 300 mA . Internal current and thermal limiting protection are provided by the presence of a short circuit at the output and an internal thermal shutdown circuit.

The MC33375 has a control pin that allows a logic level signal to turn-off or turn-on the regulator output.

Due to the low input-to-output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

## Features:

- Low Quiescent Current ( $0.3 \mu \mathrm{~A}$ in OFF mode; $125 \mu \mathrm{~A}$ in ON mode)
- Low Input-to-Output Voltage Differential of 25 mV at $\mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$, and 260 mV at $\mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA}$
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of only $0.33 \mu \mathrm{~F}$ for 2.5 V Output Voltage
- Internal Current and Thermal Limiting
- Logic Level ON/OFF Control


This device contains 41 active transistors

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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## LOW DROPOUT MICROPOWER VOLTAGE REGULATOR




PLASTIC ST SUFFIX
CASE 318E


Pins 4 and 5 Not Connected
AL = Manufacturing Code
YW = Date
xx = Version


PLASTIC
D SUFFIX
CASE 751

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 529 of this data sheet.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{L}}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, for min/max values $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, Note 1)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA} \text { to } 250 \mathrm{~mA}$ <br> 1.8 V Suffix $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{~V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}$ <br> 2.5 V Suffix <br> 3.0 V Suffix <br> 3.3 V Suffix <br> 5.0 V Suffix <br> 1.8 V Suffix $\quad \mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}, 0<\mathrm{l}_{\mathrm{O}}<100 \mathrm{~mA}$ <br> 2.5 V Suffix $\quad 2 \%$ Tolerance from $\mathrm{T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ <br> 3.0 V Suffix <br> 3.3 V Suffix <br> 5.0 V Suffix | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 1.782 \\ & 2.475 \\ & 2.970 \\ & 3.267 \\ & 4.950 \\ & \\ & 1.764 \\ & 2.450 \\ & 2.940 \\ & 3.234 \\ & 4.900 \end{aligned}$ | $\begin{aligned} & 1.80 \\ & 2.50 \\ & 3.00 \\ & 3.30 \\ & 5.00 \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & 1.818 \\ & 2.525 \\ & 3.030 \\ & 3.333 \\ & 5.05 \\ & \\ & 1.836 \\ & 2.550 \\ & 3.060 \\ & 3.366 \\ & 5.100 \end{aligned}$ | Vdc |
| Line Regulation $\quad \mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}$ to $12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$, <br> All Suffixes $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | Regline | - | 2.0 | 10 | mV |
| Load Regulation $\quad \mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ to 250 mA , All Suffixes $T_{A}=25^{\circ} \mathrm{C}$ | Regload | - | 5.0 | 25 | mV |
| $\begin{array}{cl} \hline \text { Dropout Voltage } & \\ \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA} & \mathrm{~T}_{J}=-40^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\ \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA} & \\ \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA} & \\ \mathrm{I}_{\mathrm{O}}=300 \mathrm{~mA} & \end{array}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - | $\begin{gathered} 25 \\ 115 \\ 220 \\ 260 \end{gathered}$ | $\begin{aligned} & 100 \\ & 200 \\ & 400 \\ & 500 \end{aligned}$ | mV |
| Ripple Rejection (120 Hz) $\quad \mathrm{V}_{\text {in(peak-peak) }}=\left[\mathrm{V}_{\mathrm{O}}+1.5\right] \mathrm{V}$ to $\left[\mathrm{V}_{\mathrm{O}}+5.5\right] \mathrm{V}$ | - | 65 | 75 | - | dB |
| Output Noise Voltage $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=1 \mu \mathrm{~F} \quad \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}(10 \mathrm{~Hz} \text { to } 100 \mathrm{kHz}) \\ & \mathrm{C}_{\mathrm{L}}=200 \mu \mathrm{~F} \end{aligned}$ | $V_{n}$ | - | $\begin{gathered} 160 \\ 46 \end{gathered}$ | - | $\mu \mathrm{Vrms}$ |

CURRENT PARAMETERS

| Quiescent Current ON Mode | $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ | $\mathrm{I}_{\text {QOn }}$ | - | 125 | 200 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Quiescent Current OFF Mode |  | $\mathrm{I}_{\text {QOff }}$ | - | 0.3 | 4.0 | $\mu \mathrm{A}$ |
| Quiescent Current ON Mode SAT <br> 1.8 V Suffix <br> 2.5 V Suffix <br> 3.0 V Suffix <br> 3.3 V Suffix <br> 5.0 V Suffix | $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}-0.5\right] \mathrm{V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$, Note 2 | $\mathrm{I}_{\text {QSAT }}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & 1100 \\ & 1100 \\ & 1500 \\ & 1500 \\ & 1500 \end{aligned}$ | $\begin{aligned} & 1500 \\ & 1500 \\ & 2000 \\ & 2000 \\ & 2000 \end{aligned}$ | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {in }}=\left[\mathrm{V}_{\mathrm{O}}+1\right] \mathrm{V}, \mathrm{V}_{\mathrm{O}}$ Shorted | ILIMIT | - | 450 | - | mA |

## ON/OFF INPUTS

| ```On/Off Input Voltage Logic "1" (Regulator On) \(\mathrm{V}_{\text {out }}=\mathrm{V}_{\mathrm{O}} \pm 2 \%\) Logic "0" (Regulator Off) \(\mathrm{V}_{\text {out }}<0.03 \mathrm{~V}\) Logic "0" (Regulator Off) \(\mathrm{V}_{\text {out }}<0.05 \mathrm{~V}\) (1.8 V Option)``` | $\mathrm{V}_{\text {CTRL }}$ | 2.4 | - | 0.5 0.3 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |

## THERMAL SHUTDOWN

| Thermal Shutdown | - | - | 150 | - |
| :--- | :--- | :--- | :--- | :--- |
| ${ }^{\circ} \mathrm{C}$ |  |  |  |  |

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent Current is measured where the PNP pass transistor is in saturation. $\mathrm{V}_{\mathrm{in}}=\left[\mathrm{V}_{\mathrm{O}}-0.5\right] \mathrm{V}$ guarantees this condition.

## DEFINITIONS

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage - The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage - The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.

Maximum Power Dissipation - The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current - Current which is used to operate the regulator chip and is not delivered to the load.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Maximum Package Power Dissipation - The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. $150^{\circ} \mathrm{C}$. The junction temperature is rising while the
difference between the input power $\left(\mathrm{V}_{\mathrm{CC}} \mathrm{X} \mathrm{I}_{\mathrm{CC}}\right)$ and the output power $\left(V_{\text {out }} X \mathrm{I}_{\text {out }}\right)$ is increasing.

Depending on ambient temperature, it is possible to calculate the maximum power dissipation and so the maximum current as following:

$$
P d=\frac{T_{J}-T_{A}}{R_{\theta J A}}
$$

The maximum operating junction temperature $\mathrm{T}_{\mathrm{J}}$ is specified at $150^{\circ} \mathrm{C}$, if $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, then $\mathrm{P}_{\mathrm{D}}$ can be found. By neglecting the quiescent current, the maximum power dissipation can be expressed as:

$$
I_{\text {out }}=\frac{P_{D}}{V_{C C}-V_{o u t}}
$$

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature $\left(150^{\circ} \mathrm{C}\right.$ for MC 33375$)$ and ambient temperature.

$$
R_{\theta J A}=\frac{T_{J}-T_{A}}{P_{D}}
$$



Figure 2. Line Transient Response


Figure 3. Load Transient Response


Figure 5. Output Voltage versus Input Voltage


Figure 6. Dropout Voltage versus Output Current


Figure 7. Dropout Voltage versus Temperature


Figure 9. Ground Pin Current versus Ambient Temperature


Figure 8. Ground Pin Current versus Input Voltage


Figure 10. Output Voltage versus Ambient Temperature $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1 \mathrm{~V}\right)$

## MC33375



Figure 11. Output Voltage versus Ambient Temperature ( $\mathrm{V}_{\text {in }}=12 \mathrm{~V}$ )


Figure 12. Ripple Rejection


Figure 13. Ripple Rejection


Figure 14. Enable Transient
1.8 V Option


Figure 15. Output Voltage versus Temperature


Figure 17. Ground Current versus Load Current


Figure 19. PSRR versus Frequency


Figure 16. Output Voltage versus Input Voltage


Figure 18. Quiescent Current versus Input Voltage


Figure 20. Enable Response


Figure 21. Load Transient Response


Figure 22. Typical Application Circuit

The MC33375 regulators are designed with internal current limiting and thermal shutdown making them user-friendly. Figure 15 is a typical application circuit. The output capability of the regulator is in excess of 300 mA , with a typical dropout voltage of less than 260 mV . Internal protective features include current and thermal limiting.

## EXTERNAL CAPACITORS

These regulators require only a $0.33 \mu \mathrm{~F}$ (or greater) capacitance between the output and ground for stability for $1.8 \mathrm{~V}, 2.5 \mathrm{~V}, 3.0 \mathrm{~V}$, and 3.3 V output voltage options. Output voltage options of 5.0 V require only $0.22 \mu \mathrm{~F}$ for stability. The output capacitor must be mounted as close as possible to the MC33375. If the output capacitor must be mounted further than two centimeters away from the MC33375, then a larger value of output capacitor may be required for stability. A value of $0.68 \mu \mathrm{~F}$ or larger is recommended. Most type of aluminum, tantalum, or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below $25^{\circ} \mathrm{C}$. An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths, more than 4 inches. This will reduce the circuit's sensitivity to the input line impedance at high
frequencies. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. Figure 16 shows the ESR that allows the LDO to remain stable for various load currents.


Figure 23. $E S R$ for $V_{\text {out }}=3.0 \mathrm{~V}$
Applications should be tested over all operating conditions to insure stability.

## THERMAL PROTECTION

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at $150^{\circ} \mathrm{C}$, the output is disabled. There is no hysteresis built into the thermal protection. As a result the output will appear to be oscillating during thermal limit. The output will turn off until the temperature drops below the $150^{\circ} \mathrm{C}$ then the output turns on again. The process will repeat if the junction increases above the threshold. This will continue until the existing conditions allow the junction to operate below the temperature threshold.

Thermal limit is not a substitute for proper heatsinking.

The internal current limit will typically limit current to 450 mA . If during current limit the junction exceeds $150^{\circ} \mathrm{C}$, the thermal protection will protect the device also. Current limit is not a substitute for proper heatsinking.

## OUTPUT NOISE

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor will reduce the noise on the MC33375.

## ON/OFF PIN

When this pin is pulled low, the MC33375 is off. This pin should not be left floating. The pin should be pulled high for the MC33375 to operate.


Figure 24. SOT-223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 25. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC33375

ORDERING INFORMATION

| MC33375ST-1.8T3 | 1.8 V (Fixed V) | 1\% Tolerance <br> at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> 2\% Tolerance at $\mathrm{T}_{\mathrm{J}}$ from -40 to $+125^{\circ} \mathrm{C}$ | 318E | SOT-223 |
| :---: | :---: | :---: | :---: | :---: |
| MC33375ST-2.5T3 | $\begin{gathered} 2.5 \mathrm{~V} \\ \text { (Fixed Voltage) } \end{gathered}$ |  | 318E | SOT-223 |
| MC33375D-2.5R2 |  |  | 751-5 | SOP-8 |
| MC33375ST-3.0T3 | $\begin{gathered} 3.0 \mathrm{~V} \\ \text { (Fixed Voltage) } \end{gathered}$ |  | 318E | SOT-223 |
| MC33375D-3.0R2 |  |  | 751-5 | SOP-8 |
| MC33375ST-3.3T3 | 3.3 V <br> (Fixed Voltage) |  | 318E | SOT-223 |
| MC33375D-3.3R2 |  |  | 751-5 | SOP-8 |
| MC33375ST-5.0T3 | 5.0 V <br> (Fixed Voltage) |  | 318E | SOT-223 |
| MC33375D-5.0R2 |  |  | 751-5 | SOP-8 |

## DEVICE MARKING

| Device | Version | Marking (1st line) |
| :---: | :---: | :---: |
| MC33375 | 1.8 V | 37518 |
| MC33375 | 2.5 V | 37525 |
| MC33375 | 3.0 V | 37530 |
| MC33375 | 3.3 V | 37533 |
| MC33375 | 5.0 V | 37550 |

TAPE AND REEL SPECIFICATIONS

| Device | Reel Size | Tape Width | Quantity |
| :---: | :---: | :---: | :---: |
| MC33375D | $13^{\prime \prime}$ | 12 mm embossed tape | 2500 units |
| MC33375ST | $13^{\prime \prime}$ | 8 mm embossed tape | 4000 units |

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, for min/max values $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $\left.+125^{\circ} \mathrm{C}\right)$

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 13 | Vdc |
| Power Dissipation and Thermal Characteristics $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Maximum Power Dissipation <br> Case 751 (SOP-8) D Suffix <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 318E (SOT-223) ST Suffix <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJc }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | Internally Limited $\begin{aligned} & 160 \\ & 25 \end{aligned}$ $245$ $15$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Output Current | 10 | 300 | mA |
| Maximum Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## CS8120

### 5.0 V, 300 mA Linear Regulator with RESET and ENABLE

The CS8120 is a $5.0 \mathrm{~V}, 300 \mathrm{~mA}$ precision linear regulator with two microprocessor compatible control functions and protection circuitry included on chip. The composite NPN-PNP output pass transistor assures a lower dropout voltage ( 1.0 V @ 200 mA ) without requiring excessive supply current ( 2.5 mA ).

The CS8120's two logic control functions make this regulator well suited to applications requiring microprocessor-based control at the board or module level. ENABLE controls the output stage. A high voltage ( $>2.9 \mathrm{~V}$ ) on the $\overline{\text { ENABLE }}$ lead turns off the regulator's pass transistor and sends the IC into Sleep mode where it draws only $250 \mu \mathrm{~A}$. The $\overline{\text { RESET }}$ function sends a $\overline{\text { RESET }}$ signal when the IC is powering up or whenever the output voltage moves out of regulation. The $\overline{\text { RESET }}$ signal is valid down to $\mathrm{V}_{\text {OUT }}=1.0 \mathrm{~V}$.

The CS8120 design optimizes supply rejection by switching the internal bandgap reference from the supply input to the regulator output as soon as the nominal output voltage is achieved. Additional on chip filtering enhances rejection of high frequency transients on all external leads.

The CS8120 is fault protected against short circuit, over voltage and thermal runaway conditions.

## Features

- $5.0 \mathrm{~V} \pm 4.0 \%$ Output Voltage 300 mA
- Low Dropout Voltage (1.0 V @ 150 mA )
- Low Quiescent Current ( 2.5 mA @ $\mathrm{I}_{\mathrm{OUT}}=150 \mathrm{~mA}$ )
- $\mu \mathrm{P}$ Compatible Control Functions
- $\overline{\text { RESET }}$
- $\overline{\text { ENABLE }}$
- Low Current Sleep Mode
$-\mathrm{I}_{\mathrm{Q}}=250 \mu \mathrm{~A}$
- Fault Protection
- Thermal Shutdown
- Short Circuit
- 60 V Load Dump


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http://onsemi.com


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 539 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 539 of this data sheet.

PIN CONNECTIONS


Figure 1. Block Diagram - TO-220

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| DC Input Voltage |  | -0.7 to 26 | V |
| Load Dump |  | 60 | V |
| Output Current |  | Internally Limited | - |
| Electrostatic Discharge (Human Body Model) |  | 2.0 | kV |
| Operating Temperature |  | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2) | 260 peak 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}\right.$, $\mathrm{I}_{\mathrm{OUT}}=5.0 \mathrm{~mA} ;-40 \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq 125^{\circ} \mathrm{C}$, unless otherwise noted.) Note 3

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Output Voltage, V ${ }_{\text {OUT }}$ | $7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 300 \mathrm{~mA}$ | 4.8 | 5.0 | 5.2 | V |
| Line Regulation | $7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, $\mathrm{l}_{\text {OUT }}=200 \mathrm{~mA}$ | - | - | 50 | mV |
| Load Regulation | $1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 300 \mathrm{~mA}$ | - | - | 50 | mV |
| Supply Voltage Rejection | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}_{\mathrm{DC}}+1.0 \mathrm{~V}_{\mathrm{RMS}} @ 120 \mathrm{~Hz} \\ & \text { LOAD }=25 \Omega \end{aligned}$ | 40 | 70 | - | dB |
| Dropout Voltage | IOUT $=200 \mathrm{~mA}$ | - | 1.0 | 1.5 | V |
| Quiescent Current | $\begin{aligned} & \text { ENABLE }=\text { High, } \mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V} \\ & \text { ENABLE }=\text { Low }, \mathrm{I}_{\mathrm{OUT}}=200 \mathrm{~mA} \end{aligned}$ |  | $\begin{gathered} 0.25 \\ 2.5 \end{gathered}$ | $\begin{gathered} 0.65 \\ 15 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

## Protection Circuits

| Short Circuit Current | - | 300 | 600 | - | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Thermal Shutdown | - | 150 | 190 | - | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | - | 26 | 40 | - | V |

RESET

| RESET Saturation Voltage | $1.0 \mathrm{~V}<\mathrm{V}_{\text {OUT }}<\mathrm{V}_{\text {RT(OFF) }}$, $3.1 \mathrm{k} \Omega$ Pull-Up to $\mathrm{V}_{\text {OUT }}$ | - | 0.1 | 0.4 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESET Output Leakage Current | $\begin{aligned} \text { ENABLE } & =\text { Low, } \mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RT(ON })}, \\ V_{\text {RESET }} & =V_{\text {OUT }} \end{aligned}$ | - | 0 | 25 | $\mu \mathrm{A}$ |
| Power ON/OFF RESET Peak Output Voltage | $3.1 \mathrm{k} \Omega$ Pull-Up to $\mathrm{V}_{\text {OUT }}$ | - | 0.7 | 1.0 | V |
| $\begin{aligned} & \text { RESET Threshold } \\ & \text { HIGH }\left(\mathrm{V}_{\mathrm{RH}}\right) \\ & \text { LOW }\left(\mathrm{V}_{\mathrm{RL}}\right) \end{aligned}$ | $V_{\text {OUT }}$ Increasing <br> $V_{\text {OUT }}$ Decreasing | $4.75$ | $\begin{aligned} & \mathrm{V}_{\text {OUT }}-0.10 \\ & \mathrm{~V}_{\text {OUT }}-0.14 \end{aligned}$ | $\mathrm{V}_{\text {OUT }}^{-}-0.04$ | V |
| RESET Threshold Hysteresis | - | 10 | 40 | - | mV |

ENABLE

| Input High Voltage | $7.0 \mathrm{~V}<\mathrm{V}_{\mathbb{I N}}<26 \mathrm{~V}$ | - | 2.9 | 3.9 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Low Voltage | $7.0 \mathrm{~V}<\mathrm{V}_{\mathbb{I N}}<26 \mathrm{~V}$ | 1.1 | 2.1 | - | V |
| Input Hysteresis | $7.0 \mathrm{~V}<\mathrm{V}_{\mathbb{I N}}<26 \mathrm{~V}$ | 0.4 | 0.8 | 2.8 | V |
| Input Current | $\mathrm{GND}<\mathrm{V}_{\mathbb{I N ( H I )})}<\mathrm{V}_{\mathrm{OUT}}$ | -10 | 0 | +10 | $\mu \mathrm{~A}$ |

3. To have safe operating junction temperatures, low duty cycle pulse testing is used on tests where applicable.

## PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  |  | LEAD SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { TO-220 } \\ & 5 \text { LEAD- } \end{aligned}$ | DIP-8 | SO-14 | D2Pak <br> 5 PIN |  |  |
| 1 | 2 | 1 | 1 | $\mathrm{V}_{\text {IN }}$ | Supply voltage to IC, usually direct from the battery. |
| 2 | 4 | 5 | 2 | ENABLE | CMOS compatible logical input. $\mathrm{V}_{\text {OUT }}$ is disabled i.e. placed in a high impedance state when ENABLE is high. |
| 3 | 8 | 13 | 3 | GND | Ground Connection. |
| 4 | 6 | 10 | 4 | RESET | CMOS compatible output lead. RESET goes low whenever $\mathrm{V}_{\text {OUt }}$ falls out of regulation. The RESET delay is externally programmed. |
| 5 | 1 | 14 | 5 | $V_{\text {OUT }}$ | Regulated output voltage, 5.0 V (typ). |
| N/A | 7 | 12 | - | SENSE | Kelvin Connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not desired, connect to $\mathrm{V}_{\text {OUT. }}$ |
| - | 3, 5 | $\begin{aligned} & 2,3,4,6 \\ & 7,8,9,11 \end{aligned}$ |  | NC | No Connection. |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 2. Output Voltage vs. Temperature


Figure 3. Load Regulation vs. Output Current Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 4. Line Regulation vs. Output Current Over Temperature


Figure 6. Quiescent Current vs. Output Current Over Temperature


Figure 5. Dropout Voltage vs. Output Current Over Temperature


Figure 7. Output Voltage and Supply Current vs. Input Voltage


Figure 8. RESET Output Voltage vs.
Output Voltage

## CIRCUIT DESCRIPTION

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

## Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within $\pm 4.0 \%$ over temperature and supply variation.

## Output Stage

The composite PNP-NPN output structure (Figure 9) provides 300 mA (typ) of output current while maintaining a low drop out voltage ( 1.00 V , typ) and drawing little quiescent current ( 2.5 mA ). The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.


Figure 9. Composite Output Stage of the CS8120

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 10).


Figure 10. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 26 V (e.g. load dump), the output shuts down. This response protects the internal
circuitry and enables the IC to survive unexpected voltage transients.
Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.
Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

## REGULATOR CONTROL FUNCTIONS

The CS8120 contains two microprocessor compatible control functions: $\overline{\text { ENABLE }}$ and $\overline{\text { RESET }}$ (Figure 11).

## ENABLE Function

The ENABLE function switches the output transistor. When the voltage on the ENABLE lead exceeds 2.9 V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only $250 \mu \mathrm{~A}$, until the voltage on the lead drops below 2.1 V typ. Hysteresis ( 800 mV ) is built into the ENABLE function to provide good noise immunity.

(1) $=$ No Reset Delay Capacitor
(2) = With Reset Delay Capacitor

Figure 11. Circuit Waveform for CS8120

## RESET Function

A $\overline{\mathrm{RESET}}$ signal (low voltage) is generated as the IC powers up ( $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {OUT }}-100 \mathrm{mV}$ ) or when $\mathrm{V}_{\text {OUT }}$ drops out of regulation ( $\mathrm{V}_{\text {OUT }}<\mathrm{V}_{\text {OUT }}-140 \mathrm{mV}$, typ). 40 mV of hysteresis is included in the function to minimize oscillations.
The RESET output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is
functionally independent of the rest of the IC, thereby guaranteeing that the $\overline{\text { RESET }}$ signal is valid for $\mathrm{V}_{\text {OUT }}$ as low as 1.0 V .


Figure 12. RC Network for RESET Delay Circuitry

An external RC network on the $\overline{\text { RESET }}$ lead (Figure 12) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:
where:
$\mathrm{R}_{\mathrm{TOT}}=\mathrm{R}_{\mathrm{RST}}$ in parallel with $\mathrm{R}_{\mathrm{IN}}$,
$\mathrm{R}_{\mathrm{IN}}=\mu \mathrm{P}$ port impedance,
$\mathrm{C}_{\text {RST }}=\overline{\mathrm{RESET}}$ delay capacitor,
$\mathrm{t}_{\text {Delay }}=$ desired delay time,
$\mathrm{V}_{\mathrm{RST}}=\mathrm{V}_{\text {SAT }}$ of $\overline{\text { RESET }}$ lead ( 0.7 V @ turn -ON ), and
$\mathrm{V}_{\mathrm{T}}=\mu \mathrm{P}$ logic threshold voltage.

## APPLICATION NOTES

The circuit depicted in Figure 13 lets the microprocessor control its power source, the CS8120 regulator. An I/O port on the $\mu \mathrm{P}$ and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the ENABLE lead falls below its lower threshold. The regulator's output is switched out. When the drive current is removed, the voltage on the $\overline{\text { ENABLE }}$ lead rises, the output is switched off and the IC moves into Sleep mode where it draws $250 \mu \mathrm{~A}$.

By coupling these two controls with the ENABLE, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The microprocessor can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port
allows the microprocessor to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1.
Table 1. Logic Control of CS8120 Output

| Microprocessor <br> I/O Drive | SWITCH | ENABLE | Output |
| :---: | :---: | :---: | :---: |
| ON | Closed | LOW | ON |
|  | Open | LOW | ON |
| OFF | Closed | LOW | ON |
|  | Open | HIGH | OFF |

The I/O port of the microprocessor typically provides $50 \mu \mathrm{~A}$ to Q 1 . In automotive applications the SWITCH is connected to the ignition switch.


Figure 13. Microprocessor Control of CS8120 Using External Switching Transistor Q1

## STABILITY CONSIDERATIONS

The output or compensation capacitor, $\mathrm{C}_{2}$, helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor $\mathrm{C}_{2}$ shown in Figure 14 should work for most applications, however it is not necessarily the optimized solution.

${ }^{*} \mathrm{C}_{1}$ is required if regulator is far from the power source filter.
${ }^{* *} \mathrm{C}_{2}$ is required for stability.
Figure 14. Circuit Showing Output Compensation Capacitor

To determine an acceptable value for $\mathrm{C}_{2}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause
the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 15) is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $R_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 15. Single Output Regulator With Key Performance Parameters Labeled

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \mathrm{JA}}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

ORDERING INFORMATION

| Device | Description | Shipping |
| :---: | :---: | :---: |
| CS8120YT5 | TO-220 FIVE LEAD STRAIGHT | 50 Units/Rail |
| CS8120YTVA5 | TO-220 FIVE LEAD VERTICAL | 50 Units/Rail |
| CS8120YTHA5 | TO-220 FIVE LEAD HORIZONTAL | 50 Units/Rail |
| CS8120YN8 | DIP-8 | 50 Units/Rail |
| CS8120YDP5 | D2PAK, 5-Pin | 50 Units/Rail |
| CS8120YDPR5 | D2PAK, 5-Pin | 750 Tape \& Reel |
| CS8120YD14 | SO-14 | 55 Units/Rail |
| CS8120YDR14 | SO-14 | 2500 Tape \& Reel |

## MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> FIVE LEAD | D $^{2}$ PAK <br> FIVE LEAD | DIP-8 | SO-14 | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\Theta \mathrm{JCC}}$ | Typical | 3.1 | 3.1 | 52 | 30 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta \mathrm{JA}}$ | Typical | 50 | $10-50^{*}$ | 100 | 125 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta \mathrm{JA}}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta C A}$


## CS5231-3

## 500 mA , 3.3 V Linear Regulator with Auxiliary Control

The CS5231-3 combines a three-terminal linear regulator with circuitry controlling an external PFET transistor thus managing two input supplies. The part provides a 3.3 V regulated output either from the main 5.0 V supply or a 3.3 V auxiliary that switches on when the 5.0 V supply is not present. This delivers constant, uninterrupted power to the load. The CS5231-3 meets Intel's "Instantly Available" power requirements which follows from the "Advanced Configuration and Power Interface" (ACPI) standards developed by Intel, Microsoft and Toshiba.

The CS5231-3 linear regulator provides a fixed 3.3 V output at 500 mA with an overall accuracy of $\pm 2.0 \%$. The internal NPN-PNP composite pass transistor provides a low dropout voltage and requires less supply current than a straight PNP design. Full protection with both current limit and thermal shutdown is provided.

Designed for low reverse current, the IC prevents excessive current from flowing from $V_{\text {OUT }}$ to either $\mathrm{V}_{\text {IN }}$ or ground when the regulator input voltage is lower than the output voltage.

The CS5231-3 can be used to provide power to an ASIC on a PCI Network Interface Card (NIC). When the system enters a Sleep State and the 5.0 V input drops below 4.4 V , the AuxDrv control signal on the CS5231-3 is activated turning on the external PFET. This switches the supply source from the 5.0 V input to the 3.3 V input through the PFET, guaranteeing a constant 3.3 V output to the ASIC that is "glitch free."

The CS5231-3 is available in two package types: the 5-Lead $\mathrm{D}^{2}$ PAK (TO263) package and the 8-Lead SOIC 4-Lead-fused (DF) package. Other applications include desktop computers, power supplies with multiple input sources and PCMCIA/PCI interface cards.

## Features

- Linear Regulator
$-3.3 \mathrm{~V} \pm 2.0 \%$ Output Voltage
- 3.0 mA Quiescent Current @ 500 mA
- Fast Transient Response
- Current Limit Protection
- Thermal Shutdown with Hysteresis
- $450 \mu \mathrm{~A}$ Reverse Output Current
- System Power Management
- Auxiliary Supply Control
- "Glitch Free" Transition Between Two Supplies
- Internally Fused Leads in SO-8 Package



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PIN CONNECTIONS AND MARKING DIAGRAMS

D2PAK 5-PIN


Pin 1. No Connect
2. $\mathrm{V}_{\mathrm{IN}}$
3. GND
4. VOUT
5. AuxDrv

Tab = GND


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5231-3GDP5 | D $^{2}$ PAK $^{*}$ | 50 Units/Rail |
| CS5231-3GDPR5 | D$^{2}$ PAK $^{*}$ | 750 Tape \& Reel |
| CS5231-3GDF8 | SO-8 | 95 Units/Rail |
| CS5231-3GDFR8 | SO-8 | 2500 Tape \& Reel |

* 5-PIN


Figure 1. Block Diagram

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Maximum Operating Junction Temperature | Unit |  |
| Storage Temperature Range | Reflow: (SMD styles only) (Note 1$)$ | 230 |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |
| ESD Damage Threshold (Human Body Model) | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\text {IN }}$ | 14 V | -0.3 V | 100 mA | Internally Limited |
| Output Voltage | $\mathrm{V}_{\text {OUT }}$ | 6.0 V | -0.3 V | Internally Limited | 100 mA |
| Auxiliary Drive Output | AuxDrv | 14 V | -0.3 V | 10 mA | 50 mA |
| IC Ground | GND | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.75 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<6.0 \mathrm{~V} ; \mathrm{C}_{\text {OUT }} \geq 10 \mu \mathrm{~F}\right.$ with ESR $<1.0 \Omega$, lout = 10 mA ; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Linear Regulator |  |  |  |  |  |
| Output Voltage | 10 mA < I OUT $^{\text {< }} 500 \mathrm{~mA}$. | $\begin{aligned} & 3.234 \\ & (-2 \%) \end{aligned}$ | 3.3 | $\begin{aligned} & 3.366 \\ & (+2 \%) \end{aligned}$ | V |
| Line Regulation | $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} ; \mathrm{V}_{\text {IN }}=4.75 \mathrm{~V}$ to 6.0 V | - | 1.0 | 5.0 | mV |
| Load Regulation | $\mathrm{V}_{\text {IN }}=5.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ to 500 mA | - | 5.0 | 15 | mV |
| Ground Current | $\begin{aligned} & \text { IOUT }=10 \mathrm{~mA} \\ & \mathrm{I}_{\text {OUT }}=500 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Reverse Current | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ | - | 0.45 | 1.0 | mA |
| Current Limit | $0 \mathrm{~V}<\mathrm{V}_{\text {OUT }}<3.2 \mathrm{~V}$ | 0.55 | 0.85 | 1.2 | A |
| Thermal Shutdown | Note 2 | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | Note 2 | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

Auxiliary Drive

| Upper $\mathrm{V}_{\text {IN }}$ Threshold | Increase $\mathrm{V}_{\mathrm{IN}}$ until regulator turns on and AuxDrv drives high | 4.35 | 4.5 | 4.65 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Lower $\mathrm{V}_{\text {IN }}$ Threshold | Decrease $\mathrm{V}_{\mathrm{IN}}$ until regulator turns off and AuxDrv drives low | 4.25 | 4.4 | 4.55 | V |
| $\mathrm{V}_{\text {IN }}$ Threshold Hysteresis | - | 75 | 100 | 125 | mV |
| Output Low Voltage | $\mathrm{I}_{\text {AuxDrv }}=100 \mu \mathrm{~A}, 1.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<4.5 \mathrm{~V}$ | - | 0.1 | 0.4 | V |
| Output Low Peak Voltage | Increase $\mathrm{V}_{\mathrm{IN}}$ from 0 V to 1.0 V . Record peak AuxDrv output voltage | - | 0.65 | 0.9 | V |
| AuxDrv Current Limit | $\mathrm{V}_{\text {AuxDrv }}=1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{IN}}=4.0 \mathrm{~V}$ | 0.5 | 6.0 | 25 | mA |
| Response Time | Step $\mathrm{V}_{\text {IN }}$ from 5.0 V to 4.0 V , measure time for $V_{\text {AuxDrv }}$ to drive low. Note | - | 1.0 | 10 | $\mu \mathrm{S}$ |
| Pull-Up/Down Resistance | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}$ and $\mathrm{V}_{\text {IN }}>4.7 \mathrm{~V}$. | 5.0 | 10 | 25 | k $\Omega$ |

2. Guaranteed by design, not $100 \%$ production tested. Thermal shutdown is $100 \%$ functionally tested at wafer probe.

PACKAGE PIN DESCRIPTION

| Package Lead \# |  |  |  |
| :---: | :---: | :---: | :--- |
| D$^{2}$ PAK 5-Pin | SO-8 | Lead Symbol |  |
| 1 | 1 | NC | No connection. |
| 2 | 4 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |
| $3, \mathrm{Tab}$ | $2,3,6,7$ | GND | Ground and IC substrate connection. |
| 4 | 5 | $\mathrm{~V}_{\text {OUT }}$ | Regulated output voltage. |
| 5 | 8 | AuxDrv | Output used to control an auxiliary supply voltage. This lead is driven <br> low if $V_{\text {IN }}$ is less than 4.5 V , and is otherwise pulled up to $\mathrm{V}_{\text {IN }}$ through <br> an internal $10 \mathrm{k} \Omega$ resistor. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Output Voltage vs. Junction Temperature


Figure 4. Load Regulation vs. Iout Over Temperature


Figure 6. V $_{\text {Out }}$ vs. Iout Over Junction Temperature


Figure 3. Line Regulation vs. IOUT Over Temperature


Figure 5. Reverse Current vs. Junction Temperature


Figure 7. $\mathrm{V}_{\text {IN }}$ Thresholds vs. Junction Temperature


Figure 8. Ground Current vs. Load Current


Figure 10. AuxDrv Current Limit vs. Junction Temperature


Figure 9. Region of Stable Operation


Figure 11. Transient Response


Figure 12. Application Circuit

## APPLICATION INFORMATION

## THEORY OF OPERATION

The CS5231-3 is a fixed 3.3 V linear regulator that contains an auxiliary drive control feature. When $\mathrm{V}_{\text {IN }}$ is greater than the typical 4.5 V threshold, the IC functions as a linear regulator. It provides up to 500 mA of current to a load through a composite PNP-NPN pass transistor. An output capacitor greater than $10 \mu \mathrm{~F}$ with equivalent series resistance less than $1.0 \Omega$ is required for compensation. More information is provided in the Stability Considerations section.

The CS5231-3 provides an auxiliary drive feature that allows a load to remain powered even if the $\mathrm{V}_{\text {IN }}$ supply for the IC is absent. An external p-channel FET is the only additional component required to implement this function if an auxiliary power supply is available. The PFET gate is connected to the AuxDrv lead. The PFET drain is connected to the auxiliary power supply, and the PFET source is connected to the load. The polarity of this connection is very important, since the PFET body diode will be connected between the load and the auxiliary supply. If the PFET is connected with its drain to the load and its source to the supply, the body diode will be forward-biased if the auxiliary supply is turned off. This will result in the linear regulator providing current to everything on the auxiliary supply rail.
The AuxDrv lead is internally connected to a $10 \mathrm{k} \Omega$ resistor and to a saturating NPN transistor that acts as a switch. If the $\mathrm{V}_{\text {IN }}$ supply is off, the AuxDrv output will connect the PFET gate to ground through the $10 \mathrm{k} \Omega$ resistor, and the PFET will conduct current to the load.

As the $\mathrm{V}_{\text {IN }}$ supply begins to rise, the AuxDrv lead will also rise until it reaches a typical voltage of about 650 mV . The NPN transistor connected to the AuxDrv lead will saturate at this point, and the gate of the PFET will be pulled down to a typical voltage of about 100 mV . The PFET will continue to conduct current to the load.

The $\mathrm{V}_{\text {IN }}$ supply voltage will continue to rise, but the linear regulator output is disabled until $\mathrm{V}_{\text {IN }}$ reaches a typical threshold of 4.5 V . During this time, the load continues to be powered by the auxiliary driver. Once the $4.5 \mathrm{~V} \mathrm{~V}_{\text {IN }}$ threshold is reached, the saturating NPN connected to the AuxDrv lead turns off. The on-chip $10 \mathrm{k} \Omega$ pull-up resistor will pull the PFET gate up to $\mathrm{V}_{\mathrm{IN}}$, thus turning the PFET off. The linear regulator turns on at the same time. An external compensation capacitor is required for the linear regulator to be stable, and this capacitance also serves as a charge reservoir to minimize any "glitching" that might result during the supply changeover. Hysteresis is present in the AuxDrv circuitry, requiring $\mathrm{V}_{\text {IN }}$ to drop by 100 mV (typical) after the linear regulator is providing power to the load before the AuxDrv circuitry can be re-enabled.


Figure 13. Initial Power-Up, $\mathrm{V}_{\text {AUX }}$ Not Present $R_{\text {OUT }}=8.8 \Omega$


Figure 14. Power-Up, $V_{A U X}=3.3$ V. Note the "Oscillatory Performance" as the Linear Regulator Changes the $\mathrm{V}_{\text {OUT }}$ Node. $\mathrm{I}_{\text {OUT }} \times \mathrm{R}_{\mathrm{DS}(\mathrm{ON})} \approx \mathbf{1 3 0} \mathbf{~ m V}$


Figure 15. Power-Down, $\mathrm{V}_{\mathrm{AUX}}=3.3 \mathrm{~V}$. Again, Note $\Delta V=I R_{D S(O N)} \approx 130 \mathrm{mV}$


Figure 16. Power-Up, $\mathrm{V}_{\mathrm{A} U \mathrm{X}}=3.135 \mathrm{~V}$. The "Oscillatory Performance" Mode Lasts Longer Because the Difference Between $\mathrm{V}_{\mathrm{AUX}}$ and 3.3 is Greater

$\mathrm{I}_{\mathrm{OUT}}=375 \mathrm{~mA} \quad \mathrm{~V}_{\text {AUX }}=3.135$
Figure 17. Power-Down, $\mathrm{V}_{\mathrm{AUX}}=3.135 \mathrm{~V}$. The Difference in Voltage is Now IOUT $\times \mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ Plus the Difference in Supply Voltages (3.3-V $\mathrm{V}_{\text {AUX }}$ )


Figure 18. Power-Up, $\mathrm{V}_{\mathrm{AUX}}=3.465 \mathrm{~V}$. I IOUT $\times \mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ is Compensated By Higher Value of $\mathrm{V}_{\mathrm{AUX}}$


Figure 19. Power-Down, $\mathrm{V}_{\mathrm{AUX}}=3.465 \mathrm{~V}$

## STABILITY CONSIDERATIONS

The output capacitor helps determine three main characteristics of a linear regulator: startup, transient response and stability.
Startup is affected because the output capacitor must be charged. At initial startup, the $\mathrm{V}_{\text {IN }}$ supply may not be present, and the output capacitor will be charged through the PFET. The PFET will initially provide current to the load through its body diode. The diode will act as a voltage follower until sufficient voltage is present to turn the FET on. Since most commercial power supplies have a fairly low ramp rate, charging through the body diode should effectively limit in-rush current to the capacitor.

During normal operation, transient load current requirements will be satisfied from the charge stored in the output capacitor until either the linear regulator or the auxiliary supply can respond. Larger values of capacitance will improve transient response, but will also cost more. A linear regulator will respond within microseconds, where an external power supply may take milliseconds to react. The output capacitance will provide the difference in current until this occurs. The result will be an instantaneous voltage change at the output. This change is the product of the current change and the capacitor ESR:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I} \mathrm{LOAD} \times \mathrm{ESR}
$$

This limitation directly affects load regulation. Capacitor ESR must be minimized if output voltage must be maintained within tight tolerances. In such a case, it is often advisable to use a parallel network of different types of capacitors. For example, electrolytic capacitors provide high charge storage capacity in a small size, while tantalum capacitors have low ESR. The parallel combination will result in a high capacity, low ESR network. It is also important to physically locate the capacitance network close to the load, and to connect the network to the load with wide PC board traces to minimize the metal resistance.

The CS5231-3 has been carefully designed to be stable for output capacitances greater than $10 \mu \mathrm{~F}$ with equivalent series resistance less than $1.0 \Omega$. While careful board layout is important, the user should have a stable system if these constraints are met. A graph showing the region of stability for the CS5231-3 is included in the "Typical Performance Characteristics" section of this datasheet.

## INPUT CAPACITORS AND THE $V_{\text {IN }}$ THRESHOLDS

A capacitor placed on the $\mathrm{V}_{\text {IN }}$ pin will help to improve transient response. During a load transient, the input capacitor serves as a charge "reservoir," providing the needed extra current until the external power supply can respond. One of the consequences of providing this current is an instantaneous voltage drop at $\mathrm{V}_{\text {IN }}$ due to capacitor ESR. The magnitude of the voltage change is again the product of the current change and the capacitor ESR.

It is very important to consider the maximum current step that can exist in the system. If the change in current is large enough, it is possible that the instantaneous voltage drop on $\mathrm{V}_{\text {IN }}$ will exceed the $\mathrm{V}_{\text {IN }}$ threshold hysteresis, and the IC will enter a mode of operation resembling an oscillation. As the part turns on, the output current $\mathrm{I}_{\text {OUT }}$ will increase, reaching current limit during initial charging. Increasing IOUT results in a drop at $\mathrm{V}_{\text {IN }}$ such that the shutdown threshold is reached. The part will turn off, and the load current will decrease. As IOUT decreases, $\mathrm{V}_{\text {IN }}$ will rise and the part will turn on, starting the cycle all over again. This oscillatory operation is most likely at initial start-up when the output capacitance is not charged, and in cases where the ramp-up of the $\mathrm{V}_{\mathrm{IN}}$ supply is slow. It may also occur during the power transition when the regulator turns on and the PFET turns off. A $15 \mu \mathrm{~s}$ delay exists between turn-on of the regulator and the AuxDrv pin pulling the gate of the PFET high. This delay prevents "chatter" during the power transitions. During this interval, the linear regulator will attempt to regulate the output voltage as 3.3 V . If the output voltage is significantly below 3.3 V , the IC will go into current limit while trying to raise $\mathrm{V}_{\text {OUT }}$. It is a short-lived phenomenon and is mentioned here to alert the user that the condition can exist. It is typically not a problem in applications. Careful choice of the PFET switch with respect to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ will minimize the voltage drop which the output must charge through to return to a regulated state. More information is provided in the section on choosing the PFET switch.

If required, using a few capacitors in parallel to increase the bulk charge storage and reduce the ESR should give better performance than using a single input capacitor. Short, straight connections between the power supply and $\mathrm{V}_{\text {IN }}$ lead along with careful layout of the PC board ground plane will reduce parasitic inductance effects. Wide $\mathrm{V}_{\text {IN }}$ and $V_{\text {OUT }}$ traces will reduce resistive voltage drops.

## CHOOSING THE PFET SWITCH

The choice of the external PFET switch is based on two main considerations. First, the PFET should have a very low
turn-on threshold. Choosing a switch transistor with $\mathrm{V}_{\mathrm{GS}(\mathrm{ON})} \approx 1.0 \mathrm{~V}$ will ensure the PFET will be fully enhanced with only 3.3 V of gate drive voltage. Second, the switch transistor should be chosen to have a low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ to minimize the voltage drop due to current flow in the switch. The formula for calculating the maximum allowable on-resistance is

$$
\operatorname{RDS}(\mathrm{ON}) \mathrm{MAX}=\frac{\mathrm{V}_{\mathrm{AUX}}(\mathrm{MIN})-\mathrm{V}_{\mathrm{OUT}}(\mathrm{MIN})}{1.5 \times \operatorname{lOUT}(\mathrm{MAX})}
$$

where $\mathrm{V}_{\mathrm{AUX}(\mathrm{MIN})}$ is the minimum value of the auxiliary supply voltage, $\mathrm{V}_{\text {OUT(MIN) }}$ is the minimum allowable output voltage, IOUT(MAX) is the maximum output current and 1.5 is a "fudge factor" to account for increases in $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ due to temperature.

## OUTPUT VOLTAGE SENSING

It is not possible to remotely sense the output voltage of the CS5231-3 since the feedback path to the error amplifier is not externally available. It is important to minimize voltage drops due to metal resistance of high current PC board traces. Such voltage drops can occur in both the supply traces and the return traces.
The following board layout practices will help to minimize output voltage errors:

- Always place the linear regulator as close to both load and output capacitors as possible.
- Always use the widest possible traces to connect the linear regulator to the capacitor network and to the load.
- Connect the load to ground through the widest possible traces.
- Connect the IC ground to the load ground trace at the point where it connects to the load.


## CURRENT LIMIT

The CS5231-3 has internal current limit protection. Output current is limited to a typical value of 850 mA , even under output short circuit conditions. If the load current drain exceeds the current limit value, the output voltage will be pulled down and will result in an out of regulation condition. The IC does not contain circuitry to report this fault.

## THERMAL SHUTDOWN

The CS5231-3 has internal temperature monitoring circuitry. The output is disabled if junction temperature of the IC reaches $180^{\circ} \mathrm{C}$. Thermal hysteresis is typically $25^{\circ} \mathrm{C}$ and allows the IC to recover from a thermal fault without the need for an external reset signal. The monitoring circuitry is located near the composite PNP-NPN output transistor, since this transistor is responsible for most of the on-chip power dissipation. The combination of current limit and thermal shutdown will protect the IC from nearly any fault condition.

## REVERSE CURRENT PROTECTION

During normal system operation, the auxiliary drive circuitry will maintain voltage on the $\mathrm{V}_{\text {OUT }}$ pin when $\mathrm{V}_{\text {IN }}$ is absent. IC reliability and system efficiency are improved by limiting the amount of reverse current that flows from $\mathrm{V}_{\text {OUT }}$ to ground and from $\mathrm{V}_{\text {OUT }}$ to $\mathrm{V}_{\text {IN }}$. Current flows from $V_{\text {OUT }}$ to ground through the feedback resistor divider that sets up the output voltage This resistor can range in value from $6.0 \mathrm{k} \Omega$ to about $10 \mathrm{k} \Omega$, and roughly $500 \mu \mathrm{~A}$ will flow in the typical case. Current flow from $\mathrm{V}_{\text {OUT }}$ to $\mathrm{V}_{\text {IN }}$ will be limited to leakage current after the IC shuts down. On-chip RC time constants are such that the output transistor should be turned off well before $\mathrm{V}_{\mathrm{IN}}$ drops below the $\mathrm{V}_{\text {OUT }}$ voltage.

## CALCULATING POWER DISSIPATION AND HEATSINK REQUIREMENTS

Most linear regulators operate under conditions that result in high on-chip power dissipation. This results in high junction temperatures. Since the IC has a thermal shutdown feature, ensuring the regulator will operate correctly under normal conditions is an important design consideration. Some heatsinking will usually be required.

Thermal characteristics of an IC depend on four parameters: ambient temperature ( $\mathrm{T}_{\mathrm{A}}$ in ${ }^{\circ} \mathrm{C}$ ), power dissipation ( $\mathrm{P}_{\mathrm{D}}$ in watts), thermal resistance from the die to the ambient air $\left(\theta_{\mathrm{JA}}\right.$ in ${ }^{\circ} \mathrm{C}$ per watt) and junction temperature ( $\mathrm{T}_{\mathrm{J}}$ in ${ }^{\circ} \mathrm{C}$ ). The maximum junction temperature is calculated from the formula below:

$$
\mathrm{T}_{\mathrm{J}(\mathrm{MAX})}=\mathrm{T}_{\mathrm{A}}(\mathrm{MAX})+\left(\theta_{\mathrm{JA}} \times \mathrm{P}_{\mathrm{D}}(\mathrm{MAX})\right)
$$

Maximum ambient temperature and power dissipation are determined by the design, while $\theta_{\mathrm{JA}}$ is dependent on the package manufacturer. The maximum junction temperature for operation of the CS5231-3 within specification is $150^{\circ} \mathrm{C}$. The maximum power dissipation of a linear regulator is given as

$$
\begin{aligned}
\mathrm{PD}_{\mathrm{D}(\mathrm{MAX})}= & \left(\mathrm{V}_{\mathrm{IN}}(\mathrm{MAX})-\mathrm{V}_{\mathrm{OUT}(\mathrm{MIN})}\right) \\
& \times\left(\operatorname{ILOAD}(\mathrm{MAX})+\mathrm{V}_{\mathrm{IN}(\mathrm{MAX})}\right) \\
& \times \operatorname{IGND}(\mathrm{MAX})
\end{aligned}
$$

where $\mathrm{I}_{\mathrm{GND}(\mathrm{MAX})}$ is the IC bias current.
It is possible to change the effective value of $\theta_{\mathrm{JA}}$ by adding a heatsink to the design. A heatsink serves in some manner to raise the effective area of the package, thus improving the flow of heat from the package into the surrounding air. Each material in the path of heat flow has its own characteristic thermal resistance, all measured in ${ }^{\circ} \mathrm{C}$ per watt. The thermal resistances are summed to determine the total thermal resistance between the die junction and air. There are three components of interest: junction-to-case thermal resistance $\left(\theta_{\mathrm{JC}}\right)$, case-to-heatsink thermal resistance $\left(\theta_{\mathrm{CS}}\right)$ and heatsink-to-air thermal resistance $\left(\theta_{\mathrm{SA}}\right)$. The resulting equation for junction-to-air thermal resistance is

$$
\theta \mathrm{JA}=\theta \mathrm{JC}+\theta_{\mathrm{CS}}+\theta \mathrm{SA}
$$

The value of $\theta_{\text {JC }}$ both packages of the CS5231-3 are provided in the Packaging Information section of this data sheet. The value of $\theta_{\mathrm{CS}}$ can be considered zero, since heat is conducted out of the D2 2PAK package by the IC leads and the tab, and out of the SOIC package by its IC leads that are soldered directly to the PC board.
Modification of $\theta_{\mathrm{SA}}$ is the primary means of thermal management. For surface mount components, this means modifying the amount of trace metal that connects to the IC.
The thermal capacity of PC board traces is dependent on how much copper area is used, whether or not the IC is in direct contact with the metal, whether or not the metal surface is coated with some type of sealant, and whether or not there is airflow across the PC board. The chart provided below shows heatsinking capability of a square, single sided copper PC board trace. The area is given in square millimeters, and it is assumed there is no airflow across the PC board.


Figure 20. Thermal Resistance Capability of Copper PC Board Metal Traces

TYPICAL D²PAK PC BOARD HEATSINK DESIGN
A typical design of the PC board surface area needed for the $\mathrm{D}^{2}$ PAK package is shown on page 550. Calculations were made assuming $\mathrm{V}_{\mathrm{IN}(\mathrm{MAX})}=5.25 \mathrm{~V}, \mathrm{~V}_{\text {OUT(MIN) }}=$ $3.266 \mathrm{~V}, \mathrm{I}_{\mathrm{OUT}(\mathrm{MAX})}=500 \mathrm{~mA}, \mathrm{I}_{\mathrm{GND}(\mathrm{MAX})}=5.0 \mathrm{~mA}$ and $\mathrm{T}_{\mathrm{A}}$ $=70^{\circ} \mathrm{C}$.

$$
\begin{aligned}
P D= & (5.25 \mathrm{~V}-3.266 \mathrm{~V}) \times 0.5 \mathrm{~A} \\
& +(5.25 \mathrm{~V})(0.005 \mathrm{~A})=1018 \mathrm{~mW}
\end{aligned}
$$

Maximum temperature rise

$$
\begin{gathered}
\Delta \mathrm{T}=\mathrm{T}(\mathrm{MAX})-\mathrm{T}_{\mathrm{A}}=150^{\circ} \mathrm{C}-70^{\circ} \mathrm{C}=80^{\circ} \mathrm{C} \\
\theta \mathrm{JA}(\text { worst case })=\Delta \mathrm{T} / \mathrm{PD}=80^{\circ} \mathrm{C} / 1.018 \mathrm{~W}=78.56^{\circ} \mathrm{C} / \mathrm{W}
\end{gathered}
$$

First, we determine the need for heatsinking. If we assume the maximum $\theta_{\mathrm{JA}}=50^{\circ} \mathrm{C} / \mathrm{W}$ for the $\mathrm{D}^{2} \mathrm{PAK}$, the maximum temperature rise is found to be

$$
\Delta \mathrm{T}=\mathrm{PD} \times \theta \mathrm{JA}=1.018 \mathrm{~W} \times 50^{\circ} \mathrm{C} / \mathrm{W}=50.9^{\circ} \mathrm{C}
$$

This is less than the maximum specified operating junction temperature of $125^{\circ} \mathrm{C}$, and no heatsinking is required. Since the $D^{2}$ PAK has a large tab, mounting this part to the PC board by soldering both tab and leads will provide superior performance with no PC board area penalty.

## TYPICAL 8 LEAD FUSED LEAD SOIC DESIGN

We first determine the need for a heat sink for the 8 Lead SOIC package at a load of 500 mA . Using the dissipation from the $\mathrm{D}^{2}$ PAK example of 1018 mW and the $\theta_{\mathrm{JA}}$ of the SOIC package of $110^{\circ} \mathrm{C} / \mathrm{W}$ gives a temperature rise of $112^{\circ} \mathrm{C}$. Adding this to an ambient temperature of $70^{\circ} \mathrm{C}$ gives $182^{\circ} \mathrm{C}$ junction temperature. This is an excessive temperature rise but it can be reduced by adding additional cooling in the form of added surface area of copper on the PCB. Using the relationship of maximum temperature rise of

$$
\Delta T_{J A}=T_{J}(\mathrm{MAX})-\mathrm{T}_{\mathrm{A}}=150^{\circ} \mathrm{C}-70^{\circ} \mathrm{C}=80^{\circ} \mathrm{C}
$$

We calculate the thermal resistance allowed from junction to air:
$\theta \mathrm{JA}($ worst case $)=\Delta \mathrm{TJA} / \mathrm{PD}=80^{\circ} \mathrm{C} / 1.018 \mathrm{~W}=79.6^{\circ} \mathrm{C} / \mathrm{W}$
The thermal resistance from the die to the leads (case) is $25^{\circ} \mathrm{C} / \mathrm{W}$. Subtracting these two numbers gives the allowable thermal resistance from case to ambient:
$\theta \mathrm{CA}=\theta \mathrm{JA}-\theta \mathrm{JC}=79.6^{\circ} \mathrm{C} / \mathrm{W}-25^{\circ} \mathrm{C} / \mathrm{W}=54.6^{\circ} \mathrm{C} / \mathrm{W}$
The thermal resistance of this copper area will be $54.6^{\circ} \mathrm{C} / \mathrm{W}$. We now look at Figure 20 and find the PCB trace area that will be less than $54.5^{\circ} \mathrm{C} / \mathrm{W}$. Examination shows that $750 \mathrm{~mm}^{2}$ of copper will provide cooling for this part. This would be the SOIC part with the center 4 ground leads soldered to pads in the center of a copper area about 27 mm $\times 27 \mathrm{~mm}$. A lower dissipation or the addition of air-flow could result in a smaller required surface area.

## DESCRIPTION

The CS5231-3 application circuit has been implemented as shown in the following pages. The schematic, bill of materials and printed circuit board artwork can be used to build the circuit. The design is very simple and consists of two capacitors, a p-channel FET and the CS5231-3. Five turret pins are provided for connection of supplies, meters, oscilloscope probes and loads. The CS5231-3 power supply management solution is implemented in an area less than 1.5 square inches. Due to the simplicity of the design, output current must be derated if the CS5231-3 is operated at $\mathrm{V}_{\text {IN }}$ voltages greater than 7.0 V . Figure 21 provides the derating curve on a maximum power dissipation if heatsink is added.

Operating at higher power dissipation without CS5231-3 heatsink may result in a thermal shutdown condition.


Figure 21. Demo Board Output Current Derating vs. $\mathrm{V}_{\mathbf{I N}}$

## The $\mathrm{V}_{\mathrm{IN}}$ Connection

The $\mathrm{V}_{\text {IN }}$ connection is denoted as such on the PC board. The maximum input voltage to the IC is 14 V before damage to the IC is possible. However, the specification range for the IC is $4.75 \mathrm{~V}<\mathrm{V}_{\text {IN }}<6.0 \mathrm{~V}$.

## The GND Connection

The GND connection ties the IC power return to two turret pins. The extra turret pin provides for connection of multiple instrument grounds to the demonstration board.

## The AuxDrv Connection

The AuxDrv lead of the CS5231-3 is connected to the gate of the external PFET. This connection is also brought to a turret pin to allow easy connection of an oscilloscope probe for viewing the AuxDrv waveforms.

## The $\mathrm{V}_{\text {AUX }}$ Connection

The $\mathrm{V}_{\text {AUX }}$ turret pin provides a connection point between an external 3.3 V supply and the PFET drain.

## The Vout Connection

The $\mathrm{V}_{\text {OUT }}$ connection is tied to the $\mathrm{V}_{\text {OUT }}$ lead of the CS5231-3 and the PFET source. This point provides a convenient point at which some type of lead may be applied.


Figure 22. Application Circuit Schematic

## PC Board Layout Artwork

The PC Board is a single layer copper design. The layout artwork is reproduced at actual size below.


Figure 23. Top Copper Layer


Figure 24. Top Silk Screen Layer

## Test Description

The startup and supply transition waveforms shown in Figures 13 through 19 were obtained using the application circuit board with a resistive load of $8.8 \Omega$. This provides a DC load of 375 mA when the regulated output voltage is 3.3 V. A standard 2.0 A bench supply was used to provide power to the application circuit. The transient response waveforms shown in the Typical Performance Characteristics section were obtained by switching a $6.3 \Omega$ resistor across the output.

Temperature Performance
The graph below shows thermal performance for the CS5231-3 across the normal operating output current range.


Figure 25. Package Temperature vs. Load Current ( $\mathrm{V}_{\mathrm{IN}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=23^{\circ} \mathrm{C}$ )

## PFET R ${ }_{\text {DS(ON) }}$ Performance

The graph provided below show typical $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ performance for the PFET. The data is provided as $\mathrm{V}_{\mathrm{DS}}$ vs $I_{\text {OUT }}$ for different values of $\mathrm{V}_{\mathrm{AUX}}$.


Figure 26. PFET VDS vs. IOUT

## CS5231-3

APPLICATIONS CIRCUIT BILL OF MATERIALS

| Refdes | Description | Part Number | Manufacturer | Contact Information |
| :---: | :---: | :---: | :---: | :---: |
| C1, C2 | $33 \mu \mathrm{~F}, 16 \mathrm{~V}$ tantalum capacitors | TAJD336K016 | AVX Corp | www.avxcorp.com <br> $1-843-448-9411$ |
| Q1 | p-channel FET transistor | MGSF1P02ELT1 | ON Semiconductor | http://onsemi.com |
| U1 | Linear regulator with auxiliary | CS5231-3DPS | ON Semiconductor | http://onsemi.com |
| T1-T6 | Turret pins | $40 F 6023$ | Newark Electronics | www.newark.com |
|  |  |  |  | $1-800-463-9275$ |

PACKAGE THERMAL DATA

| Parameter |  | D$^{2}$ PAK 5-Pin | SO-8 | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.5 | 25 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | $10-50^{*}$ | 110 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on thermal properties of substrate. $R_{\theta J A}=R_{\theta J C}+R_{\theta C A}$.

## CS5233-3

## 500 mA and 1.5 A, 3.3 V Dual Input Linear Regulator with Auxiliary Control

The CS5233-3 provides a glitch-free 3.3 V output from one of three possible supplies, ( $\mathrm{V}_{\mathrm{IN}}, \mathrm{V}_{\mathrm{SB}}$ and $\left.3.3 \mathrm{~V}_{\mathrm{AUX}}\right)$. An on-chip linear regulator powers the output when either $\mathrm{V}_{\mathrm{IN}}$ or $\mathrm{V}_{\mathrm{SB}}$ is available. Otherwise AuxDrv turns on an external PFET, which connects the $3.3 \mathrm{~V}_{\mathrm{AUX}}$ supply to the output. The CS5233-3 is intended to provide power to an ASIC on a PCI Network Interface Card (NIC), and meets Intel's "Instantly Available" power requirements which follow from the Advanced Configuration and Power Interface (ACPI) standards. Other applications include desktop computers, power supplies with multiple input sources, and PCMCIA interface cards.

The CS5233-3 linear regulator provides a fixed 3.3 V output at up to 1.5 A with an overall accuracy of $\pm 2 \%$. The internal NPN-PNP composite pass transistor provides a low dropout voltage and requires less supply current than a straight PNP design. Full protection with both current limit and thermal shutdown is provided. Designed for low reverse current, the IC prevents excessive current from flowing from $\mathrm{V}_{\text {OUT }}$ to either $\mathrm{V}_{\text {IN }}$ or ground when the regulator input voltage is lower than the output. The auxiliary drive control feature allows the use of an external PFET to supply power to the output when the regulator supplies are off.

The CS5233-3 regulator is available in two package types: the 5 Lead D ${ }^{2}$ PAK package (TO-263) and 8 Lead SOIC with 4 Lead Fused (DF8) package. When powered from the $\mathrm{V}_{\text {IN }}$ source, the $\mathrm{D}^{2}$ PAK is rated for 1.5 A and the 8 Lead SOIC is rated for 500 mA . Both packages are rated for 500 mA when only powered from the $\mathrm{V}_{\mathrm{SB}}$ source.

## Features

- Linear Regulator
- $3.3 \mathrm{~V} \pm 2 \%$ Output Voltage
- Current Limit
- Thermal Shutdown with Hysteresis
- $400 \mu \mathrm{~A}$ Reverse Current
- ESD Protected
- System Power Management
- Auxiliary Supply Control
- "Glitch Free" Transition Between 3 Sources
- Similar to CS5231-3
- High Output Current Capability
$-1.5 \mathrm{~A} \mathrm{D}^{2} \mathrm{PAK}$
- 500 mA 8 Lead SOIC DF8
- Internally Fused Leads in SO-8 Package


ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAMS


Pin 1. $V_{S B}$
2. $\mathrm{V}_{\mathrm{IN}}$
3. GND
4. $\mathrm{V}_{\text {OUT }}$
5. AuxDrv


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5233-3GDP5 | D$^{2}$ PAK | 50 Units/Rail |
| CS5233-3GDPR5 | D²PAK | 750 Tape \& Reel |
| CS5233-3GDF8 | SO-8 | 95 Units/Rail |
| CS5233-3GDFR8 | SO-8 | 2500 Tape \& Reel |



Figure 1. Application Diagram, 5.0 V to 3.3 V Dual Input Regulator with Auxiliary PFET Power Switch

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Operating Junction Temperature | Reflow: (SMD styles only) (Note 1 ) | 230 peak |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature Range | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input (Main) | $\mathrm{V}_{\text {IN }}$ | 6.0 V | -0.3 V | 100 mA | Internally Limited |
| IC Power Input (Standby) | $\mathrm{V}_{\text {SB }}$ | 6.0 V | -0.3 V | 100 mA | Internally Limited |
| Output Voltage | $\mathrm{V}_{\text {OUT }}$ | 6.0 V | -0.3 V | Internally Limited | 100 mA |
| Auxiliary Drive Output | AuxDrv | 6.0 V | -0.3 V | 10 mA | 50 mA |
| IC Ground | GND | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C} ; 4.75 \mathrm{~V}<\mathrm{V}_{\text {IN }}\right.$; $\mathrm{V}_{\mathrm{SB}}<6.0 \mathrm{~V}$; $\mathrm{C}_{\text {OUT }} \geq 10 \mu \mathrm{~F}$ with $\mathrm{ESR}<1.0 \Omega$, lout $=10 \mathrm{~mA}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Linear Regulator |  |  |  |  |  |
| Output Voltage | 10 mA < $\mathrm{I}_{\text {OUT }}$ < $\mathrm{I}_{\text {MAX }}$. Note 2 | $3.234-2 \%$ | 3.3 | $3.366+2 \%$ | V |
| Line Regulation | $\begin{aligned} & \text { IOUT }=10 \mathrm{~mA} ; \mathrm{V}_{\text {SOURCE }}=4.75 \mathrm{~V} \text { to } 6.0 \mathrm{~V} \text {. } \\ & \text { Note } 3 \end{aligned}$ | - | 1.0 | 5.0 | mV |
| Load Regulation | $\mathrm{V}_{\text {SOURCE }}=5.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ to $\mathrm{I}_{\text {MAX }}$. <br> Note 2 Note 3 | - | 5.0 | 15 | mV |

2. $\mathrm{I}_{\mathrm{MAX}}=1.5 \mathrm{~A}$ for $\mathrm{D}^{2}$ PAK only and with $\mathrm{V}_{\mathrm{IN}}>4.75 \mathrm{~V}$, otherwise $\mathrm{I}_{\mathrm{MAX}}=500 \mathrm{~mA}$.
3. Applies to either $\mathrm{V}_{\mathbb{I N}}$ or $\mathrm{V}_{\mathrm{SB}}$.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C} ; 4.75 \mathrm{~V}<\mathrm{V}_{\mathrm{IN}} ; \mathrm{V}_{\mathrm{SB}}<6.0 \mathrm{~V}\right.$; $\mathrm{C}_{\text {OUT }} \geq 10 \mu \mathrm{~F}$ with $\mathrm{ESR}<1.0 \Omega$, Iout = 10 mA ; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Linear Regulator |  |  |  |  |  |
| Ground Current | $\begin{aligned} & \text { IOUT }=10 \mathrm{~mA} \\ & \text { IOUT }=500 \mathrm{~mA} \\ & \text { IOUT }=1.5 \mathrm{~A} . \text { Note } 4 \end{aligned}$ | - | $\begin{aligned} & 2.0 \\ & 3.0 \\ & 9.0 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 6.0 \\ & 20 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Reverse Current | $\mathrm{V}_{\text {SOURCE }}=0 \mathrm{~V}$; $\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}$. Note 4 | - | 0.4 | 1.0 | mA |
| Current Limit $\mathrm{V}_{\text {IN }}$ Input <br> 8 Lead SOIC <br> 5 Lead D²PAK | $\begin{aligned} & 0 \mathrm{~V}<\mathrm{V}_{\mathrm{OUT}}<3.2 \mathrm{~V} \\ & \mathrm{~V}_{\text {IN }}>4.25 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 0.55 \\ 1.6 \end{gathered}$ | $\begin{aligned} & 0.8 \\ & 2.4 \end{aligned}$ | $\begin{aligned} & 1.3 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Current Limit $\mathrm{V}_{\text {SB }}$ Input Either Package | $0 \mathrm{~V}<\mathrm{V}_{\text {OUT }}<3.2 \mathrm{~V} ; \mathrm{V}_{\text {IN }}<4.25 \mathrm{~V} ; \mathrm{V}_{\mathrm{SB}}>4.25 \mathrm{~V}$ | 0.55 | 0.8 | 1.3 | A |
| Thermal Shutdown | Note 5 | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | Note 5 | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

Auxiliary Drive

| $\mathrm{V}_{\text {IN }}$ Turn-On Threshold | $\mathrm{V}_{\mathrm{SB}}=0 \mathrm{~V}$; Ramp $\mathrm{V}_{\mathrm{IN}}$ up until AuxDrv goes high and regulator turns on | 4.35 | 4.5 | 4.65 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IN }}$ Turn-Off Threshold | $\mathrm{V}_{\mathrm{SB}}=0 \mathrm{~V}$; Ramp $\mathrm{V}_{\mathrm{IN}}$ down until AuxDrv goes low and regulator turns off | 4.25 | 4.4 | 4.55 | V |
| $\mathrm{V}_{\text {SB }}$ Turn-On Threshold | $\mathrm{V}_{\mathrm{SB}}=0 \mathrm{~V}$; Ramp $\mathrm{V}_{\mathrm{SB}}$ up until AuxDrv goes high and regulator turns on | 4.35 | 4.5 | 4.65 | V |
| $\mathrm{V}_{\text {SB }}$ Turn-Off Threshold | $\mathrm{V}_{\mathrm{SB}}=0 \mathrm{~V}$; Ramp $\mathrm{V}_{\mathrm{SV}}$ down until AuxDrv goes low and regulator turns off | 4.25 | 4.4 | 4.55 | V |
| Threshold Hysteresis | - | 75 | 100 | 125 | mV |
| AuxDrv Peak Voltage | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0 \mathrm{~V} ; 0 \mathrm{~V}<\mathrm{V}_{\text {SOURCE }}<2.0 \mathrm{~V} \text {. Note } 4 \\ & \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V} ; \mathrm{I}_{\text {AuxD }}=100 \mu \mathrm{~A} ; \\ & 2.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<4.25 \mathrm{~V} ; 2.0 \mathrm{~V}<\mathrm{V}_{\mathrm{SB}}<4.25 \mathrm{~V} \\ & \mathrm{~V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{I}_{\text {AuxDrv }}=100 \mu \mathrm{~F} ; \\ & 0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<4.25 \mathrm{~V} ; 0 \mathrm{~V}<\mathrm{V}_{\text {SB }}<4.25 \mathrm{~V} \end{aligned}$ | - | $\begin{aligned} & 0.4 \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 1.8 \\ & 0.4 \\ & 0.4 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \\ & \text { v } \end{aligned}$ |
| AuxDrv High Voltage | $\mathrm{V}_{\text {IN }}$ or $\mathrm{V}_{\text {SB }}>4.65 \mathrm{~V}$ | 3.75 | 4.0 | - | V |
| AuxDrv Pin Current Limit | $\mathrm{V}_{\text {AuxDrv }}=1.0 \mathrm{~V}$; $\mathrm{V}_{\text {SOURCE }}=4.0$. Note 4 | 0.5 | 6.0 | 25 | mA |
| $\mathrm{V}_{\text {AuxDrv }}$ Turn-Off Response Time | Step $V_{\text {SOURCE }}$ from 4.0 V to 5.0 V . Note 4 Note 5 | - | 20 | 40 | $\mu \mathrm{s}$ |
| $\mathrm{V}_{\text {AuxDrv }}$ Turn-On Response Time | Step $\mathrm{V}_{\text {SOURCE }}$ from 5.0 V to 4.0 V . Note 4 Note 5 | - | 1.0 | 10 | $\mu \mathrm{s}$ |
| Pull-Up Resistance | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{IN}}>4.7 \mathrm{~V}$. Note 4 Note 5 | 5.0 | 10 | 25 | $\mathrm{k} \Omega$ |

4. Applies to either $\mathrm{V}_{\mathbb{I N}}$ or $\mathrm{V}_{\mathrm{SB}}$.
5. Guaranteed by design, not $100 \%$ production tested.

PACKAGE PIN DESCRIPTION

| Package Lead \# |  |  |  |
| :---: | :---: | :---: | :--- |
| $\mathbf{5}$ Lead D2PAK | $\mathbf{8}$ Lead SO Narrow | Lead Symbol |  |
| 1 | 1 | $\mathrm{~V}_{\mathrm{SB}}$ | Standby 5.0 V input voltage. |
| 2 | 2 | $\mathrm{~V}_{\text {IN }}$ | 5.0 V Main input voltage. |
| $3, \mathrm{Tab}$ | $5,6,7,8$ | GND | Ground and IC substrate connection. |
| 4 | 3 | $\mathrm{~V}_{\text {OUT }}$ | Regulated output voltage. |
| 5 | 4 | AuxDrv | Control voltage for the external PFET switched auxiliary supply. This <br> pin drives low if $\mathrm{V}_{\text {IN }}$ and $\mathrm{V}_{\mathrm{SB}}$ are less than 4.4 V (typical), otherwise it <br> is pulled up to the greater of $\mathrm{V}_{\text {IN }}$ or $\mathrm{V}_{\mathrm{SB}}$ through an internal diode and <br> $10 \mathrm{k} \Omega$ resistor. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Output Voltage vs. Junction Temperature, Output Voltage when Powered by $\mathrm{V}_{\mathrm{IN}}$ or $\mathrm{V}_{\mathrm{SB}}$


Figure 5. Ground Pin Current vs. Output Current, $\mathrm{V}_{\mathrm{SB}}$ Data with $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$


Figure 7. Transient Load Response, Transient Response for 1.5 A Step Load, $\mathrm{V}_{\mathrm{IN}}=5.0 \mathrm{~V}$, $\mathrm{C}_{\text {OUT }}=33 \mu \mathrm{~F} @ 0.4 \Omega$ ESR


Figure 4. Output Voltage vs. Load Current, $\mathrm{V}_{\text {SB }}$ Values Taken with $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}$


Figure 6. Reverse Current vs. Junction Temperature


Figure 8. AuxDrv Response Time


Figure 9. $\mathrm{V}_{\mathrm{IN}}$ Threshold vs. Junction Temperature, Typical Minimum and Maximum Threshold Voltages to Switch AuxDrv Control


Figure 10. AuxDrv High Voltage vs. Junction Temperature


Figure 11. AuxDrv Voltage vs. Input Voltage ( $\mathrm{V}_{\text {SB }}$ or $\mathrm{V}_{\mathrm{IN}}$ ) at Three Temperatures

## APPLICATIONS INFORMATION

INPUT AND OUTPUT VOLTAGE MATRIX

| Input |  |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IN}}$ | $\mathrm{V}_{\text {SB }}$ | $3.3 \mathrm{~V}_{\text {AUX }}$ | AuxDrv/5.0 V Detect | $\mathrm{V}_{\text {OUT }}$, 5 Lead D2PAK | $\mathrm{V}_{\text {OUT }} 8$ Lead SOIC |
| 0 V | 0 V | 0 V | On (low) | 0 V | 0 V |
| 0 V | 0 V | 3.3 V | On (low) | $3.3 \mathrm{~V}_{\text {AUX }}$ | $3.3 \mathrm{~V}_{\text {AUX }}$ |
| 0 V | 5.0 V | 0 V | Off (high) | $3.3 \mathrm{~V}_{\text {REG }}$ @ 500 mA | $3.3 \mathrm{~V}_{\text {REG }} @ 500 \mathrm{~mA}$ |
| 0 V | 5.0 V | 3.3 V | Off (high) | $3.3 \mathrm{~V}_{\text {REG }} @ 500 \mathrm{~mA}$ | $3.3 \mathrm{~V}_{\text {REG }}$ @ 500 mA |
| 5.0 V | 0 V | 0 V | Off (high) | $3.3 \mathrm{~V}_{\text {REG }} @ 1.5 \mathrm{~A}$ | $3.3 \mathrm{~V}_{\text {REG }} @ 500 \mathrm{~mA}$ |
| 5.0 V | 0 V | 3.3 V | Off (high) | $3.3 \mathrm{~V}_{\text {REG }} @ 1.5 \mathrm{~A}$ | $3.3 \mathrm{~V}_{\text {REG }} @ 500 \mathrm{~mA}$ |
| 5.0 V | 5.0 V | 0 V | Off (high) | $3.3 \mathrm{~V}_{\text {REG }}$ @ 1.5 A | $3.3 \mathrm{~V}_{\text {REG }} @ 500 \mathrm{~mA}$ |
| 5.0 V | 5.0 V | 3.3 V | Off (high) | 3.3 VREG @ 1.5 A | 3.3 V $\mathrm{REG}^{\text {@ }} 500 \mathrm{~mA}$ |

## THEORY OF OPERATION

## Linear Regulator

The CS5233-3 is a dual input fixed 3.3 V linear regulator that contains an auxiliary drive control feature. When $\mathrm{V}_{\mathrm{IN}}$ alone is present, or $\mathrm{V}_{\text {IN }}$ and $\mathrm{V}_{\text {SB }}$ are simultaneously present, the CS5233-3 uses the $\mathrm{V}_{\text {IN }}$ supply to generate the 3.3 V output at currents of up to 1.5 A . When $\mathrm{V}_{\mathrm{SB}}$ alone is present, the CS5233-3 uses the $\mathrm{V}_{\mathrm{SB}}$ supply to generate the 3.3 V output at currents of up to 500 mA . The linear regulator is composed of a composite PNP-NPN pass transistor to provide low-voltage dropout capability. An output capacitor greater than $10 \mu \mathrm{~F}$ with equivalent series resistance (ESR) less than $1.0 \Omega$ is required for compensation. More information is provided in the Stability Considerations section.

## Auxiliary Drive Feature

The CS5233-3 provides an auxiliary drive feature that allows a load to remain powered even if both supplies to the IC are absent. An external p-channel FET is the only additional component required to implement this function when the auxiliary power supply is available. The PFET gate is connected to the IC's AuxDrv output, the PFET drain is connected to the auxiliary power supply, and the PFET source is connected to the load. The polarity of this connection is very important, since the PFET body diode will be connected between the load and the auxiliary supply. If the PFET is connected with its drain to the load and its source to the supply, the body diode could be forward-biased if the auxiliary supply is not present. This would result in the linear regulator providing current to everything on the auxiliary supply rail.

The AuxDrv ( 5.0 V detect) output is pulled up to the input voltage through an internal resistor when $\mathrm{V}_{\text {IN }}$ or $\mathrm{V}_{\mathrm{SB}}$ are available. If $\mathrm{V}_{\text {IN }}$ and $\mathrm{V}_{\text {SB }}$ are not available or both drop below 4.4 V , the AuxDrv output goes low, turning on an external PFET that connects the 3.3 V auxiliary supply to the
load. The AuxDrv is low only when neither $\mathrm{V}_{\text {IN }}$ nor $\mathrm{V}_{\mathrm{SB}}$ are available.
There is 100 mV of hysteresis (typical) in the circuitry that determines if $\mathrm{V}_{\mathrm{IN}}$ or $\mathrm{V}_{\mathrm{SB}}$ are present.

## STABILITY CONSIDERATIONS

The output capacitor helps determine three main characteristics of a linear regulator: loop stability, load transient response, and start-up delay. The CS5233-3 is designed to be stable with an output capacitor that has a minimum value of $10 \mu \mathrm{~F}$ and an equivalent series resistance less than $1.0 \Omega$. To guarantee loop stability, the output capacitor should be located close to the regulator output and ground pins. The load transient response, during the time it takes the regulator to respond, is also determined by the output capacitor. For large changes in load current, the ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{ESR}
$$

There is then an additional drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{T} / \mathrm{C}
$$

where T is the time for the regulation loop to begin to respond, (typically $4.0 \mu$ s for the CS5233-3). If tight output regulation is required with fast changing loads, a capacitor network of tantalum and low ESR ceramic capacitors can be added as close to the load as possible, with enough capacitance and a reduced ESR to minimize the voltage change, as determined by the formulas above.

## Input Capacitors and the Vin Thresholds

A capacitor placed on the $\mathrm{V}_{\text {IN }}$ pin will help to improve transient response. During a load transient, the input capacitor serves as a charge "reservoir," providing the needed extra current until the external power supply can
respond. One of the consequences of providing this current is an instantaneous voltage drop at $\mathrm{V}_{\text {IN }}$ due to capacitor ESR. The magnitude of the voltage change is again the product of the current change and the capacitor ESR.

It is very important to consider the maximum current step that can exist in the system. If the change in current is large enough, it is possible that the instantaneous voltage drop on $\mathrm{V}_{\text {IN }}$ will exceed the $\mathrm{V}_{\text {IN }}$ threshold hysteresis, and the IC will enter a mode of operation resembling an oscillation. As the part turns on, the output current IOUT will increase, reaching current limit during initial charging. Increasing IOUT results in a drop at $\mathrm{V}_{\text {IN }}$ such that the shutdown threshold is reached. The part will turn off, and the load current will decrease. As IOUT decreases, $\mathrm{V}_{\text {IN }}$ will rise and the part will turn on, starting the cycle all over again. This oscillatory operation is most likely at initial start-up when the output capacitance is not charged, and in cases where the ramp-up of the $\mathrm{V}_{\mathrm{IN}}$ supply is slow. It may also occur during the power transition when the linear regulator turns on and the PFET turns off. A $20 \mu \mathrm{~s}$ delay exists between turn-on of the regulator and the AuxDrv pin pulling the gate of the PFET high. This delay prevents "chatter" during the power transitions.

If required, using a few capacitors in parallel to increase the bulk charge storage and reduce the ESR should give better performance than using a single input capacitor. Short, straight connections between the power supply and $\mathrm{V}_{\text {IN }}$ lead along with careful layout of the PC board ground plane will reduce parasitic inductance effects. Wide $\mathrm{V}_{\text {IN }}$ and $V_{\text {OUT }}$ traces will reduce resistive voltage drops.

## Choosing the PFET Switch

The choice of the external PFET switch is based on two main considerations. First, the PFET should have a very low turn-on threshold. Choosing a switch transistor with $\mathrm{V}_{\mathrm{GS}(\mathrm{ON})} \approx 1.0 \mathrm{~V}$ will ensure the PFET will be fully enhanced with only 3.3 V of gate drive voltage. Second, the switch transistor should be chosen to have a low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ to minimize the voltage drop due to current flow in the switch. The formula for calculating the maximum allowable on-resistance is

$$
\operatorname{RDS}(\mathrm{ON}) \mathrm{MAX}=\frac{\mathrm{V}_{\text {AUX }}(\mathrm{MIN})-\mathrm{V}_{\text {OUT }}(\mathrm{MIN})}{1.5 \times \operatorname{lOUT}(\mathrm{MAX})}
$$

$\mathrm{V}_{\text {AUX(MIN) }}$ is the minimum value of the auxiliary supply voltage, $\mathrm{V}_{\mathrm{OUT}(\mathrm{MIN})}$ is the minimum allowable output voltage, $\mathrm{I}_{\mathrm{OUT}(\mathrm{MAX})}$ is the maximum output current and 1.5 is a "fudge factor" to account for increases in $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ due to temperature.

## Output Voltage Sensing

It is not possible to remotely sense the output voltage of the C5233-3 since the feedback path to the error amplifier is not externally available. It is important to minimize voltage drops due to metal resistance of high current PC board traces. Such voltage drops can occur in both the supply traces and the return traces.

The following board layout practices will help to minimize output voltage errors:

- Always place the linear regulator as close to both load and output capacitors as possible.
- Always use the widest possible traces to connect the linear regulator to the capacitor network and to the load.
- Connect the load to ground through the widest possible traces.
- Connect the IC ground to the load ground trace at the point where it connects to the load.


## Current Limit

The CS5233-3 has internal current limit protection. Output current is limited to a typical value of 3.0 A for the $D^{2}$ PAK using $V_{\text {IN }}$ and 800 mA using $\mathrm{V}_{\mathrm{SB}}$, even under output short circuit conditions. If the load current drain exceeds the current limit value, the output voltage will be pulled down and will result in an out of regulation condition.

## Thermal Shutdown

The CS5233-3 has internal temperature monitoring circuitry. The output is disabled if junction temperature of the IC reaches $180^{\circ} \mathrm{C}$. Thermal hysteresis is typically $25^{\circ} \mathrm{C}$ and allows the IC to recover from a thermal fault without the need for an external reset signal. The monitoring circuitry is located near the composite PNP-NPN output transistor, since this transistor is responsible for most of the on-chip power dissipation. The combination of current limit and thermal shutdown will protect the IC from nearly any fault condition.

## Reverse Current Protection

During normal system operation, the auxiliary drive circuitry will maintain voltage on the VOUT pin. IC reliability and system efficiency are improved by limiting the amount of reverse current that flows from $\mathrm{V}_{\text {OUT }}$ to ground and from $\mathrm{V}_{\text {OUT }}$ to $\mathrm{V}_{\text {IN }}$. Current flows from $\mathrm{V}_{\text {OUT }}$ to ground through the feedback resistor divider that sets up the output voltage, typically $400 \mu \mathrm{~A}$. Current flow from V VUT to $\mathrm{V}_{\text {IN }}$ will be limited to leakage current after the IC shuts down. On-chip RC time constants are such that the output transistor should be turned off well before $\mathrm{V}_{\text {IN }}$ drops below the $\mathrm{V}_{\text {OUT }}$ voltage.

## Calculating Power Dissipation and Heatsink Requirements

Most linear regulators operate under conditions that result in high on-chip power dissipation. This results in high junction temperatures. Since the IC has a thermal shutdown feature, ensuring the regulator will operate correctly under normal conditions is an important design consideration. Some heatsinking will usually be required.

Thermal characteristics of an IC depend on four parameters: ambient temperature ( $\mathrm{T}_{\mathrm{A}}$ in ${ }^{\circ} \mathrm{C}$ ), power dissipation ( $\mathrm{P}_{\mathrm{D}}$ in watts), thermal resistance from the die to the ambient air $\left(\theta_{\mathrm{JA}}\right.$ in ${ }^{\circ} \mathrm{C}$ per watt $)$ and junction temperature
( $\mathrm{T}_{\mathrm{J}}$ in ${ }^{\circ} \mathrm{C}$ ). The maximum junction temperature is calculated from the formula below:

$$
\mathrm{T}_{\mathrm{J}(\mathrm{MAX})}=\mathrm{T}_{\mathrm{A}(\mathrm{MAX})}+\theta \mathrm{JA} \times \mathrm{P}_{\mathrm{D}}(\mathrm{MAX})
$$

Maximum ambient temperature and power dissipation are determined by the design, while $\theta_{\mathrm{JA}}$ is dependent on the package manufacturer. The maximum junction temperature for operation of the CS5233-3 within specification is $150^{\circ} \mathrm{C}$. The maximum power dissipation of a linear regulator is given as

$$
\begin{aligned}
\operatorname{PD}(\mathrm{MAX})= & \left(\mathrm{VIN}^{\prime}(\mathrm{MAX})-\mathrm{V}_{\mathrm{OUT}}(\mathrm{MIN})\right) \\
& \times \operatorname{ILOAD}(\mathrm{MAX})+\mathrm{V}_{\mathrm{IN}(\mathrm{MAX})} \\
& \times \operatorname{IGND}(\mathrm{MAX})
\end{aligned}
$$

where $\mathrm{I}_{\mathrm{GND}(\mathrm{MAX})}$ is the IC bias current.
It is possible to change the effective value of $\theta_{\mathrm{JA}}$ by adding a heatsink to the design. A heatsink serves in some manner to raise the effective area of the package, thus improving the flow of heat from the package into the surrounding air. Each material in the path of heat flow has its own characteristic thermal resistance, all measured in ${ }^{\circ} \mathrm{C}$ per watt. The thermal resistances are summed to determine the total thermal resistance between the die junction and air. There are three components of interest: junction-to-case thermal resistance $\left(\theta_{\mathrm{JC}}\right)$, case-to-heatsink thermal resistance $\left(\theta_{\mathrm{CS}}\right)$ and heatsink-to-air thermal resistance $\left(\theta_{\mathrm{SA}}\right)$. The resulting equation for junction-to-air thermal resistance is

$$
\begin{aligned}
& \theta \mathrm{JA}=\theta \mathrm{JC}+\theta \mathrm{CS}+\theta \mathrm{SA}, \text { or } \\
& \theta \mathrm{JA}=\theta \mathrm{JC}+\theta \mathrm{SA} \text { for } \theta \mathrm{CS}=0
\end{aligned}
$$

The value of $\theta_{\mathrm{JC}}$ for the CS5233-3 is provided in the Packaging Information section of this data sheet. $\theta_{\mathrm{CS}}$ can be considered zero, since heat is conducted out of the package by the IC leads and the tab of the $\mathrm{D}^{2}$ PAK package, and since the IC leads and tab are soldered directly to the PC board.

Modification of $\theta_{\mathrm{SA}}$ is the primary means of thermal management. For surface mount components, this means modifying the amount of trace metal that connects to the IC.

The thermal capacity of PC board traces is dependent on how much copper area is used, if the IC is in direct contact with the metal, whether the metal surface is coated with some type of sealant, and whether there is airflow across the PC board. The chart provided below shows heatsinking capability of a square, single sided copper PC board trace. The area is given in square millimeters, and it is assumed there is no airflow across the PC board.


Figure 12. Thermal Resistance Capability of Copper PC Board Metal Traces

PACKAGE THERMAL DATA

| Parameter |  | 5 Lead D2PAK | 8 Lead SOIC | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | $1.0-4.0$ | 25 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | $10-50^{*}$ | 110 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on thermal properties of substrate. $R_{\theta J A}=R_{\theta J C}+R_{\theta C A}$.

## CS8140, CS8141

### 5.0 V, 500 mA Linear Regulator with ENABLE, RESET, and Watchdog

The CS8140 and CS8141 are linear regulators suited for microprocessor applications in automotive environments.

These ON Semiconductor parts provide the power for the microprocessors along with many of the control functions needed in today's computer based systems. Incorporating all of these features saves both cost, and board space.

Packages are available for surface mounting as well as through hole mounting.

The CS8141 has the same feature set as the CS8140 with the exception of the response to the watchdog signals (WDI). The CS8141 only responds to input signals (WDI) which are below the preset watchdog frequency threshold.

## Features

- $5.0 \mathrm{~V} \pm 4.0 \%$, 500 mA Output Voltage
- $\mu \mathrm{P}$ Compatible Control Functions
- Watchdog
- $\overline{\text { RESET }}$
- ENABLE
- Low Dropout Voltage (1.25 V @ 500 mA )
- Low Quiescent Current ( 7.0 mA @ 500 mA )
- Low Noise, Low Drift
- Low Current SLEEP Mode ( $\mathrm{I}_{\mathrm{Q}}=250 \mu \mathrm{~A}$ )
- Fault Protection
- Thermal Shutdown
- Short Circuit
- 60 V Peak Transient Voltage

ON Semiconductor ${ }^{\text {ww }}$
http://onsemi.com


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 574 of this data sheet.

PIN CONNECTIONS


Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Operating Range |  | -0.5 to 26 | V |
| Peak Transient Voltage (46 V Load Dump @ 14 V V ${ }_{\text {BAT }}$ ) |  | 60 | V |
| Electrostatic Discharge (Human Body Model) |  | 4.0 | kV |
| WDI Input Signal Range |  | -0.3 to 7.0 | V |
| Internal Power Dissipation |  | Internally Limited | - |
| Junction Temperature Range ( $\mathrm{T}_{\mathrm{J}}$ ) |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ENABLE |  | -0.3 to $\mathrm{V}_{\mathrm{IN}}$ | V |
| Package Thermal Resistance, TO-220 Seven Lead Junction-to-Case, R ®JC Junction-to-Ambient, R $\mathrm{R}_{\text {JA }}$ |  | $\begin{aligned} & 1.6 \\ & 50 \end{aligned}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, D2PAK 7-Pin Junction-to-Case, R өJC Junction-to-Ambient, R ®JA |  | $\begin{gathered} 1.5 \\ 10-50 \dagger \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ```Package Thermal Resistance, SO-24L Junction-to-Case, R ®JC Junction-to-Ambient, \(\mathrm{R}_{\theta \mathrm{JJA}}\)``` |  | $\begin{aligned} & 16 \\ & 80 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ```Package Thermal Resistance, DIP-14 Junction-to-Case, R ®JC Junction-to-Ambient, \(\mathrm{R}_{\theta \mathrm{JA}}\)``` |  | $\begin{aligned} & 48 \\ & 85 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2) | 260 peak 230 peak | ${ }^{\circ} \mathrm{C}$ |

*The maximum package power dissipation must be observed.
$\dagger$ Depending on thermal properties of substrate $R_{\theta J A}=R_{\theta J C}+R_{\theta C A}$.

1. 10 second maximum.
2. 60 seconds max above $183^{\circ} \mathrm{C}$.

ELECTRICAL CHARACTERISTICS $\left(7.0 \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{OUT}} \leq 500 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}\right.$,
$-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$, unless otherwise noted.) Note 3 .

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage ( $\mathrm{V}_{\text {OUT }}$ ) |  |  |  |  |  |
| Output Voltage, V ${ }_{\text {OUT }}$ | 7.0 $\mathrm{V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 5.0 \mathrm{~mA}<\mathrm{l}_{\text {OUT }}<500 \mathrm{~mA}$ | 4.8 | 5.0 | 5.2 | V |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\mathrm{l}_{\text {OUT }}=500 \mathrm{~mA}$ | - | 1.25 | 1.50 | V |
| Line Regulation | $\mathrm{I}_{\text {OUT }}=50 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, | - | 5.0 | 25 | mV |
| Load Regulation | $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}, 50 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 500 \mathrm{~mA}$ | - | 5.0 | 80 | mV |
| Output Impedance, R OUT $^{\text {a }}$ | 500 mA DC and 10 mA AC , $100 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | - | 200 | - | $\mathrm{m} \Omega$ |
| Quiescent Current, (IQ) Active Mode Sleep Mode | $\begin{aligned} & 0 \leq \mathrm{l}_{\text {OUT }} \leq 500 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V} \\ & \mathrm{I}_{\text {UUT }}=0 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=13 \mathrm{~V}, \text { ENABLE }=0 \mathrm{~V} \end{aligned}$ | - | $\begin{gathered} 7.0 \\ 0.25 \end{gathered}$ | $\begin{gathered} 15 \\ 0.50 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple Rejection | $\begin{aligned} & 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 17 \mathrm{~V}, \text { IOUT }=250 \mathrm{~mA}, \\ & \mathrm{f}=120 \mathrm{~Hz} \end{aligned}$ | 60 | 75 | - | dB |
| Current Limit | - | 700 | 1200 | 2000 | mA |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT }}<1.0 \mathrm{~V}$ | 30 | 34 | 38 | V |

3. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

ELECTRICAL CHARACTERISTICS (continued) $\left(7.0 \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\mathrm{OUT}} \leq 500 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}\right.$, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$, unless otherwise noted.) Note 4 .

| $\mid$ Characteristic |
| :--- |
| Test Conditions |
| ENABLE |
| Threshold |
| HIGH |
| LOW |

RESET

| Threshold HIGH $\mathrm{V}_{\mathrm{R}(\mathrm{HI})}$ | V OUT Increasing | 4.65 | 4.90 | VOUT -0.05 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Threshold LOW $\mathrm{V}_{\text {R(LOW) }}$ | $V_{\text {Out }}$ Decreasing | 4.50 | 4.70 | 4.90 | V |
| Threshold Hysteresis ( $\mathrm{V}_{\mathrm{RH}}$ ) | (HIGH - LOW) | 150 | 200 | 250 | mV |
| RESET Output Leakage RESET $=$ HIGH | $\mathrm{V}_{\text {OUT }} \geq \mathrm{V}_{\text {R(HI) }}$ | - | - | 25 | $\mu \mathrm{A}$ |
| Output Voltage Low ( $\mathrm{V}_{\text {(LOW })}$ ) | $1.0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq \mathrm{V}_{\mathrm{R}(\text { LOW })}, \mathrm{R}_{\mathrm{P}}=2.7 \mathrm{k} \Omega$, Note 5. | - | 0.1 | 0.4 | V |
| Output Voltage Low (V $\mathrm{V}_{\text {Reak }}$ ) | $\mathrm{V}_{\text {Out }}$, Power up, Power down | - | 0.6 | 1.0 | V |
| Delay Times tpor | $\mathrm{C}_{\text {DELAY }}=0.1 \mu \mathrm{~F}$ | 30 | 47.5 | 65 | ms |
| Delay Times twdi( $\overline{\text { RESET }}$ ) | $\mathrm{C}_{\text {DELAY }}=0.1 \mu \mathrm{~F}$ | 0.5 | 1.0 | 1.5 | ms |

## Watchdog

| Input Voltage High | - | 2.0 | - | - | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Voltage Low | - | - | - | 0.8 | V |
| Input Current | WDI $\leq \mathrm{V}_{\text {OUT }}$ | - | 0 | 10 | $\mu \mathrm{A}$ |
| Threshold Frequency f ${ }_{\text {WIII(LOWER) }}$ | $\mathrm{C}_{\text {DELAY }}=0.1 \mu \mathrm{~F}$ | 64 | 77 | 96 | Hz |
| Threshold Frequency f $\begin{aligned} & \text { WII(UPPER) }\end{aligned}$ (Note 6.) | $\mathrm{C}_{\text {DELAY }}=0.1 \mu \mathrm{~F}$ | 218 | 262 | 326 | Hz |

4. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.
5. $R_{P}$ is connected to RESET and $V_{\text {OUT }}$.
6. CS8140 only.

PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  |  | LEAD SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TO-220 | D2PAK | SO-24L | DIP-14 | LEAD SYMBOL |  |
| 1 | 1 | 21 | 12 | $\mathrm{V}_{\text {IN }}$ | Supply voltage to IC, usually direct from the battery. |
| 2 | 2 | 23 | 13 | ENABLE | CMOS compatible logical input. VOUT is disabled when ENABLE is LOW and WDI is beyond its preset limits. |
| 3 | 3 | 24 | 14 | RESET | CMOS compatible output lead. RESET goes low whenever $V_{\text {OUT }}$ drops below $4.5 \%$ of it's typical value for more than $2.0 \mu \mathrm{~s}$ or WDI signal falls outside it's window limits. |
| 4 | 4 | 12, 20 | 8, 11 | GND | Ground Connection. |
| 5 | 5 | 2 | 1 | Delay | Timing capacitor for Watchdog and RESET functions. |
| 6 | 6 | 3 | 2 | WDI | CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming digital pulse train. The signal is usually generated by the system microprocessor. |
| 7 | 7 | 4 | 3 | $\mathrm{V}_{\text {OUT }}$ | Regulated output voltage, 5.0 V (typ). |
| - | - | $\begin{gathered} 1,6-11, \\ 13-19,22 \end{gathered}$ | 5-7, 9, 10 | NC | No connection. |
| - | - | 5 | 4 | Sense | Kelvin connection which allows remote sensing of output voltage for improved regulation. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. V $_{\text {OUT }}$ vs. $\mathrm{V}_{\text {IN }}$ over $\mathrm{R}_{\text {LOAD }} ; \mathbf{T}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$


Figure 4. Dropout Voltage vs. Output Current Over Temperature


Figure 6. Line Regulation vs. Output Current Over Temperature


Figure 3. $\mathrm{V}_{\text {OUT }}$ vs. $\mathrm{V}_{\text {IN }}$ Over Temperature; $\mathrm{R}_{\text {LOAD }}=25 \Omega$


Figure 5. Load Regulation vs. Output Current Over Temperature


Figure 7. Quiescent Current vs. Output Current Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 8. Quiescent Current vs. $\mathrm{V}_{\mathrm{IN}}$ Over R $\mathrm{R}_{\text {LoAD }}$; $\mathrm{T}=25^{\circ} \mathrm{C}$


Figure 10. Watchdog Frequency Thresholds
vs. Temperature


Figure 12. Ripple Rejection vs. Frequency


Figure 9. Quiescent Current vs. $\mathrm{V}_{\mathrm{IN}}$ Over Temperature; R LOAD $=25 \Omega$


Figure 11. Watchdog Frequency Threshold vs. Cbelay


Figure 13. RESET Output Voltage vs. Output Current

## DEFINITION OF TERMS

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques
such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.
Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.
Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
Current Limit: Peak current that can be delivered to the output.

## CIRCUIT DESCRIPTION

The CS8140 is a 5.0 V Watchdog Regulator with protection circuitry and three logic control functions that allow a microprocessor to control its own power supply. The CS8140 is designed for use in automotive, switch mode power supply post regulator, and battery powered systems.

Basic regulator performance characteristics include a low noise, low drift, $5.0 \mathrm{~V} \pm 4.0 \%$ precision output voltage with low dropout voltage ( 1.25 V @ $\mathrm{I}_{\mathrm{OUT}}=500 \mathrm{~mA}$ ) and low quiescent current ( 7.0 mA @ $\mathrm{I}_{\text {OUT }}=500 \mathrm{~mA}$ ). On board short circuit, thermal, and overvoltage protection make it possible to use this regulator in particularly harsh operating environments.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor or other signal source. When the signal frequency moves outside externally programmable window limits, a RESET signal is generated ( $\overline{\text { RESET }}$ ). An external capacitor (CDELAY) programs the watchdog window frequency limits as well as the power on reset (POR) and RESET delay.

The $\overline{\text { RESET }}$ function is activated by any of three conditions: the watchdog signal moves outside of its preset limits; the output voltage drops out of regulation by more than $4.5 \%$; or the IC is in its power up sequence. The $\overline{\text { RESET }}$ signal is independent of $\mathrm{V}_{\mathrm{IN}}$ and reliable down to $\mathrm{V}_{\text {OUT }}=$ 1.0 V .

In conjunction with the Watchdog, the ENABLE function controls the regulator's power consumption. The CS8140's output stage and its attendant circuitry are enabled by setting the ENABLE lead high. The regulator goes into sleep mode when the ENABLE lead goes low and the watchdog signal moves outside its preset window limits. This unique combination of control functions in the CS8140 gives the microprocessor control over its own power down sequence: i.e. it gives the microprocessor the flexibility to perform housekeeping functions before it powers down.

The CS8141 has the same features as the CS8140, except that the CS8141 only responds to input signals (WDI) which are below the preset watchdog frequency threshold.

## VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

## Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within $\pm 4.0 \%$ over temperature and supply variation.

## Output Stage

The composite PNP-NPN output structure (Figure 14) provides $500 \mathrm{~mA}(\mathrm{~min})$ of output current while maintaining a low drop out voltage ( 1.25 V ) and drawing little quiescent current ( 7.0 mA ).


Figure 14. Composite Output Stage of the CS8140/1
The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

## Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 15).
If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.
Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback
circuitry insures that the output current never exceeds a preset limit.


Figure 15. Typical Circuit Waveforms for Output Stage Protection

Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ), the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

## REGULATOR CONTROL FUNCTIONS

The CS8140 differs from all other linear regulators in its unique combination of control features.

## Watchdog and ENABLE Function

$V_{\text {OUT }}$ is controlled by the logic functions ENABLE and Watchdog (Table 1).

Table 1. V OUt as a Function of ENABLE and Watchdog

| $\mathrm{V}_{\text {OUT }}$ (V) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | WDI |  |  |  |  |
| ENABLE | Slow | Normal | Fast | High | Low |
| H | 5 | 5 | 5 | 5 | 5 |
| L | 0 | 5 | 0 | 0 | 0 |

As long as ENABLE is high or ENABLE is low and the Watchdog signal is normal, $\mathrm{V}_{\text {OUT }}$ will be at 5.0 V (typ). If ENABLE is low and the Watchdog signal moves outside programmable limits, the output transistor turns off and the IC goes into SLEEP mode. Only the ENABLE circuitry in the IC remains powered up, drawing a quiescent current of $250 \mu \mathrm{~A}$.

The Watchdog monitors the frequency of an incoming WDI signal. If the signal falls outside of the WDI window, a frequency programmable pulse train is generated at the RESET lead (Figure 16) until the correct Watchdog input signal reappears at the lead $(\mathrm{ENABLE}=\mathrm{HIGH})$.

The lower and upper window threshold limits of the watchdog function are set by the value of CDELAY. The limits are determined according to the following equations for the CS8140:
(a) $\operatorname{tWDI}($ LOWER $)=(1.3 \times 105)$ CDELAY or fWDI $($ LOWER $)=\left(7.69 \times 10^{-6}\right)$ CDELAY $^{-1}$
(b) tWDI(UPPER) $=\left(3.82 \times 10^{-4}\right)$ CDELAY or fWDI(UPPER) $=\left(2.62 \times 10^{-5}\right)$ CDELAY $^{-1}$

For the CS8141 the lower limit is determined by the equations in (a) above.
The capacitor CDELAY also determines the frequency of the $\overline{\mathrm{RESET}}$ signal and the POWER-ON- $\overline{\mathrm{RESET}}$ (POR) delay period.

## RESET Function

The RESET function is activated when the Watchdog signal is outside of its preset window (Figure 16), when the regulator is in its power up state (Figure 17) or when $\mathrm{V}_{\text {OUT }}$ drops below $\mathrm{V}_{\text {OUT }}-4.5 \%$ for more than $2.0 \mu \mathrm{~s}$ (Figure 18)
If the Watchdog signal falls outside of the preset voltage and frequency window, a frequency programmable pulse train is generated at the RESET lead (Figure 16) until the correct Watchdog input signal reappears at the lead. The duration of the RESET pulse is determined by CDELAY according to the following equation:

$$
\operatorname{tWDI}(\overline{\mathrm{RESET}})=\left(1.0 \times 10^{4}\right) \mathrm{CDELAY}
$$

## RESET CIRCUIT WAVEFORMS WITH DELAYS INDICATED

If an undervoltage condition exists, the voltage on the $\overline{\text { RESET }}$ lead goes low and the delay capacitor, C DELAY, is discharged. RESET remains low until output is in regulation, the voltage on CDELAY exceeds the upper switching threshold and the Watchdog input signal is within its set window limits (Figures 17 and 18). The delay after the output is in regulation is:

$$
\operatorname{tPOR}(\operatorname{typ})=\left(4.75 \times 10^{5}\right) \text { CDELAY }
$$

The $\overline{\text { RESET }}$ delay circuit is also programmed with the external cap C DELAY.
The output of the reset circuit is an open collector NPN. $\overline{\mathrm{RESET}}$ is operational down to $\mathrm{V}_{\text {OUT }}=1.0 \mathrm{~V}$. Both $\overline{\mathrm{RESET}}$ and its delay are governed by comparators with hysteresis to avoid undesirable oscillations.
$V_{\text {Out }}$ When Watchdog is Held High and ENABLE $=$ HIGH
$V_{\text {Out }}$ When Watchdog is Held Low and ENABLE = HIGH






Figure 16. Timing Diagrams for Watchdog and ENABLE Functions


Figure 17. Power RESET and Power Down


Figure 18. Undervoltage Triggered RESET

## APPLICATION NOTES

## CS8140 DESIGN EXAMPLE

The CS8140 with its unique integration of linear regulator and control features: RESET, ENABLE and WATCHDOG, provides a single IC solution for a microprocessor power supply. The reset delay, reset duration and watchdog frequency limits are all determined by a single capacitor. For a particular microprocessor the overriding requirement is usually the reset delay (also known as power on reset). The capacitor is chosen to meet this requirement and the reset duration and watchdog frequency follow.

The reset delay is given by:

$$
\operatorname{tPOR}(\operatorname{typ})=(4.75 \times 105) \text { CDELAY }
$$

Assume that the reset delay must be 200 ms minimum.
From the CS8140 data sheet the reset delay has a $\pm 37 \%$ tolerance due to the regulator.

Assume the capacitor tolerance is $\pm 10 \%$.

$$
\begin{aligned}
\operatorname{tPOR}(\mathrm{min})= & \left(4.75 \times 10^{5} \times 0.63\right) \times \operatorname{CDELAY} \times 0.9 \\
& \operatorname{CDELAY}(\mathrm{~min})=\frac{\mathrm{tPOR}(\mathrm{~min})}{2.69 \times 105} \\
& \operatorname{CDELAY}^{(\mathrm{min})}=0.743 \mu \mathrm{~F}
\end{aligned}
$$

Closest standard value is $0.82 \mu \mathrm{~F}$.
Minimum and maximum delays using $0.82 \mu \mathrm{~F}$ are 220 ms and 586 ms .

The duration of the reset pulse is given by:

$$
\text { TWDI( } \overline{\text { RESET }})(\text { typ })=\left(1.0 \times 10^{4}\right) \times \text { CDELAY }
$$

This has a tolerance of $\pm 50 \%$ due to the IC, and $\pm 10 \%$ due to the capacitor.

The duration of the reset pulse ranges from 3.69 ms to 13.5 ms .

The watchdog signal can be expressed as a frequency or time. From a programmers point of view, time is more useful since they must ensure that a watchdog signal is issued consistently several times per second.

The maximum and minimum watchdog times are given by:

$$
\begin{aligned}
& \operatorname{tWDI(LOWER)}=\left(1.3 \times 10^{5}\right) \text { CDELAY } \\
& \mathrm{tWDI}(\text { UPPER })=\left(3.82 \times 10^{4}\right) \text { CDELAY }
\end{aligned}
$$

There is a tolerance of $\pm 20 \%$ due to the CS8140. With a capacitor tolerance of $\pm 10 \%$ :

$$
\begin{gathered}
\text { tWDI(LOWER) }=\left(1.3 \times 10^{5}\right) \times 1.2 \times 1.1 \times \text { CDelay } \\
\text { tWDI(UPPER) }=\left(3.82 \times 10^{4}\right) \times 0.8 \times 0.9 \times \text { CDelay } \\
\text { tWDI }(\text { LOWER })=141 \mathrm{~ms}(\mathrm{max}) \\
\text { tWDI }(\mathrm{UPPER})=22.5 \mathrm{~ms}(\mathrm{max}) \\
\text { tWDI }(\mathrm{LOWER})=\left(1.3 \times 10^{5}\right) \times 0.8 \times 0.9 \times \text { CDELAY } \\
\text { tWDI }(\text { UPPER })=\left(3.82 \times 10^{4}\right) \times 1.2 \times 1.1 \times \text { CDELAY } \\
\text { tWDI }(\text { LOWER })=76 \mathrm{~ms}(\mathrm{~min}) \\
\text { tWDI }(\text { UPPER })=41 \mathrm{~ms}(\mathrm{~min})
\end{gathered}
$$

The software must be written so that a watchdog signal arrives at least every 76 ms but not faster than every 41 ms (Figure 19).


Figure 19. WDI Signal for $C_{\text {Delay }}=0.82 \mu \mathrm{~F}$ using CS8140
The CS8141 is identical to the CS8140 except that the CS8141 only has a lower watchdog frequency threshold. The designer using this part need only be concerned with $t_{\text {WDI(LOWER) }}$ as shown in Figure 20.


Figure 20. WDI Signal for $C_{\text {Delay }}=0.82 \mu \mathrm{~F}$ using CS8141

## ENERGY CONSERVATION AND SMART FEATURES

Energy conservation is another benefit of using a regulator with integrated microprocessor control features. Using the CS8140 or CS8141 as indicated in Figure 21, the microprocessor can control its own power down sequence. The momentary contact switch quickly charges C1 through R1.

When the voltage across C 1 reaches 3.95 V ( the enable threshold), the output switches on and $\mathrm{V}_{\text {OUT }}$ rises to 5.0 V . After a delay period determined by $\mathrm{C}_{\text {Delay }}$, a frequency programmable reset pulse train is generated at the reset output. The pulse train continues until the correct watchdog signal appears at the WDI lead. C1 is now left to discharge through the input impedance of the enable lead (approximately $150 \mathrm{k} \Omega$ ) and the enable signal disappears. The output voltage remains at 5.0 V as long as the CS8140 continues to receive the correct watchdog signal.
The microprocessor can power itself down by terminating its watchdog signal. When the microprocessor finishes its housekeeping or power down software routine, it stops sending a watchdog signal. In response, the regulator generates a reset signal and goes into a sleep mode where $\mathrm{V}_{\text {OUT }}$ drops to 0 V , shutting down the microprocessor.


Figure 21. Application Diagram for CS8140. The CS8140 Provides a 5.0 V Tightly Regulated Supply and Control Function to the Microprocessor. In this Application, the Microprocessor Controls its own Power Down Sequence (see text).

${ }^{* *} \mathrm{C} 2$ is required for stability.
${ }^{* * *} \mathrm{R} \leq 80 \mathrm{k} \Omega$.
Figure 22. Application Diagram

## STABILITY CONSIDERATIONS

The output or compensation capacitor $\mathrm{C}_{2}$ in Figure 22 helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor $\mathrm{C}_{2}$ shown in Figure 22 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for $\mathrm{C}_{2}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.
Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Increase the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.
Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 23) is:
$\mathrm{P}_{\mathrm{D}(\text { max })}=\left\{\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{V}_{\mathrm{OUT}(\min )}\right)_{\mathrm{IOUT}(\max )}+\mathrm{V}_{\mathrm{IN}(\max )} \mathrm{I}_{\mathrm{Q}}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
$\mathrm{I}_{\text {OUT(max) }}$ is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).


Figure 23. Single Output Regulator With Key Performance Parameters Labeled

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\text {©JA's }}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## CS8140, CS8141

## MARKING DIAGRAMS



DEVICE ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8140YT7 | TO-220 Seven Lead, Straight | 50 Units/Rail |
| CS8140YTVA7 | TO-220 Seven Lead, Vertical | 50 Units/Rail |
| CS8140YTHA7 | TO-220 Seven Lead, Horizontal | 50 Units/Rail |
| CS8140YDPS7 | D$^{2}$ PAK, 7-Pin | 50 Units/Rail |
| CS8140YDPSR7 | D$^{2}$ PAK, 7-PIN | 750 Tape \& Reel |
| CS8140YDW24 | SO-24L | 31 Units/Rail |
| CS8140YDWR24 | SO-24L | 1000 Tape \& Reel |
| CS8140YN14 | DIP-14 | 25 Units/Rail |
| CS8141YT7 | TO-220 Seven Lead, Straight | 50 Units/Rail |
| CS8141YTVA7 | TO-220 Seven Lead, Vertical | 50 Units/Rail |
| CS8141YTHA7 | TO-220 Seven Lead, Horizontal | 50 Units/Rail |
| CS8141YDPS7 | D2PAK, 7-Pin | 50 Units/Rail |
| CS8141YDPSR7 | D2PAK, 7-PIN | 750 Tape \& Reel |
| CS8141YDW24 | SO-24L | 31 Units/Rail |
| CS8141YDWR24 | SO-24L | 1000 Tape \& Reel |
| CS8141YN14 | DIP-14 | 25 Units/Rail |

## Micropower Voltage Regulator

The MC78BC00 voltage regulators are specifically designed to be used with an external power transistor to deliver high current with high voltage accuracy and low quiescent current.

The MC78BC00 series are devices suitable for constructing regulators with ultra-low dropout voltage and output current in the range of several tens of mA to hundreds of mA . These devices have a chip enable function, which minimizes the standby mode current drain. Each of these devices contains a voltage reference unit, an error amplifier, a driver transistor and feedback resistors. These devices are available in the SOT-23, 5 pin surface mount packages.

These devices are ideally suited for battery powered equipment, and power sources for hand-held audio instruments, communication equipment and domestic appliances.

## MC78BC00 Series Features:

- Ultra-Low Supply Current ( $50 \mu \mathrm{~A}$ )
- Standby Mode ( $0.2 \mu \mathrm{~A}$ )
- Ultra-Low Dropout Voltage ( 0.1 V with External Transistor and $\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ )
- Excellent Line Regulation (Typically 0.1\%/V)
- High Accuracy Output Voltage ( $\pm 2.5 \%$ )

ORDERING INFORMATION

| Device | Output <br> Voltage | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: | :---: |
| MC78BC30NTR | 3.0 |  |  |
| MC78BC33NTR | 3.3 | $\mathrm{~T}_{\mathrm{A}}=-30^{\circ}$ to $+80^{\circ} \mathrm{C}$ | SOT-23 |
| MC78BC40NTR | 4.0 |  |  |
| MC78BC50NTR | 5.0 |  |  |

Other voltages from 2.0 to 6.0 V , in 0.1 V increments, are available. Consult factory for information.

Representative Block Diagram


This device contains 13 active transistors.

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 10 | Vdc |
| Power Dissipation and Thermal Characteristics |  |  |  |
| Maximum Power Dissipation |  | mW |  |
| Case 1212 (SOT-23) H Suffix |  |  |  |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{P}_{\mathrm{D}}$ | 150 | ${ }^{\circ}$ |
| Operating Junction Temperature | $\mathrm{R}_{\text {日JA }}$ | 333 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{J}}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -30 to +80 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O}}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right.$ [Note 1], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage MC78BC30NTR MC78BC33NTR MC78BC40NTR MC78BC50NTR | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 2.925 \\ & 3.218 \\ & 3.900 \\ & 4.875 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.3 \\ & 4.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.075 \\ & 3.382 \\ & 4.100 \\ & 5.125 \end{aligned}$ | V |
| Line Regulation $\mathrm{V}_{\mathrm{O}}+0.5 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 8.0 \mathrm{~V}$ | Regline | 0 | 0.1 | 0.3 | mV |
| Load Regulation $\begin{aligned} & \mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}=1.0 \mathrm{~V} \\ & 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{O}} \leq 100 \mathrm{~mA} \end{aligned}$ | Regload | - | 40 | 60 | mV |
| Output Current (Note 2) $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}=1.0 \mathrm{~V}$ | 10 | - | 1000 | - | mA |
| Dropout Voltage $\mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - | 100 | 200 | mV |
| Supply Current $\begin{aligned} & V_{\text {in }}=8.0 \mathrm{~V} \\ & \mathrm{~V}_{\text {in }}-V_{O}=1.0 \mathrm{~V} \\ & I_{0}=0 \text { (at no load) } \end{aligned}$ | $\mathrm{I}_{\text {ss }}$ | - | 50 | 80 | $\mu \mathrm{A}$ |
| Supply Current (Standby) $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$ | $1_{\text {standby }}$ | 0.1 | 0.2 | 1.0 | $\mu \mathrm{A}$ |
| Ext Leakage Current | lıK | - | - | 0.5 | $\mu \mathrm{A}$ |
| Chip Enable Input Logic Voltage Logic "0" (Regulator "On") Logic "1" (Regulator "Off") | $\mathrm{V}_{\text {CE }}$ | $\begin{gathered} 0 \\ 1.5 \\ \hline \end{gathered}$ | - | $\begin{gathered} 0.25 \\ 8.0 \\ \hline \end{gathered}$ | V |
| Chip Enable Input Current $\begin{aligned} & \mathrm{V}_{\mathrm{CE}}=0.25 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CE}}=1.5 \mathrm{~V} \end{aligned}$ | $\mathrm{I}_{\text {CEL }}$ | $-5.0$ | $-3.0$ | $\begin{gathered} -0.1 \\ 0.1 \end{gathered}$ | $\mu \mathrm{A}$ |
| Output Voltage Temperature Coefficient | $\mathrm{T}_{\mathrm{C}}$ | - | $\pm 100$ | - | ppm/ ${ }^{\circ} \mathrm{C}$ |

NOTES: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. The output current depends upon the performance of External PNP Transistor. Use External PNP Transistor of a low saturation type, with an $\mathrm{H}_{\mathrm{FE}}$ of 100 or more.

## MC78BC00 Series

## DEFINITIONS

Dropout Voltage - The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.
Line Regulation - The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques
such that average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Maximum Power Dissipation - The maximum total device dissipation for which the regulator will operate within specifications.
Supply Current - Current which is used to operate the regulator chip and is not delivered to the load.


Figure 1. Output Voltage versus Input Voltage


Figure 2. Output Voltage versus Output Current


Figure 3. Dropout Voltage versus Output Current


Figure 4. Ripple Rejection as a Function of Frequency

## MC78BC00 Series



Figure 5. Output Voltage versus Temperature


Figure 6. Supply Current versus Temperature


Figure 7. Line Transient Response


Figure 8. Load Transient Response

## MC78BC00 Series

## APPLICATIONS INFORMATION

## Introduction

The MC78BC00 series of micropower voltage regulators are specifically designed for ultra-low dropout voltage and an output current which ranges from several tens of mA to several hundreds of mA making them ideal for battery-powered equipment. These regulators also have a chip enable function which minimizes supply current in stand-by mode. An input bypass capacitor is recommended if the regulator is located an appreciable distance ( $\geq 4$ inches) from the input voltage source. These regulators require a $10 \mu \mathrm{~F}$ capacitance between the output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or other appropriate capacitors are recommended for
operation below $25^{\circ} \mathrm{C}$. The bypass capacitors should be mounted with the shortest possible leads or track lengths directly across the regulator input and output terminals.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around $-30^{\circ} \mathrm{C}$, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ are readily available. Solid tantalum capacitors may be the better choice if small size is a requirement. However, a maximum ESR limit of $3.0 \Omega$ must be observed over temperature to maintain stability.


Figure 9. Typical Operation

## MC78BC00 Series

## External PNP Transistor

The external pin of this IC is protected by a current limit circuit from the destruction caused by excess current. The R2 resistor shown in Figure 10 is used for the protection of
the external transistor, although this circuit can operate without the resistor. Resistor R2 should be determined via the input voltage, output voltage, output current, temperature and the $\mathrm{H}_{\mathrm{FE}}$ of the external pass transistor.


Figure 10. External PNP


Figure 11. Typical Application

## CS403

### 5.0 V, 750 mA Linear Regulator with RESET

The CS403 is a linear regulator specially designed as a post regulator. The CS403 provides low noise, low drift, and high accuracy to improve the performance of a switching power supply. It is ideal for applications requiring a highly efficient and accurate linear regulator. The active RESET makes the device particularly well suited to supply microprocessor based systems. The PNP-NPN output stage assures a low dropout voltage without requiring excessive supply current. Its features include low dropout ( 1.0 V typically) and low supply drain ( 4.0 mA typical with $\mathrm{I}_{\mathrm{OUT}}=500 \mathrm{~mA}$ ).

The CS403 design optimizes supply rejection by switching the internal reference from the supply input to the regulator output as soon as the nominal output voltage is reached.

## Features

- 5.0 V $\pm 3.0 \%$ Output Voltage
- Low Drift
- High Efficiency
- Short Circuit Protection
- Active Delayed Reset
- Noise Immunity on Reset
- 750 mA Output Current


Figure 1. Block Diagram

## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com

TO-220 FIVE LEAD T SUFFIX CASE 314D
TO-220 FIVE LEAD TVA SUFFIX CASE 314K

## PIN CONNECTIONS AND MARKING DIAGRAM



| A | $=$ Assembly Location |
| :--- | :--- |
| WL, L | $=$ Wafer Lot |
| YY, Y | $=$ Year |
| WW, W | $=$ Work Week |

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS403GT5 | TO-220* <br> STRAIGHT | 50 Units/Rail |
| CS403GTVA5 | TO-220* <br> VERTICAL | 50 Units/Rail |
| CS403GTHA5 | TO-220* <br> HORIZONTAL | 50 Units/Rail |

*Five lead.

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Forward Input Voltage | Unit |  |
| Operating Junction Temperature, $T_{J}$ |  | 18 |
| Storage Temperature Range, $T_{S}$ | Wave Solder: (through hole styles only) (Note 1 ) | $\mathrm{V}^{260 ~ p e a k ~}$ |
| Lead Temperature Soldering: | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $-40^{\circ} \mathrm{C} \leq T_{\mathrm{C}} \leq 125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq T_{J} \leq 150^{\circ} \mathrm{C}$,
$7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 10 \mathrm{~V}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage, V ${ }_{\text {OUT }}$ | $\begin{aligned} & \mathrm{V}_{\text {IN }}=8.5 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=250 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & 100 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 750 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.95 \\ & 4.85 \end{aligned}$ | $\begin{aligned} & 5.00 \\ & 5.00 \end{aligned}$ | $\begin{aligned} & 5.05 \\ & 5.15 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Operating Input Voltage | 100 to 750 mA | -0.75 | - | 18.0 | V |
| Load Regulation | $100 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 750 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=8.5 \mathrm{~V}$ | - | 30 | 100 | mV |
| Dropout Voltage | lout $=750 \mathrm{~mA}$ | - | 1.4 | 1.8 | V |
| Quiescent Current | $\begin{aligned} & \text { lout }=0 \mathrm{~mA} \\ & \text { lout }=750 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 4.0 \\ & 25 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| PSRR | $\begin{aligned} & \text { IOUT }-250 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz} \\ & \mathrm{C}_{\text {OUT }}=10 \mu \mathrm{~F}, \mathrm{~V}_{\mathrm{IN}}=8.5 \mathrm{~V}+\mathrm{V}_{\mathrm{pp}} \end{aligned}$ | - | 70 | - | dB |
| Output Short Circuit Current | - | - | 1.0 | - | A |
| Reset Output Voltage | $\mathrm{I}_{\mathrm{R}}=1.6 \mathrm{~mA}, 1.0 \leq \mathrm{V}_{\text {OUT }} \leq 4.75 \mathrm{~V}$ | - | 0.08 | 0.40 | V |
| Reset Output Leakage Current | $\mathrm{V}_{\text {OUT }}$ in regulation | - | 0 | 50 | $\mu \mathrm{A}$ |
| Delay Time for Reset Output | $\mathrm{C}_{\mathrm{d}}=100 \mathrm{nF}$ | 10 | 20 | 30 | ms |
| Reset Threshold, $\mathrm{V}_{\text {RTH }}$ | $\mathrm{V}_{\text {OUT }}$ Increasing | - | - | $\mathrm{V}_{\text {OUT }}-0.04$ | V |
| Reset Threshold, $\mathrm{V}_{\text {RTL }}$ | $V_{\text {OUT }}$ Decreasing | 4.75 | - | - | V |
| Threshold Hysteresis | - | 10 | 50 | - | mV |
| Delay, V ${ }_{\text {DTC }}$ | Charge | 3.7 | 4.0 | 4.4 | V |
| Delay, V ${ }_{\text {DTD }}$ | Discharge | 3.1 | 3.5 | 3.9 | V |
| Delay Hysteresis, $\mathrm{V}_{\mathrm{DH}}$ | - | 200 | 500 | 1000 | mV |
| Reset Delay Capacitor Charging Current, $\mathrm{I}_{\mathrm{CH}}$ | - | 10 | 20 | 40 | $\mu \mathrm{A}$ |
| Reset Delay Capacitor Discharge Voltage, VDIS | - | - | 0.6 | 1.2 | V |

## PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :--- |
| $\mathbf{5}$ Lead TO-220 | LEAD SYMBOL |  |
| 1 | VIN | Input voltage. |
| 2 | RESET | CMOS compatible output lead. RESET goes low whenever V <br> out of regulation. falls |
| 3 | GND | Ground connection. |
| 4 | Delay | Timing capacitor for $\overline{\text { RESET function. }}$ |
| 5 | V OUT | Regulated output voltage, 5.0 V (typ). |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Output Voltage vs. $\mathrm{V}_{\mathrm{IN}}, \mathrm{I}_{\mathrm{Q}}$


Figure 3. Output Voltage vs. Junction Temperature


Figure 4. Dropout Voltage vs. Output
Current Over Temperature
RESET CIRCUIT


Figure 5. Reset Circuit Waveform

## CIRCUIT DESCRIPTION

The CS403 $\overline{\text { RESET }}$ function is very precise, has hysteresis on both the $\overline{\text { RESET }}$ and Delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V .

The $\overline{\text { RESET }}$ circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text { RESET }}$ output NPN transistor is controlled by the two circuits described (see Figure 1).

## Low Voltage Inhibit Circuit

This circuit monitors output voltage, and when output voltage is below the specified minimum, causes the $\overline{\text { RESET }}$ output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the RESET output transistor to go into the OFF state if allowed by the reset Delay circuit.

## Reset Delay Circuit

This circuit provides a programmable (external capacitor) delay on the $\overline{\text { RESET }}$ output lead. The Delay lead provides source current to the external delay capacitor only when the

Low Voltage Inhibit circuit indicates that output voltage is above $\mathrm{V}_{\mathrm{RT}(\mathrm{ON})}$. Otherwise, the Delay lead sinks current to ground (used to discharge the Delay capacitor). The discharge current is latched ON when the output voltage is below $\mathrm{V}_{\mathrm{RT}(\mathrm{OFF})}$, or when the voltage on the Delay capacitor is above $\mathrm{V}_{\text {DIS }}$. In other words, the Delay capacitor is fully discharged any time the output voltage falls out of regulation, even for a short period of time. This feature ensures a controlled RESET pulse is generated following detection of an error condition. The circuit allows the $\overline{\text { RESET }}$ output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $\mathrm{V}_{\text {DIS }}$.

$$
\mathrm{t}_{\mathrm{d}}=\mathrm{C}_{\mathrm{d}} \times \mathrm{V}_{\mathrm{DTC}} / \mathrm{I}_{\mathrm{CH}}=\text { CDelay } \times 2.105 \text { (typical). }
$$

where:
$\mathrm{t}_{\mathrm{d}}=$ Time delay.
$C_{d}=$ Value of external charging capacitor (see Figure 6).
$\mathrm{V}_{\mathrm{DTC}}=$ Delay Threshold charge.
$\mathrm{I}_{\mathrm{ch}}=$ Reset delay capacitor charging current.

$\mathrm{C}_{1}{ }^{*}$ is required if the regulator is far from the power source filter. $\mathrm{C}_{2}{ }^{* *}$ is required for stability.

Figure 6. Test Circuit

## APPLICATION NOTES

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor Cout shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for COUT for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.
Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the
higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.
Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.
Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.
Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.
Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 7) is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
$I_{\text {OUT(max) }}$ is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \text { JA }}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\text {©JA }}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 7. Single Output Regulator With Key Performance Parameters Labeled

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta J A}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JJC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like
$R_{\Theta J A}$, it is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## CS403

PACKAGE THERMAL DATA

| Parameter |  | TO-220 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 4.1 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8122

## 2.0\% 5.0 V, 750 mA Low Dropout Linear Regulator with Delayed RESET

The CS8122 is a precision 5.0 V linear regulator capable of sourcing in excess of 750 mA . The $\overline{\mathrm{RESET}}$ 's delay time is externally programmed using a discrete RC network. During power up, or when the output goes out of regulation, the RESET lead remains in the low state for the duration of the delay. This function is independent of the input voltage and will function correctly as long as the output voltage remains at or above 1.0 V . Hysteresis is included in the Delay and the RESET comparators to improve noise immunity. A latching discharge circuit is used to discharge the delay capacitor when it is triggered by a brief fault condition.

The regulator is protected against a variety of fault conditions: i.e. reverse battery, overvoltage, short circuit and thermal runaway conditions. The regulator is protected against voltage transients ranging from -50 V to +40 V . Short circuit current is limited to 1.2 A (typ).

The CS8122 is an improved replacement for the CS8126 and features a tighter tolerance on its output voltage ( $2.0 \%$ vs. $4.0 \%$ ).

The CS8122 is packaged in a 5 lead TO-220 with copper tab. The copper tab can be connected to a heat sink if necessary.

## Features

- 5.0 V $\pm 2.0 \%$ Regulated Output
- Low Dropout Voltage ( 0.6 V @ 0.5 A )
- 750 mA Output Current Capability
- Externally Programmed $\overline{\text { RESET }}$ Delay
- Fault Protection
- Reverse Battery
- 60 V Load Dump
- -50 V Reverse Transient
- Short Circuit
- Thermal Shutdown

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TO-220
FIVE LEAD T SUFFIX CASE 314D
TO-220
FIVE LEAD TVA SUFFIX CASE 314K

TO-220
FIVE LEAD THA SUFFIX
CASE 314A

PIN CONNECTIONS AND
MARKING INDIAGRAM


A = Assembly Location
WL, $\mathrm{L}=$ Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS8122YT5 | TO-220* <br> STRAIGHT | 50 Units/Rail |
| CS8122YTVA5 | TO-220* <br> VERTICAL | 50 Units/Rail |
| CS8122YTHA5 | TO-220* <br> HORIZONTAL | 50 Units/Rail |

*Five lead.


Figure 1. Block Diagram
ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Operating Range |  | -0.5 to 26 | V |
| Power Dissipation |  | Internally Limited | - |
| Peak Transient Voltage (46 V Load Dump @ V ${ }_{\text {IN }}=14 \mathrm{~V}$ ) |  | -50, 60 | V |
| Output Current |  | Internally Limited | - |
| Electrostatic Discharge (Human Body Model) |  | 4.0 | kV |
| Junction Temperature |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) | 260 peak | ${ }^{\circ} \mathrm{C}$ |

[^11]*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C},-40 \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 6.0 \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 500 \mathrm{~mA}\right.$,
$\mathrm{R}_{\mathrm{RESET}}=4.7 \mathrm{k} \Omega$ to $\mathrm{V}_{\mathrm{CC}}$ unless otherwise noted.) Note 2

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Output Stage (Vout)

| Output Voltage | - | 4.9 | 5.0 | 5.1 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\mathrm{l}_{\text {OUT }}=500 \mathrm{~mA}$ | - | 0.35 | 0.60 | V |
| Supply Current | lout $\leq 10 \mathrm{~mA}$ lout $\leq 100 \mathrm{~mA}$ ${ }^{\text {OUT }} \leq 500 \mathrm{~mA}$ | - | $\begin{aligned} & 2.0 \\ & 6.0 \\ & 55 \end{aligned}$ | $\begin{gathered} 7.0 \\ 12 \\ 100 \end{gathered}$ | mA <br> mA <br> mA |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=50 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Load Regulation | $50 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 500 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 10 | 50 | mV |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, 7.0 \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$, $\mathrm{l}_{\text {OUT }}=250 \mathrm{~mA}$ | 54 | 75 | - | dB |
| Current Limit | - | 0.75 | 1.20 | - | A |
| Overvoltage Shutdown | - | 32 | - | 40 | V |
| Maximum Line Transient | $\mathrm{V}_{\text {OUT }} \leq 5.5 \mathrm{~V}$ | 60 | 95 | - | V |
| Reverse Polarity Input Voltage DC | $\mathrm{V}_{\text {OUT }} \geq-0.6 \mathrm{~V}, 10 \Omega$ Load | -15 | -30 | - | V |
| Reverse Polarity Input Voltage Transient | 1.0\% Duty Cycle, T < $100 \mathrm{~ms}, 10 \Omega$ Load | -50 | -80 | - | V |
| Thermal Shutdown | Guaranteed by Design | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |

RESET and Delay Functions

| Delay Charge Current | $\mathrm{V}_{\text {DELAY }}=2.0 \mathrm{~V}$ | 5.0 | 10 | 15 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESET Threshold | $\mathrm{V}_{\text {OUT }}$ Increasing, $\mathrm{V}_{\mathrm{RT} \text { (ON) }}$ <br> $\mathrm{V}_{\text {OUT }}$ Decreasing, $\mathrm{V}_{\text {RT(OFF) }}$ | $\begin{aligned} & 4.65 \\ & 4.50 \end{aligned}$ | $\begin{aligned} & 4.90 \\ & 4.70 \end{aligned}$ | $\begin{aligned} & V_{\text {OUT }}-0.01 \\ & \text { V OUT }-0.16 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| RESET Hysteresis | $\mathrm{V}_{\mathrm{RH}}=\mathrm{V}_{\mathrm{RT} \text { (ON) }}-\mathrm{V}_{\mathrm{RT} \text { (OFF) }}$ | 150 | 200 | 250 | mV |
| Delay Threshold | Charge, $\mathrm{V}_{\mathrm{DC}(\mathrm{HI})}$ Discharge, $\mathrm{V}_{\mathrm{DC}(\mathrm{L})}$ | $\begin{aligned} & 3.25 \\ & 2.85 \end{aligned}$ | $\begin{aligned} & 3.50 \\ & 3.10 \end{aligned}$ | $\begin{aligned} & 3.75 \\ & 3.35 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Delay Hysteresis | - | 200 | 400 | 800 | mV |
| RESET Output Voltage Low | $1.0 \mathrm{~V}<\mathrm{V}_{\text {OUT }}<\mathrm{V}_{\mathrm{RT}(\mathrm{L})}, 3.0 \mathrm{k} \Omega$ to $\mathrm{V}_{\text {OUT }}$ | - | 0.1 | 0.4 | V |
| RESET Output Leakage | $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RT(H) }}$ | 0 | - | 10 | $\mu \mathrm{A}$ |
| Delay Capacitor Discharge Voltage | Discharge Latched "ON", $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RT }}$ | - | 0.2 | 0.5 | V |
| Delay Time | $\mathrm{C}_{\text {DELAY }}=0.1 \mu \mathrm{~F}$ | 16 | 32 | 48 | ms |

2. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.

DelayTime $=\frac{C_{\text {Delay }} \times V_{\text {Delay Threshold Charge }}}{\text { ICharge }}=$ CDelay $\times 3$

## PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :---: |
| $\begin{aligned} & \text { TO-220 } \\ & 5 \text { LEAD } \end{aligned}$ | LEAD SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{IN}}$ | Unregulated supply voltage to IC. |
| 2 | $\mathrm{V}_{\text {OUT }}$ | Regulated 5.0 V output. |
| 3 | GND | Ground Connection. |
| 4 | Delay | Timing capacitor for RESET function. |
| 5 | RESET | CMOS/TTL compatible output lead. RESET goes low whenever $\mathrm{V}_{\text {OUT }}$ drops below $6.0 \%$ of it's regulated value. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Quiescent Current vs. Input Voltage Over Temperature


Figure 4. Output Voltage vs. Input Voltage Over Temperature


Figure 3. Quiescent Current vs. Input Voltage Over Load Resistance


Figure 5. V ${ }_{\text {Out }}$ vs. $\mathrm{V}_{\text {IN }}$ Over R $\mathrm{R}_{\text {Load }}$

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 6. Line Regulation vs. Output Current


Figure 8. Dropout Voltage vs. Output Current


Figure 10. Ripple Rejection


Figure 7. Load Regulation vs. Output Current


Figure 9. Quiescent Current vs. Output Current


Figure 11. Output Capacitor ESR


Figure 12. RESET Circuit Waveform

## CIRCUIT DESCRIPTION

The CS8122 $\overline{\text { RESET }}$ function, has hysteresis on both the reset and delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V .

The RESET circuit output is an open collector type with ON and OFF parameters as specified. The RESET output NPN transistor is controlled by the two circuits described (see Block Diagram on page 588).

## Low Voltage Inhibit Circuit

The Low Voltage Inhibit Circuit monitors output voltage, and when output voltage is below the specified minimum, causes the $\overline{\text { RESET }}$ output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the $\overline{\text { RESET }}$ output transistor to go into the OFF state if allowed by the $\overline{\mathrm{RESET}}$ Delay circuit.

## Reset Delay Circuit

The Reset Delay Circuit provides a programmable (by external capacitor) delay on the $\overline{\text { RESET }}$ output lead. The Delay lead provides source current to the external delay capacitor only when the Low Voltage Inhibit circuit indicates that output voltage is above $\mathrm{V}_{\mathrm{RT}(\mathrm{ON})}$. Otherwise, the Delay lead sinks current to ground (used to discharge the
delay capacitor). The discharge current is latched ON when the output voltage is below $\mathrm{V}_{\mathrm{RT}(\mathrm{OFF})}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures that a controlled $\overline{\text { RESET }}$ pulse is generated following detection of an error condition. The circuit allows the RESET output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $\mathrm{V}_{\mathrm{DC}(\mathrm{HI})}$.

${ }^{*} \mathrm{C}_{I N}$ is required if regulator is far from the power source filter.
${ }^{* *} \mathrm{C}_{\text {OUT }}$ is required for stability.
Figure 13. Test Circuit

## APPLICATION NOTES

## STABILITY CONSIDERATIONS

The output or compensation capacitor, Cout, helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor Cout shown in Figure 13 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for COUT for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 14) is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
$\mathrm{I}_{\mathrm{OUT}(\max )}$ is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at

## IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta J A}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 14. Single Output Regulator With Key Performance Parameters Labeled

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta J A}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> FIVE LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $\mathrm{R}_{\Theta \mathrm{JJC}}$ | Typical | 2.1 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta \mathrm{JA}}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8126

### 5.0 V, 750 mA Low Dropout Linear Regulator with Delayed RESET

The CS8126 is a low dropout, high current 5.0 V linear regulator. It is an improved replacement for the CS8156. Improvements include higher accuracy, tighter saturation control, better supply rejection, and enhanced $\overline{\text { RESET }}$ circuitry. Familiar PNP regulator features such as reverse battery protection, overvoltage shutdown, thermal shutdown, and current limit make the CS8126 suitable for use in automotive and battery operated equipment. Additional on-chip filtering has been included to enhance rejection of high frequency transients on all external leads.

An active microprocessor $\overline{\text { RESET }}$ function is included on-chip with externally programmable delay time. During power-up, or after detection of any error in the regulated output, the RESET lead will remain in the low state for the duration of the delay. Types of errors include short circuit, low input voltage, overvoltage shutdown, thermal shutdown, or others that cause the output to become unregulated. This function is independent of the input voltage and will function correctly with an output voltage as low as 1.0 V . Hysteresis is included in both the reset and Delay comparators for enhanced noise immunity. A latching discharge circuit is used to discharge the Delay capacitor, even when triggered by a relatively short fault condition. This circuit improves upon the commonly used SCR structure by providing full capacitor discharge ( 0.2 V type).

Note: The CS8126 is lead compatible with the LM2927 and LM2926.

## Features

- Low Dropout Voltage ( 0.6 V at 0.5 A )
- 3.0\% Output Accuracy
- Active RESET
- External RESET Delay for Reset
- Protection Circuitry
- Reverse Battery Protection
- +60 V, -50 V Peak Transient Voltage
- Short Circuit Protection
- Internal Thermal Overload Protection

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## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 603 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 603 of this data sheet.


Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Dissipation |  | Internally Limited | - |
| Peak Transient Voltage (46 V Load Dump) |  | -50, 60 | V |
| Output Current |  | Internally Limited | - |
| ESD Susceptibility (Human Body Model) |  | 4.0 | kV |
| Package Thermal Resistance, TO-220 5-Lead: <br> Junction-to-Case, R QJc <br> Junction-to-Ambient, R RJA |  | $\begin{gathered} 2.1 \\ 50 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, D2PAK, 7-Pin: <br> Junction-to-Case, R QJC <br> Junction-to-Ambient, R $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{gathered} 2.1 \\ 10-50^{\star *} \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2) | 260 peak <br> 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
**Depending on thermal properties of substrate. $R_{\theta J A}=R_{\theta J C}+R_{\theta C A}$.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $+125^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{J}}=-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=6.0$ to 26 V ,
$\mathrm{I}_{\mathrm{O}}=5.0$ to $500 \mathrm{~mA}, \mathrm{R}_{\text {RESET }}=4.7 \mathrm{k} \Omega$ to $\mathrm{V}_{\mathrm{CC}}$, unless otherwise noted.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage (V $\mathrm{V}_{\text {OUT }}$ ) |  |  |  |  |  |
| Output Voltage | - | 4.85 | 5.00 | 5.15 | V |
| Dropout Voltage | $\mathrm{l}_{\text {OUT1 }}=500 \mathrm{~mA}$ | - | 0.35 | 0.60 | V |
| Supply Current | $\begin{aligned} & \text { lout } \leq 10 \mathrm{~mA} \\ & \text { lout } \leq 100 \mathrm{~mA} \\ & \text { lout } \leq 500 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 6.0 \\ & 55 \end{aligned}$ | $\begin{gathered} 7.0 \\ 12 \\ 100 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Line Regulation | $\mathrm{V}_{\mathrm{IN}}=6.0$ to 26 V , $\mathrm{l}_{\mathrm{OUT}}=50 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Load Regulation | $\mathrm{I}_{\text {OUT }}=50$ to $500 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 10 | 50 | mV |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{~V}_{\text {IN }}=7.0$ to $17 \mathrm{~V}, \mathrm{l}_{\text {OUT }}=250 \mathrm{~mA}$ | 54 | 75 | - | dB |
| Current Limit | - | 0.75 | 1.20 | - | A |
| Overvoltage Shutdown | - | 32 | - | 40 | V |
| Maximum Line Transient | $\mathrm{V}_{\text {OUT }} \leq 5.5 \mathrm{~V}$ | - | 95 | - | V |
| Reverse Polarity Input Voltage DC | $\mathrm{V}_{\text {OUT }} \geq-0.6 \mathrm{~V}, 10 \Omega$ Load | -15 | -30 | - | V |
| Reverse Polarity Input Voltage Transient | 1.0\% Duty Cycle, $\mathrm{T}<100 \mathrm{~ms}, 10 \Omega$ Load | - | -80 | - | V |
| Thermal Shutdown | Note 3 | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |

3. Guaranteed By Design

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $+125^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{J}}=-40^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=6.0$ to 26 V ,
$\mathrm{I}_{\mathrm{O}}=5.0$ to $500 \mathrm{~mA}, \mathrm{R}_{\text {RESET }}=4.7 \mathrm{k} \Omega$ to $\mathrm{V}_{\mathrm{CC}}$, unless otherwise noted.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESET and Delay Functions |  |  |  |  |  |
| Delay Charge Current | $\mathrm{V}_{\text {Delay }}=2.0 \mathrm{~V}$ | 5.0 | 10 | 15 | $\mu \mathrm{A}$ |
| RESET Threshold | $\mathrm{V}_{\text {OUT }}$ Increasing, $\mathrm{V}_{\mathrm{RT}(\mathrm{ON})}$ $\mathrm{V}_{\text {OUT }}$ Decreasing, $\mathrm{V}_{\mathrm{RT}(\mathrm{OFF})}$ | $\begin{aligned} & 4.65 \\ & 4.50 \end{aligned}$ | $\begin{aligned} & 4.90 \\ & 4.70 \end{aligned}$ | $\begin{aligned} & V_{\text {OUT }}-0.01 \\ & V_{\text {OUT }}-0.15 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| RESET Hysteresis | $\mathrm{V}_{\mathrm{RH}}=\mathrm{V}_{\mathrm{RT} \text { (ON) }}-\mathrm{V}_{\mathrm{RT}(\mathrm{OFF})}$ | 150 | 200 | 250 | mV |
| Delay Threshold | Charge, $\mathrm{V}_{\mathrm{DC}(\mathrm{HI})}$ <br> Discharge, $\mathrm{V}_{\mathrm{DC}(\mathrm{LO})}$ | $\begin{aligned} & 3.25 \\ & 2.85 \end{aligned}$ | $\begin{aligned} & 3.50 \\ & 3.10 \end{aligned}$ | $\begin{aligned} & 3.75 \\ & 3.35 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Delay Hysteresis | - | 200 | 400 | 800 | mV |
| RESET Output Voltage Low | $1.0 \mathrm{~V}<\mathrm{V}_{\text {OUT }}<\mathrm{V}_{\text {RTL }}, 3.0 \mathrm{k} \Omega$ to $\mathrm{V}_{\text {OUT }}$ | - | 0.1 | 0.4 | V |
| RESET Output Leakage Current | $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RT(ON) }}$ | - | 0 | 10 | $\mu \mathrm{A}$ |
| Delay Capacitor Discharge Voltage | Discharge Latched "ON", $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RT }}$ | - | 0.2 | 0.5 | V |
| Delay Time | $\mathrm{C}_{\text {Delay }}=0.1 \mu \mathrm{~F}^{*}$. Note 4 | 16 | 32 | 48 | ms |

$*$ Delay Time $=\frac{\mathrm{C}_{\text {Delay }} \times \mathrm{V}_{\text {DelayThreshold Charge }}}{I_{\text {Charge }}}=\mathrm{C}_{\text {Delay }} \times 3.2$
4. Assumes Ideal Capacitor

PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  | FUNCTION |
| :---: | :---: | :---: | :---: |
| TO-220 <br> 5 LEAD | $\begin{aligned} & \text { D}^{2} \text { PAK } \\ & \text { 7-PIN } \end{aligned}$ | LEAD SYMBOL |  |
| 1 | 1 | $\mathrm{V}_{\text {IN }}$ | Unregulated supply voltage to IC. |
| 2 | 2 | $\mathrm{V}_{\text {OUT }}$ | Regulated 5.0 V output. |
| 3 | 4 | GND | Ground connection. |
| 4 | 5 | Delay | Timing capacitor for RESET function. |
| 5 | 6 | RESET | CMOS/TTL compatible output lead. RESET goes low after detection of any error in the regulated output or during power up. |
| - | 3 | $\mathrm{V}_{\text {OUT(SENSE) }}$ | Remote sensing of output voltage. |
| - | 7 | NC | No Connection. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. $I_{\text {CQ }}$ vs. $\mathrm{V}_{\text {IN }}$ Over Temperature


Figure 4. $\mathrm{V}_{\text {Out }}$ vs. $\mathrm{V}_{\text {IN }}$ Over Temperature


Figure 6. Line Regulation vs. Output Current Over Temperature

Room Temp.


Figure 3. $\mathrm{I}_{\mathrm{CQ}}$ vs. $\mathrm{V}_{\mathrm{IN}}$ Over $\mathrm{R}_{\text {LOAD }}$


Figure 5. $\mathrm{V}_{\text {Out }}$ vs. $\mathrm{V}_{\text {IN }}$ Over $\mathrm{R}_{\text {Load }}$


Figure 7. Load Regulation vs. Output Current Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)


Figure 8. Dropout Voltage vs. Output Current Over Temperature


Figure 10. Ripple Rejection


Figure 9. Quiescent Current vs. Output Current Over Temperature


Figure 11. Output Capacitor ESR

RESET CIRCUIT WAVEFORM


Figure 12. RESET Circuit Waveform

## CIRCUIT DESCRIPTION

The CS8126 $\overline{\text { RESET }}$ function, has hysteresis on both the Reset and Delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V .

The RESET circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text { RESET }}$ output NPN transistor is controlled by the two circuits described (see Block Diagram).

## Low Voltage Inhibit Circuit

This circuit monitors output voltage, and when the output voltage falls below $\mathrm{V}_{\mathrm{RT} \text { (OFF) }}$, causes the $\overline{\mathrm{RESET}}$ output transistor to be in the ON (saturation) state. When the output voltage rises above $\mathrm{V}_{\mathrm{RT}(\mathrm{ON})}$, this circuit permits the $\overline{\mathrm{RESET}}$ output transistor to go into the OFF state if allowed by the RESET Delay circuit.

## RESET Delay Circuit

This circuit provides a programmable (by external capacitor) delay on the $\overline{\text { RESET }}$ output lead. The Delay lead provides source current to the external delay capacitor only when the "Low Voltage Inhibit" circuit indicates that output
voltage is above $\mathrm{V}_{\mathrm{RT}(\mathrm{ON})}$. Otherwise, the Delay lead sinks current to ground (used to discharge the delay capacitor). The discharge current is latched ON when the output voltage falls below $\mathrm{V}_{\mathrm{RT}(\mathrm{OFF})}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures a controlled $\overline{\text { RESET }}$ pulse is generated following detection of an error condition. The circuit allows the $\overline{\text { RESET }}$ output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $\mathrm{V}_{\mathrm{DC}(\mathrm{H} 1)}$.
The Delay time for the $\overline{\text { RESET }}$ function is calculated from the formula:

$$
\begin{gathered}
\text { Delay time }=\frac{C_{\text {Delay }} \times V_{\text {Delay }} \text { Threshold }}{} \\
\text { ICharge } \\
\text { Delay time }=\text { CDelay } \times 3.2 \times 10^{5}
\end{gathered}
$$

If $C_{\text {Delay }}=0.1 \mu \mathrm{~F}$, Delay time $(\mathrm{ms})=32 \mathrm{~ms} \pm 50 \%$ : i.e. 16 ms to 48 ms . The tolerance of the capacitor must be taken into account to calculate the total variation in the delay time.

${ }^{*} \mathrm{C}_{1}$ is required if the regulator is far from the power source filter.
${ }^{* *} \mathrm{C}_{2}$ is required for stability.
Figure 13. Application Diagram

## APPLICATION NOTES

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low
temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.
The value for the output capacitor $\mathrm{C}_{2}$ shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for $\mathrm{C}_{2}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.
Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.
Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.
Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.
Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.
Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.
Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 14) is:

$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at $I_{\text {OUT (max) }}$.
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
R_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PDD}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\text {©JA }}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 14. Single Output Regulator With Key Performance Parameters Labeled

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JJC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it is a function of package type. $\mathrm{R}_{\Theta C S}$ and $\mathrm{R}_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.
where:

ORDERING INFORMATION

| Device | Description | Shipping |
| :--- | :---: | :---: |
| CS8126-1YT5 | TO-220 FIVE LEAD STRAIGHT | 50 Units/Rail |
| CS8126-1YTVA5 | TO-220 FIVE LEAD VERTICAL | 50 Units/Rail |
| CS8126-1YTHA5 | TO-220 FIVE LEAD HORIZONTAL | 50 Units/Rail |
| CS8126-1YTHE5 | TO-220 FIVE LEAD SURFACE MOUNT | 50 Units/Rail |
| CS8126-1YTHER5 | TO-220 FIVE LEAD SURFACE MOUNT | 750 Tape \& Reel |
| CS8126-1YDPS7 | D²PAK, 7-PIN $_{50 \text { Units/Rail }}$CS8126-1YDPSR7$\quad$ D2PAK, 7-PIN | 750 Tape \& Reel |

## MARKING DIAGRAMS



## CS8129

### 5.0 V, 750 mA Low Dropout Linear Regulator with Lower RESET Threshold

The CS8129 is a precision 5.0 V linear regulator capable of sourcing 750 mA . The $\overline{\mathrm{RESET}}$ threshold voltage has been lowered to 4.2 V so that the regulator can be used with 4.0 V microprocessors. The lower $\overline{\text { RESET }}$ threshold also permits operation under low battery conditions (5.5 V plus a diode). The RESET's delay time is externally programmed using a discrete RC network. During power up, or when the output goes out of regulation, $\overline{\text { RESET }}$ remains in the low state for the duration of the delay. This function is independent of the input voltage and will function correctly as long as the output voltage remains at or above 1.0 V . Hysteresis is included in the Delay and the $\overline{\text { RESET }}$ comparators to improve noise immunity. A latching discharge circuit is used to discharge the delay capacitor when it is triggered by a brief fault condition.

The regulator is protected against a variety of fault conditions: i.e. reverse battery, overvoltage, short circuit and thermal runaway conditions. The regulator is protected against voltage transients ranging from -50 V to +40 V . Short circuit current is limited to 1.2 A (typ).

The CS8129 is packaged in a 5 lead TO-220 and a 16 lead surface mount package.

## Features

- 5.0 V $\pm 3.0 \%$ Regulated Output
- Low Dropout Voltage ( 0.6 V @ 0.5 A )
- 750 mA Output Current Capability
- Reduced $\overline{\text { RESET }}$ Threshold for use with 4.0 V Microprocessors
- Externally Programmed RESET Delay
- Fault Protection
- Reverse Battery
- 60 V, -50 V Peak Transient Voltage
- Short Circuit
- Thermal Shutdown

ON Semiconductor ${ }^{\text {w }}$ http://onsemi.com


TO-220 FIVE LEAD T SUFFIX CASE 314D

TO-220 FIVE LEAD TVA SUFFIX CASE 314K


TO-220 FIVE LEAD THA SUFFIX CASE 314A


SO-16L DW SUFFIX CASE 751G

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8129YT5 | TO-220* <br> STRAIGHT | 50 Units/Rail |
| CS8129YTHA5 | TO-220* <br> VERTICAL | 50 Units/Rail |
| CS8129YTVA5 | TO-220* <br> HORIZONTAL | 50 Units/Rail |
| CS8129YDW16 | SO-16L | 46 Units/Rail |
| CS8129YDWR16 | SO-16L | 1000 Tape \& Reel |

*Five lead.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 611 of this data sheet.


PIN CONNECTIONS



Figure 1. Block Diagram
ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |  |
| :--- | :---: | :---: | :---: |
| Input Operating Range | -0.5 to 26 | V |  |
| Power Dissipation | Internally Limited | - |  |
| Peak Transient Voltage (46 V Load Dump @ $14 \mathrm{~V} \mathrm{~V}_{\text {IN }}$ ) | $-50,60$ | V |  |
| Output Current | Internally Limited | - |  |
| Electrostatic Discharge (Human Body Model) | 4.0 | kV |  |
| Junction Temperature | Wave Solder (through hole styles only) (Note 1) |  |  |
| Storage Temperature Range | Reflow (SMD styles only) (Note 2) | 260 peak <br> 230 <br> peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  |  |  |

1. 10 second maximum.
2. 60 seconds max above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C},-40 \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 6.0 \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 500 \mathrm{~mA}\right.$, $\mathrm{R}_{\mathrm{RESET}}=4.7 \mathrm{k} \Omega$ to $\mathrm{V}_{\text {OUT }}$ unless otherwise noted.) Note 3

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Output Stage (VOUT)

| Output Voltage | - | 4.85 | 5.0 | 5.15 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | IOUT $=500 \mathrm{~mA}$ | - | 0.35 | 0.60 | V |
| Supply Current | $\begin{aligned} & \text { lout }=10 \mathrm{~mA} \\ & \text { lout }=100 \mathrm{~mA} \\ & \text { lout }=500 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & \hline 2.0 \\ & 6.0 \\ & 55 \end{aligned}$ | $\begin{gathered} 7.0 \\ 12 \\ 100 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=50 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Load Regulation | $50 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 500 \mathrm{~mA}, \mathrm{~V}_{\mathrm{IN}}=14 \mathrm{~V}$ | - | 10 | 50 | mV |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{~V}_{\text {IN }}=7.0$ to 17 V , l $\mathrm{l}_{\text {OUT }}=250 \mathrm{~mA}$ | 54 | 75 | - | dB |
| Current Limit | - | 0.75 | 1.20 | - | A |
| Overvoltage Shutdown | - | 32 | - | 40 | V |
| Reverse Polarity Input Voltage DC | $\mathrm{V}_{\text {OUT }} \geq-0.6 \mathrm{~V}, 10 \Omega$ Load | -15 | -30 | - | V |
| Thermal Shutdown | Guaranteed by Design | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |

RESET and Delay Functions

| Delay Charge Current | $\mathrm{V}_{\text {DELAY }}=2.0 \mathrm{~V}$ | 5.0 | 10 | 15 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESET Threshold | $\mathrm{V}_{\text {OUT }}$ Increasing, $\mathrm{V}_{\mathrm{RT}(\mathrm{ON})}$ <br> $\mathrm{V}_{\text {OUT }}$ Decreasing, $\mathrm{V}_{\text {RT(OFF) }}$ | $\begin{aligned} & 4.05 \\ & 4.00 \end{aligned}$ | $\begin{aligned} & 4.35 \\ & 4.20 \end{aligned}$ | $\begin{aligned} & 4.50 \\ & 4.45 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| RESET Hysteresis | $\mathrm{V}_{\mathrm{RH}}=\mathrm{V}_{\mathrm{RT} \text { (ON) }}-\mathrm{V}_{\text {RT(OFF) }}$ | 50 | 150 | 250 | mV |
| Delay Threshold | Charge, $\mathrm{V}_{\mathrm{DC}(\mathrm{HI})}$ Discharge, $\mathrm{V}_{\mathrm{DC}(\mathrm{LO})}$ | $\begin{aligned} & 3.25 \\ & 2.85 \end{aligned}$ | $\begin{aligned} & 3.50 \\ & 3.10 \end{aligned}$ | $\begin{aligned} & 3.75 \\ & 3.35 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Delay Hysteresis | - | 200 | 400 | 800 | mV |
| RESET Output Voltage Low | $1.0 \mathrm{~V}<\mathrm{V}_{\text {OUT }}<\mathrm{V}_{\text {RT(L) }}, 3.0 \mathrm{k} \Omega$ to $\mathrm{V}_{\text {OUT }}$ | - | 0.1 | 0.4 | v |
| RESET Output Leakage | $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RT(H) }}$ Current | - | 0 | 10 | $\mu \mathrm{A}$ |
| Delay Capacitor Discharge Voltage | Discharge Latched "ON", $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RT }}$ | - | 0.2 | 0.5 | V |
| Delay Time | $\mathrm{C}_{\text {DELAY }}=0.1 \mu \mathrm{~F}$, Note 4 | 16 | 32 | 48 | ms |

3. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.
4. Assuming ideal capacitor.

DelayTime $=\frac{\mathrm{C}_{\text {Delay }} \times \mathrm{V}_{\text {Delay Threshold Charge }}}{I_{\text {Charge }}}=\mathrm{C}_{\text {Delay }} \times 3$

PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  |  | FUNCTION |
| :---: | :---: | :---: | :---: |
| SO-16L | $\begin{aligned} & \text { TO-220 } \\ & 5 \text { LEAD } \end{aligned}$ | LEAD SYMBOL |  |
| 1 | 1 | $\mathrm{V}_{\text {IN }}$ | Unregulated supply voltage to IC. |
| 16 | 5 | $\mathrm{V}_{\text {OUT }}$ | Regulated 5.0 V output. |
| $\begin{gathered} 4,5,11,12 \\ 13 \end{gathered}$ | 3 | GND | Ground Connection. |
| 8 | 4 | Delay | Timing capacitor for RESET function. |
| 6 | 2 | RESET | CMOS/TTL compatible output lead. RESET goes low whenever $\mathrm{V}_{\text {OUT }}$ drops below $6.0 \%$ of it's regulated value. |
| 14 | N/A | $\mathrm{V}_{\text {OUT(SENSE) }}$ | Remote sensing of output voltage. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Quiescent Current vs. Input Voltage Over Temperature


Figure 4. Output Voltage vs. Input Voltage Over Temperature


Figure 3. Quiescent Current vs. Input Voltage Over Load Resistance


Figure 5. $\mathrm{V}_{\text {OUT }}$ vs. $\mathrm{V}_{\text {IN }}$ Over $\mathrm{R}_{\text {LOAD }}$

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 6. Line Regulation vs. Output Current


Figure 8. Dropout Voltage vs. Output Current


Figure 10. Ripple Rejection


Figure 7. Load Regulation vs. Output Current


Figure 9. Quiescent Current vs. Output Current


Figure 11. Output Capacitor ESR


CIRCUIT DESCRIPTION

The CS8129 $\overline{\text { RESET }}$ function has hysteresis on both the reset and delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V .
The RESET circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text { RESET }}$ output NPN transistor is controlled by the two circuits described (see Block Diagram on page 605).

## Low Voltage Inhibit Circuit

This circuit monitors output voltage, and when output voltage is below the specified minimum causes the RESET output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the RESET output transistor to go into the OFF state if allowed by the RESET Delay circuit.

## Reset Delay Circuit

This circuit provides a programmable (by external capacitor) delay on the RESET output lead. The Delay lead provides source current to the external delay capacitor only when the "Low Voltage Inhibit" circuit indicates that output voltage is above $\mathrm{V}_{\mathrm{RT}(\mathrm{ON}) \text {. Otherwise, the Delay lead sinks }}$ current to ground (used to discharge the delay capacitor). The discharge current is latched ON when the output voltage is below $\mathrm{V}_{\mathrm{RT}(\mathrm{OFF})}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures that a controlled $\overline{\text { RESET }}$ pulse is generated following detection of an error
condition. The circuit allows the RESET output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $\mathrm{V}_{\mathrm{DC}(\mathrm{HI})}$.


Figure 13. Test \& Application Circuit
The Delay time for the $\overline{\text { RESET }}$ function is calculated from the formula:

$$
\begin{gathered}
\text { Delay time }=\frac{C_{\text {Delay }} \times V_{\text {Delay Threshold }}}{I_{\text {Charge }}} \\
\text { Delay time }=\mathrm{C}_{\text {Delay }(\mu \mathrm{F})} \times 3.2 \times 10^{5}
\end{gathered}
$$

If $\mathrm{C}_{\text {Delay }}=0.1 \mu \mathrm{~F}$, Delay time $(\mathrm{ms})=32 \mathrm{~ms} \pm 50 \%$ : i.e. 16 ms to 48 ms . The tolerance of the capacitor must be taken into account to calculate the total variation in the delay time.

## APPLICATION NOTES

## STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor CouT shown in Figure 13 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for COUT for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 14) is:
$P_{D}($ max $)=\left\{V_{I N}(\text { max })-V_{\text {OUT }}(\text { min }) \mid \operatorname{IOUT}(\text { max })+V_{I N(m a x)}\right)^{Q}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at

> IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 14. Single Output Regulator With Key Performance Parameters Labeled

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \mathrm{JA}}$.

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, $Y$ = Year
WW, W = Work Week

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> FIVE LEAD | SO-16L | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.1 | 23 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | 105 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC34268

## 800 mA, 2.85 V, SCSI-2 Active Terminator, Low Dropout Voltage Regulator

The MC34268 is a medium current, low dropout positive voltage regulator specifically designed for use in SCSI-2 active termination circuits. This device offers the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum. The regulator consists of a 1.0 V dropout composite PNP/NPN pass transistor, current limiting, and thermal limiting. These devices are packaged in the 8 -pin SOP-8 and 3-pin DPAK and SOT-223 surface mount power packages.

Applications include active SCSI-2 terminators and post regulation of switching power supplies.

- 2.85 V Output Voltage for SCSI-2 Active Termination
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to $1.4 \%$ Tolerance
- No Minimum Load Required
- Space Saving DPAK, SOT-223 and SOP-8 Surface Mount Power Packages


## Simplified Block Diagram




## ON Semiconductor ${ }^{\text {™ }}$

http://onsemi.com
MARKING DIAGRAMS

| SOP-8SSUFFIX <br> CASE 751 |  | MARKING DIAGRAMS |
| :---: | :---: | :---: |
|  |  |  |
| $\begin{aligned} & A=\text { Assembly Location } \\ & L=\text { Wafer Lot } \\ & Y=\text { Year } \\ & W=\text { Work Week } \end{aligned}$ |  |  |
|  | 8 | NC |
|  | 7 <br> 6 | \} Output |
|  | 5 | NC |
| (Top View) |  |  |



Pin 1. Ground
2. Output
3. Input
4. Output
(Top View)
Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 614 of this data sheet.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Input Voltage | $\mathrm{V}_{\text {in }}$ | 15 | V |
| Power Dissipation and Thermal Characteristics DT Suffix, Plastic Package, Case 369A $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Derate Above $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Case Thermal Resistance, Junction-to-Air <br> D Suffix, Plastic Package, Case 751 <br> $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Derate Above $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Case <br> Thermal Resistance, Junction-to-Air <br> ST Suffix, Plastic Package, Case 318E <br> $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, Derate Above $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Case <br> Thermal Resistance, Junction-to-Air | $\mathrm{P}_{\mathrm{D}}$ <br> $\mathrm{R}_{\text {өJc }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {өJA }}$ | Internally Limted 5.0 87 Internally Limited 22 140 Internally Limited 15 245 | $\begin{gathered} W \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ \mathrm{~W} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ \mathrm{~W} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | 0 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

## ELECTRICAL CHARACTERISTICS

( $\mathrm{V}_{\text {in }}=4.25 \mathrm{~V}, \mathrm{C}_{\mathrm{O}}=10 \mu \mathrm{~F}$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ ) Output Voltage, over Line, Load, and Temperature ( $\mathrm{V}_{\text {in }}=3.9 \mathrm{~V}$ to 15 V , $\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}$ to 490 mA ) | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 2.81 \\ & 2.76 \end{aligned}$ | $\begin{aligned} & 2.85 \\ & 2.85 \end{aligned}$ | $\begin{aligned} & 2.89 \\ & 2.93 \end{aligned}$ | V |
| Line Regulation ( $\mathrm{V}_{\text {in }}=4.25 \mathrm{~V}$ to $15 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | Regline | - | - | 0.3 | \% |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}$ to $800 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | Regload | - | - | 0.5 | \% |
| Dropout Voltage ( $\mathrm{l}=490 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}$ | - | 0.95 | 1.1 | V |
| Ripple Rejection ( $f=120 \mathrm{~Hz}$ ) | RR | 55 | - | - | dB |
| Maximum Output Current ( $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}$ ) | $I_{\text {(max) }}$ | 800 | - | - | mA |
| Bias Current ( $\mathrm{V}_{\text {in }}=4.25 \mathrm{~V}, \mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}$ ) | $\mathrm{I}_{\mathrm{B}}$ | - | 5.0 to 3.0 | 8.0 | mA |
| Minimum Load Current to maintain Regulation ( $\mathrm{V}_{\text {in }}=15 \mathrm{~V}$ ) | $\mathrm{L}_{\mathrm{L} \text { (min) }}$ | - | - | 0 | mA |



Figure 1. Dropout Voltage versus Output Load Current


Figure 2. Transient Load Regulation


Figure 3. Typical SCSI Application

Figure 3 is a circuit of a typical SCSI terminator application. The MC34268 is designed specifically to provide 2.85 V required to drive a SCSI-2 bus. The output current capability of the regulator is in excess of 800 mA ; enough to drive standard SCSI-2, fast SCSI-2, and some wide SCSI-2 applications. The typical dropout voltage is less than 1.0 V , allowing the IC to regulate to input voltages less than 4.0 V . Internal protective features include current and thermal limiting.


Figure 4. SOP-8 Thermal Resistance versus P.C.B. Copper Length

The MC34268 requires an external $10 \mu \mathrm{~F}$ capacitor with an ESR of less than $10 \Omega$ for stability over temperature. With economical electrolytic capacitors, cold temperature operation can pose a stability problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Tantalum capacitors may be a better choice if small size is a requirement. Also, the capacitance and ESR of a tantalum capacitor is more stable over temperature.


Figure 5. DPAK Thermal Resistance versus P.C.B. Copper Length

ORDERING INFORMATION

| Device | Package | Shipping Information |
| :--- | :---: | :---: |
| MC34268D | SO-8 | 98 Units / Rail |
| MC34268DR2 | SO-8 | 2500 Units / Tape \& Reel |
| MC34268DT | DPAK | 75 Units / Rail |
| MC34268DTRK | DPAK | 2500 Units / Tape \& Reel |
| MC34268STT3 | SOT-223 | 4000 Units / Tape \& Reel |

## Product Preview

# 1.0 A Low-Dropout Positive Fixed and Adjustable Voltage Regulators 

The NCP1117 series are low dropout positive voltage regulators that are capable of providing an output current that is in excess of 1.0 A with a maximum dropout voltage of 1.2 V at 800 mA over temperature. This series contains eight fixed output voltages of 1.5 V , $1.8 \mathrm{~V}, 2.0 \mathrm{~V}, 2.5 \mathrm{~V}, 2.85 \mathrm{~V}, 3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, and 12 V that have no minimum load requirement to maintain regulation. Also included is an adjustable output version that can be programmed from 1.25 V to 18.8 V with two external resistors. On chip trimming adjusts the reference/output voltage to within $\pm 1.0 \%$ accuracy. Internal protection features consist of output current limiting, safe operating area compensation, and thermal shutdown. The NCP1117 series can operate with up to 20 V input. Devices are available in SOT-223 and DPAK packages.

## Features

- Output Current in Excess of 1.0 A
- 1.2 V Maximum Dropout Voltage at 800 mA Over Temperature
- Fixed Output Voltages of $1.5 \mathrm{~V}, 1.8 \mathrm{~V}, 2.0 \mathrm{~V}, 2.5 \mathrm{~V}, 2.85 \mathrm{~V}, 3.3 \mathrm{~V}$, 5.0 V , and 12 V
- Adjustable Output Voltage Option
- No Minimum Load Requirement for Fixed Voltage Output Devices
- Reference/Output Voltage Trimmed to $\pm 1.0 \%$
- Current Limit, Safe Operating and Thermal Shutdown Protection
- Operation to 20 V Input

Applications

- Consumer and Industrial Equipment Point of Regulation
- Active SCSI Termination for 2.85 V Version
- Switching Power Supply Post Regulation
- Hard Drive Controllers
- Battery Chargers



## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 625 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 626 of this data sheet.

## TYPICAL APPLICATIONS



[^12]MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage（Note 1） | $\mathrm{V}_{\text {in }}$ | 20 | V |
| Output Short Circuit Duration（Notes 2 and 3） | － | Infinite | － |
| Power Dissipation and Thermal Characteristics <br> Case 318H（SOT－223） <br> Power Dissipation（Note 2） <br> Thermal Resistance，Junction－to－Ambient，Minimum Size Pad <br> Thermal Resistance，Junction－to－Case <br> Case 369A（DPAK） <br> Power Dissipation（Note 2） <br> Thermal Resistance，Junction－to－Ambient，Minimum Size Pad Thermal Resistance，Junction－to－Case | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {日JC }}$ <br> $P_{D}$ <br> $R_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJc }}$ | Internally Limited 160 <br> 15 <br> Internally Limited <br> 67 <br> 6.0 | W <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> W ${ }^{\circ} \mathrm{C} / \mathrm{W}$ ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | －65 to 150 | ${ }^{\circ} \mathrm{C}$ |

1．This device series contains ESD protection and exceeds the following tests：
Human Body Model 2000 V per MIL－STD－883，Method 3015.
Machine Model Method 200 V ．
2．Internal thermal shutdown protection limits the die temperature to approximately $175^{\circ} \mathrm{C}$ ．Proper heatsinking is required to prevent activation． The maximum package power dissipation is：

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

3．The regulator output current must not exceed 1.0 A with $\mathrm{V}_{\text {in }}$ greater than 12 V ．

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\text {in }}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=10 \mu \mathrm{~F}\right.$ ，for typical value $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ，for min and max values $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ unless otherwise noted．）

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Reference Voltage，Adjustable Output Devices $\begin{aligned} & \left(V_{\text {in }}-V_{\text {out }}=2.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\text {in }}-V_{\text {out }}=1.4 \mathrm{~V} \text { to } 10 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 1.238 \\ & 1.225 \end{aligned}$ |  | $\begin{aligned} & 1.262 \\ & 1.270 \end{aligned}$ | V |
| Output Voltage，Fixed Output Devices | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\begin{array}{ll} 1.5 \mathrm{~V} \quad & \left(\mathrm{~V}_{\text {in }}=3.5 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right) \\ \left(\mathrm{V}_{\text {in }}=2.9 \mathrm{~V} \text { to } 11.5 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{array}$ |  | $\begin{aligned} & 1.485 \\ & 1.470 \end{aligned}$ | 1.500 | $\begin{aligned} & 1.515 \\ & 1.530 \end{aligned}$ |  |
| $\begin{array}{ll} 1.8 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=3.8 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right) \\ \left(\mathrm{V}_{\text {in }}=3.2 \mathrm{~V} \text { to } 11.8 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{array}$ |  | $\begin{aligned} & 1.782 \\ & 1.755 \end{aligned}$ | 1.800 | $\begin{aligned} & 1.818 \\ & 1.845 \end{aligned}$ |  |
| $\begin{array}{ll} 2.0 \mathrm{~V} \quad & \left(\mathrm{~V}_{\text {in }}=4.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\text {in }}=3.4 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{array}$ |  | $\begin{aligned} & 1.970 \\ & 1.960 \end{aligned}$ | 2.000 | $\begin{aligned} & 2.030 \\ & 2.040 \end{aligned}$ |  |
| $\begin{array}{ll} 2.5 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\text {in }}=3.9 \mathrm{~V} \text { to } 10 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{array}$ |  | $\begin{aligned} & 2.475 \\ & 2.450 \end{aligned}$ | 2.500 | $\begin{aligned} & 2.525 \\ & 2.550 \end{aligned}$ |  |
| $\begin{aligned} & 2.85 \mathrm{~V}\left(\mathrm{~V}_{\text {in }}=4.85 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right) \\ &\left(\mathrm{V}_{\text {in }}=4.25 \mathrm{~V} \text { to } 10 \mathrm{~V}, \mathrm{I}_{\text {out }} 0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \\ &\left(\mathrm{V}_{\text {in }}=4.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 500 \mathrm{~mA}, \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{aligned}$ |  | $\begin{aligned} & 2.821 \\ & 2.790 \\ & 2.790 \end{aligned}$ | 2.850 | $\begin{aligned} & 2.879 \\ & 2.910 \\ & 2.910 \end{aligned}$ |  |
| $\begin{aligned} 3.3 \mathrm{~V} \quad & \left(\mathrm{~V}_{\text {in }}=5.3 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\text {in }}=4.75 \mathrm{~V} \text { to } 10 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{aligned}$ |  | $\begin{aligned} & 3.267 \\ & 3.235 \end{aligned}$ | 3.300 | $\begin{aligned} & 3.333 \\ & 3.365 \end{aligned}$ |  |
| $\begin{array}{ll} 5.0 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=7.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\text {in }}=6.5 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{array}$ |  | $\begin{aligned} & 4.950 \\ & 4.900 \end{aligned}$ | 5.000 | $\begin{aligned} & 5.050 \\ & 5.100 \end{aligned}$ |  |
| $\begin{aligned} & 12 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=14 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \\ &\left(\mathrm{V}_{\text {in }}=13.5 \mathrm{~V} \text { to } 20 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA} \text { to } 800 \mathrm{~mA}, \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}\right) \end{aligned}$ |  | $\begin{aligned} & 11.880 \\ & 11.760 \end{aligned}$ | 12.000 | $\begin{aligned} & 12.120 \\ & 12.240 \end{aligned}$ |  |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\text {in }}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {out }}=10 \mu \mathrm{~F}\right.$, for typical value $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min and max values $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ```Line Regulation (Note 4) Adjustable ( \(\mathrm{V}_{\text {in }}=2.75 \mathrm{~V}\) to 16.25 V , \(\mathrm{I}_{\text {out }}=10 \mathrm{~mA}\) ) \(1.5 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=2.9 \mathrm{~V}\right.\) to \(\left.11.5 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\) \(1.8 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=3.2 \mathrm{~V}\right.\) to \(\left.11.8 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\) \(2.0 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=3.4 \mathrm{~V}\right.\) to \(\left.12 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\) \(2.5 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=3.9 \mathrm{~V}\right.\) to \(\left.10 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\) \(2.85 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=4.25 \mathrm{~V}\right.\) to \(\left.10 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\) \(3.3 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=4.75 \mathrm{~V}\right.\) to \(\left.15 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\) \(5.0 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=6.5 \mathrm{~V}\right.\) to \(\left.15 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\) \(12 \mathrm{~V} \quad\left(\mathrm{~V}_{\text {in }}=13.5 \mathrm{~V}\right.\) to \(\left.20 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)\)``` | $\mathrm{Reg}_{\text {line }}$ | - | $\begin{gathered} 0.04 \\ 0.3 \\ 0.4 \\ 0.5 \\ 0.5 \\ 0.8 \\ 0.8 \\ 0.9 \\ 1.0 \end{gathered}$ | $\begin{aligned} & 0.1 \\ & 1.0 \\ & 1.0 \\ & 2.5 \\ & 2.5 \\ & 3.0 \\ & 4.5 \\ & 6.0 \\ & 7.5 \end{aligned}$ | \% mV |
| ```Load Regulation (Note 4) Adjustable ( \(\mathrm{l}_{\text {out }}=10 \mathrm{~mA}\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=4.25 \mathrm{~V}\) ) \(1.5 \mathrm{~V} \quad\left(\mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=2.9 \mathrm{~V}\) ) \(1.8 \mathrm{~V} \quad\left(\mathrm{l}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=3.2 \mathrm{~V}\) ) \(2.0 \mathrm{~V} \quad\left(\mathrm{l}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=3.4 \mathrm{~V}\) ) \(2.5 \mathrm{~V} \quad\left(\mathrm{l}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=3.9 \mathrm{~V}\) ) \(2.85 \mathrm{~V} \quad\left(\mathrm{l}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(\left.800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=4.25 \mathrm{~V}\right)\) \(3.3 \mathrm{~V} \quad\left(\mathrm{l}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=4.75 \mathrm{~V}\) ) \(5.0 \mathrm{~V} \quad\left(\mathrm{l}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=6.5 \mathrm{~V}\) ) \(12 \mathrm{~V} \quad\left(\mathrm{l}_{\text {out }}=0 \mathrm{~mA}\right.\) to \(800 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=13.5 \mathrm{~V}\) )``` | $\mathrm{Reg}_{\text {line }}$ | - | $\begin{aligned} & 0.2 \\ & 2.3 \\ & 2.6 \\ & 3.0 \\ & 3.3 \\ & 3.8 \\ & 4.3 \\ & 6.7 \\ & 16 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 5.5 \\ & 6.0 \\ & 6.0 \\ & 7.5 \\ & 8.0 \\ & 10 \\ & 15 \\ & 28 \end{aligned}$ | \% mV |
| $\begin{aligned} & \text { Dropout Voltage (Measured at } \left.V_{\text {out }}-100 \mathrm{mV}\right) \\ & \left(\text { l }_{\text {out }}=100 \mathrm{~mA}\right) \\ & \left(\text { lout }_{\text {out }}=500 \mathrm{~mA}\right) \\ & \left(\mathrm{l}_{\text {out }}=800 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ |  | $\begin{aligned} & 0.95 \\ & 1.01 \\ & 1.07 \end{aligned}$ | $\begin{aligned} & 1.10 \\ & 1.15 \\ & 1.20 \end{aligned}$ | V |
| Output Current Limit ( $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}=5.0 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$, Note 5) | $\mathrm{I}_{\text {out }}$ | 1000 | 1500 | 2200 | mA |
| Minimum Required Load Current for Regulation, Adjustable Output Devices $\left(\mathrm{V}_{\mathrm{in}}=15 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{L} \text { (min) }}$ | - | 0.8 | 5.0 | mA |
| Quiescent Current $\begin{array}{ll} 1.5 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=11.5 \mathrm{~V}\right) \\ 1.8 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=11.8 \mathrm{~V}\right) \\ 2.0 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=12 \mathrm{~V}\right) \\ 2.5 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=10 \mathrm{~V}\right) \\ 2.85 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=10 \mathrm{~V}\right) \\ 3.3 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=15 \mathrm{~V}\right) \\ 5.0 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=15 \mathrm{~V}\right) \\ 12 \mathrm{~V} & \left(\mathrm{~V}_{\text {in }}=20 \mathrm{~V}\right) \end{array}$ | $\mathrm{I}_{\mathrm{Q}}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 3.6 \\ & 4.2 \\ & 4.5 \\ & 5.2 \\ & 5.5 \\ & 6.0 \\ & 6.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 10 \\ & 10 \\ & 10 \\ & 10 \\ & 10 \\ & 10 \\ & 10 \end{aligned}$ | mA |
| Thermal Regulation ( $\mathrm{A}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 30 \mathrm{~ms}$ Pulse) |  | - | 0.01 | 0.1 | \%/W |
| ```Ripple Rejection \(\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}=6.4 \mathrm{~V}, \mathrm{I}_{\text {out }}=500 \mathrm{~mA}, 10 \mathrm{~V}_{\mathrm{pp}} 120 \mathrm{~Hz}\right.\) Sinewave \()\) Adjustable 1.5 V 1.8 V 2.0 V 2.5 V 2.85 V 3.3 V 5.0 V 12 V``` | RR | $\begin{aligned} & 67 \\ & 66 \\ & 64 \\ & 64 \\ & 62 \\ & 62 \\ & 60 \\ & 57 \\ & 50 \end{aligned}$ | $\begin{aligned} & 73 \\ & 72 \\ & 70 \\ & 70 \\ & 68 \\ & 68 \\ & 64 \\ & 61 \\ & 54 \end{aligned}$ |  | dB |
| Adjustment Pin Current ( $\left.\mathrm{V}_{\text {in }}=11.25 \mathrm{~V}, \mathrm{I}_{\text {out }}=800 \mathrm{~mA}\right)$ | $\mathrm{I}_{\text {adj }}$ | - | 52 | 120 | $\mu \mathrm{A}$ |
| Adjust Pin Current Change $\left(V_{\text {in }}-V_{\text {out }}=1.4 \mathrm{~V} \text { to } 10 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA} \text { to } 800 \mathrm{~mA}\right)$ | $\Delta \mathrm{l}_{\text {adj }}$ | - | 0.4 | 5.0 | $\mu \mathrm{A}$ |
| Temperature Stability | $\mathrm{S}_{\text {T }}$ | - | 0.5 | - | \% |
| Long Term Stability ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 1000 \mathrm{Hrs}$ End Point Measurement) | $\mathrm{S}_{\mathrm{t}}$ | - | 0.3 | - | \% |
| RMS Output Noise ( $\mathrm{f}=10 \mathrm{~Hz}$ to 10 kHz ) | N | - | 0.003 | - | \% $\mathrm{V}_{\text {out }}$ |

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. The regulator output current must not exceed 1.0 A with $\mathrm{V}_{\text {in }}$ greater than 12 V .

## NCP1117



Figure 4. Output Voltage Change vs. Temperature


Figure 6. Output Short Circuit Current vs. Differential Voltage


Figure 8. Adjust Pin Current vs. Temperature


Figure 5. Dropout Voltage vs. Output Current


Figure 7. Output Short Circuit Current vs. Temperature


Figure 9. Quiescent Current Change
vs. Temperature


Figure 10. NCP1117XTA Ripple Rejection vs. Output Current


Figure 12. NCP1117XT285
Line Transient Response


Figure 14. NCP1117XT50 Line Transient Response


Figure 11. NCP1117XTA Ripple Rejection vs. Frequency


Figure 13. NCP1117XT285 Load Transient Response


Figure 15. NCP1117XT50 Load Transient Response

## NCP1117



Figure 16. NCP1117XT12 Line Transient Response


Figure 17. NCP1117XT12 Load Transient Response


Figure 18. SOT-223 Thermal Resistance and Maximum Power Dissipation vs. P.C.B. Copper Length


Figure 19. DPAK Thermal Resistance and Maximum Power Dissipation vs. P.C.B. Copper Length

## APPLICATIONS INFORMATION

## Introduction

The NCP1117 features a significant reduction in dropout voltage along with enhanced output voltage accuracy and temperature stability when compared to older industry standard three-terminal adjustable regulators. These devices contain output current limiting, safe operating area compensation and thermal shutdown protection making them designer friendly for powering numerous consumer and industrial products. The NCP1117 series is pin compatible with the older LM317 and its derivative device types.

## Output Voltage

The typical application circuits for the fixed and adjustable output regulators are shown in Figures 20 and 21. The adjustable devices are floating voltage regulators. They develop and maintain the nominal 1.25 V reference voltage between the output and adjust pins. The reference voltage is programmed to a constant current source by resistor R1, and this current flows through R2 to ground to set the output voltage. The programmed current level is usually selected to be greater than the specified 5.0 mA minimum that is required for regulation. Since the adjust pin current, $\mathrm{I}_{\mathrm{adj}}$, is significantly lower and constant with respect to the programmed load current, it generates a small output voltage error that can usually be ignored. For the fixed output devices R1 and R2 are included within the device and the ground current $\mathrm{I}_{\mathrm{gnd}}$, ranges from 3.0 mA to 5.0 mA depending upon the output voltage.

## External Capacitors

Input bypass capacitor $\mathrm{C}_{\text {in }}$ may be required for regulator stability if the device is located more than a few inches from the power source. This capacitor will reduce the circuit's sensitivity when powered from a complex source impedance and significantly enhance the output transient response. The input bypass capacitor should be mounted with the shortest possible track length directly across the regulator's input and ground terminals. A $10 \mu \mathrm{~F}$ ceramic or tantalum capacitor should be adequate for most applications.


Figure 20. Fixed Output Regulator

Frequency compensation for the regulator is provided by capacitor $\mathrm{C}_{\text {out }}$ and its use is mandatory to ensure output stability. A minimum capacitance value of $4.7 \mu \mathrm{~F}$ with an equivalent series resistance (ESR) that is within the limits of $0.25 \Omega$ to $2.2 \Omega$ is required. The capacitor type can be ceramic, tantalum, or aluminum electrolytic as long as it meets the minimum capacitance value and ESR limits over the circuit's entire operating temperature range. Higher values of output capacitance can be used to enhance loop stability and transient response with the additional benefit of reducing output noise.


Figure 21. Adjustable Output Regulator
The output ripple will increase linearly for fixed and adjustable devices as the ratio of output voltage to the reference voltage increases. For example, with a 12 V regulator, the output ripple will increase by $12 \mathrm{~V} / 1.25 \mathrm{~V}$ or 9.6 and the ripple rejection will decrease by $20 \log$ of this ratio or 19.6 dB . The loss of ripple rejection can be restored to the values shown with the addition of bypass capacitor $\mathrm{C}_{\mathrm{adj}}$, shown in Figure 21. The reactance of $\mathrm{C}_{\mathrm{adj}}$ at the ripple frequency must be less than the resistance of R1. The value of R1 can be selected to provide the minimum required load current to maintain regulation and is usually in the range of $100 \Omega$ to $200 \Omega$.

$$
\mathrm{C}_{\mathrm{adj}}>\frac{1}{2 \pi \text { fripple }^{\mathrm{R} 1}}
$$

The minimum required capacitance can be calculated from the above formula. When using the device in an application that is powered from the AC line via a transformer and a full wave bridge, the value for $\mathrm{C}_{\text {adj }}$ is:
fripple $=120 \mathrm{~Hz}, \mathrm{R} 1=120 \Omega$, then $\mathrm{C}_{\text {adj }}>11.1 \mu \mathrm{~F}$
The value for $\mathrm{C}_{\text {adj }}$ is significantly reduced in applications where the input ripple frequency is high. If used as a post regulator in a switching converter under the following conditions:
fripple $=50 \mathrm{kHz}, \mathrm{R} 1=120 \Omega$, then $\mathrm{C}_{\text {adj }}>0.027 \mu \mathrm{~F}$
Figures 10 and 11 shows the level of ripple rejection that is obtainable with the adjust pin properly bypassed.

## Protection Diodes

The NCP1117 family has two internal low impedance diode paths that normally do not require protection when used in the typical regulator applications. The first path connects between $\mathrm{V}_{\text {out }}$ and $\mathrm{V}_{\text {in }}$, and it can withstand a peak surge current of about 15 A . Normal cycling of $\mathrm{V}_{\text {in }}$ cannot generate a current surge of this magnitude. Only when $\mathrm{V}_{\text {in }}$ is shorted or crowbarred to ground and $\mathrm{C}_{\text {out }}$ is greater than $50 \mu \mathrm{~F}$, it becomes possible for device damage to occur. Under these conditions, diode D1 is required to protect the device. The second path connects between $\mathrm{C}_{\mathrm{adj}}$ and $\mathrm{V}_{\text {out }}$, and it can withstand a peak surge current of about 150 mA . Protection diode D2 is required if the output is shorted or crowbarred to ground and $\mathrm{C}_{\mathrm{adj}}$ is greater than $1.0 \mu \mathrm{~F}$.


Figure 22. Protection Diode Placement
A combination of protection diodes D1 and D2 may be required in the event that $\mathrm{V}_{\text {in }}$ is shorted to ground and $\mathrm{C}_{\mathrm{adj}}$ is greater than $50 \mu \mathrm{~F}$. The peak current capability stated for the internal diodes are for a time of $100 \mu$ s with a junction temperature of $25^{\circ} \mathrm{C}$. These values may vary and are to be used as a general guide.

## Load Regulation

The NCP1117 series is capable of providing excellent load regulation; but since these are three terminal devices, only partial remote load sensing is possible. There are two conditions that must be met to achieve the maximum available load regulation performance. The first is that the top side of programming resistor R1 should be connected as close to the regulator case as practicable. This will minimize the voltage drop caused by wiring resistance RW + from appearing in series with reference voltage that is across R1.

The second condition is that the ground end of R 2 should be connected directly to the load. This allows true Kelvin sensing where the regulator compensates for the voltage drop caused by wiring resistance RW -.


Figure 23. Load Sensing

## Thermal Considerations

This series contains an internal thermal limiting circuit that is designed to protect the regulator in the event that the maximum junction temperature is exceeded. When activated, typically at $175^{\circ} \mathrm{C}$, the regulator output switches off and then back on as the die cools. As a result, if the device is continuously operated in an overheated condition, the output will appear to be oscillating. This feature provides protection from a catastrophic device failure due to accidental overheating. It is not intended to be used as a substitute for proper heatsinking. The maximum device power dissipation can be calculated by:

$$
P_{D}=\frac{T_{J}(\max )-T_{A}}{R_{\theta J A}}
$$

The devices are available in surface mount SOT-223 and DPAK packages. Each package has an exposed metal tab that is specifically designed to reduce the junction to air thermal resistance, $\mathrm{R}_{\theta J \mathrm{JA}}$, by utilizing the printed circuit board copper as a heat dissipater. Figures 18 and 19 show typical $R_{\theta J A}$ values that can be obtained from a square pattern using economical single sided 2.0 ounce copper board material. The final product thermal limits should be tested and quantified in order to insure acceptable performance and reliability. The actual $\mathrm{R}_{\theta \mathrm{JA}}$ can vary considerably from the graphs shown. This will be due to any changes made in the copper aspect ratio of the final layout, adjacent heat sources, and air flow.


Figure 24. Constant Current Regulator


Figure 26. Regulator with Shutdown


The $50 \Omega$ resistor that is in series with the ground pin of the upper regulator level shifts its output 300 mV higher than the lower regulator. This keeps the lower regulator off until the input source is removed.

Figure 28. Battery Backed-Up Power Supply


Figure 25. Slow Turn-On Regulator


Resistor R2 sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

Figure 27. Digitally Controlled Regulator


## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

The surface mount board layout is a critical portion of the total design. The footprint for the regulator package must be of correct size to insure a proper solder connection of the


SOT-223, Case 318H
package tab and pins to the printed circuit board copper. With proper footprint pad sizes, the packages will self align when subjected to a solder reflow process.


DPAK, Case 369A

## NCP1117

ORDERING INFORMATION

| Device | Nominal Output Voltage | Package | Shipping |
| :---: | :---: | :---: | :---: |
| NCP1117DTA | Adjustable | DPAK | 75 Units/Rail |
| NCP1117DTARK | Adjustable | DPAK | 2500 Units/Tape \& Reel |
| NCP1117STAT3 | Adjustable | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT15 | 1.5 | DPAK | 75 Units/Rail |
| NCP1117DT15RK | 1.5 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST15T3 | 1.5 | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT18 | 1.8 | DPAK | 75 Units/Rail |
| NCP1117DT18RK | 1.8 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST18T3 | 1.8 | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT20 | 2.0 | DPAK | 75 Units/Rail |
| NCP1117DT20RK | 2.0 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST20T3 | 2.0 | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT25 | 2.5 | DPAK | 75 Units/Rail |
| NCP1117DT25RK | 2.5 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST25T3 | 2.5 | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT285 | 2.85 | DPAK | 75 Units/Rail |
| NCP1117DT285RK | 2.85 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST285T3 | 2.85 | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT33 | 3.3 | DPAK | 75 Units/Rail |
| NCP1117DT33RK | 3.3 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST33T3 | 3.3 | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT50 | 5.0 | DPAK | 75 Units/Rail |
| NCP1117DT50RK | 5.0 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST50T3 | 5.0 | SOT-223 | 4000 Units/Tape \& Reel |
| NCP1117DT12 | 12 | DPAK | 75 Units/Rail |
| NCP1117DT12RK | 12 | DPAK | 2500 Units/Tape \& Reel |
| NCP1117ST12T3 | 12 | SOT-223 | 4000 Units/Tape \& Reel |

## NCP1117

## MARKING DIAGRAMS

SOT-223
ST SUFFIX CASE 318H



DPAK
DT SUFFIX
CASE $369 A$


2.85 V

3.3 V

5.0 V


12 V

$$
\begin{array}{ll}
\mathrm{A} & =\text { Assembly Location } \\
\mathrm{L} & =\text { Wafer Lot } \\
\mathrm{Y} & =\text { Year } \\
\mathrm{WW}, \mathrm{~W} & =\text { Work Week }
\end{array}
$$

## MC33269

## 800 mA, Adjustable Output, Low Dropout Voltage Regulator

The MC33269 series are low dropout, medium current, fixed and adjustable, positive voltage regulators specifically designed for use in low input voltage applications. These devices offer the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum.

The regulator consists of a 1.0 V dropout composite PNP-NPN pass transistor, current limiting, and thermal shutdown.

- $3.3 \mathrm{~V}, 5.0 \mathrm{~V}, 12 \mathrm{~V}$ and Adjustable Versions.
2.85 V version available as MC34268.
- Space Saving DPAK, SOP-8 and SOT-223 Power Packages
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to $1.0 \%$ Tolerance

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

| MC33269D | Adj | MC33269D-5.0 | 5.0 V |
| :--- | :---: | :--- | :--- |
| MC33269DT | Adj | MC33269DT-5.0 | 5.0 V |
| MC33269T | Adj | MC33269T-5.0 | 5.0 V |
| MC33269D-3.3 | 3.3 V | MC33269D-12 | 12 V |
| MC33269DT-3.3 | 3.3 V | MC33269DT-12 | 12 V |
| MC33269T-3.3 | 3.3 V | MC33269T-12 | 12 V |
| MC33269ST-3.3 | 3.3 V |  |  |

ON Semiconductor ${ }^{\text {T }}$


Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.


TO-220AB T SUFFIX CASE 221A

1. Gnd/Adj
2. $V_{\text {out }}$
3. $\mathrm{V}_{\text {in }}$


Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 633 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 634 of this data sheet.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Input Voltage | $\mathrm{V}_{\text {in }}$ | 20 | V |
| Power Dissipation <br> Case 369A (DPAK) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 751 (SOP-8) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 221A $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 318E $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $P_{D}$ $\theta_{\mathrm{JA}}$ $\theta_{\mathrm{Jc}}$ <br> $P_{D}$ $\theta_{\mathrm{JA}}$ $\theta_{\mathrm{Jc}}$ <br> $P_{D}$ $\theta_{\mathrm{JA}}$ $\theta_{\mathrm{Jc}}$ $P_{D}$ $\theta_{\mathrm{JA}}$ $\theta_{\mathrm{Jc}}$ | Internally Limited 92 6.0 Internally Limited 160 25 Internally Limited 65 5.0 Internally Limited 156 15 | W ${ }^{\circ} \mathrm{C} / \mathrm{W}$ ${ }^{\circ} \mathrm{C} / \mathrm{W}$ W ${ }^{\circ} \mathrm{C} / \mathrm{W}$ ${ }^{\circ} \mathrm{C} / \mathrm{W}$ W W ${ }^{\circ} \mathrm{C} / \mathrm{W}$ ${ }^{\circ} \mathrm{C} / \mathrm{W}$ W ${ }^{\circ} \mathrm{C} / \mathrm{W}$ ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{O}}=10 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, for min/max values $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \text { Output Voltage }\left(l_{\text {out }}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right) \\ & \text { 3.3 Suffix }\left(\mathrm{V}_{\mathrm{CC}}=5.3 \mathrm{~V}\right) \\ & 5.0 \text { Suffix }\left(\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}\right) \\ & 12 \text { Suffix }\left(\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{gathered} 3.27 \\ 4.95 \\ 11.88 \\ \hline \end{gathered}$ | $\begin{array}{r} 3.3 \\ 5.0 \\ 12 \end{array}$ | $\begin{gathered} 3.33 \\ 5.05 \\ 12.12 \\ \hline \end{gathered}$ | V |
| Output Voltage (Line, Load and Temperature) (Note 1) $\begin{aligned} & \left(1.25 \mathrm{~V} \leq \mathrm{V}_{\text {in }}-V_{\text {out }} \leq 15 \mathrm{~V}, I_{\text {out }}=500 \mathrm{~mA}\right) \\ & \text { (1.35 } \left.\mathrm{V} \leq \mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }} \leq 10 \mathrm{~V}, \mathrm{I}_{\text {out }}=800 \mathrm{~mA}\right) \\ & \text { 3.3 Suffix } \\ & \text { 5.0 Suffix } \\ & \text { 12 Suffix } \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{gathered} 3.23 \\ 4.9 \\ 11.76 \end{gathered}$ | $\begin{aligned} & 3.3 \\ & 5.0 \\ & 12 \end{aligned}$ | $\begin{gathered} 3.37 \\ 5.1 \\ 12.24 \end{gathered}$ | V |
| Reference Voltage ( $\mathrm{I}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~V}_{\text {in }}-\mathrm{V}_{\text {out }}=2.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) for Adjustable Voltage | $\mathrm{V}_{\text {ref }}$ | 1.235 | 1.25 | 1.265 | V |
| Reference Voltage (Line, Load and Temperature) (Note 1) $\begin{aligned} & \left(1.25 \mathrm{~V} \leq \mathrm{V}_{\text {in }}-V_{\text {out }} \leq 15 \mathrm{~V}, \mathrm{I}_{\text {out }}=500 \mathrm{~mA}\right) \\ & \left(1.35 \mathrm{~V} \leq \mathrm{V}_{\text {in }}-V_{\text {out }} \leq 10 \mathrm{~V}, \mathrm{I}_{\text {out }}=800 \mathrm{~mA}\right) \end{aligned}$ <br> for Adjustable Voltage | $\mathrm{V}_{\text {ref }}$ | 1.225 | 1.25 | 1.275 | V |
| Line Regulation $\left(\mathrm{l}_{\text {out }}=10 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=\left[\mathrm{V}_{\text {out }}+1.5 \mathrm{~V}\right] \text { to } \mathrm{V}_{\text {in }}=20 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | Regline | - | - | 0.3 | \% |
| Load Regulation ( $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+3.0 \mathrm{~V}, \mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ to $800 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | Regload | - | - | 0.5 | \% |
| Dropout Voltage $\begin{aligned} & \left(\mathrm{I}_{\text {out }}=500 \mathrm{~mA}\right) \\ & \left(\mathrm{l}_{\text {out }}=800 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ | - | $\begin{aligned} & 1.0 \\ & 1.1 \end{aligned}$ | $\begin{aligned} & 1.25 \\ & 1.35 \end{aligned}$ | V |
| Ripple Rejection <br> ( $10 \mathrm{Vpp}, 120 \mathrm{~Hz}$ Sinewave; $\mathrm{I}_{\text {out }}=500 \mathrm{~mA}$ ) | RR | 55 | - | - | dB |
| Current Limit ( $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}=10 \mathrm{~V}$ ) | $\mathrm{L}_{\text {Limit }}$ | 800 | - | - | mA |
| Quiescent Current (Fixed Output) $\begin{aligned} & \left(1.5 \mathrm{~V} \leq \mathrm{V}_{\text {out }} \leq 3.3 \mathrm{~V}\right) \\ & \left(5 \mathrm{~V} \leq \mathrm{V}_{\text {out }} \leq 12 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{Q}}$ | - | 5.5 | $\begin{aligned} & 8.0 \\ & 20 \end{aligned}$ | mA |

1. The MC33269-12, $\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}$ is limited to 8.0 V maximum, because of the 20 V maximum rating applied to $\mathrm{V}_{\text {in }}$.

## MC33269

ELECTRICAL CHARACTERISTICS (continued) $\left(C_{O}=10 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, for min/max values $\mathrm{T}_{J}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum Required Load Current | $I_{\text {Load }}$ |  |  |  | mA |
| Fixed Output Voltage |  | - | - | 0 |  |
| Adjustable Voltage |  | 8.0 | - | - |  |
| Adjustment Pin Current | $I_{\text {Adj }}$ | - | - | 120 | $\mu \mathrm{~A}$ |



This device contains 38 active transistors.
Figure 1. Internal Schematic


Figure 2. Dropout Voltage versus Output Load Current


Figure 4. Dropout Voltage versus Temperature


Figure 6. MC33269 Ripple Rejection versus Frequency


Figure 3. Transient Load Regulation


Figure 5. MC33269-XX Output DC Current versus Input-Output Differential Voltage


Figure 7. MC33269-ADJ Ripple Rejection versus Frequency


Figure 8. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 9. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 10. SOT-223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## APPLICATIONS INFORMATION

Figures 11 through 15 are typical application circuits. The output current capability of the regulator is in excess of 800 mA , with a typical dropout voltage of less than 1.0 V . Internal protective features include current and thermal limiting.

* The MC33269 requires an external output capacitor for stability. The capacitor should be at least $10 \mu \mathrm{~F}$ with an equivalent series resistance (ESR) of less than $10 \Omega$ but greater than $0.2 \Omega$ over the anticipated operating temperature range. With economical electrolytic capacitors, cold temperature operation can pose a problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Also capacitance and ESR of a solid tantalum capacitor is more stable over temperature. The use of a low ESR ceramic capacitor placed within close proximity to the output of the device could cause instability.
** An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the


An input capacitor is not necessary for stability, however it will improve the overall performance.

Figure 11. Typical Fixed Output Application


Figure 13. Current Regulator


The Schottky diode in series with the ground leg of the upper regulator shifts its output voltage higher by the forward voltage drop of the diode. This will cause the lower device to remain off until the input voltage is removed.

Figure 14. Battery Backed-Up Power Supply
supply input filter with long wire lengths. This will reduce the circuit's sensitivity to the input line impedance at high frequencies. A $0.33 \mu \mathrm{~F}$ or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. Applications should be tested over all operating conditions to insure stability.

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at $170^{\circ} \mathrm{C}$, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

${ }^{* * *} \mathrm{C}_{\text {Adj }}$ is optional, however it will improve the ripple rejection. The MC34269 develops a 1.25 V reference voltage between the output and the adjust terminal. Resistor R1, operates with constant current to flow through it and resistor R2. This current should be set such that the Adjust Pin current causes negligible drop across resistor R2. The total current with minimum load should be greater than 8.0 mA .

Figure 12. Typical Adjustable Output Application

$\mathrm{R}_{2}$ sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

Figure 15. Digitally Controlled Voltage Regulator

## MC33269

## ORDERING INFORMATION

| Device | Package | Shipping Information |
| :--- | :---: | :---: |
| MC33269D | SO-8 | 98 Units / Rail |
| MC33269DR2 | SO-8 | 2500 Units / Tape \& Reel |
| MC33269DT | DPAK | 75 Units / Rail |
| MC33269DTRK | DPAK | 2500 Units / Tape \& Reel |
| MC33269T | TO-220 | 50 Units / Rail |
| MC33269D-3.3 | SO-8 | 98 Units / Rail |
| MC33269DR2-3.3 | SO-8 | 2500 Units / Tape \& Reel |
| MC33269DT-3.3 | DPAK | 75 Units / Rail |
| MC33269DTRK-3.3 | DPAK | 2500 Units / Tape \& Reel |
| MC33269ST-3.3T3 | SOT-223 | 4000 Units / Tape \& Reel |
| MC33269T-3.3 | TO-220 | 50 Units / Rail |
| MC33269D-5.0 | SO-8 | 98 Units / Rail |
| MC33269DR2-5.0 | SO-8 | 2500 Units / Tape \& Reel |
| MC33269DT-5.0 | DPAK | 75 Units / Rail |
| MC33269DTRK-5.0 | DPAK | 2500 Units / Tape \& Reel |
| MC33269T-5.0 | TO-220 | 50 Units / Rail |
| MC33269D-12 | SO-8 | 98 Units / Rail |
| MC33269DR2-12 | SO-8 | 2500 Units / Tape \& Reel |
| MC33269DT-12 | DPAK | 75 Units / Rail |
| MC33269DTRK-12 | DPAK | 2500 Units / Tape \& Reel |
| MC33269T-12 | TO-220 | 50 Units / Rail |

## MC33269

## MARKING DIAGRAMS

## SO-8 D SUFFIX CASE 751



DPAK

## DT SUFFIX

CASE 369A


TO-220AB
T SUFFIX
CASE 221A

$\begin{array}{ll}\text { A } & =\text { Assembly Location } \\ \text { WL, L } & =\text { Wafer Lot } \\ \text { Y } & =\text { Year } \\ \text { WW, W } & =\text { Work Week }\end{array}$

## CS5201-3

### 1.0 A, 3.3 V Fixed Linear Regulator

The CS5201-3 linear regulator provides 1.0 A @ 3.3 V reference at 1.0 A with an output voltage accuracy of $\pm 1.5 \%$.

This regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages less than 1.2 V at 1.0 A output current.

The maximum quiescent current is only 10 mA at full load. Device protection includes over-current and thermal shutdown.

The CS5201-3 is pin compatible with the LT1086 family of linear regulators.

The regulator is available in TO-220, surface mount $\mathrm{D}^{2}$, and SOT-223 packages.

## Features

- Output Current to 1.0 A
- Output Accuracy to $\pm 1.5 \%$ Over Temperature
- Dropout Voltage (typical) 1.0 V @ 1.0 A
- Fast Transient Response
- Fault Protection
- Current Limit
- Thermal Shutdown


Figure 1. Applications Diagram

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http://onsemi.com


ORDERING INFORMATION* $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5201-3GT3 | TO-220 $\ddagger$ | 50 Units/Rail |
| CS5201-3GDP3 | D$^{2}$ PAK $\ddagger$ | 50 Units/Rail |
| CS5201-3GDPR3 | D$^{2}$ PAK $\ddagger$ | 750 Tape \& Reel |
| CS5201-3GST3 | SOT-223 $\ddagger$ | 80 Units/Rail |
| CS5201-3GSTR3 | SOT-223 $\ddagger$ | 2500 Tape \& Reel |

*Additional ordering information can be found on page 640 of this data sheet.
$\dagger$ Consult your local sales representative for other fixed output voltage versions.
$\ddagger$ TO-220 are all 3 -pin, straight leaded. D2PAK and SOT-223 are all 3-pin.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 640 of this data sheet.

## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {IN }}$ |  | 7.0 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak 230 Peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |
| ESD Damage Threshold (Human Body Model) |  | 2.0 | kV |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\text {DROPOUT }}<\mathrm{V}_{\mathrm{IN}}<7.0 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=1.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fixed Output Voltage |  |  |  |  |  |
| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} \\ & 0 \leq \mathrm{I}_{\text {OUT }} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 3.250 \\ (-1.5 \%) \end{gathered}$ | 3.300 | $\begin{gathered} 3.350 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $2.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 3.7 \mathrm{~V}$; IOUT $=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=2.0 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 1.0 \mathrm{~A}$ | - | 0.04 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~A}$ | - | 1.0 | 1.2 | V |
| Current Limit | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$ | 1.0 | 3.1 | - | A |
| Quiescent Current | $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation (Note 6) | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | 0.020 | \%/W |
| Ripple Rejection (Note 6) | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} ; \text { lout }=1.0 \mathrm{~A} ; \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {PP }} \end{aligned}$ | - | 80 | - | dB |
| Thermal Shutdown (Note 7) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 7) | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.
6. Guaranteed by design, not $100 \%$ tested in production.
7. Thermal shutdown is $100 \%$ functionally tested in production.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |  | Function |
| :---: | :---: | :---: | :---: | :--- | :--- |
| TO-220 | D$^{2}$ PAK | SOT-223 | Pin Symbol |  |  |
| 1 | 1 | 1 | GND | Ground connection. |  |
| 2 | 2 | 2 | V $_{\text {OUT }}$ | Regulated output voltage (case). |  |
| 3 | 3 | 3 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |  |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 4. Reference Voltage vs. Temperature


Figure 6. Ripple Rejection vs. Frequency


Figure 7. Transient Response


Figure 8. Short Circuit Current vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$

## APPLICATIONS INFORMATION

The CS5201-3 linear regulator provides a fixed 3.3 V output voltage at currents up to 1.0 A . The regulator is protected against overcurrent conditions and includes thermal shutdown.

The CS5201-3 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5201-3 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and
ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\mathrm{IN}}$ drops. In the CS5201-3 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 9 is recommended.


Figure 9. Protection Diode Scheme for Large Output Capacitors

## Output Voltage Sensing

Since the CS5201-3 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the regulator should be connected as shown in Figure 10.


Figure 10. Conductor Parasitic Resistance Effects Can Be Minimized With the Above Grounding Scheme For Fixed Output Regulators

## Calculating Power Dissipation and Heat Sink Requirements

The CS5201-3 linear regulator includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $P_{D}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{4}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta \mathrm{SA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{6}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (4).

The value for $\mathrm{R}_{\Theta \mathrm{JC}}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS5201-3 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta} \mathrm{SA}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

## CS5201-3

ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5201-3GT3 | $1.0 \mathrm{~A}, 3.3 \mathrm{~V}$ Output | TO-220 THREE LEAD, STRAIGHT |
| CS5201-3GDP3 | $1.0 \mathrm{~A}, 3.3 \mathrm{~V}$ Output | D$^{2}$ PAK 3-PIN |
| CS5201-3GDPR3 | $1.0 \mathrm{~A}, 3.3 \mathrm{~V}$ Output | D$^{2}$ PAK 3-PIN (Tape \& Reel) |
| CS5201-3GST3 | $1.0 \mathrm{~A}, 3.3 \mathrm{~V}$ Output | SOT-223 |
| CS5201-3GSTR3 | $1.0 \mathrm{~A}, 3.3 \mathrm{~V}$ Output | SOT-223 (Tape \& Reel) |

## MARKING DIAGRAMS



SOT-223 ST SUFFIX CASE 318E


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D$^{2}$ PAK <br> 3-PIN | SOT-223 | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 3.5 | 3.5 | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | $10-50^{*}$ | 156 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J A}=\mathrm{R}_{\Theta J C}+\mathrm{R}_{\Theta C A}$


## CS5201-1

### 1.0 A Adjustable Linear Regulator

The CS5201-1 linear regulator provides 1.0 A with an output voltage accuracy of $\pm 1.0 \%$. The device uses two external resistors to set the output voltage within a 1.25 V to 5.5 V range.

This regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages less than 1.2 V at 1.0 A output current. Device protection includes overcurrent and thermal shutdown.

The CS5201 is pin compatible with the LT1086 family of linear regulators.

The regulator is available in TO-220, surface mount $\mathrm{D}^{2}$, and SOT-223 packages.

## Features

- Output Current to 1.0 A
- Output Accuracy to $\pm 1.0 \%$ Over Temperature
- Dropout Voltage (typical) 1.0 V @ 1.0 A
- Fast Transient Response
- Fault Protection
- Current Limit
- Thermal Shutdown


Figure 1. Applications Diagram

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ORDERING INFORMATION* $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5201-1GT3 | TO-220 $\ddagger$ | 50 Units/Rail |
| CS5201-1GDP3 | D$^{2}$ PAK $\ddagger$ | 50 Units/Rail |
| CS5201-1GDPR3 | D$^{2}$ PAK $\ddagger$ | 750 Tape \& Reel |
| CS5201-1GST3 | SOT-223 $\ddagger$ | 80 Units/Rail |
| CS5201-1GSTR3 | SOT-223 $\ddagger$ | 2500 Tape \& Reel |

*Additional ordering information can be found on page 647 of this data sheet.
$\dagger$ Consult your local sales representative for fixed output voltage versions.
$\ddagger$ TO-220 are all 3-pin, straight leaded. D2 PAK and SOT-223 are all 3-pin.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 647 of this data sheet.

ABSOLUTE MAXIMUM RATINGS*


1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\text {DROPOUT }}<\mathrm{V}_{\mathrm{IN}}<7.0 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=1.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Adjustable Output Voltage |  |  |  |  |  |
| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V} \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.241 \\ (-1.0 \%) \end{gathered}$ | 1.254 | $\begin{gathered} 1.266 \\ (+1.0 \%) \end{gathered}$ | V |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 5.75 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 1.0 \mathrm{~A}$ | - | 0.04 | 0.40 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~A}$ | - | 1.0 | 1.2 | V |
| Current Limit | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C}$ | 1.1 | 3.1 | - | A |
| Minimum Load Current (Note 6) | $\mathrm{V}_{\mathrm{IN}}=7.0 \mathrm{~V}, \mathrm{~V}_{\text {Adj }}=0 \mathrm{~V}$ | - | 0.6 | 2.0 | mA |
| Adjust Pin Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 50 | 100 | $\mu \mathrm{A}$ |
| Thermal Regulation (Note 7) | $30 \mathrm{~ms} \mathrm{Pulse}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | 0.020 | \%/W |
| Ripple Rejection (Note 7) | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\text {OUT }}=1.0 \mathrm{~A} ; \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \\ & \mathrm{V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {PP }} \end{aligned}$ | - | 80 | - | dB |
| Thermal Shutdown (Note 8) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 8) | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.
6. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum load requirement.
7. Guaranteed by design, not $100 \%$ tested in production.
8. Thermal shutdown is $100 \%$ functionally tested in production.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |  |
| :---: | :---: | :---: | :---: | :--- |
| TO-220 | D$^{2}$ PAK | SOT-223 | Pin Symbol |  |
| 1 | 1 | 1 | Adj | Adjust pin (low side of the internal reference). |
| 2 | 2 | 2 | $\mathrm{~V}_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | 3 | 3 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 4. Reference Voltage vs. Temperature


Figure 6. Minimum Load Current vs.
$\mathbf{V}_{\text {IN }} \mathbf{V}_{\text {OUT }}$


Figure 7. Adjust Pin Current vs. Temperature


Figure 9. Transient Response


Figure 8. Ripple Rejection vs. Frequency


Figure 10. Short Circuit Current vs. $\mathrm{V}_{\text {IN }}$ - $\mathrm{V}_{\text {OUT }}$

## APPLICATIONS INFORMATION

The CS5201-1 linear regulator provides adjustable voltages at currents up to 1.0 A . The regulator is protected against overcurrent conditions and includes thermal shutdown.

The CS5201-1 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The CS5201-1 has an output voltage range of 1.25 V to 5.5 V . An external resistor divider sets the output voltage as shown in Figure 11. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R 1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.

The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{R E F} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{A d j} \times R 2
$$

The term $\mathrm{I}_{\text {Adj }} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R1 is chosen so that the minimum load current is at least 2.0 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. While not required, a bypass capacitor from the adjust pin to ground will improve ripple rejection and transient response. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Type and value may be varied to obtain optimum performance vs. price.


Figure 11. Resistor Divider Scheme

## Short Circuit Protection

The CS5201-1 linear regulator has an absolute maximum specification of 7.0 V for the voltage difference between $\mathrm{V}_{\mathrm{IN}}$ and Vout. However, the IC may be used to regulate voltages in excess of 7.0 V . The main considerations in such a design are power-up and short circuit capability.

In most applications, ramp-up of the power supply to $\mathrm{V}_{\mathrm{IN}}$ is fairly slow, typically on the order of several tens of milliseconds, while the regulator responds in less than one microsecond. In this case, the linear regulator begins charging the load as soon as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential is large enough that the pass transistor conducts current. The load at this point is essentially at ground, and the supply voltage is on the order of several hundred millivolts, with the result that the pass transistor is in dropout. As the supply to $\mathrm{V}_{\text {IN }}$ increases, the pass transistor will remain in dropout, and current is passed to the load until $\mathrm{V}_{\text {OUT }}$ reaches the point at which the IC is in regulation. Further increase in the supply voltage brings the pass transistor out of dropout. The result is that the output voltage follows the power supply ramp-up, staying in dropout until the regulation point is reached. In this manner, any output voltage may be regulated. There is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 7.0 V is not exceeded.

However, the possibility of destroying the IC in a short circuit condition is very real for this type of design. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Over-voltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential to less than 7.0 V if failsafe operation is required. One possible clamp circuit is
illustrated in Figure 12; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit condition indefinitely while protecting the IC.


Figure 12. Short Circuit Protection Circuit for High Voltage Application.

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.
The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.
A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5201-1 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{ESR}
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5201-1 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 13 is recommended.


Figure 13. Protection Diode for Large Output Capacitors

## Output Voltage Sensing

Since the CS5201-1 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load.

For the adjustable regulator, the best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 14. If R1 is connected to the load, RC is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes.

$$
\mathrm{R}_{\mathrm{C}} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 14. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitic Resistance Effects

## Calculating Power Dissipation and Heat Sink Requirements

The CS5201-1 linear regulator includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.
The case is connected to V Vut on the CS5201-1, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.
The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{7}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
$I_{\text {OUT(max) }}$ is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta \mathrm{JA}}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta \mathrm{SA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{9}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (7).

The value for $\mathrm{R}_{\Theta J C}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS5201-1 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and
thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5201-1GT3 | 1.0 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |
| CS5201-1GDP3 | 1.0 A, Adj. Output | D$^{2}$ PAK 3-PIN |
| CS5201-1GDPR3 | 1.0 A, Adj. Output | D$^{2}$ PAK 3-PIN (Tape \& Reel) |
| CS5201-1GST3 | 1.0 A, Adj. Output | SOT-223 |
| CS5201-1GSTR3 | 1.0 A, Adj. Output | SOT-223 (Tape \& Reel) |

MARKING DIAGRAMS


SOT-223
ST SUFFIX CASE 318E


A =Assembly Location
WL, L = Wafer Lot
$\mathrm{YY}, \mathrm{Y}=$ Year
WW, W = Work Week

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D $^{2}$ PAK <br> 3-PIN | SOT-223 | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 3.5 | 3.5 | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{*}$ | 156 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$


## CS52015-3

### 1.5 A, 3.3 V Fixed Linear Regulator

The CS52015-3 linear regulator provides 1.5 A @ 3.3 V reference at 1.0 A with an output voltage accuracy of $\pm 1.5 \%$.

The regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages less than 1.4 V at 1.5 A output current. The maximum quiescent current is only 10 mA at full load. Device protection includes over-current and thermal shutdown.

The CS52015-3 is pin compatible with the LT1086 family of linear regulators but has lower dropout voltage.

The regulator is available in TO-220, surface mount $\mathrm{D}^{2}$, and SOT-223 packages.

## Features

- Output Current to 1.5 A
- Output Accuracy to $\pm 1.5 \%$ Over Temperature
- Dropout Voltage (typical) 1.05 V @ 1.5 A
- Fast Transient Response
- Fault Protection
- Current Limit
- Thermal Shutdown


Figure 1. Applications Diagram

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


ORDERING INFORMATION* $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS52015-3GT3 | TO-220 $\ddagger$ | 50 Units/Rail |
| CS52015-3GDP3 | D$^{2}$ PAK $\ddagger$ | 50 Units/Rail |
| CS52015-3GDPR3 | D2PAK $\ddagger$ | 750 Tape \& Reel |
| CS52015-3GST3 | SOT-223 $\ddagger$ | 80 Units/Rail |
| CS52015-3GSTR3 | SOT-223 $\ddagger$ | 2500 Tape \& Reel |

*Additional ordering information can be found on page 653 of this data sheet.
$\dagger$ Consult your local sales representative for other fixed output voltage versions.
$\ddagger$ TO-220 are all 3 -pin, straight leaded. D2 PAK and SOT-223 are all 3-pin.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 653 of this data sheet.

## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {IN }}$ |  | 7.0 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak <br> 230 Peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |
| ESD Damage Threshold |  | 2.0 | kV |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\text {DROPOUT }}<\mathrm{V}_{\mathrm{IN}}<7.0 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=1.5 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fixed Output Voltage |  |  |  |  |  |
| Output Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \\ & 0 \leq \mathrm{I}_{\text {OUT }} \leq 1.5 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 3.250 \\ (-1.5 \%) \end{gathered}$ | 3.300 | $\begin{gathered} 3.350 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $2.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 3.7 \mathrm{~V}$; IOUT $=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=2.0 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 1.5 \mathrm{~A}$ | - | 0.04 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=1.5 \mathrm{~A}$ | - | 1.05 | 1.4 | V |
| Current Limit | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$ | 1.6 | 3.1 | - | A |
| Quiescent Current | $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation (Note 6) | $30 \mathrm{~ms} \mathrm{Pulse}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | 0.020 | \%/W |
| Ripple Rejection (Note 6) | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\text {OUT }}=1.5 \mathrm{~A} ; \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \\ & \mathrm{V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {PP }} \end{aligned}$ | - | 80 | - | dB |
| Thermal Shutdown (Note 7) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 7) | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.
6. Guaranteed by design, not $100 \%$ tested in production.
7. Thermal shutdown is $100 \%$ functionally tested in production.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |  | Function |
| :---: | :---: | :---: | :---: | :--- | :--- |
| TO-220 | D$^{2}$ PAK | SOT-223 | Pin Symbol |  |  |
| 1 | 1 | 1 | GND | Ground connection. |  |
| 2 | 2 | 2 | V $_{\text {OUT }}$ | Regulated output voltage (case). |  |
| 3 | 3 | 3 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |  |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Ripple Rejection vs. Frequency


Figure 4. Output Voltage vs. Temperature


Figure 6. Short Circuit Current vs.


Figure 7. Transient Response


Figure 8. Load Regulation vs. Output Current

## APPLICATIONS INFORMATION

The CS52015-3 linear regulator provides a 3.3 V output voltage at currents up to 1.5 A . The regulator is protected against overcurrent conditions and includes thermal shutdown.

The CS52015-3 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS52015-3 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\mathrm{IN}}$ drops. In the CS52015-3 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 9 is recommended.


Figure 9. Protection Diode Scheme for Large Output Capacitors

## Output Voltage Sensing

Since the CS52015-3 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the regulator should be connected as shown in Figure 10.


Figure 10. Conductor Parasitic Resistance Effects Can Be Minimized With the Above Grounding Scheme For Fixed Output Regulators

## Calculating Power Dissipation and Heat Sink Requirements

The CS52015-3 linear regulator includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V OUT on the CS52015-3, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JJ}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{10}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S \mathrm{~A}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{12}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (10).

The value for $\mathrm{R}_{\Theta J C}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS52015-3 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta} \mathrm{SA}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \text { JA }}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part Number | Type | Description |
| :---: | :---: | :---: |
| CS52015-3GT3 | 1.5 A, 3.3 V Output | TO-220 THREE LEAD, STRAIGHT |
| CS52015-3GDP3 | 1.5 A, 3.3 V Output | D2PAK 3-PIN |
| CS52015-3GDPR3 | 1.5 A, 3.3 V Output | D2PAK 3-PIN (Tape \& Reel) |
| CS52015-3GST3 | 1.5 A, 3.3 V Output | SOT-223 |
| CS52015-3GSTR3 | 1.5 A, 3.3 V Output | SOT-223 (Tape \& Reel) |

## MARKING DIAGRAMS



SOT-223 ST SUFFIX CASE 318E


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D $^{2}$ PAK <br> 3-PIN | SOT-223 | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 3.5 | 3.5 | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{\star}$ | 156 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J A}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta C A}$


## CS52015-1

### 1.5 A Adjustable Linear Regulator

The CS52015-1 linear regulator provides 1.5 A with an accuracy of $\pm 1.0 \%$. The device uses two external resistors to set the output voltage within a 1.25 V to 5.5 V range.

The regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages less than 1.4 V at 1.5 A output current. Device protection includes overcurrent and thermal shutdown.

The CS52015-1 is pin compatible with the LT1086 family of linear regulators but has lower dropout voltage.

The regulator is available in TO-220, surface mount $\mathrm{D}^{2}$, and SOT-223 packages.

## Features

- Output Current to 1.5 A
- Output Accuracy to $\pm 1.0 \%$ Over Temperature
- Dropout Voltage (typical) 1.05 V @ 1.5 A
- Fast Transient Response
- Fault Protection
- Current Limit
- Thermal Shutdown


Figure 1. Application Diagram

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


ORDERING INFORMATION* $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS52015-1GT3 | TO-220 $\ddagger$ | 50 Units/Rail |
| CS52015-1GDP3 | D2PAK $\ddagger$ | 50 Units/Rail |
| CS52015-1GDPR3 | D$^{2}$ PAK $\ddagger$ | 750 Tape \& Reel |
| CS52015-1GST3 | SOT-223 $\ddagger$ | 80 Units/Rail |
| CS52015-1GSTR3 | SOT-223 $\ddagger$ | 2500 Tape \& Reel |

*Additional ordering information can be found on page 660 of this data sheet.
$\dagger$ Consult your local sales representative for fixed output voltage versions.
$\ddagger$ TO-220 are all 3 -pin, straight leaded. D2PAK and SOT-223 are all 3-pin.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 660 of this data sheet.

ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ |  | 7.0 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak 230 Peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |
| ESD Damage Threshold |  | 2.0 | kV |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\text {DROPOUT }}<\mathrm{V}_{\mathrm{IN}}<7.0 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=1.5 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Adjustable Output Voltage |  |  |  |  |  |
| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V} \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 1.5 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.241 \\ (-1.0 \%) \end{gathered}$ | 1.254 | $\begin{gathered} 1.266 \\ (+1.0 \%) \end{gathered}$ | V |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 5.75 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 1.5 \mathrm{~A}$ | - | 0.04 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=1.5 \mathrm{~A}$ | - | 1.05 | 1.4 | V |
| Current Limit | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C}$ | 1.6 | 3.1 | - | A |
| Minimum Load Current (Note 6) | $\mathrm{V}_{\mathrm{IN}}=7.0 \mathrm{~V}, \mathrm{~V}_{\text {Adj }}=0 \mathrm{~V}$ | - | 0.6 | 2.0 | mA |
| Adjust Pin Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 50 | 100 | $\mu \mathrm{A}$ |
| Thermal Regulation (Note 7) | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | 0.020 | \%/W |
| Ripple Rejection (Note 7) | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\text {OUT }}=1.5 \mathrm{~A} ; \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} \text {; } \\ & \quad \mathrm{V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {PP }} \end{aligned}$ | - | 80 | - | dB |
| Thermal Shutdown (Note 8) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 8) | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.
6. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum requirement.
7. Guaranteed by design, not $100 \%$ tested in production.
8. Thermal shutdown is $100 \%$ functionally tested in production.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |  |
| :---: | :---: | :---: | :---: | :--- |
| TO-220 | D2PAK | SOT-223 | Pin Symbol |  |
| 1 | 1 | 1 | Adj | Adjust pin (low side of the internal reference). |
| 2 | 2 | 2 | V $_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | 3 | 3 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 4. Reference Voltage vs. Temperature


Figure 6. Minimum Load Current vs.
$\mathrm{V}_{\text {IN }} \mathrm{V}_{\text {OUT }}$


Figure 7. Adjust Pin Current vs. Temperature


Figure 9. Transient Response


Figure 8. Ripple Rejection vs. Frequency


Figure 10. Short Circuit Current vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$

## APPLICATIONS INFORMATION

The CS52015-1 linear regulator provides adjustable voltages at currents up to 1.5 A . The regulator is protected against overcurrent conditions and includes thermal shutdown.

The CS52015-1 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The CS52015-1 has an output voltage range of 1.25 V to 5.5 V . An external resistor divider sets the output voltage as shown in Figure 11. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.
The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{R E F} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{A d j} \times R 2
$$

The term $\mathrm{I}_{\text {Adj }} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R 1 is chosen so that the minimum load current is at least $2.0 \mathrm{~mA} . \mathrm{R} 1$ and R2 should be the same type, e.g. metal film for best tracking over temperature. While not required, a bypass capacitor from the adjust pin to ground will improve ripple rejection and transient response. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Type and value may be varied to obtain optimum performance vs. price.


Figure 11. Resistor Divider Scheme

## Short Circuit Protection

The CS52015-1 linear regulator has an absolute maximum specification of 7.0 V for the voltage difference between $\mathrm{V}_{\text {IN }}$ and $\mathrm{V}_{\text {OUT }}$. However, the IC may be used to regulate voltages in excess of 7.0 V . The main considerations in such a design are power-up and short circuit capability.

In most applications, ramp-up of the power supply to $\mathrm{V}_{\mathrm{IN}}$ is fairly slow, typically on the order of several tens of milliseconds, while the regulator responds in less than one microsecond. In this case, the linear regulator begins charging the load as soon as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential is large enough that the pass transistor conducts current. The load at this point is essentially at ground, and the supply voltage is on the order of several hundred millivolts, with the result that the pass transistor is in dropout. As the supply to $\mathrm{V}_{\text {IN }}$ increases, the pass transistor will remain in dropout, and current is passed to the load until $\mathrm{V}_{\text {OUT }}$ reaches the point at which the IC is in regulation. Further increase in the supply voltage brings the pass transistor out of dropout. The result is that the output voltage follows the power supply ramp-up, staying in dropout until the regulation point is reached. In this manner, any output voltage may be regulated. There is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 7.0 V is not exceeded.

However, the possibility of destroying the IC in a short circuit condition is very real for this type of design. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Over-voltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential to less than 7.0 V if failsafe operation is required. One possible clamp circuit is
illustrated in Figure 12; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit condition indefinitely while protecting the IC.


Figure 12. Short Circuit Protection Circuit for High Voltage Application.

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.
The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS52015-1 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{ESR}
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close as possible to the load for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS52015-1 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 13 is recommended.


Figure 13. Protection Diode for Large Output Capacitors

## Output Voltage Sensing

Since the CS52015-1 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load.

For the adjustable regulator, the best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 14. If R1 is connected to the load, RC is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes.

$$
\mathrm{R}_{\mathrm{C}} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 14. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitic Resistance Effects

## Calculating Power Dissipation and Heat Sink Requirements

The CS52015-1 linear regulator includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.
The case is connected to V Vut on the CS52015-1, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.
The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{13}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:
$P_{D}($ max $)=\left\{\mathrm{V}_{\operatorname{IN}(\text { max })}-\mathrm{V}_{\mathrm{OUT}(\text { min })}\right\}_{\mathrm{I}} \mathrm{OUT}($ max $)+\mathrm{V}_{\mathrm{IN}(\text { max })} \mathrm{I}_{\mathrm{Q}}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
$I_{\text {OUT(max) }}$ is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta \mathrm{JA}}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\text {©SA }}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{15}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (13).

The value for $\mathrm{R}_{\Theta J C}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS52015-1 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and
thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS52015-1GT3 | 1.5 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |
| CS52015-1GDP3 | 1.5 A, Adj. Output | D²PAK 3-PIN |
| CS52015-1GDPR3 | 1.5 A, Adj. Output | D$^{2}$ PAK 3-PIN (Tape \& Reel) |
| CS52015-1GST3 | 1.5 A, Adj. Output | SOT-223 |
| CS52015-1GSTR3 | 1.5 A, Adj. Output | SOT-223 (Tape \& Reel) |

MARKING DIAGRAMS


SOT-223
ST SUFFIX
CASE 318E


A = Assembly Location
WL, L = Wafer Lot
$\mathrm{YY}, \mathrm{Y}=$ Year
WW, W = Work Week

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D$^{2}$ PAK <br> 3-PIN | SOT-223 | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 3.5 | 3.5 | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{\star}$ | 156 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$


## CS5203-3

### 3.0 A, 3.3 V Fixed Linear Regulator

The CS5203-3 linear regulator provides 3.3 V reference at 3.0 A with an output voltage accuracy of $\pm 1.5 \%$.

This regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to provide 3.0 A of output current with dropout voltages of less than 1.15 V . The maximum quiescent current is only 10 mA at full load. Device protection includes over-current and thermal shutdown.

The CS5203-3 is pin compatible with the LT1085 family of linear regulators.

The regulator is available in a surface mount $\mathrm{D}^{2}$ package.

## Features

- Output Current to 3.0 A
- Output Accuracy to $\pm 1.5 \%$ Over Temperature
- Dropout Voltage (typical) 1.15 V @ 3.0 A
- Fast Transient Response
- Fault Protection
- Current Limit
- Thermal Shutdown


Figure 1. Application Diagram

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http://onsemi.com

$\mathrm{Tab}=\mathrm{V}_{\text {OUT }}$
Pin 1. GND
2. $V_{\text {OUT }}$
3. $\mathrm{V}_{\mathrm{IN}}$
$D^{2}$ PAK
3-PIN
DP SUFFIX
CASE 418E

## MARKING DIAGRAM



$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION* $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5203-3GDP3 | D$^{2}$ PAK $\ddagger$ | 50 Units/Rail |
| CS5203-3GDPR3 | D$^{2}$ PAK $\ddagger$ | 750 Tape \& Reel |

*Additional ordering information can be found on page 665 of this data sheet.
$\dagger$ Consult your local sales representative for other package options.
$\ddagger D^{2} P A K$ are all 3-pin.

## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {IN }}$ |  | 7.0 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow (SMD styles only) Note 1 | 230 Peak | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold (Human Body Model) |  | 2.0 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\text {DROPOUT }}<\mathrm{V}_{\text {IN }}<7.0 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=3.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fixed Output Voltage |  |  |  |  |  |
| Output Voltage (Notes 2 and 3) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \\ & 0 \leq \mathrm{I}_{\text {OUT }} \leq 3.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 3.250 \\ (-1.5 \%) \end{gathered}$ | 3.300 | $\begin{gathered} 3.350 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $2.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 3.7 \mathrm{~V}$; I IOUT $=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation (Notes 2 and 3) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=2.0 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 3.0 \mathrm{~A}$ | - | 0.04 | 0.4 | \% |
| Dropout Voltage (Note 4) | $\mathrm{I}_{\text {OUT }}=3.0 \mathrm{~A}$ | - | 1.15 | 1.4 | V |
| Current Limit | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$ | 3.1 | 4.6 | - | A |
| Quiescent Current | IOUT $=10 \mathrm{~mA}$ | - | 6.0 | 10 | mA |
| Thermal Regulation (Note 5) | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | 0.020 | \%/W |
| Ripple Rejection (Note 5) | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\text {OUT }}=3.0 \mathrm{~A} ; \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \\ & \mathrm{V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {PP }} \end{aligned}$ | - | 80 | - | dB |
| Thermal Shutdown (Note 6) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 6) | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

2. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to temperature changes must be taken into account seperately.
3. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
4. Dropout voltage is a measurement of the minimum input/output differential at full load.
5. Guaranteed by design, not tested in production.
6. Thermal shutdown is $100 \%$ functionally tested in production.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |
| :---: | :---: | :--- |
| $\mathbf{D}^{2}$ PAK | Pin Symbol |  |
| 1 | GND | Ground connection. |
| 2 | V $_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 4. Output Voltage Deviation vs. Temperature


Figure 6. Ripple Rejection vs. Frequency


Figure 7. Transient Response


Figure 8. Short Circuit Current vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$

## APPLICATIONS INFORMATION

The CS5203-3 linear regulator provides a fixed 3.3 V output voltage at currents up to 3.0 A . The regulator is protected against overcurrent conditions and includes thermal shutdown.

The CS5203-3 has a composite PNP-NPN output transistor and requires an output capacitor for stability.

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5203-3 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5203-3 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 9 is recommended.


Figure 9. Protection Diode Scheme for Large Output Capacitors

## Output Voltage Sensing

Since the CS5203-3 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the regulator should be connected as shown in Figure 10.


Figure 10. Conductor Parasitic Resistance Effects Can Be Minimized With the Above Grounding Scheme For Fixed Output Regulators

## Calculating Power Dissipation and Heat Sink Requirements

The CS5203-3 linear regulator includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{16}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S \mathrm{~A}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{18}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J \text { J }}$ is calculated using equation (3) and the result can be substituted in equation (16).

The value for $\mathrm{R}_{\Theta \mathrm{JC}}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS5203-3 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta} \mathrm{SA}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5203-3GDP3 | 3.0 A, 3.3 V Output | D$^{2}$ PAK 3-PIN |
| CS5203-3GDPR3 | 3.0 A, 3.3 V Output | D$^{2}$ PAK 3-PIN (Tape \& Reel) |

PACKAGE THERMAL DATA

| Parameter |  | D $^{2}$ PAK, 3-PIN | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 3.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta \mathrm{JA}}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta C A}$


## CS5203A-1, CS5203A-2, CS5203A-3, CS5203A-5

### 3.0 A Adjustable, and Fixed 1.5 V, 3.3 V and 5.0 V Linear Regulators

The CS5203A series of linear regulators provides 3.0 A at adjustable and fixed voltages with an accuracy of $\pm 1.0 \%$ and $\pm 2.0 \%$ respectively. The adjustable version uses two external resistors to set the output voltage within a 1.25 V to 13 V range.

The regulators are intended for use as post regulators and microprocessor supplies. The fast loop response and low dropout voltage make these regulators ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulators are fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The CS5203A is pin compatible with the LT1085 family of linear regulators but has lower dropout voltage.

The regulators are available in TO-220 and surface mount $\mathrm{D}^{2} \mathrm{PAK}$ packages.

## Features

- Output Current to 3.0 A
- Output Trimmed to $\pm 1.0 \%$
- Dropout Voltage 1.05 V @ 3.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram - CS5203A-1


ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5203A-1GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5203A-1GDP3 | D$^{2}$ PAK $\dagger$ | 50 Units/Rail |
| CS5203A-1GDPR3 | D2 2PAK $\dagger$ | 750 Tape \& Reel |
| CS5203A-2GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5203A-2GDP3 | D$^{2}$ PAK $\dagger$ | 50 Units/Rail |
| CS5203A-2GDPR3 | D2PAK $\dagger$ | 750 Tape \& Reel |
| CS5203A-2GDPSR33 | D2PAK $\dagger$ | 750 Tape \& Reel |
| CS5203A-3GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5203A-3GDP3 | D2PAK $\dagger$ | 50 Units/Rail |
| CS5203A-3GDPR3 | D2PAK $\dagger$ | 750 Tape \& Reel |
| CS5203A-3GDPSR33 | D2PAK $\dagger$ | 750 Tape \& Reel |
| CS5203A-5GT3 | TO-220 $\dagger$ | 50 Units/Rail |

*Additional ordering information can be found on page 674 of this data sheet.
†TO-220 is 3-pin, straight leaded. D²PAK are all 3-pin.
DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 674 of this data sheet.


Figure 2. Block Diagram - CS5203A-2, -3, -5

## ABSOLUTE MAXIMUM RATINGS*

|  | Parameter | Value |
| :--- | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ | Unit |  |
| Operating Temperature Range | 17 | V |
| Junction Temperature | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | Wave Solder (through hole styles only) Note 1 | 150 |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}$ Tantalum, $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }} \leq 15 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=3.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Adjustable Output Voltage (CS5203A-1)

| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}, \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 3.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 1.241 \\ & (-1 \%) \end{aligned}$ | 1.254 | $\begin{aligned} & 1.266 \\ & (+1 \%) \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 3.0 \mathrm{~A}$ | - | 0.03 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=3.0 \mathrm{~A}$ | - | 1.05 | 1.15 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{J} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=15 \mathrm{~V} \end{aligned}$ | $3.2$ | $\begin{aligned} & 5.5 \\ & 2.5 \end{aligned}$ |  | $\begin{aligned} & \mathrm{A} \\ & \mathrm{~A} \end{aligned}$ |
| Minimum Load Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=7.0 \mathrm{~V}$ | - | 1.2 | 6.0 | mA |
| Adjust Pin Current | - | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjust Pin Current Change | $\begin{gathered} 1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 4.0 \mathrm{~V} ; \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 3.0 \mathrm{~A} \end{gathered}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| Thermal Regulation | 30 ms pulse; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%/W |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
4. Specifictions apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## CS5203A-1, CS5203A-2, CS5203A-3, CS5203A-5

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 15 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=3.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- |

Adjustable Output Voltage (CS5203A-1) (continued)

| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{C}_{\text {Adj }}=25 \mu \mathrm{~F} ;$ lout $=3.0 \mathrm{~A}$ | - | 85 | - | dB |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Temperature Stability | - | - | 0.5 | - | $\%$ |
| RMS Output Noise | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | $\% \mathrm{~V}_{\mathrm{OUT}}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}$ Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 15 \mathrm{~V}$,
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{l}_{\text {full load }}=3.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Fixed Output Voltage (CS5203A-2, CS5203A-3, CS5203A-5)

| Reference Voltage (Notes 6 and 7) CS5203A-5 CS5203A-3 CS5203A-2 | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 0 \leq \mathrm{IOUT} \leq 3.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 0 \leq \mathrm{IOUT} \leq 3.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 0 \leq \mathrm{IOUT} \leq 3.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 4.9(-2 \%) \\ 3.234(-2 \%) \\ 1.47(-2 \%) \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 3.3 \\ & 1.5 \end{aligned}$ | $\begin{gathered} 5.1(+2 \%) \\ 3.366(+2 \%) \\ 1.53(+2 \%) \end{gathered}$ | $\begin{aligned} & V \\ & V \\ & V \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; I IOUT $=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 6 and 7) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 3.0 \mathrm{~A}$ | - | 0.03 | 0.4 | \% |
| Dropout Voltage (Note 8) | $\mathrm{I}_{\text {OUT }}=3.0 \mathrm{~A}$ | - | 1.05 | 1.15 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{J} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=15 \mathrm{~V} \end{aligned}$ | $3.2$ | $\begin{aligned} & 5.5 \\ & 2.5 \end{aligned}$ | - | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; I $_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{pulse;} \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%/W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; lout $=3.0 \mathrm{~A}$ | - | 78 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise (\%V ${ }_{\text {OUT }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

6. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
7. Specifictions apply for an external Kelvin sense connection atr a point on the output pin $1 / 4^{\prime \prime}$ from the bottom of the package.
8. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  | Pin Symbol | Function |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5203A-1 |  | CS5203A-2, -3, -5 |  |  |  |
| D2PAK | TO-220 | D2PAK | TO-220 |  |  |
| 1 | 1 | N/A | N/A | Adj | Adjust pin (low side of the internal reference). |
| 2 | 2 | 2 | 2 | $\mathrm{V}_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | 3 | 3 | 3 | $\mathrm{V}_{\text {IN }}$ | Input voltage. |
| N/A | N/A | 1 | 1 | GND | Ground connection. |

## CS5203A-1, CS5203A-2, CS5203A-3, CS5203A-5

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 7. Adjust Pin Current vs. Temperature


Figure 4. Reference Voltage vs. Temperature


Figure 6. Minimum Load Current


Figure 8. Ripple Rejection vs. Frequency (Fixed Versions)


Figure 9. Ripple Rejection vs. Frequency (Adjustable Versions)

## APPLICATIONS INFORMATION

The CS5203A family of linear regulators provides fixed or adjustable voltages at currents up to 3.0 A . The regulators are protected against short circuit, and include thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increases.

The CS5203A has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The adjustable regulator (CS5203A-1) has an output voltage range of 1.25 V to 13 V . An external resistor divider sets the output voltage as shown in Figure 10. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R 2 that adds to the 1.25 V across R 1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.

The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{R E F} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{A d j} \times R 2
$$

The term $\mathrm{I}_{\mathrm{Adj}} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R1 is chosen so that the minimum load current is at least 10 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. The adjust pin is bypassed to improve the transient response and ripple rejection of the regulator.


Figure 10. Resistor Divider Scheme for the Adjustable Version

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.
The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5203A the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current.

The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under load transient conditions. The output capacitor network should be as close as possible to the load for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\mathrm{IN}}$ drops. In the CS5203A-X family of linear regulators, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figures 11 and 12 is recommended.


Figure 11. Protection Diode Scheme for Adjustable Output Regulator


Figure 12. Protection Diode Scheme for Fixed Output Regulators

## Output Voltage Sensing

Since the CS5203A is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the fixed regulators should be connected as shown in Figure 13.


Figure 13. Conductor Parasitic Resistance can be Minimized with the Above Grounding Scheme for Fixed Output Regulators

For the adjustable regulator, the best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 14. If R1 is connected to the load, $\mathrm{R}_{\mathrm{C}}$ is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes

$$
\mathrm{R}_{\mathrm{C}} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 14. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitics

## Calculating Power Dissipation and Heat Sink Requirements

The CS5203A series of linear regulators includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V OUT on the CS5203A, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{19}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:
$P_{D}($ max $)=\left\{V_{I N}(\right.$ max $)-V_{O U T}($ min $\left.)\right\} I_{O U T}($ max $)+V_{I N(m a x)}{ }^{l Q}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\mathrm{\Theta SA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{21}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (19).

The value for $\mathrm{R}_{\Theta J C}$ is normally quoted as a single figure for a given package type based on an average die size. For a high current regulator such as the CS5203A the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $R_{\Theta J A}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part Number | Type | Description |
| :---: | :---: | :---: |
| CS5203A-1GT3 | 3.0 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |
| CS5203A-1GDP3 | 3.0 A, Adj. Output | D2PAK 3-PIN |
| CS5203A-1GDPR3 | 3.0 A, Adj. Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5203A-2GT3 | 3.0 A, 1.5 V Output | TO-220 THREE LEAD, STRAIGHT |
| CS5203A-2GDP3 | 3.0 A, 1.5 V Output | D2PAK 3-PIN |
| CS5203A-2GDPR3 | 3.0 A, 1.5 V Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5203A-2GDPSR3 | 3.0 A, 1.5 V Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5203A-3GT3 | 3.0 A, 3.3 V Output | TO-220 THREE LEAD, STRAIGHT |
| CS5203A-3GDP3 | 3.0 A, 3.3 V Output | D2PAK 3-PIN |
| CS5203A-3GDPR3 | 3.0 A, 3.3 V Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5203A-3GDPSR3 | 3.0 A, 3.3 V Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5203A-5GT3 | 3.0 A, 5.0 V Output | TO-220 THREE LEAD, STRAIGHT |

MARKING DIAGRAMS


PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D2PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta \mathrm{JA}}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta C A}$


## CS5253B-8

### 3.0 A LDO 5-Pin 2.5 V Fixed Linear Regulator for Remote Sense Applications

This new very low dropout linear regulator reduces total power dissipation in the application. To achieve very low dropout, the internal pass transistor is powered separately from the control circuitry. Furthermore, with the control and power inputs tied together, this device can be used in single supply configuration and still offer a better dropout voltage than conventional PNP-NPN based LDO regulators. In this mode the dropout is determined by the minimum control voltage.

The CS5253B-8 is offered in a five-terminal $\mathrm{D}^{2}$ PAK package, which allows for the implementation of a remote-sense pin permitting very accurate regulation of output voltage directly at the load, where it counts, rather than at the regulator. This remote sensing feature virtually eliminates output voltage variations due to load changes and resistive voltage drops. Typical load regulation measured at the sense pin is less than 1.0 mV for an output voltage of 2.5 V with a load step of 10 mA to 3.0 A .

The CS5253B-8 has a very fast transient loop response.
Internal protection circuitry provides for "bust-proof" operation, similar to three-terminal regulators. This circuitry, which includes overcurrent, short circuit, and overtemperature protection will self protect the regulator under all fault conditions.

The CS5253B-8 is ideal for generating a 2.5 V supply to power graphics controllers used on VGA cards. Its remote sense and low value capacitance requirements make this a low cost high performance solution. The CS5253B-8 is optimized from the CS5253-1 to allow a lower value of output capacitor to be used at the expense of a slower transient response.

## Features

- V ${ }_{\text {OUT }}$ Fixed @ $2.5 \mathrm{~V} \pm 1.5 \%$
- $V_{\text {POWER }}$ Dropout < 0.40 V @ 3.0 A
- $V_{\text {CONTROL }}$ Dropout < 1.05 V @ 3.0 A
- $1.5 \%$ Trimmed Reference
- Fast Transient Response
- Remote Voltage Sensing
- Thermal Shutdown
- Current Limit
- Short Circuit Protection
- Drop-In Replacement for EZ1582
- Backwards Compatible with 3-Pin Regulators
- Very Low Dropout Reduces Total Power Consumption

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$D^{2}$ PAK 5-PIN DP SUFFIX

$$
\mathrm{Tab}=\mathrm{V}_{\mathrm{OUT}}
$$

Pin 1. $V_{\text {SENSE }}$
2. GND
3. Vout
4. $\mathrm{V}_{\text {CONTROL }}$
5. $\mathrm{V}_{\text {POWER }}$

## MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week
ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5253B-8GDP5 | D$^{2}$ PAK $^{*}$ | 50 Units/Rail |
| CS5253B-8GDPR5 | D$^{2}$ PAK $^{*}$ | 750 Tape \& Reel |

*5-Pin.


Figure 1. Application Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| V ${ }_{\text {POWER }}$ Input Voltage |  | 6.0 | V |
| VCONTROL Input Voltage |  | 13 | V |
| Operating Junction Temperature Range, $\mathrm{T}_{J}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold |  | 2.0 | kV |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} ; \mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\text {OUT }}\right.$ and $\mathrm{GND}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5253B-8 |  |  |  |  |  |
| Output Voltage | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \text {, } \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \text { to } 3.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 2.463 \\ (-1.5 \%) \end{gathered}$ | 2.5 | $\begin{gathered} 2.538 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \end{aligned}$ | - | 0.02 | 0.2 | \% |
| Load Regulation | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}, \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \text { to } 3.0 \mathrm{~A} \text {, with Remote Sense } \end{aligned}$ | - | 0.04 | 0.3 | \% |
| Minimum Load Current (Note 2) | $\mathrm{V}_{\text {CONTROL }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.3 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=+1.0 \%$ | - | 0 | 0 | mA |
| Control Pin Current (Note 3) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\text {CONTROL }}=3.9 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=3.0 \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 6.0 \\ & 35 \end{aligned}$ | $\begin{gathered} 10 \\ 120 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ground Pin Current | $\mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}$, I l OUT $=10 \mathrm{~mA}$ | - | 7 | 10 | mA |
| Current Limit | $\mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=-4.0 \%$ | 3.1 | 4.0 | - | A |
| Short Circuit Current | $\mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | 2.0 | 3.5 | - | A |

2. The minimum load current is the minimum current required to maintain regulation.
3. The $\mathrm{V}_{\text {CONTROL }}$ pin current is the drive current required for the output transistor. This current will track output current with roughly a $1: 100$ ratio. The minimum value is equal to the quiescent current of the device.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}\right.$; $\mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\text {OUT }}$ and $\mathrm{GND}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5253B-8 |  |  |  |  |  |
| Ripple Rejection (Note 4) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=\mathrm{V}_{\text {POWER }}=3.9 \mathrm{~V}, \mathrm{~V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {P-P }} @ \\ & 120 \mathrm{~Hz}, \text { IOUT }=3.0 \mathrm{~A} \end{aligned}$ | 60 | 80 | - | dB |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{Pulse}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | - | \%/W |
| VControl Dropout Voltage (Minimum $\mathrm{V}_{\text {CONTROL }}$ - $\mathrm{V}_{\text {OUT }}$ ) (Note 5) | $\begin{aligned} & \mathrm{V}_{\text {POWER }}=3.13 \mathrm{~V}, \text { IOUT }=100 \mathrm{~mA} \\ & \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}, \text { IOUT }=1.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {POWER }}=3.13 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=3.0 \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 0.90 \\ & 1.00 \\ & 1.05 \end{aligned}$ | $\begin{aligned} & 1.15 \\ & 1.15 \\ & 1.30 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| V POWER Dropout Voltage (Minimum $\mathrm{V}_{\text {POWER }}$ - $\mathrm{V}_{\text {OUT }}$ ) (Note 5) | $\mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}$, IOUT $=100 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~A}$ <br> $\mathrm{V}_{\text {CONTROL }}=3.9 \mathrm{~V}$, I $\mathrm{I}_{\text {UTT }}=3.0 \mathrm{~A}$ | - | $\begin{aligned} & 0.05 \\ & 0.15 \\ & 0.40 \end{aligned}$ | $\begin{aligned} & 0.15 \\ & 0.25 \\ & 0.60 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| RMS Output Noise | Freq $=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Temperature Stability | - | 0.5 | - | - | \% |
| Thermal Shutdown (Note 6) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {CONTRoL }}$ Supply Only Output Current | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=13 \mathrm{~V}, \mathrm{~V}_{\text {POWER }} \text { Not Connected, } \\ & \text { GND }=\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SENSE }}=0 \mathrm{~V} \end{aligned}$ | - | - | 50 | mA |
| VPower Supply Only Output Current | $\begin{aligned} & \mathrm{V}_{\text {POWER }}=6.0 \mathrm{~V}, \mathrm{~V}_{\text {CONTROL }} \text { Not Connected, } \\ & \text { GND }=\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SENSE }}=0 \mathrm{~V} \end{aligned}$ | - | 0.1 | 1.0 | mA |

4. This parameter is guaranteed by design and is not $100 \%$ production tested.
5. Dropout is defined as either the minimum control voltage ( $\mathrm{V}_{\text {CONTROL }}$ ) or minimum power voltage ( $\mathrm{V}_{\text {POWER }}$ ) to output voltage differential required to maintain $1.5 \%$ regulation at a particular load current.
6. This parameter is guaranteed by design, but not parametrically tested in production. However, a $100 \%$ thermal shutdown functional test is performed on each part.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| D2PAK | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\text {SENSE }}$ | This Kelvin sense pin allows for remote sensing of the output voltage at the load for improved regulation. It is internally connected to the positive input of the voltage sensing error amplifier. |
| 2 | GND | This pin is connected to system ground. |
| 3 | V OUT | This pin is connected to the emitter of the power pass transistor and provides a regulated voltage capable of sourcing 3.0 A of current. |
| 4 | $\mathrm{V}_{\text {CONTROL }}$ | This is the supply voltage for the regulator control circuitry. For the device to regulate, this voltage should be between 0.9 V and 1.3 V (depending on the output current) greater than the output voltage. The control pin current will be about $1.0 \%$ of the output current. |
| 5 | $V_{\text {POWER }}$ | This is the power input voltage. This pin is physically connected to the collector of the power pass transistor. For the device to regulate, this voltage should be between 0.1 V and 0.6 V greater than the output voltage depending on the output current. The output load current of 3.0 A is supplied through this pin. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Output Voltage vs Junction Temperature


Figure 4. Output Current vs $\mathrm{V}_{\text {POWER }}$ - $\mathrm{V}_{\text {OUT }}$


Figure 5. Transient Response Comparison between CS5253-1 and CS5253B-8


Figure 7. Load Regulation vs Output Current


Figure 9. VPOWER Dropout Voltage vs Output Current


Figure 6. Short Circuit Output Current vs Junction Temperature


Figure 8. $\mathrm{V}_{\text {CONTROL }}$ Only Output Current vs Junction Temperature


Figure 10. VPOwer Only Output Current vs Junction Temperature


Figure 11. Ripple Rejection vs Frequency


Figure 13. V Control Dropout Voltage vs Output Current


Figure 12. Current Limit vs $V_{\text {OUT }}$


Figure 14. VControl Supply Current vs Junction Temperature


Figure 15. Stability vs ESR

## APPLICATIONS NOTES

## THEORY OF OPERATION

The CS5253B-8 linear regulator is fixed at 2.5 V at currents up to 3.0 A . The regulator is protected against short circuits, and includes a thermal shutdown circuit with hysteresis. The output, which is current limited, consists of a PNP-NPN transistor pair and requires an output capacitor for stability.

## $V_{\text {POWER }}$ Function

The CS5253B-8 utilizes a two supply approach to maximize efficiency. The collector of the power device is brought out to the VPOWER pin to minimize internal power dissipation under high current loads. $\mathrm{V}_{\text {CONTROL }}$ provides for the control circuitry and the drive for the output NPN transistor. $\mathrm{V}_{\text {CONTROL }}$ should be at least 1.0 V greater than the output voltage. Special care has been taken to ensure that there are no supply sequencing problems. The output voltage will not turn on until both supplies are operating. If the control voltage comes up first, the output current will be limited to about three milliamperes until the power input voltage comes up. If the power input voltage comes up first, the output will not turn on at all until the control voltage comes up. The output can never come up unregulated.

The CS5253B-8 can also be used as a single supply device with the control and power inputs tied together. In this mode, the dropout will be determined by the minimum control voltage.

## Output Voltage Sensing

The CS5253B-8 five terminal linear regulator includes a dedicated $\mathrm{V}_{\text {SENSE }}$ function. This allows for true Kelvin sensing of the output voltage. This feature can virtually eliminate errors in the output voltage due to load regulation. Regulation will be optimized at the point where the sense pin is tied to the output.

DESIGN GUIDELINES

## Remote Sense

Remote sense operation can be easily obtained with the CS5253B-8 but some care must be paid to the layout and positioning of the filter capacitors around the part. The ground side of the input capacitors on the +5.0 V and +3.3 V lines and the local $\mathrm{V}_{\text {OUT }}$-to-ground output capacitor on the IC must be tied close to the ground pin of the regulator. This will establish the stability of the part. The IC ground may then be connected to ground remotely at the load, giving the ground portion remote sense operation.
The $\mathrm{V}_{\text {SENSE }}$ line can then be tied remotely at the positive load connection, giving the feedback remote sense operation. The remote sense lines should be Kelvin connected so as to eliminate the effect of load current voltage drop. An optional bypass capacitor may be used at the load to reduce the effect of load variations and spikes.

## Current Limit

The internal current limit circuit limits the output current under excessive load conditions.

## Short Circuit Protection

The device includes short circuit protection circuitry that clamps the output current at approximately 500 mA less than its current limit value. This provides for a current foldback function, which reduces power dissipation under a direct shorted load.

## Thermal Shutdown

The thermal shutdown circuitry is guaranteed by design to activate above a die junction temperature of approximately $150^{\circ} \mathrm{C}$ and to shut down the regulator output. This circuitry has $25^{\circ} \mathrm{C}$ of typical hysteresis, thereby allowing the regulator to recover from a thermal fault automatically.


Figure 16. Remote Sense

## Calculating Power Dissipation and Heat Sink Requirements

High power regulators such as the CS5253B-8 usually operate at high junction temperatures. Therefore, it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used. Since the package tab is connected to VOUT on the CS5253B-8, electrical isolation may be required for some applications. Also, as with all high power packages, thermal compound in necessary to ensure proper heat flow. For added safety, this high current LDO includes an internal thermal shutdown circuit

The thermal characteristics of an IC depend on the following four factors: junction temperature, ambient temperature, die power dissipation, and the thermal resistance from the die junction to ambient air. The maximum junction temperature can be determined by:

$$
\mathrm{T}_{\mathrm{J}(\max )}=\mathrm{T}_{\mathrm{A}(\max )}+\mathrm{PD}_{(\max )} \times \mathrm{R}_{\Theta \mathrm{JA}}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type. The maximum power dissipation for a regulator is:

$$
\begin{aligned}
\mathrm{PD}_{(\max )}= & \left(\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{V}_{\mathrm{OUT}(\min )}\right) \operatorname{IOUT}(\max ) \\
& \left.+\mathrm{VIN}_{\text {I }} \text { max }\right) \times \operatorname{IIN}(\max )
\end{aligned}
$$

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment has a thermal resistance which is measured in degrees per watt. Like series electrical resistances, these thermal resistances are summed to determine the total thermal resistance between the die junction and the surrounding air, $\mathrm{R}_{\Theta J A}$. This total thermal resistance is comprised of three components. These resistive terms are measured from junction to case ( $\mathrm{R}_{\Theta \mathrm{JIC}}$ ), case to heat sink $\left(\mathrm{R}_{\Theta C S}\right)$, and heat sink to ambient air $\left(\mathrm{R}_{\Theta S A}\right)$. The equation is:

$$
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A}
$$

The value for $\mathrm{R}_{\Theta J C}$ is $2.5^{\circ} \mathrm{C}$ /watt for the CS5253B-8 in the D2PAK package. For a high current regulator such as the CS5253B-8 the majority of heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while the $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta J \text { J }}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see our application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## PACKAGE THERMAL DATA

| Parameter |  | D $^{2}$ PAK, 5-Pin | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$.

## CS5203-1

### 3.0 A Adjustable Linear Regulator

The CS5203-1 linear regulator provides 3.0 A at adjustable output voltages with an accuracy of $\pm 1.5 \%$. The device uses two external resistors to set the output voltage within a 1.25 V to 5.5 V range.

The regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages less than 1.4 V at 3.0 A output current. Device protection includes overcurrent and thermal shutdown.

The CS5203-1 is pin compatible with the LT1085 family of linear regulators but has lower dropout voltage.

The regulator is available in TO-220 and surface mount $\mathrm{D}^{2}$ packages.

## Features

- Output Current to 3.0 A
- Output Accuracy to $\pm 1.5 \%$ Over Temperature
- Dropout Voltage (typical) 1.2 V @ 3.0 A
- Fast Transient Response
- Fault Protection
- Current Limit
- Thermal Shutdown


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ORDERING INFORMATION* $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5203-1GT3 | TO-220 $\ddagger$ | 50 Units/Rail |
| CS5203-1GDP3 | D$^{2}$ PAK $\ddagger$ | 50 Units/Rail |
| CS5203-1GDPR3 | D$^{2}$ PAK $\ddagger$ | 750 Tape \& Reel |

*Additional ordering information can be found on page 690 of this data sheet.
$\dagger$ Consult your local sales representative for fixed output voltage versions.
$\ddagger$ TO-220 is 3 -pin, straight leaded. D²PAK is a 3 -pin.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 690 of this data sheet.

Figure 1. Applications Diagram

ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{IN}}$ |  | 7.0 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold |  | 2.0 | kV |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak 230 Peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\text {DROPOUT }}<\mathrm{V}_{\mathrm{IN}}<7.0 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=3.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Adjustable Output Voltage |  |  |  |  |  |
| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V} \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 3.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.235 \\ (-1.5 \%) \end{gathered}$ | 1.254 | $\begin{gathered} 1.273 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $2.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 5.75 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=2.0 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 3.0 \mathrm{~A}$ | - | 0.04 | 0.4 | \% |
| Dropout Voltage (Note 5) | IOUT $=3.0 \mathrm{~A}$ | - | 1.15 | 1.40 | V |
| Current Limit | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C}$ | 3.1 | 4.6 | - | A |
| Minimum Load Current (Note 6) | $\mathrm{V}_{\mathrm{IN}}=7.0 \mathrm{~V}, \mathrm{~V}_{\text {Adj }}=0 \mathrm{~V}$ | - | 0.6 | 2.0 | mA |
| Adjust Pin Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 50 | 100 | $\mu \mathrm{A}$ |
| Thermal Regulation (Note 7) | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | 0.020 | \%/W |
| Ripple Rejection (Note 7) | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\mathrm{OUT}}=3.0 \mathrm{~A} ; \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {PP }} \end{aligned}$ | - | 80 | - | dB |
| Thermal Shutdown (Note 8) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 8) | - | - | - | 25 | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.
6. Minimum load current is defined as the minimum output current required to maintain regulation. The reference resistor in the output divider is usually sized to fulfill the minimum load current requirement.
7. Guaranteed by design, not $100 \%$ functionally tested in production.
8. Guaranteed by design, not $100 \%$ parametrically tested in production. However, every part is subject to functional testing for thermal shutdown.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |
| :---: | :---: | :---: | :--- |
| TO-220 | $\mathbf{D}^{2}$ PAK | Pin Symbol |  |
| 1 | 1 | Adj | Adjust pin (low side of the internal reference). |
| 2 | 2 | $\mathrm{~V}_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | 3 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Ripple Rejection vs. Frequency


Figure 4. Bandgap Reference Voltage Deviation vs. Temperature


Figure 6. Minimum Load Current vs. $\mathbf{V}_{\text {IN }}-V_{\text {OUT }}$


Figure 7. Adjust Pin Current vs. Temperature


Figure 9. Adjust Pin Current vs. Output Current

Figure 8. Adjust Pin Current vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$


Figure 10. Transient Response


Figure 11. Short Circuit Current vs.
$\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$

## APPLICATIONS INFORMATION

The CS5203-1 linear regulator provides adjustable voltages at currents up to 3.0 A . The regulator is protected against overcurrent conditions and includes thermal shutdown.

The CS5203-1 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The CS5203-1 has an output voltage range of 1.25 V to 5.5 V . An external resistor divider sets the output voltage as shown in Figure 12. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.

The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{\text {REF }} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{A d j} \times R 2
$$

The term $\mathrm{I}_{\text {Adj }} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R1 is chosen so that the minimum load current is at least 2.0 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. While not required, a bypass capacitor from the adjust pin to ground will improve ripple rejection and transient response. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Type and value may be varied to obtain optimum performance vs. price.


Figure 12. Resistor Divider Scheme

The CS5201-1 linear regulator has an absolute maximum specification of 7.0 V for the voltage difference between $\mathrm{V}_{\text {IN }}$ and Vout. However, the IC may be used to regulate voltages in excess of 7.0 V . The main considerations in such a design are power-up and short circuit capability.

In most applications, ramp-up of the power supply to $\mathrm{V}_{\text {IN }}$ is fairly slow, typically on the order of several tens of milliseconds, while the regulator responds in less than one microsecond. In this case, the linear regulator begins charging the load as soon as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential is large enough that the pass transistor conducts current. The load at this point is essentially at ground, and the supply voltage is on the order of several hundred millivolts, with the result that the pass transistor is in dropout. As the supply to $\mathrm{V}_{\mathrm{IN}}$ increases, the pass transistor will remain in dropout, and current is passed to the load until $V_{\text {OUT }}$ reaches the point at which the IC is in regulation. Further increase in the supply voltage brings the pass transistor out of dropout. The result is that the output voltage follows the power supply ramp-up, staying in dropout until the regulation point is reached. In this manner, any output voltage may be regulated. There is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 7.0 V is not exceeded.
However, the possibility of destroying the IC in a short circuit condition is very real for this type of design. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Over-voltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential to less than 7.0 V if failsafe operation is required. One possible clamp circuit is illustrated in Figure 13; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit condition indefinitely while protecting the IC.


Figure 13. Short Circuit Protection Circuit for High Voltage Application.

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5203-1 the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5203-1 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 14 is recommended.


Figure 14. Protection Diode Scheme for Large Output Capacitors

## Output Voltage Sensing

Since the CS5203-1 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load.
For the adjustable regulator, the best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 15. If R1 is connected to the load, $\mathrm{R}_{\mathrm{C}}$ is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes.

$$
\mathrm{R}_{\mathrm{C}} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 15. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitic Resistance Effects

## Calculating Power Dissipation and Heat Sink Requirements

The CS5203-1 linear regulator includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V Vut on the CS5203-1, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{22}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:
$P_{D}($ max $)=\left\{V_{I N}(\right.$ max $)-V_{O U T}($ min $\left.)\right\} I_{O U T}($ max $)+V_{I N(m a x)}{ }^{l Q}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S \mathrm{~A}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{24}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (22).
The value for $\mathrm{R}_{\Theta \mathrm{JC}}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS5203-1 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \text { JA }}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5203-1GT3 | 3.0 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |
| CS5203-1GDP3 | 3.0 A, Adj. Output | D$^{2}$ PAK 3-PIN |
| CS5203-1GDPR3 | 3.0 A, Adj. Output | D$^{2}$ PAK 3-PIN (Tape \& Reel) |

## MARKING DIAGRAMS

TO-220
THREE LEAD
T SUFFIX
CASE 221A
$D^{2}$ PAK
3-PIN DP SUFFIX CASE 418E


PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D2PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 3.5 | 3.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J A}=\mathrm{R}_{\Theta J C}+\mathrm{R}_{\Theta C A}$


## CS5253-1

### 3.0 A LDO 5-Pin Adjustable Linear Regulator

This new very low dropout linear regulator reduces total power dissipation in the application. To achieve very low dropout, the internal pass transistor is powered separately from the control circuitry. Furthermore, with the control and power inputs tied together, this device can be used in single supply configuration and still offer a better dropout voltage than conventional PNP-NPN based LDO regulators. In this mode the dropout is determined by the minimum control voltage.

The CS5253-1 is offered in a five-terminal D ${ }^{2}$ PAK package, which allows for the implementation of a remote-sense pin permitting very accurate regulation of output voltage directly at the load, where it counts, rather than at the regulator. This remote sensing feature virtually eliminates output voltage variations due to load changes and resistive voltage drops. Typical load regulation measured at the sense pin is less than 1.0 mV for an output voltage of 2.5 V with a load step of 10 mA to 3.0 A .

The CS5253-1 has a very fast transient loop response which can be adjusted using a small capacitor on the Adjust pin.

Internal protection circuitry provides for "bust-proof" operation, similar to three-terminal regulators. This circuitry, which includes overcurrent, short circuit, and overtemperature protection will self protect the regulator under all fault conditions.

The CS5253-1 is ideal for generating a 2.5 V supply to power graphics controllers used on VGA cards.

## Features

- V
- $V_{\text {POWER }}$ Dropout < 0.40 V @ 3.0 A
- $\mathrm{V}_{\text {CONTROL }}$ Dropout < 1.05 V @ 3.0 A
- $1.0 \%$ Trimmed Reference
- Fast Transient Response
- Remote Voltage Sensing
- Thermal Shutdown
- Current Limit
- Short Circuit Protection
- Drop-In Replacement for EZ1582
- Backwards Compatible with 3-Pin Regulators
- Very Low Dropout Reduces Total Power Consumption

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device Package Shipping <br> CS5253-1GDP5 D$^{2}$ PAK $^{*}$ 50 Units/Rail <br> CS5253-1GDPR5 D $^{2}$ PAK $^{*}$ 750 Tape \& Reel |
| :--- |
| *5-Pin. |



Figure 1. Application Diagram

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| V ${ }_{\text {POWER }}$ Input Voltage |  | 6.0 | V |
| $\mathrm{V}_{\text {CONTROL }}$ Input Voltage |  | 13 | V |
| Operating Junction Temperature Range, $\mathrm{T}_{J}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold |  | 2.0 | kV |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} ; \mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\mathrm{OUT}}\right.$ and $\mathrm{V}_{\text {ADJ }}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5253-1 |  |  |  |  |  |
| Reference Voltage | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \text {, } \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \text { to } 3.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.237 \\ (-1.0 \%) \end{gathered}$ | 1.250 | $\begin{gathered} 1.263 \\ (+1.0 \%) \end{gathered}$ | V |
| Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.5 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=1.75 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \end{aligned}$ | - | 0.02 | 0.2 | \% |
| Load Regulation | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V} \text {, } \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \text { to } 3.0 \mathrm{~A} \text {, with Remote Sense } \end{aligned}$ | - | 0.04 | 0.3 | \% |
| Minimum Load Current (Note 2) | $\mathrm{V}_{\text {CONTROL }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.3 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=+1.0 \%$ | - | 5.0 | 10 | mA |
| Control Pin Current (Note 3) | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}$, IOUT $=100 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=3.0 \mathrm{~A}$ | - | $\begin{aligned} & 6.0 \\ & 35 \end{aligned}$ | $\begin{gathered} 10 \\ 120 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Adjust Pin Current | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 60 | 120 | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=-1.0 \%$ | 3.1 | 4.0 | - | A |
| Short Circuit Current | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | 2.0 | 3.5 | - | A |
| Ripple Rejection (Note 4) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=\mathrm{V}_{\text {POWER }}=3.25 \mathrm{~V}, \mathrm{~V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {P-P }} @ \\ & 120 \mathrm{~Hz}, \mathrm{I}_{\text {OUT }}=4.0 \mathrm{~A}, \mathrm{C}_{\text {ADJ }}=0.1 \mu \mathrm{~F} \end{aligned}$ | 60 | 80 | - | dB |

2. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum load current requirement.
3. The $\mathrm{V}_{\text {CONTROL }}$ pin current is the drive current required for the output transistor. This current will track output current with roughly a $1: 100$ ratio. The minimum value is equal to the quiescent current of the device.
4. This parameter is guaranteed by design and is not $100 \%$ production tested.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}\right.$; $\mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\text {OUT }}$ and $\mathrm{V}_{\text {ADJ }}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5253-1 |  |  |  |  |  |
| Thermal Regulation | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | - | \%/W |
| $V_{\text {CONTRoL }}$ Dropout Voltage (Minimum $\left.\mathrm{V}_{\text {CONTROL }}-\mathrm{V}_{\text {OUT }}\right)$ (Note 5) | $\begin{aligned} & \mathrm{V}_{\text {POWER }}=2.05 \mathrm{~V}, \text { IOUT } \\ & \mathrm{V}_{\text {POWER }}=2.05 \mathrm{~V}, \text { IOUT }=1.0 \mathrm{~mA} \\ & \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \text { IOUT } \end{aligned}=3.0 \mathrm{~A}$ | - | $\begin{aligned} & 0.90 \\ & 1.00 \\ & 1.05 \end{aligned}$ | $\begin{aligned} & 1.15 \\ & 1.15 \\ & 1.30 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \\ & \text { V } \end{aligned}$ |
| $V_{\text {POWER }}$ Dropout Voltage (Minimum $\mathrm{V}_{\text {POWER }}-\mathrm{V}_{\text {OUT }}$ ) (Note 5) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \text { I IOUT }=100 \mathrm{~mA} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=1.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=3.0 \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 0.05 \\ & 0.15 \\ & 0.40 \end{aligned}$ | $\begin{aligned} & 0.15 \\ & 0.25 \\ & 0.60 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| RMS Output Noise | Freq $=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Temperature Stability | - | 0.5 | - | - | \% |
| Thermal Shutdown (Note 6) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {CONTROL }}$ Supply Only Output Current | $\mathrm{V}_{\text {CONTROL }}=13 \mathrm{~V}$, $\mathrm{V}_{\text {POWER }}$ Not Connected, $\mathrm{V}_{\mathrm{ADJ}}=\mathrm{V}_{\mathrm{OUT}}=\mathrm{V}_{\mathrm{SENSE}}=0 \mathrm{~V}$ | - | - | 50 | mA |
| VPower Supply Only Output Current | $\begin{aligned} & \mathrm{V}_{\text {POWER }}=6.0 \mathrm{~V}, \mathrm{~V}_{\text {CONTROL }} \text { Not Connected, } \\ & \mathrm{V}_{\text {ADJ }}=\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SENSE }}=0 \mathrm{~V} \end{aligned}$ | - | 0.1 | 1.0 | mA |

5. Dropout is defined as either the minimum control voltage ( $\mathrm{V}_{\text {CONTROL }}$ ) or minimum power voltage ( $\mathrm{V}_{\text {POWER }}$ ) to output voltage differential required to maintain $1.0 \%$ regulation at a particular load current.
6. This parameter is guaranteed by design, but not parametrically tested in production. However, a $100 \%$ thermal shutdown functional test is performed on each part.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| D2PAK | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\text {SENSE }}$ | This Kelvin sense pin allows for remote sensing of the output voltage at the load for improved regulation. It is internally connected to the positive input of the voltage sensing error amplifier. |
| 2 | Adjust | This pin is connected to the low side of the internally trimmed $1.0 \%$ bandgap reference voltage and carries a bias current of about $50 \mu \mathrm{~A}$. A resistor divider from Adjust to $\mathrm{V}_{\text {OUT }}$ and from Adjust to ground sets the output voltage. Also, transient response can be improved by adding a small bypass capacitor from this pin to ground. |
| 3 | $\mathrm{V}_{\text {OUT }}$ | This pin is connected to the emitter of the power pass transistor and provides a regulated voltage capable of sourcing 3.0 A of current. |
| 4 | V ${ }_{\text {CONTROL }}$ | This is the supply voltage for the regulator control circuitry. For the device to regulate, this voltage should be between 0.9 V and 1.3 V (depending on the output current) greater than the output voltage. The control pin current will be about $1.0 \%$ of the output current. |
| 5 | $V_{\text {POWER }}$ | This is the power input voltage. This pin is physically connected to the collector of the power pass transistor. For the device to regulate, this voltage should be between 0.1 V and 0.6 V greater than the output voltage depending on the output current. The output load current of 3.0 A is supplied through this pin. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Reference Voltage vs Junction Temperature

Figure 5. Transient Response


Figure 4. Load Regulation vs Output Current

Figure 6. Output Current vs $\mathrm{V}_{\text {POWER }}$ - $\mathrm{V}_{\text {OUT }}$


Figure 7. Adjust Pin Current vs Junction Temperature


Figure 9. Short Circuit Output Current vs Junction Temperature


Figure 11. V control Only Output Current vs Junction Temperature


Figure 8. Minimum Load Current vs $\mathrm{V}_{\text {CONTROL }}-\mathrm{V}_{\text {OUT }}$


Figure 10. Ripple Rejection vs Frequency


Figure 12. $\mathrm{V}_{\text {control }}$ Dropout Voltage vs Output Current


Figure 13. VPOWER Dropout Voltage vs Output Current


Figure 15. VPOWER Only Output Current vs Junction Temperature


Figure 17. Current Limit vs $V_{\text {OUT }}$


Figure 14. Minimum Load Current vs $\mathrm{V}_{\text {POWER }}$ - $\mathrm{V}_{\text {OUT }}$


Figure 16. VCONTROL Supply Current vs Junction Temperature


Figure 18. Stability vs ESR

## APPLICATIONS NOTES

## THEORY OF OPERATION

The CS5253-1 linear regulator provides adjustable voltages from 1.26 V to 5.0 V at currents up to 3.0 A . The regulator is protected against short circuits, and includes a thermal shutdown circuit with hysteresis. The output, which is current limited, consists of a PNP-NPN transistor pair and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## $V_{\text {Power }}$ Function

The CS5253-1 utilizes a two supply approach to maximize efficiency. The collector of the power device is brought out to the $V_{\text {POWER }}$ pin to minimize internal power dissipation under high current loads. $\mathrm{V}_{\text {CONTROL }}$ provides for the control circuitry and the drive for the output NPN transistor. $\mathrm{V}_{\text {CONTROL }}$ should be at least 1.0 V greater than the output voltage. Special care has been taken to ensure that there are no supply sequencing problems. The output voltage will not turn on until both supplies are operating. If the control voltage comes up first, the output current will be limited to about three milliamperes until the power input voltage comes up. If the power input voltage comes up first, the output will not turn on at all until the control voltage comes up. The output can never come up unregulated.

The CS5253-1 can also be used as a single supply device with the control and power inputs tied together. In this mode, the dropout will be determined by the minimum control voltage.

## Output Voltage Sensing

The CS5253-1 five terminal linear regulator includes a dedicated $\mathrm{V}_{\text {SENSE }}$ function. This allows for true Kelvin sensing of the output voltage. This feature can virtually eliminate errors in the output voltage due to load regulation. Regulation will be optimized at the point where the sense pin is tied to the output.

## DESIGN GUIDELINES

## Adjustable Operation

This LDO adjustable regulator has an output voltage range of 1.26 V to 5.0 V . An external resistor divider sets the output voltage as shown in Figure 19. The regulator's voltage sensing error amplifier maintains a fixed 1.260 V reference between the output pin and the adjust pin.


Figure 19. Typical Application Schematic. The Resistor Divider Sets $\mathrm{V}_{\text {OUT }}$, With the Internal 1.260 V Reference Dropped Across R1.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.260 V across R1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of V VUT is necessary. The output voltage is set according to the formula:

$$
\mathrm{V} \text { OUT }=1.260 \mathrm{~V} \times \frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}+\mathrm{R} 2 \times \mathrm{I} \mathrm{ADJ}
$$

The term $\mathrm{I}_{\mathrm{ADJ}} \times \mathrm{R} 2$ represents the error added by the adjust pin current. R1 is chosen so that the minimum load current is at least $10 \mathrm{~mA} . \mathrm{R} 1$ and R 2 should be of the same composition for best tracking over temperature. The divider resistors should be placed physically as close to the load as possible.

While not required, a bypass capacitor connected between the adjust pin and ground will improve transient response and ripple rejection. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Value and type may be varied to optimize performance vs. price.

## Other Adjustable Operation Considerations

The CS5253-1 linear regulator has an absolute maximum specification of 6.0 V for the voltage difference between $\mathrm{V}_{\text {Power }}$ and $\mathrm{V}_{\text {OUT }}$. However, the IC may be used to regulate voltages in excess of 6.0 V . The two main
considerations in such a design are the sequencing of power supplies and short circuit capability.

Power supply sequencing should be such that the $\mathrm{V}_{\text {CONTROL }}$ supply is brought up coincidentally with or before the $\mathrm{V}_{\text {POWER }}$ supply. This allows the IC to begin charging the output capacitor as soon as the VPOWER to $V_{\text {OUT }}$ differential is large enough that the pass transistor conducts. As VPOWER increases, the pass transistor will remain in dropout, and current is passed to the load until $\mathrm{V}_{\text {OUT }}$ is in regulation. Further increase in the supply voltage brings the pass transistor out of dropout. In this manner, any output voltage less than 13 V may be regulated, provided the $V_{\text {POWER }}$ to $V_{\text {OUT }}$ differential is less than 6.0 V. In the case where $\mathrm{V}_{\text {CONTROL }}$ and $\mathrm{V}_{\text {POWER }}$ are shorted, there is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {POWER }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 6.0 V is not exceeded.

There is a possibility of damaging the IC when VPOWER - V VUT is greater than 6.0 V if a short circuit occurs. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Overvoltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp the $\mathrm{V}_{\text {POWER }}$ to $\mathrm{V}_{\text {OUT }}$ differential to less than 6.0 V if fail safe operation is required. One possible clamp circuit is illustrated in Figure 20; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit condition indefinitely while protecting the IC.


Figure 20. This Circuit Is an Example of How the CS5253-1 Can Be Short-Circuit Protected When Operating With $\mathrm{V}_{\mathrm{OUT}}>6.0 \mathrm{~V}$

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: loop stability, start-up delay, and load transient response. Different capacitor types vary widely in tolerance, ESR (equivalent
series resistance), ESL (equivalent series inductance), and variation over temperature. Tantalum and aluminum electrolytic capacitors work best, with electrolytic capacitors being less expensive in general, but varying more in capacitor value and ESR over temperature.
The CS5253-1 requires an output capacitor to guarantee loop stability. The Stability vs ESR graph in the typical performance section shows the minimum ESR needed to guarantee stability, but under ideal conditions. These include: having $\mathrm{V}_{\text {OUT }}$ connected to $\mathrm{V}_{\text {SENSE }}$ directly at the IC pins; the compensation capacitor located right at the pins with a minimum lead length; the adjust feedback resistor divider ground, (bottom of R2 in Figure 19), connected right at the capacitor ground; and with power supply decoupling capacitors located close to the IC pins. The actual performance will vary greatly with board layout for each application. In particular, the use of the remote sensing feature will require a larger capacitor with less ESR. For most applications, a minimum of $33 \mu \mathrm{~F}$ tantalum or $150 \mu \mathrm{~F}$ aluminum electrolytic, with an ESR less than $1.0 \Omega$ over temperature, is recommended. Larger capacitors and lower ESR will improve stability.

The load transient response, during the time it takes the regulator to respond, is also determined by the output capacitor. For large changes in load current, the ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{ESR}
$$

There is then an additional drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{T} / \mathrm{C}
$$

where T is the time for the regulation loop to begin to respond. The very fast transient response time of the CS5253-1 allows the ESR effect to dominate. For microprocessor applications, it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best transient response.

## Protection Diodes

When large external capacitors are used with a linear regulator, it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage, and the rate at which $\mathrm{V}_{\text {CONTROL }}$ drops. In the CS5253-1 regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 21 is recommended.


Figure 21. Diode Protection Circuit
A rule of thumb useful in determining if a protection diode is required is to solve for current:

$$
I=\frac{C \times V}{T}
$$

where:
I is the current flow out of the load capacitance when $\mathrm{V}_{\text {CONTROL }}$ is shorted,
C is the value of load capacitance
V is the output voltage, and
T is the time duration required for $\mathrm{V}_{\mathrm{CONTROL}}$ to transition from high to being shorted.
If the calculated current is greater than or equal to the typical short circuit current value provided in the specifications, serious thought should be given to the use of a protection diode.

## Current Limit

The internal current limit circuit limits the output current under excessive load conditions.

## Short Circuit Protection

The device includes short circuit protection circuitry that clamps the output current at approximately 500 mA less than its current limit value. This provides for a current foldback function, which reduces power dissipation under a direct shorted load.

## Thermal Shutdown

The thermal shutdown circuitry is guaranteed by design to activate above a die junction temperature of approximately $150^{\circ} \mathrm{C}$ and to shut down the regulator output. This circuitry has $25^{\circ} \mathrm{C}$ of typical hysteresis, thereby allowing the regulator to recover from a thermal fault automatically.

## Calculating Power Dissipation and Heat Sink Requirements

High power regulators such as the CS5253-1 usually operate at high junction temperatures. Therefore, it is
important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used. Since the package tab is connected to $\mathrm{V}_{\text {OUT }}$ on the CS5253-1, electrical isolation may be required for some applications. Also, as with all high power packages, thermal compound in necessary to ensure proper heat flow. For added safety, this high current LDO includes an internal thermal shutdown circuit

The thermal characteristics of an IC depend on the following four factors: junction temperature, ambient temperature, die power dissipation, and the thermal resistance from the die junction to ambient air. The maximum junction temperature can be determined by:

$$
\mathrm{T}_{\mathrm{J}(\max )}=\mathrm{T}_{\mathrm{A}(\max )}+\mathrm{PD}_{(\max )} \times \mathrm{R}_{\Theta \mathrm{JA}}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type. The maximum power dissipation for a regulator is:

$$
\begin{aligned}
\mathrm{PD}_{(\max )}= & \left(\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{V}_{\mathrm{OUT}(\text { min })}\right) \mathrm{I}_{\mathrm{OUT}}(\text { max }) \\
& +\mathrm{V}_{\mathrm{IN}(\text { max })} \times \mathrm{I}_{\mathrm{IN}(\text { max })}
\end{aligned}
$$

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment has a thermal resistance which is measured in degrees per watt. Like series electrical resistances, these thermal resistances are summed to determine the total thermal resistance between the die junction and the surrounding air, $\mathrm{R}_{\Theta \mathrm{JA}}$. This total thermal resistance is comprised of three components. These resistive terms are measured from junction to case ( $\mathrm{R}_{\Theta J C}$ ), case to heat $\operatorname{sink}\left(\mathrm{R}_{\Theta C S}\right)$, and heat sink to ambient air $\left(\mathrm{R}_{\Theta S A}\right)$. The equation is:

$$
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A}
$$

The value for $\mathrm{R}_{\mathrm{QJC}}$ is $2.5^{\circ} \mathrm{C} /$ watt for the CS5253-1 in the $D^{2}$ PAK package. For a high current regulator such as the CS5253-1 the majority of heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while the $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see our application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

CS5253-1

PACKAGE THERMAL DATA

| Parameter |  | D $^{2}$ PAK, 5-Pin | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$.

## CS5204-2

### 4.0 A, 1.5 V Fixed Linear Regulator

The CS5204-2 linear regulator provides $4.0 \mathrm{~A} @ 1.5 \mathrm{~V}$ with an accuracy of $\pm 2.0 \%$.

The fast loop response and low dropout voltage make this regulator ideal for GTL bus termination where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulator is fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The regulator is available in TO-220 and surface mount $\mathrm{D}^{2}$ packages.

## Features

- Output Current to 4.0 A
- Output Voltage Trimmed to $\pm 2.0 \%$
- Dropout Voltage (typical) 1.10 V @ 4.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram

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MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
YY, $Y$ = Year
WW, W = Work Week
ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5204-2GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5204-2GDP3 | D$^{2}$ PAK $\dagger$ | 50 Units/Rail |
| CS5204-2GDPR3 | D$^{2}$ PAK $\dagger$ | 750 Tape \& Reel |

*Additional ordering information can be found on page 705 of this data sheet.
† TO-220 are all 3-pin, straight leaded. D²PAK are all 3-pin.

## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {CC }}$ |  | 17 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak <br> 230 Peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathbb{I N}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }} \leq 10 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=4.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |


| Output Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \\ & 0 \leq \mathrm{I}_{\mathrm{OUT}} \leq 4.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.47 \\ (-2.0 \%) \end{gathered}$ | 1.50 | $\begin{gathered} 1.53 \\ (+2.0 \%) \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 4.0 \mathrm{~A}$ | - | 0.05 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=4.0 \mathrm{~A}$ | - | 1.1 | 1.2 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=15 \mathrm{~V} \end{aligned}$ | $4.5$ | $\begin{aligned} & 8.5 \\ & 2.5 \end{aligned}$ | - | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{Pulse}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%/W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; $\mathrm{l}_{\text {OUT }}=4.0 \mathrm{~A}$ | - | 75 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise (\%V $\mathrm{V}_{\text {OUT }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | - | 0.003 | - | \% $\mathrm{N}_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |
| :---: | :---: | :---: | :--- |
| TO-220 | D $^{2}$ PAK | Pin Symbol |  |
| 1 | 1 | GND | Ground connection. |
| 2 | 2 | V OUT | Regulated output voltage (case). |
| 3 | 3 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Dropout Voltage vs. Output Current


Figure 4. Load Regulation vs. Output Current


Figure 3. Reference Voltage vs. Temperature


Figure 5. Minimum Load Current


Figure 6. Ripple Rejection vs. Frequency

## APPLICATIONS INFORMATION

The CS5204-2 linear regulator provides fixed 1.5 V voltage at currents up to 4.0 A . The regulator is protected against short circuit, and includes thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increase.

The CS5204-2 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5204-2 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5204-2 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 7 is recommended.


Figure 7. Protection Diode Scheme

## Output Voltage Sensing

Since the CS5204-2 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the regulator should be connected as shown in Figure 8.


Figure 8. Conductor Parasitic Resistance Effects Can Be Minimized With the Above Grounding Scheme

## Calculating Power Dissipation and Heat Sink Requirements

The CS5204-2 linear regulator includes thermal shutdown and safe operating area circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V VUT on the CS5204-2, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{25}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta \mathrm{SA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{27}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (25).
$\mathrm{R}_{\Theta \mathrm{JC}}$ is $1.6^{\circ} \mathrm{C} / \mathrm{Watt}$ for the CS5204-2. For a high current regulator such as the CS5204-2 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

## ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5204-2GT3 | $4.0 \mathrm{~A}, 1.5 \mathrm{~V}$ Output | TO-220 THREE LEAD, STRAIGHT |
| CS5204-2GDP3 | $4.0 \mathrm{~A}, 1.5$ V Output | D$^{2}$ PAK 3-PIN |
| CS5204-2GDPR3 | $4.0 \mathrm{~A}, 1.5$ V Output | D$^{2}$ PAK 3-PIN (Tape \& Reel) |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D$^{2}$ PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\Theta J C}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$


## CS5204-1, CS5204-3, CS5204-5

### 4.0 A Adjustable, and 3.3 V and 5.0 V Fixed Linear Regulators

The CS5204-x series of linear regulators provides 4.0 A at adjustable and fixed voltages with an accuracy of $\pm 1.0 \%$ and $\pm 2.0 \%$ respectively. The adjustable version uses two external resistors to set the output voltage within a 1.25 V to 13 V range.

The regulators are intended for use as post regulators and microprocessor supplies. The fast loop response and low dropout voltage make these regulators ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulators are fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The regulators are available in TO-220 and surface mount $\mathrm{D}^{2} \mathrm{PAK}$ packages.

## Features

- Output Current to 4.0 A
- Output Trimmed to $\pm 1.0 \%$
- Dropout Voltage 1.10 V @ 4.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram - CS5204-1


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


MARKING DIAGRAMS


ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5204-1GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5204-1GDP3 | D2PAK $\dagger$ | 50 Units/Rail |
| CS5204-1GDPR3 | D2PAK $\dagger$ | 750 Tape \& Reel |
| CS5204-3GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5204-3GDP3 | D2PAK $\dagger$ | 50 Units/Rail |
| CS5204-3GDPR3 | D2PAK $\dagger$ | 750 Tape \& Reel |
| CS5204-5GT3 | TO-220 $\dagger$ | 50 Units/Rail |

*Additional ordering information can be found on page 713 of this data sheet
$\dagger$ TO-220 is 3 -pin, straight leaded. $D^{2}$ PAK are all 3 -pin.


Figure 2. Block Diagram - CS5204-3, -5

## ABSOLUTE MAXIMUM RATINGS*

|  | Parameter | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage, $V_{\text {CC }}$ |  | 17 | $\mathrm{~V}^{\circ}$ |
| Operating Temperature Range | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |  |
| Junction Temperature | Wave Solder (through hole styles only) Note 1 |  |  |
| Seflow (SMD styles only) Note 2 | 260 Peak <br> 230 Peak | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering: |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\text {IN }}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }} \leq 15 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=4.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Adjustable Output Voltage (CS5204-1)

| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}, \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 4.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 1.241 \\ & (-1 \%) \end{aligned}$ | 1.254 | $\begin{aligned} & 1.266 \\ & (+1 \%) \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; I ${ }_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 4.0 \mathrm{~A}$ | - | 0.05 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=4.0 \mathrm{~A}$ | - | 1.1 | 1.2 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $4.5$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | - | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Minimum Load Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=7.0 \mathrm{~V}$ | - | 1.2 | 6.0 | mA |
| Adjust Pin Current | - | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjust Pin Current Change | $\begin{gathered} 1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 4.0 \mathrm{~V} ; \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 4.0 \mathrm{~A} \end{gathered}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{pulse;} \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%/W |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
4. Specifictions apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## CS5204-1, CS5204-3, CS5204-5

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 15 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=4.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Adjustable Output Voltage (CS5204-1) (continued)

| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{C}_{\mathrm{Adj}}=25 \mu \mathrm{~F} ;$ IOUT $=4.0 \mathrm{~A}$ | - | 82 | - | dB |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Temperature Stability | - | - | 0.5 | - | $\%$ |
| RMS Output Noise | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | $\% \mathrm{~V}_{\mathrm{OUT}}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}$ Tantalum, $\mathrm{V}_{\mathrm{IN}^{\prime}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 10 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{l}_{\text {full load }}=4.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Fixed Output Voltage (CS5204-3, CS5204-5)

| Reference Voltage (Notes 6 and 7) $\begin{aligned} & \text { CS5204-5 } \\ & \text { CS5204-3 } \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 0 \leq \mathrm{IOUT} \leq 4.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 0 \leq \mathrm{IOUT} \leq 4.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 4.9(-2 \%) \\ 3.234(-2 \%) \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 3.3 \end{aligned}$ | $\begin{gathered} 5.1(+2 \%) \\ 3.366(+2 \%) \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; I $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 6 and 7) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 4.0 \mathrm{~A}$ | - | 0.05 | 0.4 | \% |
| Dropout Voltage (Note 8) | $\mathrm{I}_{\text {OUT }}=4.0 \mathrm{~A}$ | - | 1.1 | 1.2 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $4.5$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | $-$ | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{pulse;} \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%/W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; lout $=4.0 \mathrm{~A}$ | - | 75 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise (\%V ${ }_{\text {OUT }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

6. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
7. Specifictions apply for an external Kelvin sense connection atr a point on the output pin $1 / 4$ " from the bottom of the package.
8. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  | Pin Symbol | Function |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5204-1 |  | CS5204-3, -5 |  |  |  |
| D2PAK | TO-220 | D2PAK | TO-220 |  |  |
| 1 | 1 | N/A | N/A | Adj | Adjust pin (low side of the internal reference). |
| 2 | 2 | 2 | 2 | $\mathrm{V}_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | 3 | 3 | 3 | $\mathrm{V}_{\mathrm{IN}}$ | Input voltage. |
| N/A | N/A | 1 | 1 | GND | Ground connection. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 7. Adjust Pin Current vs. Temperature


Figure 4. Reference Voltage vs. Temperature


Figure 6. Minimum Load Current


Figure 8. Ripple Rejection vs. Frequency (Fixed Versions)


Figure 9. Ripple Rejection vs. Frequency (Adjustable Versions)

## APPLICATIONS INFORMATION

The CS5204-x family of linear regulators provides fixed or adjustable voltages at currents up to 4.0 A . The regulators are protected against short circuit, and include thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increases.

The CS5204-x has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The adjustable regulator (CS5204-1) has an output voltage range of 1.25 V to 13 V . An external resistor divider sets the output voltage as shown in Figure 10. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.

The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{R E F} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{A d j} \times R 2
$$

The term $\mathrm{I}_{\text {Adj }} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R1 is chosen so that the minimum load current is at least 10 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. The adjust pin is bypassed to improve the transient response and ripple rejection of the regulator.


Figure 10. Resistor Divider Scheme for the Adjustable Version

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet provides this information.
A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5204-x the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current.

The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under load transient conditions. The output capacitor network should be as close as possible to the load for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\mathrm{IN}}$ drops. In the CS5204-x family of linear regulators, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figures 11 and 12 is recommended.


Figure 11. Protection Diode Scheme for Adjustable Output Regulator


Figure 12. Protection Diode Scheme for Fixed Output Regulators

## Output Voltage Sensing

Since the CS5204-x is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the fixed regulators should be connected as shown in Figure 13.


Figure 13. Conductor Parasitic Resistance can be Minimized with the Above Grounding Scheme for Fixed Output Regulators

For the adjustable regulator, the best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 14. If R1 is connected to the load, $\mathrm{R}_{\mathrm{C}}$ is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes

$$
\mathrm{RC} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 14. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitics

## Calculating Power Dissipation and Heat Sink Requirements

The CS5204-x series of linear regulators includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V VUT on the CS5204-x, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{28}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:
$P_{D}($ max $)=\left\{V_{I N}(\right.$ max $)-V_{O U T}($ min $\left.)\right\} I_{O U T}($ max $)+V_{I N(m a x)}{ }^{l Q}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S \mathrm{~A}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{30}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (28).

The value for $\mathrm{R}_{\Theta J C}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS5204-x the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part Number | Type | Description |
| :---: | :---: | :---: |
| CS5204-1GT3 | 4.0 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |
| CS5204-1GDP3 | 4.0 A, Adj. Output | D2PAK 3-PIN |
| CS5204-1GDPR3 | 4.0 A, Adj. Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5204-3GT3 | 4.0 A, 3.3 V Output | TO-220 THREE LEAD, STRAIGHT |
| CS5204-3GDP3 | 4.0 A, 3.3 V Output | D2PAK 3-PIN |
| CS5204-3GDPR3 | 4.0 A, 3.3 V Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5204-5GT3 | 4.0 A, 5.0 V Output | TO-220 THREE LEAD, STRAIGHT |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D2PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J \mathrm{~A}}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta C A}$


## CS5205-2

### 5.0 A, 1.5 V Fixed Linear Regulator

The CS5205-2 linear regulator provides 5.0 A @ 1.5 V with an accuracy of $\pm 2.0 \%$.

The regulator is intended for use as an active termination for the GTL bus on Intel based motherboards. The fast loop response and low dropout voltage make these regulators ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulator is fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The CS5205-2 is available in TO-220 and surface mount $\mathrm{D}^{2}$ packages.

## Features

- Output Current to 5.0 A
- Output Voltage Trimmed to $\pm 2.0 \%$
- Dropout Voltage 1.2 V @ 5.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
YY, $Y$ = Year
WW, W = Work Week
ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5205-2GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5205-2GDP3 | D$^{2}$ PAK $\dagger$ | 50 Units/Rail |
| CS5205-2GDPR3 | D$^{2}$ PAK $\dagger$ | 750 Tape \& Reel |

*Additional ordering information can be found on page 719 of this data sheet.
$\dagger$ TO-220 are all $3-$ pin, straight leaded. D2PAK are all 3-pin.

## MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {CC }}$ |  | 17 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak 230 Peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathbb{I N}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }} \leq 10 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=5.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Fixed Output Voltage

| Output Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \\ & 0 \leq \mathrm{I}_{\text {OUT }} \leq 5.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.47 \\ (-2.0 \%) \end{gathered}$ | 1.50 | $\begin{gathered} 1.53 \\ (+2.0 \%) \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; I OUT $=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 5.0 \mathrm{~A}$ | - | 0.08 | 0.40 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=5.0 \mathrm{~A}$ | - | 1.2 | 1.3 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $5.5$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | - | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%/W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; lout $=5.0 \mathrm{~A}$ | - | 75 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise (\%V ${ }_{\text {OUT }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | - | 0.003 | - | $\% N_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  | Function |
| :---: | :---: | :---: | :--- | :--- |
| TO-220 | D$^{2}$ PAK | Pin Symbol |  |  |
| 1 | 1 | GND | Ground connection. |  |
| 2 | 2 | V $_{\text {OUT }}$ | Regulated output voltage (case). |  |
| 3 | 3 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |  |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Dropout Voltage vs. Output Current


Figure 4. Load Regulation vs. Output Current


Figure 3. Reference Voltage vs. Temperature


Figure 5. Minimum Load Current


Figure 6. Ripple Rejection vs. Frequency (Fixed Versions)

## APPLICATIONS INFORMATION

The regulator is protected against short circuit, and includes thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increase.

The CS5205-2 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5205-2 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5205-2 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 7 is recommended.


Figure 7. Protection Diode Scheme for Fixed Output Regulators

## Output Voltage Sensing

Since the CS5205-2 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the regulator should be connected as shown in Figure 8.


Figure 8. Conductor Parasitic Resistance Effects Can Be Minimized With the Above Grounding Scheme for Fixed Output Regulators

## Calculating Power Dissipation and Heat Sink Requirements

The CS5205-2 includes thermal shutdown and safe operating area circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to VOUT on the CS5205-2, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $P_{D}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{31}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta \mathrm{SA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{33}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (31).
$\mathrm{R}_{\Theta \mathrm{JC}}$ is $1.6^{\circ} \mathrm{C} /$ Watt for the CS5205-2. For a high current regulator such as the CS5205-2 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

## ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5205-2GT3 | 5.0 A, 1.5 V Output | TO-220 THREE LEAD, STRAIGHT |
| CS5205-2GDP3 | 5.0 A, 1.5 V Output | D23PAK 3-PIN |
| CS5205-2GDPR3 | 5.0 A, 1.5 V Output | D23AK 3-PIN (Tape \& Reel) |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D$^{2}$ PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\Theta J C}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$


## CS5205-1, CS5205-3, CS5205-5

### 5.0 A Adjustable, and 3.3 V and 5.0 V Fixed Linear Regulators

The CS5205-x series of linear regulators provides 5.0 A at adjustable and fixed voltages with an accuracy of $\pm 1.0 \%$ and $\pm 2.0 \%$ respectively. The adjustable version uses two external resistors to set the output voltage within a 1.25 V to 13 V range.

The regulators are intended for use as post regulators and microprocessor supplies. The fast loop response and low dropout voltage make these regulators ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulators are fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The CS5205-x is pin compatible with the LT1084 family of linear regulators but has lower dropout voltage.

The regulators are available in TO-220 and surface mount $\mathrm{D}^{2} \mathrm{PAK}$ packages.

## Features

- Output Current to 5.0 A
- Output Trimmed to $\pm 1.0 \%$
- Dropout Voltage 1.2 V @ 5.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram - CS5205-1


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
YY, $Y$ = Year
WW, W = Work Week

## ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5205-1GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5205-1GDP3 | D$^{2}$ PAK $\dagger$ | 50 Units/Rail |
| CS5205-1GDPR3 | D$^{2}$ PAK $\dagger$ | 750 Tape \& Reel |
| CS5205-3GT3 | TO-220 $\dagger$ | 50 Units/Rail |
| CS5205-3GDP3 | D$^{2}$ PAK $\dagger$ | 50 Units/Rail |
| CS5205-3GDPR3 | D$^{2}$ PAK $\dagger$ | 750 Tape \& Reel |
| CS5205-5GT3 | TO-220 $\dagger$ | 50 Units/Rail |

[^13]

Figure 2. Block Diagram - CS5205-3, -5

## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ |  | 17 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak 230 Peak | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathbb{I N}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }} \leq 15 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=5.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Adjustable Output Voltage (CS5205-1)

| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}, \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 5.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 1.241 \\ & (-1 \%) \end{aligned}$ | 1.254 | $\begin{aligned} & 1.266 \\ & (+1 \%) \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; I IOUT $=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 5.0 \mathrm{~A}$ | - | 0.08 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{l}_{\text {OUT }}=5.0 \mathrm{~A}$ | - | 1.2 | 1.3 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $5.5$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | - | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Minimum Load Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=7.0 \mathrm{~V}$ | - | 1.2 | 6.0 | mA |
| Adjust Pin Current | - | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjust Pin Current Change | $\begin{gathered} 1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 4.0 \mathrm{~V} ; \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 5.0 \mathrm{~A} \end{gathered}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{pulse;} \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%W |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
4. Specifictions apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## CS5205-1, CS5205-3, CS5205-5

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}$ Tantalum, $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 15 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=5.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Adjustable Output Voltage (CS5205-1) (continued)

| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{C}_{\mathrm{Adj}}=25 \mu \mathrm{~F} ; \mathrm{IOUT}=5.0 \mathrm{~A}$ | - | 82 | - | dB |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Temperature Stability | - | - | 0.5 | - | $\%$ |
| RMS Output Noise | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | $\% \mathrm{~V}_{\mathrm{OUT}}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}$ Tantalum, $\mathrm{V}_{\mathrm{IN}^{\prime}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 10 \mathrm{~V}$,
$0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{l}_{\text {full load }}=5.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Fixed Output Voltage (CS5205-3, CS5205-5)

| Reference Voltage (Notes 6 and 7) $\begin{aligned} & \text { CS5205-5 } \\ & \text { CS5205-3 } \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 0 \leq \mathrm{IOUT} \leq 5.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 0 \leq \mathrm{IOUT} \leq 5.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 4.9(-2 \%) \\ 3.234(-2 \%) \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 3.3 \end{aligned}$ | $\begin{gathered} 5.1 \text { (+2\%) } \\ 3.366 \text { (+2\%) } \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; I l OUT $=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 6 and 7) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 5.0 \mathrm{~A}$ | - | 0.08 | 0.40 | \% |
| Dropout Voltage (Note 8) | $\mathrm{l}_{\text {OUT }}=5.0 \mathrm{~A}$ | - | 1.2 | 1.3 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{J} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $5.5$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | - | $\begin{aligned} & \mathrm{A} \\ & \mathrm{~A} \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{pulse;} \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\text {OUT }}=5.0 \mathrm{~A}$ | - | 75 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise (\%V ${ }_{\text {Out }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

6. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
7. Specifictions apply for an external Kelvin sense connection atr a point on the output pin $1 / 4$ " from the bottom of the package.
8. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  | Pin Symbol | Function |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5205-1 |  | CS5205-3, -5 |  |  |  |
| D2PAK | TO-220 | D2PAK | TO-220 |  |  |
| 1 | 1 | N/A | N/A | Adj | Adjust pin (low side of the internal reference). |
| 2 | 2 | 2 | 2 | $V_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | 3 | 3 | 3 | $\mathrm{V}_{\text {IN }}$ | Input voltage. |
| N/A | N/A | 1 | 1 | GND | Ground connection. |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 7. Adjust Pin Current vs. Temperature


Figure 4. Reference Voltage vs. Temperature


Figure 6. Minimum Load Current


Figure 8. Ripple Rejection vs. Frequency (Fixed Versions)


Figure 9. Ripple Rejection vs. Frequency (Adjustable Versions)

## APPLICATIONS INFORMATION

The CS5205-x family of linear regulators provide fixed or adjustable voltages at currents up to 5.0 A. The regulators are protected against short circuit, and include thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increases.

The CS5205-x has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The adjustable regulator (CS5205-1) has an output voltage range of 1.25 V to 13 V . An external resistor divider sets the output voltage as shown in Figure 10. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R 1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.

The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{\text {REF }} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{A d j} \times R 2
$$

The term $\mathrm{I}_{\text {Adj }} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R1 is chosen so that the minimum load current is at least 10 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. The adjust pin is bypassed to improve the transient response and ripple rejection of the regulator.


Figure 10. Resistor Divider Scheme for the Adjustable Version

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet provides this information.
A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5205-x the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current.

The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under load transient conditions. The output capacitor network should be as close as possible to the load for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5205-x family of linear regulators, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figures 11 and 12 is recommended.


Figure 11. Protection Diode Scheme for Adjustable Output Regulator


Figure 12. Protection Diode Scheme for Fixed Output Regulators

## Output Voltage Sensing

Since the CS5205-x is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the fixed regulators should be connected as shown in Figure 13.


Figure 13. Conductor Parasitic Resistance can be Minimized with the Above Grounding Scheme for Fixed Output Regulators

For the adjustable regulator, the best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 14. If R1 is connected to the load, $\mathrm{R}_{\mathrm{C}}$ is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes

$$
\mathrm{RC} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 14. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitics

## Calculating Power Dissipation and Heat Sink Requirements

The CS5205-x series of linear regulators includes thermal shutdown and current limit circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to VOUT on the CS5205-x, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{34}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:
$P_{D}($ max $)=\left\{V_{I N}(\right.$ max $)-V_{O U T}($ min $\left.)\right\} I_{O U T}($ max $)+V_{I N(m a x)}{ }^{l} \mathrm{Q}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S \mathrm{SA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{36}
\end{equation*}
$$

The value for $\mathrm{R}_{\text {©JA }}$ is calculated using equation (3) and the result can be substituted in equation (34).

The value for $\mathrm{R}_{\Theta \mathrm{JC}}$ is $3.5^{\circ} \mathrm{C} / \mathrm{W}$ for a given package type based on an average die size. For a high current regulator such as the CS5205-x the majority of the heat is generated in the power transistor section. The value for $R_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part Number | Type | Description |
| :---: | :---: | :---: |
| CS5205-1GT3 | 5.0 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |
| CS5205-1GDP3 | 5.0 A, Adj. Output | D2PAK 3-PIN |
| CS5205-1GDPR3 | 5.0 A, Adj. Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5205-3GT3 | 5.0 A, 3.3 V Output | TO-220 THREE LEAD, STRAIGHT |
| CS5205-3GDP3 | 5.0 A, 3.3 V Output | D2PAK 3-PIN |
| CS5205-3GDPR3 | 5.0 A, 3.3 V Output | D2PAK 3-PIN (Tape \& Reel) |
| CS5205-5GT3 | 5.0 A, 5.0 V Output | TO-220 THREE LEAD, STRAIGHT |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D2PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J \mathrm{~A}}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta C A}$


## CS5205A-1

### 5.0 A Adjustable Linear Regulator

The CS5205A-1 linear regulator provides 5.0 A at an adjustable voltage with an accuracy of $\pm 1 \%$. Two external resistors are used to set the output voltage within a 1.25 V to 13 V range.

The regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulator is fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The CS5205A-1 is pin compatible with the LT1084 family of linear regulators but has lower dropout voltage.

The regulator is available in $T O-220$ and surface mount $\mathrm{D}^{2}$ packages.

## Features

- Output Current to 5.0 A
- Output Trimmed to $\pm 1 \%$
- Dropout Voltage 1.15 V @ 5.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram


MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
$Y Y, Y \quad=$ Year WW, W = Work Week

ORDERING INFORMATION $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5205A-1GT3 | TO-220* | 50 Units/Rail |
| CS5205A-1GDP3 | D$^{2}$ PAK $^{*}$ | 50 Units/Rail |
| CS5205A-1GDPR3 | D$^{2}$ PAK $^{*}$ | 750 Tape \& Reel |

* TO-220 is 3-pin, straight leaded, $D^{2}$ PAK is 3-pin. $\dagger$ Additional ordering information can be found on page 734 of this data sheet.


## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {CC }}$ |  | 17 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak 230 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathbb{I N}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathbb{I N}} \leq 15 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$,
$\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=5.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Adjustable Output Voltage |  |  |  |  |  |
| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}, \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 5.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 1.241 \\ & (-1 \%) \end{aligned}$ | 1.254 | $\begin{aligned} & 1.266 \\ & (+1 \%) \end{aligned}$ | V |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 5.0 \mathrm{~A}$ | - | 0.08 | 0.4 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=5.0 \mathrm{~A} ; \mathrm{T}_{J} \geq 25^{\circ} \mathrm{C}$ | - | 1.15 | 1.25 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $5.5$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | - | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Minimum Load Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=7.0 \mathrm{~V}$ | - | 1.2 | 6.0 | mA |
| Adjust Pin Current |  | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjust Pin Current Change | $\begin{gathered} 1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 4.0 \mathrm{~V} \text {; } \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 5.0 \mathrm{~A} \end{gathered}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{pulse} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{C}_{\text {Adj }}=25 \mu \mathrm{~F} ; \mathrm{l}_{\text {OUT }}=5.0 \mathrm{~A}$ | - | 82 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
4. Specifictions apply for an external Kelvin sense connection at a point on the output pin $1 / 4^{\prime \prime}$ from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |
| :---: | :---: | :---: | :--- |
| TO-220 | D $^{2}$ PAK | Pin Symbol |  |
| 1 | 1 |  | Adjust pin (low side of the internal reference). |
| 2 | 2 | $\mathrm{~V}_{\mathrm{OUT}}$ | Regulated output voltage (case). |
| 3 | 3 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Dropout Voltage vs. Output Current


Figure 4. Load Regulation vs. Output Current


Figure 3. Reference Voltage vs. Temperature


Figure 5. Minimum Load Current


Figure 6. Ripple Rejection vs. Frequency

## APPLICATIONS INFORMATION

The CS5205A-1 linear regulator provides an adjustable voltage at currents up to 5.0 A . The regulator is protected against short circuit, and include thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increases.

The CS5205A-1 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The adjustable regulator (CS5205A-1) has an output voltage range of 1.25 V to 13 V . An external resistor divider sets the output voltage as shown in Figure 7. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.

The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{R E F} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{\text {Adj }} \times R 2
$$

The term $\mathrm{I}_{\text {Adj }} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R1 is chosen so that the minimum load current is at least 10 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. The adjust pin is bypassed to improve the transient response and ripple rejection of the regulator.


Figure 7. Resistor Divider Scheme for the Adjustable Version

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet provides this information.
A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5205A-1 the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{ESR}
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under load transient conditions. The output capacitor network should be as close as possible to the load for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5205A-1 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 8 is recommended.


Figure 8. Protection Diode Scheme for Adjustable Output Regulator

## Output Voltage Sensing

Since the CS5205A-1 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load.

Best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 9. If R1 is connected to the load, $\mathrm{R}_{\mathrm{C}}$ is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes

$$
\mathrm{R}_{\mathrm{C}} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 9. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitics

## Calculating Power Dissipation and Heat Sink Requirements

The CS5205A-1 linear regulator includes thermal shutdown and safe operating area circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.
The case is connected to $V_{\text {OUT }}$ on the CS5205A-1, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.
The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{37}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:
$\mathrm{P}_{\mathrm{D}(\text { max })}=\left\{\mathrm{V}_{\mathrm{IN}(\text { max })}-\mathrm{V}_{\mathrm{OUT}(\min )}\right\}_{\mathrm{I}} \mathrm{OUT}(\max )+\mathrm{V}_{\mathrm{IN}(\text { max })} \mathrm{l}_{\mathrm{Q}}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
$I_{\text {OUT(max) }}$ is the maximum output current, for the application $\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\mathrm{ESA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{39}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (37).

The value for $\mathrm{R}_{\Theta J C}$ is normally quoted as a single figure for a given package type based on an average die size. For a high current regulator such as the CS5205A-1 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact
area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

## ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5205A-1GT3 | 5.0 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |
| CS5205A-1GDP3 | 5.0 A, Adj. Output | D$^{2}$ PAK 3-PIN |
| CS5205A-1GDPR3 | 5.0 A, Adj. Output | D2PAK 3-PIN (Tape \& Reel) |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D2PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$


## CS5206-1, CS5206-3, CS5206-5

### 6.0 A Adjustable, and Fixed 3.3 V and 5.0 V Linear Regulators

The CS5206-X series of linear regulators provides 6.0 A at adjustable and fixed voltages of 3.3 V and 5.0 V with an accuracy of $\pm 1 \%$ and $\pm 2 \%$ respectively. The adjustable version uses two external resistors to set the output voltage within a 1.25 V to 13 V range.

The regulators are intended for use as post regulators and microprocessor supplies. The fast loop response and low dropout voltage make these regulators ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulators are fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The regulators are available in TO-220 and surface mount $\mathrm{D}^{2} \mathrm{PAK}$ packages.

## Features

- Output Current to 6.0 A
- Output Trimmed to $\pm 1 \%$
- Dropout Voltage 1.3 V @ 6.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram - CS5206-1


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MARKING DIAGRAMS

$x \quad=1,3$, or 5
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year WW, W = Work Week

ORDERING INFORMATION $\dagger$

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5206-1GT3 | TO-220* | 50 Units/Rail |
| CS5206-1GDP3 | D$^{2}$ PAK $^{*}$ | 50 Units/Rail |
| CS5206-1GDPR3 | D$^{2}$ PAK | 750 Tape \& Reel |
| CS5206-3GT3 | TO-220 | 50 Units/Rail |
| CS5206-3GDP3 | D$^{2}$ PAK | 50 Units/Rail |
| CS5206-3GDPR3 | D$^{2}$ PAK | 750 Tape \& Reel |
| CS5206-5GT3 | TO-220 | 50 Units/Rail |

* TO-220 are all 3-pin, straight leaded. D²PAK are all 3-pin.
$\dagger$ Additional ordering information can be found on page 742 of this data sheet.


Figure 2. Block Diagram - CS5206-2, -3

## MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ |  | 17 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak <br> 230 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}\right.$, $\mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}$, Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 15 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J}=+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=6.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Adjustable Output Voltage (CS5206-1) |  |  |  |  |  |
| Reference Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}, \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 6.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 1.241 \\ & (-1 \%) \end{aligned}$ | 1.254 | $\begin{aligned} & 1.266 \\ & (+1 \%) \end{aligned}$ | V |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ |  | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 6.0 \mathrm{~A}$ |  | 0.1 | 0.4 | \% |
| Dropout Voltage (Note 5) | I OUT $=6.0 \mathrm{~A}$ |  | 1.3 | 1.4 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | 6.5 | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | 6.0 | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Minimum Load Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=7.0 \mathrm{~V}$ |  | 1.2 | 100 | mA |
| Adjust Pin Current |  |  | 50 | 5.0 | $\mu \mathrm{A}$ |
| Adjust Pin Current Change | $\begin{gathered} 1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 4.0 \mathrm{~V} ; \\ 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 6.0 \mathrm{~A} \end{gathered}$ |  | 0.2 |  | $\mu \mathrm{A}$ |
| Thermal Regulation | 30 ms pulse; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 0.003 |  | \%/W |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
4. Specifictions apply for an external Kelvin sense connection atr a point on the output pin $1 / 4^{\prime \prime}$ from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## CS5206-1, CS5206-3, CS5206-5

ELECTRICAL CHARACTERISTICS continued ( $\mathrm{C}_{\mathbb{I N}}=10 \mu \mathrm{~F}$, $\mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}$, Tantalum, $\mathrm{V}_{\mathbb{I N}}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{I N} \leq 15 \mathrm{~V}$, $0^{\circ} \mathrm{C} \leq T_{A} \leq 70^{\circ} \mathrm{C}, \mathrm{T}_{J}=+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=6.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Adjustable Output Voltage (CS5206-1) continued

| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{C}_{\text {Adj }}=25 \mu \mathrm{~F} ; \mathrm{IOUT}=6.0 \mathrm{~A}$ |  | 82 |  |
| :--- | :--- | :---: | :---: | :---: |
| Temperature Stability |  |  | 0.5 |  |
| RMS Output Noise | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 0.003 |  |
| Thermal Shutdown |  | 150 | 180 | $\%$ |
| Thermal Shutdown Hysteresis |  |  | 25 | ${ }^{\circ} \mathrm{V}$ OUT |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}\right.$, Tantalum, $\mathrm{V}_{\mathrm{IN}^{\prime}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }} \leq 10 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J}=+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=6.0 \mathrm{~A}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Fixed Output Voltage (CS5206-3, CS5206-5)

| Reference Voltage (Notes 6 and 7) CS5206-5 CS5206-3 | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}, \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 6.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 4.9(-2 \%) \\ 3.234(-2 \%) \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 3.3 \end{aligned}$ | $\begin{gathered} 5.1(+2 \%) \\ 3.366(+2 \%) \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ |  | 0.04 | 0.20 | \% |
| Load Regulation (Notes 6 and 7) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 6.0 \mathrm{~A}$ |  | 0.1 | 0.4 | \% |
| Dropout Voltage (Note 8) | IOUT $=6.0 \mathrm{~A}$ |  | 1.3 | 1.4 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{J} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | 6.5 | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | 6.0 | $\begin{aligned} & \mathrm{A} \\ & \mathrm{~A} \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ |  | 5.0 | 10 | mA |
| Thermal Regulation | 30 ms pulse; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 0.003 |  | \%/W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{C}_{\text {Adj }}=25 \mu \mathrm{~F} ; \mathrm{l}_{\text {OUT }}=6.0 \mathrm{~A}$ |  | 75 |  | dB |
| Temperature Stability |  |  | 0.5 |  | \% |
| RMS Output Noise (\%V ${ }_{\text {Out }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ |  | 0.003 |  | \%V $\mathrm{V}_{\text {OUT }}$ |
| Thermal Shutdown |  | 150 | 180 |  | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis |  |  | 25 |  | ${ }^{\circ} \mathrm{C}$ |

6. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account separately.
7. Specifictions apply for an external Kelvin sense connection atr a point on the output pin $1 / 4^{\prime \prime}$ from the bottom of the package.
8. Dropout voltage is a measurement of the minimum input/output differentail at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  | Pin Symbol | Function |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5206-1 |  | CS5206-3, CS5206-5 |  |  |  |
| D2PAK | TO-220 | D2PAK | TO-220 |  |  |
| 1 | 1 | N/A | N/A | Adj | Adjust pin (low side of the internal reference) |
| 2 | 2 | 2 | 2 | $\mathrm{V}_{\text {OUT }}$ | Regulated output voltage (case) |
| 3 | 3 | 3 | 3 | $\mathrm{V}_{\text {IN }}$ | Input voltage |
| N/A | N/A | 1 | 1 | Gnd | Ground connection |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. Dropout Voltage vs. Output Current


Figure 5. Load Regulation vs. Output Current


Figure 7. Adjust Pin Current vs. Temperature


Figure 4. Reference Voltage vs. Temperature


Figure 6. Minimum Load Current


Figure 8. Ripple Rejection vs. Frequency (Fixed Versions)


Figure 9. Ripple Rejection vs. Frequency (Adjustable Version)

## APPLICATIONS INFORMATION

The CS5206-X family of linear regulators provide fixed or adjustable voltages at currents up to 6.0 A. The regulators are protected against short circuit, and include thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increases.

The CS5206-X has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The adjustable regulator (CS5206-1) has an output voltage range of 1.25 V to 13 V . An external resistor divider sets the output voltage as shown in Figure 10. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R 1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary.

The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{\text {REF }} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{A d j} \times R 2
$$

The term $\mathrm{I}_{\text {Adj }} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R1 is chosen so that the minimum load current is at least 10 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. The adjust pin is
bypassed to improve the transient response and ripple rejection of the regulator.


Figure 10. Resistor Divider Scheme for the Adjustable Version

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.
The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet provides this information.
A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the

CS5206-X the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under load transient conditions. The output capacitor network should be as close as possible to the load for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\mathrm{IN}}$ drops. In the CS5206-X family of linear regulators, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figures 11 and 12 is recommended.


Figure 11. Protection Diode Scheme for Adjustable Output Regulator


Figure 12. Protection Diode Scheme for Fixed Output Regulators

## Output Voltage Sensing

Since the CS5206-X is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the fixed regulators should be connected as shown in Figure 13.


Figure 13. Conductor Parasitic Resistance can be Minimized with the Above Grounding Scheme for Fixed Output Regulators
For the adjustable regulator, the best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 14. If R1 is connected to the load, $\mathrm{R}_{\mathrm{C}}$ is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes

$$
\mathrm{RC} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 14. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitics

## Calculating Power Dissipation and Heat Sink Requirements

The CS5206-X series of linear regulators includes thermal shutdown and safe operating area circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction
temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to $\mathrm{V}_{\text {OUT }}$ on the CS5206-X, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $P_{D}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{40}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:
$\mathrm{P}_{\mathrm{D}(\text { max })}=\left\{\mathrm{V}_{\mathrm{IN}(\text { max })}-\mathrm{V}_{\mathrm{OUT}(\text { min })}\right\}_{\mathrm{I}} \mathrm{OUT}($ max $)+\mathrm{V}_{\mathrm{IN}(\text { max })}{ }^{\mathrm{l} Q}$
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application $\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S \mathrm{~A}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{42}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (40).

The value for $\mathrm{R}_{\Theta J C}$ is normally quoted as a single figure for a given package type based on an average die size. For a high current regulator such as the CS5206-X the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta \text { JSA }}$ depends on the heat sink type, while $\mathrm{R}_{\Theta \text { JICS }}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $R_{\Theta J A}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :--- | :--- |
| CS5206-1GT3 | 6A, Adj. Output | 3-Pin TO-220 Straight |
| CS5206-1GDP3 | 6A, Adj. Output | 3-Pin D²PAK |
| CS5206-1GDPR3 | 6A, Adj. Output | 3-Pin D2PAK (Tape \& Reel) |
| CS5206-3GT3 | 6A, 3.3V Output | 3-Pin TO-220 Straight |
| CS5206-3GDP3 | 6A, 3.3V Output | 3-Pin D²PAK |
| CS5206-3GDPR3 | 6A, 3.3V Output | 3-Pin D²PAK (Tape \& Reel) |
| CS5206-5GT3 | 6A, 5V Output | 3-Pin TO-220 Straight |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 | D $^{2}$ PAK | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$


## CS5207-2

### 7.0 A, 1.5 V Fixed Linear Regulator

The CS5207-2 provides 7.0 A at 1.5 V with an accuracy of $\pm 2.0 \%$. The regulator is intended for use as an active termination for the GTL bus on Intel based motherboards. The fast loop response and low dropout voltage make these regulators ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulators are fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The CS5207-2 is available in TO-220 packages.

## Features

- Output Current to 7.0 A
- Output Voltage Trimmed to $\pm 2.0 \%$
- Dropout Voltage 1.45 V @ 7.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram

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PIN CONNECTIONS AND MARKING DIAGRAMS


Tab $=\mathrm{V}_{\text {OUT }}$
Pin 1. GND
2. $\mathrm{V}_{\text {OUT }}$
3. $\mathrm{V}_{\mathrm{IN}}$

$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
Y Y, Y & =\text { Year } \\
\text { WW, } W=\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION*

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5207-2GT3 | TO-220 $\dagger$ | 50 Units/Rail |

*Additional ordering information can be found on page 747 of this data sheet.
$\dagger$ TO-220 is 3-pin, straight leaded.

## ABSOLUTE MAXIMUM RATINGS*

|  | Parameter | Value |
| :--- | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ | Unit |  |
| Operating Temperature Range | 17 |  |
| Junction Temperature | V |  |
| Storage Temperature Range | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Solder (through hole styles only) Note 1 | 260 Peak | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}$ Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq 10 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$,
$\mathrm{T}_{j} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=7.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Fixed Output Voltage

| Output Voltage (Notes 2 and 3) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.65 \mathrm{~V} ; \\ & 0 \leq \mathrm{I}_{\text {OUT }} \leq 7.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.47 \\ (-2.0 \%) \end{gathered}$ | 1.50 | $\begin{gathered} 1.53 \\ (+2.0 \%) \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $1.65 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 2 and 3) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.65 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 7.0 \mathrm{~A}$ | - | 0.08 | 0.40 | \% |
| Dropout Voltage (Note 4) | $\mathrm{l}_{\text {OUT }}=7.0 \mathrm{~A}$ | - | 1.42 | 1.65 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{\mathrm{J}} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=12 \mathrm{~V} \end{aligned}$ | $7.1$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | - | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%/W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; $\mathrm{l}_{\text {OUT }}=7.0 \mathrm{~A}$ | - | 80 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise (\%V ${ }_{\text {Out }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}$ | - | 0.003 | - | \% $\mathrm{N}_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

2. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account seperately.
3. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
4. Dropout voltage is a measurement of the minimum input/output differential at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  | Function |
| :---: | :---: | :--- | :--- |
| TO-220 | Pin Symbol |  |  |
| 1 | GND | Ground connection. |  |
| 2 | $\mathrm{~V}_{\text {OUT }}$ | Regulated output voltage (case). |  |
| 3 | $\mathrm{~V}_{\mathrm{IN}}$ | Input voltage. |  |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Dropout Voltage vs. Output Current


Figure 4. Load Regulation vs. Output Current


Figure 3. Output Voltage vs. Temperature


Figure 5. Ripple Rejection vs. Frequency

## APPLICATIONS INFORMATION

The CS5207-2 linear regulator provides a fixed 1.5 V output at currents up to 7.0 A . The regulator is protected against short circuit, and includes thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increase.

The CS5207-2 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5207-2 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5207-2 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 6 is recommended.


Figure 6. Protection Diode Scheme for Fixed Output Regulators

## Output Voltage Sensing

Since the CS5207-2 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load. For best results the regulator should be connected as shown in Figure 7.


Figure 7. Conductor Parasitic Resistance Effects Can Be Minimized With the Above Grounding Scheme for Fixed Output Regulators

## Calculating Power Dissipation and Heat Sink Requirements

The CS5207-2 includes thermal shutdown and safe operating area circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to VOUT on the CS5207-2, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $P_{D}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{43}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\text {©SA }}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{45}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (43).
$\mathrm{R}_{\Theta \mathrm{JC}}$ is $1.6^{\circ} \mathrm{C} /$ Watt for the CS5207-2. For a high current regulator such as the CS5207-2 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

## ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :---: | :---: |
| CS5207-2GT3 | 7.0 A, 1.5 V Output | TO-220 THREE LEAD, STRAIGHT |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5207-3

### 7.0 A, 3.3 V Fixed Linear Regulator

The CS5207-3 linear regulator provides 7.0 A @ 3.3 V with an accuracy of $\pm 2.0 \%$.

The regulator is intended for use as post regulator and microprocessor supply. The fast loop response and low dropout voltage make these regulators ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current level. The maximum quiescent current is only 10 mA at full load.

The regulator is fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The CS5207-3 is available in TO-220 and surface mount $\mathrm{D}^{2}$ packages.

## Features

- Output Current to 7.0 A
- Output Voltage Trimmed to $\pm 2.0 \%$
- Dropout Voltage 1.4 V @ 7.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram

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MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
YY, $Y$ = Year WW, W = Work Week
ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5207-3GT3 | TO-220* $^{*}$ | 50 Units/Rail |
| CS5207-3GDP3 | D$^{2}$ PAK $^{*}$ | 50 Units/Rail |
| CS5207-3GDPR3 | D$^{2}$ PAK $^{*}$ | 750 Tape \& Reel |

*TO-220 are all 3-pin, straight leaded. D2PAK are all 3-pin.

## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {CC }}$ |  | 17 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak <br> 230 Peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathbb{I N}}=10 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{OUT}}=22 \mu \mathrm{~F}\right.$ Tantalum, $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathbb{I N}} \leq 15 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{I}_{\text {full load }}=7.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 3.3 V Fixed Output Voltage |  |  |  |  |  |
| Output Voltage (Notes 3 and 4) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.6 \mathrm{~V} ; \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 7.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 3.234 \\ (-2.0 \%) \end{gathered}$ | 3.300 | $\begin{gathered} 3.366 \\ (+2.0 \%) \end{gathered}$ | V |
| Line Regulation | $1.6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 3 and 4) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.6 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 7.0 \mathrm{~A}$ | - | 0.13 | 0.5 | \% |
| Dropout Voltage (Note 5) | $\mathrm{I}_{\text {OUT }}=7.0 \mathrm{~A}$ | - | 1.4 | 1.55 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{J} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $7.1$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }} \leq 9.0 \mathrm{~V}$; $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 5.0 | 10 | mA |
| Thermal Regulation | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\text {OUT }}=7.0 \mathrm{~A}$ | - | 80 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise (\%V ${ }_{\text {OUT }}$ ) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account seperately.
4. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
5. Dropout voltage is a measurement of the minimum input/output differential at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |
| :---: | :---: | :---: | :--- |
| TO-220 | D $^{2}$ PAK | Pin Symbol |  |
| 1 | 1 | GND | Ground connection. |
| 2 | 2 | V OUT | Regulated output voltage (case). |
| 3 | 3 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Dropout Voltage vs. Output Current


Figure 4. Load Regulation vs. Output Current


Figure 3. Output Voltage vs. Temperature


Figure 5. Ripple Rejection vs. Frequency

## APPLICATIONS INFORMATION

The CS5207-3 linear regulator provides a fixed 3.3 V output currents up to 7.0 A . The regulator is protected against short circuit, and includes thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increase.

The CS5207-3 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5207-3 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5207-3 regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 6 is recommended.


Figure 6. Protection Diode Scheme for Fixed Output Regulator

## Output Voltage Sensing

Since the CS5207-3 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load.
Best load regulation occurs when the regulator is connected to the load as shown in Figure 7.


Figure 7. Grounding Scheme for the Output Regulator to Minimize Parasitics

## Calculating Power Dissipation and Heat Sink Requirements

The CS5207-3 linear regulator includes thermal shutdown and safe operating area circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V VUT on the CS5207-3, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $P_{D}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{46}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S A}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{48}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (46).
$\mathrm{R}_{\Theta \mathrm{JC}}$ is $1.6^{\circ} \mathrm{C} /$ Watt for the CS5207-3. For a high current regulator such as the CS5207-3 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | D $^{2}$ PAK <br> 3-PIN | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 1.6 | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J A}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta C A}$


## CS5207-1

### 7.0 A Adjustable Linear Regulator

The CS5207-1 linear regulator provides 7.0 A adjustable voltages with an accuracy of $\pm 1.5 \%$. Two external resistors are used to set the output voltage within a 1.25 V to 13 V range.

The regulator is intended for use as post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V depending on the output current. The maximum quiescent current is only 10 mA at full load.

The regulator is fully protected against overload conditions with protection circuitry for Safe Operating Area (SOA), overcurrent and thermal shutdown.

The regulator is available in TO-220 package. A 3.3 V , fixed version is also available. Please consult your local sales representative for more information.

## Features

- Output Current to 7.0 A
- Output Trimmed to $\pm 1.5 \%$
- Dropout Voltage 1.4 V @ 7.0 A
- Fast Transient Response
- Fault Protection Circuitry
- Thermal Shutdown
- Overcurrent Protection
- Safe Area Protection


Figure 1. Block Diagram


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TO-220
THREE LEAD
T SUFFIX CASE 221A

PIN CONNECTIONS AND MARKING DIAGRAMS


Tab $=\mathrm{V}_{\text {OUT }}$
Pin 1. Adj
2. VOUT
3. $\mathrm{V}_{\mathrm{IN}}$

A = Assembly Location
WL, L = Wafer Lot
$Y Y, Y \quad=$ Year
WW, W = Work Week

## ORDERING INFORMATION* $\dagger$

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5207-1GT3 | TO-220 $\ddagger$ | 50 Units/Rail |

*Additional ordering information can be found on page 758 of this data sheet.
$\dagger$ Consult your local sales representative for fixed output voltage versions.
$\ddagger$ TO-220 is 3-pin, straight leaded.

## ABSOLUTE MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ |  | 17 | V |
| Operating Temperature Range |  | -40 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 | 260 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $\mathrm{C}_{\mathrm{IN}}=10 \mu \mathrm{~F}, \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F}$ Tantalum, $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }} \leq 15 \mathrm{~V}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}$, $\mathrm{T}_{J} \leq+150^{\circ} \mathrm{C}$, unless otherwise specified, $\mathrm{l}_{\text {full load }}=7.0 \mathrm{~A}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Adjustable Output Voltage |  |  |  |  |  |
| Reference Voltage (Notes 2 and 3) | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.6 \mathrm{~V} ; \mathrm{V}_{\text {Adj }}=0 \mathrm{~V} \\ & 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 7.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.235 \\ (-1.5 \%) \end{gathered}$ | 1.254 | $\begin{gathered} 1.272 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $1.6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 6.0 \mathrm{~V}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.04 | 0.20 | \% |
| Load Regulation (Notes 2 and 3) | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=1.6 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 7.0 \mathrm{~A}$ | - | 0.13 | 0.5 | \% |
| Dropout Voltage (Note 4) | l OUT $=7.0 \mathrm{~A}$ | - | 1.4 | 1.55 | V |
| Current Limit | $\begin{aligned} & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V} ; \mathrm{T}_{J} \geq 25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=9.0 \mathrm{~V} \end{aligned}$ | $7.1$ | $\begin{aligned} & 8.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Minimum Load Current | $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}=7.0 \mathrm{~V}$ | - | 1.2 | 6.0 | mA |
| Adjust Pin Current | - | - | 50 | 100 | $\mu \mathrm{A}$ |
| Adjust Pin Current Change | $1.6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }} \leq 4.0 \mathrm{~V} ; 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 7.0 \mathrm{~A}$ | - | 0.2 | 5.0 | $\mu \mathrm{A}$ |
| Thermal Regulation | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%W |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{C}_{\text {Adj }}=25 \mu \mathrm{~F} ; \mathrm{l}_{\text {OUT }}=7.0 \mathrm{~A}$ | - | 80 | - | dB |
| Temperature Stability | - | - | 0.5 | - | \% |
| RMS Output Noise | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz} ; \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%V ${ }_{\text {OUT }}$ |
| Thermal Shutdown | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

2. Load regulation and output voltage are measured at a constant junction temperature by low duty cycle pulse testing. Changes in output voltage due to thermal gradients or temperature changes must be taken into account seperately.
3. Specifications apply for an external Kelvin sense connection at a point on the output pin $1 / 4$ " from the bottom of the package.
4. Dropout voltage is a measurement of the minimum input/output differential at full load.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |
| :---: | :---: | :--- |
| TO-220 | Pin Symbol |  |
| 1 |  | Adjust pin (low side of the internal reference). |
| 2 | $\mathrm{~V}_{\text {OUT }}$ | Regulated output voltage (case). |
| 3 | $\mathrm{~V}_{\text {IN }}$ | Input voltage. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Dropout Voltage vs. Output Current


Figure 4. Load Regulation vs. Output Current


Figure 3. Reference Voltage vs. Temperature


Figure 5. Minimum Load Current


Figure 6. Ripple Rejection vs. Frequency

## APPLICATIONS INFORMATION

The CS5207-1 linear regulator provides adjustable voltages at currents up to 7.0 A . The regulator is protected against short circuit, and includes thermal shutdown and safe area protection (SOA) circuitry. The SOA protection circuitry decreases the maximum available output current as the input-output differential voltage increases.

The CS5207-1 has a composite PNP-NPN output transistor and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## Adjustable Operation

The adjustable regulator has an output voltage range of 1.25 V to 13 V . An external resistor divider sets the output voltage as shown in Figure 7. The regulator maintains a fixed 1.25 V (typical) reference between the output pin and the adjust pin.

A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.25 V across R 1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of VOUT is necessary.
The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{\text {REF }} \times\left(\frac{R 1+R 2}{R 1}\right)+I_{\text {Adj }} \times R 2
$$

The term $\mathrm{I}_{\mathrm{Adj}} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R 1 is chosen so that the minimum load current is at least 10 mA . R1 and R2 should be the same type, e.g. metal film for best tracking over temperature. The adjust pin is bypassed to improve the transient response and ripple rejection of the regulator.


Figure 7. Resistor Divider Scheme for the Adjustable Version

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.
A $22 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5207-1 the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta \mathrm{V}=\Delta \mathrm{I} \times \mathrm{ESR}
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\text {IN }}$ drops. In the CS5207-1 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 8 is recommended.


Figure 8. Protection Diode Scheme for Adjustable Output Regulator

## Output Voltage Sensing

Since the CS5207-1 is a three terminal regulator, it is not possible to provide true remote load sensing. Load regulation is limited by the resistance of the conductors connecting the regulator to the load.

Best load regulation occurs when R1 is connected directly to the output pin of the regulator as shown in Figure 9. If R1 is connected to the load, $\mathrm{R}_{\mathrm{C}}$ is multiplied by the divider ratio and the effective resistance between the regulator and the load becomes.

$$
\mathrm{RC} \times\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}\right)
$$

where $\mathrm{R}_{\mathrm{C}}=$ conductor parasitic resistance.


Figure 9. Grounding Scheme for Adjustable Output Regulator to Minimize Parasitic Resistance Effects

## Calculating Power Dissipation and Heat Sink Requirements

The CS5207-1 linear regulator includes thermal shutdown and safe operating area circuitry to protect the device. High power regulators such as these usually operate at high junction temperatures so it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used.

The case is connected to V ${ }_{\text {OUT }}$ on the CS5207-1, electrical isolation may be required for some applications. Thermal compound should always be used with high current regulators such as these.

The thermal characteristics of an IC depend on the following four factors:

1. Maximum Ambient Temperature $\mathrm{T}_{\mathrm{A}}\left({ }^{\circ} \mathrm{C}\right)$
2. Power dissipation $\mathrm{P}_{\mathrm{D}}$ (Watts)
3. Maximum junction temperature $\mathrm{T}_{\mathrm{J}}\left({ }^{\circ} \mathrm{C}\right)$
4. Thermal resistance junction to ambient $\mathrm{R}_{\Theta \mathrm{JA}}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$

These four are related by the equation

$$
\begin{equation*}
T_{J}=T_{A}+P_{D} \times R_{\Theta J A} \tag{49}
\end{equation*}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type.

The maximum power dissipation for a regulator is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT(min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current, for the application
$\mathrm{I}_{\mathrm{Q}}$ is the maximum quiescent current at $\mathrm{I}_{\mathrm{OUT}(\max )}$.
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine $\mathrm{R}_{\Theta J A}$, the total thermal resistance between the junction and the surrounding air.

1. Thermal Resistance of the junction to case, $\mathrm{R}_{\Theta \mathrm{JC}}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
2. Thermal Resistance of the case to Heat Sink, $\mathrm{R}_{\Theta C S}$ ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ )
3. Thermal Resistance of the Heat Sink to the ambient air, $\mathrm{R}_{\Theta S A}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
These are connected by the equation:

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{51}
\end{equation*}
$$

The value for $\mathrm{R}_{\Theta J A}$ is calculated using equation (3) and the result can be substituted in equation (49).

The value for $\mathrm{R}_{\Theta \mathrm{JC}}$ is normally quoted as a single figure for a given package type based on average die size. For a high current regulator such as the CS5207-1 the majority of the heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $R_{\Theta J A}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

ADDITIONAL ORDERING INFORMATION

| Orderable Part <br> Number | Type | Description |
| :--- | :---: | :---: |
| CS5207-1GT3 | 7.0 A, Adj. Output | TO-220 THREE LEAD, STRAIGHT |

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $\mathrm{R}_{\Theta J C}$ | Typical | 1.6 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5207A-1

### 7.0 A LDO 3-Pin Adjustable Linear Regulator

The CS5207A-1 linear regulator provides 7.0 A at adjustable voltages from 1.25 V to 5.0 V . This adjustable device requires two external resistors to set the output voltage and provide the minimum load current for proper regulation.

This regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V at 7.0 A .

This regulator is protected against overload conditions with overcurrent and thermal shutdown protection circuitry.

The CS5207A-1 is pin compatible with the LT1584 family of linear regulators but has lower dropout voltage and faster transient response.

This regulator is available in a TO-220 package.

## Features

- 1.25 V to 5.0 V V OUT @ 7.0 A
- Dropout Voltage < 1.0 V @ 7.0 A
- $1.5 \%$ Trimmed Reference
- Fast Transient Response
- Thermal Shutdown
- Current Limit
- Short Circuit Protection
- Drop-In Replacement for LT1584


Figure 1. Applications Diagram

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TO-220
THREE LEAD
T SUFFIX
CASE 221A

PIN CONNECTIONS AND MARKING DIAGRAMS


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5207A-1GT3 | TO-220* | 50 Units/Rail |

*TO-220 is 3-pin, straight leaded.

## ABSOLUTE MAXIMUM RATINGS*

|  | Parameter | Value |
| :--- | :---: | :---: |
| Input Voltage | Unit |  |
| Operating Junction Temperature Range | 6.0 | V |
| Storage Temperature Range | Wave Solder (through hole styles only) Note 1 | 260 Peak |
| Lead Temperature Soldering: | -60 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold | ${ }^{\circ} \mathrm{C}$ |  |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Adjustable Output Voltage |  |  |  |  |  |
| Reference Voltage | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}$ to 5.5 V , IOUT $=10 \mathrm{~mA}$ to 7.0 A | $\begin{gathered} 1.234 \\ (-1.5 \%) \end{gathered}$ | 1.253 | $\begin{gathered} 1.271 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}$ to 5.5 V , I IOUT $=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ to 7.0 A | - | 0.04 | 0.50 | \% |
| Minimum Load Current (Note 2) | $\mathrm{V}_{\text {IN }}=5.0 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=+1.5 \%$ | - | 5.0 | 10 | mA |
| Adjust Pin Current | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 70 | 120 | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=-1.5 \%$ | 7.1 | 8.0 | - | A |
| Short Circuit Current | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | 5.0 | 9.0 | - | A |
| Ripple Rejection (Note 3) | $\begin{aligned} & \mathrm{V}_{\text {IN }}=3.25 \mathrm{~V}, \mathrm{~V}_{\text {RIPPLE }}=1.0 \mathrm{VP}_{\text {P-P }} @ 120 \mathrm{~Hz}, \\ & \mathrm{I}_{\text {OUT }}=4.0 \mathrm{~A}, \mathrm{C}_{\text {Adj }}=0.1 \mu \mathrm{~F} ; \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F} \end{aligned}$ | 60 | 80 | - | dB |
| Thermal Regulation (Note 3) | 30 ms Pulse, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | - | \%/W |
| Dropout Voltage (Minimum $\left.\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right)$ (Note 4) | $\begin{aligned} & \text { lout }=100 \mathrm{~mA} \\ & \text { l }_{\text {OUT }}=1.0 \mathrm{~A} \\ & \text { l }_{\text {OUT }}=2.75 \mathrm{~A} \\ & \text { l Out }=4.0 \mathrm{~A} \\ & \text { I OUT }=7.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 0.92 \\ & 0.93 \\ & 0.94 \\ & 0.95 \\ & 0.96 \end{aligned}$ | $\begin{aligned} & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.25 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| RMS Output Noise | Freq $=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Temperature Stability | - | - | 0.5 | - | \% |
| Thermal Shutdown (Note 5) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 5) | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

2. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum load current requirement.
3. This parameter is guaranteed by design and is not $100 \%$ production tested.
4. Dropout voltage is defined as the minimum input/output voltage differential required to maintain $1.5 \%$ regulation.
5. This parameter is guaranteed by design, but not parametrically tested in production. However, a $100 \%$ thermal shutdown functional test is performed on each part.

PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |
| :---: | :---: | :--- |
| TO-220 | Pin Symbol |  |
| 1 | Adjust | This pin is connected to the low side of the internally trimmed $1.5 \%$ bandgap reference <br> voltage and carries a bias current of about $70 \mu \mathrm{~A}$. A resistor divider from Adj to $\mathrm{V}_{\text {OUT }}$ and from <br> Adj to ground sets the output voltage. Also, transient response can be improved by adding a <br> small bypass capacitor from this pin to ground. |
| 2 | $\mathrm{~V}_{\text {OUT }}$ | This pin is connected to the emitter of the power pass transistor and provides a regulated <br> voltage capable of sourcing 7.0 A of current. |
| 3 | $\mathrm{~V}_{\mathrm{IN}}$ | This is the supply voltage for the regulator. For the device to regulate, this voltage should be <br> between 1.0 V and 1.25 V (depending on the output current) greater than the output voltage. |



Figure 2. Block Diagram

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. Reference Voltage vs. Temperature


Figure 4. Load Regulation vs. Output Current


Figure 5. Adjust Pin Current vs. Temperature


Figure 7. Dropout Voltage vs. Output Current


Figure 9. Minimum Load Current vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$


Figure 6. Adjust Pin vs. Iout


Figure 8. Short Circuit vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$


Figure 10. Ripple Rejection vs. Frequency

## APPLICATION NOTES

## THEORY OF OPERATION

The CS5207A-1 linear regulator has a composite PNP-NPN output stage that requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## ADJUSTABLE OPERATION

## Design Guidelines

This LDO adjustable regulator has an output voltage range of 1.25 V to 5.0 V . An external resistor divider sets the output voltage as shown in Figure 11. The regulator's voltage sensing error amplifier maintains a fixed 1.25 V reference between the output pin and the adjust pin.

A resistor divider network $R_{1}$ and $R_{2}$ causes a fixed current to flow to ground. This current creates a voltage across $\mathrm{R}_{2}$ that adds to the 1.25 V across $\mathrm{R}_{1}$ and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through $\mathrm{R}_{2}$ and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary. The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{\text {REF }} \times\left(\frac{R_{1}+R_{2}}{R_{1}}\right)+R_{2} \times I_{A d j}
$$

The term $\mathrm{I}_{\mathrm{Adj}} \times \mathrm{R}_{2}$ represents the error added by the adjust pin current.
$\mathrm{R}_{1}$ is chosen so that the minimum load current is at least 10 mA . $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ should be of the same composition for best tracking over temperature. For best results, the divider resistor should be placed near the regulator with a seperate metal trace connecting them to output..


Figure 11.
While not required, a bypass capacitor connected between the adjust pin and ground will improve transient response and ripple rejection. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Value and type may be varied to optimize performance vs price.

OTHER ADJUSTABLE OPERATION CONSIDERATIONS
The CS5207A-1 linear regulator has an absolute maximum specification of 6.0 V for the voltage difference between $\mathrm{V}_{\text {IN }}$ and $\mathrm{V}_{\text {OUT }}$. However, the IC may be used to regulate voltages in excess of 6.0 V . The main considerations in such a design are power-up and short circuit capability.
In most applications, ramp-up of the power supply to $\mathrm{V}_{\text {IN }}$ is fairly slow, typically on the order of several tens of milliseconds, while the regulator responds in less than one microsecond. In this case, the linear regulator begins charging the output capacitor as soon as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential is large enough that the pass transistor conducts current. V ${ }_{\text {OUT }}$ is essentially at ground, and $\mathrm{V}_{\text {IN }}$ is on the order of several hundred millivolts, so the pass transistor is in dropout. As $\mathrm{V}_{\text {IN }}$ increases, the pass transistor will remain in dropout, and current is passed to the load until $\mathrm{V}_{\text {OUT }}$ is in regulation. Further increase in $\mathrm{V}_{\text {IN }}$ brings the pass transistor out of dropout. The result is that the output voltage follows the power supply ramp-up, staying in dropout until the regulation point is reached. In this manner, any output voltage may be regulated. There is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 6.0 V is not exceeded.

However, maximum ratings of the IC will be exceeded in a short circuit condition. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Over-voltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential to less than 6.0 V if failsafe operation is required. One possible clamp circuit is illustrated in Figure 12; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit conditions indefinitely while protecting the IC.


Figure 12.

## STABILITY CONSIDERATIONS

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $300 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5207A-1 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\mathrm{IN}}$ drops. In the CS5207A-1 regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 13 is recommended.

A rule of thumb useful in determining if a protection diode is required is to solve for current

$$
\mathrm{I}=\frac{\mathrm{C} \times \mathrm{V}}{\mathrm{~T}}
$$

where:
I is the current flow out of the load capacitance when $\mathrm{V}_{\mathrm{IN}}$ is shorted,
C is the value of the load capacitance,
V is the output voltage, and
T is the time duaration required for $\mathrm{V}_{\mathrm{IN}}$ to transition from high to being shorted.

If the calculated current is greater than or equal to the typical short circuit current value provided in the specifications, serious thought should be given to including a protection diode.


Figure 13.

## Current Limit

The internal current limit circuit limits the output current under excessive load conditions and protects the regulator.

## Short Circuit Protection

The device includes foldback short circuit current limit that clamps the output current at approximately two amperes less than its current limit value.

## Thermal Shutdown

The thermal shutdown circuitry is guaranteed by design to become activated above a die junction temperature of $150^{\circ} \mathrm{C}$ and to shut down the regulator output. This circuitry includes a thermal hysteresis circuit with $25^{\circ} \mathrm{C}$ of typical hysteresis, thereby allowing the regulator to recover from a thermal fault automatically.

## Calculating Power Dissipation and Heat Sink Requirements

High power regulators such as the CS5207A-1 usually operate at high junction temperatures. Therefore, it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used. Since the package tab is connected to $\mathrm{V}_{\text {OUT }}$ on the CS5207A-1, electrical isolation may be required for some applications. Also, as with all high power packages, thermal compound is necessary to ensure proper heat flow. For added safety, this high current LDO includes an internal thermal shutdown circuit
The thermal characteristics of an IC depend on the following four factors. Junction temperature, ambient temperature, die power dissipation, and the thermal resistance from the die junction to ambient air. The maximum junction temperature can be determined by:

$$
\mathrm{T}_{\mathrm{J}(\max )}=\mathrm{T}_{\mathrm{A}(\max )}+\mathrm{P}_{\mathrm{D}(\max )} \times \mathrm{R}_{\Theta \mathrm{JA}}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type. The maximum power dissipation for a regulator is:
$\mathrm{P}_{\mathrm{D}(\max )}=\left(\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{V}_{\mathrm{OUT}}(\min )\right) \mathrm{IOUT}_{\mathrm{O}}(\max )+\mathrm{V}_{\mathrm{IN}(\text { max }} \times \mathrm{I}_{\mathrm{IN}(\text { max })}$
A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine the total thermal resistance between the die junction and the surrounding air, $\mathrm{R}_{\Theta \mathrm{JC}}$. This total thermal resistance is comprised of three components. These resistive terms are measured from junction to case ( $\mathrm{R}_{\Theta \mathrm{JC}}$ ), case to heat sink ( $\mathrm{R}_{\Theta C S}$ ), and heat sink to ambient air ( $\mathrm{R}_{\Theta S A}$ ). The equation is:

$$
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A}
$$

$\mathrm{R}_{\Theta \mathrm{JC}}$ is rated @ $1.4^{\circ} \mathrm{C} / \mathrm{W}$ for the CS5207A-1. For a high current regulator such as the CS5207A-1 the majority of heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while the $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $R_{\Theta J A}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 1.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5257A-1

### 7.0 A LDO 5-Pin Adjustable Linear Regulator

This new very low dropout regulator is designed to power the next generation of advanced microprocessors. To achieve very low dropout, the internal pass transistor is powered separately from the control circuitry. Furthermore, with the control and power inputs tied together, this device can be used in single supply configuration and still offer a better dropout voltage than conventional PNP-NPN based LDO regulators. In this mode the dropout is determined by the minimum control voltage.

It is supplied in five-terminal TO-220 and $\mathrm{D}^{2}$ PAK packages, allowing for the implementation of a remote-sense pin permitting very accurate regulation of output voltage directly at the load, where it counts, rather than at the regulator. This remote sensing feature virtually eliminates output voltage variations due to load changes and resistive voltage drops. Typical load regulation measured at the sense pin is 1.0 mV for an output voltage of 2.5 V with a load step of 10 mA to 7.0 A .

The very fast transient loop response easily meets the needs of the latest microprocessors. In addition, a small capacitor on the Adjust pin will further improve the transient capabilities.

Internal protection circuitry provides for "bust-proof" operation, similar to three-terminal regulators. This circuitry, which includes overcurrent, short circuit, supply sequencing and overtemperature protection will self protect the regulator under all fault conditions.

The CS5257A-1 is ideal for generating a secondary $2.0-2.5 \mathrm{~V}$ low voltage supply on a motherboard where both 5.0 V and 3.3 V are already available.

## Features

- 1.25 V to $5.0 \mathrm{~V} \mathrm{~V}_{\text {OUT }}$ at 7.0 A
- $\mathrm{V}_{\text {POWER }}$ Dropout < 0.35 V @ 7.0 A
- $\mathrm{V}_{\text {CONTROL }}$ Dropout < $1.1 \mathrm{~V} @ 7.0 \mathrm{~A}$
- $1.5 \%$ Trimmed Reference
- Fast Transient Response
- Remote Voltage Sensing
- Thermal Shutdown
- Current Limit
- Short Circuit Protection
- Drop-In Replacement for LT1580
- Backwards Compatible with 3-Pin Regulators

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


MARKING DIAGRAMS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5257A-1GT5 | TO-220 <br> FIVE LEAD | 50 Units/Rail |
| CS5257A-1GDP5 | D²PAK* $^{*}$ | 50 Units/Rail |
| CS5257A-1GDPR5 | D²PAK* $^{*}$ | 750 Tape \& Reel |

*5-Pin.


Figure 1. Application Diagram

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| $V_{\text {POWER }}$ Input Voltage |  | 6.0 | V |
| $\mathrm{V}_{\text {CONTROL }}$ Input Voltage |  | 13 | V |
| Operating Junction Temperature Range, $\mathrm{T}_{\mathrm{J}}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold |  | 2.0 | kV |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 peak 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C} ; \mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\text {OUT }}\right.$ and $\mathrm{V}_{\text {ADJ }}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

CS5257A-1

| Reference Voltage | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \text {, } \\ & 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 7.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.234 \\ (-1.5 \%) \end{gathered}$ | 1.253 | $\begin{gathered} 1.272 \\ (+1.5 \%) \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.5 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=1.75 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \end{aligned}$ | - | 0.02 | 0.2 | \% |
| Load Regulation (Note 3) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \text { to } 7.0 \mathrm{~A} \text {, with Remote Sense } \end{aligned}$ | - | 0.04 | 0.2 | \% |
| Minimum Load Current (Note 4) | $\mathrm{V}_{\text {CONTROL }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.3 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=+1.0 \%$ | - | 5.0 | 10 | mA |
| Control Pin Current (Note 5) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \text { IOUT }=100 \mathrm{~mA} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \text { IOUT }=4.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=1.75 \mathrm{~V}, \text { IOUT }=4.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \text { IOUT }=7.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 30 \\ & 33 \\ & 60 \end{aligned}$ | $\begin{gathered} 10 \\ 60 \\ 70 \\ 180 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Adjust Pin Current | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 60 | 120 | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=-1.5 \%$ | 7.1 | 10 | - | A |

3. This parameter is guaranteed by design and is not $100 \%$ production tested.
4. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum load current requirement.
5. The $\mathrm{V}_{\text {CONTROL }}$ pin current is the drive current required for the output transistor. This current will track output current with roughly a $1: 100$ ratio. The minimum value is equal to the quiescent current of the device.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}\right.$; $\mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\text {OUT }}$ and $\mathrm{V}_{\text {ADJ }}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## CS5257A-1

| Short Circuit Current | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.05 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | 5.0 | 9.0 | - | A |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Ripple Rejection (Note 6) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=\mathrm{V}_{\text {POWER }}=3.25 \mathrm{~V} \\ & \mathrm{~V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\mathrm{P}-\mathrm{P}} @ 120 \mathrm{~Hz} \text {, I IOUT }=4.0 \mathrm{~A}, \\ & \mathrm{C}_{\text {ADJ }}=0.1 \mu \mathrm{~F} \end{aligned}$ | 60 | 80 | - | dB |
| Thermal Regulation | 30 ms Pulse, $\mathrm{T}_{\text {A }}=25^{\circ} \mathrm{C}$ | - | 0.002 | - | \%/W |
| Vcontrol Dropout Voltage (Minimum $\left.\mathrm{V}_{\text {CONTROL }}-\mathrm{V}_{\text {OUT }}\right)$ (Note 7) | $V_{\text {POWER }}=2.05 \mathrm{~V}$, IOUT $=100 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {POWER }}=2.05 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=1.0 \mathrm{~A}$ <br> $\mathrm{V}_{\text {POWER }}=2.05 \mathrm{~V}$, IOUT $=2.75 \mathrm{~A}$ <br> $\mathrm{V}_{\text {POWER }}=2.05 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=4.0 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {POWER }}=2.05 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=7.0 \mathrm{~A}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & 1.00 \\ & 1.00 \\ & 1.00 \\ & 1.00 \\ & 1.10 \end{aligned}$ | $\begin{aligned} & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.25 \end{aligned}$ | $\begin{aligned} & V \\ & V \\ & V \\ & V \\ & V \end{aligned}$ |
| V POWER Dropout Voltage (Minimum VPOWER - V ${ }_{\text {OUT }}$ ) (Note 7) | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=100 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, IOUT $=1.0 \mathrm{~A}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=2.75 \mathrm{~A}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=4.0 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, IOUT $=7.0 \mathrm{~A}$ |  | $\begin{aligned} & 0.10 \\ & 0.15 \\ & 0.20 \\ & 0.26 \\ & 0.35 \end{aligned}$ | $\begin{aligned} & 0.15 \\ & 0.20 \\ & 0.30 \\ & 0.40 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & V \\ & V \\ & V \\ & V \\ & V \end{aligned}$ |
| RMS Output Noise | Freq $=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Temperature Stability | - | - | 0.5 | - | \% |
| Thermal Shutdown (Note 8) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | - | 25 | ${ }^{\circ} \mathrm{C}$ |
| VCONTRoL Supply Only Output Current | $\mathrm{V}_{\text {CONTROL }}=13 \mathrm{~V}$, $\mathrm{V}_{\text {POWER }}$ Not Connected, $V_{\text {ADJ }}=V_{\text {OUT }}=V_{\text {SENSE }}=0 \mathrm{~V}$ | - | - | 50 | mA |
| VPOWER Supply Only Output Current | $\begin{aligned} & \mathrm{V}_{\text {POWER }}=6.0 \mathrm{~V}, \mathrm{~V}_{\text {CONTROL }} \text { Not Connected, }, \\ & \mathrm{V}_{\text {ADJ }}=\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SENSE }}=0 \mathrm{~V} \end{aligned}$ | - | 0.1 | 1.0 | mA |

6. This parameter is guaranteed by design and is not $100 \%$ production tested.
7. Dropout is defined as either minimum control voltage ( $\mathrm{V}_{\text {CONTROL }}$ ) or minimum power voltage ( $\mathrm{V}_{\text {POWER }}$ ) to output voltage differential required to maintain $1.5 \%$ regulation at a particular load.
8. This parameter is guaranteed by design, but not parametrically tested in production. However, a $100 \%$ thermal shutdown functional test is performed on each part.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| TO-220 | D2PAK |  |  |
| 1 | 1 | $\mathrm{V}_{\text {SENSE }}$ | This Kelvin sense pin allows for remote sensing of the output voltage at the load for improved regulation. It is internally connected to the positive input of the voltage sensing error amplifier. |
| 2 | 2 | Adjust | This pin is connected to the low side of the internally trimmed $1.5 \%$ bandgap reference voltage and carries a bias current of about $50 \mu \mathrm{~A}$. A resistor divider from Adjust to $\mathrm{V}_{\text {OUT }}$ and from Adjust to ground sets the output voltage. Also, transient response can be improved by adding a small bypass capacitor from this pin to ground. |
| 3 | 3 | $\mathrm{V}_{\text {OUT }}$ | This pin is connected to the emitter of the power pass transistor and provides a regulated voltage capable of sourcing 7.0 A of current. |
| 4 | 4 | $\mathrm{V}_{\text {CONTROL }}$ | This is the supply voltage for the regulator control circuitry. For the device to regulate, this voltage should be between 1.0 V and 1.25 V (depending on the output current) greater than the output voltage. The control pin current will be about $1.0 \%$ of the power pin output current. |
| 5 | 5 | $\mathrm{V}_{\text {POWER }}$ | This is the power input voltage. This pin is physically connected to the collector of the power pass transistor. For the device to regulate, this voltage should be between 0.1 V and 0.65 V greater than the output voltage depending on the output current. The output load current of 7.0 A is supplied through this pin. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Reference Voltage vs Temperature


Figure 5. Transient Response


Figure 4. Load Regulation vs Output Current


Figure 6. Short Circuit Current vs $\mathrm{V}_{\text {POWER }}-\mathrm{V}_{\text {OUT }}$


Figure 7. Adjust Pin Current vs Temperature


Figure 9. Adjust Pin Current vs $\mathrm{V}_{\text {control }}$ - $\mathrm{V}_{\text {OUT }}$

Figure 11. Adjust Pin Current vs $\mathrm{V}_{\text {POWER }}-\mathrm{V}_{\text {OUT }}$


Figure 8. Minimum Load Current vs $\mathrm{V}_{\text {CONTROL }}-\mathrm{V}_{\text {OUT }}$


Figure 10. Ripple Rejection vs Frequency


Figure 12. $\mathrm{V}_{\text {CONTROL }}$ Dropout Voltage vs IOUT


Figure 13. VPOwER Dropout Voltage vs Iout


Figure 15. Adjust Pin Current vs Output Current

## APPLICATIONS NOTES

## THEORY OF OPERATION

The CS5257A-1 linear regulator provides adjustable voltages from 1.25 V to 5.0 V at currents up to 7.0 A . The regulator is protected against short circuits, and includes a thermal shutdown circuit with hysteresis. The output, which is current limited, consists of a PNP-NPN transistor pair and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## $V_{\text {POWER }}$ Function

The CS5257A-1 utilizes a two supply approach to maximize efficiency. The collector of the power device is brought out to the $\mathrm{V}_{\text {POWER }}$ pin to minimize internal power dissipation under high current loads. $\mathrm{V}_{\text {CONTROL }}$ provides power for the control circuitry and the drive for the output NPN transistor. $\mathrm{V}_{\text {CONTROL }}$ should be at least 1.0 V greater than the output voltage. Special care has been taken to ensure
that there are no supply sequencing problems. The output voltage will not turn on until both supplies are operating. If the control voltage comes up first, the output current will be typically limited to about 3.0 mA until the power input voltage comes up. If the power input voltage comes up first the output will not turn on at all until the control voltage comes up. The output can never come up unregulated.

The CS5257A-1 can also be used as a single supply device with the control and power inputs tied together. In this mode, the dropout will be determined by the minimum control voltage.

## Output Voltage Sensing

The CS5257A-1 five terminal linear regulator includes a dedicated $\mathrm{V}_{\text {SENSE }}$ function. This allows for true Kelvin sensing of the output voltage. This feature can virtually eliminate errors in the output voltage due to load regulation.

Regulation will be optimized at the point where the sense pin is tied to the output.

## DESIGN GUIDELINES

## Adjustable Operation

This LDO adjustable regulator has an output voltage range of 1.25 V to 5.0 V . An external resistor divider sets the output voltage as shown in Figure 16. The regulator's voltage sensing error amplifier maintains a fixed 1.253 V reference between the output pin and the adjust pin.


Figure 16. An External Resistor Divider Sets the Value of $V_{\text {OUt }}$. The 1.253 V Reference Voltage Drops Across R1.
A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.253 V across R 1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary. The output voltage is set according to the formula:

$$
\mathrm{VOUT}=1.253 \mathrm{~V} \times \frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}+\mathrm{R} 2 \times \mathrm{I}_{\mathrm{AD}} \mathrm{~J}
$$

The term $\mathrm{I}_{\mathrm{ADJ}} \times \mathrm{R} 2$ represents the error added by the adjust pin current. R1 is chosen so that the minimum load current is a least 10 mA . R1 and R2 should be of the same composition for best tracking over temperature. The divider resistors should be placed physically as close to the load as possible.

While not required, a bypass capacitor connected between the adjust pin and ground will improve transient response and ripple rejection. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Value and type may be varied to optimize performance vs. price.

## Other Adjustable Operation Considerations

The CS5257A-1 linear regulator has an absolute maximum specification of 6.0 V for the voltage difference between $V_{\text {IN }}$ and Vout. However, the IC may be used to regulate voltages in excess of 6.0 V . The two main considerations in such a design are the sequencing of power supplies and short circuit capability.

Power supply sequencing should be such that the $\mathrm{V}_{\text {CONTROL }}$ supply is brought up coincidentally with or before the $\mathrm{V}_{\text {POWER }}$ supply. This allows the IC to begin charging the output capacitor as soon as the $\mathrm{V}_{\text {POWER }}$ to $V_{\text {OUT }}$ differential is large enough that the pass transistor conducts. As VPOWER increases, the pass transistor will remain in dropout, and current is passed to the load until $\mathrm{V}_{\text {OUT }}$ is in regulation. Further increase in the supply voltage brings the pass transistor out of dropout. In this manner, any output voltage less than 13 V may be regulated, provided the $\mathrm{V}_{\text {POWER }}$ to $\mathrm{V}_{\text {OUT }}$ differential is less than 6.0 V . In the case where $\mathrm{V}_{\text {CONTROL }}$ and $\mathrm{V}_{\text {POWER }}$ are shorted, there is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {POWER }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 6.0 V is not exceeded.
There is a possibility of damaging the IC when $V_{\text {POWER }}$ $-\mathrm{V}_{\text {IN }}$ is greater than 6.0 V if a short circuit occurs. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Overvoltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp the $\mathrm{V}_{\text {POWER }}$ to $\mathrm{V}_{\text {OUT }}$ differential to less than 6.0 V if fail safe operation is required. One possible clamp circuit is illustrated in Figure 17; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit condition indefinitely while protecting the IC.


Figure 17. Example Clamp Circuitry for $V_{\text {POWER }}-V_{\text {OUT }}>6.0 \mathrm{~V}$

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.
The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The
aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $300 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5257A-1 the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage, and the rate at which $\mathrm{V}_{\text {CONTROL }}$ drops. In the CS5257A-1 regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 18 is recommended.


Figure 18. Diode Protection Against $\mathrm{V}_{\text {control }}$ Short Circuit Conditions

Use of the diode has the added benefit of bleeding $\mathrm{V}_{\text {OUT }}$ to ground if $\mathrm{V}_{\text {CONTROL }}$ is shorted. This prevents an unregulated output from causing system damage.

A rule of thumb useful in determining if a protection diode is required is to solve for current

$$
\mathrm{I}=\frac{\mathrm{C} \times \mathrm{V}}{\mathrm{~T}}
$$

where:
I is the current flow out of the load capacitance when $\mathrm{V}_{\text {CONTROL }}$ is shorted,
C is the value of load capacitance,
V is the output voltage, and
T is the time duration required for $\mathrm{V}_{\text {CONTROL }}$ to transition from high to being shorted.
If the calculated current is greater than or equal to the typical short circuit current value provided in the specifications, serious thought should be given to the use of a protection diode.

## Current Limit

The internal current limit circuit limits the output current under excessive load conditions.

## Short Circuit Protection

The device includes short circuit protection circuitry that clamps the output current at approximately two amperes less than its current limit value. This provides for a current foldback function, which reduces power dissipation under a direct shorted load.

## Thermal Shutdown

The thermal shutdown circuitry is guaranteed by design to activate above a die junction temperature of approximately $150^{\circ} \mathrm{C}$ and to shut down the regulator output. This circuitry has $25^{\circ} \mathrm{C}$ of typical hysteresis, thereby allowing the regulator to recover from a thermal fault automatically.

## Calculating Power Dissipation and Heat Sink Requirements

High power regulators such as the CS5257A-1 usually operate at high junction temperatures. Therefore, it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used. Since the package tab is connected to $\mathrm{V}_{\text {OUT }}$ on the CS5257A-1, electrical isolation may be required for some applications. Also, as with all high power packages, thermal compound in necessary to ensure proper heat flow. For added safety, this high current LDO includes an internal thermal shutdown circuit.
The thermal characteristics of an IC depend on the following four factors: junction temperature, ambient temperature, die power dissipation, and the thermal resistance from the die junction to ambient air. The maximum junction temperature can be determined by:

$$
\mathrm{T}_{\mathrm{J}(\max )}=\mathrm{T}_{\mathrm{A}(\max )}+\mathrm{PD}_{(\max )} \times \mathrm{R}_{\Theta \mathrm{JA}}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the
maximum junction temperature and the thermal resistance depend on the manufacturer and the package type. The maximum power dissipation for a regulator is:

$$
\begin{aligned}
\mathrm{PD}_{(\max )}= & \left(\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{VOUT}_{\text {(min })}\right) \operatorname{IOUT}(\max ) \\
& +\mathrm{VIN}_{\operatorname{IN}(\max )} \times \operatorname{IIN}(\max )
\end{aligned}
$$

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment has a thermal resistance which is measured in degrees per watt. Like series electrical resistances, these thermal resistances are summed to determine the total thermal resistance between the die junction and the surrounding air, $\mathrm{R}_{\Theta J A}$. This total thermal resistance is comprised of three components. These resistive terms are measured from junction to case $\left(\mathrm{R}_{\Theta \mathrm{JC}}\right)$, case to heat sink $\left(\mathrm{R}_{\Theta C S}\right)$, and heat sink to ambient air $\left(\mathrm{R}_{\Theta S A}\right)$. The equation is:

$$
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A}
$$

The value for $\mathrm{R}_{\Theta \mathrm{JC}}$ is $1.4^{\circ} \mathrm{C} /$ watt for the CS5257A-1 in both the TO-220 and D ${ }^{2}$ PAK packages. For a high current regulator such as the CS5257A-1 the majority of heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while the $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see our application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

PACKAGE THERMAL DATA

| Parameter |  | TO-220 Five Lead | D$^{2}$ PAK, 5-Pin | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 1.4 | 1.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$.

## CS5208-1

### 8.0 A LDO 3-Pin Adjustable Linear Regulator

The CS5208-1 linear regulator provides 8.0 A at adjustable voltages from 1.25 V to 4.5 V . This adjustable device requires two external resistors to set the output voltage and provide the minimum load current for proper regulation.

This regulator is intended for use as a post regulator and microprocessor supply. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage operation and good transient response are important.

The circuit is designed to operate with dropout voltages as low as 1.0 V at 8.0 A .

The regulator is protected against overload conditions with overcurrent and thermal shutdown protection circuitry.

The regulator is available in a TO-220 package.

## Features

- 1.25 V to $4.5 \mathrm{~V}_{\text {OUT }}$ at 8.0 A
- Dropout Voltage < 1.0 V @ 8.0 A
- $1.5 \%$ Trimmed Reference
- Fast Transient Response
- Thermal Shutdown
- Current Limit
- Short Circuit Protection


Figure 1. Applications Diagram
ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com

TO-220
THREE LEAD
T SUFFIX
CASE 221A
PIN CONNECTIONS AND MARKING DIAGRAMS

$\mathrm{Tab}=\mathrm{V}_{\text {OUT }}$
Pin 1. Adjust
2. $\mathrm{V}_{\text {OUT }}$
3. $\mathrm{V}_{\mathrm{IN}}$
A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week
ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5208-1GT3 | TO-220* | 50 Units/Rail |

*TO-220 is 3-pin, straight leaded.

ABSOLUTE MAXIMUM RATINGS*

|  | Parameter | Value |
| :--- | :---: | :---: |
| Input Voltage | Unit |  |
| Operating Junction Temperature Range | 6.0 | V |
| Storage Temperature Range | $0 \leq \mathrm{T}_{\mathrm{J}} \leq 150$ | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Dave Solder (through hole styles only) Note 1 | 260 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C}, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, \mathrm{V}_{\text {Adj }}=0 \mathrm{~V}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Adjustable Output Voltage

| Reference Voltage | $\begin{aligned} & \mathrm{V}_{\text {IN }}=2.75 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \text { to } 8.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.234 \\ (-1.5 \%) \end{gathered}$ | 1.253 | $\begin{gathered} 1.271 \\ (+1.5 \%) \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}$ to 5.5 V , $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 0.02 | 0.20 | \% |
| Load Regulation | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}$, $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}$ to 8.0 A | - | 0.04 | 0.50 | \% |
| Minimum Load Current (Note 2) | $\mathrm{V}_{\text {IN }}=5.0 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=+1.5 \%$ | - | 5.0 | 10 | mA |
| Adjust Pin Current | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$ | - | 70 | 120 | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=-1.5 \%$ | 8.1 | 9.0 | - | A |
| Short Circuit Current | $\mathrm{V}_{\text {IN }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | 6.0 | 8.5 | - | A |
| Ripple Rejection (Note 3) | $\begin{gathered} \mathrm{V}_{\text {IN }}=3.25 \mathrm{VAvg}, \mathrm{~V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {P-P }} @ 120 \mathrm{~Hz}, \\ \mathrm{I}_{\text {OUT }}=4.0 \mathrm{~A}, \mathrm{C}_{\text {Adj }}=0.1 \mu \mathrm{~F} ; \mathrm{C}_{\text {OUT }}=22 \mu \mathrm{~F} \end{gathered}$ | 60 | 80 | - | dB |
| Thermal Regulation (Note 3) | $30 \mathrm{~ms} \mathrm{Pulse}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | - | \%/W |
| Dropout Voltage (Minimum $\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\text {OUT }}$ ) (Note 4) | $\begin{aligned} & \text { IOUT }=100 \mathrm{~mA} \\ & \text { IOUT }=1.0 \mathrm{~A} \\ & \text { IOUT }=2.75 \mathrm{~A} \\ & \text { IOUT }=4.0 \mathrm{~A} \\ & \text { IOUT }=8.0 \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 0.92 \\ & 0.93 \\ & 0.94 \\ & 0.95 \\ & 0.96 \end{aligned}$ | $\begin{aligned} & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.30 \end{aligned}$ | V V V V V |
| RMS Output Noise | Freq $=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \% $\mathrm{V}_{\text {OUT }}$ |
| Temperature Stability | - | - | 0.5 | - | \% |
| Thermal Shutdown (Note 5) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis (Note 5) | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

2. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum load current requirement.
3. This parameter is guaranteed by design and is not $100 \%$ production tested.
4. Dropout voltage is defined as the minimum input/output voltage differential required to maintain $1.5 \%$ regulation.
5. This parameter is guaranteed by design, but not parametrically tested in production. However, a $100 \%$ thermal shutdown functional test is performed on each part.

## CS5208-1

PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |
| :---: | :---: | :--- |
| TO-220 | Pin Symbol |  |
| 1 | Adjust | This pin is connected to the low side of the internally trimmed $1.5 \%$ bandgap reference <br> voltage and carries a bias current of about $70 \mu \mathrm{~A}$. A resistor divider from Adj to $\mathrm{V}_{\text {OUT }}$ and from <br> Adj to ground sets the output voltage. Also, transient response can be improved by adding a <br> small bypass capacitor from this pin to ground. |
| 2 | $\mathrm{~V}_{\text {OUT }}$ | This pin is connected to the emitter of the power pass transistor and provides a regulated <br> voltage capable of sourcing 8.0 A of current. |
| 3 | $\mathrm{~V}_{\mathrm{IN}}$ | This is the supply voltage for the regulator. For the device to regulate, this voltage should be <br> between 1.1 V and 1.30 V (depending on the output current) greater than the output voltage. |



Figure 2. Block Diagram

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. Reference Voltage vs. Temperature


Figure 4. Load Regulation vs. Output Current


Figure 5. Adjust Pin Current vs. Temperature


Figure 7. Dropout Voltage vs. Output Current


Figure 9. Minimum Load Current vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$


Figure 6. Adjust Pin vs. IOUT


Figure 8. Short Circuit vs. $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$


Figure 10. Ripple Rejection vs. Frequency

## APPLICATION NOTES

## THEORY OF OPERATION

The CS5208-1 linear regulator has a composite PNP-NPN output stage that requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## ADJUSTABLE OPERATION

## Design Guidelines

This LDO adjustable regulator has an output voltage range of 1.25 V to 4.5 V . An external resistor divider sets the output voltage as shown in Figure 11. The regulator's voltage sensing error amplifier maintains a fixed 1.25 V reference between the output pin and the adjust pin.

A resistor divider network $R_{1}$ and $R_{2}$ causes a fixed current to flow to ground. This current creates a voltage across $\mathrm{R}_{2}$ that adds to the 1.25 V across $\mathrm{R}_{1}$ and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through $\mathrm{R}_{2}$ and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary. The output voltage is set according to the formula:

$$
V_{\text {OUT }}=V_{\text {REF }} \times\left(\frac{R_{1}+R_{2}}{R_{1}}\right)+R_{2} \times I_{A d j}
$$

The term $\mathrm{I}_{\mathrm{Adj}} \times \mathrm{R}_{2}$ represents the error added by the adjust pin current.
$\mathrm{R}_{1}$ is chosen so that the minimum load current is at least 10 mA . $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ should be of the same composition for best tracking over temperature. The divider resistors should be placed as close to the IC as possible and connected to the output with a seperate metal trace.


Figure 11.
While not required, a bypass capacitor connected between the adjust pin and ground will improve transient response and ripple rejection. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Value and type may be varied to optimize performance vs price.

OTHER ADJUSTABLE OPERATION CONSIDERATIONS
The CS5208-1 linear regulator has an absolute maximum specification of 6.0 V for the voltage difference between $\mathrm{V}_{\text {IN }}$ and $\mathrm{V}_{\text {OUT }}$. However, the IC may be used to regulate voltages in excess of 6.0 V . The main considerations in such a design are power-up and short circuit capability.
In most applications, ramp-up of the power supply to $\mathrm{V}_{\text {IN }}$ is fairly slow, typically on the order of several tens of milliseconds, while the regulator responds in less than one microsecond. In this case, the linear regulator begins charging the output capacitor as soon as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential is large enough that the pass transistor conducts current. V ${ }_{\text {OUT }}$ is essentially at ground, and $\mathrm{V}_{\text {IN }}$ is on the order of several hundred millivolts, so the pass transistor is in dropout. As $\mathrm{V}_{\text {IN }}$ increases, the pass transistor will remain in dropout, and current is passed to the load until $\mathrm{V}_{\text {OUT }}$ is in regulation. Further increase in $\mathrm{V}_{\text {IN }}$ brings the pass transistor out of dropout. The result is that the output voltage follows the power supply ramp-up, staying in dropout until the regulation point is reached. In this manner, any output voltage may be regulated. There is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 6.0 V is not exceeded.

However, the maximum ratings of the IC will be exceeded in a short circuit condition. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Over-voltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp $\mathrm{V}_{\text {IN }}$ to $\mathrm{V}_{\text {OUT }}$ differential to less than 6.0 V if failsafe operation is required. One possible clamp circuit is illustrated in Figure 12; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit conditions indefinitely while protecting the IC.


Figure 12.

## STABILITY CONSIDERATIONS

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.

The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $300 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5208-1 the transient response and stability improve with higher values of capacitance. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which $\mathrm{V}_{\mathrm{IN}}$ drops. In the CS5208-1 regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 13 is recommended.

A rule of thumb useful in determining if a protection diode is required is to solve for current

$$
\mathrm{I}=\frac{\mathrm{C} \times \mathrm{V}}{\mathrm{~T}}
$$

where:
I is the current flow out of the load capacitance when $\mathrm{V}_{\mathrm{IN}}$ is shorted,
C is the value of the load capacitance,
V is the output voltage, and
T is the time duaration required for $\mathrm{V}_{\text {IN }}$ to transition from high to being shorted.

If the calculated current is greater than or equal to the typical short circuit current value provided in the specifications, serious thought should be given to including a protection diode.


Figure 13.

## Current Limit

The internal current limit circuit limits the output current under excessive load conditions and protects the regulator.

## Short Circuit Protection

The device includes foldback short circuit current limit that clamps the output current at approximately two amperes less than its current limit value.

## Thermal Shutdown

The thermal shutdown circuitry is guaranteed by design to become activated above a die junction temperature of $150^{\circ} \mathrm{C}$ and to shut down the regulator output. This circuitry includes a thermal hysteresis circuit with $25^{\circ} \mathrm{C}$ of typical hysteresis, thereby allowing the regulator to recover from a thermal fault automatically.

## Calculating Power Dissipation and Heat Sink Requirements

High power regulators such as the CS5208-1 usually operate at high junction temperatures. Therefore, it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used. Since the package tab is connected to $\mathrm{V}_{\text {OUT }}$ on the CS5208-1, electrical isolation may be required for some applications. Also, as with all high power packages, thermal compound is necessary to ensure proper heat flow. For added safety, this high current LDO includes an internal thermal shutdown circuit
The thermal characteristics of an IC depend on the following four factors. Junction temperature, ambient temperature, die power dissipation, and the thermal resistance from the die junction to ambient air. The maximum junction temperature can be determined by:

$$
\mathrm{T}_{\mathrm{J}(\max )}=\mathrm{T}_{\mathrm{A}(\max )}+\mathrm{P}_{\mathrm{D}(\max )} \times \mathrm{R}_{\Theta \mathrm{JA}}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type. The maximum power dissipation for a regulator is:

$$
\mathrm{P}_{\mathrm{D}(\max )}=\left(\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{V}_{\mathrm{OUT}(\min )}\right) \mathrm{IOUT}_{\mathrm{O}}(\max )+\mathrm{V}_{\mathrm{IN}(\max )} \times \mathrm{I}_{\mathrm{IN}(\max )}
$$

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment has a thermal resistance. Like series electrical resistances, these resistances are summed to determine the total thermal resistance between the die junction and the surrounding air, $\mathrm{R}_{\Theta \mathrm{JC}}$. This total thermal resistance is comprised of three components. These resistive terms are measured from junction to case ( $\mathrm{R}_{\Theta J C}$ ), case to heat sink ( $\mathrm{R}_{\Theta C S}$ ), and heat sink to ambient air ( $\mathrm{R}_{\Theta S A}$ ). The equation is:

$$
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A}
$$

$\mathrm{R}_{\Theta \mathrm{JC}}$ is rated @ $1.4^{\circ} \mathrm{C} / \mathrm{W}$ for the CS5208-1. For a high current regulator such as the CS5208-1 the majority of heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while the $\mathrm{R}_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $R_{\Theta J A}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://onsemi.com.

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> THREE LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 1.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5258-1

### 8.0 A LDO 5-Pin Adjustable Linear Regulator

This new very low dropout regulator is designed to power the next generation of advanced microprocessors. To achieve very low dropout, the internal pass transistor is powered separately from the control circuitry. Furthermore, with the control and power inputs tied together, this device can be used in single supply configuration and still offer a better dropout voltage than conventional PNP-NPN based LDO regulators. In this mode the dropout is determined by the minimum control voltage.

It is supplied in a five-terminal TO-220 package, which allows for the implementation of a remote-sense pin permitting very accurate regulation of output voltage directly at the load, where it counts, rather than at the regulator. This remote sensing feature virtually eliminates output voltage variations due to load changes and resistive voltage drops. Typical load regulation measured at the sense pin is 1.0 mV for an output voltage of 2.5 V with a load step of 10 mA to 8.0 A .

The very fast transient loop response easily meets the needs of the latest microprocessors. In addition, a small capacitor on the Adjust pin will further improve the transient capabilities.

Internal protection circuitry provides for "bust-proof" operation, similar to three-terminal regulators. This circuitry, which includes overcurrent, short circuit, supply sequencing and overtemperature protection, will self protect the regulator under all fault conditions.

The CS5258-1 is ideal for generating a secondary $2.0-2.5 \mathrm{~V}$ low voltage supply on a motherboard where both 5.0 V and 3.3 V are already available.

## Features

- 1.25 V to $5.0 \mathrm{~V} \mathrm{~V}_{\text {OUT }}$ at 8.0 A
- VPOWER Dropout < 0.4 V @ 8.0 A
- $V_{\text {CONTROL }}$ Dropout < 1.15 V @ 8.0 A
- $1.5 \%$ Trimmed Reference
- Fast Transient Response
- Remote Voltage Sensing
- Thermal Shutdown
- Current Limit
- Short Circuit Protection
- Backwards Compatible with 3-Pin Regulators

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com

$\mathrm{Tab}=\mathrm{V}_{\text {OUT }}$
Pin 1. V ${ }_{\text {SENSE }}$
2. Adjust
3. $\mathrm{V}_{\text {OUT }}$
4. $\mathrm{V}_{\text {CONTROL }}$
5. VPOWER

TO-220
FIVE LEAD
T SUFFIX
CASE 314D


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5258-1GT5 | TO-220 <br> FIVE LEAD | 50 Units/Rail |



Figure 1. Application Diagram

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| V POWER Input Voltage |  | 6.0 | V |
| $\mathrm{V}_{\text {CONTROL }}$ Input Voltage |  | 13 | V |
| Operating Junction Temperature Range, $\mathrm{T}_{J}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold |  | 2.0 | kV |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 | 260 peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C} ; \mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\mathrm{OUT}}\right.$ and $\mathrm{V}_{\text {ADJ }}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS5258-1 |  |  |  |  |  |
| Reference Voltage | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \text {, } \\ & 10 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 8.0 \mathrm{~A} \end{aligned}$ | $\begin{gathered} 1.234 \\ (-1.5 \%) \end{gathered}$ | 1.253 | $\begin{gathered} 1.272 \\ (+1.5 \%) \end{gathered}$ | V |
| Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.5 \mathrm{~V} \text { to } 12 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=1.75 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \\ & \mathrm{I}_{\text {OUT }}=10 \mathrm{~mA} \end{aligned}$ | - | 0.02 | 0.2 | \% |
| Load Regulation (Note 2) | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V}$, <br> IOUT $=10 \mathrm{~mA}$ to 8.0 A , with Remote Sense | - | 0.04 | 0.2 | \% |
| Minimum Load Current (Note 3) | $\mathrm{V}_{\text {CONTROL }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=3.3 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=+1.0 \%$ | - | 5.0 | 10 | mA |
| Control Pin Current (Note 4) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V}, \text { IOUT }=100 \mathrm{~mA} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V}, \text { IOUT }=4.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=1.75 \mathrm{~V}, \text { IOUT }=4.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V}, \text { IOUT }=8.0 \mathrm{~A} \end{aligned}$ |  | $\begin{aligned} & 6.0 \\ & 30 \\ & 33 \\ & 80 \end{aligned}$ | $\begin{gathered} 10 \\ 60 \\ 70 \\ 180 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Adjust Pin Current | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V}$, IOUT $=10 \mathrm{~mA}$ | - | 60 | 120 | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V}, \Delta \mathrm{~V}_{\text {OUT }}=-1.5 \%$ | 8.1 | 10 | - | A |
| Short Circuit Current | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {POWER }}=2.15 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | 6.0 | 9.0 | - | A |

2. This parameter is guaranteed by design and is not $100 \%$ production tested.
3. The minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum load current requirement.
4. The $\mathrm{V}_{\text {CONTROL }}$ pin current is the drive current required for the output transistor. This current will track output current with roughly a 1:100 ratio. The minimum value is equal to the quiescent current of the device.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}\right.$; $\mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\text {OUT }}$ and $\mathrm{V}_{\text {ADJ }}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

CS5258-1

| Ripple Rejection (Note 5) | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=\mathrm{V}_{\text {POWER }}=3.25 \mathrm{~V} \mathrm{Avg} \\ & \mathrm{~V}_{\text {RIPPLE }}=1.0 \mathrm{~V}_{\text {P-P }} @ 120 \mathrm{~Hz} \text {, I } \\ & \mathrm{C}_{\text {ADJ }}=4.0 \mathrm{~A}, \end{aligned}$ | 60 | 80 | - | dB |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Thermal Regulation | $30 \mathrm{~ms} \mathrm{Pulse}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.002 | - | \%/W |
| $V_{\text {CONTROL }}$ Dropout Voltage (Minimum $\mathrm{V}_{\text {CONTROL }}-\mathrm{V}_{\text {OUT }}$ ) (Note 6) | $\mathrm{V}_{\text {POWER }}=2.15 \mathrm{~V}$, IOUT $=100 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {POWER }}=2.15 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=1.0 \mathrm{~A}$ <br> $\mathrm{V}_{\text {POWER }}=2.15 \mathrm{~V}$, IOUT $=2.75 \mathrm{~A}$ <br> $\mathrm{V}_{\text {POWER }}=2.15 \mathrm{~V}$, IOUT $=4.0 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {POWER }}=2.15 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=8.0 \mathrm{~A}$ |  | $\begin{aligned} & 1.00 \\ & 1.00 \\ & 1.00 \\ & 1.00 \\ & 1.15 \end{aligned}$ | $\begin{aligned} & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.15 \\ & 1.30 \end{aligned}$ | $\begin{aligned} & V \\ & V \\ & V \\ & V \\ & V \end{aligned}$ |
| $V_{\text {POWER }}$ Dropout Voltage (Minimum $\mathrm{V}_{\text {POWER }}$ - $\mathrm{V}_{\text {OUT }}$ ) (Note 6) | $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=100 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, IOUT $=1.0 \mathrm{~A}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=2.75 \mathrm{~A}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=4.0 \mathrm{~mA}$ <br> $\mathrm{V}_{\text {CONTROL }}=2.75 \mathrm{~V}$, IOUT $=8.0 \mathrm{~A}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 0.10 \\ & 0.15 \\ & 0.20 \\ & 0.26 \\ & 0.40 \end{aligned}$ | $\begin{aligned} & 0.15 \\ & 0.20 \\ & 0.30 \\ & 0.40 \\ & 0.70 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| RMS Output Noise | Freq $=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.003 | - | \%V $\mathrm{V}_{\text {OUT }}$ |
| Temperature Stability | - | - | 0.5 | - | \% |
| Thermal Shutdown (Note 7) | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |
| $V_{\text {Control }}$ Supply Only Output Current | $\begin{aligned} & \mathrm{V}_{\text {CONTROL }}=13 \mathrm{~V}, \mathrm{~V}_{\text {POWER }} \text { Not Connected, } \\ & \mathrm{V}_{\text {ADJ }}=\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SENSE }}=0 \mathrm{~V} \end{aligned}$ | - | - | 50 | mA |
| VPower Supply Only Output Current | $\begin{aligned} & \mathrm{V}_{\text {POWER }}=6.0 \mathrm{~V}, \mathrm{~V}_{\text {CONTROL }} \text { Not Connected }, \\ & \mathrm{V}_{\text {ADJ }}=\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SENSE }}=0 \mathrm{~V} \end{aligned}$ | - | 0.1 | 1.0 | mA |

5. This parameter is guaranteed by design and is not $100 \%$ production tested.
6. Dropout is defined as either minimum control voltage ( $\mathrm{V}_{\text {CONTROL }}$ ) or minimum power voltage ( $\mathrm{V}_{\text {POWER }}$ ) to output voltage differential required to maintain $1.5 \%$ regulation at a particular load.
7. This parameter is guaranteed by design, but not parametrically tested in production. However, a $100 \%$ thermal shutdown functional test is performed on each part.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| TO-220 | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\text {SENSE }}$ | This Kelvin sense pin allows for remote sensing of the output voltage at the load for improved regulation. It is internally connected to the positive input of the voltage sensing error amplifier. |
| 2 | Adjust | This pin is connected to the low side of the internally trimmed $1.5 \%$ bandgap reference voltage and carries a bias current of about $50 \mu \mathrm{~A}$. A resistor divider from Adjust to $\mathrm{V}_{\text {OUT }}$ and from Adjust to ground sets the output voltage. Also, transient response can be improved by adding a small bypass capacitor from this pin to ground. |
| 3 | $\mathrm{V}_{\text {OUT }}$ | This pin is connected to the emitter of the power pass transistor and provides a regulated voltage capable of sourcing 8.0 A of current. |
| 4 | $\mathrm{V}_{\text {CONTROL }}$ | This is the supply voltage for the regulator control circuitry. For the device to regulate, this voltage should be between 1.0 V and 1.3 V (depending on the output current) greater than the output voltage. The control pin current will be about $1.0 \%$ of the power pin output current. |
| 5 | $V_{\text {POWER }}$ | This is the power input voltage. This pin is physically connected to the collector of the power pass transistor. For the device to regulate, this voltage should be between 0.1 V and 0.7 V greater than the output voltage depending on the output current. The output load current of 8.0 A is supplied through this pin. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Reference Voltage vs Temperature


Figure 5. Adjust Pin Current vs Temperature


Figure 4. Reference Voltage vs Temperature


Figure 6. Ripple Rejection vs Frequency


Figure 7. VPOWER Dropout Voltage vs IOUT


Figure 9. Minimum Load Current vs $\mathrm{V}_{\text {CONTROL }}-\mathrm{V}_{\text {OUT }}$


Figure 11. Short Circuit Current vs $\mathrm{V}_{\text {POWER }}$ - $\mathrm{V}_{\text {OUT }}$


Figure 8. V ${ }_{\text {control }}$ Dropout vs Iout


Figure 10. Current Step Transient Response


Figure 12. Adjust Pin Current vs Output Current



Figure 15. Minimum Load Current vs $\mathrm{V}_{\text {POWER }}-\mathrm{V}_{\text {OUT }}$

## APPLICATIONS NOTES

## THEORY OF OPERATION

The CS5258-1 linear regulator provides adjustable voltages from 1.25 V to 5.0 V at currents up to 8.0 A . The regulator is protected against short circuits, and includes a thermal shutdown circuit with hysteresis. The output, which is current limited, consists of a PNP-NPN transistor pair and requires an output capacitor for stability. A detailed procedure for selecting this capacitor is included in the Stability Considerations section.

## $V_{\text {POWER }}$ Function

The CS5258-1 utilizes a two supply approach to maximize efficiency. The collector of the power device is brought out to the $\mathrm{V}_{\text {POWER }}$ pin to minimize internal power dissipation under high current loads. VCONTROL provides power for the control circuitry and the drive for the output NPN transistor. $\mathrm{V}_{\text {CONTROL }}$ should be at least 1.0 V greater than the output voltage. Special care has been taken to ensure
that there are no supply sequencing problems. The output voltage will not turn on until both supplies are operating. If the control voltage comes up first, the output current will be typically limited to about 3.0 mA until the power input voltage comes up. If the power input voltage comes up first the output will not turn on at all until the control voltage comes up. The output can never come up unregulated.
The CS5258-1 can also be used as a single supply device with the control and power inputs tied together. In this mode, the dropout will be determined by the minimum control voltage.

## Output Voltage Sensing

The CS5258-1 five terminal linear regulator includes a dedicated $\mathrm{V}_{\text {SENSE }}$ function. This allows for true Kelvin sensing of the output voltage. This feature can virtually eliminate errors in the output voltage due to load regulation. Regulation will be optimized at the point where the sense pin is tied to the output.

## DESIGN GUIDELINES

## Adjustable Operation

This LDO adjustable regulator has an output voltage range of 1.25 V to 5.0 V . An external resistor divider sets the output voltage as shown in Figure 16. The regulator's voltage sensing error amplifier maintains a fixed 1.253 V reference between the output pin and the adjust pin.


Figure 16. An External Resistor Divider Sets the Value of $\mathrm{V}_{\text {OUt }}$. The 1.253 V Reference Voltage Drops Across R1.
A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R2 that adds to the 1.253 V across R 1 and sets the overall output voltage. The adjust pin current (typically $50 \mu \mathrm{~A}$ ) also flows through R2 and adds a small error that should be taken into account if precise adjustment of $\mathrm{V}_{\text {OUT }}$ is necessary. The output voltage is set according to the formula:

$$
\mathrm{V}_{\mathrm{OUT}}=1.253 \mathrm{~V} \times \frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 1}+\mathrm{R} 2 \times \mathrm{I}_{\mathrm{ADJ}}
$$

The term $\mathrm{I}_{\mathrm{ADJ}} \times \mathrm{R} 2$ represents the error added by the adjust pin current.

R 1 is chosen so that the minimum load current is a least 10 mA . R1 and R2 should be of the same composition for best tracking over temperature. The divider resistors should be located as close to the load as possible.

While not required, a bypass capacitor connected between the adjust pin and ground will improve transient response and ripple rejection. A $0.1 \mu \mathrm{~F}$ tantalum capacitor is recommended for "first cut" design. Value and type may be varied to optimize performance vs. price.

## Other Adjustable Operation Considerations

The CS5258-1 linear regulator has an absolute maximum specification of 6.0 V for the voltage difference between $\mathrm{V}_{\mathrm{IN}}$ and V Vut. However, the IC may be used to regulate voltages in excess of 6.0 V . The two main considerations in such a design are the sequencing of power supplies and short circuit capability.

Power supply sequencing should be such that the $\mathrm{V}_{\text {CONTROL }}$ supply is brought up coincidentally with or
before the $\mathrm{V}_{\text {POWER }}$ supply. This allows the IC to begin charging the output capacitor as soon as the $\mathrm{V}_{\text {POWER }}$ to $V_{\text {OUT }}$ differential is large enough that the pass transistor conducts. As $V_{\text {POWER }}$ increases, the pass transistor will remain in dropout, and current is passed to the load until $\mathrm{V}_{\text {OUT }}$ is in regulation. Further increase in the supply voltage brings the pass transistor out of dropout. In this manner, any output voltage less than 13 V may be regulated, provided the $\mathrm{V}_{\text {POWER }}$ to $\mathrm{V}_{\text {OUT }}$ differential is less than 6.0 V . In the case where $\mathrm{V}_{\text {CONTROL }}$ and $\mathrm{V}_{\text {POWER }}$ are shorted, there is no theoretical limit to the regulated voltage as long as the $\mathrm{V}_{\text {POWER }}$ to $\mathrm{V}_{\text {OUT }}$ differential of 6.0 V is not exceeded.

There is a possibility of damaging the IC when $V_{\text {POWER }}$ $-\mathrm{V}_{\text {IN }}$ is greater than 6.0 V if a short circuit occurs. Short circuit conditions will result in the immediate operation of the pass transistor outside of its safe operating area. Overvoltage stresses will then cause destruction of the pass transistor before overcurrent or thermal shutdown circuitry can become active. Additional circuitry may be required to clamp the $V_{\text {POWER }}$ to $V_{\text {OUT }}$ differential to less than 6.0 V if fail safe operation is required. One possible clamp circuit is illustrated in Figure 17; however, the design of clamp circuitry must be done on an application by application basis. Care must be taken to ensure the clamp actually protects the design. Components used in the clamp design must be able to withstand the short circuit condition indefinitely while protecting the IC.


Figure 17. Example Clamp Circuitry for $V_{\text {POWER }}-V_{\text {OUT }}>6.0 \mathrm{~V}$

## Stability Considerations

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability.
The capacitor value and type is based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive
solution. However, when the circuit operates at low temperatures, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet provides this information.

A $300 \mu \mathrm{~F}$ tantalum capacitor will work for most applications, but with high current regulators such as the CS5258-1 the transient response and stability improve with higher values of capacitor. The majority of applications for this regulator involve large changes in load current so the output capacitor must supply the instantaneous load current. The ESR of the output capacitor causes an immediate drop in output voltage given by:

$$
\Delta V=\Delta I \times E S R
$$

For microprocessor applications it is customary to use an output capacitor network consisting of several tantalum and ceramic capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close to the load as possible for the best results.

## Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage, and the rate at which $\mathrm{V}_{\text {CONTROL }}$ drops. In the CS5258-1 regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 18 is recommended. Use of the diode has the added benefit of bleeding $\mathrm{V}_{\text {OUT }}$ to ground if $\mathrm{V}_{\text {CONTROL }}$ is shorted. This prevents an unregulated output from causing system damage.


Figure 18. Diode Protection Against $V_{\text {CONTROL }}$ Short Circuit Conditions

A rule of thumb useful in determining if a protection diode is required is to solve for current

$$
\mathrm{I}=\frac{\mathrm{C} \times \mathrm{V}}{\mathrm{~T}}
$$

where:
I is the current flow out of the load capacitance when $\mathrm{V}_{\text {CONTROL }}$ is shorted,
C is the value of load capacitance,
V is the output voltage, and
T is the time duration required for $\mathrm{V}_{\text {CONTROL }}$ to transition from high to being shorted.
If the calculated current is greater than or equal to the typical short circuit current value provided in the specifications, serious thought should be given to the use of a protection diode.

## Current Limit

The internal current limit circuit limits the output current under excessive load conditions.

## Short Circuit Protection

The device includes short circuit protection circuitry that clamps the output current at approximately two amperes less than its current limit value. This provides for a current foldback function, which reduces power dissipation even further under a direct shorted load.

## Thermal Shutdown

The thermal shutdown circuitry is guaranteed by design to activate above a die junction temperature of approximately $150^{\circ} \mathrm{C}$ and to shut down the regulator output. This circuitry has $25^{\circ} \mathrm{C}$ of typical hysteresis, thereby allowing the regulator to recover from a thermal fault automatically.

## Calculating Power Dissipation and Heat Sink Requirements

High power regulators such as the CS5258-1 family usually operate at high junction temperatures. Therefore, it is important to calculate the power dissipation and junction temperatures accurately to ensure that an adequate heat sink is used. Since the package tab is connected to $\mathrm{V}_{\text {OUT }}$ on the CS5258-1, electrical isolation may be required for some applications. Also, as with all high power packages, thermal compound is necessary to ensure proper heat flow. For added safety, this high current LDO includes an internal thermal shutdown circuit.
The thermal characteristics of an IC depend on the following four factors: junction temperature, ambient temperature, die power dissipation, and the thermal resistance from the die junction to ambient air. The maximum junction temperature can be determined by:

$$
\mathrm{T}_{\mathrm{J}(\max )}=\mathrm{T}_{\mathrm{A}(\max )}+\mathrm{PD}_{(\max )} \times \mathrm{R}_{\Theta \mathrm{JA}}
$$

The maximum ambient temperature and the power dissipation are determined by the design while the maximum junction temperature and the thermal resistance depend on the manufacturer and the package type. The maximum power dissipation for a regulator is:

$$
\begin{aligned}
\mathrm{PD}_{(\max )}= & \left(\mathrm{VIN}_{\mathrm{IN}}^{\max )}-\mathrm{VOUT}(\min )\right) \mathrm{IOUT}(\max ) \\
& +\mathrm{VIN}(\max ) \times \operatorname{IIN}(\max )
\end{aligned}
$$

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment has a thermal resistance which is measured in degrees per watt. Like series electrical resistances, these thermal resistances are summed to determine the total thermal resistance between the die junction and the surrounding air, $\mathrm{R}_{\Theta \mathrm{JA}}$. This total thermal resistance is comprised of three components. These resistive terms are measured from junction to case ( $\mathrm{R}_{\Theta \mathrm{JC}}$ ), case to heat sink $\left.\mathrm{R}_{\Theta C S}\right)$, and heat sink to ambient air $\left(\mathrm{R}_{\Theta S A}\right)$. The equation is:

$$
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A}
$$

The value for $\mathrm{R}_{\Theta \mathrm{JC}}$ is $1.4^{\circ} \mathrm{C}$ watt for the CS5258-1 in the TO-220 package. For a high current regulator such as the CS5258-1 the majority of heat is generated in the power transistor section. The value for $\mathrm{R}_{\Theta S A}$ depends on the heat sink type, while the $R_{\Theta C S}$ depends on factors such as package type, heat sink interface (is an insulator and thermal grease used?), and the contact area between the heat sink and the package. Once these calculations are complete, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated and the proper heat sink selected. For further discussion on heat sink selection, see our application note "Thermal Management for Linear Regulators," document number SR006AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## PACKAGE THERMAL DATA

| Parameter |  | TO-220 Five Lead | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 1.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

300 mA Very Low Noise, Low
Dropout Linear Regulator
The NCP2860 is a low noise, low dropout linear regulator that has been designed to supply $2.77 \mathrm{~V} / 300 \mathrm{~mA}$ from 3.0 V to 6.0 V input. If wished, the "SET" pin enables to adjust the output voltage level that then depends on the voltage applied to this pin. The excellent performances the NCP2860 features in terms of transient responses, PSRR and noise, make it an ideal solution for audio applications (e.g. audio amplifier drivers).

## Features

- High Output Current (300 mA Max)
- Low Output Voltage Noise: $60 \mu \mathrm{Vrms}$
- Low Dropout ( $150 \mathrm{mV} @ \mathrm{I}_{\text {out }}=300 \mathrm{~mA}$ )
- Thermal Overload and Short Circuit Protections
- Very Low Consumption in Shutdown Mode (10 nA)
- High Power Supply Rejection Ratio ( 60 dB @ 1.0 kHz )
- $\overline{\text { FAULT Indicator }}$
- Programmable Output Voltage
- Soft Start


## Typical Applications

- Cellular Phone
- Handheld Instruments




## ON Semiconductor ${ }^{\text {w }}$

## http://onsemi.com

MARKING DIAGRAM


A = Assembly Location
$\mathrm{Y}=$ Year
W = Work Week

## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP2860DM277R2 | Micro8 | 4000 Units/Reel |

PIN DESCRIPTION

| Pin | Name | Description |
| :---: | :---: | :--- |
| 1,4 | OUT | "OUT" is the regulator output. A low ESR, bypass capacitor should be connected for stable operation. |
| 2 | IN | "IN" is the supply input that is connected to the power source (up to 6.0 V ). Bypass with a $2.2 \mu \mathrm{~F}$ capacitor. |
| 3 | GND | Ground |
| 5 | SET | Ground the "SET" pin to set the output voltage to 2.77 V. Refer to the "output voltage setting" paragraph if <br> you need to program another value. |
| 6 | N.C. | This pin is non-connected. |
| 7 | STDWN | If the "STDWN" pin is low, the circuit enters the shutdown mode. |
| 8 | FAULT | The "FAULT" terminal is a high impedance, open drain output. If the circuit is out of regulation, the voltage <br> pin goes low. Otherwise (normal operation or shutdown mode), this pin is high impedance. Connect the pin <br> to ground, if unused. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage, Shutdown Pin, Voltage Range (Note 1) | $\mathrm{V}_{\text {inmax }}$ | -0.3, +6.0 | V |
| Thermal Resistance (Note 2) | - | 230 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Maximum Junction Temperature | $\mathrm{T}_{\text {Jmax }}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {Smax }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10s) | $\mathrm{T}_{\text {max }}$ | 300 | ${ }^{\circ} \mathrm{C}$ |
| ESD Capability Human Body Model Machine Model | - | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{gathered} \text { kV } \\ \text { V } \end{gathered}$ |
| Latch-up Capability @ $85^{\circ} \mathrm{C}$ | - | +/-100 | mA |

1. The recommended input voltage range for NCP2860 proper operation is 2.7 V to 6.0 V .
2. Circuit being mounted on a board that has no metal oxide traces attached to the leads. The addition of plated copper can lower the thermal resistance.

TYPICAL ELECTRICAL CHARACTERISTICS ${ }^{*}\left(V_{i n}=3.6 \mathrm{~V}, \mathrm{SET}=\mathrm{GND}, \mathrm{T}_{\mathrm{A}}\right.$ from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage @ $\mathrm{I}_{\text {out }}=100 \mu \mathrm{~A}, 300 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=3.2 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ $\mathrm{T}_{\mathrm{A}}$ from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $V_{\text {out }}$ | $\begin{aligned} & \hline 2.73 \\ & 2.70 \end{aligned}$ | $\begin{aligned} & \hline 2.77 \\ & 2.77 \end{aligned}$ | $\begin{aligned} & \hline 2.81 \\ & 2.84 \end{aligned}$ | V |
| Supply Current @ $\mathrm{I}_{\text {out }}=0, \mathrm{~V}_{\text {in }}=3.2 \mathrm{~V}$ | $\mathrm{I}_{\mathrm{cc}-0}$ | - | 355 | 700 | $\mu \mathrm{A}$ |
| Supply Current @ $\mathrm{I}_{\text {out }}=300 \mathrm{~mA}, \mathrm{~V}_{\text {in }}=3.2 \mathrm{~V}$ | $\mathrm{I}_{\text {cc-300 }}$ | - | 1.1 | - | mA |
| Supply Current in Shutdown Mode (STDWN Pin Grounded) <br> @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $1_{\text {stdwn }}$ | - | 0.01 | 1.0 | $\mu \mathrm{A}$ |
| Dropout Voltage @ $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ (Note 3) | $\mathrm{V}_{\text {drop-1 }}$ | - | 0.6 | - | mV |
| Dropout Voltage @ Iout $=150 \mathrm{~mA}$ (Note 3) | $V_{\text {drop-150 }}$ | - | 75 | 150 | mV |
| Dropout Voltage @ Iout $=300 \mathrm{~mA}$ (Note 3) | $\mathrm{V}_{\text {drop-300 }}$ | - | 150 | - | mV |
| SET Threshold (SET = OUT) @ $\mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ and $\mathrm{V}_{\text {in }}=3.6 \mathrm{~V}$ or $6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ $\mathrm{T}_{\mathrm{A}}$ from $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & \hline 1.226 \\ & 1.220 \end{aligned}$ | $\begin{aligned} & \hline 1.244 \\ & 1.244 \end{aligned}$ | $\begin{aligned} & 1.262 \\ & 1.270 \end{aligned}$ | V |
| SET Input Leakage Current @ $\mathrm{V}_{\text {SET }}=1.25 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $l_{\text {leak }}$ | - | 10 | 200 | nA |
| Short Circuit Output Current Limitation @ $\mathrm{V}_{\text {in }}=3.2 \mathrm{~V}$ and $\mathrm{V}_{\text {out }}=2.2 \mathrm{~V}$ | $I_{\text {max_c }}$ | 310 | 465 | 700 | mA |
| Start-Up Current Limitation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\text {in }}=3.2 \mathrm{~V}$ and $\mathrm{V}_{\text {out }}=2.2 \mathrm{~V}$ | Imax_stup | - | 220 | - | mA |
| Line Regulation, $\mathrm{V}_{\text {in }}$ varying between 3.0 V and $6.0 \mathrm{~V} @ \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ | Line $_{\text {Reg1 }}$ | -0.1 | 0.01 | 0.1 | \%/V |
| Line Regulation, $\mathrm{V}_{\text {in }}$ varying between 3.0 V and $6.0 \mathrm{~V} @ \mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ | Line $_{\text {Reg2 }}$ | -0.1 | 0.01 | 0.1 | \%/V |
| Line Regulation, $\mathrm{V}_{\text {in }}$ varying between 3.0 V and $6.0 \mathrm{~V} @ \mathrm{I}_{\text {out }}=1.0 \mathrm{~mA}$ and (SET = OUT) | Line $_{\text {Reg3 }}$ | -0.1 | 0.03 | 0.1 | \%/V |
| Line Regulation, $\mathrm{V}_{\text {in }}$ varying between 3.0 V and $6.0 \mathrm{~V} @ \mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ and (SET = OUT) | Line $_{\text {Reg } 4}$ | -0.1 | 0.03 | 0.1 | \%/V |
| Load Regulation, $\mathrm{I}_{\text {out }}$ varying from 0.1 mA to $300 \mathrm{~mA}, \mathrm{SET}=\mathrm{OUT}$, @ $\mathrm{V}_{\text {in }}=3.2 \mathrm{~V}$ | LoadReg1 $^{\text {R }}$ | - | 0.0002 | - | \%/mA |
| Load Regulation, I ${ }_{\text {out }}$ varying from 0.1 mA to $300 \mathrm{~mA}, \mathrm{SET}$ Grounded, @ $\mathrm{V}_{\text {in }}=3.2 \mathrm{~V}$ | Load $_{\text {Reg2 }}$ | - | 0.001 | - | \%/mA |
| $\begin{aligned} & \text { Output Voltage Noise @ SET = OUT, C } \text { out }=22 \mu \mathrm{~F} \text { (Note 4) } \\ & 10 \mathrm{~Hz}<\mathrm{f}<10 \mathrm{kHz} \\ & 10 \mathrm{~Hz}<\mathrm{f}<100 \mathrm{kHz} \end{aligned}$ | - | - | $\begin{aligned} & 15 \\ & 35 \end{aligned}$ | - | $\mu \mathrm{V}_{\text {rms }}$ |
| $\begin{aligned} & \text { Output Voltage Noise @ SET = GND, C }{ }_{\text {out }}=22 \mu \mathrm{~F} \text { (Note 4) } \\ & 10 \mathrm{~Hz}<\mathrm{f}<10 \mathrm{kHz} \\ & 10 \mathrm{~Hz}<\mathrm{f}<100 \mathrm{kHz} \end{aligned}$ | - | - | $\begin{aligned} & 35 \\ & 60 \end{aligned}$ | - | $\mu \mathrm{V}_{\text {rms }}$ |
| Output Voltage Noise Density @ SET = GND, C out $=22 \mu \mathrm{~F}, 10 \mathrm{~Hz}<\mathrm{f}<100 \mathrm{kHz}$ (Note 4) | - | - | 400 | - | $\mathrm{nV}(\mathrm{Hz})^{-1 / 2}$ |
| Power Supply Rejection Ratio @ 1.0 kHz and $\mathrm{l}_{\text {out }}=100 \mathrm{~mA}$ | PSRR | - | 60 | - | dB |
| Shutdown Threshold (with hysteresis) @ $\mathrm{V}_{\text {in }}=3.2 \mathrm{~V}$ | $\mathrm{V}_{\text {stdwn }}$ | 0.4 | - | 2.0 | V |
| Shutdown Pin Bias Current @ STDWN = IN or GND and T ${ }_{\text {A }}=25^{\circ} \mathrm{C}$ | $\mathrm{I}_{\text {stdwn }}$ | - | - | 100 | nA |
| FAULT Detection Voltage @ Iout $=200 \mathrm{~mA}$ | $\mathrm{V}_{\text {fault-th }}$ | - | 120 | 280 | mV |
| FAULT Output Low Voltage @ $\mathrm{I}_{\text {sink }}=2.0 \mathrm{~mA}$ | $V_{\text {fault-out }}$ | - | 0.15 | 0.4 | V |
| FAULT Output OFF Leakage Current @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\mathrm{I}_{\text {fault }}$ | - | 0.1 | 100 | nA |
| Start-Up Time @ C ${ }_{\text {out }}=10 \mu \mathrm{~F}, \mathrm{~V}_{\text {out }}=2.7 \mathrm{~V}$ (Note 4) | $\mathrm{T}_{\text {stup }}$ | - | 135 | - | $\mu \mathrm{s}$ |
| Thermal Shutdown Threshold | $\mathrm{T}_{\text {limit }}$ | - | 170 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | $\mathrm{H}_{\text {temp }}$ | - | 30 | - | ${ }^{\circ} \mathrm{C}$ |

*The specification gives the targeted values. This specification may have to be slightly adjusted after the temperature characterization of the die.
3. The dropout voltage is defined as $\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right)$ when $\mathrm{V}_{\text {out }}$ is 100 mV below the value of $\mathrm{V}_{\text {out }}$ when $\mathrm{V}_{\text {in }}=3.1 \mathrm{~V}$.
4. Refer to characterization curves for more details.

TYPICAL ELECTRICAL CHARACTERISTICS
$\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+0.5 \mathrm{~V}, \mathrm{C}_{\text {in }}=\mathrm{C}_{\text {out }}=2.2 \mu \mathrm{~F}, \mathrm{SET}=\mathrm{GND}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted. $)$


Figure 1. Normalized Output Voltage vs. Load Current


Figure 3. Supply Current vs. Load Current


Figure 5. Dropout Voltage vs. Load Current


Figure 2. Normalized Output Voltage vs. Temperature


Figure 4. No Load Supply Current vs. Input Voltage


Figure 6. Fault Detect Threshold vs. Load Current

TYPICAL ELECTRICAL CHARACTERISTICS
$\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+0.5 \mathrm{~V}, \mathrm{C}_{\text {in }}=\mathrm{C}_{\text {out }}=2.2 \mu \mathrm{~F}, \mathrm{SET}=\mathrm{GND}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted. $)$


Figure 7. Power Supply Rejection Ratio


Figure 8. Output Noise Spectral Density


Figure 9. Load Transient Response
Figure 10. Line Transient

TYPICAL ELECTRICAL CHARACTERISTICS
$\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+0.5 \mathrm{~V}, \mathrm{C}_{\text {in }}=\mathrm{C}_{\text {out }}=2.2 \mu \mathrm{~F}, \mathrm{SET}=\mathrm{GND}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted. $)$


Figure 11. Power-Down Response ( $I_{\text {load }}=100 \mathrm{~mA}$ )


Figure 13. Shutdown/Power-Up $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+0.5 \mathrm{~V}\right.$, $\left.I_{\text {load }}=50 \mathrm{~mA}\right)$


Figure 12. Power-Up Response ( $l_{\text {load }}=100 \mathrm{~mA}$ )


Figure 14. Shutdown/Power-Up $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+0.5 \mathrm{~V}\right.$, $I_{\text {load }}=0 \mathrm{~mA}$ )

## DETAILED OPERATING DESCRIPTION

## Internal Pass Transistor

The NCP2860 incorporates a $0.5 \Omega$ typical P-channel MOSFET pass transistor. The P -channel MOSFET requires no drive current and then compared to the PNP based regulators, this solution drastically reduces the quiescent current and associated losses.

## Shutdown Block

The circuit turns into shutdown mode when the shutdown pin is in low state. In this mode, the internal biasing current sources are disconnected so that the pass transistor is off and the consumption reduced to a minimum value. Practically, the shutdown consumption is in the range of 10 nA . When this function is unused, "IN" is generally applied to the shutdown pin.

## Current Limitation

The NCP2860 incorporates a short circuit protection that prevents the pass transistor current from exceeding 465 mA typically. The current limit is set to 220 mA during the start-up phase.

## Thermal Protection

The thermal protection protects the die against excessive overheating. Practically, when the junction temperature exceeds $170^{\circ} \mathrm{C}$, an internal thermal sensor sends a logical signal to the shutdown block so that the circuit enters the shutdown mode. Once the die has cooled enough (typically $30^{\circ} \mathrm{C}$ ), the circuit enters a new working phase.

## Output Voltage Setting

The output voltage is set to 2.77 V if the "SET" pin is grounded. It can also be programmed to a different value. To do so, a portion of the output voltage must be applied to the "SET" pin. If a (R1, R2) resistors divider is used, then:

$$
\mathrm{V}_{\text {out }}=(1+\mathrm{R} 1 / \mathrm{R} 2) * \mathrm{~V}_{\text {ref }}
$$

Therefore, as $\mathrm{V}_{\text {ref }}$ typically equals 1.244 V :

$$
\mathrm{V}_{\text {out }}=1.244 *(1+\mathrm{R} 1 / \mathrm{R} 2)
$$

Now if R1 and R2 are high impedance resistors, the leakage current that is absorbed by the "SET" pin, may have to be taken into account as follows:

$$
\mathrm{V}_{\text {out }}=[1.244 *(1+\mathrm{R} 1 / \mathrm{R} 2)]+\left(\mathrm{R} 1 * \mathrm{I}_{\mathrm{lk}}\right) \text { where } \mathrm{I}_{\mathrm{lk}} \text { is the }
$$ "SET" pin leakage current.

If the output voltage is directly applied to the "SET" pin, $\mathrm{V}_{\text {out }}=\mathrm{V}_{\text {ref }}=1.244 \mathrm{~V}$.


## Regulation

The circuit incorporates a transconductance error amplifier. The error amplifier output varies in response to load and input voltage variations to control the pass transistor current so that the "OUT" pin delivers the wished voltage. No compensation capacitor is required.

## Fault Detection Circuitry

The circuit detects when the input-output differential voltage is too low to ensure a correct load and line regulation at the output. The input-output differential threshold scales proportionally with the load current to be always just higher than the dropout.
When the circuit detects a fault condition, an internal switch connects "FAULT" to ground. In normal operation, the "FAULT" terminal is an open-drain-N-channel MOSFET and if a pull-up resistor is connected between "OUT" and "FAULT", "FAULT" goes high. The pull-up resistor is generally selected in the range of $100 \mathrm{k} \Omega$ to minimize the current consumption.

## Application Information

It is recommended to use $2.2 \mu \mathrm{~F}$ capacitors on the input and on the output of the NCP2860. Capacitor type is not very critical. Simply the ESR should be lower than $0.5 \Omega$ to ensure a stable operation over the temperature and output current ranges. It could be convenient to increase the capacitor size and its quality (lower ESR) only if it was necessary to further improve the noise performances, the Power Supply Rejection Ratio or the fast transient response.


Figure 15. With External Output Voltage Adjustment


Figure 16. Application for 2.77 V Output Voltage

# Very Low Dropout/ Ultra Low Noise 5 Outputs Voltage Regulator 

The MC33765 is an ultra low noise, very low dropout voltage regulator with five independent outputs which is available in TSSOP 16 surface mount package.

The MC33765 is available in 2.8 V . The output voltage is the same for all five outputs but each output is capable of supplying different currents up to 150 mA for output 4 . The device features a very low dropout voltage ( 0.11 V typical for maximum output current), very low quiescent current ( $5.0 \mu \mathrm{~A}$ maximum in OFF mode, $130 \mu \mathrm{~A}$ typical in ON mode) and one of the output (output 3) exhibits a very low noise level which allows the driving of noise sensitive circuitry. Internal current and thermal limiting protections are provided.

Additionally, the MC33765 has an independent Enable input pin for each output. It includes also a common Enable pin to shutdown the complete circuit when not used. The Common Enable pin has the highest priority over the five independent Enable input pins.

The voltage regulators VR1, VR2 and VR3 have a common input voltage pin $\mathrm{V}_{\mathrm{CC}} 1$.

The other voltage regulators VR4 and VR5 have a common input voltage pin $\mathrm{V}_{\mathrm{CC}} 2$.

- Five Independent Outputs at 2.8 V Typical, based upon voltage version
- Internal Trimmed Voltage Reference
- $\mathrm{V}_{\text {out }}$ Tolerance $\pm 3.0 \%$ over the Temperature Range $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
- Enable Input Pin (Logic-Controlled Shutdown) for Each of the Five Outputs
- Common Enable Pin to Shutdown the Whole Circuit
- Very Low Dropout Voltage (0.11 V Typical for Output 1, 2, 3 and 5; 0.17 V Typical for Output 4 at Maximum Current)
- Very Low Quiescent Current (Maximum $5.0 \mu \mathrm{~A}$ in OFF Mode, $130 \mu \mathrm{~A}$ Typical in ON Mode)
- Ultra Low Noise for VR3 ( $30 \mu \mathrm{~V}$ RMS Max, $100 \mathrm{~Hz}<\mathrm{f}<100 \mathrm{kHz}$ )
- Internal Current and Thermal Limit
- 100 nF for VR1, VR2, VR4 and VR5 and $1.0 \mu \mathrm{~F}$ for VR3 for Stability
- Supply Voltage Rejection: 60 dB (Typical) @ f $=1.0 \mathrm{kHz}$


## ON Semiconductor

http://onsemi.com
MARKING
DIAGRAMS

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33765DTB | TSSOP16 | 96 Units/Rail |
| MC33765DTBR2 | TSSOP16 | 2500 Units/Reel |

Simplified Block Diagram


## MAXIMUM RATINGS

| Rating | Symbol | Pin \# | Value | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ |  | 5.3 | V |
| Thermal Resistance Junction-to-Air | $\mathrm{R}_{\text {өJA }}$ |  | 140 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ |  | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ |  | 125 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $\mathrm{T}_{\operatorname{Jmax}}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |

## CONTROL ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C} / \mathrm{Max}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ )

| Characteristics | Symbol | Pin \# | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Independent Enable Pins |  |  |  |  |  |  |
| Input Voltage Range | $\mathrm{V}_{\text {ON/OFF(1-5) }}$ |  | 0 | - | $\mathrm{V}_{\mathrm{CC}}$ | V |
| Control Input Impedance |  |  | 100 | - | - | k $\Omega$ |
| Logic "0", i.e. OFF State Logic "1", i.e. ON State | $\mathrm{V}_{\text {ON/OFF }}(1-5)$ |  | $\stackrel{-}{2.0}$ | - | $0.5$ | V |

## Common Enable Pin

| Input Voltage Range | $\mathrm{V}_{\mathrm{CE}}$ | 2 | 0 | - | $\mathrm{V}_{\mathrm{CC}}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Control Input Impedance |  | 2 | 100 | - | - | $\mathrm{k} \Omega$ |
| Logic "0", i.e. OFF State | $\mathrm{V}_{\mathrm{CE}}$ | 2 | - | - | 0.3 | V |
| Logic "1", i.e. ON State |  |  | 2.0 | - | - |  |

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C} / \mathrm{Max}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ )

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |

## CURRENT CONSUMPTION with NO LOAD

| Current Consumption at Logic " 0 " for the complete device, i.e. Common Enable and All Independent Enable pins at OFF State | $\mathrm{IQ}_{\text {OFF }}$ | - | - | 5.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Consumption at Logic " 1 " for the complete device, i.e. Common Enable and All Independents Enable pins at ON State | $\mathrm{IQ}_{\mathrm{ON} 1}$ | - | 470 | - | $\mu \mathrm{A}$ |
| Current Consumption at Logic "1", Common Enable at ON State and All Independents Enable pins at OFF State | IQON2 | - | 130 | - | $\mu \mathrm{A}$ |

## REGULATOR ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C} / \mathrm{Max}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ )

| Characteristics | Symbol | Pin \# | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply and Output Voltages, Dropout and Load Regulation |  |  |  |  |  |  |
| Supply Voltage $\mathrm{V}_{\text {CC }} \quad$ MC33765 (2.8V) | $\mathrm{V}_{\mathrm{CC} 1}, \mathrm{~V}_{\mathrm{CC} 2}$ | 15, 10 | 3.0 | 3.6 | 5.3 | V |
| Regulator Output Voltage for VR1, VR2, VR3, VR4 and VR5 MC33765 (2.8V) | $\mathrm{V}_{\text {OUT(1-5) }}$ | $\begin{gathered} 14,13,12, \\ 11,9 \end{gathered}$ | 2.7 | 2.8 | 2.85 | V |
| Dropout Voltage for VR1, VR2, VR3, VR5 (Note 1) | $\mathrm{V}_{\text {CC }}-\mathrm{V}_{\text {OUT }}$ | $\begin{gathered} 14,13, \\ 12,9 \end{gathered}$ | - | 0.11 | 0.17 | V |
| Dropout Voltage for VR4 (Note 1) | $\mathrm{V}_{\text {CC }}-\mathrm{V}_{\text {OUT4 }}$ | 11 | - | 0.17 | 0.30 | V |
| Load Regulation ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{Reg}_{\text {load(1-5) }}$ | $\begin{gathered} 9,11,12, \\ 13,14 \end{gathered}$ | - | - | 0.5 | $\begin{aligned} & \mathrm{mV} / \\ & \mathrm{mA} \end{aligned}$ |

Max Power Dissipation and Total DC Output Current (VR1 + VR2 + VR3 + VR4 + VR5) (Note 2)

| Max Power Dissipation at $\mathrm{V}_{\mathrm{CC}}=5.3 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C}\right)$ | $\mathrm{P}_{\mathrm{dmax}}$ |  | - | - | 285 | mW |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Max. Total RMS Output Current at $\mathrm{V}_{\mathrm{CC}}=5.3 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{RMS}}$ |  | - | - | 130 | mA |
| Max Power Dissipation at $\mathrm{V}_{\mathrm{CC}}=5.3 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{P}_{\mathrm{dmax}}$ |  | - | - | 700 | mW |
| Max. Total RMS Output Current at $\mathrm{V}_{\mathrm{CC}}=5.3 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{RMS}}$ |  | - | - | 250 | mA |

## Output Currents (Note 3)

| Regulator VR1 Output Current | Iout1 | 14 | 10 | - | 30 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Regulator VR2 Output Current | IOUT2 | 13 | 10 | - | 40 | mA |
| Regulator VR3 Output Current | IOUT3 | 12 | 0 | - | 50 | mA |
| Regulator VR4 Output Current | IOUT4 | 11 | 10 | - | 150 | mA |
| Regulator VR5 Output Current | Iout5 | 9 | 10 | - | 60 | mA |
| Current Limit for VR1, VR2, VR3, VR4, VR5 [Twice the max Output Current for each output] | $\mathrm{I}_{\text {MAX }}$ | $\begin{gathered} 14,13,12, \\ 11,9 \end{gathered}$ | - | $\begin{gathered} \hline 2 \times \text { lout } \\ (1-5) \end{gathered}$ | - | mA |

## External Capacitors

| External Compensation Capacitors for VR1, VR2, VR4, VR5 | $\mathrm{C}_{(1-2,4-5)}$ | $14,13,11,9$ | 0.10 | - | 1.0 | $\mu \mathrm{~F}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| External Compensation Capacitors for VR3 | $\mathrm{C}_{4}$ | 12 | 1.0 | - | - | $\mu \mathrm{F}$ |
| External Compensation Capacitors ESR |  |  | 0.05 | 1.0 | 3.0 | $\Omega$ |

## Ripple Rejections

| Ripple Rejection VR1, VR2, VR4, VR5 <br> (at Max. Current, $1.0 \mathrm{kHz}, \mathrm{C}=100 \mathrm{nF}$ ) | $\frac{\left(\Delta \mathrm{V}_{\mathrm{OUT}}\right)}{\left(\Delta \mathrm{V}_{\mathrm{CC}}\right)}$ | 14,13, <br> 11,9 | 50 | 60 | - | dB |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Ripple Rejection VR1, VR2, VR4, VR5 <br> (at Max. Current, $\mathrm{f}=10 \mathrm{kHz}, \mathrm{C}=100 \mathrm{nF})$ | $\frac{\left(\Delta \mathrm{V}_{\mathrm{OUT}}\right)}{\left(\Delta \mathrm{V}_{\mathrm{CC}}\right)}$ | 14,13, <br> 11,9 | 40 | 45 | - | dB |
| Ripple Rejection of VR3 <br> (at Max. Current, $\mathrm{f}=1.0 \mathrm{kHz}, \mathrm{C}=1.0 \mu \mathrm{~F})$ | $\frac{\left(\Delta \mathrm{V}_{\mathrm{OUT}}\right)}{\left(\Delta \mathrm{V}_{\mathrm{CC}}\right)}$ | 12 | 50 | 60 | - | dB |
| Ripple Rejection of VR3 <br> (at Max. Current, $\mathrm{f}=10 \mathrm{kHz}, \mathrm{C}=1.0 \mu \mathrm{~F})$ | $\frac{\left(\Delta \mathrm{V}_{\mathrm{OUT}}\right)}{\left(\Delta \mathrm{V}_{\mathrm{CC}}\right)}$ | 12 | 40 | 45 | - | dB |
| Ripple Rejection of VR3 <br> (at Max. Current, $\mathrm{f}=100 \mathrm{kHz}, \mathrm{C}=1.0 \mu \mathrm{~F})$ | $\frac{\left(\Delta \mathrm{V}_{\mathrm{OUT}}\right)}{\left(\Delta \mathrm{V}_{\mathrm{CC}}\right)}$ | 12 | 18 | 22 | - | dB |

1. Typical dropout voltages have been measured at currents: Output1: 25 mA , Output2: 35 mA , Output3: 40 mA , Output4: 140 mA , Output5: 40 mA Maximum value of dropout voltages are measured at maximum specified current
2. See package power dissipation and thermal protection.
3. Maximum Output Currents are peak values. Total DC current have to be set upon maximum power dissipation specification. Only Output 3 has been designed to be stable at minimum current of 0 mA .

## REGULATOR ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C} / \mathrm{Max} \mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ )

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dynamic Parameters |  |  |  |  |  |
| Rise Time ( $1 \% \rightarrow 99 \%$ ) Common Enable at ON state, $\mathrm{C}_{\text {bypass }}=10 \mathrm{nF}$, $\mathrm{I}_{\text {out }}$ at max. current <br> VR1, VR2, VR4, VR5 with Cout $=100 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ VR3 with $\mathrm{C}_{\text {OUT }}=1.0 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\mathrm{t}_{\text {on }}$ | - |  | $\begin{gathered} 30 \\ 150 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{s} \\ & \mu \mathrm{~s} \end{aligned}$ |
| Fall Time ( $99 \% \rightarrow 1 \%$ ) [COUT $=100 \mathrm{nF}$, I IOUT $=30 \mathrm{~mA}$ ] (Note 4) | $\mathrm{t}_{\text {off }}$ | - | 100 | - | $\mu \mathrm{s}$ |
| Overshoot (Cout $=100 \mathrm{nF}$ for VR1, VR2, VR4, VR5 and $\mathrm{C}_{\text {OUT }}=1.0 \mu \mathrm{~F}$ for VR3) at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Common Enable at ON state, independent enable from OFF to ON state |  | - | 5 | 8 | \% |
| Settling Time (to $\pm 0.1 \%$ of nominal) at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Common Enable at ON state, independent enable from OFF to ON state |  | - | 95 | - | $\mu \mathrm{s}$ |

## Noise and Crosstalks

| Noise Voltage ( $100 \mathrm{~Hz}<\mathrm{f}<100 \mathrm{kHz}$ ) with $\mathrm{C}_{\text {bypass }}=100 \mathrm{nF}$ VR1, VR2, VR4, VR5 with Cout $=100 \mathrm{nF}$ VR3 with Cout $=1.0 \mu \mathrm{~F}$ | - | $\begin{aligned} & 40 \\ & 25 \end{aligned}$ | $30$ | $\mu \mathrm{V}$ RMS |
| :---: | :---: | :---: | :---: | :---: |
| Static crosstalk (DC shift) between the Regulator Output, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ (Note 5) | - | 150 | 200 | $\mu \mathrm{V}$ |
| Dynamic CrossTalk Attenuation between the Regulator Outputs $(\mathrm{f}=10 \mathrm{kHz}), \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}(\text { Note } 6)$ | 30 | 35 | - | dB |

## Thermal Shutdown

| Thermal Shutdown | - | 160 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | :--- | :--- |

4. The Fall time is highly dependent on the load conditions, i.e. load current for a specified value of $\mathrm{C}_{\text {out }}$.
5. Static Crosstalk is a DC shift caused by switching ON one of the outputs through independent enable to all other outputs. This parameter is highly dependent on overall PCB layout and requires the implementation of low-noise GROUND rules (e.g. Ground plane).
6. Dynamic crosstalk is the ratio between a forced output signal to signal transferred to other outputs. This requires special device configuration to be measured.

## MC33765

MC33765 TYPICAL OSCILLOSCOPE SHOTS


Figure 1. Crosstalk response of MC33765 showing extremely weak interaction between outputs Output 4 is banged from 0 to 150 mA


Figure 3. Single Common Enable response time (Cbypass discharged)


Figure 2. Repetitive Common Enable response time


Figure 4. Output response from seperate Enable

## MC33765



Figure 5. Output 4 is banged from 3 mA to 150 mA


Figure 6. Output 5 is banged from 3 mA to 50 mA


Figure 7. Typical input voltage rejection (Cout $=100 \mathrm{nF}$ )


Figure 8. Typical input voltage rejection (Cout $=1 \mu \mathrm{~F}$ )


Figure 9. Dropout Voltage versus Output Current


Figure 11. Maximum Output Current versus Temperature


Figure 10. Ground Current versus Individual Output


Figure 12. Dropout Voltage versus Operating Temperature: OUT1


Figure 13. Dropout Voltage versus Operating Temperature: OUT2


Figure 14. Dropout Voltage versus Operating Temperature: OUT3

## MC33765



Figure 15. Dropout Voltage versus Operating Temperature: OUT4


Figure 16. Dropout Voltage versus Operating Temperature: OUT5

## DEFINITIONS

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage - The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential input/output), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage - The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.


Maximum Power Dissipation - The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current - Current which is used to operate the regulator chip with no load current.

Line Regulation - The change in input voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Thermal Protection - Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically $160^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

Maximum Package Power Dissipation and RMS Current - The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. $125^{\circ} \mathrm{C}$. The junction temperature is rising while the difference between the input power ( $\mathrm{V}_{\mathrm{CC}} \mathrm{X}_{\mathrm{CC}}$ ) and the output power ( $\mathrm{V}_{\text {out }} \mathrm{X} \mathrm{I}_{\text {out }}$ ) is increasing.

As MC33765 device exhibits five independent outputs $\mathrm{I}_{\text {out }}$ is specified as the maximum RMS current combination of the five output currents.

As the device can be switched ON/OFF through independent Enable (ON/OFF pin) or Common Enable, the output signal could be, for example, a square wave. Let's assume that the device is ON during $\mathrm{T}_{\mathrm{ON}}$ on a signal period T. The RMS current will be given by:

$$
{ }^{{ }^{\text {utt }_{\text {RMS }}}}=I_{\mathrm{P}} \times \sqrt{\mathrm{D}}
$$

where $\quad \mathrm{D}=\frac{\mathrm{T}^{\mathrm{O}} \mathrm{ON}}{\mathrm{T}}$


Depending on ambient temperature, it is possible to calculate the maximum power dissipation and so the maximum RMS current as following:

$$
P d=\frac{T_{J}-T_{A}}{R_{\theta J A}}
$$

The maximum operating junction temperature $\mathrm{T}_{\mathrm{J}}$ is specified at $125^{\circ} \mathrm{C}$, if $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, then $\mathrm{P}_{\mathrm{D}}=700 \mathrm{~mW}$. By neglecting the quiescent current, the maximum power dissipation can be expressed as:

$$
I_{\text {out }}=\frac{P_{D}}{V_{C C}-V_{\text {out }}}
$$

So that in the more drastic conditions:
$\mathrm{V}_{\mathrm{CC}}=5.3 \mathrm{~V}, \mathrm{~V}_{\text {out }}=2.7 \mathrm{~V}$ then the maximum RMS value of $\mathrm{I}_{\text {out }}$ is 269 mA .

The maximum power dissipation supported by the device is a lot increased when using appropriate application design. Mounting pad configuration on the PCB, the board material and also the ambient temperature are affected the rate of temperature rise. It means that when the $\mathrm{I}_{\mathrm{C}}$ has good thermal conductivity through PCB, the junction temperature will be "low" even if the power dissipation is great.

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature $\left(160^{\circ} \mathrm{C}\right.$ for MC 33765$)$ and ambient temperature.

$$
R_{\theta J A}=\frac{T_{J}-T_{A}}{P_{D}}
$$

## MC33765

## DESIGN HINTS

## Reducing the cross-talk between the MC33765 outputs

One of the origin of the DC shift finds its seat in the layout surrounding the integrated circuit. Particular care has to be taken when routing the output ground paths. Star grounding

or a ground plane are the absolute conditions to reduce the noise or shift associated to common impedance situations, as depicted by Figure 17.


Figure 17. Star Cabling Avoids Coupling by Common Ground Impedance

The first left cabling will generate a voltage shift which will superimpose on the output voltages, thus creating an undesirable offset. By routing the return grounds to a single
low impedance point, you naturally shield the circuit against common impedance disturbances. Figure 18 portraits the text fixture implemented to test the response of the MC33765.


Figure 18. DC Shift Text Fixture

## DESIGN HINTS (cont.)

Output 4 was banged from 0 to 150 mA via its dedicated control pin, while output 3 fixed at 50 mA was monitored. The circuit has been implemented on a PCB equipped with a
ground plane and routed with short copper traces. The results are shown hereafter, revealing the excellent behavior of the MC33765 when crosstalks outputs is at utmost importance.


Figure 20. Vin $=5 \mathrm{~V}, \mathrm{Y} 1=1 \mathrm{mV} / \mathrm{div}$

## MC33765

## TECHNICAL TERMS

Rise Time - Common Enable being in ON state, the device is switched on by ON/OFF pin control.
Let's call $t_{1}$ the time when ON/OFF signal reaches $1 \%$ of its nominal value.

Let's call $t_{2}$ the time when output signal reaches $99 \%$ of its nominal value.

The rise time for this device is specified as:

$$
\mathrm{t}_{\mathrm{ON}}=\mathrm{t}_{1}-\mathrm{t}_{2}
$$

Fall Time - The fall time is highly dependent on the output capacitor and so device design is not impacting at all this parameter.

Overshoot, Settling Time - As regulators are based on regulation loop through an error amplifier, this type of device requires a certain time to stabilize and reach its nominal value.
The overshoot is defined as the voltage difference between the peak voltage and steady state when switching ON the regulator.
The settling time is equal to the time required by the regulator to stabilize to its nominal value ( $\pm 0.5 \%$ ) after peak value when switching ON the regulator.


## MC33762

## Dual Ultra Low-Noise Low Dropout Voltage Regulator with 1.0 V ON/OFF Control

The MC33762 is a dual Low DropOut (LDO) regulator featuring excellent noise performances. Thanks to its innovative design, the circuit reaches an impressive $40 \mu \mathrm{VRMS}$ noise level without an external bypass capacitor. Housed in a small $\mu 8$ package, it represents the ideal designer's choice when space and noise are at premium.

The absence of external bandgap capacitor accelerates the response time to a wake-up signal and keeps it within $40 \mu \mathrm{~s}$, making the MC33762 as a natural candidate for portable applications.

The MC33762 also hosts a novel architecture which prevents excessive undershoots in the presence of fast transient bursts, as in any bursting systems.

Finally, with a static line regulation better than -75 dB , it naturally shields the downstream electronics from choppy lines.

## Features

- Nominal Output Current of 80 mA with a 100 mA Peak Capability
- Ultra-Low Noise: $150 \mathrm{nV} / \sqrt{ } \mathrm{Hz}$ @ $100 \mathrm{~Hz}, 40 \mu \mathrm{VRMS}$ $100 \mathrm{~Hz}-100 \mathrm{kHz}$ Typical, $\mathrm{I}_{\text {out }}=60 \mathrm{~mA}, \mathrm{Co}=1.0 \mu \mathrm{~F}$
- Fast Response Time from OFF to ON: $40 \mu$ s Typical
- Ready for 1.0 V Platforms: ON with a 900 mV High Level
- Typical Dropout of 90 mV @ $30 \mathrm{~mA}, 160 \mathrm{mV}$ @ 80 mA
- Ripple Rejection: 70 dB @ 1.0 kHz
- $1.5 \%$ Output Precision @ $25^{\circ} \mathrm{C}$
- Thermal Shutdown
- $\mathrm{V}_{\text {out }}$ Available at $2.5 \mathrm{~V}, 2.8 \mathrm{~V}$, and 3.0 V
- Separate Dice for Each Regulator Provides Maximum Isolation Between Regulators
- Operating Range from -40 to $+85^{\circ} \mathrm{C}$


## Applications

- Noise Sensitive Circuits: VCOs RF Stages, etc.
- Bursting Systems (TDMA Phones)
- All Battery Operated Devices

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


Micro8 ${ }^{\text {m }}$
DM SUFFIX
CASE 846A

## PIN CONFIGURATION AND MARKING DIAGRAM


(Top View)
Y = Year
WW = Work Week

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 826 of this data sheet.


Figure 1. Simplified Block Diagram

## PIN FUNCTION DESCRIPTIONS

| Pin \# | Pin Name | Function |  |
| :---: | :---: | :--- | :--- |
| 1 | Gnd1 | Ground of the 1st LDO |  |
| 2 | En1 | Enables the 1st LDO | A 900 mV level on this pin is sufficient to start this LDO. A 150 mV shuts it down. |
| 3 | Gnd2 | Ground of the 2nd LDO |  |
| 4 | En2 | Enables the 2nd LDO | A 900 mV level on this pin is sufficient to start this LDO. A 150 mV shuts it down. |
| 5 | $\mathrm{~V}_{\mathrm{cc} 2}$ | 2nd LDO $\mathrm{V}_{\mathrm{cc}}$ pin | This pin brings the power to the 1st LDO and requires adequate decoupling. |
| 6 | $\mathrm{~V}_{\text {out2 }}$ | Shuts or wakes-up the IC | This pin requires a $1.0 \mu \mathrm{~F}$ output capacitor to be stable. |
| 7 | $\mathrm{~V}_{\mathrm{cc} 1}$ | 1st LDO $\mathrm{V}_{\mathrm{cc}}$ pin | This pin brings the power to the 1st LDO and requires adequate decoupling. |
| 8 | $\mathrm{~V}_{\text {out1 }}$ | Delivers the output voltage | This pin requires a $1.0 \mu \mathrm{~F}$ output capacitor to be stable. |

## MAXIMUM RATINGS

| Rating | Pin \# | Symbol | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |
| Power Supply Voltage | 1 | $\mathrm{V}_{\text {in }}$ | - | 12 | V |
| ESD Capability, HBM Model | All Pins | - | - | 1.0 | kV |
| ESD Capability, Machine Model | All Pins | - | - | 200 | V |
| Maximum Power Dissipation NW Suffix, Plastic Package Thermal Resistance Junction-to-Air |  | $\overline{P_{D}}$ <br> $\mathrm{R}_{\theta \mathrm{JJ}-\mathrm{A}}$ |  | Internally Limited $240$ | $\begin{gathered} \mathrm{w} \\ { }^{\circ} \mathrm{C} / \mathrm{w} \end{gathered}$ |
| Operating Ambient Temperature <br> Maximum Junction Temperature (Note 1) <br> Maximum Operating Junction Temperature (Note 2) | - | $\begin{gathered} \mathrm{T}_{\mathrm{A}} \\ \mathrm{~T}_{\mathrm{Jmax}} \\ \mathrm{~T}_{\mathrm{J}} \end{gathered}$ | - | $\begin{gathered} -40 \text { to }+85 \\ 150 \\ 125 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |
| Storage Temperature Range | - | $\mathrm{T}_{\text {stg }}$ | - | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Internally limited by shutdown.
2. Specifications are guaranteed below this value.

## ELECTRICAL CHARACTERISTICS

(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, max $\mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristics | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Logic Control Specifications |  |  |  |  |  |  |
| Input Voltage Range | 2-4 | $\mathrm{V}_{\text {ON/OFF }}$ | 0 | - | $\mathrm{V}_{\text {in }}$ | V |
| ON/OFF Input Resistance (all versions) | 2-4 | $\mathrm{R}_{\text {ON/OFF }}$ | - | 250 | - | $\mathrm{k} \Omega$ |
| ON/OFF Control Voltages (Note 3) Logic Zero, OFF State, $\mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}$ Logic One, ON State, $\mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}$ | 2-4 | $\mathrm{V}_{\text {ON/OFF }}$ | $\overline{900}$ | - | 150 - | mV |

## Currents Parameters

| Current Consumption in OFF State (all versions) OFF Mode Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0, \mathrm{~V}_{\text {OFF }}=150 \mathrm{mV}$ | - | $\mathrm{IQ}_{\text {OFF }}$ | - | 0.1 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Current Consumption in ON State (all versions) ON Mode Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0, \mathrm{~V}_{\mathrm{ON}}=3.5 \mathrm{~V}$ | - | $\mathrm{IQ}_{\mathrm{ON}}$ | - | 180 | - | $\mu \mathrm{A}$ |
| Current Consumption in ON State (all versions), ON Mode Saturation Current: $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}-0.5 \mathrm{~V}$, No Output Load | - | $\mathrm{I}_{\text {SAT }}$ | - | 800 | - | $\mu \mathrm{A}$ |
| Current Limit $\mathrm{V}_{\text {in }}=$ Vout $_{\text {nom }}+1.0 \mathrm{~V}$, <br> Output is brought to Vout $_{\text {nom }}-0.3 \mathrm{~V}$ (all versions) | - | $I_{\text {MAX }}$ | 100 | 180 | - | mA |

Output Voltages

| $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<80 \mathrm{~mA}$ <br> 2.5 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 2.462 | 2.5 | 2.537 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| 2.8 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 2.758 | 2.8 | 2.842 | V |
| 3.0 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 2.955 | 3.0 | 3.045 | V |
| 3.3 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 3.250 | 3.3 | 3.349 | V |
| 3.6 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 3.546 | 3.6 | 3.654 | V |
| Other Voltages up to 5.0 V Available in 50 mV Increment Steps | $5-7$ | $\mathrm{~V}_{\text {out }}$ | -1.5 | X | +1.5 | $\%$ |
| $\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, 1.0 \mathrm{~mA}<\mathrm{I}_{\text {out }}<80 \mathrm{~mA}$ <br> 2.5 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 2.425 | 2.5 | 2.575 | V |
| 2.8 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 2.716 | 2.8 | 2.884 | V |
| 3.0 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 2.91 | 3.0 | 3.090 | V |
| 3.3 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 3.201 | 3.3 | 3.399 | V |
| 3.6 V | $5-7$ | $\mathrm{~V}_{\text {out }}$ | 3.492 | 3.6 | 3.708 | V |
| Other Voltages up to 5.0 V Available in 50 mV Increment Steps | $5-7$ | $\mathrm{~V}_{\text {out }}$ | -3.0 | X | +3.0 | $\%$ |

## Line and Load Regulation, Dropout Voltages

| Line Regulation (all versions) <br> $V_{\text {out }}+1.0 \mathrm{~V}<\mathrm{V}_{\text {in }}<12 \mathrm{~V}, \mathrm{I}_{\text {out }}=80 \mathrm{~mA}$ | $5-7$ | Reg $_{\text {line }}$ | - | - | 20 | mV |
| :--- | :---: | :--- | :--- | :--- | :---: | :---: |
| Load <br> Regulation (all versions) |  |  |  |  |  |  |
| $\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}, \mathrm{C}_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\text {out }}=1.0$ to 80 mA | $5-7$ | Reg $_{\text {load }}$ | - | - | 40 | mV |
| Dropout Voltage (all versions) (Note 3) |  |  |  |  |  |  |
| $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}$ | $5-7$ | $\mathrm{~V}_{\text {in }}-V_{\text {out }}$ | - | 90 | 150 | mV |
| $\mathrm{I}_{\text {out }}=60 \mathrm{~mA}$ | $5-7$ | $\mathrm{~V}_{\text {in }}-V_{\text {out }}$ | - | 140 | 200 |  |
| $\mathrm{I}_{\text {out }}=80 \mathrm{~mA}$ | $5-7$ | $\mathrm{~V}_{\text {in }}-V_{\text {out }}$ | - | 160 | 250 |  |

3. Voltage slope should be greater than $2.0 \mathrm{mV} / \mathrm{\mu s}$

## ELECTRICAL CHARACTERISTICS (continued)

(For typical values $T_{A}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, max $\mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristics | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## Dynamic Parameters

$\left.\begin{array}{|l|c|c|c|c|c|c|}\hline \begin{array}{c}\text { Ripple Rejection (all versions) } \\ V_{\text {in }}=V_{\text {out }}+1.0 \mathrm{~V}+1.0 \mathrm{kHz} 100 \mathrm{mVpp} \text { Sinusoidal Signal }\end{array} & 5-7 & \text { Ripple } & - & -70 & - & \mathrm{dB} \\ \hline \text { Output Noise Density @ } 1.0 \mathrm{kHz} & 5-7 & - & - & 150 & - & \mathrm{nV} / \\ \sqrt{ } \mathrm{Hz}\end{array}\right]$

Thermal Shutdown

| Thermal Shutdown (all versions) | - | - | - | - | 125 |
| :--- | :--- | :--- | :--- | :--- | :--- |

## DEFINITIONS

## Load Regulation

The change in output voltage for a change in output current at a constant chip temperature.

## Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential value). The dropout level is affected by the chip temperature, load current and minimum input supply requirements.

## Output Noise Voltage

This is the integrated value of the output noise over a specified frequency range. Input voltage and output current are kept constant during the measurement. Results are expressed in $\mu$ VRMS.

## Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specs.

## Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

## Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected. One usually distinguishes static line regulation or DC line regulation (a DC step in the input voltage generates a corresponding step in the output voltage) from ripple rejection or audio susceptibility where the input is combined with a frequency generator to sweep from a few hertz up to a defined boundary while the output amplitude is monitored.

## Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically $125^{\circ} \mathrm{C}$, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

## Maximum Package Power Dissipation

The maximum power package power dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. $125^{\circ} \mathrm{C}$. Depending on the ambient temperature, it is possible to calculate the maximum power dissipation and thus the maximum available output current.

## MC33762

## Characterization Curves

Curves are Common to Both Regulators


Figure 2. Ground Current versus Output Current


Figure 4. Dropout versus Output Current


Figure 3. Quiescent Current versus Temperature


Figure 5. Output Voltage versus Output Current


Figure 6. Dropout versus Temperature

## APPLICATION HINTS

## Input Decoupling

As with any regulator, it is necessary to reduce the dynamic impedance of the supply rail that feeds the component. A $1.0 \mu \mathrm{~F}$ capacitor either ceramic or tantalum is recommended and should be connected close to the MC33762 package. Higher values will correspondingly improve the overall line transient response.

## Output Decoupling

Thanks to a novel concept, the MC33762 is a stable component and does not require any specific Equivalent Series Resistance (ESR) neither a minimum output current. Capacitors exhibiting ESRs ranging from a few $\mathrm{m} \Omega$ up to $3.0 \Omega$ can thus safely be used. The minimum decoupling value is $1.0 \mu \mathrm{~F}$ and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices.

## Noise Performances

Unlike other LDOs, the MC33762 is a true low-noise regulator. Without the need of an external bypass capacitor, it typically reaches the incredible level of $40 \mu \mathrm{VRMS}$ overall noise between 100 Hz and 100 kHz . To give maximum insight on noise specifications, ON Semiconductor includes spectral density graphics. The classical bypass capacitor impacts the start-up phase of standard LDOs. However, thanks to its low-noise architecture, the MC33762 operates without a bypass element and thus offers a typical $40 \mu$ s start-up phase.

## Protections

The MC33762 hosts several protections, giving natural ruggedness and reliability to the products implementing the component. The output current is internally limited to a maximum value of 180 mA typical while temperature shutdown occurs if the die heats up beyond $125^{\circ} \mathrm{C}$. These values let you assess the maximum differential voltage the device can sustain at a given output current before its protections come into play.

The maximum dissipation the package can handle is given by:

$$
P_{\max }=\frac{T_{J \max }-T_{A}}{R_{\theta J A}}
$$

If $\mathrm{T}_{\text {Jmax }}$ is limited to $125^{\circ} \mathrm{C}$, then the MC33762 can dissipate up to $395 \mathrm{~mW} @ 25^{\circ} \mathrm{C}$. The power dissipated by the MC33762 can be calculated from the following formula:

$$
\text { Ptot }=\left(\mathrm{v}_{\text {in }} \times \mathrm{I}_{\text {gnd }}\left(\mathrm{I}_{\text {out }}\right)\right)+\left(\mathrm{v}_{\text {in }}-\mathrm{v}_{\text {out }}\right) \times \mathrm{I}_{\text {out }}
$$

or

$$
\mathrm{Vin}_{\max }=\frac{\text { Ptot }+\mathrm{V}_{\text {out }} \times \mathrm{I}_{\text {out }}}{I_{\text {gnd }}+I_{\text {out }}}
$$

If a 80 mA output current is needed, the ground current is extracted from the data-sheet curves: $4.0 \mathrm{~mA} @ 80 \mathrm{~mA}$. For a half $2.8 \mathrm{~V} \mathrm{MC} 33762(2.8 \mathrm{~V})$ operating at $25^{\circ} \mathrm{C}$, the maximum input voltage will then be 7.3 V .

## Typical Applications

The following picture portrays the typical application of the MC33762.

## MC33762



Figure 7. A Typical Application Schematic

As for any low noise designs, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. Connections shall be kept short and wide. Layout example
as given in the MC33761 application hints can be used as a starting basis.

## Understanding the Load Transient Improvement

The MC33762 features a novel architecture which allows the user to easily implement the regulator in burst systems where the time between two current shots is kept very small.

The quality of the transient response time is related to many parameters, among which the closed-loop bandwidth with the corresponding phase margin plays an important role. However, other characteristics also come into play like the series pass transistor saturation. When a current perturbation suddenly appears on the output, e.g. a load increase, the error amplifier reacts and actively biases the PNP transistor. During this reaction time, the LDO is in open-loop and the output impedance is rather high. As a result, the voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place with a positive overshoot. The problem appears when this overshoot decays down to the LDO steady-state value.


Figure 8. A Standard LDO Behavior when the Load Current Disappears


Figure 10. Without Load Transient Improvement

During this decreasing phase, the LDO stops the PNP bias and one can consider the LDO asleep (Figure 8). If by misfortune a current shot appears, the reaction time is incredibly lengthened and a strong undershoot takes place. This reaction is clearly not acceptable for line sensitive devices, such as VCOs or other Radio-Frequency parts. This problem is dramatically exacerbated when the output current drops to zero rather than a few mA. In this later case, the internal feedback network is the only discharge path, accordingly lengthening the output voltage decay period (Figure 9).
The MC33762 cures this problem by implementing a clever design where the LDO detects the presence of the overshoot and forces the system to go back to steady-state as soon as possible, ready for the next shot. Figure 10 and 11 show how it positively improves the response time and decreases the negative peak voltage.


Figure 9. A Standard LDO Behavior when the Load Current Appears in the Decay Zone


Figure 11. MC33762 with Load Transient Improvement

## MC33762

## MC33762 Has a Fast Start-Up Phase

Thanks to the lack of bypass capacitor the MC33762 is able to supply its downstream circuitry as soon as the OFF to ON signal appears. In a standard LDO, the charging time of the external bypass capacitor hampers the response time. A simple solution consists in suppressing this bypass element but, unfortunately, the noise rises to an
unacceptable level. MC33762 offers the best of both worlds since it no longer includes a bypass capacitor and starts in less than $40 \mu$ s typically (Repetitive at 200 Hz ). It also ensures an incredible low-noise level of $40 \mu$ VRMS $100 \mathrm{~Hz}-100 \mathrm{kHz}$. The following picture details the typical 33762 startup phase.


Figure 12. Repetitive Start-Up Waveforms

TYPICAL TRANSIENT RESPONSES


Figure 13. Output is Pulsed from 2.0 mA to 80 mA

Figure 15. Load Transient Improvement Effect


Figure 14. Discharge Effects from 0 to 40 mA


Figure 16. Load Transient Improvement Effect

TYPICAL TRANSIENT RESPONSES


Figure 17. MC33762 Typical Noise Density Performance


Figure 18. MC33762 Typical Ripple Rejection Performance


Figure 19. Output Impedance Plot
$C_{\text {out }}=1.0 \mu \mathrm{~F}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {out }}+1.0 \mathrm{~V}$

## MC33762

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface
between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.


## MC33762

ORDERING INFORMATION

| Part Number | Voltage Output | Package | Shipping |
| :---: | :---: | :---: | :---: |
| MC33762DM-2525R2 | $2.5 \mathrm{~V} \& 2.5 \mathrm{~V}$ | Micro8 | 4000 Units / Tape \& Reel |
| MC33762DM-2828R2 | $2.8 \mathrm{~V} \& 2.8 \mathrm{~V}$ | Micro8 | 4000 Units / Tape \& Reel |
| MC33762DM-3030R2 | $3.0 \mathrm{~V} \& 3.0 \mathrm{~V}$ | Micro8 | 4000 Units / Tape \& Reel |

## MC33566

## Smart Voltage Regulator for Peripheral Card Applications

The MC33566 Low Dropout Regulator is designed for computer peripheral card applications complying with the instantly available requirements as specified by ACPI objectives. The MC33566 permits glitch-free transitions from "sleep" to "active" system modes and has internal logic circuitry to detect whether the system is being powered from the motherboard main 5.0 V power supply or the 3.3 V aux supply.

The MC33566 provides a regulated output voltage of 3.3 V via either an internal low dropout 5.0 V-to-3.3 V voltage regulator or an external P-channel MOSFET, depending on the operating status of the system in which the card is installed. During normal operating mode ( 5.0 V main supply available) the 3.3 V output is provided from the internal low dropout regulator at an output current of 0.4 A . When the motherboard enters sleep mode, the MC33566 operates from the 3.3 V aux supply and routes the aux current to the output via the external P-channel MOSFET bypass transistor controlled by the drive out pin. As a result, the output voltage provided to the peripheral card remains constant at 3.3 V even during host systems transitions to and from sleep mode.

## MC33566 Features:

- Output Current up to 0.4 A
- Excellent Line and Load Regulation
- Low Dropout Voltage
- Prevents Reverse Current Flow During Sleep Mode
- Glitch-Free Transfer from Sleep Mode to Active Mode
- Compatible with Instantly Available PC Systems


Figure 1. Simplified Block Diagram


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC33566D2T-1 | D2PAK | 50 Units/Rail |
| MC33566D2T-1RK | D2PAK | 2500 Tape \& Reel |

PIN ASSIGNMENTS AND FUNCTIONS

| Pin \# | Pin Name | Pin Description |
| :---: | :---: | :--- |
| 1 | $+3.3 \mathrm{~V}_{\mathrm{aux}}$ | Auxiliary input. Typical voltage 3.3 V. |
| 2 | $+5.0 \mathrm{~V}_{\text {in }}$ | This is the input supply for the IC. Typical voltage 5.0 V. (Notes 1 and 2) |
| 3 | Gnd | Logic and power ground. |
| 4 | $+3.3 \mathrm{~V}_{\text {out }}$ | 3.3 V output provided to the application circuit (output current is sourced to this pin from the <br> 5.0 V input.) |
| 5 | Drive out | This output drives a P-channel MOSFET with up to 2000 pF of "effective" gate capacitance. <br> Recommended devices are the MMFT5P03HD and MTSF1P02HD. Drive out has active internal <br> pull-up and pull-down circuitry to guarantee fast transitions. |

MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| $+5.0 \mathrm{~V}_{\text {in }}$ Supply Voltage | $\mathrm{V}_{\text {in }}$ | 7.0 | Vdc |
|  | $\mathrm{V}_{\text {in }}$ | $-0.5($ Note 3$)$ | Vdc |
|  | $\mathrm{T}_{\mathrm{a}}$ | -5.0 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | -5.0 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 seconds) | $\mathrm{T}_{\mathrm{L}}$ | 300 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance | $\mathrm{R}_{\text {өJA }}($ Note 4$)$ | 65 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

AC ELECTRICAL SPECIFICATIONS (Notes 5, 6, and 7)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive High Delay ( $\mathrm{V}_{\text {in }}$ ramping up) <br> $\mathrm{C}_{\text {drive }}=1.2 \mathrm{nF}$, measured from $+5.0 \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {thresHi }}$ to $\mathrm{V}_{\text {Drive }}=2.0 \mathrm{~V}$ | $t_{\text {DH }}$ | - | 0.5 | 3.5 | $\mu \mathrm{S}$ |
| Drive Low Delay ( $\mathrm{V}_{\text {in }}$ ramping down) <br> $\mathrm{C}_{\text {drive }}=1.2 \mathrm{nF}$, measured from $+5.0 \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {thresLo }}$ to $\mathrm{V}_{\text {Drive }}=2.0 \mathrm{~V}$ | $t_{\text {DL }}$ | - | 0.5 | 3.5 | $\mu \mathrm{S}$ |

1. See 5.0 V Detect Thresholds Diagram.
2. Recommended source impedance for 5.0 V supply: $\leq 0.12 \Omega$. This will ensure that $\mathrm{I}_{0} \times \mathrm{R}_{\text {source }}<\mathrm{V}_{\text {hyst }}$, thus avoiding driveout toggling during 5.0 V detect threshold transitions.
3. $\mathrm{V}_{\text {in }}$ should not be allowed to go negative relative to ground.
4. Mounted on recommended minimum PCB pad on FR4, 2-oz. copper circuit board.
5. AC specs are guaranteed by characterization, but not production tested after characterization.
6. See Figure 3. Application Block Diagram.
7. See Timing Diagram.

DC ELECTRICAL CHARACTERISTICS (Note 8)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $+5.0 \mathrm{~V}_{\text {in }}$ Supply Voltage Range | $+5.0 \mathrm{~V}_{\text {in }}$ | 4.35 | 5.0 | 5.5 | Vdc |
| Reverse Leakage Current from Output | $\mathrm{I}_{\text {reverse }}$ | - | - | 25 | $\mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {aux }}$ Quiescent Current | $\mathrm{I}_{\text {qaux }}$ | - | - | 2.0 | mA |
| $+5.0 \mathrm{~V}_{\text {in }}$ Quiescent Current, Operating | $\mathrm{I}_{\text {qvin }}$ | - | - | 10 | mA |
| Load Capacitance (Note 9) | $\mathrm{C}_{\text {load }}$ | 4.7 | 22 | - | $\mu \mathrm{F}$ |

REGULATOR OUTPUT

| Output Voltage $\begin{aligned} & \left(4.35 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 5.5 \mathrm{~V}, 0 \mathrm{~mA} \leq \mathrm{I}_{0} \leq 400 \mathrm{~mA}\right) \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \left(\mathrm{~T}_{J}=-5^{\circ} \mathrm{C} \text { to } 150^{\circ} \mathrm{C}\right) \end{aligned}$ | +3.3 $\mathrm{V}_{\text {out }}$ | $\begin{aligned} & 3.267 \\ & 3.234 \end{aligned}$ | $\begin{aligned} & 3.30 \\ & 3.30 \end{aligned}$ | $\begin{aligned} & 3.333 \\ & 3.366 \end{aligned}$ | Vdc |
| :---: | :---: | :---: | :---: | :---: | :---: |
| In-to-Out Voltage $\left(3.9 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 4.35 \mathrm{~V}, \mathrm{~V}_{\text {aux }}=3.3 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{d}}$ | 3.0 | - | - | Vdc |
| Voltage Out at Max Voltage In $\left(\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {outmax }}$ | 3.1 | 3.3 | 3.5 | Vdc |
| Line Regulation $\left(I_{0}=400 \mathrm{~mA}\right)$ | Linereg | - | - | 0.4 | \% |
| Load Regulation $\left(\mathrm{I}_{0}=0 \text { to } 400 \mathrm{~mA}\right)$ | Loadreg | - | - | 0.8 | \% |

5.0 V DETECT

| Low Threshold Voltage <br> $\left(+5.0 \mathrm{~V}_{\text {in }}\right.$ Falling, $\left.\mathrm{I}_{\mathrm{O}}=400 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {thresLo }}$ | 3.9 | 4.05 | - | Vdc |
| :--- | :---: | :---: | :---: | :---: | :---: |
| High Threshold Voltage <br> $\left(+5.0 \mathrm{~V}_{\text {in }}\right.$ Rising, $\left.\mathrm{I}_{\mathrm{O}}=400 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {thresHi }}$ | - | 4.2 | 4.35 | Vdc |
| Hysteresis | $\mathrm{V}_{\text {hyst }}$ | 0.05 | - | - | Vdc |

## DRIVE OUTPUT

| Output Peak Source Current <br> $\left(+5.0 \mathrm{~V}_{\text {in }}>\mathrm{V}_{\text {thresHi }}\right)$ | $\mathrm{I}_{\text {peak }}$ | 15 | - | - | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Peak Sink Current <br> $\left(+5.0 \mathrm{~V}_{\text {in }}<\mathrm{V}_{\text {thresLo }}\right)$ | $\mathrm{I}_{\text {peak }}$ | 15 | - | - | mA |
| Low Output Voltage <br> $\left(\mathrm{I}_{\mathrm{oL}}=200 \mu \mathrm{~A}, \mathrm{~V}_{\text {in }}<\mathrm{V}_{\text {thresLo }}\right)$ | $\mathrm{V}_{\mathrm{oL}}$ | - | 100 | 200 | mVdc |
| High Output Voltage <br> $\left(\mathrm{I}_{\mathrm{oH}}=200 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{oH}}$ | 3.4 | - | - | Vdc |

8. $-5^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{a}}<70^{\circ} \mathrm{C}, 4.35 \mathrm{~V}<\mathrm{V}_{\text {in }}<5.5 \mathrm{~V}, \mathrm{C}_{\text {load }} \geq 4.7 \mu \mathrm{~F}$ unless otherwise noted.
9. $4.7 \mu \mathrm{~F}$ minimum over temperature; $22 \mu \mathrm{~F}$ recommended; $500 \mathrm{~m} \Omega$ ESR maximum.


Figure 2. Functional Block Diagram
FUNCTIONAL DESCRIPTION

Input Blocking - The internal NPN pass transistor of the LDO regulator ensures that no significant reverse current will flow from $+3.3 \mathrm{~V}_{\text {out }}$ back to the $+5.0 \mathrm{~V}_{\text {in }}$ input when the 5.0 V input is not powered and the $3.3 \mathrm{~V}_{\text {in }}$ supply is present.
5.0 Volt Detect - Internal circuitry detects the presence of the 5.0 V input supply. When the 5.0 V supply drops below a given threshold, the $+3.3 \mathrm{~V}_{\mathrm{in}}$ bypass transistor (an external P -channel MOSFET) is enabled. The 5.0 V detect logic is active throughout the entire range of ramp-up from 0 to 5.5 V . Additionally, the drive out signal is never turned ON or OFF inappropriately during ramp-up of the $+5.0 \mathrm{~V}_{\text {in }}$ supply. Also, $+3.3 \mathrm{~V}_{\text {out }}$ never drops below 3.0 V while $+5.0 \mathrm{~V}_{\mathrm{in}}$ is above the 5.0 V detect minimum threshold.

Glitch-free Transfer - The design of the 5.0 V detect circuitry and drive out control circuitry guarantees that the $+3.3 \mathrm{~V}_{\text {out }}$ will not exceed the output voltage specification listed in the table of DC Operating Specifications even with $+5.0 \mathrm{~V}_{\text {in }}$ ramping up and down at the extremes of the slew rates in the table of AC Operating Specifications.
Offset Voltage Performance - To ensure performance when external offsets are present on the $+5.0 \mathrm{~V}_{\text {in }}$ and $+3.3 \mathrm{~V}_{\text {in }}$ power inputs, the device has been designed to be capable of operating with either one or both of these inputs rising from or falling to zero volts, or with offsets of 0.05 V to 0.9 V as the inputs ramp up and down.


Figure 3. Application Block Diagram


NOTE:
(1) $V_{\text {in }}$ rise and fall times ( $10 \%$ to $90 \%$ ) to be $\geq 100 \mu \mathrm{~s}$.

Figure 4. 5.0 V Detect Thresholds Diagram


NOTE: $\mathrm{V}_{\text {out }}$ capacitor $\geq 4.7 \mu \mathrm{~F}$ over operating temperature range. Maximum ESR permissable $=500 \mathrm{~m} \Omega$ over operating temperature range.

Figure 6. Predicted Gain and Phase at Zero Load Current


NOTE:
(1) $\mathrm{V}_{\text {in }}$ rise and fall times ( $10 \%$ to $90 \%$ ) to be $\leq 100 \mathrm{~ns}$.

Figure 5. Timing Diagram


Figure 7. Predicted Gain and Phase at Full Load Current

## MC33567

## Dual Linear Controller for High Current Voltage Regulation

The MC33567 Dual Linear Power Supply Controller is designed to facilitate power management for motherboard applications where reliable regulation of high current supply planes is required. It provides the Drive, Sense and Control signals to interface two external, N-channel MOSFETs for regulating two different supply planes. Undervoltage, short circuit detection places the operation of the system into a protected mode pending removal of the short.

## Features

- MC33567-1: Two, Independent Regulated Supplies 1.515 V - Supply for GTL and AGP Planes 1.818 V - Supply for I/O Plane and Memory Termination
- MC33567-2: Dual 2.525 V Supplies for Clock and Memory
- Undervoltage Detection and Protection Mode
- Drive Capability for SOT-223, DPAK, and D ${ }^{2}$ PAK MOSFETs
- Bypass Function for 3.3 V AGP Card Detection


## Applications

- Motherboards
- Dual Power Supplies



## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com

MARKING DIAGRAM

$x=1$ or 2
A =Assembly Location
L = Wafer Lot
$Y=$ Year
W = Work Week

PIN CONNECTIONS


## Simplified Functional Block Diagram



## MAXIMUM RATINGS*

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\text {cc }}$ | 12.5 | Vdc |
| Operating Ambient Temperature | Ta | 0 to +80 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | TJ | -5 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 seconds) | $\mathrm{T}_{\mathrm{L}}$ | 300 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance, Junction to Ambient | $\mathrm{R}_{\text {өJA }}$ Note 1 | 159 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction to Case | $\mathrm{R}_{\text {өJC }}$ | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

1. Minimum pad test board with 5 MIL wide and 2.8 MIL thick copper traces 1 inch long.
*All characterizing done with MTD3055VL N-Channel MOSFETs.

## DC ELECTRICAL CHARACTERISTICS

|  | Characteristic | Symbol | Min | Typ | Max |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{cc}}$ | 9.0 | 12 | 12.5 | V |
| Quiescent Current | $\mathrm{I}_{\mathrm{qL}}$ | - | 6.0 | 9.0 | mA |
|  | $\mathrm{I}_{\mathrm{qH}}$ | - | 7.0 | 10 |  |

## UNDER VOLTAGE LOCKOUT

| Undervoltage Lockout | UVLO | 7.0 | 8.5 | 9.0 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Hysteresis | $\mathrm{V}_{\text {hys }}$ | 0.2 | 0.5 | 0.9 | V |

## DRIVE

| Drive Voltage (Gate to Ground) | $\mathrm{V}_{\text {drv }}$ | - | - | 10.5 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Gate Drive Source Output Current (Pin 1, Pin 7) | $\mathrm{I}_{\text {pkdrv }}$ | 10 | 20 | 30 | mA |
| Gate Drive Sink Current (Steady State) | $\mathrm{I}_{\text {sink }}$ | 5.0 | 7.0 | 10 | mA |

## SHUTDOWN

| Shutdown Threshold | SHDN | 0.8 | 1.13 | 1.3 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Shutdown Hysteresis | SHDN $_{\text {hys }}$ | - | 130 | - | mV |
| Shutdown Disable Time | SHDN $_{\text {tdis }}$ | - | 0.5 | 2.0 | $\mu \mathrm{~s}$ |
| Shutdown Current Threshold | $\mathrm{I}_{\text {SHDN }}$ | - | 37 | - | $\mu \mathrm{A}$ |

## SHORT CIRCUIT

| Short Circuit Response Time | $\mathrm{SC}_{\text {td }}$ | - | 250 | - | $\mu \mathrm{s}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Short Circuit On Time | $\mathrm{SC}_{\text {ton }}$ | 0.5 | 0.8 | 1.5 | ms |
| Short Circuit Off Time | $\mathrm{SC}_{\text {toff }}$ | 20 | 40 | 60 | ms |
| Short Circuit/Undervoltage Detect <br> (Load current increased until output drops) | $\mathrm{SC}_{\text {uvd }}$ | 70 | - | 80 | $\%$ Vout |

## OUTPUT REGULATION

| MC33567-1 |  |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Regulator 1 | $V_{\text {reg1 }}$ | - | 1.818 | - |  |
| Regulator 2 | $V_{\text {reg2 }}$ | - | 1.515 | - |  |
| MC33567-2 | - | - | 2.525 | - |  |
| Output Voltage Regulation (Full-Load to No-Load @ $25-70^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {reg\% }}$ | -2.5 | - | +2.5 | $\%$ |



* Internal ground disables bypass on function on the 1.818 V regulator in the MC33567-1 and on the 2.525 V regulators in the $\mathrm{MC} 33567-2$. A1 and A2 are undervoltage comparators.

Figure 1. Functional Block Diagram
PIN ASSIGNMENTS AND FUNCTIONS

| PIN \# | PIN NAME | PIN DESCRIPTION |
| :---: | :---: | :--- |
| 1 | Gate 1 drive | Drives MOSFET into linear region. Is internally clamped to ground in power down mode. |
| 2 | Sense 1 line | Returns regulated output from MOSFET. |
| 3 | Shutdown 1 | At TTL high level turns off regulation for gate 1. Effectively grounds gate 1. (Internal pull-up to 3.3 V) |
| 4 | Ground |  |
| 5 | Shutdown 2 | At TTL high level turns off regulation for gate 2. Effectively grounds gate 2. (Internal pull-up to 3.3 V) |
| 6 | Sense 2 line | Returns regulated output from MOSFET. |
| 7 | Gate 2 drive | Drives MOSFET into linear region for 1.515 V operation. Saturates external FET in bypass mode. <br> Is internally clamped to ground in power down mode. |
| 8 | 12 volt input | Supply voltage for operation and gate drive output. |

## OPERATING DESCRIPTION

The MC33567 Dual Linear Controller is designed for power management applications where high current, voltage regulation is needed. Some computer applications include:

- 1.515 V - AGP (Advanced Graphic Port) and GTL+ (Gunning Transistor Logic - Intel's electrical bus technology)
- $1.818 \mathrm{~V}-\mathrm{I} / \mathrm{O}$ planes on motherboard
- 2.525 V - Clock and memory


## Hiccup Mode

If the output drops below $75 \%$ of the regulated threshold for greater than $250 \mu$ s or a short circuit condition exists, that output will go into hiccup mode. This means that the output is turned ON for 1.0 ms and OFF for 40 ms for a duty cycle of 1:40. Please refer to Figure 2. Each transition from low to high of the input restarts the hiccup mode holdoff period. Once the short circuit is removed or the output comes back to the regulated threshold, it will operate under normal operating conditions.


Figure 2. Hiccup Mode Duty Cycle

## Shutdown

The SHUTDOWN pin is connected to the external board (AGP or GTL+). Please refer to Figure 3.


PIN 5 TRUTH TABLE
Pin 5 No connect $=1.515 \mathrm{~V}$ LDO drive out active Pin $5<0.8 \mathrm{~V}=$ shutdown (drive out 0 V ) $1.3 \mathrm{~V}<\operatorname{pin} 5<4.1 \mathrm{~V}=1.515 \mathrm{~V}$ LDO drive out active Pin $5>4.2 \mathrm{~V}=3.3 \mathrm{~V}$ bypass mode (drive out $=\mathrm{V}_{\text {in }}$ for FET )

The way in which the external board is wired to the shutdown pin will determine the output of the MC33567. Listed are the conditions the external board is wired and the corresponding output voltages:

1. If there is no connection on the external board, there is an open and the output will be the regulated output voltage.
2. If there is a ground on the external board which will cause the SHUTDOWN pin to be less than 0.8 V , the MOSFET turns off and there is no output voltage.
3. If there is a resistor on the external board pulling the SHUTDOWN pin above 4.1 V , the output will be in the bypass mode. In this mode, the MOSFET is fully on, or fully enhanced, and the output will be whatever voltage is supplied to the input voltage of the MOSFET, $\mathrm{V}_{\text {in }}$.
4. If the SHUTDOWN pin is between 1.3 V and 4.1 V , the output will be the regulated voltage.
Tables 1 and 2 are the logic tables for the SHUTDOWN pins. Note that the logic tables are not the same for the 1.515 V regulator and the 1.818 V regulator. The MC33567-2 does not have the Full-On Bypass feature.

Table 1. Logic Table for Shutdown (Pin 5) on the 1.515 V Regulator

| SHUTDOWN Pin | $\mathbf{1 . 5 1 5} \mathbf{V}$ Regulator Output |
| :---: | :---: |
| No Connect | 1.515 V |
| $<0.8 \mathrm{~V}$ | Shutdown |
| $1.3 \mathrm{~V}<$ SHDN $<4.1 \mathrm{~V}$ | 1.515 V |
| $>4.2 \mathrm{~V}$ | $\mathrm{~V}_{\text {in }}=$ Bypass |

Table 2. Logic Table for Shutdown (Pin 3)
on the 1.818 V Regulator

| SHUTDOWN Pin | $\mathbf{1 . 8 1 8} \mathbf{V}$ Regulator Output |
| :---: | :---: |
| No Connect | 1.818 V |
| $<0.8 \mathrm{~V}$ | Shutdown |
| $>1.3 \mathrm{~V}$ | 1.818 V |

Figure 3. 1.5 V/3.3 V AGP Card Detection

## Sense

The SENSE pins provide tight regulation of the load voltages with varying load currents. When the load is located at a distance, there will be a voltage drop due to the resistance loss of the trace. If the load is not near the MC33567, it is recommended that the SENSE pins be used. Connect the SENSE pins as close to the load as possible. Use a separate trace to connect the source of the N-Channel MOSFET to the load. Refer to Figure 4.


Figure 4.

## Capacitor Selection

Stable operation is achieved by preserving an adequate phase margin. A rule of thumb for preserving an adequate phase margin is:

$$
\begin{aligned}
& C \cdot R \geq 10 \times 10^{-6} \\
& R \geq \frac{10 \times 10^{-6}}{C}
\end{aligned}
$$

Where:

$$
\begin{aligned}
& \mathrm{C}=\text { load capacitance } \\
& \mathrm{R}=\text { equivalent series resistance }(\mathrm{ESR}) \text { of the capacitor }
\end{aligned}
$$

For example, if the load capacitor is $400 \mu \mathrm{~F}$, then the ESR of the capacitor would need to be no less than $25 \mathrm{~m} \Omega$.

$$
25 \mathrm{~m} \Omega \geq \frac{10 \times 10^{-6}}{400 \mu \mathrm{~F}}
$$

This rule of thumb assumes that all capacitors across the load are the same type and value. If different types and values are used in parallel across the load, then each individual capacitor must meet the requirements of the given equation.

## PCB Layout Guidelines

It is recommended that the MC33567 be placed as physically close as possible to the external series pass MOSFET transistors. Use short traces to minimize extraneous signals from being magnetically or electrostatically induced on the sense or drive lines. Place the sense trace and power trace in the same plane and same direction. The power trace is to be placed from the series pass transistor source lead to the load. Avoid routing the sense lead near the load current return path. Also avoid unterminated runs of the sense leads. If it is desired to have options where the sense lead is placed on the board, use $0 \Omega$ resistor jumpers to make the alternate sense lead connection near the sense pin.

## N-Channel MOSFET Selection

The ON Semiconductor MTD3055VL N-Channel MOSFET was used in the characterization of the MC33567. To select a N-Channel MOSFET the drain-source on-resistance, $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$, must be considered. For best results, $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ needs to be low. Below is the calculation for $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$. The 0.5 in the equation is to prevent saturation and to account for tolerance build-up.

$$
\mathrm{R}_{\mathrm{DS}(\mathrm{on})} \leq 0.5 \frac{\mathrm{~V}_{\text {in }}-\mathrm{V}_{\text {out }}}{\mathrm{I}_{\text {Load }}}
$$

Where:

$$
\begin{aligned}
& \mathrm{V}_{\text {in }}=3.3 \mathrm{~V} \text { typically } \\
& \mathrm{V}_{\text {out }}=1.515 \mathrm{~V}, 1.818 \mathrm{~V} \text {, or } 2.525 \mathrm{~V} \\
& \mathrm{I}_{\text {Load }}=\text { Current at load }
\end{aligned}
$$

Select a N-channel MOSFET that has a $\mathrm{R}_{\mathrm{DS}(\text { on })}$ lower than the calculated value.


Figure 5. Application Block Diagram

Parts List

| Qty | Reference | Part/Description | Vendor | Notes |
| :---: | :---: | :---: | :---: | :---: |
| 4 | C1, C2, C3, C4 | $100 \mu$ F Electrolytic Capacitor | Various |  |
| 1 | U1 | MC33567 | ON Semiconductor |  |
| 2 | Q1, Q2 | MTD3055VL | ON Semiconductor | N-Channel MOSFET |

## MC33567 TYPICAL CHARACTERISTICS



Figure 6. Gain-Phase Plot @ $50 \mathrm{~m} \Omega$


Figure 7. Gain-Phase Plot @ $200 \mathrm{~m} \Omega$


Figure 8. Regulator 1 Load Regulation vs. Temperature Gate Drive 2 Open


Figure 10. Gate Drive Sink Current vs. Temperature


Figure 12. Regulator 1 Line Regulation vs. Temperature 50 mA Load ( 3.0 V to 3.6 V )


Figure 9. Regulator 2 Load Regulation vs. Temperature Gate Drive 1 is Open


Figure 11. SHDN Quiescent Current vs. Temperature 50 mA Load


Figure 13. Regulator 2 Line Regulation vs. Temperature 50 mA Load (3.0 V to 3.6 V)


Figure 14. Under Voltage Lock Out Threshold vs. Temperature


Figure 16. Regulator 2 Maximum Gate Voltage with $\mathrm{SHDN}=4.2 \mathrm{~V}$ vs. Temperature $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$


Figure 15. Under Voltage Hysteresis vs. Temperature


Figure 17. Hiccup Off Time Temperature


Figure 18. Hiccup On Time vs. Temperature

## MC33567

## ORDERING INFORMATION

| Device | Output Voltage <br> $\left(\mathbf{V}_{\text {out } 1}\right)$ | Regulated/Bypass <br> $\left(\mathbf{V}_{\text {out2 }}\right)$ | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| MC33567D-1 | 1.8 V | $1.5 \mathrm{~V} / 3.3 \mathrm{~V}$ | SO-8 | 98 Units/Rail |
| MC33567D-1R2 | 1.8 V | $1.5 \mathrm{~V} / 3.3 \mathrm{~V}$ | SO-8 | 2500 Tape \& Reel |
| MC33567D-2 | 2.5 V | 2.5 V | SO-8 | 98 Units/Rail |
| MC33567D-2R2 | 2.5 V | 2.5 V | SO-8 | 2500 Tape \& Reel |

## 100 mA, 5.0 V Voltage Regulator and Supervisory Circuit for Microprocessors

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These integrated circuits feature a $5.0 \mathrm{~V} / 100 \mathrm{~mA}$ regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- 5.0 V Regulator Output Current in Excess of 100 mA
- Internal Short Circuit Current Limiting
- Pinned Out 2.6 V Reference
- Low Voltage Reset Comparator
- Power Warning Comparator with Programmable Hysteresis
- Uncommitted Comparator
- Low Standby Current
- Internal Thermal Shutdown Protection
- Heat Tab Power Package


MC34160 MC33160

## MICROPROCESSOR VOLTAGE REGULATOR/ SUPERVISORY CIRCUIT

## SEMICONDUCTOR TECHNICAL DATA


-

PIN CONNECTIONS


| Device | Operating <br> Temperature Range | Package |
| :--- | :---: | :---: |
| MC34160DW | $T_{A}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | SOP-16L |
| MC 34160 P |  | DIP-16 |
| MC33160DW | $\mathrm{T}_{A}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SOP-16L |
|  |  | DIP-16 |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $V_{\text {CC }}$ | 40 | V |
| Chip Disable Input Voltage (Pin 15, Note 1) | $V_{C D}$ | -0.3 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Comparator Input Current (Pins 1, 2, 9) | $l_{\text {in }}$ | -2.0 to +2.0 | mA |
| Comparator Output Voltage (Pins 6, 7, 8) | $\mathrm{V}_{\mathrm{O}}$ | 40 | V |
| Comparator Output Sink Current (Pins 6, 7, 8) | $I_{\text {Sink }}$ | 10 | mA |
| Power Dissipation and Thermal Characteristics <br> P Suffix, Dual-In-Line Case 648C <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13) <br> DW Suffix, Surface Mount Case 751G <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13) | $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJc }}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | $\begin{aligned} & 80 \\ & 15 \\ & \\ & 94 \\ & 18 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature $\begin{aligned} & \text { MC34160 } \\ & \text { MC33160 } \end{aligned}$ | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{I}_{\mathrm{ref}}=100 \mu \mathrm{~A}\right)$ For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REGULATOR SECTION |  |  |  |  |  |
| Total Output Variation ( $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ to 40 V , $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to $100 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ | $\mathrm{V}_{\mathrm{O}}$ | 4.75 | 5.0 | 5.25 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | Regline | - | 5.0 | 40 | mV |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~V}$ to $100 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | Regload | - | 20 | 50 | mV |
| Ripple Rejection $\left(\mathrm{V}_{\mathrm{CC}}=25 \mathrm{~V} \text { to } 35 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=40 \mathrm{~mA}, \mathrm{f}=120 \mathrm{~Hz}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | RR | 50 | 6.5 | - | dB |

## REFERENCE SECTION

| Total Output Variation $\left(\mathrm{V}_{\mathrm{CC}}=7.0\right.$ to 40 V,$$ <br> $\mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~mA}$ to $2.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ | $\mathrm{V}_{\text {ref }}$ | 2.47 | 2.6 | 2.73 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right.$ to $\left.40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | Regline | - | 2.0 | 20 | mV |
| Load Regulation $\left(\mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~mA}\right.$ to $\left.2.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | Reg $_{\text {load }}$ | - | 4.0 | 30 | mV |

RESET COMPARATOR

| Threshold Voltage |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\quad$ High State Output (Pin 11 Increasing) | $\mathrm{V}_{\mathrm{IH}}$ | - | $\left(\mathrm{V}_{\mathrm{O}}-0.11\right)$ | $\left(\mathrm{V}_{\mathrm{O}}-0.05\right)$ | V |
| Low State Output (Pin 11 Decreasing) | $\mathrm{V}_{\mathrm{IL}}$ | 4.55 | $\left(\mathrm{~V}_{\mathrm{O}}-0.18\right)$ | - |  |
| Hysteresis | $\mathrm{V}_{\mathrm{H}}$ | 0.02 | 0.07 | - |  |
| Output Sink Saturation $\left(\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{I}_{\text {Sink }}=2.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | - | 0.4 | V |
| Output Off-State Leakage $\left(\mathrm{V}_{\mathrm{OH}}=40 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{OH}}$ | - | - | 4.0 | $\mu \mathrm{~A}$ |

NOTES: 1. The maximum voltage range is -0.3 V to $\mathrm{V}_{\mathrm{CC}}$ or +35 V , whichever is less.
2. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34160 $\quad \mathrm{T}_{\text {high }}=70^{\circ} \mathrm{C}$ for MC34160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}, \mathrm{I}_{\text {ref }}=100 \mu \mathrm{~A}$ ) For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $T_{A}$ is the operating ambient temperature range that applies [Notes 2 and 3 ], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| POWER WARNING COMPARATOR |  |  |  |  |  |
| Input Offset Voltage | $\mathrm{V}_{10}$ | - | 1.2 | 10 | mV |
| Input Bias Current ( $\mathrm{V}_{\text {Pin } 9}=3.0 \mathrm{~V}$ ) | $\mathrm{IIB}^{\text {I }}$ | - | - | 0.5 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Input Hysteresis Current }\left(\mathrm{V}_{\text {Pin } 9}=\mathrm{V}_{\text {ref }}-100 \mathrm{mV}\right) \\ & \mathrm{R}_{\text {Pin } 10}=24 \mathrm{k} \\ & \mathrm{R}_{\text {Pin } 10}=\infty \end{aligned}$ | $\mathrm{IH}^{\text {H}}$ | $\begin{aligned} & 40 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 50 \\ & 7.5 \end{aligned}$ | $\begin{aligned} & 60 \\ & 11 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Sink Saturation ( $\mathrm{I}_{\text {Sink }}=2.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {OL }}$ | - | 0.13 | 0.4 | V |
| Output Off-State Leakage ( $\mathrm{V}_{\mathrm{OH}}=40 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{OH}}$ | - | - | 4.0 | $\mu \mathrm{A}$ |

UNCOMMITTED COMPARATOR

| Input Offset Voltage (Output Transition Low to High) | $\mathrm{V}_{\mathrm{IO}}$ | - | - | 20 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Hysteresis Voltage (Output Transition High to Low) | $\mathrm{I}_{\mathrm{H}}$ | 140 | 200 | 260 | mV |
| Input Bias Current (Vin 1, 2 $=2.6 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{IB}}$ | - | - | -1.0 | $\mu \mathrm{~A}$ |
| Input Common Mode Voltage Range | $\mathrm{V}_{\mathrm{ICR}}$ | 0.6 to 5.0 | - | - | V |
| Output Sink Saturation ( $\mathrm{I}_{\text {Sink }}=2.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{OL}}$ | - | 0.13 | 0.4 | V |
| Output Off-State Leakage $\left(\mathrm{V}_{\mathrm{OH}}=40 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{OH}}$ | - | - | 4.0 | $\mu \mathrm{~A}$ |

TOTAL DEVICE

| Chip Disable Threshold Voltage (Pin 15) High State (Chip Disabled) Low State (Chip Enabled) | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | $2.5$ |  | $\overline{0.8}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Chip Disable Input Current (Pin 15) High State $\left(\mathrm{V}_{\text {in }}=2.5 \mathrm{~V}\right)$ Low State ( $\mathrm{V}_{\text {in }}=0.8 \mathrm{~V}$ ) | $\begin{aligned} & I_{I H} \\ & I_{I L} \end{aligned}$ |  |  | $\begin{gathered} 100 \\ 30 \end{gathered}$ | $\mu \mathrm{A}$ |
| Chip Disable Input Resistance (Pin 15) | $\mathrm{R}_{\text {in }}$ | 50 | 100 | - | k $\Omega$ |
| Operating Voltage Range <br> $\mathrm{V}_{\mathrm{O}}$ (Pin 11) Regulated <br> $\mathrm{V}_{\text {ref }}$ (Pin 16) Regulated | $\mathrm{V}_{\mathrm{CC}}$ | $\begin{aligned} & 7.0 \text { to } 40 \\ & 5.0 \text { to } 40 \end{aligned}$ |  |  | V |
| Power Supply Current Standby (Chip Disable High State) Operating (Chip Disable Low State) | $\mathrm{I}_{\mathrm{Cc}}$ | - | $\begin{gathered} 0.18 \\ 1.5 \end{gathered}$ | $\begin{gathered} 0.35 \\ 3.0 \end{gathered}$ | mA |

NOTES: 1. The maximum voltage range is -0.3 V to $\mathrm{V}_{\mathrm{CC}}$ or +35 V , whichever is less.
2. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34160 $\quad \mathrm{T}_{\text {high }}=70^{\circ} \mathrm{C}$ for MC34160
$-40^{\circ} \mathrm{C}$ for MC33160 $\quad 85^{\circ} \mathrm{C}$ for MC33160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.


Figure 1. Regulator Output Voltage Change versus Source Current


Figure 2. Reference and Regulator Output versus Supply Voltage


Figure 3. Reference Output Voltage Change versus Source Current


Figure 5. Power Warning Comparator Delay versus Temperature


Figure 7. Comparator Output Saturation versus Sink Current


Figure 4. Power Warning Hysteresis Current versus Programming Resistor


Figure 6. Uncommitted Comparator Delay versus Temperature


Figure 8. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dlssipation versus P.C.B. Copper Length


Figure 9. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

PIN FUNCTION DESCRIPTION

| Pin | Function | Description |
| :---: | :--- | :--- |
| 1 | Comparator Inverting Input | This is the Uncommitted Comparator Inverting input. It is typically connected to a <br> resistor divider to monitor a voltage. |
| 2 | Comparator Noninverting Input | This is the Uncommitted Comparator Noninverting input. It is typically connected to a <br> reference voltage. |
| 3 | N.C. | No connection. This pin is not internally connected. |
| $4,5,12,13$ | Gnd | These pins are the control circuit grounds and are connected to the source and load <br> ground returns. They are part of the IC lead frame and can be used for heatsinking. |
| 6 | Comparator Output | This is the Uncommitted Comparator output. It is an open collector sink-only output <br> requiring a pull-up resistor. |
| 7 | Reset | This is the Reset Comparator output. It is an open collector sink-only output requiring <br> a pull-up resistor. |
| 8 | Power Warning | This is the Power Warning Comparator output. It is an open collector sink-only output <br> requiring a pull-up resistor. |
| 10 | Hysteresis Adjust | This is the Power Warning Comparator noninverting input. It is typically connected to a <br> resistor divider to monitor the input power source voltage. |
| 11 | Regulator Output | The Power Warning Comparator hysteresis is programmed by a resistor connected <br> from this pin to ground. |
| 14 | VCC | This is the 5.0 V Regulator output. |
| 15 | Chip Disable | This pin is the positive supply input of the control IC. |
| 16 | Vref | This input is used to switch the IC into a standby mode turning off all outputs. |
| 16 | This is the 2.6 V Reference output. It is intended to be used in conjunction with the <br> Power Warning and Uncommitted comparators. |  |

The MC34160 series is a monolithic voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These devices are specified for operation over an input voltage of 7.0 V to 40 V , and with a junction temperature of $-40^{\circ}$ to $+150^{\circ} \mathrm{C}$. A typical microprocessor application is shown in Figure 10.

## Regulator

The 5.0 V regulator is designed to source in excess of 100 mA output current and is short circuit protected. The output has a guaranteed tolerance of $\pm 5.0 \%$ over line, load, and temperature. Internal thermal shutdown circuitry is included to limit the maximum junction temperature to a safe level. When activated, typically at $170^{\circ} \mathrm{C}$, the regulator output turns off.

In specific situations a combination of input and output bypass capacitors may be required for regulator stability. If the regulator is located an appreciable distance ( $\geq 4^{\prime \prime}$ ) from the supply filter, an input bypass capacitor ( $\mathrm{C}_{\mathrm{in}}$ ) of $0.33 \mu \mathrm{~F}$ or greater is suggested. Output capacitance values of less than 5.0 nF may cause regulator instability at light load ( $\leq$ 1.0 mA ) and cold temperature. An output bypass capacitor of $0.1 \mu \mathrm{~F}$ or greater is recommended to ensure stability under all load conditions. The capacitors selected must provide good high frequency characteristics.

Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator does not have external sense inputs.

## Reference

The 2.6 V bandgap reference is short circuit protected and has a guaranteed output tolerance of $\pm 5.0 \%$ over line, load, and temperature. It is intended to be used in conjunction with the Power Warning and Uncommitted comparator. The reference can source in excess of 2.0 mA and sink a maximum of $10 \mu \mathrm{~A}$. For additional current sinking capability, an external load resistor to ground must be used.

Reference biasing is internally derived from either $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{O}}$, allowing proper operation if either drops below nominal.

## Chip Disable

This input is used to switch the IC into a standby mode. When activated, internal biasing for the entire die is removed causing all outputs to turn off. This reduces the power supply current $\left(\mathrm{I}_{\mathrm{CC}}\right)$ to less than 0.3 mA .

## Comparators

Three separate comparators are incorporated for voltage monitoring. Their outputs can provide diagnostic
information to the microprocessor, preventing system malfunctions.
The Reset Comparator Inverting Input is internally connected to the 2.6 V reference while the Noninverting Input monitors $\mathrm{V}_{\mathrm{O}}$. The $\overline{\text { Reset }}$ Output is active low when $\mathrm{V}_{\mathrm{O}}$ falls approximately 180 mV below its regulated voltage. To prevent erratic operation when crossing the comparator threshold, 70 mV of hysteresis is provided.
The Power Warning Comparator is typically used to detect an impending loss of system power. The Inverting Input is internally connected to the reference, fixing the threshold at 2.6 V . The input power source $\mathrm{V}_{\text {in }}$ is monitored by the Noninverting Input through the $\mathrm{R}_{1} / \mathrm{R}_{2}$ divider (Figure 10). This input features an adjustable $10 \mu \mathrm{~A}$ to 50 $\mu \mathrm{A}$ current $\operatorname{sink} \mathrm{I}_{\mathrm{H}}$ that is programmed by the value selected for resistor $\mathrm{R}_{\mathrm{H}}$. A default current of $6.5 \mu \mathrm{~A}$ is provided if $\mathrm{R}_{\mathrm{H}}$ is omitted. When the comparator input falls below 2.6 V , the current sink is activated. This produces hysteresis if $\mathrm{V}_{\text {in }}$ is monitored through a series resistor $\left(\mathrm{R}_{1}\right)$. The comparator thresholds are defined as follows:

$$
\begin{aligned}
& \mathrm{V}_{\text {th }(\text { lower })}=\mathrm{V}_{\text {ref }} \quad\left(1+\frac{\mathrm{R} 1}{\mathrm{R}_{2}}\right)-\mathrm{I}_{\mathrm{IB}} \mathrm{R}_{1} \\
& \mathrm{~V}_{\text {th }(\text { upper) }}=\mathrm{V}_{\text {ref }} \\
& \left(1+\frac{\mathrm{R} 1}{\mathrm{R}_{2}}\right)+\mathrm{I}_{\mathrm{H}} \mathrm{R}_{1}
\end{aligned}
$$

The nominal hysteresis current $\mathrm{I}_{\mathrm{H}}$ equals $1.2 \mathrm{~V} / \mathrm{R}_{\mathrm{H}}$ (Figure 4).

The Uncommitted Comparator can be used to synchronize the microprocessor with the ac line signal for timing functions, or for synchronous load switching. It can also be connected as a line loss detector as shown in Figure 11. The comparator contains 200 mV of hysteresis preventing erratic output behavior when crossing the input threshold.

The Power Warning and Uncommitted Comparators each have a transistor base-emitter connected across their inputs. The base input normally connects to a voltage reference while the emitter input connects to the voltage to be monitored. The transistor limits the negative excursion on the emitter input to -0.7 V below the base input by supply current from $\mathrm{V}_{\mathrm{CC}}$. This clamp current will prevent forward biasing the IC substrate. Zener diodes are connected to the comparator inputs to enhance the ICs electrostatic discharge capability. Resistors $R_{1}$ and $R_{\text {in }}$ must limit the input current to a maximum of $\pm 2.0 \mathrm{~mA}$.

Each comparator output consists of an open collector NPN transistor capable of sinking 2.0 mA with a saturation voltage less than 0.4 V , and standing off 40 V with minimal leakage. Internal bias for the Reset and Power Warning Comparators is derived from either $\mathrm{V}_{\mathrm{CC}}$ or the regulator output to ensure functionality when either is below nominal.

## Heat Tab Package

The MC34160 is contained in a 16 lead plastic dual-in-line package in which the die is mounted on a special Heat Tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the surrounding air. The pictorial in Figure 8 shows a simple but effective method of utilizing the printed circuit board
medium as a heat dissipator by soldering these tabs to an adequate area of copper foil. This permits the use of standard board layout and mounting practices while having the ability to more than halve the junction to air thermal resistance. The example and graph are for a symmetrical layout on a single sided board with one ounce per square foot copper.


Figure 10. Typical Microprocessor Application


Figure 11. Line Loss Detector Application


Figure 12. Time Delayed Microprocessor Reset

## CS8271

## Adjustable Micropower Low Dropout Linear Regulator with ENABLE

The CS8271 is an adjustable micropower voltage regulator with very low quiescent current ( $60 \mu \mathrm{~A}$ typical at $100 \mu \mathrm{~A}$ load). The output supplies 100 mA of load current with a maximum dropout voltage of only 600 mV . Control logic includes ENABLE. The combination of low quiescent current, outstanding regulator performance and control logic makes the CS8271 ideal for any battery operated equipment.

The logic level ENABLE compatible pin allows the user to put the regulator into a shutdown mode where it draws only $50 \mu \mathrm{~A}$ of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and over temperature conditions. The device can withstand 60 V load dump transients making it suitable for use in automotive environments.

The CS8271 is pin compatible with the National Semiconductor LM2931.

## Features

- Low Quiescent Current
- Adjustable Output: 5.0 V to 12 V
- ENABLE for Sleep Mode Control
- 100 mA Output Current Capability
- Fault Protection
- +60 V Load Dump
-     - 15 V Reverse Voltage Short Circuit
- Thermal Shutdown
- Low Reverse Current (Output to Input)

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http://onsemi.com
SO-8
D SUFFIX
CASE 751

## PIN CONNECTIONS AND MARKING DIAGRAM



$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8271YD8 | SO-8 | 95 Units/Rail |
| CS8271YDR8 | SO-8 | 2500 Tape \& Reel |
| CS8271YN8 | DIP-8 | 50 Units/Rail |

*Consult your local sales representative for other package options.


Figure 1. Block Diagram

MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| Power Dissipation | Internally Limited | - |
| Peak Transient Voltage (46 V Load Dump @ V ${ }_{\text {IN }}=14 \mathrm{~V}$ ) | -50, 60 | V |
| Reverse Battery | -15 | V |
| Output Current | Internally Limited | - |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| Junction Temperature | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: <br> Wave Solder (through hole styles only) (Note 1) <br> Reflow (SMD styles only) (Note 2) | 260 peak 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |
| Adj, ENABLE | -0.3, 10 | V |
| $\mathrm{V}_{\text {OUT }}$ | -0.3, 20 | V |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 30 \mathrm{~V}, 5.0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 12 \mathrm{~V}$, I $\mathrm{I}_{\text {OUT }}=10 \mathrm{~mA}$,
$-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, \mathrm{V}_{\text {ENABLE }}=0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage |  |  |  |  |  |
| Dropout Voltage | $\begin{aligned} & \text { lout }=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {DROP }}=\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \\ & \text { lout }=100 \mathrm{~mA}, \mathrm{~V}_{\text {DROP }}=\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \end{aligned}$ | - | $\begin{aligned} & 100 \\ & 400 \end{aligned}$ | $\begin{aligned} & 150 \\ & 600 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | Measure $\mathrm{V}_{\text {OUT }}$ when $\mathrm{I}_{\text {OUT }}=100 \mu \mathrm{~A}, 100 \mathrm{~mA}$. $L_{\text {REG }}=A B S\left(\Delta V_{\text {OUT }}\right)$ | - | 0.1 | 1.0 | \% $\mathrm{V}_{\text {OUT }}$ |
| Line Regulation | lout $=1.0 \mathrm{~mA}$. Measure $\mathrm{V}_{\text {OUT }}$ when $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {OUT }}+1.0 \mathrm{~V}, 30 \mathrm{~V}$, $\mathrm{LN}_{\text {REG }}=\mathrm{ABS}\left(\Delta \mathrm{V}_{\text {OUT }}\right)$ | - | 0.1 | 0.5 | \% $\mathrm{V}_{\text {OUT }}$ |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) Active Mode | $\begin{aligned} & \mathrm{V}_{\text {IN }}=6.0 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {OUT }} \text { setup for } 5.0 \mathrm{~V}, \\ & \mathrm{I}_{\mathrm{Q}}=\mathrm{IV}_{\text {IN }}-\mathrm{I}_{\text {OUT }} \\ & \mathrm{V}_{\text {IN }}=13 \mathrm{~V}, I_{\text {OUT }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {OUT }} \text { setup for } 12 \mathrm{~V}, \\ & I_{\mathrm{Q}}=\mathrm{IV}_{\text {IN }}-100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}=30 \mathrm{~V}, I_{\text {OUT }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {OUT }} \text { setup for } 5.0 \mathrm{~V} . \\ & I_{\mathrm{Q}}=\mathrm{IV}_{\text {IN }}-100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}=30 \mathrm{~V}, I_{\text {OUT }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {OUT }} \text { setup for } 12 \mathrm{~V} . \\ & \mathrm{I}_{\mathrm{Q}}=\mathrm{IV}_{\text {IN }}-100 \mu \mathrm{~A} \\ & \mathrm{I}_{\text {OUT }}=50 \mathrm{~mA}, I_{\mathrm{Q}}=\mathrm{IV}_{\text {IN }}-50 \mathrm{~mA} \\ & \mathrm{I}_{\text {OUT }}=100 \mathrm{~mA}, I_{\mathrm{Q}}=\mathrm{IV}_{\text {IN }}-100 \mathrm{~mA} \end{aligned}$ |  | $\begin{gathered} 55 \\ 130 \\ 150 \\ 20 \\ 4.0 \\ 12 \end{gathered}$ | 120 <br> 200 <br> 450 <br> 500 <br> 7.0 <br> 21 | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> mA <br> mA |
| Quiescent Current, ( $\mathrm{l}_{\mathrm{Q}}$ ) Sleep Mode | $\begin{aligned} & \mathrm{V}_{\mathbb{I N}}=6.0 \mathrm{~V}, \overline{\text { ENABLE }}=2.5 \mathrm{~V}, \mathrm{I}_{\text {QSLEEP }}=\mathrm{I} \mathrm{~V}_{\mathrm{IN}} \\ & \mathrm{~V}_{\mathrm{IN}}=30 \mathrm{~V}, \text { ENABLE }=2.5 \mathrm{~V}, \mathrm{I}_{\text {QSLEEP }}=\mathrm{IV}_{\mathrm{IN}} \end{aligned}$ | - | $\begin{aligned} & 20 \\ & 75 \end{aligned}$ | $\begin{gathered} 50 \\ 350 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Ripple Rejection | $f=120 \mathrm{~Hz}$, Note 3 | 60 | 75 | - | dB |
| Current Limit | $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {OUT }}-500 \mathrm{mV}$, $\mathrm{I}_{\text {LIM }}=\mathrm{IV}_{\text {OUT }}$ | 105 | 200 | 300 | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$, $\mathrm{I}_{\text {SHRT }}=\mathrm{IV}_{\text {OUT }}$ | 15 | 100 | 215 | mA |
| Thermal Limit | Note 3 | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Overvoltage Shutdown | Adjust $\mathrm{V}_{\text {IN }}$ from 28 V to 40 V until $\mathrm{V}_{\text {OUT }} \leq 1.0 \mathrm{~V}$ | 30 | 34 | 38 | V |
| Reverse Current | $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}, \mathrm{I}_{\text {REV }}=\mathrm{IV}_{\text {OUT }}, \mathrm{V}_{\text {OUT }}=13.2 \mathrm{~V}$ | - | 100 | 200 | $\mu \mathrm{A}$ |

## ENABLE

| Enable Threshold |  | - | 1.15 | 2.0 | 2.6 | V |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Enable Input Current | $V_{\overline{\text { ENABLE }}}=2.6 \mathrm{~V}$ | - | 10 | 20 | $\mu \mathrm{~A}$ |  |
|  | $\mathrm{~V}_{\mathrm{ENABLE}}=5.0 \mathrm{~V}$ | - | 35 | 50 | $\mu \mathrm{~A}$ |  |

## Adjustment Pin <br> R1: Feedback resistor between $\mathrm{V}_{\text {OUT }}$ and Adjust, R2: Adjust resistor to ground.

| Reference Voltage | $100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 100 \mathrm{~mA}$ | 1.246 | 1.272 | 1.297 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Adjustment Pin Current | $\mathrm{I}_{\text {ADJ }}=\left(\mathrm{V}_{\text {REF }} / \mathrm{R} 2\right)-\left(\left(\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {REF }}\right) / \mathrm{R} 1\right)$ | - | 20 | 500 | nA |

3. Guaranteed by design, not $100 \%$ tested in production.

## PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD \# |  | LEAD SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| SO-8 | DIP-8 |  |  |
| 1 | 1 | V OUT | 100 mA output; adjustable from 5.0 V to 12 V . |
| 2 | 2 | GND | Ground. |
| 3, 6, 7 | 3,6,7 | NC | No connection. |
| 4 | 4 | Adj | Resistor divider from $\mathrm{V}_{\text {Out }}$ to Adj, sets output voltage. |
| 5 | 5 | ENABLE | Logic level switch, when High, regulator is in sleep mode. |
| 8 | 8 | $\mathrm{V}_{\mathrm{IN}}$ | Input voltage. |

## CIRCUIT DESCRIPTION

## OUTPUT VOLTAGE ADJUSTMENT

The output voltage of the CS8271 is adjustable to any value between 5.0 V and the maximum input voltage minus the dropout voltage. To adjust the output voltage, a pair of external resistors R1 and R2 are connected as shown in Figure 2.

The equation for the output voltage is

$$
V_{\text {OUT }}=V_{R E F} \times\left(\frac{R 1+R 2}{R 2}\right)+I_{A d j} \times R 1
$$

where $\mathrm{V}_{\text {REF }}$ is the typical reference voltage and $\mathrm{I}_{\text {Adj }}$ is the adjust pin bias current. This is usually 500 nA maximum.


Figure 2. Output Voltage Adjustment

## OUTPUT STAGE PROTECTION

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 3).

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients up to 60 V in magnitude.

Short circuit protection limits the amount of current the output transistor can supply. In the case of a CS8271 under a short circuit condition, the output transistor current is limited to 100 mA .
Should the junction temperature of the power device exceed $180^{\circ} \mathrm{C}$ (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.


Figure 3. Typical Circuit Waveforms for Output Stage Protection

## ENABLE

The ENABLE function switches the output transistor. When the voltage on the $\overline{\text { ENABLE }}$ pin exceeds 2.0 V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only $20 \mu \mathrm{~A}$ (typ), until the voltage on this input drops below the ENABLE threshold.

## APPLICATION NOTES

## SELECTING THE RIGHT CAPACITOR VALUE

The output compensation capacitor COUT, determines three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The selection of a capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provide this information.

The value for the output compensation capacitor COUT shown in Figure 4 should work for most applications, but it is not necessarily the least expensive or the optimal solution.


Figure 4. Test and Application Circuit Showing An Output Compensation Capacitor

To determine an acceptable value for $\mathrm{C}_{\text {OUT }}$ for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. (Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible).

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.
Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.
Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.
Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.
Capacitance on the Adjust pin combined with the feedback resistors R1 and R2 can affect loop stability and should also be considered. The CS8271 internal circuitry produces about 5.0 pF to Ground on the Adjust pin. This capacitance, plus any additional external capacitance on the Adjust pin will create a pole when combined with the resistive feedback network. The effect can be significant when using large values for the feedback resistors to minimize quiescent current.
A capacitor connected from the Adjust pin to Ground provides additional means to compensate the regulator by creating a pole. Alternately, a capacitor can be connected from the Adjust pin to V VUT to create a zero.

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 5) is:

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT (min) }}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with
$\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 5. Single Output Regulator With Key Performance Parameters Labeled


Figure 6. Application Diagram

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | DIP-8 | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 45 | 52 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 165 | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8183

## Dual Micropower 200 mA Low Dropout Tracking Regulator/Line Driver

The CS8183 is a dual low dropout tracking regulator designed to provide adjustable buffered output voltages that closely track $( \pm 10 \mathrm{mV})$ the reference inputs. The outputs deliver up to 200 mA while being able to be configured higher, lower or equal to the reference voltages.

The outputs have been designed to operate over a wide range ( 2.8 V to 45 V ) while still maintaining excellent DC characteristics. The CS8183 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45 V load dump transients and -50 V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The $\mathrm{V}_{\text {REF }} / E N A B L E$ leads serve two purposes. They are used to provide the input voltage as a reference for the output and they also can be pulled low to place the device in sleep mode where it nominally draws less than $30 \mu \mathrm{~A}$ from the supply.

## Features

- Two Regulated Outputs $200 \mathrm{~mA}, \pm 10 \mathrm{mV}$ Track Worst Case
- Low Dropout (0.35 V typ. @ 200 mA )
- Low Quiescent Current
- Independent Thermal Shutdown
- Short Circuit Protection
- Wide Operating Range
- Internally Fused Leads in the SO-20L Package

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SO-20L
DWF SUFFIX CASE 751D

PIN CONNECTIONS AND MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS8183YDWF20 | SO-20L | 37 Units/Rail |
| CS8183YDWFR20 | SO-20L | 1000 Tape \& Reel |



Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Storage Temperature |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Supply Voltage Range (continuous) |  | 15 to 45 | V |
| Supply Voltage Range (normal, continuous) |  | 3.4 to 45 | V |
| Peak Transient Voltage ( $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}$, Load Dump Transient $=31 \mathrm{~V}$ ) |  | 45 | V |
| Voltage Range (Adj, $\mathrm{V}_{\text {REF }} / \mathrm{ENABLE}$, $\mathrm{V}_{\text {OUT }}$ ) |  | -10 to 45 | V |
| Maximum Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance: <br> Junction-to-Case, R 日JC <br> Junction-to-Ambient, R ®JA |  | $\begin{aligned} & 18 \\ & 73 \end{aligned}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ESD Capability (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$; $\mathrm{V}_{\text {REF }} /$ ENABLE $>2.75 \mathrm{~V} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq+125^{\circ} \mathrm{C}$; $\mathrm{C}_{\mathrm{OUT}} \geq 10 \mu \mathrm{~F}$; $0.1 \Omega<$ Cout - ESR $^{2} 1.0 \Omega$ @ 10 kHz ; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Regular Output 1, 2

| $V_{\text {REF }}$ - $V_{\text {OUT }}$ <br> V Out Tracking Error | $4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 200 \mathrm{~mA}$, Note 2 | -10 | - | 10 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\begin{aligned} & \text { lout }=100 \mu \mathrm{~A} \\ & \text { lout }=200 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 100 \\ & 350 \end{aligned}$ | $\begin{aligned} & 150 \\ & 600 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Line Regulation | $4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, Note 2 | - | - | 10 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 200 \mathrm{~mA}$, Note 2 | - | - | 10 | mV |
| Adj Lead Current | Loop in Regulation | - | 0.2 | 1.0 | $\mu \mathrm{A}$ |
| Current Limit | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, \mathrm{~V}_{\text {REF }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=90 \%$ of $\mathrm{V}_{\text {REF }}$, Note 2 | 225 | - | 700 | mA |
| Quiescent Current (lin - Iout) | $\begin{aligned} & \mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=200 \mathrm{~mA} \\ & \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {REF }} / \mathrm{ENABLE}=0 \mathrm{~V} \end{aligned}$ | - | $\begin{aligned} & 15 \\ & 75 \\ & 30 \end{aligned}$ | $\begin{gathered} 25 \\ 150 \\ 55 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Reverse Current | $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 0.2 | 1.5 | mA |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$, IOUT $=200 \mathrm{~mA}, 4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | 60 | - | - | dB |
| Thermal Shutdown | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |

$V_{\text {REF/FNABLE 1, }} 2$

| Enable Voltage | - | 0.80 | 2.00 | 2.75 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | $\mathrm{V}_{\text {REF }} / \mathrm{ENABLE} 1,2>2.0 \mathrm{~V}$ | - | 0.2 | 1.0 | $\mu \mathrm{A}$ |

2. V OUT connected to Adj lead.

## PACKAGE PIN DESCRIPTION

| Package Lead Number |  |  |
| :---: | :---: | :---: |
| SO-20L | Lead Symbol | Function |
| 1 | $\mathrm{V}_{\text {IN } 1}$ | Input voltage for $\mathrm{V}_{\text {OUT1 }}$. |
| 2 | $\mathrm{V}_{\text {OUT1 }}$ | Regulated output voltage 1. |
| $3,4,7,8,13,14,17,18$ | NC | No connection. |
| 5, 6, 15, 16 | GND | Ground (4 leads fused) |
| 9 | $V_{\text {ADJ1 }}$ | Adjust lead for $\mathrm{V}_{\text {Out1 }}$. |
| 10 | $\mathrm{V}_{\text {REF }}$ /ENABLE1 | Reference voltage and ENABLE input for $\mathrm{V}_{\text {OUT1 }}$. |
| 11 | $\mathrm{V}_{\text {ADJ2 }}$ | Adjust lead for $\mathrm{V}_{\text {Out2 }}$. |
| 12 | $\mathrm{V}_{\text {REF/ } / E N A B L E 2 ~}$ | Reference voltage and ENABLE input for $\mathrm{V}_{\text {OUT2 }}$. |
| 19 | $\mathrm{V}_{\text {IN2 }}$ | Input voltage for $\mathrm{V}_{\text {OUT2 }}$. |
| 20 | $\mathrm{V}_{\text {OUT2 }}$ | Regulated output voltage 2. |

## CIRCUIT DESCRIPTION

## ENABLE Function

By pulling the $\mathrm{V}_{\mathrm{REF}} /$ ENABLE 1, 2 lead below 2.0 V typically, (see Figure 5 or Figure 6), the IC is disabled and enters a sleep state where the device draws less than $30 \mu \mathrm{~A}$ from supply. When the $\mathrm{V}_{\mathrm{REF}} /$ ENABLE lead is greater than $2.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}$ tracks the $\mathrm{V}_{\mathrm{REF}} / \mathrm{ENABLE}$ lead normally.

## Output Voltage

Figures 2 through 7 only display one channel of the device for simplicity. The configurations shown apply for both channels.


$$
\text { VOUT }=V_{\text {REF }}
$$

Figure 2. Tracking Regulator at the Same Voltage


Figure 4. Tracking Regulator at Lower Voltages


Figure 6. Alternative ENABLE Circuit

[^14]The outputs are capable of supplying 200 mA to the load while configured as a similiar (Figure 2), lower (Figure 4), or higher (Figure 3) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the $\mathrm{V}_{\text {REF }}$ lead as the non-inverting.

The device can also be configured as a high-side driver as displayed in Figure 7.


Figure 3. Tracking Regulator at Higher Voltages


Figure 5. Tracking Regulator with ENABLE Circuit


Figure 7. High-Side Driver

## APPLICATION NOTES

## Switched Application

The CS8183 has been designed for use in systems where the reference voltage on the $\mathrm{V}_{\text {REF }} /$ /ENABLE pin is continuously on. Typically, the current into the $\mathrm{V}_{\text {REF/ }}$ /ENABLE pin will be less than $1.0 \mu \mathrm{~A}$ when the voltage on the $\mathrm{V}_{\text {IN }}$ pin (usually the ignition line) has been switched out ( $\mathrm{V}_{\text {IN }}$ can be at high impedance or at ground.) Reference Figure 8.


Figure 8.

## External Capacitors

Output capacitors for the CS8183 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

The output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to $-40^{\circ} \mathrm{C}$, a capacitor rated at that temperature must be used.
More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators."

## Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 9) is:

$$
\begin{align*}
\mathrm{PD}(\max )= & \left\{\mathrm{V}_{\mathrm{IN}}(\max )-\mathrm{V}_{\text {OUT1 }}(\min )\right\} \operatorname{IOUT1}(\max ) \\
& +\left\{\mathrm{V}_{\mathrm{IN}}(\max )-\mathrm{V}_{\text {OUT2 }}(\min )\right\} \operatorname{IOUT2}(\max 2) \\
& +\mathrm{V}_{\mathrm{IN}}(\max ) \mathrm{I} \mathrm{Q} \tag{1}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\text { max })}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$V_{\text {OUT2(min) }}$ is the minimum output voltage from $V_{\text {OUT2 }}$, Iout1(max) is the maximum output current, for the application,
IOUT2(max) is the maximum output current, for the application,
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).
Once the value of $\mathrm{PD}(\max )$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
R_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\text {©JA's }}$ less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.


Figure 9. Dual Output Regulator with Key Performance Parameters Labeled

## Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.
Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \mathrm{JA}}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©IC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta \mathrm{SA}}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\text {©JC }}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## CS8363

### 3.3 V Dual Micropower Low Dropout Regulator with ENABLE and RESET

The CS8363 is a precision micropower dual voltage regulator with $\overline{\text { ENABLE }}$ and $\overline{\text { RESET. }}$

The 3.3 V standby output is accurate within $\pm 2 \%$ while supplying loads of 100 mA . Quiescent current is low, typically $140 \mu \mathrm{~A}$ with a $300 \mu \mathrm{~A}$ load. The active $\overline{\mathrm{RESET}}$ output monitors the 3.3 V standby output and is low during power-up and regulator dropout conditions. The $\overline{\text { RESET }}$ circuit includes hysteresis and is guaranteed to operate correctly with 1.0 V on the standby output.

The second output tracks the 3.3 V standby output through an external adjust lead, and can supply loads of 250 mA with a typical dropout voltage of 400 mV . The logic level lead ENABLE is used to control this tracking regulator output.

Both outputs are protected against overvoltage, short circuit, reverse battery and overtemperature conditions. The robustness and low quiescent current of the CS8363 makes it not only well suited for automotive microprocessor applications, but for any battery powered microprocessor applications.

## Features

- 2 Regulated Outputs
- Standby Output 3.3 V $\pm 2 \%$; 100 mA
- Adjustable Tracking Output; 250 mA
- Low Dropout Voltage
- RESET for $V_{\text {STBY }}$
- ENABLE for VTRK
- Low Quiescent Current
- Protection Features
- Independent Thermal Shutdown
- Short Circuit
- 60 V Load Dump
- Reverse Battery

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http://onsemi.com


D2PAK 7-PIN DPS SUFFIX CASE 936H

Pin 1. $V_{\text {StBy }}$
2. $\mathrm{V}_{\mathrm{IN}}$
3. $\mathrm{V}_{\text {TRK }}$
4. GND
5. Adj
6. ENABLE
7. RESET

MARKING DIAGRAM


ORDERING INFORMATION*

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS8363YDPS7 | D²PAK, 7-PIN | 50 Units/Rail |
| CS8363YDPSR7 | D2PAK, 7-PIN | 750 Tape \& Reel |

*Contact your local sales representative for SO-16L package option.


Figure 1. Block Diagram. Consult Your Local Sales Representative for Positive ENABLE Option

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\mathrm{IN}}$ | -16 to 26 | V |
| Positive Transient Input Voltage, $\mathrm{tr}>1.0 \mathrm{~ms}$ | 60 | V |
| Negative Transient Invput Voltage, T < $100 \mathrm{~ms}, 1.0$ \% Duty Cycle | -50 | V |
| Input Voltage Range (ENABLE, RESET) | -0.3 to 10 | V |
| Junction Temperature | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| Lead Temperature Soldering <br> Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 peak 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, $\mathrm{I}_{\text {OUT } 1}=\mathrm{I}_{\mathrm{OUT} 2}=100 \mu \mathrm{~A},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$;
unless otherwise stated.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Tracking Output ( $\mathrm{V}_{\text {TRK }}$ ) |  |  |  |  |  |
| $\mathrm{V}_{\text {TRK }}$ Tracking Error ( $\mathrm{V}_{\text {STBY }}-\mathrm{V}_{\text {TRK }}$ ) | $\begin{aligned} & \text { 6.0 } \mathrm{V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {TRK }} \leq 250 \mathrm{~mA} \text {. } \\ & \text { Note } 3 \end{aligned}$ | -25 | - | +25 | mV |
| Adjust Pin Current, $\mathrm{I}_{\text {Adj }}$ | Loop in Regulation | - | 1.5 | 5.0 | $\mu \mathrm{A}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$. Note 3 | - | 5.0 | 50 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {TRK }} \leq 250 \mathrm{~mA}$. Note 3 | - | 5.0 | 50 | mV |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {TRK }}$ ) | $\begin{aligned} & I_{\text {TRK }}=100 \mu \mathrm{AA} . \\ & I_{\text {TRK }}=250 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 100 \\ & 400 \end{aligned}$ | $\begin{aligned} & 150 \\ & 700 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Current Limit | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {TRK }}=3.0 \mathrm{~V}$ | 275 | 500 | - | mA |
| Quiescent Current | $\begin{aligned} & \mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {TRK }}=250 \mathrm{~mA} \text {, No Load on } \mathrm{V}_{\text {STBY }} \\ & \mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {TRK }}=500 \mu \mathrm{~A}, \mathrm{I}_{\text {STBY }}=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{gathered} 25 \\ 145 \end{gathered}$ | $\begin{gathered} 50 \\ 220 \end{gathered}$ | $\begin{gathered} \mathrm{mA} \\ \mu \mathrm{~A} \end{gathered}$ |
| Reverse Current | $\mathrm{V}_{\text {TRK }}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V}$ | - | 200 | 1500 | $\mu \mathrm{A}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\text {TRK }}=250 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |

Standby Output ( $\mathrm{V}_{\text {STBY }}$ )

| Output Voltage, $\mathrm{V}_{\text {STBY }}$ | $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {STBY }} \leq 100 \mathrm{~mA}$. | 3.234 | 3.3 | 3.366 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$. | - | 5.0 | 50 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {STBY }} \leq 100 \mathrm{~mA}$. | - | 5.0 | 50 | mV |
| Dropout Voltage ( $\left.\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {STBY }}\right)$ | $\begin{aligned} & \mathrm{I}_{\text {STBY }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {IN }}=4.2 \mathrm{~V} \\ & \mathrm{I}_{\text {STBY }}=100 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=4.2 \mathrm{~V} \end{aligned}$ | - | - | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Current Limit | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {STBY }}=3.0 \mathrm{~V}$ | 125 | 200 | - | mA |
| Short Circuit Current | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {STBY }}=0 \mathrm{~V}$ | 10 | 100 | - | mA |
| Quiescent Current | $\begin{aligned} & \mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {STBY }}=100 \mathrm{~mA}, I_{\text {TRK }}=0 \mathrm{~mA} \\ & \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {STBY }}=300 \mu \mathrm{I}, \mathrm{I}_{\text {TRK }}=0 \mathrm{~mA} \end{aligned}$ | - | $\begin{gathered} 10 \\ 140 \end{gathered}$ | $\begin{gathered} 20 \\ 200 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Reverse Current | $\mathrm{V}_{\text {STBY }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 200 | $\mu \mathrm{A}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\text {STBY }}=100 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |

RESET ENABLE Functions

| ENABLE Input Threshold | - | 0.8 | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ENABLE Input Bias Current | $\mathrm{V}_{\text {ENABLE }}=0 \mathrm{~V}$ to 10 V | -10 | 0 | 10 | $\mu \mathrm{A}$ |
| RESET Hysteresis | - | 10 | 50 | 100 | mV |
| RESET Threshold Low ( $\mathrm{V}_{\mathrm{RL}}$ ) | $\mathrm{V}_{\text {STBY }}$ Decreasing, $\mathrm{V}_{\text {IN }}>4.5 \mathrm{~V}$ | 92.5 | 95 | 97.5 | \% $\mathrm{V}_{\text {STBY }}$ |
| RESET Leakage | - | - | - | 25 | $\mu \mathrm{A}$ |
| Output Voltage, Low (V $\mathrm{V}_{\text {RLO }}$ ) | $1.0 \mathrm{~V} \leq \mathrm{V}_{\text {STBY }} \leq \mathrm{V}_{\mathrm{RL}}, \mathrm{R}_{\mathrm{RST}}=10 \mathrm{k} \Omega$ | - | 0.1 | 0.4 | V |
| Output Voltage, Low (V ${ }_{\text {RPEAK }}$ ) | $\mathrm{V}_{\text {StBY }}$, Power Up, Power Down | - | 0.6 | 1.0 | V |
| $\mathrm{V}_{\text {IN }}\left(\mathrm{V}_{\text {RST }}\right.$ Low) | $\mathrm{V}_{\text {STBY }}=3.3 \mathrm{~V}$ | - | 4.0 | 4.5 | V |

Protection Circuitry (Both Outputs)

| Independent Thermal Shutdown | $V_{\text {STBY }}$ <br> $V_{\text {TRK }}$ | 150 <br> 150 | 180 <br> 165 | - <br> - | ${ }^{\circ} \mathrm{C}$ <br> ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Overvoltage Shutdown |  | 30 | 34 | 38 | V |

3. $\mathrm{V}_{\text {TRK }}$ connected to Adj lead. $\mathrm{V}_{\text {TRK }}$ can be set to higher values by using an external resistor divider.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| D2PAK | PIN SYMBOL |  |
| 1 | $\mathrm{~V}_{\text {STBY }}$ | FUNCTION |

## CIRCUIT DESCRIPTION

## ENABLE Function

The ENABLE function switches the output transistor for $V_{\text {TRK }}$ on and off. When the ENABLE lead voltage exceeds 1.4 V (typ), $\mathrm{V}_{\text {TRK }}$ turns off. This input has several hundred millivolts of hysteresis to prevent spurious output activity during power-up or power-down.

## RESET Function

The $\overline{\text { RESET }}$ is an open collector NPN transistor, controlled by a low voltage detection circuit sensing the $\mathrm{V}_{\text {STBY }}(3.3 \mathrm{~V}$ ) output voltage. This circuit guarantees the RESET output stays below $1.0 \mathrm{~V}\left(0.1 \mathrm{~V}\right.$ typ) when $\mathrm{V}_{\text {STBY }}$ is as low as 1.0 V to ensure reliable operation of microprocessor-based systems.

## $V_{\text {TRK }}$ Output Voltage

This output uses the same type of output device as $\mathrm{V}_{\text {STBY }}$, but is rated for 250 mA . The output is configured as a tracking regulator of the standby output. By using the standby output as a voltage reference, giving the user an external programming lead (Adj lead), output voltages from 3.3 V to 20 V are easily realized. The programming is done with a simple resistor divider, and following the formula:

$$
V_{\mathrm{TRK}}=\mathrm{V}_{\mathrm{STBY}} \times(1+\mathrm{R} 1 / \mathrm{R} 2)+\mathrm{I}_{\mathrm{Adj}} \times \mathrm{R} 1
$$

If another 3.3 V output is needed, simply connect the Adj lead to the $\mathrm{V}_{\text {TRK }}$ output lead.


Figure 2. Test and Application Circuit, 3.3 V, 5.0 V Regulator

*C1 is required if regulator is located far from power supply filter.
${ }^{* *} \mathrm{C} 2$ and C3 are required for stability.
Figure 3. Test and Application Circuit, Dual 3.3 V Regulator

## APPLICATION NOTES

## External Capacitors

Output capacitors for the CS8363 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to $-40^{\circ} \mathrm{C}$, capacitors rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators," document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 4) is
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,

IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at both IOUT1(max) and IOUT2(max).
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\text {©JA }}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 4. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

## CS8363

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \mathrm{JA}}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE THERMAL DATA

| Parameter |  | D$^{2}$ PAK, 7-Pin | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 3.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {®JA }}$ | Typical | $10-50^{\star}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

${ }^{*}$ Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$.

## CS8361

### 5.0 V Dual Micropower Low Dropout Regulator with ENABLE and RESET

The CS8361 is a precision micropower dual voltage regulator with $\overline{\text { ENABLE }}$ and $\overline{\text { RESET. }}$

The 5.0 V standby output is accurate within $\pm 2 \%$ while supplying loads of 100 mA and has a typical dropout voltage of 400 mV . Quiescent current is low, typically $140 \mu \mathrm{~A}$ with a $300 \mu \mathrm{~A}$ load. The active RESET output monitors the 5.0 V standby output and is low during power-up and regulator dropout conditions. The $\overline{\text { RESET }}$ circuit includes hysteresis and is guaranteed to operate correctly with 1.0 V on the standby output.

The second output tracks the 5.0 V standby output through an external adjust lead, and can supply loads of 250 mA with a typical dropout voltage of 400 mV . The logic level $\overline{\text { ENABLE }}$ lead is used to control this tracking regulator output.

Both outputs are protected against overvoltage, short circuit, reverse battery and overtemperature conditions. The robustness and low quiescent current of the CS8361 makes it not only well suited for automotive microprocessor applications, but for any battery powered microprocessor applications.

## Features

- 2 Regulated Outputs
- Standby Output 5.0 V $\pm 2 \%$; 100 mA
- Tracking Output $5.0 \mathrm{~V} ; 250 \mathrm{~mA}$
- Low Dropout Voltage ( 0.4 V at Rated Current)
- RESET Option
- ENABLE Option
- Low Quiescent Current
- Protection Features
- Independent Thermal Shutdown
- Short Circuit
- 60 V Load Dump
- Reverse Battery
- Internally Fused Leads in SO-16L Package

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PIN CONNECTIONS AND
MARKING DIAGRAM


|  | Pin | 1. $\mathrm{V}_{\text {STBY }}$ |
| :---: | :---: | :---: |
|  |  | 2. $\mathrm{V}_{\text {IN }}$ |
|  |  | 3. $\mathrm{V}_{\text {TRK }}$ |
|  |  | 4. GND |
| \|||||| |  | 5. Adj |
| T |  | 6. ENABLE |
|  |  | 7. RESET |

A = Assembly Location
WL, L = Wafer Lot
YY, $Y$ = Year
WW, W = Work Week

## ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8361YDPS7 | D$^{2}$ PAK $\dagger$ | 50 Units/Rail |
| CS8361YDPSR7 | D $^{2}$ PAK $\dagger$ | 750 Tape \& Reel |
| CS8361YDWF16 | SO-16L | 46 Units/Rail |
| CS8361YDWFR16 | SO-16L | 1000 Tape \& Reel |

*Contact your local sales representative for other package options including PSOP-20, TO-220 Seven Lead, DIP-16, and SO-20L.
$\dagger 7-$ Pin.


Figure 1. Block Diagram. Consult Your Local Sales Representative for Positive ENABLE Option

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {IN }}$ | -16 to 26 | V |
| Positive Transient Input Voltage, tr > 1.0 ms | 60 | V |
| Negative Transient Invput Voltage, T < $100 \mathrm{~ms}, 1.0$ \% Duty Cycle | -50 | V |
| Input Voltage Range (ENABLE, RESET) | -0.3 to 10 | V |
| Tracking Regulator ( $\mathrm{V}_{\text {TRK }}$, Adj) | 20 | V |
| Junction Temperature | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| Lead Temperature Soldering <br> Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 peak 230 peak | ${ }^{\circ} \mathrm{C} \mathrm{C}$ |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, I IOUT1 $=\mathrm{I}_{\text {OUT2 }}=100 \mu \mathrm{~A},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}$; unless otherwise stated.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Tracking Output ( $\mathrm{V}_{\text {TRK }}$ ) |  |  |  |  |  |
| $\mathrm{V}_{\text {TRK }}$ Tracking Error ( $\mathrm{V}_{\text {STBY }}-\mathrm{V}_{\text {TRK }}$ ) | $\begin{aligned} & \text { 6.0 } \mathrm{V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {TRK }} \leq 250 \mathrm{~mA} . \\ & \text { Note } 3 \end{aligned}$ | -25 | - | +25 | mV |
| Adjust Pin Current, ${ }_{\text {Adj }}$ | Loop in Regulation | - | 1.5 | 5.0 | $\mu \mathrm{A}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$. Note 3 | - | 5.0 | 50 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {TRK }} \leq 250 \mathrm{~mA}$. Note 3 | - | 5.0 | 50 | mV |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {TRK }}$ ) | $\begin{aligned} & I_{\text {TRK }}=100 \mu \mathrm{~A} . \\ & \mathrm{I}_{\text {TRK }}=250 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 100 \\ & 400 \end{aligned}$ | $\begin{aligned} & 150 \\ & 700 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Current Limit | $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V}, \mathrm{~V}_{\text {TRK }}=4.5 \mathrm{~V}$ | 275 | 500 | - | mA |
| Quiescent Current | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {TRK }}=250 \mathrm{~mA}$, No Load on $\mathrm{V}_{\text {STBY }}$ | - | 25 | 50 | mA |
| Reverse Current | $\mathrm{V}_{\text {TRK }}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0 \mathrm{~V}$ | - | 200 | 1500 | $\mu \mathrm{A}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{l}_{\text {TRK }}=250 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |

Standby Output ( $\mathrm{V}_{\text {STBY }}$ )

| Output Voltage, $\mathrm{V}_{\text {STBY }}$ | $6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {STBY }} \leq 100 \mathrm{~mA}$. | 4.9 | 5.0 | 5.1 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$. | - | 5.0 | 50 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {STBY }} \leq 100 \mathrm{~mA}$. | - | 5.0 | 50 | mV |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {STBY }}$ ) | $\begin{aligned} & \mathrm{I}_{\text {STBY }}=100 \mu \mathrm{~A} . \\ & \mathrm{I}_{\text {STBY }}=100 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 100 \\ & 400 \end{aligned}$ | $\begin{aligned} & 150 \\ & 600 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Current Limit | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {STBY }}=4.5 \mathrm{~V}$ | 125 | 200 | - | mA |
| Short Circuit Current | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{~V}_{\text {STBY }}=0 \mathrm{~V}$ | 10 | 100 | - | mA |
| Quiescent Current | $\begin{aligned} & \mathrm{V}_{\text {IN }}=12 \mathrm{~V}, I_{\text {STBY }}=100 \mathrm{~mA}, I_{\text {TRK }}=0 \mathrm{~mA} \\ & \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, I_{\text {STBY }}=300 \mu \mathrm{I}, I_{\text {TRK }}=0 \mathrm{~mA} \end{aligned}$ | - | $\begin{gathered} 10 \\ 140 \end{gathered}$ | $\begin{gathered} 20 \\ 200 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Reverse Current | $\mathrm{V}_{\text {STBY }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 200 | $\mu \mathrm{A}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{I}_{\text {STBY }}=100 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |

RESET ENABLE Functions

| ENABLE Input Threshold | - | 0.8 | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ENABLE Input Bias Current | $\mathrm{V}_{\text {ENABLE }}=0 \mathrm{~V}$ to 10 V | -10 | 0 | 10 | $\mu \mathrm{A}$ |
| RESET Threshold High ( $\mathrm{V}_{\mathrm{RH}}$ ) | $\mathrm{V}_{\text {STBY }}$ Increasing | 4.59 | 4.87 | $\mathrm{V}_{\text {STBY }}-0.02$ | V |
| RESET Hysteresis | - | 60 | 120 | 180 | mV |
| RESET Threshold Low ( $\mathrm{V}_{\mathrm{RL}}$ ) | $\mathrm{V}_{\text {STBY }}$ Decreasing | 4.53 | 4.75 | $\mathrm{V}_{\text {STBY }}-0.08$ | V |
| RESET Leakage | - | - | - | 25 | $\mu \mathrm{A}$ |
| Output Voltage, Low (V $\mathrm{V}_{\text {LLO }}$ ) | $1.0 \mathrm{~V} \leq \mathrm{V}_{\text {STBY }} \leq \mathrm{V}_{\mathrm{RL}}, \mathrm{R}_{\mathrm{RST}}=10 \mathrm{k} \Omega$ | - | 0.1 | 0.4 | V |
| Output Voltage, Low (VRPEAK) | $\mathrm{V}_{\text {StBY }}$, Power Up, Power Down | - | 0.6 | 1.0 | V |

## Protection Circuitry (Both Outputs)

| Independent Thermal Shutdown | $V_{\text {STBY }}$ <br> $V_{\text {TRK }}$ | 150 <br> 150 | 180 <br> 165 | - <br> - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| ${ }^{\circ} \mathrm{C}$ |  |  |  |  |  |$|$

3. $\mathrm{V}_{\text {TRK }}$ connected to Adj lead. $\mathrm{V}_{\text {TRK }}$ can be set to higher values by using an external resistor divider.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| D2PAK, 7 Pin | SO-16L |  |  |
| 1 | 16 | $\mathrm{V}_{\text {STBY }}$ | Standby output voltage delivering 100 mA . |
| 2 | 1 | $\mathrm{V}_{\text {IN }}$ | Input voltage. |
| 3 | 3 | $\mathrm{V}_{\text {TRK }}$ | Tracking output voltage controlled by ENABLE delivering 250 mA . |
| 4 | 4, 5, 12, 13 | GND | Reference ground connection. |
| 5 | 6 | Adj | Resistor divider from $\mathrm{V}_{\text {TRK }}$ to Adj. Sets the output voltage on $\mathrm{V}_{\text {TRK }}$. If tied to $\mathrm{V}_{\text {TRK }}, \mathrm{V}_{\text {TRK }}$ will track $\mathrm{V}_{\text {STBY }}$. |
| 6 | 8 | ENABLE | Provides on/off control of the tracking output, active LOW. |
| 7 | 9 | RESET | CMOS compatible output lead that goes low whenever $\mathrm{V}_{\text {STBY }}$ falls out of regulation. |
|  | $\begin{gathered} 2,7,10,11 \\ 14,15 \end{gathered}$ | NC | No connection. |

## CIRCUIT DESCRIPTION

## ENABLE Function

The ENABLE function switches the output transistor for $\mathrm{V}_{\text {TRK }}$ on and off. When the ENABLE lead voltage exceeds 1.4 V (typ), $\mathrm{V}_{\text {TRK }}$ turns off. This input has several hundred millivolts of hysteresis to prevent spurious output activity during power-up or power-down.

## RESET Function

The RESET is an open collector NPN transistor, controlled by a low voltage detection circuit sensing the $\mathrm{V}_{\text {STBY }}(5.0 \mathrm{~V})$ output voltage. This circuit guarantees the RESET output stays below $1.0 \mathrm{~V}\left(0.1 \mathrm{~V}\right.$ typ) when $\mathrm{V}_{\text {STBY }}$ is as low as 1.0 V to ensure reliable operation of microprocessor- based systems.

## $\mathrm{V}_{\text {TRK }}$ Output Voltage

This output uses the same type of output device as $\mathrm{V}_{\mathrm{STBY}}$, but is rated for 250 mA . The output is configured as a tracking regulator of the standby output. By using the standby output as a voltage reference, giving the user an external programming lead (Adj lead), output voltages from 5.0 V to 20 V are easily realized. The programming is done with a simple resistor divider (Figure 2), and following the formula:

$$
V_{\text {TRK }}=V_{\text {STBY }} \times(1+\mathrm{R} 1 / R 2)+I_{\text {Adj }} \times R 1
$$

If another 5.0 V output is needed, simply connect the Adj lead to the $\mathrm{V}_{\text {TRK }}$ output lead.


Figure 2. Test and Application Circuit, 5.0 V, 8.0 V Regulator

*C1 is required if regulator is located far from power supply filter.
${ }^{* *} \mathrm{C} 2$ and C3 are required for stability.
Figure 3. Test and Application Circuit, Dual 5.0 V Regulator

## APPLICATION NOTES

## External Capacitors

Output capacitors for the CS8361 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to $-40^{\circ} \mathrm{C}$, capacitors rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators," document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 4) is
where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,

IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at both IOUT1(max) and IOUT2(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
R_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\text {©JA }}$ can be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 4. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

## CS8361

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \mathrm{JA}}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE THERMAL DATA

| Parameter |  | SO-16L | D$^{2}$ PAK, 7-Pin | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 18 | 3.5 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {®JA }}$ | Typical | 75 | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*Depending on thermal properties of substrate. $R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C A}$.

## CS8147

## 10 V/5.0 V Low Dropout Dual Regulator with ENABLE

The CS8147 is a $10 \mathrm{~V} / 5.0 \mathrm{~V}$ dual output linear regulator. The 10 V $\pm 5.0 \%$ output sources 500 mA and the $5.0 \mathrm{~V} \pm 3 \%$ output sources 70 mA . The secondary output is inherently stable and does not require an external capacitor.

The on board ENABLE function controls the regulator's two outputs. When ENABLE is high, the regulator is placed in SLEEP mode. Both outputs are disabled and the regulator draws only $70 \mu \mathrm{~A}$ of quiescent current.

The regulator is protected against overvoltage conditions. Both outputs are protected against short circuit and thermal runaway conditions.

The CS8147 is packaged in a 5 lead TO-220 with copper tab. The copper tab can be connected to a heat sink if necessary.

## Features

- Two Regulated Outputs
- $10 \mathrm{~V} \pm 5.0 \%$; 500 mA
$-5.0 \mathrm{~V} \pm 3.0 \%$; 70 mA
- $70 \mu \mathrm{~A}$ SLEEP Mode Current
- Inherently Stable Secondary Output (No Output Capacitor Required)
- Fault Protection
- Overvoltage Shutdown
- Reverse Battery
- 60 V Peak Transient
- -50 V Reverse Transient
- Short Circuit
- Thermal Shutdown
- CMOS Compatible ENABLE Input with Low (IOUT(max) Input Current
ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8147YT5 | TO-220* <br> STRAIGHT | 50 Units/Rail |
| CS8147YTVA5 | TO-220* <br> VERTICAL | 50 Units/Rail |
| CS8147YTHA5 | TO-220* <br> HORIZONTAL | 50 Units/Rail |

*Five lead.


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage: | DC Positive Peak Transient Voltage (Note 1) Negative Peak Transient Voltage | $\begin{gathered} -18 \text { to } 26 \\ 60 \\ -50 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| ESD (Human Body Model) |  | 2.0 | kV |
| ENABLE Input |  | -0.3 to 10 | V |
| Internal Power Dissipation |  | Internally Limited | - |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 2) | 260 peak | ${ }^{\circ} \mathrm{C}$ |

1. 46 V Load Dump @ $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$
2. 10 second maximum.
*The maximum package power dissipation must be observed.

## CS8147

ELECTRICAL CHARACTERISTICS for V OUT: $\left(\mathrm{V}_{\text {IN }}=14 \mathrm{~V}\right.$, $\mathrm{I}_{\text {OUT } 1}=I_{\text {OUT } 2}=5.0 \mathrm{~mA},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}$, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$, ENABLE $=$ LOW; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Primary Output (Vout1)

| Output Voltage | $13 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, \mathrm{l}_{\text {OUT } 1} \leq 500 \mathrm{~mA}$ | 9.50 | 10.00 | 10.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\mathrm{l}_{\text {OUT1 }}=500 \mathrm{~mA}$ | - | 0.5 | 0.7 | V |
| Line Regulation | $11 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 18 \mathrm{~V}$, lout $1=250 \mathrm{~mA}$ | - | 45 | 90 | mV |
| Load Regulation | $5.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1} \leq 500 \mathrm{~mA}$ | - | 15 | 75 | mV |
| Quiescent Current | $\mathrm{l}_{\text {OUT } 1} \leq 1.0 \mathrm{~mA}$, No Load on $\mathrm{V}_{\text {OUT2 }}, \mathrm{V}_{\text {IN }}=18 \mathrm{~V}$ $\mathrm{l}_{\text {OUT } 1}=500 \mathrm{~mA}$, No Load on $\mathrm{V}_{\text {OUT2 }}, \mathrm{V}_{\text {IN }}=11 \mathrm{~V}$ | - | $\begin{aligned} & 3.0 \\ & 60 \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 120 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Quiescent Current | ENABLE $=$ HIGH, $\mathrm{V}_{\text {OUT1 }}, \mathrm{V}_{\text {OUT2 }}=\mathrm{OFF}$ | - | 70 | 200 | $\mu \mathrm{A}$ |
| Current Limit | - | 0.55 | 0.80 | - | A |
| Long Term Stability | - | - | 50 | - | mV/khr |
| Overvoltage Shutdown | $\mathrm{V}_{\text {OUT1 }}$ and $\mathrm{V}_{\text {OUT2 }}$ | 32 | 36 | 40 | V |

Secondary Output (VOUT2)

| Output Voltage | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT2 }} \leq 70 \mathrm{~mA}$ | 4.85 | 5.00 | 5.15 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\mathrm{l}_{\text {OUT2 }} \leq 70 \mathrm{~mA}$ | - | 1.5 | 2.5 | V |
| Line Regulation | $11 \leq \mathrm{V}_{\text {IN }} \leq 18 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=70 \mu \mathrm{~A}$ | - | 4.0 | 50 | mV |
| Load Regulation | $1.0 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT2 } 2} \leq 70 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 10 | 50 | mV |
| Current Limit | - | - | 150 | - | mA |

ENABLE Function (ENABLE)

| Input ENABLE Threshold | VOUT2(ON) <br> VOUT1(OFF) | - | 1.40 | 2.50 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input ENABLE Current | Input Voltage Range 0 to 5.0 V | 0.8 | 1.40 | - | V |

PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :--- |
| $\mathbf{5}$ Lead TO-220 | LEAD SYMBOL | FUNCTION |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 2. Dropout Voltage vs. Output Current (VOUT1)


Figure 4. Quiescent Current vs. Output Current (vouti)


Figure 6. $V_{\text {OUT2 }}$ vs. Temperature


Figure 3. Dropout Voltage vs. Output Current (VOUT2)


Figure 5. Quiescent Current vs. Output Current (Vout2)


Figure 7. Line Regulation vs.
Output Current (Vout1)


Figure 8. Load Regulation vs. Output Current (VOUT1)


Figure 10. ENABLE Input Current vs. Input Voltage


Figure 12. Quiescent Current ( $l_{C Q}$ ) vs. $V_{\text {IN }}$ Over R Load


Figure 9. Load Regulation vs. Output Current (VOUT2)


Figure 11. Quiescent Current (ICQ) vs. $V_{\text {IN }}$ Overtemperature


Figure 13. V $_{\text {OUT1 }}$ vs. Temperature

## DEFINITION OF TERMS

Dropout Voltage - The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Current Limit - Peak current that can be delivered to the output.

Input Voltage - The DC voltage applied to the input terminals with respect to ground.

Input Output Differential - The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Long Term Stability - Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage - The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current - The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.
Ripple Rejection - The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of VOUT - The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.


Figure 14. Typical Circuit Waveform

${ }^{*} \mathrm{C}_{1}$ is required if the regulator is located away from the power source filter.
${ }^{* *} \mathrm{C}_{2}$ is required for stability.
Figure 15. Test \& Applications Circuit

## APPLICATION NOTES

Since both outputs are controlled by the same ENABLE, the CS8147 is ideal for applications where a sleep mode is required. Using the CS8147, a section of circuitry such as a display and nonessential 5.0 V circuits can be shut down under microprocessor control to conserve energy.

The test applications circuit diagram shows an automotive radio application where the display is powered by 10 V from $\mathrm{V}_{\text {OUT1 }}$ and the Tuner IC is powered by 5.0 V from $\mathrm{V}_{\text {OUT2 }}$. Neither output is required unless both the ignition and the Radio On/OFF switch are on.

## Stability Considerations

The secondary output $\mathrm{V}_{\text {OUT2 }}$ is inherently stable and does not require a compensation capacitor. However a compensation capacitor connected between $V_{\text {OUT1 }}$ and ground is required for stability in most applications.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C 2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine acceptable value for C 2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.
Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.
Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.
Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found for each output, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

## Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 16) is

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,
IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be compared with those in the package section of the data sheet. Those packages with
$\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 16. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta \mathrm{JA}}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $\mathrm{R}_{\Theta J A}$, it too is a function of package type. $\mathrm{R}_{\Theta C S}$ and $\mathrm{R}_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## PACKAGE THERMAL DATA

| Parameter |  | TO-220 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 2.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {OJA }}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8156

## 12 V, 5.0 V Low Dropout Dual Regulator with ENABLE

The CS8156 is a low dropout $12 \mathrm{~V} / 5.0 \mathrm{~V}$ dual output linear regulator. The $12 \mathrm{~V} \pm 5.0 \%$ output sources 750 mA and the $5.0 \mathrm{~V} \pm 2.0 \%$ output sources 100 mA .

The on board ENABLE function controls the regulator's two outputs. When the ENABLE lead is low, the regulator is placed in SLEEP mode. Both outputs are disabled and the regulator draws only 200 nA of quiescent current.

The regulator is protected against overvoltage conditions. Both outputs are protected against short circuit and thermal runaway conditions.

The CS8156 is packaged in a 5 lead TO-220 with copper tab. The copper tab can be connected to a heat sink if necessary.

## Features

- Two Regulated Outputs
$-12 \mathrm{~V} \pm 5.0 \% ; 750 \mathrm{~mA}$
- $5.0 \mathrm{~V} \pm 2.0 \%$; 100 mA
- Very Low SLEEP Mode Current Drain 200 nA
- Fault Protection
- Reverse Battery
- +60 V, -50 V Peak Transient Voltage
- Short Circuit
- Thermal Shutdown
- CMOS Compatible ENABLE


ON Semiconductor ${ }^{2 \times 1}$
http://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAM

$\mathrm{Tab}=\mathrm{GND}$
Pin 1. $\mathrm{V}_{\mathrm{IN}}$
2. Vout1
3. GND
4. ENABLE
5. VOUT2
$\begin{array}{ll}\text { A } & =\text { Assembly Location } \\ \text { WL, L } & =\text { Wafer Lot } \\ Y Y, Y & =\text { Year } \\ \text { WW, } W & =\text { Work Week }\end{array}$

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8156YT5 | TO-220* <br> STRAIGHT | 50 Units/Rail |
| CS8156YTVA5 | TO-220* <br> VERTICAL | 50 Units/Rail |
| CS8156YTHA5 | TO-220* <br> HORIZONTAL | 50 Units/Rail |

*Five lead.


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage: | Operating Range Peak Transient Voltage (Note 1) | $\begin{gathered} -0.5 \text { to } 26 \\ 60 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Internal Power Dissipation |  | Internally Limited | - |
| Operating Temperature Range |  | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 2) | 260 peak | ${ }^{\circ} \mathrm{C}$ |

1. Load Dump $=46 \mathrm{~V}$
2. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS for $\mathrm{V}_{\text {OUT: }}:\left(\mathrm{V}_{\mathrm{IN}}=14.5 \mathrm{~V}, \mathrm{I}_{\text {OUT } 1}=5.0 \mathrm{~mA}, \mathrm{I}_{\mathrm{OUT} 2}=5.0 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C}\right.$, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Output Stage ( $\mathrm{V}_{\text {OUT1 }}$ )

| Output Voltage, (V $\mathrm{VOUT} 1^{\text {) }}$ | $13 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 16 \mathrm{~V}$, $\mathrm{l}_{\text {OUT } 1} \leq 750 \mathrm{~mA}$ | 11.2 | 12.0 | 12.8 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\begin{aligned} & \text { IOUT1 }=500 \mathrm{~mA} \\ & \text { IOUT1 }=750 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 0.4 \\ & 0.6 \end{aligned}$ | $\begin{aligned} & 0.6 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Line Regulation | $13 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 16 \mathrm{~V}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1}<100 \mathrm{~mA}$ | - | 15 | 80 | mV |
| Load Regulation | $5.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1} \leq 500 \mathrm{~mA}$ | - | 15 | 80 | mV |
| Quiescent Current | lout1 $\leq 500 \mathrm{~mA}$, No Load on Standby IOUT1 $\leq 750 \mathrm{~mA}$, No Load on Standby | - | $\begin{gathered} 45 \\ 100 \end{gathered}$ | $\begin{aligned} & 125 \\ & 250 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Quiescent Current (Sleep Mode) | ENABLE = Low | - | 0.2 | 50 | $\mu \mathrm{A}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$, $\mathrm{l}_{\text {OUT }}=5.0 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=1.5 \mathrm{~V}$ PP at $15.5 \mathrm{~V}_{\text {DC }}$ | 42 | 70 | - | dB |
| Current Limit | - | 0.75 | 1.20 | 2.50 | A |
| Maximum Line Transient | $\mathrm{V}_{\text {OUT } 1} \leq 13 \mathrm{~V}$ | 60 | 90 | - | V |
| Reverse Polarity Input Voltage, DC | $\mathrm{V}_{\text {OUT } 1} \geq-0.6 \mathrm{~V}, 10 \Omega$ Load | -18 | -30 | - | V |
| Reverse Polarity Input Voltage, Transient | $\begin{aligned} & \text { 1.0\% Duty Cycle, } \mathrm{t}=100 \mathrm{~ms}, \mathrm{~V}_{\text {OUT }} \geq-6.0 \mathrm{~V} \text {, } \\ & 10 \Omega \text { Load } \end{aligned}$ | -50 | -80 | - | V |
| Output Noise Voltage | $10 \mathrm{~Hz}-100 \mathrm{kHz}$ | - | - | 500 | $\mu \mathrm{Vrms}$ |
| Output Impedance | $500 \mathrm{~mA} \mathrm{DC} \mathrm{and} 10 \mathrm{~mA} \mathrm{rms}, 100 \mathrm{~Hz}$ | - | 0.2 | 1.0 | $\Omega$ |
| Overvoltage Shutdown | - | 28 | 34 | 45 | V |

Standby Output (VOUT2)

| Output Voltage, (VOUT2) | $9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 16 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT2 }} \leq 100 \mathrm{~mA}$ | 4.90 | 5.00 | 5.10 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Dropout Voltage | lout2 $\leq 100 \mathrm{~mA}$ | - | - | 0.60 | V |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{OUT}} \leq 100 \mathrm{~mA}$ | - | 5.0 | 50 | mV |
| Load Regulation | $1.0 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT2 }} \leq 100 \mathrm{~mA} ; 9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 16 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz} ; \mathrm{l}_{\text {OUT }}=100 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=1.5 \mathrm{~V}_{\text {PP }}$ at $14.5 \mathrm{~V}_{\mathrm{DC}}$ | 42 | 70 | - | dB |
| Current Limit | - | 100 | 200 | - | mA |

## ENABLE Function (ENABLE)

| Input ENABLE Threshold | $V_{\text {OUT1 }}$ Off <br> $V_{\text {OUT1 }}$ On | $2.00$ | $\begin{aligned} & 1.25 \\ & 1.25 \end{aligned}$ | 0.80 - | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input ENABLE Current | $\mathrm{V}_{\text {ENABLE }} \leq \mathrm{V}_{\text {THRESHOLD }}$ | -10 | 0 | 10 | $\mu \mathrm{A}$ |

PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :---: |
| 5 Lead TO-220 | LEAD SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{IN}}$ | Supply voltage, usually direct from battery. |
| 2 | $\mathrm{V}_{\text {OUT1 }}$ | Regulated output $12 \mathrm{~V}, 750 \mathrm{~mA}$ (typ). |
| 3 | GND | Ground connection. |
| 4 | ENABLE | CMOS compatible input lead; switches outputs on and off. When ENABLE is high $V_{\text {OUT } 1}$ and $V_{\text {OUT2 }}$ are active. |
| 5 | $\mathrm{V}_{\text {OUT2 }}$ | Regulated output $5.0 \mathrm{~V}, 100 \mathrm{~mA}$ (typ). |

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 2. Dropout Voltage vs. IOut2


Figure 4. Vout1 vs. Temperature


Figure 6. ENABLE Current vs. ENABLE Voltage


Figure 3. Vout1 vs. Input Voltage


Figure 5. $\mathrm{V}_{\text {OUT2 }}$ vs. Temperature


Figure 7. ENABLE Current vs. ENABLE Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)


Figure 8. Line Transient Response ( $\mathrm{V}_{\mathrm{OUT} 1}$ )


Figure 10. Load Transient Response

$$
\left(\mathrm{V}_{\text {OUT } 1}\right)
$$



Figure 12. Maximum Power Dissipation (TO-220)


Figure 9. Line Transient Response ( $\mathrm{V}_{\mathrm{OUT} 2}$ )


Figure 11. Load Transient Response (Vout2)


Figure 13. Quiescent Current vs. Output Current for $\mathrm{V}_{\text {OUT2 }}$

TYPICAL PERFORMANCE CHARACTERISTICS (continued)


Figure 14. Quiescent Current vs. Output Current for $\mathrm{V}_{\text {OUT1 }}$


Figure 16. Load Regulation vs. Output Current fo $\mathrm{V}_{\text {OUT2 }}$


Figure 15. Line Regulation vs. Output Current for $\mathrm{V}_{\text {OUT2 }}$


Figure 17. Line Regulation vs. Output Current for Vout1


Figure 18. Load Regulation vs. Output
Current for $\mathrm{V}_{\text {OUT1 }}$

## DEFINITION OF TERMS

Dropout Voltage - The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage - The DC voltage applied to the input terminals with respect to ground.

Input Output Differential - The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Long Term Stability - Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage - The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.
Quiescent Current - The part of the positive input current that does not contribute to the positive load current, i.e., the regulator ground lead current.

Ripple Rejection - The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of VOUT - The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.


Figure 19. Typical Circuit Waveform

## APPLICATION NOTES

## Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the cheapest solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitors C2 and C3 shown in the test and applications circuit should work for most applications, however it is not necessarily the best solution.

To determine acceptable values for C 2 and C 3 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part for each output.
Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor $\mathrm{C}_{2}$ will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.
Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations
are observed, the capacitor is large enough to ensure a stable design under steady state conditions.
Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.
Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.
Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.
Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.
Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found for each output, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than $50 \%$ of the maximum allowable ESR found in step 3 above.

Repeat steps 1 through 7 with $\mathrm{C}_{3}$, the capacitor on the other output.

## Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 20) is
where:
$\mathrm{V}_{\mathrm{IN}(\text { max })}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
VOUT2(min) is the minimum output voltage from $V_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,

IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
R_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}^{2}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta J \text { J }}$ can be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\text {©JA }}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 20. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$ where:

$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## CS8156


${ }^{*} \mathrm{C}_{1}$ is required if the regulator is far from power supply filter.
${ }^{* *} \mathrm{C}_{2}, \mathrm{C}_{3}$ required for stability.
Figure 21. Test \& Application Circuit

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> FIVE LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 2.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8161

## 12 V, 5.0 V Low Dropout Dual Regulator with ENABLE

The CS8161 is a $12 \mathrm{~V} / 5.0 \mathrm{~V}$ dual output linear regulator. The $12 \mathrm{~V} \pm 5.0 \%$ output sources 400 mA and the $5.0 \mathrm{~V} \pm 2.0 \%$ output sources 200 mA .

The on board ENABLE function controls the regulator's two outputs. When the ENABLE pin is low, the regulator is placed in SLEEP mode. Both outputs are disabled and the regulator draws only 200 nA of quiescent current.

The primary output, $V_{\text {OUT1 }}$ is protected against overvoltage conditions. Both outputs are protected against short circuit and thermal runaway conditions.

The CS8161 is packaged in a 5 lead TO-220 with copper tab. The copper tab can be connected to a heat sink if necessary.

## Features

- Two Regulated Outputs
- $12 \mathrm{~V} \pm 5.0 \%$; 400 mA
$-5.0 \mathrm{~V} \pm 2.0 \% ; 200 \mathrm{~mA}$
- Very Low SLEEP Mode Current Drain 200 nA
- Fault Protection
- Reverse Battery (-15 V)
- 74 V Load Dump
- -100 V Reverse Transient
- Short Circuit
- Thermal Shutdown


PIN CONNECTIONS AND MARKING DIAGRAM

$\mathrm{Tab}=\mathrm{GND}$
Pin 1. $\mathrm{V}_{\mathrm{IN}}$
2. Vout1
3. GND
4. ENABLE
5. V OUT2

A = Assembly Location
WL, L = Wafer Lot
$Y Y, Y \quad=$ Year
WW, W = Work Week

ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8161YT5 | TO-220** <br> STRAIGHT | 50 Units/Rail |
| CS8161YTVA5 | TO-220** <br> VERTICAL | 50 Units/Rail |
| CS8161YTHA5 | TO-220** <br> HORIZONTAL | 50 Units/Rail |

*Consult your local sales representative for SO-16L package option.
**Five lead.


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*
$\left.\begin{array}{|l|r|c|c|}\hline & \text { Rating } & \text { Value } & \text { Unit } \\ \hline \text { Input Voltage: } & \begin{array}{c}\text { Operating Range } \\ \\ \text { Internal Power Dissipation } \\ \text { Overvoltage Protection }\end{array} & -15 \text { to } 26 \\ 74\end{array}\right)$

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

## CS8161

ELECTRICAL CHARACTERISTICS for $\mathrm{V}_{\text {OUT: }}\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$; $\mathrm{l}_{\text {OUT } 1}=5.0 \mathrm{~mA}$; l $_{\text {OUT2 }}=5.0 \mathrm{~mA}$; $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq+150^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Primary Output Stage ( $\mathrm{V}_{\text {OUT1 }}$ )

| Output Voltage, V ${ }_{\text {OUT1 }}$ | $13 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, $\mathrm{l}_{\text {OUT } 1} \leq 400 \mathrm{~mA}$ | 11.4 | 12.0 | 12.6 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | IOUT1 $=400 \mathrm{~mA}$ | - | 0.35 | 0.6 | V |
| Line Regulation | $13 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 20 \mathrm{~V}, 5.0 \mathrm{~mA} \leq$ lout $<400 \mathrm{~mA}$ | - | - | 80 | mV |
| Load Regulation | $5.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1} \leq 400 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | - | 80 | mV |
| Quiescent Current | $\mathrm{l}_{\text {OUT1 }} \leq 100 \mathrm{~mA}$, No Load on $\mathrm{V}_{\text {OUT2 }}$ $\mathrm{l}_{\text {OUT1 }} \leq 400 \mathrm{~mA}$, No Load on $\mathrm{V}_{\text {OUT2 }}$ | - | $\begin{aligned} & 8.0 \\ & 50 \end{aligned}$ | $\begin{aligned} & 12 \\ & 75 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple Rejection | $f=120 \mathrm{~Hz}, \mathrm{l}_{\text {OUT }}=300 \mu \mathrm{~A}, \mathrm{~V}_{\text {IN }}=15.0 \mathrm{~V}_{\text {DC }}, 2.0 \mathrm{~V}_{\text {RMS }}$ | 42 | - | - | dB |
| Current Limit | - | 0.40 | - | 1.0 | A |
| Reverse Polarity Input Voltage, DC | $\mathrm{V}_{\text {OUT1 }} \geq-0.6 \mathrm{~V}, 10 \Omega$ Load | - | -30 | -18 | V |
| Reverse Polarity Input Voltage, Transient | $\begin{aligned} & \text { 1.0\% Duty Cycle, } \mathrm{t}=100 \mathrm{~ms}, \mathrm{~V}_{\text {OUT }} \geq-6.0 \mathrm{~V} \text {, } \\ & 10 \Omega \text { Load } \end{aligned}$ | - | -80 | -50 | V |
| Overvoltage Shutdown | - | 28 | 34 | 45 | V |
| Short Circuit Current | - | - | - | 700 | mA |

Secondary Output (VOUT2)

| Output Voltage, (V OUT2 $^{\text {) }}$ | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, $\mathrm{I}_{\text {OUT2 }} \leq 200 \mathrm{~mA}$ | 4.90 | - | 5.10 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\mathrm{l}_{\text {OUT2 }} \leq 200 \mathrm{~mA}$ | - | 0.35 | 0.60 | V |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 200 \mathrm{~mA}$ | - | - | 50 | mV |
| Load Regulation | $1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT2 }} \leq 200 \mathrm{~mA} ; \mathrm{V}_{\text {IN }}=14 \mathrm{~V}$ | - | - | 50 | mV |
| Quiescent Current | $\begin{aligned} & \mathrm{I}_{\text {OUT2 }}=50 \mathrm{~mA} \\ & \mathrm{I}_{\text {OUT2 } 2}=200 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 5.0 \\ & 20 \end{aligned}$ | $\begin{aligned} & 10 \\ & 35 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; $\mathrm{l}_{\text {OUT }}=10 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=15 \mathrm{~V}, 2.0 \mathrm{~V}_{\text {RMS }}$ | 42 | - | - | dB |
| Current Limit | - | 200 | - | 600 | mA |
| Short Circuit Current | - | - | - | 400 | mA |

ENABLE Function (ENABLE)

| Input ENABLE Threshold | V <br>  <br>  <br>  <br> VOUT1 Off | - | 1.30 | 0.80 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input ENABLE Current | $\mathrm{V}_{\text {ENABLE }}=5.5 \mathrm{~V}$ | 2.00 | 1.30 | - | V |
|  | $\mathrm{V}_{\text {ENABLE }}<0.8 \mathrm{~V}$ | 80 | - | 500 | $\mu \mathrm{~A}$ |
|  |  | -10 | - | 10 | $\mu \mathrm{~A}$ |

## Other Features

| Sleep Mode | $\mathrm{V}_{\text {ENABLE }}<0.4 \mathrm{~V}$ | - | 0.2 | 50 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Thermal Shutdown |  | - | 150 | - | 210 |
| ${ }^{\circ} \mathrm{C}$ |  |  |  |  |  |
| Quiescent Current in Dropout | $\mathrm{I}_{\text {OUT1 }}=100 \mathrm{~mA}$, I IOUT2 $=50 \mathrm{~mA}$ | - | - | 60 | mA |

PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :--- |
| 5 Lead TO-220 | LEAD SYMBOL |  |
| 1 | $\mathrm{~V}_{\text {IN }}$ | Fupply voltage, usually direct from battery. |
| 2 | $\mathrm{~V}_{\text {OUT1 }}$ | Regulated output $12 \mathrm{~V}, 400 \mathrm{~mA}$ (typ). |
| 3 | GND | Ground connection. |
| 4 | ENABLE | CMOS compatible input lead; switches outputs on and off. <br> When ENABLE is high $\mathrm{V}_{\text {OUT1 }}$ and $\mathrm{V}_{\text {OUT2 }}$ are active. |
| 5 | V OUT2 | Regulated output $5.0 \mathrm{~V}, 200 \mathrm{~mA}$ (typ). |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Output Voltage vs. Temperature for $\mathrm{V}_{\text {OUT1 }}$


Figure 4. Load Regulation vs. Output Current for $\mathrm{V}_{\text {OUT1 }}$


Figure 3. Line Regulation vs. Output Current for Vout1


Figure 5. Quiescent Current vs. Output Current for $\mathrm{V}_{\text {OUT1 }}$

TYPICAL PERFORMANCE CHARACTERISTICS (continued)


Figure 6. Dropout Voltage vs. Output Voltage for $\mathrm{V}_{\text {OUT1 }}$


Figure 8. Output Voltage vs. Temperature for $V_{\text {OUT2 }}$


Figure 10. Load Regulation vs. Output Current for $\mathrm{V}_{\text {OUT2 }}$


Figure 7. Quiescent Current vs. Output Current @ Dropout for $\mathrm{V}_{\text {OUT1 }}$


Figure 9. Line Regulation vs. Output Current for Vout2


Figure 11. Quiescent Current vs. Output Current for $\mathrm{V}_{\text {OUT2 }}$

TYPICAL PERFORMANCE CHARACTERISTICS (continued)


Figure 12. Dropout Voltage vs. Output Current for $\mathrm{V}_{\text {OUT2 }}$


Figure 14. Enable Threshold Voltage vs. Temperature


Figure 13. Quiescent Current vs. Output Current @ Dropout for V


Figure 15. ENABLE Current vs. ENABLE Voltage


Figure 16. 12 mA ENABLE Current vs.
ENABLE Voltage

## DEFINITION OF TERMS

Dropout Voltage - The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage - The DC voltage applied to the input terminals with respect to ground.

Input Output Differential - The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Long Term Stability - Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage - The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.
Quiescent Current - The part of the positive input current that does not contribute to the positive load current, i.e., the regulator ground lead current.

Ripple Rejection - The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
Temperature Stability of VOUT - The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.


Figure 17. Typical Circuit Waveform

${ }^{*} \mathrm{C}_{1}$ required if regulator is located far from power supply filter.
${ }^{* *} \mathrm{C}_{2}, C_{3}$ required for stability, value may be increased. Capacitor must operate at minimum temperature expected.
Figure 18. Application Diagram

## APPLICATION NOTES

Since both outputs are controlled by the same ENABLE, the CS8161 is ideal for applications where a sleep mode is required. Using the CS8161, a section of circuitry such as a display and nonessential 5.0 V circuits can be shut down under microprocessor control to conserve energy.

The example in the Applications Diagram (Figure 18) shows an automotive radio application where the display is powered by the 12 V on $\mathrm{V}_{\text {OUT1 }}$ and the Tuner IC is powered by the 5.0 V on $\mathrm{V}_{\text {OUT2 }}$. Neither output is required unless both the ignition and the Radio On/Off switch are on.

## Stability Considerations

The output or compensation capacitor (Application diagram $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$ ) helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the cheapest solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The values for the output capacitors $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$ shown in the test and applications circuit should work for most applications, however it is not necessarily the best solution.

To determine acceptable values for $\mathrm{C}_{2}$ and $\mathrm{C}_{3}$ for a particular application, start with tantalum capacitors of the recommended value on each output and work towards less expensive alternative parts for each output in turn.
Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs on the oscilloscope. A decade box connected in series with the capacitor $\mathrm{C}_{2}$ will simulate the higher ESR of an aluminum capacitor.(Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible)
Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.
Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.
Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase.

This point represents the worst case input voltage conditions.
Step 5: If the capacitor $\mathrm{C}_{2}$ is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. (A smaller capacitor will usually cost less and occupy less board space.) If the capacitor oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.
Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real work environment. Vary the ESR to reduce ringing.
Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.
Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20 \%$ so the minimum value found should be increased by at least $50 \%$ to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than $50 \%$ of the maximum allowable ESR found in step 3 above. Once the value for $\mathrm{C}_{2}$ is determined, repeat the steps to determine the appropriate value for $\mathrm{C}_{3}$.

## Calculating Power Dissipation in a

## Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 19) is

```
\(P_{D}(\) max \()=\left\{V_{I N}(\right.\) max \(\left.)-V_{O U T 1(m i n)}\right){ }^{\text {IOUT1 }}\) (max) \()+\)
    \(\left(\mathrm{V}_{\mathrm{IN}(\text { max })}-\mathrm{V}_{\text {OUT2 }}(\min )\right.\) IIOUT2(max) \(+\mathrm{V}_{\mathrm{IN}(\text { max })} \mathrm{IQ}_{\text {(1) }}\)
```

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,
$\mathrm{I}_{\text {OUT2 (max) }}$ is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
R_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \text { JA }}$ can be compared with those in the package section of the data sheet. Those packages with
$\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 19. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $\mathrm{R}_{\Theta J A}$, it too is a function of package type. $\mathrm{R}_{\Theta C S}$ and $\mathrm{R}_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> FIVE LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 2.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta J A}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8281

### 5.0 V/250 mA, $5.0 \mathrm{~V} / 100 \mathrm{~mA}$ Micropower Low Dropout Regulator with ENABLE

The CS8281 is a precision, dual 5.0 V micropower linear voltage regulator. The switched primary output ( $\mathrm{V}_{\text {OUT1 }}$ ) supplies up to 250 mA while the secondary ( $\mathrm{V}_{\text {OUT2 }}$ ) is capable of supplying 100 mA . Both outputs have a maximum dropout voltage of 600 mV and low reverse current. Quiescent current drain is typically $150 \mu \mathrm{~A}$ when supplying $100 \mu \mathrm{~A}$ from each output.

The ENABLE input provides logic level control of the primary output. With the primary output disabled, quiescent current drain is typically $100 \mu \mathrm{~A}$ when supplying $100 \mu \mathrm{~A}$ from the secondary output.

The CS8281 is extremely robust with protection provided for reverse battery, short circuit, overvoltage, and overtemperature on both outputs.

The CS8281 is available in a 5 -lead D ${ }^{2}$ PAK.

## Features

- $5.0 \mathrm{~V} / 250 \mathrm{~mA}$ Primary Output
- $5.0 \mathrm{~V} / 100 \mathrm{~mA}$ Secondary Output
- 3.0\% Tolerance, Both Outputs
- ON/OFF Control for Primary Output
- Low Quiescent Current Drain ( $100 \mu \mathrm{~A} \mathrm{~V}_{\mathrm{OUT} 2}$ )
- Low Reverse Current
- Protection Features
- Reverse Battery (-15 V)
- 74 V Load Dump
- Short Circuit
- Overtemperature
- Overvoltage (34 V)

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAM


Tab $=$ GND
Pin 1. $\mathrm{V}_{\mathrm{IN}}$
2. $\mathrm{V}_{\mathrm{OUT} 1}$
3. GND
4. V OUT2
5. ENABLE

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
ORDERING INFORMATION*

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS8281YDP5 | D2PAK, <br> 5-PIN | 50 Units/Rail |
| CS8281YDPR5 | D2PAK, <br> 5-PIN | 750 Tape \& Reel |

*Consult your local sales representative for SO-8, SO-16, DIP-8, DIP-16, TO-220 FIVE LEAD, and D2PAK 7-PIN packaging options.


Figure 1. Block Diagram

## ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |  |
| :--- | :---: | :---: | :---: |
| Input Voltage |  | -15 to 74 | V |
| Power Dissipation | Internally Limited | - |  |
| Operating Temperature Range | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |  |
| Maximum Junction Temperature | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature Range | Reflow (SMD styles only) (Note 1$)$ | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Electrostatic Discharge (Human Body Model) | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering |  | 4.0 | kV |

1. 16 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS: $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, \mathrm{I}_{\text {OUT } 1}=\mathrm{l}_{\text {OUT } 2}=100 \mu \mathrm{~A},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq 125^{\circ} \mathrm{C}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Primary Output Stage (Vout1)

| Output Voltage, V ${ }_{\text {OUT1 }}$ | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT } 1} \leq 250 \mathrm{~mA}$ | 4.85 | 5.00 | 5.15 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\begin{aligned} & \text { lout }=250 \mathrm{~mA} \\ & \text { lout } 1=100 \mu \mathrm{~A} \end{aligned}$ |  | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Load Regulation | $1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1} \leq 250 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Quiescent Current | ENABLE $=$ HIGH, $\mathrm{V}_{\text {IN }}=16 \mathrm{~V}, \mathrm{I}_{\text {OUT } 1}=250 \mathrm{~mA}$ | - | 22 | 50 | mA |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{l}_{\text {OUT } 1}=125 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |
| Current Limit | - | 260 | 400 | - | mA |
| Short Circuit Current Limit | $\mathrm{V}_{\text {OUT1 }}=0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=16 \mathrm{~V}$ | 25 | - | - | mA |
| Reverse Current | $\mathrm{V}_{\text {OUT } 1}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 1500 | $\mu \mathrm{A}$ |

Secondary Output (VOUT2)

| Output Voltage, (V OUT2 $^{\text {) }}$ | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT } 1} \leq 100 \mathrm{~mA}$ | 4.85 | 5.00 | 5.15 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\begin{aligned} & \text { lout2 }=100 \mathrm{~mA} \\ & \text { IOUT2 }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT2 }} \leq 100 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Quiescent Current | $\begin{aligned} & \text { ENABLE }=\text { LOW, } \mathrm{V}_{\text {IN }}=12.8 \mathrm{~V} \\ & \text { ENABLE }=\mathrm{HIGH}, \mathrm{~V}_{\mathrm{IN}}=16 \mathrm{~V} \end{aligned}$ | - | $\begin{gathered} 100 \\ 8.0 \end{gathered}$ | $\begin{gathered} 150 \\ 25 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; $\mathrm{l}_{\text {OUT2 }}=50 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |
| Current Limit | - | 105 | 200 | - | mA |
| Short Circuit Current Limit | $\mathrm{V}_{\text {OUT2 }}=0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=16 \mathrm{~V}, \mathrm{l}_{\text {OUT }}=0 \mathrm{~A}$ | 25 | - | - | mA |
| Reverse Current | $\mathrm{V}_{\text {OUT2 }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 250 | $\mu \mathrm{A}$ |

ENABLE Function (ENABLE)

| Input Threshold | $\mathrm{ENABLE}=\mathrm{LOW}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$ | - | 1.2 | 0.8 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | $\mathrm{ENABLE}=\mathrm{HIGH}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$ | 2.0 | 1.2 | - | V |
| Input Bias Current | $0 \mathrm{~V} \leq \mathrm{V}_{\text {ENABLE }} \leq 5.0 \mathrm{~V}$ | -2.0 | 0 | 2.0 | $\mu \mathrm{~A}$ |

## Protection Circuits

| Overtemperature Threshold | - | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Overvoltage Shutdown | - | 30 | 34 | 38 | V |

PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :---: |
| D2PAK, 5-PIN | LEAD SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\text {IN }}$ | Supply voltage to IC, usually direct from battery. |
| 2 | $\mathrm{V}_{\text {OUT1 }}$ | 5.0 V regulated output which is activated by ENABLE input. |
| 3 | GND | Ground connection. |
| 4 | $\mathrm{V}_{\text {OUT2 }}$ | Standby output 5.0 V, 100 mA capability; always on. |
| 5 | ENABLE | CMOS compatible input lead; switches $\mathrm{V}_{\text {OUt1 }}$. When ENABLE is high, $\mathrm{V}_{\text {OUT1 }}$ is active. |

## DEFINITION OF TERMS

Current Limit - Peak current that can be delivered to the output.

Dropout Voltage - The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Output Differential - The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Input Voltage - The DC voltage applied to the input terminals with respect to ground.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Long Term Stability - Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Quiescent Current - The part of the positive input current that does not contribute to the positive load current, i.e., the regulator ground lead current.

Ripple Rejection - The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Short Circuit Current Limit - Peak current that can be delivered by the outout when forced to 0 V .

Temperature Stability of Vout - The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.


Figure 2. Typical Circuit Waveform

## APPLICATION NOTES

## General

The CS8281 is a micropower dual 5.0 V regulator. All bias required to operate the internal circuitry is derived from the standby output, $V_{\text {OUT2 }}$. If this output experiences an over current situation and collapses, then $\mathrm{V}_{\text {OUT1 }}$ will also collapse (see Figure 2).

If there is critical circuitry that must remain active under most conditions it should be connected to VOUT2. Any circuitry that is likely to be subjected to a short circuit, e.g., circuitry outside the module, should be connected to $V_{\text {OUT1 }}$.

## External Capacitors

Output capacitors are required for stability with the CS8281. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability.

Worst-case is determined at the minimum ambient temperature and maximum load expected.
Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.
Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to $-40^{\circ} \mathrm{C}$, capacitors rated at that temperature must be used.
More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators," document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## ENABLE

The ENABLE function controls V ${ }_{\text {OUT1 }}$. When ENABLE is high, $V_{\text {OUT1 }}$ is on. When ENABLE is low, $V_{\text {OUT1 }}$ is off.

## Calculating Power Dissipation in a <br> Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 3) is


where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,
IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at both IOUT1(max) and IOUT2(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 3. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JJC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## TEST \& APPLICATION DIAGRAM



[^15]Figure 4. Test \& Application Circuit

## CS8281

PACKAGE THERMAL DATA

| Parameter |  | D $^{2}$ PAK, 5-PIN | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J A}=\mathrm{R}_{\Theta J C}+\mathrm{R}_{\Theta \mathrm{CA}}$


## CS8371

### 8.0 V/1.0 A, $5.0 \mathrm{~V} / 250 \mathrm{~mA}$ Dual Regulator with Independent Output Enables and NOCAP ${ }^{\text {M }}$

The CS8371 is an $8.0 \mathrm{~V} / 5.0 \mathrm{~V}$ dual output linear regulator. The 8.0 $\mathrm{V} \pm 5.0 \%$ output sources 1.0 A , while the $5.0 \mathrm{~V} \pm 5.0 \%$ output sources 250 mA . Each output is controlled by its own ENABLE lead. Setting the ENABLE input high turns on the associated regulator output. Holding both ENABLE inputs low puts the IC into sleep mode where current consumption is less than $10 \mu \mathrm{~A}$.

The regulator is protected against overvoltage, short-circuit and thermal runaway conditions. The device can withstand 45 V load dump transients making suitable for use in automotive environments. ON's proprietary NOCAP solution is the first technology which allows the output to be stable without the use of an external capacitor.

The CS8371 is available in a 7 lead TO-220 package with copper tab. The tab can be connected to a heatsink if necessary.

## Features

- Two Regulated Outputs
- 8.0 V $\pm 5.0 \%$; 1.0 A
- $5.0 \mathrm{~V} \pm 5.0 \% ; 250 \mathrm{~mA}$
- Independent ENABLE for Each Output
- Seperate Sense Feedback Lead for 8.0 V Output
- < $10 \mu \mathrm{~A}$ Sleep Mode Current
- Fault Protection
- Overvoltage Shutdown
- +45 V Peak Transient Voltage
- Short Circuit
- Thermal Shutdown
- CMOS Compatible, Low Current ENABLE Inputs


PIN CONNECTIONS AND
MARKING DIAGRAM

$\mathrm{Tab}=\mathrm{GND}$
Pin 1. ENABLE ${ }_{1}$
2. ENABLE $_{2}$
3. $V_{\text {OUT2 }}$
4. GND
5. Sense
6. $\mathrm{V}_{\mathrm{CC}}$
7. VOUT1

A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8371ET7 | TO-220* <br> STRAIGHT | 50 Units/Rail |
| CS8371ETVA7 | TO-220* <br> VERTICAL | 50 Units/Rail |
| CS8371ETHA7 | TO-220* <br> HORIZONTAL | 50 Units/Rail |

*Seven lead.


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Power Dissipation | Internally Limited | - |
| ENABLE Input Voltage Range | -0.6 to +10 | V |
| Load Current (8.0 V Regulator) | Internally Limited | - |
| Load Current (5.0 V Regulator) | Internally Limited | - |
| Transient Peak Voltage (31 V Load Dump @ 14 V V CC ) | 45 | V |
| Storage Temperature Range | Wave Solder (through hole styles only) (Note 1) | 260 peak |
| Junction Temperature Range | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering: | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS: $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}, 10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}\right.$, ENABLE $_{1}=\mathrm{ENABLE}_{2}=5.0 \mathrm{~V}$, IOUT1 $=$ lout2 $=5.0 \mathrm{~mA}$, unless otherwise stated.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Primary Output ( $\mathrm{V}_{\text {OUT1 }}$ ) |  |  |  |  |  |
| Output Voltage | l OUT1 $=1.0 \mathrm{~A}$ | 7.60 | 8.00 | 8.40 | V |
| Line Regulation | $10.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}$ | - | - | 50 | mV |
| Load Regulation | $5.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1} \leq 1.0 \mathrm{~A}$ | - | - | 150 | mV |
| Sleep Mode Quiescent Current | $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}, \mathrm{ENABLE}_{1}=\mathrm{ENABLE}_{2}=0 \mathrm{~V}$ | 0 | 0.2 | 10.0 | $\mu \mathrm{A}$ |
| Quiescent Current | $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}, \mathrm{l}_{\text {OUT } 1}=1.0 \mathrm{~A}, \mathrm{I}_{\text {OUT2 }}=250 \mathrm{~mA}$ | - | - | 30 | mA |
| Dropout Voltage | $\begin{aligned} & \mathrm{I}_{\text {OUT } 1}=250 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{OUT} 1}=1.0 \mathrm{~A} \end{aligned}$ | - | - | $\begin{aligned} & 1.2 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Quiescent Bias Current |  | $\begin{aligned} & \text { - } \\ & \text { _ } \end{aligned}$ |  | $\begin{aligned} & 10 \\ & 22 \end{aligned}$ | mA <br> mA |
| Ripple Rejection | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V} \text { with } 1.0 \mathrm{~V}_{\mathrm{PP}} \mathrm{AC}, \mathrm{C}_{\text {OUT }}=0 \mu \mathrm{~F} \\ & \mathrm{f}=10 \mathrm{kHz}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V} \text { with } 1.0 \mathrm{~V}_{\mathrm{PP}} \mathrm{AC}, \mathrm{C}_{\text {OUT }}=0 \mu \mathrm{~F} \\ & \mathrm{f}=20 \mathrm{kHz}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V} \text { with } 1.0 \mathrm{~V}_{\mathrm{PP}} \mathrm{AC}, \mathrm{C}_{\text {Out }}=0 \mu \mathrm{~F} \end{aligned}$ | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 90 \\ & 74 \\ & 68 \end{aligned}$ | - | dB <br> dB <br> dB |
| Current Limit | $\mathrm{V}_{\mathrm{CC}}=16 \mathrm{~V}$ | 1.1 | - | 2.5 | A |
| Overshoot Voltage | $5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{REG} 1} \leq 1.0 \mathrm{~A}$ | - | - | 6.0 | V |
| Output Noise | $10 \mathrm{~Hz}-100 \mathrm{kHz}$ | - | 300 | - | $\mu \mathrm{V}_{\text {rms }}$ |

Secondary Output (VOUT2)

| Output Voltage | IOUT2 $=250 \mathrm{~mA}$ | 4.75 | 5.00 | 5.25 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation | $7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}$ | - | - | 40 | mV |
| Load Regulation | $5.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT2 }} \leq 250 \mathrm{~mA}$ | - | - | 100 | mV |
| Dropout Voltage | $\begin{aligned} & \mathrm{I}_{\text {OUT2 }}=5.0 \mathrm{~mA} \\ & \mathrm{I}_{\text {OUT2 } 2}=250 \mathrm{~mA} \end{aligned}$ | - | - | $\begin{aligned} & 2.2 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Quiescent Bias Current | $\begin{aligned} & \mathrm{I}_{\text {OUT2 }}=5.0 \mathrm{~mA}, \text { ENABLE1 }=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V}, \\ & \mathrm{I}_{\mathrm{Q}}=\mathrm{I}_{\mathrm{CC}}-\mathrm{I}_{\text {OUT2 }} \\ & \mathrm{I}_{\text {OUT2 }}=250 \mathrm{~mA}, \text { ENABLE1 }=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V}, \\ & \mathrm{I}_{\mathrm{Q}}=\mathrm{I}_{\mathrm{CC}}-\mathrm{I}_{\text {OUT2 }} \end{aligned}$ |  |  | $\begin{aligned} & 7.0 \\ & 8.0 \end{aligned}$ | mA <br> mA |
| Ripple Rejection | $\begin{aligned} & \mathrm{f}=120 \mathrm{~Hz}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V} \text { with } 1.0 \mathrm{~V}_{\text {PP }} \mathrm{AC}, \mathrm{C}_{\text {OUT }}=0 \mu \mathrm{~F} \\ & \mathrm{f}=10 \mathrm{kHz}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V} \text { with } 1.0 \mathrm{~V}_{\mathrm{PP}} \mathrm{AC}, \mathrm{C}_{\text {OUT }}=0 \mu \mathrm{~F} \\ & \mathrm{f}=20 \mathrm{kHz}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V} \text { with } 1.0 \mathrm{~V}_{\mathrm{PP}} A C, C_{\text {Out }}=0 \mu \mathrm{~F} \end{aligned}$ |  | $\begin{aligned} & 90 \\ & 75 \\ & 67 \end{aligned}$ | - | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Current Limit | $\mathrm{V}_{\mathrm{CC}}=16 \mathrm{~V}$ | 270 | - | 600 | mA |
| Overshoot Voltage | $5.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{REG} 2} \leq 250 \mathrm{~mA}$ | - | - | 4.3 | V |
| Output Noise | $10 \mathrm{~Hz}-100 \mathrm{kHz}$ | - | 170 | - | $\mu \mathrm{V}_{\text {rms }}$ |

ENABLE Function (ENABLE)

| Input Current | $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}, 0 \mathrm{~V} \leq \mathrm{ENABLE} \leq 5.5 \mathrm{~V}$ | -150 | - | 150 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Voltage | Low | 0 | - | 0.8 | V |
|  | High | 2.0 | - | 5.0 | V |

## Protection Circuitry

| ESD Threshold | Human Body Model | $\pm 2.0$ | $\pm 4.0$ | - | kV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Overvoltage Shutdown | - | 24 | - | 30 | V |
| Thermal Shutdown | Guaranteed by Design | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Hysteresis |  | - | 30 | - | ${ }^{\circ} \mathrm{C}$ |

PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :--- |
| $\mathbf{7}$ Lead TO-220 | LEAD SYMBOL |  |
| 1 | ENABLE $_{1}$ | ENABLE control for the $8.0 \mathrm{~V}, 1.0 \mathrm{~A}$ output. |
| 2 | ENABLE $_{2}$ | ENABLE control for the $5.0 \mathrm{~V}, 250 \mathrm{~mA}$ output. |
| 3 | V OUT2 $^{2}$ | $5.0 \mathrm{~V} \pm 5.0 \%, 250 \mathrm{~mA}$ regulated output. |
| 4 | GND | Ground. |
| 5 | Sense | Sense feedback for the primary 8.0 V output. |
| 6 | $\mathrm{~V}_{\text {CC }}$ | Supply voltage, usually from battery. |
| 7 | $\mathrm{~V}_{\text {OUT1 }}$ | $8.0 \mathrm{~V} \pm 5.0 \%, 1.0$ A regulated output. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Regulator 1 Output Voltage


Figure 4. Regulator 1 Dropout Voltage


Figure 3. Regulator 2 Output Voltage


Figure 5. Regulator 2 Dropout Voltage


Figure 6. Regulator 1 Current Limit


Figure 8. Quiescent Current


Figure 10. Regulator 1 Quiescent Current


Figure 7. Regulator 2 Current Limit


Figure 9. Quiescent Current


Figure 11. Regulator 2 Quiescent Current


Figure 12. Regulator 1 Load Regulation


Figure 14. Regulator 1 Startup


Figure 16. Regulator 1 Line Transient Response


Figure 13. Regulator 2 Load Regulation


Figure 15. Regulator 2 Startup


Figure 17. Regulator 2 Line Transient Response


Figure 18. Regulator 1 Load Transient Response


Figure 20. Regulator 1 Ripple Rejection


Figure 19. Regulator 2 Load Transient Response


Figure 21. Regulator 2 Ripple Rejection


Figure 22. Regulator 1 Stability

## DEFINITION OF TERMS

Dropout Voltage - The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Current Limit - Peak current that can be delivered to the output.

Input Voltage - The DC voltage applied to the input terminals with respect to ground.

Input Output Differential - The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Long Term Stability - Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage - The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.
Quiescent Current - The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.
Ripple Rejection - The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of Vout - The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.


Figure 23. Applications Circuit

## APPLICATION NOTES

With seperate control of each output channel, the CS8371 is ideal for applications where each load must be switched independently. In an automotive radio, the 8.0 V output drives the displays and tape drive motors while the 5.0 V output supplies the Tuner IC and memory.

## Stability Considerations/NOCAP

Normally a low dropout or quasi-low dropout regulator (or any type requiring a slow lateral PNP in the control loop) necessitates a large external compensation capacitor at the output of the IC. The external capacitor is also used to curtail overshoot, determine startup delay time and load transient response.

Traditional LDO regulators typically have low unity gain bandwidth, display overshoot and poor ripple rejection. Compensation is also an issue because the high frequency
load capacitor value, ESR (Equivalent Series Resistance) and board layout parasitics all can create oscillations if not properly accounted for.
NOCAP is an ON Semiconductor exclusive output stage which internally compensates the LDO regulator over temperature, load and line variations without the need for an expensive external capacitor. It incorporates high gain ( $>80 \mathrm{~dB}$ ) and large unity gain bandwidth ( $>100 \mathrm{kHz}$ ) while maintaining many of the characteristics of a single-pole amplifier (large phase margin and no overshoot).
NOCAP is ideally suited for slow switching or steady loads. If the load displays large transient current requirements, such as with high frequency microprocessors, an output storage capacitor may be needed. Some large capacitor and small capacitor ESR values at the output may
cause small signal oscillations at the output. This will depend on the load conditions. With these types of loads, a traditional output stage may be better suited for proper operation.

Output 1 employs NOCAP. Refer to the plots in the Typical Performance Characteristics section for appropriate output capacitor selections for stability if an external capacitor is required by the switching characteristics of the load. Output 2 has a Darlington NPN-type output structure and is inherently stable with any type of capacitive load or no capacitor at all.

## Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 24) is

$$
\begin{aligned}
& \left.P_{D}(\text { max })=\left\{V_{I N}(\text { max })-V_{O U T 1(m i n)}\right) \text { IOUT1 } \text { max }\right)+
\end{aligned}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,
IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at IOUT(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{PD}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \text { JA }}$ can be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 24. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

PACKAGE THERMAL DATA

| Parameter |  | TO-220 <br> SEVEN LEAD | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8391

## $5.0 \mathrm{~V} / 250 \mathrm{~mA}, 5.0 \mathrm{~V} / 100 \mathrm{~mA}$ Micropower Low Dropout Regulator with ENABLE

The CS8391 is a precision, dual 5.0 V micropower linear voltage regulator. The switched primary output ( $\mathrm{V}_{\text {OUT1 }}$ ) supplies up to 250 mA while the secondary ( $\mathrm{V}_{\text {OUT2 }}$ ) is capable of supplying 100 mA . Both outputs have a maximum dropout voltage of 600 mV and low reverse current. Quiescent current drain is typically $150 \mu \mathrm{~A}$ when supplying $100 \mu \mathrm{~A}$ from each output.

The ENABLE input provides logic level control of the primary output. With the primary output disabled, quiescent current drain is typically $100 \mu \mathrm{~A}$ when supplying $100 \mu \mathrm{~A}$ from the secondary output.

The CS8391 is extremely robust with protection provided for reverse battery, short circuit, and overtemperature on both outputs

The CS8391 is available in a 5 -lead D ${ }^{2} \mathrm{PAK}$.

## Features

- $5.0 \mathrm{~V} / 250 \mathrm{~mA}$ Primary Output
- $5.0 \mathrm{~V} / 100 \mathrm{~mA}$ Secondary Output
- 3.0\% Tolerance, Both Outputs
- ON/OFF Control for Primary Output
- Low Quiescent Current Drain ( $100 \mu \mathrm{~A} \mathrm{~V}_{\mathrm{OUT} 2}$ )
- Low Reverse Current
- Protection Features
- Reverse Battery (-15 V)
- Short Circuit
- Overtemperature

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAM


$$
\mathrm{Tab}=\mathrm{GND}
$$

Pin 1. $V_{I N}$
2. $\mathrm{V}_{\mathrm{OUT} 1}$
3. GND
4. Vout2
5. ENABLE

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
ORDERING INFORMATION*

| Device | Package | Shipping |
| ---: | :---: | :---: |
| CS8391YDP5 | D2PAKK, <br> 5-PIN | 50 Units/Rail |
| CS8391YDPR5 | D2PAK, <br> 5-PIN | 750 Tape \& Reel |

*Consult your local sales representative for SO-8, SO-16, DIP-8, DIP-16, TO-220 FIVE LEAD, and $\mathrm{D}^{2}$ PAK 7-PIN packaging options.


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage |  | -15 to 45 | V |
| Power Dissipation |  | Internally Limited | - |
| Operating Temperature Range |  | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Electrostatic Discharge (Human Body Model) |  | 4.0 | kV |
| Lead Temperature Soldering | Wave Solder (through hole styles only)(Note 1) Reflow (SMD styles only) (Note 2) | 260 peak 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS: $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, $\mathrm{I}_{\text {OUT } 1}=\mathrm{I}_{\mathrm{OUT} 2}=100 \mu \mathrm{~A},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq 125^{\circ} \mathrm{C}$, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Primary Output Stage ( $\mathrm{V}_{\text {OUT } 1}$ ) |  |  |  |  |  |
| Output Voltage, V ${ }_{\text {OUT1 }}$ | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT } 1} \leq 250 \mathrm{~mA}$ | 4.85 | 5.00 | 5.15 | V |
| Dropout Voltage | $\begin{aligned} & \text { lout }=250 \mathrm{~mA} \\ & \text { lout }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Load Regulation | $1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1} \leq 250 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Quiescent Current | ENABLE $=$ HIGH, $\mathrm{V}_{\text {IN }}=16 \mathrm{~V}, \mathrm{louT} 1=250 \mathrm{~mA}$ | - | 22 | 50 | mA |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}, \mathrm{l}_{\text {OUT } 1}=125 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |
| Current Limit | - | 260 | 400 | - | mA |
| Short Circuit Current Limit | $\mathrm{V}_{\text {OUT1 }}=0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=16 \mathrm{~V}$ | 25 | - | - | mA |
| Reverse Current | $\mathrm{V}_{\text {OUT1 }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 1500 | $\mu \mathrm{A}$ |

Secondary Output (VOUT2)

| Output Voltage, (V $\mathrm{V}_{\text {Ot2 }}$ ) | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT } 1} \leq 100 \mathrm{~mA}$ | 4.85 | 5.00 | 5.15 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\begin{aligned} & \text { lout2 }=100 \mathrm{~mA} \\ & \text { lout2 }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT2 }} \leq 100 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Quiescent Current | $\begin{aligned} & \text { ENABLE }=\mathrm{LOW}, \mathrm{~V}_{\mathrm{IN}}=12.8 \mathrm{~V} \\ & \text { ENABLE }=\mathrm{HIGH}, \mathrm{~V}_{\text {IN }}=16 \mathrm{~V}, \mathrm{I}_{\text {OUT2 } 2}=100 \mathrm{~mA} \end{aligned}$ |  | $\begin{aligned} & 100 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 150 \\ & 25 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; $\mathrm{l}_{\text {OUT2 }}=50 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |
| Current Limit | - | 105 | 200 | - | mA |
| Short Circuit Current Limit | $\mathrm{V}_{\text {OUT2 }}=0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=16 \mathrm{~V}, \mathrm{I}_{\text {OUT1 }}=0 \mathrm{~A}$ | 25 | - | - | mA |
| Reverse Current | $\mathrm{V}_{\text {OUT2 }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 250 | $\mu \mathrm{A}$ |

ENABLE Function (ENABLE)

| Input Threshold | ENABLE $=\operatorname{LOW}, 7.0 \mathrm{~V} \leq \mathrm{V}$ IN $\leq 26 \mathrm{~V}$ | - | 1.2 | 0.8 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | ENABLE $=\mathrm{HIGH}, 7.0 \mathrm{~V} \leq \mathrm{V}$ IN $\leq 26 \mathrm{~V}$ | 2.0 | 1.2 | - | V |
| Input Bias Current | $0 \mathrm{~V} \leq \mathrm{V}_{\text {ENABLE }} \leq 5.0 \mathrm{~V}$ | -2.0 | 0 | 2.0 | $\mu \mathrm{~A}$ |

## Protection Circuits

Overtemperature Threshold
Note 3
150

${ }^{\circ} \mathrm{C}$
3. Guaranteed by design.

PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :---: |
| D2PAK, 5-PIN | LEAD SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{IN}}$ | Supply voltage to IC, usually direct from battery. |
| 2 | $V_{\text {OUT1 }}$ | 5.0 V regulated output which is activated by ENABLE input. |
| 3 | GND | Ground connection. |
| 4 | $V_{\text {OUT2 }}$ | Standby output 5.0 V, 100 mA capability; always on. |
| 5 | ENABLE | CMOS compatible input lead; switches $\mathrm{V}_{\text {OUT1 }}$. When ENABLE is high, Vout1 is active. |

## DEFINITION OF TERMS

Current Limit - Peak current that can be delivered to the output.

Dropout Voltage - The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Output Differential - The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Input Voltage - The DC voltage applied to the input terminals with respect to ground.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.
Long Term Stability - Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.
Quiescent Current - The part of the positive input current that does not contribute to the positive load current, i.e., the regulator ground lead current.

Ripple Rejection - The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
Short Circuit Current Limit - Peak current that can be delivered by the outout when forced to 0 V .
Temperature Stability of Vout - The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.


Figure 2. Typical Circuit Waveform

## APPLICATION NOTES

## General

The CS8391 is a micropower dual 5.0 V regulator. All bias required to operate the internal circuitry is derived from the standby output, $V_{\text {OUT2 } 2}$. If this output experiences an over current situation and collapses, then Vout1 will also collapse (see Figure 2).

If there is critical circuitry that must remain active under most conditions it should be connected to $\mathrm{V}_{\text {OUT2 }}$. Any circuitry that is likely to be subjected to a short circuit, e.g., circuitry outside the module, should be connected to $\mathrm{V}_{\text {OUT1 }}$ -

## External Capacitors

Output capacitors are required for stability with the CS8391. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability.

Worst-case is determined at the minimum ambient temperature and maximum load expected.
Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.
Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to $-40^{\circ} \mathrm{C}$, capacitors rated at that temperature must be used.
More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators," document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## ENABLE

The ENABLE function controls V OUT1. When ENABLE is high, V VUT1 is on. When ENABLE is low, V ${ }_{\text {OUT1 }}$ is off.

## Calculating Power Dissipation in a <br> Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 3) is
$\mathrm{P}_{\mathrm{D}(\text { max })}=\left\{\mathrm{V}_{\mathrm{IN}(\text { max })}-\mathrm{VOUT1}^{(\text {min })}\right)_{\text {IOUT1 }}($ max $)+$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,
IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at both IOUT1(max) and IOUT2(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta J A}$ can be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.


Figure 3. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\text {©JC }}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heat sink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heat sink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.


[^16]Figure 4. Test \& Application Circuit

CS8391

PACKAGE THERMAL DATA

| Parameter |  | D $^{2}$ PAK, 5-PIN | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta J A}=\mathrm{R}_{\Theta J C}+\mathrm{R}_{\Theta \mathrm{CA}}$


## CS8481

### 3.3 V/250 mA, $5.0 \mathrm{~V} / 100 \mathrm{~mA}$ Micropower Low Dropout Regulator with ENABLE

The CS8481 is a precision, dual micropower linear voltage regulator. The switched 3.3 V primary output ( $\mathrm{V}_{\text {OUT1 }}$ ) supplies up to 250 mA while the secondary 5.0 V ( $\mathrm{V}_{\text {OUT2 }}$ ) is capable of supplying 100 mA . Both outputs have a maximum dropout voltage of 600 mV and low reverse current. Quiescent current drain is typically $150 \mu \mathrm{~A}$ when supplying $100 \mu \mathrm{~A}$ from each output.

The ENABLE input provides logic level control of the primary output. With the primary output disabled, quiescent current drain is typically $100 \mu \mathrm{~A}$ when supplying $100 \mu \mathrm{~A}$ from the secondary output.

The CS8481 is extremely robust with protection provided for reverse battery, short circuit, overvoltage, and overtemperature on both outputs.

The CS8481 is available in a 5 -lead $\mathrm{D}^{2} \mathrm{PAK}$.

## Features

- $3.3 \mathrm{~V} / 250 \mathrm{~mA}$ Primary Output
- $5.0 \mathrm{~V} / 100 \mathrm{~mA}$ Secondary Output
- 3.0\% Tolerance, Both Outputs
- ON/OFF Control for Primary Output
- Low Quiescent Current Drain ( $100 \mu \mathrm{~A} \mathrm{~V}_{\mathrm{OUT} 2}$ )
- Low Reverse Current
- Protection Features
- Reverse Battery (-15 V)
- 74 V Peak Transient Voltage
- Short Circuit
- Overtemperature
- Overvoltage (34 V)

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAM

$\mathrm{Tab}=\mathrm{GND}$
Pin 1. $V_{I N}$
2. $\mathrm{V}_{\mathrm{OUT} 1}$
3. GND
4. V OUT2
5. ENABLE

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
ORDERING INFORMATION*

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS8481YDP5 | D2PAK, <br> 5-PIN | 50 Units/Rail |
| CS8481YDPR5 | D2PAK, <br> 5-PIN | 750 Tape \& Reel |

*Consult your local sales representative for SO-8, SO-16, DIP-8, DIP-16, TO-220 FIVE LEAD, and D$^{2}$ PAK 7-PIN packaging options.


Figure 1. Block Diagram

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage ( $\mathrm{V}_{\text {IN }}$ ) | Operating Range Reverse Battery Peak Transient Voltage ( 60 V Load Dump @ $14 \mathrm{~V} \mathrm{~V}_{\mathrm{IN}}$ ) | $\begin{gathered} 30 \\ -15 \\ 74 \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { V } \\ & \text { V } \end{aligned}$ |
| ENABLE |  | 10 | V |
| Power Dissipation |  | Internally Limited | - |
| Maximum Junction Temperature |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Electrostatic Discharge (Human Body Model) |  | 4.0 | kV |
| Lead Temperature Soldering | Reflow (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

## CS8481

ELECTRICAL CHARACTERISTICS: $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$, I OUT1 $1=\mathrm{I}_{\text {OUT } 2}=100 \mu \mathrm{~A},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$,
$-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq 125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Primary Output Stage ( $\mathrm{V}_{\text {OUT } 1}$ ) |  |  |  |  |  |
| Output Voltage, V ${ }_{\text {OUT1 }}$ | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT } 1} \leq 250 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Load Regulation | $1.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT } 1} \leq 250 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Quiescent Current | ENABLE $=\mathrm{HIGH}, \mathrm{V}_{\text {IN }}=16 \mathrm{~V}, \mathrm{I}_{\text {OUT } 1}=250 \mathrm{~mA}$ | - | 22 | 50 | mA |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$, $\mathrm{l}_{\text {OUT } 1}=125 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |
| Current Limit | $9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | 260 | 400 | - | mA |
| Short Circuit Current Limit | $\mathrm{V}_{\text {OUT1 }}=0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=16 \mathrm{~V}$ | 25 | - | - | mA |
| Reverse Current | $\mathrm{V}_{\text {OUT } 1}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 1500 | $\mu \mathrm{A}$ |

Secondary Output (VOUT2)

| Output Voltage, (V ${ }_{\text {OUT2 }}$ ) | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT2 }} \leq 100 \mathrm{~mA}$ | 4.85 | 5.00 | 5.15 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\begin{aligned} & \text { IOUT2 }=100 \mathrm{~mA} \\ & \text { lout2 }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Load Regulation | $100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT2 }} \leq 100 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=14 \mathrm{~V}$ | - | 5.0 | 50 | mV |
| Quiescent Current | $\begin{aligned} & \text { ENABLE }=\mathrm{LOW}, \mathrm{~V}_{\text {IN }}=12.8 \mathrm{~V} \\ & \text { ENABLE }=\mathrm{HIGH}, \mathrm{~V}_{\mathrm{IN}}=16 \mathrm{~V}, \mathrm{I} \text { OUT2 }=100 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 100 \\ & 8.0 \end{aligned}$ | $\begin{gathered} 150 \\ 30 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| Ripple Rejection | $\mathrm{f}=120 \mathrm{~Hz}$; lout2 $=10 \mathrm{~mA}, 7.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 17 \mathrm{~V}$ | 60 | 70 | - | dB |
| Current Limit | $9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | 105 | 200 | - | mA |
| Short Circuit Current Limit | $\mathrm{V}_{\text {OUT2 }}=0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=16 \mathrm{~V}, \mathrm{l}_{\text {OUT1 }}=0 \mathrm{~A}$ | 25 | - | - | mA |
| Reverse Current | $\mathrm{V}_{\text {OUT2 }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=0 \mathrm{~V}$ | - | 100 | 250 | $\mu \mathrm{A}$ |

ENABLE Function (ENABLE)

| Input Threshold | ENABLE $=\mathrm{LOW}, 6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | - | 1.2 | 0.8 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | ENABLE $=\mathrm{HIGH}, 6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | 2.0 | 1.2 | - | V |
| Input Bias Current | $0 \mathrm{~V} \leq \mathrm{V}_{\text {ENABLE }} \leq 5.0 \mathrm{~V}$ | -2.0 | 0 | 2.0 | $\mu \mathrm{~A}$ |

## Protection Circuits

| Overtemperature Threshold | Note 2 | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Overvoltage Shutdown | - | 30 | 34 | 38 | V |

2. Guaranteed by Design.

## PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :---: |
| D2PAK, 5-PIN | LEAD SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{IN}}$ | Supply voltage to IC, usually direct from battery. |
| 2 | $\mathrm{V}_{\text {OUT1 }}$ | 3.3 V regulated output which is activated by ENABLE input. |
| 3 | GND | Ground connection. |
| 4 | $V_{\text {OUT2 }}$ | Standby output 5.0 V, 100 mA capability; always on. |
| 5 | ENABLE | CMOS compatible input lead; switches $\mathrm{V}_{\text {OUT1 }}$. When ENABLE is high, $\mathrm{V}_{\text {OUT } 1}$ is active. |

## DEFINITION OF TERMS

Current Limit - Peak current that can be delivered to the output.

Dropout Voltage - The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Output Differential - The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Input Voltage - The DC voltage applied to the input terminals with respect to ground.

Line Regulation - The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation - The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability - Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Quiescent Current - The part of the positive input current that does not contribute to the positive load current, i.e., the regulator ground lead current.

Ripple Rejection - The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.
Short Circuit Current Limit - Peak current that can be delivered by the outout when forced to 0 V .

Temperature Stability of Vout - The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.


Figure 2. Typical Circuit Waveform

## APPLICATION NOTES

## General

The CS8481 is a micropower dual regulator. All bias required to operate the internal circuitry is derived from the standby output, $\mathrm{V}_{\text {OUT2 }}$. If this output experiences an over current situation and collapses, then VOUT1 will also collapse (see Figure 2).

If there is critical circuitry that must remain active under most conditions it should be connected to VOUT2. Any circuitry that is likely to be subjected to a short circuit, e.g., circuitry outside the module, should be connected to $V_{\text {OUT1 }}$.

## External Capacitors

Output capacitors are required for stability with the CS8481. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability.

Worst-case is determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.
Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to $-40^{\circ} \mathrm{C}$, capacitors rated at that temperature must be used.
More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, "Compensation for Linear Regulators," document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## ENABLE

The ENABLE function controls V OUT1. When ENABLE is high, V VUT1 is on. When ENABLE is low, $V_{\text {OUT1 }}$ is off.

## Calculating Power Dissipation in a <br> Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 3) is
$\mathrm{P}_{\mathrm{D}(\text { max })}=\left\{\mathrm{V}_{\mathrm{IN}(\text { max })}-\mathrm{VOUT1}^{(\text {min })}\right)_{\text {IOUT1 }}($ max $)+$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT1(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT1 }}$,
$\mathrm{V}_{\text {OUT2(min) }}$ is the minimum output voltage from $\mathrm{V}_{\text {OUT2 }}$,
IOUT1(max) is the maximum output current, for the application,
IOUT2(max) is the maximum output current, for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at both IOUT1(max) and IOUT2(max).

Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta J A}$ can be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 3. Dual Output Regulator With Key Performance Parameters Labeled.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JIC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.


[^17]Figure 4. Test \& Application Circuit

## CS8481

PACKAGE THERMAL DATA

| Parameter |  | D $^{2}$ PAK, 5-PIN | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 2.4 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | $10-50^{*}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

* Depending on thermal properties of substrate. $\mathrm{R}_{\Theta \mathrm{JA}}=\mathrm{R}_{\Theta \mathrm{JC}}+\mathrm{R}_{\Theta \mathrm{CA}}$


## Advance Information <br> Micropower 150 mA LDO Linear Regulators with ENABLE, Delay, RESET, and Monitor Flag

The NCV8501 is a family of precision micropower voltage regulators. Their output current capability is 150 mA . The family has output voltage options for adjustable, $2.5 \mathrm{~V}, 3.3 \mathrm{~V}, 5.0 \mathrm{~V}, 8.0 \mathrm{~V}$, and 10 V .

The output voltage is accurate within $\pm 2.0 \%$ with a maximum dropout voltage of 0.6 V at 150 mA . Low quiescent current is a feature drawing only $70 \mu \mathrm{~A}$ with a $100 \mu \mathrm{~A}$ load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active $\overline{\text { RESET (with }}$ DELAY), and a flag monitor which can be used to provide an early warning signal to the microprocessor of a potential impending $\overline{\text { RESET }}$ signal. The use of the flag monitor allows the microprocessor to finish any signal processing before the $\overline{\text { RESET }}$ shuts the microprocessor down.

The active $\overline{\text { RESET }}$ circuit includes hysteresis, and operates correctly at an output voltage as low as 1.0 V . The RESET function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

## Features

- Output Voltage Options: Adjustable, 2.5 V, 3.3 V, 5.0 V, 8.0 V, 10 V
- $\pm 2.0 \%$ Output
- Low $70 \mu \mathrm{~A}$ Quiescent Current
- Fixed or Adjustable Output Voltage
- Active RESET
- ENABLE
- 150 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage
- -15 V Reverse Voltage
- Short Circuit
- Thermal Overload
- Early Warning through $\overline{\text { FLAG }} /$ MON Leads


[^18]
## NCV8501 Series

## PIN CONNECTIONS, ADJUSTABLE OUTPUT



PIN CONNECTIONS, FIXED OUTPUT


Figure 1. Application Diagram

MAXIMUM RATINGS* $\dagger$

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IN }}$ (DC) |  | -15 to 45 | V |
| Peak Transient Voltage (46 V Load Dump @ V ${ }_{\text {IN }}=14 \mathrm{~V}$ ) |  | 60 | V |
| Operating Voltage |  | 45 | V |
| Input Voltage Range ( $\overline{\text { RESET, }}$ FLAG ) |  | -0.3 to 10 | V |
| Input Voltage Range (MON) |  | -0.3 to 45 | V |
| Input Voltage Range (ENABLE) |  | 60 | V |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Junction Temperature, $\mathrm{T}_{J}$ |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature, $\mathrm{T}_{\mathrm{S}}$ |  | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance, SO-8: Junction-to-Case, R ®Jc Junction-to-Ambient, R ®JA |  | $\begin{gathered} 45 \\ 165 \end{gathered}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, SO-14: Junction-to-Case, R өJc Junction-to-Ambient, $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{gathered} 30 \\ 115 \end{gathered}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, SOW-16 E PAD: <br> Junction-to-Case, R ®Jc <br> Junction-to-Ambient, R ®JA |  | $\begin{aligned} & 1.0 \\ & 36 \end{aligned}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
$\dagger$ During the voltage range which exceeds the maximum tested voltage of $\mathrm{V}_{\mathbf{I N}}$, operation is assured, but not specified. Wider limits may apply.
Thermal dissipation must be observed closely.
ELECTRICAL CHARACTERISTICS (lout $=1.0 \mathrm{~mA}$, ENABLE $=\mathrm{TBD},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$;
unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Output Voltage for 2.5 V Option $\left(4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 6.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 4.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 2.450 \\ & 2.425 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 2.550 \\ & 2.575 \end{aligned}$ | $\begin{aligned} & \text { v } \\ & \text { V } \end{aligned}$ |
| Output Voltage for 3.3 V Option $\left(4.5 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 7.3 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 4.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 3.234 \\ & 3.201 \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 3.3 \end{aligned}$ | $\begin{aligned} & 3.366 \\ & 3.399 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Output Voltage for 5.0 V Option $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 6.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.90 \\ & 4.85 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 5.10 \\ & 5.15 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Output Voltage for 8.0 V Option $\left(9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 12 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 7.84 \\ & 7.76 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 8.16 \\ & 8.24 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Output Voltage for 10 V Option $\left(11 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 14 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 11 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 9.8 \\ & 9.7 \end{aligned}$ | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | $\begin{aligned} & 10.2 \\ & 10.3 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) (5.0 V, 8.0 V, 10 V Options Only) | $\begin{aligned} & \text { I OUT }=150 \mathrm{~mA} \\ & \text { IOUT }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 5.0 \mathrm{~mA} \leq \mathrm{l}_{\text {OUT }} \leq 150 \mathrm{~mA}$ | - | 5.0 | 30 | mV |
| Line Regulation | [ $\mathrm{V}_{\text {OUT }}($ (typ $\left.)+1.0\right]<\mathrm{V}<26 \mathrm{~V}$, I IUT $=1.0 \mathrm{~mA}$ | - | 5.0 | 40 | mV |
| Quiescent Current, (IQ) Active Mode | $\begin{aligned} & \text { Iout }=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {IN }}=12 \mathrm{~V}, \text { Delay }=3.0 \mathrm{~V}, \mathrm{MON}=3.0 \mathrm{~V} \\ & \text { IOUT }=75 \mathrm{~mA}, \text { Delay }=3.0 \mathrm{~V}, \mathrm{MON}=3.0 \mathrm{~V} \\ & \text { IOUT } \leq 150 \mathrm{~mA} \text {, Delay }=3.0 \mathrm{~V}, \mathrm{MON}=3.0 \mathrm{~V} \end{aligned}$ | - | $\begin{aligned} & 70 \\ & 6.0 \\ & 12 \end{aligned}$ | $\begin{gathered} \text { TBD } \\ 9.0 \\ 19 \end{gathered}$ | $\mu \mathrm{A}$ <br> mA <br> mA |
| Quiescent Current, (IQ) Sleep Mode | ENABLE $=0 \mathrm{~V}$ | - | 12 | 25 | $\mu \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS (continued) (Iout $=1.0 \mathrm{~mA}$, ENABLE $=$ TBD, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Current Limit | - | 160 | 300 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 40 | 190 | - | mA |
| Thermal Shutdown | (Guaranteed by Design) | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |

## Reset Function (RESET)

| RESET Threshold for 2.5 V Option $\mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right)$ <br> LOW ( $\mathrm{V}_{\mathrm{RL}}$ ) | $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$ (Note 2) <br> $V_{\text {OUT }}$ Increasing <br> $\mathrm{V}_{\text {OUT }}$ Decreasing | $\begin{aligned} & 2.225 \\ & 2.200 \end{aligned}$ | $\begin{aligned} & 2.350 \\ & 2.300 \end{aligned}$ | $\begin{aligned} & 2.475 \\ & 2.400 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ```RESET Threshold for 3.3 V Option HIGH ( \(\mathrm{V}_{\mathrm{RH}}\) ) LOW ( \(\mathrm{V}_{\mathrm{RL}}\) )``` | $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$ (Note 2) <br> $V_{\text {OUT }}$ Increasing <br> $\mathrm{V}_{\text {OUT }}$ Decreasing | $\begin{aligned} & 2.937 \\ & 2.904 \end{aligned}$ | $\begin{aligned} & 3.102 \\ & 3.036 \end{aligned}$ | $\begin{aligned} & 3.267 \\ & 3.168 \end{aligned}$ | V |
| RESET Threshold for 5.0 V Option $\mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right)$ $\operatorname{LOW}\left(\mathrm{V}_{\mathrm{RL}}\right)$ | $V_{\text {OUT }}$ Increasing <br> $V_{\text {OUT }}$ Decreasing | $\begin{aligned} & 4.45 \\ & 4.40 \end{aligned}$ | $\begin{aligned} & 4.70 \\ & 4.60 \end{aligned}$ | $\begin{aligned} & 4.95 \\ & 4.80 \end{aligned}$ | V |
| RESET Threshold for 8.0 V Option $\begin{aligned} & \mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right) \\ & \operatorname{LOW}\left(\mathrm{V}_{\mathrm{RL}}\right) \end{aligned}$ | $V_{\text {OUT }}$ Increasing <br> $V_{\text {OUT }}$ Decreasing | $\begin{aligned} & 7.12 \\ & 7.04 \end{aligned}$ | $\begin{aligned} & 7.52 \\ & 7.36 \end{aligned}$ | $\begin{aligned} & 7.92 \\ & 7.68 \end{aligned}$ | V |
| RESET Threshold for 10 V Option $\begin{aligned} & \mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right) \\ & \operatorname{LOW}\left(\mathrm{V}_{\mathrm{RL}}\right) \end{aligned}$ | $V_{\text {OUT }}$ Increasing <br> $V_{\text {OUT }}$ Decreasing | $\begin{aligned} & 8.90 \\ & 8.80 \end{aligned}$ | $\begin{aligned} & 9.40 \\ & 9.20 \end{aligned}$ | $\begin{aligned} & 9.90 \\ & 9.60 \end{aligned}$ | V |
| RESET Hysteresis | (HIGH - LOW) | - | 100 | - | mV |
| Output Voltage Low (VRLO) Low ( $\left.\mathrm{V}_{\mathrm{R}(\text { PEAK })}\right)$ | $1.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{OUT}} \leq \mathrm{V}_{\mathrm{RL}}, \overline{R_{\text {RESET }}}=10 \mathrm{k}$ <br> $\mathrm{V}_{\text {OUt }}$, Power up, Power down | - | $\begin{aligned} & 0.1 \\ & 0.6 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 1.0 \end{aligned}$ | V |
| Delay Switching Threshold ( $\mathrm{V}_{\mathrm{DT}}$ ) | - | 1.4 | 1.8 | 2.2 | V |
| Reset Delay Low Voltage | $\mathrm{V}_{\text {OUT }}$ < RESET Threshold Low(min) | - | - | 0.1 | V |
| Delay Charge Current | Delay $=1.0 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}>\mathrm{V}_{\text {RH }}$ | 2.0 | 3.0 | 5.0 | $\mu \mathrm{A}$ |
| Delay Discharge Current | Delay $=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=1.5 \mathrm{~V}$ | 10 | - | - | mA |

FLAG/Monitor

| Monitor Threshold | - | TBD | 1.28 | TBD | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Hysteresis | - | 20 | 100 | 200 | mV |
| Input Current | $\mathrm{V}_{\text {MON }}=2.0 \mathrm{~V}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| Output Saturation Voltage | $\mathrm{V}_{\mathrm{MON}}=0 \mathrm{~V}, \mathrm{I}_{\text {FLAG }}=1.0 \mathrm{~mA}$ | - | 0.1 | 0.4 | V |

## Voltage Adjust (Adjustable Output only)

| Threshold |  | - | TBD | 1.28 |
| :--- | :--- | :---: | :---: | :---: |
| Input Current | SENSE $=0 \mathrm{~V}$ | - | -20 | TBD |

## ENABLE

| Input Threshold | Low <br> High | - <br> TBD | - <br> - | TBD <br> - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Current | ENABLE = 14 V | - | - | TBD | $\mu \mathrm{A}$ |

[^19]
## NCV8501 Series

PACKAGE PIN DESCRIPTION, ADJUSTABLE OUTPUT

| Package Pin Number |  |  |  |
| :---: | :---: | :---: | :--- |
| SO-8 | SOW-16 <br> E PAD | Pin Symbol |  |
| 1 | 7 |  | Input Voltage. |
| 2 | 15 | MON | Monitor. Input for early warning comparator. If not needed connect to V $_{\text {OUT. }}$ |
| 3 | 9 | ENABLE | ENABLE control for the IC. A high powers the device up. |
| 4 | $3-6,8$, <br> $10-12,14$ | NC | No connection. |
| 5 | 13 | GND | Ground. All GND leads must be connected to Ground. |
| 6 | 16 | $\overline{\text { FLAG }}$ | Open collector output from early warning comparator. |
| 7 | 1 | V $_{\text {ADJ }}$ | Voltage Adjust. A resistor divider from $\mathrm{V}_{\text {OUT }}$ to this lead sets the output voltage. |
| 8 | 2 | V $_{\text {OUT }}$ | $\pm 2.0 \%, 150 \mathrm{~mA}$ output. |

NOTE: Tentative pinout for SOW-16 E Pad.

## PACKAGE PIN DESCRIPTION, FIXED OUTPUT

| Package Pin Number |  |  |  | Function |
| :---: | :---: | :---: | :---: | :---: |
| SO-8 | SO-14 | $\begin{gathered} \text { SOW-16 } \\ \text { E PAD } \end{gathered}$ | Pin Symbol |  |
| 1 | 13 | 7 | $\mathrm{V}_{\mathrm{IN}}$ | Input Voltage. |
| 2 | 14 | 8 | MON | Monitor. Input for early warning comparator. If not needed connect to $\mathrm{V}_{\text {OUT }}$. |
| 3 | 6 | 9 | ENABLE | ENABLE control for the IC. A high powers the device up. |
| 4 | 2 | 10 | DELAY | Timing capacitor for RESET function. |
| 5 | 11 | 13 | GND | Ground. All GND leads must be connected to Ground. |
| 6 | 7 | 16 | RESET | Active reset (accurate to $\mathrm{V}_{\text {OUT }} \geq 1.0 \mathrm{~V}$ ) |
| 7 | 8 | 1 | FLAG | Open collector output from early warning comparator. |
| 8 | 9 | 2 | V OUT | $\pm 2.0 \%, 150 \mathrm{~mA}$ output. |
| - | $\begin{gathered} 1,3-5,10 \\ 12 \end{gathered}$ | $\begin{gathered} 3-6,11, \\ 12,14,15 \end{gathered}$ | NC | No connection. |

NOTE: Tentative pinouts for SO-14 and SOW-16 E Pad. 5.0 V option only for SO-14.


Figure 2. Block Diagram

## CIRCUIT DESCRIPTION

## REGULATOR CONTROL FUNCTIONS

The NCV8501 contains the microprocessor compatible control function $\overline{\text { RESET }}$ (Figure 3).


Figure 3. Reset and Delay Circuit Wave Forms

## RESET Function

A $\overline{\text { RESET }}$ signal (low voltage) is generated as the IC powers up until $\mathrm{V}_{\text {OUT }}$ is within $6.0 \%$ of the regulated output voltage, or when V VUT drops out of regulation, and is lower than $8.0 \%$ below the regulated output voltage. Hysteresis is included in the function to minimize oscillations.

The $\overline{\text { RESET }}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text { RESET }}$ signal is valid for $\mathrm{V}_{\text {OUT }}$ as low as 1.0 V .

## ENABLE Function

The part stays in a low $\mathrm{I}_{\mathrm{Q}}$ sleep mode when the ENABLE pin is held low. The part has an internal pull down if the pin is left floating. This is intended for failure modes only. An external connection (active pulldown, resistor, or switch) for normal operation is recommended.

The integrity of the ENABLE pin allows it to be tied directly to the battery line. It will withstand load dump potentials.


Figure 4. ENABLE Function

## Delay Function

The reset delay circuit provides a programmable (by an external capacitor) delay on the RESET output lead. The delay lead provides source current (typically $3.0 \mu \mathrm{~A}$ ) to the external delay capacitor only when the output voltage, $V_{\text {OUT }}$, has dropped below the reset threshold. Otherwise, the delay pin is always grounded through an internal NPN. If reset delay is not needed, this pin should be left open.

## FLAG/Monitor Function

An on-chip comparator is provided to perform an early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the FLAG pin
will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the bandgap reference. The actual trip point can be programmed externally using a resistor divider to the input monitor (MON) (Figure 5).


Figure 5. Flag/Monitor Function

## Voltage Adjust

Figure 6 shows the device setup for a user configurable output voltage. The feedback to the $\mathrm{V}_{\mathrm{ADJ}}$ pin is taken from a voltage divider referenced to the output voltage. The loop is balanced around the SENSE threshold (1.28 V typical).


Figure 6. Adjustable Output Voltage

## APPLICATION NOTES

## FLAG MONITOR

Figure 7 shows the FLAG Monitor waveforms as a result of the circuit depicted in Figure 5. As the input voltage falls $\left(\mathrm{V}_{\mathrm{IN}}\right)$, the Monitor threshold is crossed. This causes the voltage on the FLAG output to go low sending a warning signal to the microprocessor that a RESET signal may occur in a short period of time. TWARNING is the time the microprocessor has to complete the function it is currently working on and get ready for the $\overline{\text { RESET }}$ shutdown signal.


Figure 7. FLAG Monitor Circuit Waveform

## SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$
\text { tDELAY }=\frac{\left[\text { CDELAY }\left(\mathrm{V}_{\mathrm{dt}}-\text { Reset Delay Low Voltage }\right)\right]}{\text { Delay Charge Current }}
$$

Example:
Using C $_{\text {DELAY }}=33 \mathrm{nF}$.
Assume reset Delay Low Voltage $=0$.
Use the typical value for $\mathrm{V}_{\mathrm{dt}}=1.8 \mathrm{~V}$.
Use the typical value for Delay Charge Current $=3.0 \mu \mathrm{~A}$.

$$
\text { tDELAY }=\frac{[33 \mathrm{nF}(1.8-0)]}{3.0 \mu \mathrm{~A}}=19.8 \mathrm{~ms}
$$

## STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor Cout shown in Figure 8 should work for most applications, however it is not necessarily the optimized solution.

${ }^{*} \mathrm{C}_{\text {IN }}$ required if regulator is located far from the power supply filter
${ }^{* *}$ Cout required for stability. Capacitor must operate at minimum temperature expected

Figure 8. Test and Application Circuit Showing Output Compensation

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 9) is:

$$
\begin{align*}
\mathrm{PD}(\max )= & {\left[V \operatorname{IN}(\max )-\mathrm{VOUT}^{\text {min })}\right] \operatorname{IOUT}(\max ) }  \tag{1}\\
& +\mathrm{V}_{\operatorname{IN}(\max )} \mathrm{I} \mathrm{Q}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT }(\mathrm{min})}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at
$I_{O U T(m a x)}$.
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta J A}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 9. Single Output Regulator with Key Performance Parameters Labeled

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JJC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

NCV8501 Series

ORDERING INFORMATION

| Device | Output Voltage | Package | Shipping |
| :---: | :---: | :---: | :---: |
| NCV8501DADJ | Adjustable | SO-8 | 95 Units/Rail |
| NCV8501DADJR2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8501PDWADJ |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8501PDWADJR2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8501D25 | 2.5 V | SO-8 | 95 Units/Rail |
| NCV8501D25R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8501PDW25 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8501PDW25R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8501D33 | 3.3 V | SO-8 | 95 Units/Rail |
| NCV8501D33R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8501PDW33 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8501PDW33R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8501D50 | 5.0 V | SO-8 | 95 Units/Rail |
| NCV8501D50R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8501PDW50 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8501PDW50R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8501PD50 |  | SO-14 | 55 Units/Rail |
| NCV8501PD50R2 |  | SO-14 | 2500 Tape \& Reel |
| NCV8501D80 | 8.0 V | SO-8 | 95 Units/Rail |
| NCV8501D80R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8501PDW80 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8501PDW80R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8501D100 | 10 V | SO-8 | 95 Units/Rail |
| NCV8501D100R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8501PDW100 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8501PDW100R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |

## NCV8501 Series

## MARKING DIAGRAMS



| SO－14 | SOW－16 <br> E PAD |
| :---: | :---: |
|  | 16 |
| NCV8501x <br> AWLYWW | AHA日ABA |
| $\underset{1}{0} \begin{aligned} & 0 \\ & 1 \end{aligned}$ | O AWLYYWW |
|  | 日晫晫昭 <br> 1 |


| x |  |
| :---: | :---: |
| A | ＝Assembly Location |
| WL，L | ＝Wafer Lot |
| YY，Y | ＝Year |
| WW，W | ＝Work Week |

## NCV8502 Series

## Advance Information Micropower 150 mA LDO Linear Regulators with Delay, Adjustable RESET, and Monitor Flag

The NCV8502 is a family of precision micropower voltage regulators. Their output current capability is 150 mA . The family has output voltage options for adjustable, $2.5 \mathrm{~V}, 3.3 \mathrm{~V}, 5.0 \mathrm{~V}, 8.0 \mathrm{~V}$, and 10 V .

The output voltage is accurate within $\pm 2.0 \%$ with a maximum dropout voltage of 0.6 V at 150 mA . Low quiescent current is a feature drawing only $70 \mu \mathrm{~A}$ with a $100 \mu \mathrm{~A}$ load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active $\overline{\text { RESET (with }}$ DELAY), and a flag monitor which can be used to provide an early warning signal to the microprocessor of a potential impending $\overline{\text { RESET }}$ signal. The use of the flag monitor allows the microprocessor to finish any signal processing before the $\overline{\text { RESET }}$ shuts the microprocessor down.

The active $\overline{\text { RESET }}$ circuit includes hysteresis, and operates correctly at an output voltage as low as 1.0 V . The RESET function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of external resistor divider to $\mathrm{R}_{\mathrm{ADJ}}$ lead.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

## Features

- Output Voltage Options: Adjustable, 2.5 V, 3.3 V, 5.0 V, 8.0 V, 10 V
- $\pm 2.0 \%$ Output
- Low $70 \mu \mathrm{~A}$ Quiescent Current
- Fixed or Adjustable Output Voltage
- Active RESET
- Adjustable Reset
- 150 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage
-     - 15 V Reverse Voltage
- Short Circuit
- Thermal Overload
- Early Warning through $\overline{\text { FLAG/MON Leads }}$



## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 943 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 944 of this data sheet.


## ON Semiconductor ${ }^{\text {w }}$

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D SUFFIX
CASE 751

SO-14
PD SUFFIX
CASE 751A

SOIC 16 LEAD
WIDE BODY
EXPOSED PAD
DW SUFFIX
CASE 751R

[^20]
## NCV8502 Series

## PIN CONNECTIONS, ADJUSTABLE OUTPUT




PIN CONNECTIONS, FIXED OUTPUT


SO-14


SOW-16 E PAD



Figure 1. Application Diagram

MAXIMUM RATINGS＊$\dagger$

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IN}}$（DC） |  | －15 to 45 | V |
| Peak Transient Voltage（46 V Load Dump＠V ${ }_{\text {IN }}=14 \mathrm{~V}$ ） |  | 60 | V |
| Operating Voltage |  | 45 | V |
| Input Voltage Range（ $\overline{\text { RESET，}}$ FLAG ） |  | －0．3 to 10 | V |
| Input Voltage Range（MON，V ${ }_{\text {ADJ }}$ ） |  | －0．3 to 45 | V |
| ESD Susceptibility（Human Body Model） |  | 2.0 | kV |
| Junction Temperature， $\mathrm{T}_{J}$ |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature， $\mathrm{T}_{S}$ |  | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ```Package Thermal Resistance, SO-8: Junction-to-Case, R⿴囗⿱一𫝀口 Junction-to-Ambient, R⿴囗⿱一𫝀口A``` |  | $\begin{gathered} 45 \\ 165 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance，SO－14： <br> Junction－to－Case，R QJC <br> Junction－to－Ambient，R $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{gathered} 30 \\ 115 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance，SOW－16 E PAD： <br> Junction－to－Case，R $\mathrm{R}_{\theta \mathrm{J}}$ <br> Junction－to－Ambient，R $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{aligned} & 1.0 \\ & 36 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering： | Reflow：（SMD styles only）（Note 1） | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1． 60 second maximum above $183^{\circ} \mathrm{C}$ ．
＊The maximum package power dissipation must be observed．
$\dagger$ During the voltage range which exceeds the maximum tested voltage of $\mathrm{V}_{\mathbb{N}}$ ，operation is assured，but not specified．Wider limits may apply． Thermal dissipation must be observed closely．

ELECTRICAL CHARACTERISTICS（lout $=1.0 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$ ；
unless otherwise specified．）

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Output Voltage for 2．5 V Option $\left(4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 6.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 4.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 2.450 \\ & 2.425 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 2.550 \\ & 2.575 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Output Voltage for 3．3 V Option $\left(4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 7.3 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 4.5 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 3.234 \\ & 3.201 \end{aligned}$ | $\begin{aligned} & 3.3 \\ & 3.3 \end{aligned}$ | $\begin{aligned} & 3.366 \\ & 3.399 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Output Voltage for 5.0 V Option $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 6.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 4.90 \\ & 4.85 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 5.10 \\ & 5.15 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Output Voltage for 8.0 V Option $\left(9.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 12 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 9.0 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{I} \leq \mathrm{IOUT} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 7.84 \\ & 7.76 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 8.16 \\ & 8.24 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Output Voltage for 10 V Option $\left(11 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right)$ | $\begin{aligned} & 14 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \\ & 11 \mathrm{~V}<\mathrm{V}_{\text {IN }}<16 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 9.8 \\ & 9.7 \end{aligned}$ | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | $\begin{aligned} & 10.2 \\ & 10.3 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Dropout Voltage（ $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ） <br> （5．0 V，8．0 V， 10 V Options Only） | $\begin{aligned} & \text { IOUT }=150 \mathrm{~mA} \\ & \text { IOUT }=100 \mu \mathrm{~A} \end{aligned}$ | - | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 5.0 \mathrm{~mA} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA}$ | － | 5.0 | 30 | mV |
| Line Regulation | ［ $\mathrm{V}_{\text {OUT }}($ typ $\left.)+1.0\right]<\mathrm{V}<26 \mathrm{~V}$ ，I $\mathrm{IOUT}=1.0 \mathrm{~mA}$ | － | 5.0 | 40 | mV |
| Quiescent Current，（IQ） Active Mode | $\begin{aligned} & \text { lout }=100 \mu \mathrm{~A}, \mathrm{~V}_{\text {IN }}=12 \mathrm{~V} \text {, Delay }=3.0 \mathrm{~V}, \mathrm{MON}=3.0 \mathrm{~V} \\ & \text { lout }=75 \mathrm{~mA} \text {, Delay }=3.0 \mathrm{~V}, \mathrm{MON}=3.0 \mathrm{~V} \\ & \text { lout } \leq 150 \mathrm{~mA}, \text {, Delay }=3.0 \mathrm{~V}, \mathrm{MON}=3.0 \mathrm{~V} \end{aligned}$ | - | $\begin{aligned} & 70 \\ & 6.0 \\ & 12 \end{aligned}$ | $\begin{gathered} \text { TBD } \\ 9.0 \\ 19 \end{gathered}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |

ELECTRICAL CHARACTERISTICS (continued) (lout $=1.0 \mathrm{~mA},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Current Limit | - | 160 | 300 | - | mA |
| Short Circuit Output Current | $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ | 40 | 190 | - | mA |
| Thermal Shutdown | (Guaranteed by Design) | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |

Reset Function (RESET)

| RESET Threshold for 2.5 V Option $\mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right)$ $\text { LOW ( } \mathrm{V}_{\mathrm{RL}} \text { ) }$ | $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V} \text { (Note 2) }$ <br> $V_{\text {OUT }}$ Increasing <br> $\mathrm{V}_{\text {OUT }}$ Decreasing | $\begin{aligned} & 2.225 \\ & 2.200 \end{aligned}$ | $\begin{aligned} & 2.350 \\ & 2.300 \end{aligned}$ | $\begin{aligned} & 2.475 \\ & 2.400 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\overline{\text { RESET Threshold for 3.3 } \mathrm{V} \text { Option }}$ $\mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right)$ $\text { LOW }\left(\mathrm{V}_{\mathrm{RL}}\right)$ | $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$ (Note 2) <br> $V_{\text {OUT }}$ Increasing <br> $\mathrm{V}_{\text {OUT }}$ Decreasing | $\begin{aligned} & 2.937 \\ & 2.904 \end{aligned}$ | $\begin{aligned} & 3.102 \\ & 3.036 \end{aligned}$ | $\begin{aligned} & 3.267 \\ & 3.168 \end{aligned}$ | V |
| $\overline{\text { RESET Threshold for 5.0 } \mathrm{V} \text { Option }}$ $\mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right)$ $\text { LOW }\left(\mathrm{V}_{\mathrm{RL}}\right)$ | $V_{\text {OUT }}$ Increasing <br> Vout Decreasing | $\begin{aligned} & 4.45 \\ & 4.40 \end{aligned}$ | $\begin{aligned} & 4.70 \\ & 4.60 \end{aligned}$ | $\begin{aligned} & 4.95 \\ & 4.80 \end{aligned}$ | V |
| RESET Threshold for 8.0 V Option $\mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right)$ $\text { LOW ( } \left.\mathrm{V}_{\mathrm{RL}}\right)$ | $V_{\text {OUT }}$ Increasing <br> $V_{\text {OUT }}$ Decreasing | $\begin{aligned} & 7.12 \\ & 7.04 \end{aligned}$ | $\begin{aligned} & 7.52 \\ & 7.36 \end{aligned}$ | $\begin{aligned} & 7.92 \\ & 7.68 \end{aligned}$ | V |
| RESET Threshold for 10 V Option $\begin{aligned} & \mathrm{HIGH}\left(\mathrm{~V}_{\mathrm{RH}}\right) \\ & \operatorname{LOW}\left(\mathrm{V}_{\mathrm{RL}}\right) \end{aligned}$ | $V_{\text {OUt }}$ Increasing <br> $V_{\text {OUT }}$ Decreasing | $\begin{aligned} & 8.90 \\ & 8.80 \end{aligned}$ | $\begin{aligned} & 9.40 \\ & 9.20 \end{aligned}$ | $\begin{aligned} & 9.90 \\ & 9.60 \end{aligned}$ | V |
| RESET Hysteresis | (HIGH - LOW) | - | 100 | - | mV |
| Output Voltage Low (VRLO) Low ( $\left.\mathrm{V}_{\mathrm{R}(\text { PEAK })}\right)$ | $1.0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq \mathrm{V}_{\mathrm{RL}}, \overline{\mathrm{R}_{\text {RESET }}}=10 \mathrm{k}$ Vout, Power up, Power down | - | $\begin{aligned} & 0.1 \\ & 0.6 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 1.0 \end{aligned}$ | V |
| Delay Switching Threshold (V $\mathrm{V}_{\text {DT }}$ ) | - | 1.4 | 1.8 | 2.2 | V |
| Reset Delay Low Voltage | $\mathrm{V}_{\text {OUT }}$ < RESET Threshold Low(min) | - | - | 0.1 | V |
| Delay Charge Current | Delay $=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}>\mathrm{V}_{\text {RH }}$ | 2.0 | 3.0 | 5.0 | $\mu \mathrm{A}$ |
| Reset Adjust Switching Voltage $\left.\left(\mathrm{V}_{\mathrm{R}(\mathrm{ADJ}}\right)\right)$ | - | TBD | 1.28 | TBD | V |
| Delay Discharge Current | Delay $=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=1.5 \mathrm{~V}$ | 10 | - | - | mA |

## FLAG/Monitor

| Monitor Threshold | - | TBD | 1.28 | TBD | V |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Hysteresis |  | - | 20 | 100 | 200 | mV |
| Input Current | $\mathrm{V}_{\text {MON }}=2.0 \mathrm{~V}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{~A}$ |  |
| Output Saturation Voltage | $\mathrm{V}_{\text {MON }}=0 \mathrm{~V}, \mathrm{I}_{\text {FLAG }}=1.0 \mathrm{~mA}$ | - | 0.1 | 0.4 | V |  |

## Voltage Adjust (Adjustable Output only)

| Threshold | - | TBD | 1.28 | TBD | V |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Input Current | SENSE $=0 \mathrm{~V}$ | - | -20 | TBD | $\mu \mathrm{A}$ |

[^21]
## NCV8502 Series

## PACKAGE PIN DESCRIPTION, ADJUSTABLE OUTPUT

| Package Pin Number |  |  |  |
| :---: | :---: | :---: | :--- |
| SO-8 | SOW-16 <br> E PAD | Pin Symbol |  |
| 1 | 7 |  | Input Voltage. |
| 2 | 15 | MON | Monitor. Input for early warning comparator. If not needed connect to $V_{\text {OUT. }}$ |
| 3,4 | $3-6,8-12$, <br> 14 | NC | No connection. |
| 5 | 13 | GND | Ground. All GND leads must be connected to Ground. |
| 6 | 16 | FLAG | Open collector output from early warning comparator. |
| 7 | 1 | V $_{\text {ADJ }}$ | Voltage Adjust. A resistor divider from $\mathrm{V}_{\text {OUT }}$ to this lead sets the output voltage. |
| 8 | 2 | V OUT | $\pm 2.0 \%, 150 \mathrm{~mA}$ output. |

NOTE: Tentative pinout for SOW-16 E Pad.

## PACKAGE PIN DESCRIPTION, FIXED OUTPUT

| Package Pin Number |  |  |  | Function |
| :---: | :---: | :---: | :---: | :---: |
| SO-8 | SO-14 | SOW-16 <br> E PAD | Pin Symbol |  |
| 1 | 13 | 7 | $\mathrm{V}_{\text {IN }}$ | Input Voltage. |
| 2 | 14 | 8 | MON | Monitor. Input for early warning comparator. If not needed connect to $\mathrm{V}_{\text {OUT }}$. |
| 3 | 1 | 9 | $\mathrm{R}_{\text {ADJ }}$ | Reset Adjust. If not needed connect to ground. |
| 4 | 2 | 10 | DELAY | Timing capacitor for RESET function. |
| 5 | 11 | 13 | GND | Ground. All GND leads must be connected to Ground. |
| 6 | 7 | 16 | RESET | Active reset (accurate to $\mathrm{V}_{\text {OUT }} \geq 1.0 \mathrm{~V}$ ) |
| 7 | 8 | 1 | FLAG | Open collector output from early warning comparator. |
| 8 | 9 | 2 | $\mathrm{V}_{\text {OUT }}$ | $\pm 2.0 \%, 150 \mathrm{~mA}$ output. |
| - | 3-6, 10, 12 | $\begin{gathered} 3-6,11, \\ 12,14,15 \end{gathered}$ | NC | No connection. |

NOTE: Tentative pinouts for SO-14 and SOW-16 E Pad. 5.0 V option only for SO-14.


Figure 2. Block Diagram

## CIRCUIT DESCRIPTION

## REGULATOR CONTROL FUNCTIONS

The NCV8502 contains the microprocessor compatible control function $\overline{\text { RESET }}$ (Figure 3).


Figure 3. Reset and Delay Circuit Wave Forms

## RESET Function

A $\overline{\text { RESET }}$ signal (low voltage) is generated as the IC powers up until $\mathrm{V}_{\text {OUT }}$ is within $6.0 \%$ of the regulated output voltage, or when V VUT drops out of regulation, and is lower than $8.0 \%$ below the regulated output voltage. Hysteresis is included in the function to minimize oscillations.

The $\overline{\text { RESET }}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text { RESET }}$ signal is valid for $\mathrm{V}_{\text {OUT }}$ as low as 1.0 V .

## Adjustable Reset Function

The reset threshold can be made lower by connecting an external resistor divided to the $\mathrm{R}_{\text {ADJ }}$ lead from the $\mathrm{V}_{\text {OUT }}$ lead, as displayed in Figure 4. This lead is grounded to select the default value of 4.6 V .


Figure 4. Adjustable RESET

## Delay Function

The reset delay circuit provides a programmable (by an external capacitor) delay on the RESET output lead. The delay lead provides source current (typically $3.0 \mu \mathrm{~A}$ ) to the external delay capacitor only when the output voltage, $V_{\text {OUT }}$, has dropped below the reset threshold. Otherwise, the delay pin is always grounded through an internal NPN. If reset delay is not needed, this pin should be left open.

## FLAG/Monitor Function

An on-chip comparator is provided to perform an early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with
the microprocessor. The signal received from the FLAG pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the bandgap reference. The actual trip point can be programmed externally using a resistor divider to the input monitor (MON) (Figure 5).


Figure 5. Flag/Monitor Function

## Voltage Adjust

Figure 6 shows the device setup for a user configurable output voltage. The feedback to the $\mathrm{V}_{\mathrm{ADJ}}$ pin is taken from a voltage divider referenced to the output voltage. The loop is balanced around the SENSE threshold (1.28 V typical).


Figure 6. Adjustable Output Voltage

## APPLICATION NOTES

## FLAG MONITOR

Figure 7 shows the FLAG Monitor waveforms as a result of the circuit depicted in Figure 5. As the input voltage falls $\left(\mathrm{V}_{\mathrm{IN}}\right)$, the Monitor threshold is crossed. This causes the voltage on the $\overline{\text { FLAG }}$ output to go low sending a warning signal to the microprocessor that a $\overline{\text { RESET }}$ signal may occur in a short period of time. T TWARNING is the time the microprocessor has to complete the function it is currently working on and get ready for the $\overline{\text { RESET }}$ shutdown signal.


Figure 7. FLAG Monitor Circuit Waveform

## SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$
\text { tDELAY }=\frac{\left[\text { CDELAY }\left(\mathrm{V}_{\mathrm{dt}}-\text { Reset Delay Low Voltage }\right)\right]}{\text { Delay Charge Current }}
$$

Example:
Using C $_{\text {DELAY }}=33 \mathrm{nF}$.
Assume reset Delay Low Voltage $=0$.
Use the typical value for $\mathrm{V}_{\mathrm{dt}}=1.8 \mathrm{~V}$.
Use the typical value for Delay Charge Current $=3.0 \mu \mathrm{~A}$.

$$
\text { tDELAY }=\frac{[33 \mathrm{nF}(1.8-0)]}{3.0 \mu \mathrm{~A}}=19.8 \mathrm{~ms}
$$

## STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.-40^{\circ} \mathrm{C}\right)$, both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor Cout shown in Figure 8 should work for most applications, however it is not necessarily the optimized solution.

${ }^{*} \mathrm{C}_{\text {IN }}$ required if regulator is located far from the power supply filter
${ }^{* *}$ Cout required for stability. Capacitor must operate at minimum temperature expected

Figure 8. Test and Application Circuit Showing Output Compensation

## CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 9) is:

$$
\begin{align*}
\mathrm{PD}(\max )^{=} & {\left[\mathrm{VIN}_{\operatorname{IN}(\max )}-\mathrm{VOUT}_{\mathrm{min})}\right) \operatorname{lOUT}(\max ) }  \tag{1}\\
& +\mathrm{V}_{\mathrm{IN}(\max )} \mathrm{I} \mathrm{Q}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\max )}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT }(\mathrm{min})}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at
$I_{O U T(m a x)}$.
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta J A}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta J A}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.
In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.


Figure 9. Single Output Regulator with Key Performance Parameters Labeled

## HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JJC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

## NCV8502 Series

ORDERING INFORMATION

| Device | Output Voltage | Package | Shipping |
| :---: | :---: | :---: | :---: |
| NCV8502DADJ | Adjustable | SO-8 | 95 Units/Rail |
| NCV8502DADJR2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8502PDWADJ |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8502PDWADJR2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8502D25 | 2.5 V | SO-8 | 95 Units/Rail |
| NCV8502D25R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8502PDW25 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8502PDW25R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8502D33 | 3.3 V | SO-8 | 95 Units/Rail |
| NCV8502D33R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8502PDW33 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8502PDW33R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8502D50 | 5.0 V | SO-8 | 95 Units/Rail |
| NCV8502D50R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8502PDW50 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8502PDW50R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8502PD50 |  | SO-14 | 55 Units/Rail |
| NCV8502PD50R2 |  | SO-14 | 2500 Tape \& Reel |
| NCV8502D80 | 8.0 V | SO-8 | 95 Units/Rail |
| NCV8502D80R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8502PDW80 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8502PDW80R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |
| NCV8502D100 | 10 V | SO-8 | 95 Units/Rail |
| NCV8502D100R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8502PDW100 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8502PDW100R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |

## NCV8502 Series

## MARKING DIAGRAMS


$x \quad=$ Voltage Ratings as Indicated Below:
A = Adjustable
$2=2.5 \mathrm{~V}$
$3=3.3 \mathrm{~V}$
$5=5.0 \mathrm{~V}$
$8=8.0 \mathrm{~V}$
$0=10 \mathrm{~V}$
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## NCV8508 Series

## Advance Information <br> Low Dropout Linear Regulators with Watchdog, RESET, and Wake Up

The NCV8508 is a precision micropower voltage regulator family. The part contains many of the required operational requirements for powering microprocessors. Its robustness makes it suitable for severe automotive environments. The devices low dropout voltage ensures operation of loads (i.e. microprocessors) when the battery voltage is low such as during the cranking cycle of an automobile. In addition to being a good fit for the automotive environment, the NCV8508 is ideal for use in battery operated, microprocessor controlled equipment because of its extremely low quiescent current.

## Features

- Output Voltage Options: 3.3 V or 5.0 V
- $\pm 3.0 \%$ Output Voltage
- IOUT Up to 250 mA
- Quiescent Current Independent of Load
- Micropower Compatible Control Functions:
- Wake Up
- Watchdog
- $\overline{\text { RESET }}$
- Low Dropout Voltage
- Low Quiescent Current (100 $\mu \mathrm{A}$ typ)
- Protection Features:
- Thermal Shutdown
- Short Circuit
- 45 V Operation
- Internally Fused Leads in SO-16L Package

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 954 of this data sheet.

$$
3=3.3 \mathrm{~V}
$$

$$
5=5.0 \mathrm{~V}
$$

A $\quad=$ Assembly Location
WW, W = Work Week

This document contains information on a new product. Specifications and information herein are subject to change without notice.


SO-16L


SOW-16

## E PAD




Figure 1. Application Circuit

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage, $\mathrm{V}_{\text {IN }}$ |  | -0.3 to 45 | V |
| Output Voltage, V ${ }_{\text {OUT }}$ |  | -0.3 to 18 | V |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Logic Inputs/Outputs (Reset, WDI, Wakeup) |  | -0.3 to +7.0 | V |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ```Package Thermal Resistance, SO-8: Junction-to-Case, R өJc Junction-to-Ambient, R \({ }_{\text {日JA }}\)``` |  | $\begin{gathered} 45 \\ 165 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, SO-16L: Junction-to-Case, R ®JC Junction-to-Ambient, R ®JA |  | $\begin{aligned} & 18 \\ & 75 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, SOW-16 E PAD: Junction-to-Case, R ®JC Junction-to-Ambient, R ®JA |  | $\begin{aligned} & 1.0 \\ & 36 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow: (SMD styles only) (Note 2) | 260 peak 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} ; 6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 28 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{l}_{\mathrm{OUT}} \leq 150 \mathrm{~mA}, \mathrm{C}_{2}=1.0 \mu \mathrm{~F}\right.$,
$R_{\text {Delay }}=60 \mathrm{k}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output |  |  |  |  |  |
| Output Voltage, , V ${ }_{\text {Out }}$ for 3.3 V Option | - | 3.201 | 3.300 | 3.399 | V |
| Output Voltage, V ${ }_{\text {Out }}$ for 5.0 V Option | - | 4.85 | 5.00 | 5.15 | V |
| Dropout Voltage ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ ) | $\mathrm{l}_{\text {Out }}=150 \mathrm{~mA}$. Note 3 | - | 425 | 800 | mV |
| Load Regulation | $\mathrm{V}_{\text {IN }}=14 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\text {OUT }} \leq 150 \mathrm{~mA}$ | - | 5.0 | 30 | mV |
| Line Regulation | $6.0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 28 \mathrm{~V}$, I ${ }_{\text {OUT }}=5.0 \mathrm{~mA}$ | - | 5.0 | 20 | mV |
| Current Limit | - | 250 | 400 | - | mA |
| Thermal Shutdown | Guaranteed by Design | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Quiescent Current | $\mathrm{V}_{\text {IN }}=12 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=150 \mathrm{~mA}$ | - | 100 | 150 | $\mu \mathrm{A}$ |

RESET

| Threshold for 3.3 V Option | - | 2.970 | 3.069 | 3.168 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Threshold for 5.0 V Option | - | 4.50 | 4.65 | 4.80 | V |
| Output Low | $\mathrm{R}_{\text {LOAD }}=10 \mathrm{k}$ to $\mathrm{V}_{\text {OUT, }} \mathrm{V}_{\text {OUT }} \geq 1.0 \mathrm{~V}$ | - | 0.2 | 0.4 | V |
| Output High | $\mathrm{R}_{\text {LOAD }}=10 \mathrm{k}$ to GND | $\mathrm{V}_{\text {OUT }}-0.5$ | $V_{\text {OUT }}-0.25$ | - | V |
| Delay Time | $\begin{aligned} & V_{I N}=14 \mathrm{~V}, R_{\text {Delay }}=60 \mathrm{k}, \mathrm{I}_{\text {OUT }}=5.0 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{IN}}=14 \mathrm{~V}, R_{\text {Delay }}=120 \mathrm{k}, \mathrm{I}_{\text {OUT }}=5.0 \mathrm{~mA} \end{aligned}$ | $2.0$ | $\begin{aligned} & 3.0 \\ & 6.0 \end{aligned}$ | $4.0$ | ms |

## Watchdog Input

| Threshold High | - | 70 | - | - | $\% V_{\text {OUT }}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Threshold Low | - | - | - | 30 | $\% V_{\text {OUT }}$ |
| Hysteresis | - | 25 | 100 | - | mV |
| Input Current | WDI = 6.0 V | - | 0.1 | +10 | $\mu \mathrm{~A}$ |
| Pulse Width | $50 \%$ WDI falling edge to <br> $50 \%$ WDI rising edge and <br> $50 \%$ WDI rising edge to <br> $50 \%$ WDI falling edge, (see Figure 5) | 5.0 | - | - | $\mu \mathrm{s}$ |

Wake Up Output ( $\mathrm{V}_{\mathrm{IN}}=14 \mathrm{~V}$, IOUT $=5.0 \mathrm{~mA}$ )

| Wake Up Period | See Figures 4 and 5, $R_{\text {DELAY }}=60 \mathrm{k}$ <br> See Figures 4 and 5, R RELAY $=120 \mathrm{k}$ | $19$ | $\begin{aligned} & 25 \\ & 50 \end{aligned}$ | $31$ | $\begin{aligned} & \mathrm{ms} \\ & \mathrm{~ms} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Wake Up Duty Cycle Nominal | See Figure 3. | 45 | 50 | 55 | \% |
| RESET HIGH to <br> Wake Up Rising Delay Time | $R_{\text {DELAY }}=60 \mathrm{k}$ <br> $50 \%$ RESET rising edge to <br> $50 \%$ Wake Up edge, R $\mathrm{R}_{\text {DELAY }}=120 \mathrm{k}$ <br> (see Figures 3 and 4) | $10$ | $\begin{gathered} 12.5 \\ 25 \end{gathered}$ | $15$ | $\begin{aligned} & \mathrm{ms} \\ & \mathrm{~ms} \end{aligned}$ |
| Wake Up Response to Watchdog Input | $50 \%$ WDI falling edge to $50 \%$ Wake Up falling edge | - | 0.1 | 5.0 | $\mu \mathrm{s}$ |
| Wake Up Response to RESET | $50 \%$ RESET falling edge to $50 \%$ Wake Up falling edge. $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V} \rightarrow 4.5 \mathrm{~V}$ | - | 0.1 | 5.0 | $\mu \mathrm{s}$ |
| Output Low | $\mathrm{R}_{\text {LOAD }}=10 \mathrm{k}$ | - | 0.2 | 0.4 | V |
| Output High | $\mathrm{R}_{\text {LOAD }}=10 \mathrm{k}$ | $\mathrm{V}_{\text {OUT }}-0.5$ | $\mathrm{V}_{\text {OUT }}-0.25$ | - | V |

3. Measured when the output voltage has dropped 100 mV from the nominal value

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} ; 6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 28 \mathrm{~V}, 100 \mu \mathrm{~A} \leq \mathrm{I}_{\mathrm{OUT}} \leq 150 \mathrm{~mA}, \mathrm{C}_{2}=1.0 \mu \mathrm{~F}\right.$, $R_{\text {Delay }}=60 \mathrm{k}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Delay |  |  |  |  |  |
| Output Voltage | $\mathrm{I}_{\text {DELAY }}=50 \mu \mathrm{~A}$. Note 4 | - | 1.25 | - | V |

4. Current drain on the Delay pin directly affects the Delay Time, Wake Up Period, and the RESET to Wake Up Delay Time..

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: | :---: |
| SO-8 | SO-16L | SOW-16 <br> E PAD |  |  |
| 4 | 8 | 8 | $V_{\text {OUT }}$ | Regulated output voltage $\pm 3.0 \%$. |
| 5 | 9 | 9 | $\mathrm{V}_{\text {IN }}$ | Supply Voltage to the IC. |
| 6 | 11 | 11 | WDI | CMOS compatible input lead. The watchdog function monitors the falling edge of the incoming signal. |
| 2 | 4, 5, 12, 13 | 5 | GND | Ground connection. |
| 7 | 14 | 14 | WAKE UP | CMOS compatible output consisting of a continuously generated signal used to Wake Up the microprocessor from sleep mode. |
| 8 | 15 | 15 | RESET | CMOS compatible output lead RESET goes low whenever $\mathrm{V}_{\text {OUT }}$ drops by more than $7.0 \%$ from nominal, or during the absence of a correct watchdog signal. |
| 1 | 16 | 16 | Delay | Buffered bandgap voltage used to create timing current for RESET and Wake Up from $R_{\text {Delay. }}$ |
| - | 1-3, 6, 10 | $\begin{gathered} 1-4,6,10,12 \\ 13 \end{gathered}$ | NC | No Connection. |
| 3 | 7 | 7 | Sense | Kelvin connection which allows remote sensing of the output voltage for improved regulation. Connect to $\mathrm{V}_{\text {OUT }}$ if remote sensing is not required. |



Figure 2. Block Diagram

## NCV8508 Series

TIMING DIAGRAMS


Figure 3. Power Up, Sleep Mode and Normal Operation


Figure 4. Error Condition: Watchdog Remains Low and a RESET Is Issued


Figure 5. Power Down and Restart Sequence

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 6. Quiescent Current vs Output Current


Figure 8. POR Delay vs Temp, R ${ }_{\text {DELAY }}=60 \mathrm{k} \Omega$


Figure 10. Wakeup Period vs Temp, R ${ }_{\text {DELAY }}=60 \mathrm{k} \Omega$


Figure 7. Load Transient Response


Figure 9. POR Delay vs R $\mathrm{R}_{\text {DeLAY }}$


Figure 11. Wake Up Period vs R DeLay

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 12. Dropout Voltage vs Output Current


Figure 13. Output Voltage vs Temperature


Figure 14. Output Current vs Input Voltage

## DEFINITION OF TERMS

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques
such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

## DETAILED OPERATING DESCRIPTION

The NCV8508 is a precision micro-power voltage regulator with very low quiescent current $(100 \mu \mathrm{~A}$ typical at 250 mA load). A typical dropout voltage is 425 mV at 150 mA . Microprocessor control logic includes Watchdog,

Wake Up and RESET. This unique combination of extremely low quiescent current and full microprocessor control makes the NCV8508 ideal for use in battery
operated, microprocessor controlled equipment in addition to being a good fit in the automotive environment.

The NCV8508 Wake Up function brings the microprocessor out of Sleep mode. The microprocessor in turn, signals its Wake Up status back to the NCV8508 by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The NCV8508 responds to the falling edge of the Watchdog signal which it expects at least once during each wake-up period. When the correct Watchdog signal is received, a falling edge is issued on the wake-up signal line.
$\overline{\text { RESET }}$ is independent of $\mathrm{V}_{\text {IN }}$ and operates correctly to an output voltage as low as 1.0 V . A signal is issued in any of three situations. During power up the $\overline{\operatorname{RESET}}$ is held low until the output voltage is in regulation. During operation if
the output voltage shifts below the regulation limits, the $\overline{\text { RESET }}$ toggles low and remains low until proper output voltage regulation is restored. And finally, a $\overline{\text { RESET }}$ signal is issued if the regulator does not receive a Watchdog signal within the Wake Up period.

The RESET pulse width, Wake Up signal frequency, and Wake Up delay time are all set by one external resistor, $\mathrm{R}_{\text {Delay }}$.
The Delay pin is a buffered bandgap voltage (1.25 V). It can be used as a reference for an external tracking regulator like the CS8182.

The regulator is protected against short circuit and thermal runaway conditions. The device runs through 45 volt transients, making it suitable for use in automotive environments.

## CIRCUIT DESCRIPTION

## Functional Description

To reduce the drain on the battery a system can go into a low current consumption mode when ever its not performing a main routine. The Wake Up signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 volt square wave with a duty cycle of $50 \%$ at a frequency that is determined by a timing resistor, $\mathrm{R}_{\text {Delay }}$.

When the microprocessor receives a rising edge from the Wake Up output, it must issue a watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

The first falling edge of the watchdog signal causes the Wake Up to go low within $2.0 \mu \mathrm{~s}$ (typ) and remain low until the next Wake Up cycle (see Figure 15). Other watchdog pulses received within the same cycle are ignored (Figure 3).

During power up, $\overline{\mathrm{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text { RESET }}$ toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text { RESET }}$ delay, $\overline{\text { RESET }}$ returns high.

The Watchdog circuitry continuously monitors the input watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wake Up cycle will cause a RESET pulse to occur at the end of the Wake Up cycle. (see Figure 4).

The Wake Up output is pulled low during a $\overline{\text { RESET }}$ regardless of the cause of the $\overline{\text { RESET. After the } \overline{\text { RESET }}}$ returns high, the Wake Up cycle begins again (see Figure 4).

The RESET Delay Time, Wake Up signal frequency and $\overline{\text { RESET }}$ high to Wake Up delay time are all set by one external resistor $\mathrm{R}_{\text {Delay. }}$

Wake Up period $=\left(4.17 \times 10^{-7}\right) \mathrm{R}_{\text {Delay }}$
$\overline{\text { RESET }}$ Delay Time $=\left(5.21 \times 10^{-8}\right)$ R Delay
$\overline{\text { RESET }}$ HIGH to Wake Up Delay Time $=\left(2.08 \times 10^{-7}\right) \mathrm{R}_{\text {Delay }}$

Capacitor temperature coefficient and tolerance as well as the tolerance of the NCV8508 must be taken into account in order to get the correct system tolerance for each parameter.


Figure 15. Wake Up Response to WDI


Figure 16. Wake Up Response to RESET (Low Voltage)

## NCV8508 Series

## APPLICATION NOTES

## Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 17) is:

$$
\begin{align*}
\left.\mathrm{PD}_{\mathrm{D}} \max \right)= & {\left[\mathrm{V}_{\mathrm{IN}(\max )}-\mathrm{V}_{\mathrm{OUT}}(\min )\right] \mathrm{IOUT}(\max ) }  \tag{1}\\
& +\mathrm{V}_{\mathrm{IN}(\max )} \mathrm{Q} \mathrm{Q}
\end{align*}
$$

where:
$\mathrm{V}_{\mathrm{IN}(\text { max })}$ is the maximum input voltage,
$\mathrm{V}_{\text {OUT }(\mathrm{min})}$ is the minimum output voltage,
IOUT(max) is the maximum output current for the application, and
$\mathrm{I}_{\mathrm{Q}}$ is the quiescent current the regulator consumes at
IOUT(max).


Figure 17. Single Output Regulator with Key Performance Parameters Labeled
Once the value of $\mathrm{P}_{\mathrm{D}(\max )}$ is known, the maximum permissible value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can be calculated:

$$
\begin{equation*}
\mathrm{R}_{\Theta J A}=\frac{150^{\circ} \mathrm{C}-\mathrm{T}_{\mathrm{A}}}{\mathrm{P}_{\mathrm{D}}} \tag{2}
\end{equation*}
$$

The value of $\mathrm{R}_{\Theta \mathrm{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\mathrm{R}_{\Theta \mathrm{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below $150^{\circ} \mathrm{C}$.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

## Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $\mathrm{R}_{\Theta J A}$ :

$$
\begin{equation*}
R_{\Theta J A}=R_{\Theta J C}+R_{\Theta C S}+R_{\Theta S A} \tag{3}
\end{equation*}
$$

where:
$\mathrm{R}_{\Theta \mathrm{JC}}=$ the junction-to-case thermal resistance,
$\mathrm{R}_{\Theta C S}=$ the case-to-heatsink thermal resistance, and
$\mathrm{R}_{\Theta S A}=$ the heatsink-to-ambient thermal resistance.
$\mathrm{R}_{\Theta \mathrm{JC}}$ appears in the package section of the data sheet. Like $R_{\Theta J A}$, it too is a function of package type. $R_{\Theta C S}$ and $R_{\Theta S A}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

ORDERING INFORMATION*

| Device | Output Voltage | Package | Shipping |
| :---: | :---: | :---: | :---: |
| NCV8508D50 | 5.0 V | SO-8 | 95 Units/Rail |
| NCV8508D50R2 |  | SO-8 | 2500 Tape \& Reel |
| NCV8508DW50 |  | SO-16L | 46 Units/Rail |
| NCV8508DW50R2 |  | SO-16L | 1000 Tape \& Reel |
| NCV8508PDW50 |  | SOW-16 Exposed Pad | 46 Units/Rail |
| NCV8508PDW50R2 |  | SOW-16 Exposed Pad | 1000 Tape \& Reel |

*Consult your local sales representative for 3.3 V option.

## CS5101

## Secondary Side Post Regulator for AC/DC and DC/DC Multiple Output Converters

The CS5101 is a bipolar monolithic secondary side post regulator (SSPR) which provides tight regulation of multiple output voltages in AC-DC or DC-DC converters. Leading edge pulse width modulation is used with the CS5101.

The CS5101 is designed to operate over an 8.0 V to 45 V supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) range and up to a 75 V drive voltage $\left(\mathrm{V}_{\mathrm{C}}\right)$.

The CS5101 features include a totem pole output with 1.5 A peak output current capability, externally programmable overcurrent protection, an on chip $2.0 \%$ precision 5.0 V reference, internally compensated error amplifier, externally synchronized switching frequency, and a power switch drain voltage monitor. It is available in a 14 lead plastic DIP or a 16 lead wide body SO package.

## Features

- 1.5 A Peak Output (Grounded Totem Pole)
- 8.0 V to 75 V Gate Drive Voltage
- 8.0 V to 45 V Supply Voltage
- 300 ns Propagation Delay
- $1.0 \%$ Error Amplifier Reference Voltage
- Lossless Turn On and Turn Off
- Sleep Mode: < $100 \mu \mathrm{~A}$
- Overcurrent Protection with Dedicated Differential Amp
- Synchronization to External Clock
- External Power Switch Drain Voltage Monitor

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com
DIP-14
NSUFFIX
CASE 646

## PIN CONNECTIONS AND MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5101EN14 | DIP-14 | 25 Units/Rail |
| CS5101EDW16 | SO-16L | 46 Units/Rail |
| CS5101EDWR16 | SO-16L | 1000 Tape \& Reel |



Figure 1. Application Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ |  | -0.3 to 45 | V |
| $\mathrm{V}_{\text {SYNC }}$ and Output Supply Voltages, $\mathrm{V}_{\mathrm{C}}, \mathrm{V}_{\mathrm{G}}, \mathrm{V}_{\text {SYNC }}, \mathrm{V}_{\mathrm{D}}$ |  | -0.3 to 75 | V |
| $\mathrm{V}_{\text {IS }}$, $\mathrm{V}_{\text {IS- }}\left(\mathrm{V}_{\text {CC }}-4.0 \mathrm{~V}\right.$, up to 24 V$)$ |  | -0.3 to 24 | V |
| $\mathrm{V}_{\text {REF }}, \mathrm{V}_{\text {FB }}, \mathrm{V}_{\text {COMP }}, \mathrm{V}_{\text {RAMP, }}, \mathrm{V}_{\text {ISCOMP }}$ |  | -0.3 to 10 | V |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Temperature Range |  | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Output Energy (Capacitive Load Per Cycle) |  | 5.0 | $\mu \mathrm{J}$ |
| ESD Human Body |  | 2.0 | kV |
| Lead Temperature Soldering | Wave Solder (through hole styles only)(Note 1) Reflow (SMD styles only) (Note 2) | 260 peak 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 second maximum
2. 60 second maximum above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS: $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 10 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<45 \mathrm{~V}\right.$,
$8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<75 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Error Amplifier |  |  |  |  |  |
| Input Voltage Initial Accuracy | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\text {COMP }}, \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~T}=25^{\circ} \mathrm{C}$, Note 3 | 1.98 | 2.00 | 2.02 | V |
| Input Voltage | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\text {COMP, }}$, includes line and temp | 1.94 | 2.00 | 2.06 | V |
| Input Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}, \mathrm{IV}_{\mathrm{FB}}$ flows out of pin | - | - | 500 | nA |
| Open Loop Gain | $1.5 \mathrm{~V}<\mathrm{V}_{\text {COMP }}<3.0 \mathrm{~V}$ | 60 | 70 | - | dB |
| Unity Gain Bandwidth | $1.5 \mathrm{~V}<\mathrm{V}_{\text {COMP }}<3.0 \mathrm{~V}$, Note 3 | 0.7 | 1.0 | - | MHz |
| Output Sink Current | $\mathrm{V}_{\mathrm{COMP}}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.2 \mathrm{~V}$ | 2.0 | 8.0 | - | mA |
| Output Source Current | $\mathrm{V}_{\mathrm{COMP}}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.8 \mathrm{~V}$ | 2.0 | 6.0 | - | mA |
| $\mathrm{V}_{\text {COMP }}$ High | $\mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V}$ | 3.3 | 3.5 | 3.7 | V |
| $\mathrm{V}_{\text {COMP }}$ Low | $\mathrm{V}_{\mathrm{FB}}=2.2 \mathrm{~V}$ | 0.85 | 1.0 | 1.15 | V |
| PSRR | $10 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<45 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}}$, Note 3 | 60 | 70 | - | dB |

## Voltage Reference

| Output Voltage Initial Accuracy | $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~T}=25^{\circ} \mathrm{C}$, Note 3 | 4.9 | 5.0 | 5.1 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Voltage | $0 \mathrm{~A}<\mathrm{I}_{\mathrm{REF}}<8.0 \mathrm{~mA}$ | 4.8 | 5.0 | 5.2 | V |
| Line Regulation | $10 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<45 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=0 \mathrm{~A}$ | - | 10 | 60 | mV |
| Load Regulation | $0 \mathrm{~A}<\mathrm{I}_{\mathrm{REF}}<8.0 \mathrm{~mA}$ | - | 20 | 60 | mV |
| Current Limit | $\mathrm{V}_{\mathrm{REF}}=4.8 \mathrm{~V}$ | 10 | 50 | - | mA |
| $\mathrm{V}_{\text {REF-OK FAULT }} \mathrm{V}$ | $\mathrm{V}_{\text {SYNC }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {REF }}=\mathrm{V}_{\text {LOAD }}$ | 4.10 | 4.40 | 4.60 | V |
| $\mathrm{~V}_{\text {REF-OK }} \mathrm{V}$ | $\mathrm{V}_{\text {SYNC }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {REF }}=\mathrm{V}_{\text {LOAD }}$ | 4.30 | 4.50 | 4.80 | V |
| $\mathrm{~V}_{\text {REF-OK }}$ Hysteresis | - | 40 | 100 | 250 | mV |

Current Sense Amplifier

| IS COMP High V | IS $+=5.0 \mathrm{~V}$, IS- = IS COMP | 4.7 | 5.0 | 5.3 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IS COMP Low V | IS $+=0 \mathrm{~V}$, IS- = IS COMP | 0.5 | 1.0 | 1.3 | V |
| Source Current | $\mathrm{IS}+=5.0 \mathrm{~V}$, IS- $=0 \mathrm{~V}$ | 2.0 | 10 | - | mA |
| Sink Current | IS- = 5.0 V, IS $+=0 \mathrm{~V}$ | 10 | 20 | - | mA |
| Open Loop Gain | $1.5 \mathrm{~V} \leq \mathrm{V}_{\text {COMP }} \leq 4.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=4.0 \mathrm{k} \Omega$ | 60 | 80 | - | dB |
| CMRR | Note 3 | 60 | 80 | - | dB |
| PSRR | $10 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<45 \mathrm{~V}$, Note 3 | 60 | 80 | - | dB |
| Unity Gain Bandwidth | $1.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{COMP}} \leq 4.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=4.0 \mathrm{k} \Omega$, Note 3 | 0.5 | 0.8 | - | MHz |
| Input Offset Voltage | $\mathrm{V}_{\text {IS }}+=2.5 \mathrm{~V}, \mathrm{~V}_{\text {IS }}=\mathrm{V}_{\text {ISCOMP }}$ | -8.0 | 0 | 8.0 | mV |
| Input Bias Currents | $\mathrm{V}_{\text {IS }}+=\mathrm{V}_{\text {IS }}=0 \mathrm{~V}$, IIS flows out of pins | - | 20 | 250 | nA |
| Input Offset Current (IS+, IS-) | - | -250 | 0 | 250 | nA |
| Input Signal Voltage Range | Note 3 | -0.3 | - | $\mathrm{V}_{C C}-4.0$ | V |

3. Guaranteed by design. Not $100 \%$ tested in production.

## CS5101

ELECTRICAL CHARACTERISTICS: (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, 10 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<45 \mathrm{~V}\right.$, 8.0 V $<\mathrm{V}_{\mathrm{C}}<75 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RAMP/SYNC Generator |  |  |  |  |  |
| RAMP Source Current Initial Accuracy | $\mathrm{V}_{\text {SYNC }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {RAMP }}=2.5 \mathrm{~V}, \mathrm{~T}=25^{\circ} \mathrm{C}$, Note 4 | 0.18 | 0.20 | 0.22 | mA |
| RAMP Source Current | $\mathrm{V}_{\text {SYNC }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {RAMP }}=2.5 \mathrm{~V}$ | 0.16 | 0.20 | 0.24 | mA |
| RAMP Sink Current | $\mathrm{V}_{\text {SYNC }}=0 \mathrm{~V}, \mathrm{~V}_{\text {RAMP }}=2.5 \mathrm{~V}$ | 1.0 | 4.0 | - | mA |
| RAMP Peak Voltage | $\mathrm{V}_{\text {SYNC }}=5.0 \mathrm{~V}$ | 3.3 | 3.5 | 3.7 | V |
| RAMP Valley Voltage | $\mathrm{V}_{\text {SYNC }}=0 \mathrm{~V}$ | 1.4 | 1.5 | 1.6 | V |
| RAMP Dynamic Range | $\mathrm{V}_{\text {RAMPDR }}=\mathrm{V}_{\text {RAMPPK }}-\mathrm{V}_{\text {RAMPVY }}$ | 1.7 | 2.0 | 2.3 | V |
| RAMP Sleep Threshold Voltage | $\mathrm{V}_{\text {RAMP }} @ \mathrm{~V}_{\text {REF }}<2.0 \mathrm{~V}$ | 0.3 | 0.6 | 1.0 | V |
| SYNC Threshold | $\mathrm{V}_{\text {SYNC }} @ \mathrm{~V}_{\text {RAMP }}>2.5 \mathrm{~V}$ | 2.3 | 2.5 | 2.7 | V |
| SYNC Input Bias Current | $\mathrm{V}_{\text {SYNC }}=0 \mathrm{~V}$, ISYNC flows out of pin | - | 1.0 | 20 | $\mu \mathrm{A}$ |

## Output Stage

| $\mathrm{V}_{\mathrm{G}}$, High | $\mathrm{V}_{\mathrm{SYNC}}=5.0 \mathrm{~V}, \mathrm{IV} \mathrm{V}_{\mathrm{G}}=200 \mathrm{~mA}, \mathrm{~V}_{\mathrm{C}}-\mathrm{V}_{\mathrm{G}}$ | - | 1.6 | 2.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{G}}$, Low | $\mathrm{V}_{\mathrm{SYNC}}=0 \mathrm{~V}, \mathrm{IV} \mathrm{V}_{\mathrm{G}}=200 \mathrm{~mA}$ | - | 0.9 | 1.5 | V |
| $\mathrm{~V}_{\mathrm{G}}$ Rise Time | Switch $\mathrm{V}_{\mathrm{SYNC}}$ High, $\mathrm{C}_{\mathrm{G}}=1.0 \mathrm{nF}, \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$, <br> measure 2.0 V to 8.0 V | - | 30 | 75 | ns |
| $\mathrm{~V}_{\mathrm{G}}$ Fall Time | Switch $\mathrm{V}_{\mathrm{SYNC}}$ Low, $\mathrm{C}_{\mathrm{G}}=1.0 \mathrm{nF}, \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$, <br> measure 8.0 V to 2.0 V | - | 40 | 100 | ns |
| $\mathrm{~V}_{\mathrm{G}}$ Resistance to GND | Remove supplies, $\mathrm{V}_{\mathrm{G}}=10 \mathrm{~V}$ | - | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\mathrm{D}}$ Resistance to GND | Remove supplies, $\mathrm{V}_{\mathrm{D}}=10 \mathrm{~V}$ | 500 | 1500 | - | $\Omega$ |

General

| $I_{\text {cc }}$, Operating | $\mathrm{V}_{\text {SYNC }}=5.0 \mathrm{~V}$ | - | 12 | 18 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $I_{\text {cc }}$ in UVL | $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$ | - | 300 | 500 | $\mu \mathrm{A}$ |
| Icc in Sleep Mode High | $\mathrm{V}_{\text {RAMP }}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=45 \mathrm{~V}$ | - | 80 | 200 | $\mu \mathrm{A}$ |
| ICC in Sleep Mode Low | $\mathrm{V}_{\text {RAMP }}=0 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=10 \mathrm{~V}$ | - | 20 | 50 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{C}}$, Operating High | $\mathrm{V}_{\mathrm{SYNC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{IS}^{-}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=75 \mathrm{~V}$ | - | 4.0 | 8.0 | mA |
| $\mathrm{I}_{\mathrm{C}}$, Operating Low | $\mathrm{V}_{\mathrm{SYNC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{IS}^{-}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=8.0 \mathrm{~V}$ | - | 3.0 | 6.0 | mA |
| UVLO Start Voltage | - | 7.4 | 8.0 | 9.2 | V |
| UVLO Stop Voltage | - | 6.4 | 7.0 | 8.3 | V |
| UVLO Hysteresis | - | 0.8 | 1.0 | 1.2 | V |
| Leading Edge, t ${ }_{\text {DELAY }}$ | $\mathrm{V}_{\text {SYNC }}=2.5 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{G}}=8.0 \mathrm{~V}$ | - | 280 | - | ns |
| Trailing Edge, ${ }_{\text {DELAY }}$ | $\mathrm{V}_{\text {SYNC }}=2.5 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{G}}=2.0 \mathrm{~V}$ | - | 750 | - | ns |

4. Guaranteed by design. Not $100 \%$ tested in production.

## CS5101

PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  | LEAD SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| DIP-14 | SO-16L |  |  |
| 1 | 1 | SYNC | Synchronization input. |
| 2 | 2 | $\mathrm{V}_{\mathrm{CC}}$ | Logic supply ( 10 V to 45 V ). |
| 3 | 3 | $V_{\text {REF }}$ | 5.0 V voltage reference. |
| 4 | - | LGND | Logic level ground (analog and digital ground tied). |
| 5 | 6 | $\mathrm{V}_{\mathrm{FB}}$ | Error amplifier inverting input. |
| 6 | 7 | COMP | Error amplifier output and compensation. |
| 7 | 8 | RAMP | RAMP programmable with the external capacitor. |
| 8 | 9 | IS+ | Current sense amplifier non-inverting input. |
| 9 | 10 | IS- | Current sense amplifier inverting input. |
| 10 | 11 | IS COMP | Current sense amplifier compensation and output. |
| 11 | 12, 13 | PGND | Power ground. |
| 12 | 14 | $V_{G}$ | External power switch gate drive. |
| 13 | 15 | $\mathrm{V}_{\mathrm{C}}$ | Output power stage supply voltage (8.0 V to 75 V ). |
| 14 | 16 | $V_{D}$ | External FET DRAIN voltage monitor. |
| - | 5 | AGND | Analog ground. |
| - | 4 | DGND | Digital ground. |

## CIRCUIT DESCRIPTION



Figure 2. Block Diagram

## Theory of Operation

The CS5101 is designed to regulate voltages in multiple output power supplies. Functionally, it is similar to a magnetic amplifier, operating as a switch with a delayed turn-on. It can be used with both single ended and dual ended topologies.

The $\mathrm{V}_{\mathrm{FB}}$ voltage is monitored by the error amplifier EA. It is compared to an internal reference voltage and the amplified differential signal is fed through an inverting amplifier into the buffer, BUF. The buffered signal is compared at the PWM comparator with the ramp voltage generated by capacitor $C_{R}$. When the ramp voltage $V_{R}$, exceeds the control voltage $\mathrm{V}_{\mathrm{C}}$, the output of the PWM comparator goes high, latching its state through the LATCH, the output stage transistor $\mathrm{Q}_{1}$ turns on, and the external power switch, usually an $\mathrm{N}-\mathrm{FET}$, turns on.

## SYNC Function

The SYNC circuit is activated at time $t_{1}$ (Figure 3) when the voltage at the SYNC pin exceeds the threshold level (2.5V) of the SYNC comparator. The external ramp capacitor $C_{R}$ is allowed to charge through the internal current source $I(200 \mu \mathrm{~A})$. At time $t_{2}$, the ramp voltage intersects with the control voltage $\mathrm{V}_{\mathrm{C}}$ and the output of the PWM comparator goes high, turning on the output stage and the external power switch. At the same time, the PWM comparator is latched by the RS latch, LATCH.


Figure 3. Waveforms for CS5101. The Number to the Left of Each Curve Refers to a Node On the Application Diagram on Page 956.

The logic state of the LATCH can be changed only when both the voltage level of the trailing edge of the power pulse at the SYNC pin is less than the threshold voltage of the SYNC comparator ( 2.5 V ) and the RAMP voltage is less than the threshold voltage of the RAMP comparator (1.65 V). On the negative going transition of the secondary side pulse $\mathrm{V}_{\mathrm{SY}}$, gate $\mathrm{G}_{2}$ output goes high, resetting the latch at time $\mathrm{t}_{3}$. Capacitor $C_{R}$ is discharged through transistor $Q_{4} . C_{R}$ 's output goes low disabling the output stage, and the external power switch (an N-FET) is turned off.

## RAMP Function

The value of the ramp capacitor $C_{R}$ is based on the switching frequency of the regulator and the maximum duty cycle of the secondary pulse $\mathrm{V}_{\mathrm{SY}}$.
If the RAMP pin is pulled externally to 0.3 V or below, the SSPR is disabled. Current drawn by the IC is reduced to less than $100 \mu \mathrm{~A}$, and the IC is in SLEEP mode.

## FAULT Function

The voltage at the $\mathrm{V}_{\mathrm{CC}}$ pin is monitored by the undervoltage lockout comparator with hysteresis. When $\mathrm{V}_{\mathrm{CC}}$ falls below the UVL threshold, the 5.0 V reference and all the circuitry running off of it is disabled. Under this condition the supply current is reduced to less than $500 \mu \mathrm{~A}$.
The $\mathrm{V}_{\mathrm{CC}}$ supply voltage is further monitored by the $\mathrm{V}_{\mathrm{CC}}$ OK comparator. When $\mathrm{V}_{\mathrm{CC}}$ is reduced below $\mathrm{V}_{\mathrm{REF}}$ -0.7 V , a fault signal is sent to gate $\mathrm{G}_{1}$. This fault signal, which determines if $\mathrm{V}_{\mathrm{CC}}$ is absent, works in conjunction with the ramp signal to disable the output, but only after the current cycle has finished and the RS latch is reset. Therefore this fault will not cause the output to turn off during the middle of an on pulse, but rather will utilize lossless turn-off. This feature protects the FET from overvoltage stress. This is accomplished through gate $G_{1}$ by driving transistor $\mathrm{Q}_{4}$ on.

An additional fault signal is derived from the REF_OK comparator. $\mathrm{V}_{\text {REF }}$ is monitored so to disable the output through gate $G_{1}$ when the $V_{\text {REF }}$ voltage falls below the OK threshold. As in the $\mathrm{V}_{\mathrm{CC}}$ _OK fault, the REF_OK fault disables the output after the current cycle has been completed. The fault logic will operate normally only when $\mathrm{V}_{\mathrm{REF}}$ voltage is within the specification limits of REF_OK.

## DRAIN Function

The drain pin, $\mathrm{V}_{\mathrm{D}}$ monitors the voltage on the drain of the power switch and derives energy from it to keep the output stage in an off state when $\mathrm{V}_{\mathrm{C}}$ or $\mathrm{V}_{\mathrm{CC}}$ is below the minimum specified voltage.


Figure 4. CS5101 Bench Test on DIP-14 Package

PACKAGE THERMAL DATA

| Parameter |  | DIP-14 | SO-16L | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 23 | 48 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 105 | 85 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## NCP4300A

## Dual Operational Amplifier and Voltage Reference

The NCP4300A is a monolithic integrated circuit specifically designed to control the output current and voltage levels of switch mode battery chargers and power supplies. This device contains a precision 2.6 V shunt reference and two operational amplifiers. Op-Amp 1 is designed to perform voltage control and has its non-inverting input internally connected to the reference. Op-Amp 2 is designed for current control and has both inputs uncommitted. The NCP4300A offers the power converter designer a control solution that features increased precision with a corresponding reduction in system complexity and cost. This device is available in an 8-lead surface mount package.

## Features

## Operational Amplifier

- Low Input Offset Voltage: 0.5 mV
- Input Common Mode Voltage Range Includes Ground
- Low Supply Current: $210 \mu \mathrm{~A} / \mathrm{Op}-\mathrm{Amp}\left(@ \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right.$ )
- Medium Unity Gain Bandwidth: 0.7 MHz
- Large Output Voltage Swing: 0 V to $\mathrm{V}_{\mathrm{CC}}-1.5 \mathrm{~V}$
- Wide Power Supply Voltage Range: 3.0 V to 35 V


## Voltage Reference

- Fixed Output Voltage Reference: 2.60 V
- High Precision Over Temperature: $1.0 \%$
- Wide Sink Current Range: $80 \mu \mathrm{~A}$ to 80 mA


## Typical Applications

- Battery Charger
- Switch Mode Power Supply



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PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP4300ADR2 | SO-8 | 2500/Tape \& Reel |

Figure 1. Functional Block Diagram

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (VCC to GND) | $\mathrm{V}_{\mathrm{CC}}$ | 36 | V |
| ESD Protection Voltage at any Pin (Human Body Model) | $\mathrm{V}_{\mathrm{ESD}}$ | $2.0 \mathrm{~K}(\mathrm{~min})$ | V |
| Op-Amp 1 and 2 Input Voltage Range (Pins 2, 5, 6) | $\mathrm{V}_{\mathrm{IR}}$ | -0.6 to $\mathrm{V}_{\mathrm{CC}}+0.6$ | V |
| Op-Amp 2 Input Differential Voltage Range (Pins 5, 6) | $\mathrm{V}_{\mathrm{IDR}}$ | $\mathrm{V}_{\mathrm{CC}}$ to GND | V |
| Voltage Reference Cathode Current (Pin 3) | $\mathrm{I}_{\mathrm{K}}$ | 100 | mA |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | 0 to 105 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{stg}}$ | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |

THERMAL CHARACTERISTICS

| Rating | Symbol | Value |  |
| :--- | :---: | :---: | :---: |
| Thermal Resistance, Junction to Ambient | Unit |  |  |
| Thermal Resistance, Junction to Case | $R_{\theta J A}$ |  | 155 |
| ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |  |  |

TYPICAL ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Total Supply Current, excluding Current in the Voltage Reference | $\mathrm{I}_{\mathrm{CC}}$ | - | 0.42 | 0.8 | mA |
| $\mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}$, no load; $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}$ |  |  |  |  |  |

Op-Amp 1 (Op-amp with non-inverting input connected to the internal Vref)
( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {out }}=1.4 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted)

| Input Offset Voltage $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{10}$ | - | 0.5 - | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage Temperature Coefficient $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 7.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current (Inverting input only) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | IB | - | $-50$ | $\begin{aligned} & -150 \\ & -150 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~V}_{\text {out }}=1.4 \mathrm{~V} \text { to } 11.4 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | Avol | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ |  | - | V/mV |
| Power Supply Rejection ( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ to 30 V ) | PSRR | 40 | 90 | - | dB |
| Output Source Current ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~V}_{\text {out }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {ID }}=+1.0 \mathrm{~V}$ ) | $\mathrm{l}_{+}$ | 10 | 16 | - | mA |
| Output Sink Current ( $\left.\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~V}_{\text {out }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {ID }}=-1.0 \mathrm{~V}\right)$ | $\mathrm{l}_{0}$ | 10 | 25 | - | mA |
| Output Voltage Swing, High ( $\left.\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{ID}}=+1.0 \mathrm{~V}\right)$ $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 27 \\ & 27 \end{aligned}$ | 28 | - | V |
| Output Voltage Swing, Low ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{ID}}=-1.0 \mathrm{~V}$ ) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | $17$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | mV |
| Slew Rate ( $\mathrm{V}_{\text {in }}=0.5$ to $2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{A}_{\mathrm{V}}=1.0, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$ ) | SR | 0.3 | 0.5 | - | V/ $\mu \mathrm{s}$ |
| Unity Gain Bandwidth ( $\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{V}_{\text {in }}=0.5 \mathrm{Vpp} @$ $\mathrm{f}=70 \mathrm{kHz}$ ) | BW | 0.3 | 0.7 | - | MHz |
| Total Harmonic Distortion ( $\mathrm{f}=1.0 \mathrm{kHz}, \mathrm{A}_{\mathrm{V}}=10, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}$, $\mathrm{V}_{\text {out }}=2.0 \mathrm{~V}_{\mathrm{PP}}$ ) | THD | - | 0.02 | - | \% |

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Op-Amp 2 (Independent op-amp) $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {out }}=1.4 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Input Offset Voltage $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{10}$ | - |  | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage Temperature Coefficient $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 7.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Offset Current $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | 1 IO |  | 2.0 - | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ | nA |
| Input Bias Current $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $I_{\text {IB }}$ |  | $-50$ | $\begin{aligned} & -150 \\ & -150 \end{aligned}$ | nA |
| Input Common Mode Voltage Range ( $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ to 35 V ) | VICR | - | $\begin{gathered} 0 \text { to } \\ \mathrm{v}_{\mathrm{CC}}-1.5 \end{gathered}$ | - | V |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~V}_{\text {out }}=1.4 \mathrm{~V} \text { to } 11.4 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | Avol | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | $\begin{gathered} 100 \\ \hline \end{gathered}$ | - | V/mV |
| Power Supply Rejection ( $\mathrm{V}_{\text {CC }}=5.0 \mathrm{~V}$ to 30 V ) | PSRR | 40 | 90 | - | dB |
| $\begin{aligned} & \text { Common Mode Rejection }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V} \text { to } 3.5 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | CMRR | $\begin{aligned} & 40 \\ & 30 \end{aligned}$ | $60$ | - | dB |
| Output Source Current ( $\left.\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~V}_{\text {out }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {ID }}=+1.0 \mathrm{~V}\right)$ | $\mathrm{l}_{+}$ | 10 | 16 | - | mA |
| Output Sink Current ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~V}_{\text {out }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {ID }}=-1.0 \mathrm{~V}$ ) | lo- | 10 | 25 | - | mA |
| Output Voltage Swing, $\operatorname{High}\left(\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{ID}}=+1.0 \mathrm{~V}\right)$ $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 27 \\ & 27 \end{aligned}$ | $28$ | - | V |
| Output Voltage Swing, Low $\left(R_{L}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{ID}}=-1.0 \mathrm{~V}\right)$ $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | VOL | - | $17$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | mV |
| Slew Rate ( $\mathrm{V}_{\text {in }}=0.5$ to $3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{A}_{\mathrm{v}}=1.0, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$ ) | SR | 0.3 | 0.5 | - | V/ $/ \mathrm{s}$ |
| Unity Gain Bandwidth ( $\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{V}_{\mathrm{in}}=0.5 \mathrm{Vpp} @$ $\mathrm{f}=70 \mathrm{kHz}$ ) | BW | 0.3 | 0.7 | - | MHz |
| Total Harmonic Distortion ( $\mathrm{f}=1.0 \mathrm{KHz}, \mathrm{A}_{\mathrm{V}}=10, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}$, $\mathrm{V}_{\text {out }}=2.0 \mathrm{~V}_{\mathrm{PP}}$ ) | THD | - | 0.02 | - | \% |

## Voltage Reference

| $\begin{aligned} & \text { Reference Voltage }\left(\mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}\right) \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\stackrel{-}{2.574}$ | $\begin{aligned} & 2.60 \\ & 2.60 \end{aligned}$ | $2 . \overline{-}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Reference Input Voltage Deviation Over Full Temperature Range $\left(\mathrm{I}_{\mathrm{K}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C}\right)$ | $\Delta \mathrm{V}_{\text {ref }}$ | - | 5.0 | 22 | mV |
| Minimum Cathode Current for Regulation | $\mathrm{I}_{\mathrm{K}(\text { min })}$ | - | 55 | 80 | $\mu \mathrm{A}$ |
| Dynamic Impedance $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{K}}=1.0 \text { to } 80 \mathrm{~mA}, \mathrm{f}<1.0 \mathrm{KHz} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{K}}=1.0 \mathrm{~mA} \text { to } 60 \mathrm{~mA}, \mathrm{f}<1.0 \mathrm{KHz} \end{aligned}$ | $\left\|Z_{K A}\right\|$ | - | 0.3 | $\begin{aligned} & 0.5 \\ & 0.6 \end{aligned}$ | $\Omega$ |



Figure 2. Reference Cathode Current vs. Cathode Voltage


Figure 4. Reference Dynamic Impedance vs. Ambient Temperature


Figure 6. Input Offset Voltage
vs. Ambient Temperature


Figure 3. Reference Voltage
vs. Ambient Temperature


Figure 5. Reference Stability
vs. Load Capacitance


Figure 7. Input Bias Current vs. Ambient Temperature


Figure 8. Common Mode Rejection Ratio vs. Supply Voltage

## DETAILED OPERATING DESCRIPTION

## INTRODUCTION

Power supplies and battery chargers require precise control of output voltage and current in order to prevent catastrophic damage to the system connected. Many present day power sources contain a wide assortment of building blocks and glue devices to perform the required sensing for proper regulation. Typical feedback loop circuits may consist of a voltage and current amplifier, summing circuitry and a reference. The NCP4300A contains all of these basic functions in a manner that is easily adaptable to many of the various power source-load configurations.

## OPERATING DESCRIPTION

The NCP4300A is an analog regulation control circuit that is designed to simultaneously close the voltage and current feedback loops in power supply and battery charger applications. This device can control the feedback loop in either constant-voltage (CV) or constant-current (CC) mode with smooth crossover. A concise description of the integrated circuit blocks is given in below. The functional block diagram of the IC is shown in Figure 1.

## Internal Reference

An internal precision band gap reference is used to set the 2.6 V voltage threshold and current threshold setting. The
reference is initially trimmed to a $\pm 0.5 \%$ tolerance at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and is guaranteed to be within $\pm 1.0 \%$ over an ambient temperature range of $0^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$.

## Voltage Sensing Operational Amplifier (Op-Amp 1)

The internal Op-Amp 1 is designed to perform the voltage control function. The non-inverting input of the op-amp is connected to the precision voltage reference internally. The inverting input of the op-amp monitors the voltage information derived from the system output. As the control threshold is internally connected to the voltage reference, the voltage regulation threshold is fixed at 2.6 V . For any output voltage from 2.6 V up to the maximum limit can be configurated with an external resistor divider. The output terminal of Op-Amp 1 (pin 1) provides the error signal for output voltage control. The output pin also provides a means for external compensation.

## Independent Operational Amplifier (Op-Amp 2)

The internal Op-Amp 2 is configurated as a general purpose op-amp with all terminals available for the user. With the low offset voltage provided, 0.5 mV , this op-amp can be used for current sensing in a constant current regulator.


The above circuit demonstrates the use of the NCP4300A in a constant-current constant-voltage switch mode battery charger application. The charging current level is set by resistors R3, R4, and R5. The reference voltage is divided down by resistors R3 and R4 to create an offset voltage at pin 6. This results in a high state at the op amp output, pin 7. As the battery pack charge current increases, a proportional increasing voltage is developed across R5 that will eventually cancel out the pin 6 offset voltage. This will cause the op amp output to sink current from the opto isolator diode, and control the SMPS block in a constant-current mode. Resistors R1 and R2 divide the battery pack voltage down to the 2.6 V reference level. As the battery pack voltage exceeds the desired programmed level, the voltage at pin 2 will become slightly greater than pin 3 . This will cause the op amp output to sink current from the opto isolator diode, and control the SMPS block in a constant-voltage mode. The formulas for programming the output current and voltage are given below.

$$
\begin{array}{rl}
\mathrm{l}_{\text {out }}=\frac{V_{\text {ref }}}{\left(\frac{R 3}{R 4}+1\right) R 5} & V_{\text {out }}=\left(\frac{R 1}{R 2}+1\right) V_{\text {ref }} \\
& \\
\text { With }: \begin{array}{l}
R 3=30 \mathrm{k} \\
R 4=1.2 \mathrm{k}
\end{array} & \text { With }: R 1=4.7 \mathrm{k} \\
R 5=0.1 & R 2=3.6 \mathrm{k} \\
l_{\text {out }}=1.0 \mathrm{~A} & V_{\text {out }}=6.0 \mathrm{~V}
\end{array}
$$

Figure 9. Constant-Current Constant-Voltage Switch Mode Battery Charger

## MC44608

## Few External Components Reliable and Flexible SMPS Controller

The MC44608 is a high performance voltage mode controller designed for off-line converters. This high voltage circuit that integrates the start-up current source and the oscillator capacitor, requires few external components while offering a high flexibility and reliability.

The device also features a very high efficiency stand-by management consisting of an effective Pulsed Mode operation. This technique enables the reduction of the stand-by power consumption to approximately 1.0 W while delivering 300 mW in a 150 W SMPS.

- Integrated Start-Up Current Source
- Lossless Off-Line Start-Up
- Direct Off-Line Operation
- Fast Start-Up


## General Features

- Flexibility
- Duty Cycle Control
- Undervoltage Lockout with Hysteresis
- On Chip Oscillator Switching Frequency 40, 75, or 100 kHz
- Secondary Control with Few External Components


## Protections

- Maximum Duty Cycle Limitation
- Cycle by Cycle Current Limitation
- Demagnetization (Zero Current Detection) Protection
- "Over V ${ }_{\text {CC }}$ Protection" Against Open Loop
- Programmable Low Inertia Over Voltage Protection Against Open Loop
- Internal Thermal Protection


## SMPS Controller

- Pulsed Mode Techniques for a Very High Efficiency Low Power Mode
- Lossless Startup
- Low dV/dT for Low EMI Radiations

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PDIP-8
P SUFFIX CASE 626

## PIN CONNECTIONS AND MARKING DIAGRAM



AWL = Manufacturing Code YYWW = Date Code

ORDERING INFORMATION

| Device | Switching <br> Frequency | Package | Shipping |
| :---: | :---: | :---: | :---: |
| MC44608P40 | 40 kHz | Plastic <br> DIP-8 | $50 /$ Rail |
| MC44608P75 | 75 kHz | Plastic <br> DIP-8 | $50 /$ Rail |
| MC44608P100 | 100 kHz | Plastic <br> DIP-8 | $50 /$ Rail |



Figure 1. Representative Block Diagram

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Total Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ | 30 | mA |
| Output Supply Voltage with Respect to Ground | $\mathrm{V}_{\mathrm{CC}}$ | 16 | V |
| All Inputs except Vi | $\mathrm{V}_{\text {inputs }}$ | -1.0 to +16 | V |
| Line Voltage Absolute Rating | $\mathrm{V}_{\mathrm{i}}$ | 500 | V |
| Recommended Line Voltage Operating Condition | $\mathrm{V}_{\mathrm{i}}$ | 400 | V |
| Power Dissipation and Thermal Characteristics <br> Maximum Power Dissipation at $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $\mathrm{P}_{\mathrm{D}}$ | 600 | mW |
| Operating Junction Temperature | $\mathrm{R}_{\theta J \mathrm{~A}}$ | $\mathrm{~T}_{\mathrm{J}}$ | 100 |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | 150 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OUTPUT SECTION |  |  |  |  |  |
| Output Resistor <br> Sink Resistance Source Resistance | RoL $\mathrm{R}_{\mathrm{OH}}$ | 5.0 | $\begin{aligned} & 8.5 \\ & 15 \end{aligned}$ | 15 - | $\Omega$ |
| Output Voltage Rise Time (from 3.0 V up to 9.0 V) (Note 1.) | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | - | ns |
| Output Voltage Falling Edge Slew-Rate (from 9.0 V down to 3.0 V ) (Note 1.) | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | - | ns |

CONTROL INPUT SECTION

| Duty Cycle @ $\mathrm{I}_{\text {pin3 }}=2.5 \mathrm{~mA}$ | $\mathrm{~d}_{2 \mathrm{~mA}}$ | - | - | 2.0 | $\%$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Duty Cycle @ $\mathrm{I}_{\text {pin3 }}=1.0 \mathrm{~mA}$ | $\mathrm{~d}_{1 \mathrm{~mA}}$ | 36 | 43 | 48 | $\%$ |
| Control Input Clamp Voltage (Switching Phase) @ $\mathrm{I}_{\text {pin3 }}=-1.0 \mathrm{~mA}$ |  | 4.75 | 5.0 | 5.25 | V |
| Latched Phase Control Input Voltage (Stand-by) @ $\mathrm{I}_{\text {pin3 }}=+500 \mu \mathrm{~A}$ | $\mathrm{~V}_{\text {LP-stby }}$ | 3.4 | 3.9 | 4.3 | V |
| Latched Phase Control Input Voltage (Stand-by) @ $\mathrm{I}_{\text {pin3 }}=+1.0 \mathrm{~mA}$ | $\mathrm{~V}_{\text {LP-stby }}$ | 2.4 | 3.0 | 3.7 | V |

CURRENT SENSE SECTION

| Maximum Current Sense Input Threshold | $\mathrm{V}_{\text {CS-th }}$ | 0.95 | 1.0 | 1.05 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | $\mathrm{I}_{\mathrm{B}-\mathrm{cs}}$ | -1.8 | - | 1.8 | $\mu \mathrm{A}$ |
| Stand-By Current Sense Input Current | ICS-stby | 180 | 200 | 220 | $\mu \mathrm{A}$ |
| Start-up Phase Current Sense Input Current | ICS-stup | 180 | 200 | 220 | $\mu \mathrm{A}$ |
| Propagation Delay (Current Sense Input to Output @ $\mathrm{V}_{\mathrm{TH}} \mathrm{T}$ MOS $=3.0 \mathrm{~V}$ ) | $\mathrm{T}_{\text {PLH(In/Out) }}$ | - | 220 | - | ns |
| Leading Edge Blanking Duration MC44608P40 | $\mathrm{T}_{\text {Leb }}$ | - | 480 | - | ns |
| Leading Edge Blanking Duration MC44608P75 | $\mathrm{T}_{\text {LEB }}$ | - | 250 | - | ns |
| Leading Edge Blanking Duration MC44608P100 | $\mathrm{T}_{\text {LeB }}$ | - | 200 | - | ns |
| Leading Edge Blanking + Propagation Delay MC44608P40 | TDLY | 500 | 680 | 900 | ns |
| Leading Edge Blanking + Propagation Delay MC44608P75 | $\mathrm{T}_{\text {DLY }}$ | 370 | 470 | 570 | ns |
| Leading Edge Blanking + Propagation Delay MC44608P100 | $\mathrm{T}_{\text {DLY }}$ | 300 | 420 | 500 | ns |

OSCILLATOR SECTION

| Normal Operation Frequency MC44608P40 | $\mathrm{f}_{\text {osc }}$ | 36 | 40 | 44 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Normal Operation Frequency MC44608P75 | $\mathrm{f}_{\text {osc }}$ | 68 | 75 | 82 | kHz |
| Normal Operation Frequency MC44608P100 | $\mathrm{f}_{\text {osc }}$ | 90 | 100 | 110 | kHz |
| Maximum Duty Cycle @ $\mathrm{f}=\mathrm{f}_{\text {osc }}$ | $\mathrm{d}_{\max }$ | 78 | 82 | 86 | $\%$ |

OVERVOLTAGE SECTION

| Quick OVP Input Filtering $\left(\mathrm{R}_{\text {demag }}=100 \mathrm{k} \Omega\right)$ | $\mathrm{T}_{\text {filt }}$ | - | 250 | - | ns |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay ( $\mathrm{I}_{\text {demag }}>\mathrm{I}_{\text {ovp }}$ to output low) | $\mathrm{T}_{\text {PHL(In/Out })}$ | - | 2.0 | - | $\mu \mathrm{s}$ |
| Quick OVP Current Threshold | $\mathrm{I}_{\text {OVP }}$ | 105 | 120 | 140 | $\mu \mathrm{~A}$ |
| Protection Threshold Level on $\mathrm{V}_{\text {CC }}$ | $\mathrm{V}_{\text {CC-OVP }}$ | 14.8 | 15.3 | 15.8 | V |
| Minimum Gap Between $\mathrm{V}_{\text {CC-OVP }}$ and $\mathrm{V}_{\text {stup-th }}$ | $\mathrm{V}_{\text {CC-OVP }}-$ <br> $\mathrm{V}_{\text {stup }}$ | 1.0 | - | - | V |

1. This parameter is measured using 1.0 nF connected between the output and the ground.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ unless otherwise noted) (Note 2.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEMAGNETIZATION DETECTION SECTION (Note 3.) |  |  |  |  |  |
| Demag Comparator Threshold ( $\mathrm{V}_{\text {pin1 }}$ increasing) | $\mathrm{V}_{\text {dmg-th }}$ | 30 | 50 | 69 | mV |
| Demag Comparator Hysteresis (Note 4.) | $\mathrm{H}_{\text {dmg }}$ | - | 30 | - | mV |
| Propagation Delay (Input to Output, Low to High) | tpHL(In/Out) | - | 300 | - | ns |
| Input Bias Current ( $\mathrm{V}_{\text {demag }}=50 \mathrm{mV}$ ) | $\mathrm{I}_{\text {dem-lb }}$ | -0.6 | - | - | $\mu \mathrm{A}$ |
| Negative Clamp Level ( $\left.\mathrm{l}_{\text {demag }}=-1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {cl-neg-dem }}$ | -0.9 | -0.7 | -0.4 | V |
| Positive Clamp Level @ I ${ }_{\text {demag }}=125 \mu \mathrm{~A}$ | $\begin{aligned} & \mathrm{V}_{\text {cl-pos- }} \\ & \text { dem-H } \end{aligned}$ | 2.05 | 2.3 | 2.8 | V |
| Positive Clamp Level @ $\mathrm{I}_{\text {demag }}=25 \mu \mathrm{~A}$ | $\begin{aligned} & \mathrm{V}_{\text {Cl-pos- }} \\ & \text { dem-L } \end{aligned}$ | 1.4 | 1.7 | 1.9 | V |

## OVERTEMPERATURE SECTION

| Trip Level Over Temperature | $\mathrm{T}_{\text {high }}$ | - | 160 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Hysteresis | $\mathrm{T}_{\text {hyst }}$ | - | 30 | - | ${ }^{\circ} \mathrm{C}$ |

STAND-BY MAXIMUM CURRENT REDUCTION SECTION

| Normal Mode Recovery Demag Pin Current Threshold | $I_{\text {dem-NM }}$ | 20 | 25 | 30 | $\mu \mathrm{~A}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |

K FACTORS SECTION FOR PULSED MODE OPERATION

| $I_{\text {ccs }} / \mathrm{I}_{\text {stup }}$ | MC44608P40 | $10 \times \mathrm{K} 1$ | 2.4 | 2.9 | 3.8 | - |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Iccs $/ I_{\text {stup }}$ | MC44608P75 | $10 \times \mathrm{K} 1$ | 2.8 | 3.3 | 4.2 | - |
| $\mathrm{I}_{\text {ccs }} / \mathrm{I}_{\text {stup }}$ | MC44608P100 | $10 \times \mathrm{K} 1$ | 3.1 | 7.0 | 4.5 | - |
| $\mathrm{I}_{\text {CLL }} / \mathrm{I}_{\text {stup }}$ |  | $10^{3} \times \mathrm{K} 2$ | 46 | 52 | 63 | - |
| $\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 2\right) /\left(\mathrm{V}_{\text {stup }}-\right.$ UVLO1 $)$ |  | $10^{2} \times \mathrm{K}_{\text {sstup }}$ | 1.8 | 2.2 | 2.6 | - |
| (UVLO1 - UVLO2) / ( $\mathrm{V}_{\text {stup }}$ - UVLO1) |  | $10^{2} \times \mathrm{K}_{\text {sl }}$ | 90 | 120 | 150 | - |
| $\mathrm{I}_{\text {cs }} / \mathrm{V}_{\text {csth }}$ |  | $10^{6} \times \mathrm{Y}_{\text {cstby }}$ | 175 | 198 | 225 | - |
| Demag ratio $\mathrm{I}_{\text {ovp }} / \mathrm{I}_{\text {dem }} \mathrm{NM}$ |  | Dmgr | 3.0 | 4.7 | 5.5 | - |
| ( $\mathrm{V}_{1.0} \mathrm{~mA}$ - V3 0.5 mA ) / $(1.0 \mathrm{~mA}-0.5 \mathrm{~mA})$ |  | R3 | - | 1800 | - | $\Omega$ |
| $\mathrm{V}_{\text {control }}$ Latch-off |  | V3 | - | 4.8 | - | V |

## SUPPLY SECTION

| Minimum Start-up Voltage | $\mathrm{V}_{\text {ilow }}$ | - | - | 50 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ Start-up Voltage | $\mathrm{V}_{\text {stup-th }}$ | 12.5 | 13.1 | 13.8 | V |
| Output Disabling $\mathrm{V}_{\text {CC }}$ Voltage After Turn On | $\mathrm{V}_{\text {uvlo } 1}$ | 9.5 | 10 | 10.5 | V |
| Hysteresis ( $\mathrm{V}_{\text {stup-th }}-\mathrm{V}_{\text {uvlo1 }}$ ) | $\mathrm{H}_{\text {stup-uvlo1 }}$ | - | 3.1 | - | V |
| $\mathrm{V}_{\mathrm{CC}}$ Undervoltage Lockout Voltage | $\mathrm{V}_{\text {uvlo2 }}$ | 6.2 | 6.6 | 7.0 | V |
| Hysteresis ( $\mathrm{V}_{\text {uvlo1 }}-\mathrm{V}_{\text {uvlo2 }}$ ) | $\mathrm{H}_{\text {uvl01-uvlo2 }}$ | - | 3.4 | - | V |
| Absolute Normal Condition $\mathrm{V}_{\mathrm{CC}}$ Start Current $@\left(\mathrm{~V}_{\mathrm{i}}=100 \mathrm{~V}\right)$ and ( $\mathrm{V}_{\mathrm{CC}}=9.0 \mathrm{~V}$ ) | -(lcc) | 7.0 | 9.5 | 12.8 | mA |
| $\begin{array}{ll}\text { Switching Phase Supply Current (no load) } & \text { MC44608P40 } \\ & \text { MC44608P75 } \\ & \text { MC44608P100 }\end{array}$ | Iccs | $\begin{aligned} & 2.0 \\ & 2.4 \\ & 2.6 \end{aligned}$ | $\begin{aligned} & 2.6 \\ & 3.2 \\ & 3.4 \end{aligned}$ | $\begin{aligned} & \hline 3.6 \\ & 4.0 \\ & 4.5 \end{aligned}$ | mA |
| Latched Off Phase Supply Current | ICC-latch | 0.3 | 0.5 | 0.68 | mA |
| Hiccup Mode Duty Cycle (no load) | $\delta_{\text {Hiccup }}$ | - | 10 | - | \% |

2. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V . Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. This function can be inhibited by connecting pin 1 to GND.
4. Guaranteed by design (non tested).

PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
| :---: | :---: | :---: |
| 1 | Demag | The Demag pin offers 3 different functions: Zero voltage crossing detection ( 50 mV ), $24 \mu \mathrm{~A}$ current detection and $120 \mu \mathrm{~A}$ current detection. The $24 \mu \mathrm{~A}$ level is used to detect the secondary reconfiguration status and the $120 \mu \mathrm{~A}$ level to detect an Over Voltage status called Quick OVP. |
| 2 | $\mathrm{I}_{\text {sense }}$ | The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the power MOSFET. When $I_{\text {sense }}$ reaches 1.0 V , the Driver output (pin 5 ) is disabled. This is known as the Over Current Protection function. A $200 \mu \mathrm{~A}$ current source is flowing out of the pin 3 during the start-up phase and during the switching phase in case of the Pulsed Mode of operation. A resistor can be inserted between the sense resistor and the pin 2 , thus a programmable peak current detection can be performed during the SMPS stand-by mode. |
| 3 | Control Input | A feedback current from the secondary side of the SMPS via the opto-coupler is injected into this pin. A resistor can be connected between this pin and GND to allow the programming of the Burst duty cycle during the Stand-by mode. |
| 4 | Ground | This pin is the ground of the primary side of the SMPS. |
| 5 | Driver | The current and slew rate capability of this pin are suited to drive Power MOSFETs. |
| 6 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the IC. The driver output gets disabled when the voltage becomes higher than 15 V and the operating range is between 6.6 V and 13 V . An intermediate voltage level of 10 V creates a disabling condition called Latched Off phase. |
| 7 |  | This pin is to provide isolation between the $\mathrm{V}_{\mathrm{i}}$ pin 8 and the $\mathrm{V}_{\mathrm{CC}}$ pin 6. |
| 8 | $\mathrm{V}_{\mathrm{i}}$ | This pin can be directly connected to a 500 V voltage source for start-up function of the IC. During the Start-up phase a 9.0 mA current source is internally delivered to the $\mathrm{V}_{\mathrm{CC}}$ pin 6 allowing a rapid charge of the $\mathrm{V}_{\mathrm{CC}}$ capacitor. As soon as the IC starts-up, this current source is disabled. |

## OPERATING DESCRIPTION

## Regulation



Figure 2. Regulator

The pin 3 senses the feedback current provided by the opto coupler. During the switching phase the switch S2 is closed and the shunt regulator is accessible by the pin 3 . The shunt regulator voltage is typically 5.0 V . The dynamic resistance of the shunt regulator represented by the zener diode is $20 \Omega$. The gain of the Control input is given on Figure 11 which shows the duty cycle as a function of the current injected into the pin 3 .

A 4.0 kHz filter network is inserted between the shunt regulator and the PWM comparator to cancel the high frequency residual noise.

The switch S3 is closed in Stand-by mode during the Latched Off Phase while the switch S2 remains open. (See section PULSED MODE DUTY CYCLE CONTROL).
The resistor Rdpulsed (Rduty cycle burst) has no effect on the regulation process. This resistor is used to determine the burst duty cycle described in the chapter "Pulsed Duty Cycle Control" on page 8.

## PWM Latch

The MC44608 works in voltage mode. The on-time is controlled by the PWM comparator that compares the oscillator sawtooth with the regulation block output (refer to the block diagram on page 2).
The PWM latch is initialized by the oscillator and is reset by the PWM comparator or by the current sense comparator in case of an over current. This configuration ensures that only a single pulse appears at the circuit output during an oscillator cycle.

## Current Sense

The inductor current is converted to a positive voltage by inserting a ground reference sense resistor $\mathrm{R}_{\text {Sense }}$ in series with the power switch.
The maximum current sense threshold is fixed at 1.0 V . The peak current is given by the following equation:

$$
\mathrm{Ipk}_{\text {max }}=\frac{1}{\mathrm{R}_{\text {sense }^{(\Omega)}}}(\mathrm{A})
$$

In stand-by mode, this current can be lowered as due to the activation of a $200 \mu \mathrm{~A}$ current source:

$$
\mathrm{Ipk}_{\max -\mathrm{stby}}=\frac{1-\left(\mathrm{R}_{\mathrm{cs}}(\mathrm{k} \Omega) \times 0,2\right)}{\mathrm{R}_{\mathrm{sense}^{(\Omega)}}(\mathrm{A})}
$$



Figure 3. Current Sense

The current sense input consists of a filter ( $6.0 \mathrm{k} \Omega, 4.0 \mathrm{pF}$ ) and of a leading edge blanking. Thanks to that, this pin is not sensitive to the power switch turn on noise and spikes and practically in most applications, no filtering network is required to sense the current.

Finally, this pin is used:

- as a protection against over currents (Isense $>\mathrm{I}$ )
- as a reduction of the peak current during a Pulsed Mode switching phase.

The overcurrent propagation delay is reduced by producing a sharp output turn off (high slew rate). This results in an abrupt output turn off in the event of an over current and in the majority of the pulsed mode switching sequence.

## Demagnetization Section

The MC44608 demagnetization detection consists of a comparator designed to compare the $\mathrm{V}_{\mathrm{CC}}$ winding voltage to a reference that is typically equal to 50 mV .

This reference is chosen low to increase effectiveness of the demagnetization detection even during start-up.

A latch is incorporated to turn the demagnetization block output into a low level as soon as a voltage less than 50 mV is detected, and to keep it in this state until a new pulse is generated on the output. This avoids any ringing on the input signal which may alter the demagnetization detection.

For a higher safety, the demagnetization block output is also directly connected to the output, which is disabled during the demagnetization phase.

The demagnetization pin is also used for the quick, programmable OVP. In fact, the demagnetization input current is sensed so that the circuit output is latched off when this current is detected as higher than $120 \mu \mathrm{~A}$.


Figure 4. Demagnetization Block
This function can be inhibited by grounding it but in this case, the quick and programmable OVP is also disabled.

## Oscillator

The MC44608 contains a fixed frequency oscillator. It is built around a fixed value capacitor CT successively charged and discharged by two distinct current sources ICH and IDCH. The window comparator senses the CT voltage value and activates the sources when the voltage is reaching the 2.4 V/4.0 V levels.


Figure 5. Oscillator Block
The complete demagnetization status DMG is used to inhibit the recharge of the CT capacitor. Thus in case of incomplete transformer demagnetization the next switching cycle is postpone until the DMG signal appears. The oscillator remains at 2.4 V corresponding to the sawtooth valley voltage. In this way the SMPS is working in the so called SOPS mode (Self Oscillating Power Supply). In that case the effective switching frequency is variable and no longer depends on the oscillator timing but on the external working conditions (Refer to DMG signal in the Figure 6).


Figure 6.

The OSC and Clock signals are provided according to the Figure 6. The Clock signals correspond to the CT capacitor discharge. The bottom curve represents the current flowing in the sense resistor Rcs. It starts from zero and stops when the sawtooth value is equal to the control voltage Vcont. In this way the SMPS is regulated with a voltage mode control.

## Overvoltage Protection

The MC44608 offers two OVP functions:

- a fixed function that detects when $\mathrm{V}_{\mathrm{CC}}$ is higher than 15.4 V
- a programmable function that uses the demag pin. The current flowing into the demag pin is mirrored and compared to the reference current $\operatorname{Iovp}(120 \mu \mathrm{~A})$. Thus this OVP is quicker as it is not impacted by the $\mathrm{V}_{\mathrm{CC}}$ inertia and is called QOVP.

In both cases, once an OVP condition is detected, the output is latched off until a new circuit START-UP.

## Start-up Management

The $V_{i}$ pin 8 is directly connected to the HV DC rail Vin. This high voltage current source is internally connected to the $V_{C C}$ pin and thus is used to charge the $V_{C C}$ capacitor. The $\mathrm{V}_{\mathrm{CC}}$ capacitor charge period corresponds to the Start-up phase. When the $\mathrm{V}_{\mathrm{CC}}$ voltage reaches 13 V , the high voltage 9.0 mA current source is disabled and the device starts working. The device enters into the switching phase.

It is to be noticed that the maximum rating of the $\mathrm{V}_{\mathrm{i}}$ pin 8 is 500 V . ESD protection circuitry is not currently added to this pin due to size limitations and technology constraints. Protection is limited by the drain-substrate junction in avalanche breakdown. To help increase the application safety against high voltage spike on that pin it is possible to insert a small wattage $1.0 \mathrm{k} \Omega$ series resistor between the $\mathrm{V}_{\mathrm{in}}$ rail and pin 8.

The Figure 7 shows the $\mathrm{V}_{\mathrm{CC}}$ voltage evolution in case of no external current source providing current into the $\mathrm{V}_{\mathrm{CC}}$ pin during the switching phase. This case can be encountered in SMPS when the self supply through an auxiliary winding is not present (strong overload on the SMPS output for example). The Figure 17 also depicts this working configuration.


Figure 7. Hiccup Mode
In case of the hiccup mode, the duty cycle of the switching phase is in the range of $10 \%$.

## Mode Transition

The LW latch Figure 8 is the memory of the working status at the end of every switching sequence.

Two different cases must be considered for the logic at the termination of the SWITCHING PHASE:

1. No Over Current was observed
2. An Over Current was observed

These 2 cases are corresponding to the signal labelled NOC in case of "No Over Current" and "OC" in case of Over Current. So the effective working status at the end of the ON time memorized in LW corresponds to $\mathrm{Q}=1$ for no over current and $\mathrm{Q}=0$ for over current.

This sequence is repeated during the Switching phase.
Several events can occur:

1. SMPS switch OFF
2. SMPS output overload
3. Transition from Normal to Pulsed Mode
4. Transition from Pulsed Mode to Normal Mode


Figure 8. Transition Logic

## - 1. SMPS SWITCH OFF

When the mains is switched OFF, so long as the bulk electrolithic bulk capacitor provides energy to the SMPS, the controller remains in the switching phase. Then the peak current reaches its maximum peak value, the switching frequency decreases and all the secondary voltages are reduced. The $\mathrm{V}_{\mathrm{CC}}$ voltage is also reduced. When $\mathrm{V}_{\mathrm{CC}}$ is equal to 10 V , the SMPS stops working.

## - 2. Overload

In the hiccup mode the 3 distinct phases are described as follows (refer to Figure 7):

The SWITCHING PHASE: The SMPS output is low and the regulation block reacts by increasing the ON time (dmax $=80 \%$ ). The OC is reached at the end of every switching cycle. The LW latch (Figure 8) is reset before the VPWM signal appears. The SMPS output voltage is low. The $\mathrm{V}_{\mathrm{CC}}$ voltage cannot be maintained at a normal level as the auxiliary winding provides a voltage which is also reduced in a ratio similar to the one on the output (i.e. Vout nominal / Vout short-circuit). Consequently the $\mathrm{V}_{\mathrm{CC}}$ voltage is reduced at an operating rate given by the combination $\mathrm{V}_{\mathrm{CC}}$ capacitor value together with the $\mathrm{I}_{\mathrm{CC}}$ working consumption ( 3.2 mA ) according to the equation 2 . When $\mathrm{V}_{\mathrm{CC}}$ crosses 10V the WORKING PHASE gets terminated. The LW latch remains in the reset status.

The LATCHED-OFF PHASE: The $\mathrm{V}_{\mathrm{CC}}$ capacitor voltage continues to drop. When it reaches 6.5 V this phase is terminated. Its duration is governed by equation 3 .

The START-UP PHASE is reinitiated. The high voltage start-up current source $\left(-\mathrm{I}_{\mathrm{CC} 1}=9.0 \mathrm{~mA}\right)$ is activated and the MODE latch is reset. The $\mathrm{V}_{\mathrm{CC}}$ voltage ramps up according to the equation 1 . When it reaches 13 V , the IC enters into the SWITCHING PHASE.

The NEXT SWITCHING PHASE: The high voltage current source is inhibited, the MODE latch $(\mathrm{Q}=0)$ activates the NORMAL mode of operation. Figure 3 shows that no current is injected out pin 2 . The over current sense level corresponds to 1.0 V .

As long as the overload is present, this sequence repeats. The SWITCHING PHASE duty cycle is in the range of $10 \%$.

## - 3. Transition from Normal to Pulsed Mode

In this sequence the secondary side is reconfigured (refer to the typical application schematic on page 13). The high voltage output value becomes lower than the NORMAL mode regulated value. The TL431 shunt regulator is fully OFF. In the SMPS stand-by mode all the SMPS outputs are lowered except for the low voltage output that supply the wake-up circuit located at the isolated side of the power supply. In that mode the secondary regulation is performed by the zener diode connected in parallel to the TL431.

The secondary reconfiguration status can be detected on the SMPS primary side by measuring the voltage level present on the auxiliary winding Laux. (Refer to the Demagnetization Section). In the reconfigured status, the Laux voltage is also reduced. The $\mathrm{V}_{\mathrm{CC}}$ self-powering is no longer possible thus the SMPS enters in a hiccup mode similar to the one described under the Overload condition.

In the SMPS stand-by mode the 3 distinct phases are:
The SWITCHING PHASE: Similar to the Overload mode. The current sense clamping level is reduced
according to the equation of the current sense section, page 5 . The C.S. clamping level depends on the power to be delivered to the load during the SMPS stand-by mode. Every switching sequence ON/OFF is terminated by an OC as long as the secondary Zener diode voltage has not been reached. When the Zener voltage is reached the ON cycle is terminated by a true PWM action. The proper SWITCHING PHASE termination must correspond to a NOC condition. The LW latch stores this NOC status.

The LATCHED OFF PHASE: The MODE latch is set.
The START-UP PHASE is similar to the Overload Mode. The MODE latch remains in its set status $(\mathrm{Q}=1)$.

The SWITCHING PHASE: The Stand-by signal is validated and the $200 \mu \mathrm{~A}$ is sourced out of the Current Sense pin 2.

## - 4. Transition from Stand-by to Normal

The secondary reconfiguration is removed. The regulation on the low voltage secondary rail can no longer be achieved, thus at the end of the SWITCHING PHASE, no PWM condition can be encountered. The LW latch is reset.
At the next WORKING PHASE a NORMAL mode status takes place.

In order to become independent of the recovery time constant on the secondary side of the SMPS an additional reset input R2 is provided on the MODE latch. The condition Idemag $<24 \mu \mathrm{~A}$ corresponds to the activation of the secondary reconfiguration status. The R2 reset insures a direct return into the Normal Mode.

## Pulsed Mode Duty Cycle Control

During the sleep mode of the SMPS the switch S3 is closed and the control input pin 3 is connected to a 4.6 V voltage source thru a $500 \Omega$ resistor. The discharge rate of the $\mathrm{V}_{\mathrm{CC}}$ capacitor is given by $\mathrm{I}_{\mathrm{CC} \text {-latch }}$ (device consumption during the LATCHED OFF phase) in addition to the current drawn out of the pin 3. Connecting a resistor between the Pin 3 and GND ( $\mathrm{R}_{\text {DPULSED }}$ ) a programmable current is drawn from the $\mathrm{V}_{\mathrm{CC}}$ through pin 3. The duration of the LATCHED OFF phase is impacted by the presence of the resistor R $_{\text {DPULSED. }}$. The equation 3 shows the relation to the pin 3 current.

## Pulsed Mode Phases

Equations 1 through 8 define and predict the effective behavior during the PULSED MODE operation. The equations 6,7 , and 8 contain $\mathrm{K}, \mathrm{Y}$, and D factors. These factors are combinations of measured parameters. They appear in the parameter section "Kfactors for pulsed mode operation" page 4 . In equations 3 through 8 the pin 3 current is the current defined in the above section "Pulsed Mode Duty Cycle Control".

## EQUATION 1

Start-up Phase Duration:

$$
\mathrm{t}_{\text {start-up }}=\frac{\mathrm{C}_{\mathrm{Vcc}} \times\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 2\right)}{\mathrm{I}_{\text {stup }}}
$$

where: $I_{\text {stup }}$ is the start-up current flowing through $V_{C C}$ pin
$\mathrm{C}_{\mathrm{Vcc}}$ is the $\mathrm{V}_{\mathrm{CC}}$ capacitor value

## EQUATION 2

Switching Phase Duration:

$$
\mathrm{t}_{\text {switch }}=\frac{\mathrm{C}_{\mathrm{V}_{c c}} \times\left(\mathrm{V}_{\text {stup }}-\text { UVLO1 }\right)}{\mathrm{I}_{\mathrm{ccS}}+\mathrm{I}_{\mathrm{G}}}
$$

where: $I_{C C S}$ is the no load circuit consumption in switching phase $I_{G}$ is the current consumed by the Power Switch

## EQUATION 3

Latched-off Phase Duration:

$$
\mathrm{t}_{\text {latched }- \text { off }}=\frac{\mathrm{C}_{\mathrm{Vcc}} \times(\mathrm{UVLO} 1-\text { UVLO2 })}{\mathrm{I}_{\mathrm{ccL}}+\mathrm{I}_{\mathrm{pin} 3}}
$$

where: $I_{\mathrm{CCL}}$ is the latched off phase consumption
$I_{\text {pin3 }}$ is the current drawn from pin3 adding a resistor

## EQUATION 4

Burst Mode Duty Cycle:

$$
d_{B M}=\frac{t_{\text {switch }}}{t_{\text {start }- \text { up }}+t_{\text {switch }}+t_{\text {latched-off }}}
$$

## EQUATION 5

$$
d_{B M}=\frac{\frac{C_{V c c} \times\left(V_{\text {stup }}-U V L O 1\right)}{I_{c c S}+I_{G}}}{\frac{C_{V c c} \times\left(V_{\text {stup }}-U V L O 2\right)}{I_{\text {stup }}}+\frac{C_{V_{c c}} \times\left(V_{\text {stup }}-U V L O 1\right)}{I_{c c S}+I_{G}}+\frac{C_{V_{c c}} \times(U V L O 1-U V L O 2)}{I_{c c L}+I_{\text {pin3 }}}}
$$

## EQUATION 6

$$
\mathrm{d}_{\mathrm{BM}}=\frac{1}{1+\left(\mathrm{k}_{\mathrm{S} / \text { Stup }} \times \frac{\mathrm{I}_{\mathrm{CCS}}+\mathrm{I}_{\mathrm{G}}}{\mathrm{I}_{\text {stup }}}\right)+\left(\mathrm{k}_{\mathrm{S} / \mathrm{L}} \times \frac{\mathrm{I}_{\mathrm{ccS}}+\mathrm{I}_{\mathrm{G}}}{\mathrm{I}_{\mathrm{ccL}}+\mathrm{I}_{\mathrm{pin} 3}}\right)}
$$

where: $\mathrm{k}_{\mathrm{S} / \text { Stup }}=\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 2\right) /\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 1\right)$
$\mathrm{k}_{\mathrm{S} / \mathrm{L}}=(\mathrm{UVLO} 1-\mathrm{UVLO} 2) /\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 1\right)$

## EQUATION 7

$$
\mathrm{d}_{\mathrm{BM}}=\frac{1}{1+\left(\frac{\mathrm{I}_{\mathrm{CCS}}+\mathrm{I}_{\mathrm{G}}}{\mathrm{I}_{\text {stup }}} \times\left(\mathrm{k}_{\mathrm{S} / \text { Stup }}+\left(\mathrm{k}_{\mathrm{S} / \mathrm{L}} \times \frac{\mathrm{I}_{\text {stup }}}{\mathrm{I}_{\mathrm{ccL}}+\mathrm{I}_{\text {pin3 }}}\right)\right)\right.}
$$

## EQUATION 8

$$
\mathrm{d}_{\mathrm{BM}}=\frac{1}{1+\left\{\left(\mathrm{k} 1+\frac{\mathrm{I}_{\mathrm{G}}}{\mathrm{I}_{\text {stup }}}\right) \times\left(\mathrm{k}_{\mathrm{S} / \text { Stup }}+\left(\mathrm{k}_{\mathrm{S} / \mathrm{L}} \times \frac{1}{\mathrm{k} 2+\left(\frac{\mathrm{I}_{\text {pin3 }}}{I_{\text {stup }}}\right)}\right)\right]\right\}}
$$

where: $\mathrm{k} 1=\mathrm{I}_{\text {ccs }} / \mathrm{I}_{\text {stup }}$
$\mathrm{k} 2=\mathrm{I}_{\mathrm{ccL}} / \mathrm{s}_{\text {stup }}$
$\mathrm{k}_{\mathrm{S} / \text { Stup }}=\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 2\right) /\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 1\right)$
$\mathrm{k}_{\mathrm{S} / \mathrm{L}}=(\mathrm{UVLO} 1-\mathrm{UVLO} 2) /\left(\mathrm{V}_{\text {stup }}-\mathrm{UVLO} 1\right)$

## PULSED MODE CURRENT SENSE CLAMPING LEVEL

Equations 9, 10, 11 and 12 allow the calculation of the Rcs value for the desired maximum current peak value during the SMPS stand-by mode.

## EQUATION 9

$$
\text { Ipk }_{\text {stby }}=\frac{\mathrm{V}_{\mathrm{cs}-\mathrm{th}}-\left(\mathrm{R}_{\mathrm{cs}} \times \mathrm{I}_{\mathrm{cs}}\right)}{\mathrm{R}_{\mathrm{S}}}
$$

where: $\mathrm{V}_{\mathrm{cs}-\mathrm{th}}$ is the CS comparator threshold
$\mathrm{I}_{\text {CS }}$ is the CS internal current source
$R_{S}$ is the sensing resistor
$R_{\text {cs }}$ is the resistor connected between pin 2 and $R_{S}$

## EQUATION 10

$$
\mathrm{Ipk}_{\mathrm{stby}}=\mathrm{V}_{\mathrm{cs}-\mathrm{th}} \times \frac{1-\left(\mathrm{R}_{\mathrm{cs}} \times \frac{\mathrm{I}_{\mathrm{cs}}}{\mathrm{~V}_{\mathrm{cs}-\mathrm{th}}}\right)}{\mathrm{R}_{\mathrm{S}}}
$$

## EQUATION 11

$$
\mathrm{lpk}_{\mathrm{stby}}=\mathrm{V}_{\mathrm{cs}-\mathrm{th}} \times \frac{1-\left(\mathrm{R}_{\mathrm{cs}} \times \mathrm{Y}_{\mathrm{cs}-\mathrm{stby}}\right)}{\mathrm{R}_{\mathrm{S}}}
$$

where: $\mathrm{Y}_{\text {cs-stby }}=\mathrm{I}_{\text {cs }} / \mathrm{V}_{\text {cs-th }}$
Taking into account the circuit propagation delay ( $\delta \mathrm{t}_{\mathrm{cs}}$ ) and the Power Switch reaction time ( $\delta \mathrm{t}_{\mathrm{ps}}$ ):
EQUATION 12

$$
\text { Ipk }_{\text {stby }}=\left[V_{\mathrm{cs}-\mathrm{th}} \times \frac{1-\left(\mathrm{R}_{\mathrm{cs}} \times \mathrm{Y}_{\mathrm{cs}-\mathrm{stby}}\right)}{R_{\mathrm{S}}}\right]+\frac{\mathrm{V}_{\mathrm{in}} \times\left(\delta \mathrm{t}_{\mathrm{cs}}+\delta \mathrm{t}_{\mathrm{ps}}\right)}{\mathrm{L}_{\mathrm{p}}}
$$



Figure 9. Output Switching Speed


Figure 11. Duty Cycle Control


Figure 13. Vpin3 During the Latched Off Period


Figure 10. Frequency Stability


Figure 12. Vpin3 During the Working Period


Figure 14. Device Consumption when Switching


Figure 15. High Voltage Current Source


Figure 16. Overload Burst Mode


Figure 17. Hiccup Mode Waveforms

The data in Figure 16 corresponds to the waveform in Figure 17. The Figure 17 shows $\mathrm{V}_{\mathrm{CC}}, \mathrm{I}_{\mathrm{CC}}, \mathrm{I}_{\text {sense }}(\mathrm{pin} 2)$ and $\mathrm{V}_{\text {out }}$ (pin 5). $\mathrm{V}_{\text {out }}$ (pin 5) in fact shows the envelope of the
output switching pulses. This mode corresponds to an overload condition.

The Figure 19 represents a complete power supply using the secondary reconfiguration.

| The specification is as follows: | Input source: <br>  <br> 3 Outputs | 85 Vac to 265 Vac |
| :--- | :--- | :--- |
|  | $112 \mathrm{~V} / 0.45 \mathrm{~A}$ |  |
|  | $16 \mathrm{~V} / 1.5 \mathrm{~A}$ |  |
|  | Output power | $8.0 \mathrm{~V} / 1.0 \mathrm{~A}$ |
|  | 80 W |  |
|  | Stand-by mode | @ Pout $=300 \mathrm{~mW}, 1.3 \mathrm{~W}$ |



Figure 18. Typical Application

The secondary reconfiguration is activated by the $\mu \mathrm{P}$ through the switch. The dV/dt appearing on the high voltage winding (pins 14 of the transformer) at every TMOS switch off, produces a current spike through the series RC network R7, C17. According to the switch position this spike is either absorbed by the ground (switch closed) or flows into the thyristor gate (switch open) thus firing the MCR22-6. The closed position of the switch corresponds to the Pulsed Mode activation. In this secondary side SMPS status the high voltage winding (12-14) is connected through D12 and DZ 1 to the 8.0 V low voltage secondary rail. The voltages
applied to the secondary windings $12-14,10-11$ and $6-7$ (Vaux) are thus divided by ratio N12-14 / N9-8 (number of turns of the winding 12-14 over number of turns of the winding 9-8). In this reconfigured status all the secondary voltages are lowered except the 8.0 V one. The regulation during every pulsed or burst is performed by the zener diode DZ3 which value has to be chosen higher than the normal mode regulation level. This working mode creates a voltage ripple on the 8.0 V rail which generally must be post regulated for the microProcessor supply.


Figure 19. SMPS Pulsed Mode

The Figure 19 shows the SMPS behavior while working in the reconfigured mode. The top curve represents the $\mathrm{V}_{\mathrm{CC}}$ voltage (pin 6 of the MC44608). The middle curve represents the 8.0 V rail. The regulation is taking place at 11.68 V . On the bottom curve the pin 2 voltage is shown. This voltage represents the current sense signal. The pin 2
voltage is the result of the $200 \mu \mathrm{~A}$ current source activated during the start-up phase and also during the working phase which flows through the R4 resistor. The used high resolution mode of the oscilloscope does not allow to show the effective ton current flowing in the sensing resistor R11.

## PWM Current-Mode Controller for Low-Power Universal Off-Line Supplies

Housed in SO-8 or DIP-8 package, the NCP1200 represents a major leap toward ultra-compact Switch-Mode Power Supplies. Thanks to a novel concept, the circuit allows the implementation of a complete offline battery charger or a standby SMPS with few external components. Furthermore, an integrated output short-circuit protection lets the designer build an extremely low-cost AC/DC wall adapter associated with a simplified feedback scheme.

With an internal structure operating at a fixed $40 \mathrm{kHz}, 60 \mathrm{kHz}$ or 100 kHz , the controller drives low gate-charge switching devices like an IGBT or a MOSFET thus requiring a very small operating power. Thanks to current-mode control, the NCP1200 drastically simplifies the design of reliable and cheap offline converters with extremely low acoustic generation and inherent pulse-by-pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the skip cycle mode and provides excellent efficiency at light loads. Because this occurs at low peak current, no acoustic noise takes place.

Finally, the IC is self-supplied from the DC rail, eliminating the need of an auxiliary winding. This feature ensures operation in presence of low output voltage or shorts.

## Features

- No Auxiliary Winding Operation
- Internal Output Short-Circuit Protection
- Extremely Low No-Load Standby Power
- Current-Mode with Skip-Cycle Capability
- Internal Leading Edge Blanking
- 110 mA Peak Current Source/Sink Capability
- Internally Fixed Frequency at $40 \mathrm{kHz}, 60 \mathrm{kHz}$ and 100 kHz
- Direct Optocoupler Connection
- Built-in Frequency Jittering for Lower EMI
- SPICE Models Available for TRANsient and AC Analysis
- Internal Temperature Shutdown


## Typical Applications

- AC/DC Adapters
- Offline Battery Chargers
- Auxiliary/Ancillary Power Supplies (USB, Appliances, TVs, etc.)


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## PIN CONNECTIONS


(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 995 of this data sheet.


Figure 1. Typical Application

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Function | Description |
| :---: | :---: | :--- | :--- |
| 1 | Adj | Adjust the skipping peak current | This pin lets you adjust the level at which the cycle skipping process <br> takes place |
| 2 | FB | Sets the peak current setpoint | By connecting an optocoupler to this pin, the peak current setpoint is <br> adjusted accordingly to the output power demand |
| 3 | CS | Current sense input | This pin senses the primary current and routes it to the internal <br> comparator via an L.E.B |
| 4 | Gnd | The IC ground |  |
| 5 | Drv | Driving pulses | The driver's output to an external MOSFET |
| 6 | VCC | Supplies the IC | This pin is connected to an external bulk capacitor of typically $10 \mu \mathrm{~F}$ |
| 7 | NC | No Connection | This un-connected pin ensures adequate creepage distance |
| 8 | HV | Generates the $\mathrm{V}_{\mathrm{CC}}$ from the line | Connected to the high-voltage rail, this pin injects a constant current into <br> the $\mathrm{V}_{\mathrm{CC}}$ bulk capacitor |



Figure 2. Internal Circuit Architecture

## MAXIMUM RATINGS

| Rating | Symbol | Value | Units |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 16 | V |
| Thermal Resistance Junction-to-Air, PDIP8 version | $\mathrm{R}_{\theta \mathrm{JA}}$ | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance Junction-to-Air, SOIC version | $\mathrm{R}_{\theta \mathrm{JA}}$ | 178 |  |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{Jmax}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Typical Temperature Shutdown | - | 140 |  |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Capability, HBM model (All pins except $\mathrm{V}_{\mathrm{CC}}$ and HV$)$ | - | 2.0 | kV |
| ESD Capability, Machine model | - | 200 | V |
| Maximum Voltage on pin $8(\mathrm{HV})$, pin $6\left(\mathrm{~V}_{\mathrm{CC}}\right)$ grounded | - | 450 | V |
| Maximum Voltage on pin $8(\mathrm{HV})$, pin $6\left(\mathrm{~V}_{\mathrm{CC}}\right)$ decoupled to ground with $10 \mu \mathrm{~F}$ | - | 500 | V |

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{J}=-25^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, Max $\mathrm{T}_{J}=150^{\circ} \mathrm{C}$,
$\mathrm{V}_{\mathrm{CC}}=11 \mathrm{~V}$ unless otherwise noted)

| Rating | Pin | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

DYNAMIC SELF-SUPPLY (All frequency versions, otherwise noted)

| $\mathrm{V}_{\text {CC }}$ increasing level at which the current source turns-off | 6 | $\mathrm{V}_{\text {CCOFF }}$ | 10.3 | 11.4 | 12.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ decreasing level at which the current source turns-on | 6 | $\mathrm{V}_{\text {CCON }}$ | 8.8 | 9.8 | 11 | V |
| $\mathrm{V}_{\text {CC }}$ decreasing level at which the latch-off phase ends | 6 | $\mathrm{V}_{\text {CClatch }}$ | - | 6.3 | - | V |
| Internal IC Consumption, no output load on pin 6 | 6 | $\mathrm{I}_{\mathrm{CC} 1}$ | - | 710 | $\begin{gathered} 880 \\ \text { Note } 1 \end{gathered}$ | $\mu \mathrm{A}$ |
| Internal IC Consumption, 1 nF output load on pin 6, $\mathrm{F}_{\text {Sw }}=40 \mathrm{kHz}$ | 6 | $\mathrm{I}_{\text {CC2 }}$ | - | 1.2 | 1.4 <br> Note 2 | mA |
| Internal IC Consumption, 1 nF output load on pin 6, $\mathrm{F}_{\text {SW }}=60 \mathrm{kHz}$ | 6 | $\mathrm{I}_{\mathrm{CC} 2}$ | - | 1.4 | $\begin{gathered} 1.6 \\ \text { Note } 2 \end{gathered}$ | mA |
| Internal IC Consumption, 1 nF output load on pin 6, Fsw $=100 \mathrm{kHz}$ | 6 | $\mathrm{I}_{\text {CC2 }}$ | - | 1.9 | $\begin{gathered} 2.2 \\ \text { Note } 2 \end{gathered}$ | mA |
| Internal IC Consumption, latch-off phase | 6 | $\mathrm{ICC3}^{\text {c }}$ | - | 350 | - | $\mu \mathrm{A}$ |

## INTERNAL CURRENT SOURCE

| High-voltage current source, $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | 8 | $\mathrm{I}_{\mathrm{C} 1}$ | 2.8 | 4.0 | - | mA |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| High-voltage current source, $\mathrm{V}_{\mathrm{CC}}=0$ | 8 | $\mathrm{I}_{\mathrm{C} 2}$ | - | 4.9 | - | mA |

## DRIVE OUTPUT

| Output voltage rise-time @ CL $=1 \mathrm{nF}, 10-90 \%$ of output signal | 5 | $\mathrm{~T}_{\mathrm{r}}$ | - | 67 | - | ns |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Output voltage fall-time @ CL $=1 \mathrm{nF}, 10-90 \%$ of output signal | 5 | $\mathrm{~T}_{\mathrm{f}}$ | - | 28 | - | ns |
| Source resistance (drive $=0$, Vgate $=\mathrm{V}_{\mathrm{CCHMAX}}-1 \mathrm{~V}$ ) | 5 | $\mathrm{R}_{\mathrm{OH}}$ | 27 | 40 | 61 | $\Omega$ |
| Sink resistance (drive $=11 \mathrm{~V}$, Vgate $=1 \mathrm{~V}$ ) | 5 | $\mathrm{R}_{\mathrm{OL}}$ | 5 | 12 | 20 | $\Omega$ |

CURRENT COMPARATOR (Pin 5 un-loaded)

| Input Bias Current @ 1 V input level on pin 3 | 3 | $\mathrm{I}_{\mathrm{IB}}$ | - | 0.02 | - | $\mu \mathrm{A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum internal current setpoint | 3 | $\mathrm{I}_{\text {Limit }}$ | 0.8 | 0.9 | 1.0 | V |
| Default internal current setpoint for skip cycle operation | 3 | $\mathrm{I}_{\text {Lskip }}$ | - | 350 | - | mV |
| Propagation delay from current detection to gate OFF state | 3 | $\mathrm{~T}_{\text {DEL }}$ | - | 100 | 160 | ns |
| Leading Edge Blanking Duration | 3 | $\mathrm{~T}_{\text {LEB }}$ | - | 230 | - | ns |

INTERNAL OSCILLATOR ( $\mathrm{V}_{\mathrm{CC}}=11 \mathrm{~V}$, pin 5 loaded by $1 \mathrm{k} \Omega$ )

| Oscillation frequency, 40 kHz version | - | $\mathrm{f}_{\mathrm{OSc}}$ | 36 | 42 | 48 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillation frequency, 60 kHz version | - | fosc | 52 | 61 | 70 | kHz |
| Oscillation frequency, 100 kHz version | - | $\mathrm{f}_{\mathrm{Osc}}$ | 86 | 103 | 116 | kHz |
| Built-in frequency jittering, $\mathrm{F}_{\text {SW }}=40 \mathrm{kHz}$ | - | $\mathrm{f}_{\text {jitter }}$ | - | 300 | - | $\mathrm{Hz} / \mathrm{V}$ |
| Built-in frequency jittering, $\mathrm{F}_{\text {SW }}=60 \mathrm{kHz}$ | - | $\mathrm{f}_{\text {jitter }}$ | - | 450 | - | $\mathrm{Hz} / \mathrm{V}$ |
| Built-in frequency jittering, $\mathrm{F}_{\text {SW }}=100 \mathrm{kHz}$ | - | $\mathrm{f}_{\mathrm{jitter}}$ | - | 620 | - | $\mathrm{Hz} / \mathrm{V}$ |
| Maximum duty-cycle | - | Dmax | 74 | 80 | 87 | $\%$ |

FEEDBACK SECTION (Vcc = 11 V , pin 5 loaded by $1 \mathrm{k} \Omega$ )

| Internal pull-up resistor | 2 | Rup | - | 8.0 | - |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Pin 3 to current setpoint division ratio | - | Iratio | - | 4.0 | - |

## SKIP CYCLE GENERATION

| Default skip mode level | 1 | Vskip | 1.1 | 1.4 | 1.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin 1 internal output impedance | 1 | Zout | - | 25 | - | $\mathrm{k} \Omega$ |

1. Max value @ $T_{J}=-25^{\circ} \mathrm{C}$.
2. Max value @ $T_{J}=25^{\circ} \mathrm{C}$, please see characterization curves.


Figure 3. HV Pin Leakage Current vs. Temperature


Figure 5. $\mathrm{V}_{\mathrm{Cc}}$ ON vs. Temperature

Figure 7. Icc2 vs. Temperature


Figure 4. VCc OFF vs. Temperature


Figure 6. $\mathrm{I}_{\mathrm{CC} 1}$ vs. Temperature


Figure 8. Switching Frequency vs. $\mathrm{T}_{\mathrm{J}}$


Figure 9. $\mathrm{V}_{\mathrm{Cc}}$ Latchoff vs. Temperature


Figure 11. DRV Source/Sink Resistances


Figure 13. $\mathbf{V}_{\text {skip }}$ vs. Temperature


Figure 10. I ${ }_{\text {CC3 }}$ vs. Temperature


Figure 12. Current Sense Limit vs. Temperature


Figure 14. Max Duty-Cycle vs. Temperature

## APPLICATIONS INFORMATION

## INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch-off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part-count is the key parameter, particularly in low-cost AC/DC adapters, auxiliary supplies etc. Thanks to its high-performance High-Voltage technology, the NCP1200 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low-pass filter and self-supply. This later point emphasizes the fact that ON Semiconductor's NCP1200 does NOT need an auxiliary winding to operate: the product is naturally supplied from the high-voltage rail and delivers a $\mathrm{V}_{\mathrm{CC}}$ to the IC. This system is called the Dynamic Self-Supply (DSS).

## Dynamic Self-Supply

The DSS principle is based on the charge/discharge of the $\mathrm{V}_{\mathrm{CC}}$ bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with a bunch of simple logical equations:

POWER-ON: IF $\mathrm{V}_{\mathrm{CC}}<\mathrm{V}_{\mathrm{CCOFF}}$ THEN Current Source is ON , no output pulses

IF $\mathrm{V}_{\mathrm{CC}}$ decreasing $>\mathrm{V}_{\mathrm{CCON}}$ THEN Current Source is OFF, output is pulsing
IF $\mathrm{V}_{\mathrm{CC}}$ increasing $<\mathrm{V}_{\text {CCOFF }}$ THEN Current Source is ON, output is pulsing

Typical values are: $\mathrm{V}_{\mathrm{CCOFF}}=11.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CCON}}=9.8 \mathrm{~V}$
To better understand the operational principle, Figure 15's sketch offers the necessary light:


Figure 15. The Charge/Discharge Cycle Over a $10 \mu \mathrm{~F} \mathrm{~V}_{\mathrm{cc}}$ Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge, Qg. If we select a MOSFET like the MTD1N60E, Qg equals 11 nC (max). With a maximum switching frequency of 48 kHz (for the P40 version), the average power necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:
Fsw $\cdot \mathrm{Qg} \cdot \mathrm{V}_{\mathrm{Cc}} \quad$ with
Fsw $=$ maximum switching frequency
$\mathrm{Qg}=$ MOSFET's gate charge
$\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{GS}}$ level applied to the gate
To obtain the final driver contribution to the IC consumption, simply divide this result by $\mathrm{V}_{\mathrm{CC}}$ : Idriver $=$ $\mathrm{Fsw} \cdot \mathrm{Qg}=530 \mu \mathrm{~A}$. The total standby power consumption at no-load will therefore heavily rely on the internal IC consumption plus the above driving current (altered by the driver's efficiency). Suppose that the IC is supplied from a 400 V DC line. To fully supply the integrated circuit, let's imagine the 4 mA source is ON during 8 ms and OFF during 50 ms . The IC power contribution is therefore: 400 V .4 mA
. $0.16=256 \mathrm{~mW}$. If for design reasons this contribution is still too high, several solutions exist to diminish it:

1. Use a MOSFET with lower gate charge Qg
2. Connect pin through a diode (1N4007 typically) to one of the mains input. The average value on pin 8 becomes $\frac{2 \text { * } V_{\text {mains PEAK }}}{\pi}$. Our power contribution example drops to: 160 mW .


Figure 16. A simple diode naturally reduces the average voltage on pin 8
3. Permanently force the $\mathrm{V}_{\mathrm{CC}}$ level above $\mathrm{V}_{\mathrm{CCH}}$ with an auxiliary winding. It will automatically disconnect the internal start-up source and the IC will be fully self-supplied from this winding. Again, the total power drawn from the mains will significantly decrease. Make sure the auxiliary voltage never exceeds the 16 V limit.

## Skipping Cycle Mode

The NCP1200 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so-called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 18 ). Suppose we have the following component values:
Lp, primary inductance $=1 \mathrm{mH}$
$\mathrm{F}_{\mathrm{SW}}$, switching frequency $=48 \mathrm{kHz}$
Ip skip $=300 \mathrm{~mA}$ (or $350 \mathrm{mV} /$ Rsense)
The theoretical power transfer is therefore:
$\frac{1}{2} \cdot \mathrm{Lp} \cdot \mathrm{Ip}^{2} \cdot \mathrm{Fsw}=2.2 \mathrm{~W}$
If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms , then the total power transfer is: 2.2 . $0.1=220 \mathrm{~mW}$.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:


Figure 17. Feedback Voltage Variations

When FB is above the skip cycle threshold (1.4 V by default), the peak current cannot exceed $1 \mathrm{~V} /$ Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1 / 4 (Figure 19). The user still has the flexibility to alter this 1.4 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level.


Figure 18. Output pulses at various power levels ( $\mathrm{X}=5 \mu \mathrm{~s} / \mathrm{div}$ ) $\mathrm{P} 1<\mathrm{P} 2<\mathrm{P} 3$


Figure 19. The skip cycle takes place at low peak currents which guarantees noise free operation

## Power Dissipation

The NCP1200 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1200 current consumption. The total power dissipation can be evaluated using: $\left(\mathrm{V}_{\text {HVDC }}-11 \mathrm{~V}\right) \cdot I C C 2$. If we operate the device on a 250 VAC rail, the maximum rectified voltage can go up to 350 VDC . As a result, the worse case dissipation occurs on the 100 kHz version which will dissipate $340.1 .8 \mathrm{~mA} @ \mathrm{Tj}=-25^{\circ} \mathrm{C}=612 \mathrm{~mW}$ (however this 1.8 mA number will drop at higher operating temperatures). A DIP8 package offers a junction-to-ambient thermal resistance of $\mathrm{R}_{\theta \mathrm{J}-\mathrm{A}} 100^{\circ} \mathrm{C} / \mathrm{W}$. The maximum power dissipation can thus be computed knowing the maximum operating ambient temperature (e.g. $70^{\circ} \mathrm{C}$ ) together with the maximum allowable junction temperature ( $125^{\circ} \mathrm{C}$ ): Pmax $=\frac{\mathrm{T}_{\mathrm{Jmax}}-\mathrm{T}_{\text {Amax }}}{\mathrm{R}_{\text {R日J-A }}}=550 \mathrm{~mW}$. As we can see, we do not reach the worse consumption budget imposed by the 100 kHz version. Two solutions exist to cure this trouble. The first one consists in adding some copper area around the NCP1200 DIP8 footprint. By adding a min-pad area of $80 \mathrm{~mm}^{2}$ of $35 \mu$ copper ( 1 oz .) $\mathrm{R}_{\theta \mathrm{J}-\mathrm{A}}$ drops to about $75^{\circ} \mathrm{C} / \mathrm{W}$ which allows the use of the 100 kHz version. The other solutions are:

1. Add a series diode with pin 8 (as suggested in the above lines) to drop the maximum input voltage down to $222 \mathrm{~V}((2 \times 350) / \mathrm{pi})$ and thus dissipate less than 400 mW
2. Implement a self-supply through an auxiliary winding to permanently disconnect the self-supply.
SO-8 package offers a worse $\mathrm{R}_{\theta \mathrm{J}-\mathrm{A}}$ compared to that of the DIP8 package: $178^{\circ} \mathrm{C} / \mathrm{W}$. Again, adding some copper area around the PCB footprint will help decrease this number: 12 mm x 12 mm to drop $\mathrm{R}_{\theta \mathrm{J}-\mathrm{A}}$ down to $100^{\circ} \mathrm{C} / \mathrm{W}$ with $35 \mu$ copper thickness ( 1 oz. ) or $6.5 \mathrm{~mm} \times 6.5 \mathrm{~mm}$ with $70 \mu$ copper thickness ( 2 oz .). As one can see, we do not recommend using the SO-8 package for the 100 kHz version with DSS active as the IC may not be able to sustain the power (except if you have the adequate place on your PCB). However, using the solution of the series diode or the self-supply through the auxiliary winding does not cause any problem with this frequency version. These options are thoroughly described in the AND8023/D.

## Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short-circuit protection. A short-circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.1 V , as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, the NCP1200 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty-cycle. The system recovers when the fault condition disappears.
During the start-up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time-out used by this IC works with the $\mathrm{V}_{\mathrm{CC}}$ decoupling capacitor: as soon as the $\mathrm{V}_{\mathrm{CC}}$ decreases from the $\mathrm{V}_{\mathrm{CCOFF}}$ level (typically 11.4 V ) the device internally watches for an overload current situation. If this condition is still present when $\mathrm{V}_{\mathrm{CCON}}$ is reached, the controller stops the driving pulses, prevents the self-supply current source to restart and puts all the circuitry in standby, consuming as little as $350 \mu \mathrm{~A}$ typical ( $\mathrm{I}_{\mathrm{CC} 3}$ parameter). As a result, the $\mathrm{V}_{\mathrm{CC}}$ level slowly discharges toward 0 . When this level crosses 6.3 V typical, the controller enters a new startup phase by turning the current source on: $\mathrm{V}_{\mathrm{CC}}$ rises toward 11.4 V and again delivers output pulses at the $\mathrm{UVLO}_{\mathrm{H}}$ crossing point. If the fault condition has been removed before $\mathrm{UVLO}_{\mathrm{L}}$ approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 20 shows the evolution of the signals in presence of a fault.


Figure 20. If the fault is relaxed during the $\mathrm{V}_{\mathrm{CC}}$ natural fall down sequence, the IC automatically resumes. If the fault persists when $\mathrm{V}_{\mathrm{Cc}}$ reached $\mathrm{UVLO}_{\mathrm{L}}$, then the controller cuts everything off until recovery.

## Calculating the $\mathrm{V}_{\mathrm{cc}}$ Capacitor

As the above section describes, the fall down sequence depends upon the $\mathrm{V}_{\mathrm{CC}}$ level: how long does it take for the $\mathrm{V}_{\mathrm{CC}}$ line to go from 11.4 V to 9.8 V ? The required time depends on the start-up sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 11.4 V to 9.8 V , otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6 ms . Therefore a $\mathrm{V}_{\mathrm{CC}}$ fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.5 mA , we can calculate the required capacitor using the following formula: $\Delta t=\frac{\Delta V \cdot C}{i}$, with $\Delta V=2 V$. Then for a wanted $\Delta t$ of 10 ms ,

C equals $8 \mu \mathrm{~F}$ or $10 \mu \mathrm{~F}$ for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to $350 \mu \mathrm{~A}$ typical. This appends at $\mathrm{V}_{\mathrm{CC}}=9.8 \mathrm{~V}$ and it remains stuck until $\mathrm{V}_{\mathrm{CC}}$ reaches 6.5 V : we are in latch-off phase. Again, using the calculated $10 \mu \mathrm{~F}$ and $350 \mu \mathrm{~A}$ current consumption, this latch-off phase lasts: 109 ms .

## A Typical Application

Figure 21 depicts a low-cost 3.5 W AC/DC 6.5 V wall adapter. This is a typical application where the wall-pack must deliver a raw DC level to a given internally regulated apparatus: toys, calculators, CD-players etc. Thanks to the inherent short-circuit protection of the NCP1200, you only need a bunch of components around the IC, keeping the final cost at an extremely low level. The transformer is available from different suppliers as detailed on the following page.


Figure 21. A typical AC/DC wall adapter showing the reduced part count thanks to the NCP1200

T1: Lp $=2.9 \mathrm{mH}, \mathrm{Np}: \mathrm{Ns}=1: 0.08$, leakage $=80 \mu \mathrm{H}, \mathrm{E} 16$ core, NCP1200P40
To help designers during the design stage, several manufacturers propose ready-to-use transformers for the above application, but can also develop devices based on your particular specification:

## Eldor Corporation Headquarter

Via Plinio 10,
22030 Orsenigo
(Como) Italia
Tel.: +39-031-636 111
Fax : +39-031-636 280
Email: eldor@eldor.it
www.eldor.it
ref. 1: 2262.0058C: 3.5 W version
$(\mathrm{Lp}=2.9 \mathrm{mH}$, Lleak $=80 \mu \mathrm{H}$, E16)
ref. 2: 2262.0059A: 5 W version
$(\mathrm{Lp}=1.6 \mathrm{mH}$, Lleak $=45 \mu \mathrm{H}$, E16)

## EGSTON GesmbH

Grafenbergerstraße 37
3730 Eggenburg
Austria
Tel.: +43 (2984) 2226-0
Fax : +43 (2984) 2226-61
Email: info@egston.com
http://www.egston.com/english/index.htm
ref. 1: F0095001: 3.5 W version
$(\mathrm{Lp}=2.7 \mathrm{mH}$, Lleak $=30 \mu \mathrm{H}$, sandwich configuration, E16)

## Atelier Special de Bobinage

125 cours Jean Jaures
38130 ECHIROLLES FRANCE
Tel.: 33 (0)4 76230224
Fax: 33 (0)4 76226489
Email: asb@wanadoo.fr
ref. 1: NCP1200-10 W-UM: 10 W for USB
( $\mathrm{Lp}=1.8 \mathrm{mH}, 60 \mathrm{kHz}, 1: 0.1, \mathrm{RM} 8$ pot core)

## Coilcraft

1102 Silver Lake Road
Cary, Illinois 60013 USA
Tel: (847) 639-6400
Fax: (847) 639-1469
Email: info@coilcraft.com
http://www.coilcraft.com
ref. 1: Y8844-A: 3.5 W version
$(\mathrm{Lp}=2.9 \mathrm{mH}$, Lleak $=65 \mu \mathrm{H}$, E16)
ref. 2: Y8848-A: 10 W version
$(\mathrm{Lp}=1.8 \mathrm{mH}$, Lleak $=45 \mu \mathrm{H}, 1: 01, \mathrm{E}$ core $)$

## Improving the Output Drive Capability

The NCP1200 features an asymmetrical output stage used to soften the EMI signature. Figure 22 depicts the way the driver is internally made:


Figure 22. The higher ON resistor slows down the MOSFET while the lower OFF resistor ensures fast turn-off.
In some cases, it is possible to expand the output drive capability by adding either one or two bipolar transistors. Figures 23, 24, and 25 give solutions whether you need to improve the turn-on time only, the turn-off time or both. Rd is there to damp any overshoot resulting from long copper traces. It can be omitted with short connections. Results showed a rise fall time improvement by 5 X with standard 2N2222/2N2907:


Figure 23. Improving Both Turn-On and Turn-Off Times


Figure 24. Improving Turn-Off Time Only


Figure 25. Improving Turn-On Time Only

If the leakage inductance is kept low, the MTD1N60E can withstand accidental avalanche energy, e.g. during a high-voltage spike superimposed over the mains, without the help of a clamping network. If this leakage path permanently forces a drain-source voltage above the MOSFET BVdss ( 600 V ), a clamping network is mandatory and must be built around Rclamp and Clamp. Dclamp shall react extremely fast and can be a MUR160 type. To calculate the component values, the following formulas will help you:

$$
\begin{aligned}
& \frac{\mathrm{R}_{\text {clamp }}=}{2 \cdot \mathrm{~V}_{\text {clamp }} \cdot\left(\mathrm{V}_{\text {clamp }}-\left(\mathrm{V}_{\text {out }}+\mathrm{Vf} \mathrm{sec}\right) \cdot \mathrm{N}\right)} \\
& \mathrm{L}_{\text {leak }} \cdot \mathrm{Ip}^{2} \cdot \mathrm{Fsw} \\
& \mathrm{C}_{\text {clamp }}=\frac{\mathrm{V}_{\text {clamp }}}{\mathrm{V}_{\text {ripple }} \cdot \mathrm{Fsw} \cdot \mathrm{R}_{\text {clamp }}}
\end{aligned}
$$

with:
$\mathbf{V}_{\text {clamp: }}$ the desired clamping level, must be selected to be between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.
$\mathbf{V}_{\text {out }}+\mathbf{V f}$ : the regulated output voltage level + the secondary diode voltage drop
$\mathbf{L}_{\text {leak }}$ : the primary leakage inductance
$\mathbf{N}$ : the Ns:Np conversion ratio
$\mathbf{F}_{\mathbf{S W}}$ : the switching frequency
$V_{\text {ripple: }}$ the clamping ripple, could be around 20 V
Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn-off. The peak voltage at which the leakage forces the drain is calculated by:

$$
\mathrm{V}_{\text {max }}=\mathrm{lp} \cdot \sqrt{\frac{\mathrm{~L}_{\text {leak }}}{\mathrm{C}_{\text {lump }}}}
$$

where $\mathrm{C}_{\text {lump }}$ represents the total parasitic capacitance seen at the MOSFET opening. Typical values for Rsnubber and Csnubber in this 4 W application could respectively be 1.5 $\mathrm{k} \Omega$ and 47 pF . Further tweaking is nevertheless necessary to tune the dissipated power versus standby power.

## Available Documents

"Implementing the NCP1200 in Low-cost AC/DC Converters", AND8023/D
"Conducted EMI Filter Design for the NCP1200", AND8032/D
"Ramp Compensation for the NCP1200", AND8029/D
TRANSient and AC models available to download at: http://onsemi.com/pub/NCP1200
NCP1200 design spreadsheet available to download at: http://onsemi.com/pub/NCP1200

ORDERING INFORMATION

| Device | Type | Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP1200P40 | $\mathrm{F}_{\text {SW }}=40 \mathrm{kHz}$ | 1200 P 40 | PDIP8 | 50 Units / Rail |
| NCP1200D40R2 | $\mathrm{F}_{\mathrm{SW}}=40 \mathrm{kHz}$ | 200 D 4 | SO-8 | 2500 Units /Reel |
| NCP1200P60 | $\mathrm{F}_{\mathrm{SW}}=60 \mathrm{kHz}$ | 1200 P 60 | PDIP8 | 50 Units / Rail |
| NCP1200D60R2 | $\mathrm{F}_{\mathrm{SW}}=60 \mathrm{kHz}$ | 200 D 6 | SO-8 | 2500 Units /Reel |
| NCP1200P100 | $\mathrm{F}_{\mathrm{SW}}=100 \mathrm{kHz}$ | 1200 P 100 | PDIP8 | 50 Units / Rail |
| NCP1200D100R2 | $\mathrm{F}_{\mathrm{SW}}=100 \mathrm{kHz}$ | 200 D 1 | SO-8 | 2500 Units / Reel |

## NCP1203

## Advance Information <br> PWM Current-Mode Controller for Universal Off-Line Supplies Featuring Standby and Short Circuit Protection

Housed in SO-8 or DIP8 package, the NCP1203 represents a major leap toward ultra-compact Switch-Mode Power Supplies and represents an excellent candidate to replace the UC384X devices. Thanks to its proprietary SmartMOS Very High Voltage Technology, the circuit allows the implementation of complete off-line AC/DC adapters, battery charger and a high-power SMPS with few external components.

With an internal structure operating at a fixed $40 \mathrm{kHz}, 60 \mathrm{kHz}$ or 100 kHz switching frequency, the controller features a high-voltage start-up FET which ensures a clean and loss-less start up sequence. Its current-mode control naturally provides good audio-susceptibility and inherent pulse-by-pulse control.

When the current set point falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so-called skip cycle mode and provides improved efficiency at light loads while offering excellent performance in standby conditions. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The NCP1203 also includes an efficient protective circuitry which, in presence of an output over load condition, disables the output pulses while the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto-recovers. Finally, a temperature shutdown with hysteresis helps building safe and robust power supplies.

## Features

- High-Voltage Start Up Current Source
- Auto-Recovery Internal Output Short-Circuit Protection
- Extremely Low No-Load Standby Power
- Current-Mode with Adjustable Skip-Cycle Capability
- Internal Leading Edge Blanking
- 250 mA Peak Current Capability
- Internally Fixed Frequency at $40 \mathrm{kHz}, 61 \mathrm{kHz}$ and 100 kHz
- Direct Optocoupler Connection
- Undervoltage Lockout at 7.6 V Typical
- SPICE Models Available for TRANsient and AC Analysis
- Pin to Pin Compatible with NCP1200


## Applications

- AC/DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

[^22] herein are subject to change without notice.

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONNECTIONS

(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| NCP1203P60 | PDIP8 | 50 Units/Tube |
| NCP1203D60R2 | SO-8 | 2500/Tape \& Reel |
| NCP1203P40 | PDIP8 | 50 Units/Tube |
| NCP1203D40R2 | SO-8 | 2500/Tape \& Reel |
| NCP1203P100* $^{*}$ | PDIP8 | 50 Units/Tube |
| NCP1203D100R2 $^{*}$ | SO-8 | 2500/Tape \& Reel |

* Intro Pending Q1, 2002


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Function | Pin Description |
| :---: | :---: | :---: | :--- |
| 1 | Adj | Adjust the skipping peak current | This pin lets you adjust the level at which the cycle skipping process takes <br> place. Shorting this pin to ground, permanently disables the skip cycle <br> feature. |
| 2 | FB | Sets the peak current setpoint | By connecting an optocoupler to this pin, the peak current setpoint is <br> adjusted accordingly to the output power demand. Skip cycle occurs when <br> FB falls below Vpin1. |
| 3 | CS | Current sense input | This pin senses the primary current and routes it to the internal comparator <br> via an L.E.B. |
| 4 | Gnd | The IC ground | - |
| 5 | Drv | Driving pulses | The driver's output to an external MOSFET. |
| 6 | Vcc | Supplies the IC | This pin is connected to an external bulk capacitor of typically 22 $\mu$ F. |
| 7 | NC | - | This unconnected pin ensures adequate creepage distance. |
| 8 | HV | Ensure a clean and lossless <br> start up sequence | Connected to the high-voltage rail, this pin injects a constant current into <br> the Vcc capacitor during the start up sequence. |



Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | Vcc | 16 | V |
| Thermal Resistance Junction-to-Air, PDIP8 Version Thermal Resistance Junction-to-Air, SOIC Version | $R_{\theta J A}$ <br> $R_{\theta J A}$ | $\begin{aligned} & 100 \\ & 178 \end{aligned}$ | $\begin{aligned} & \hline{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Maximum Junction Temperature | $T J_{\text {MAX }}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Temperature Shutdown (60 kHz) | - | 170 | ${ }^{\circ} \mathrm{C}$ |
| Hysteresis in Shutdown | - | 30 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | - | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Capability, HBM Model (All pins except Vcc and HV) | - | 2.0 | KV |
| ESD Capability, Machine Model | - | 200 | V |
| Maximum Voltage on Pin 8 (HV), Pin 6 (Vcc) Grounded | - | 450 | V |
| Maximum Voltage on Pin 8 (HV), Pin 6 (Vcc) Decoupled to Ground with $10 \mu \mathrm{~F}$ | - | 500 | V |

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{J}}=0^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, $\mathrm{Max}_{\mathrm{J}}=150^{\circ} \mathrm{C}$, $\mathrm{Vcc}=11 \mathrm{~V}$ unless otherwise noted.)

| Characteristic | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

Supply Section (All frequency versions, otherwise noted)

| Turn-on Threshold Level, Vcc Going Up | VCC ${ }_{\text {OFF }}$ | 6 | 12.2 | 12.8 | 14 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage after Turn-on | $\mathrm{VCC}_{(\text {min }}$ | 6 | 7.2 | 7.8 | 8.4 | V |
| Vcc Decreasing Level at which the Latch-off Phase Ends | $\mathrm{VCC}_{\text {latch }}$ | 6 | - | 4.9 | - | V |
| Internal IC Consumption, No Output Load on Pin 6 | ICC1 | 6 | - | 750 | $\begin{gathered} 880 \\ (\text { Note 1) } \end{gathered}$ | $\mu \mathrm{A}$ |
| Internal IC Consumption, 1.0 nF Output Load on Pin 6, $\mathrm{F}_{\mathrm{Sw}}=40 \mathrm{kHz}$ | ICC2 | 6 | - | 1.2 | $\begin{gathered} 1.4 \\ \text { (Note 2) } \end{gathered}$ | mA |
| Internal IC Consumption, 1.0 nF Output Load on Pin 6, $\mathrm{F}_{\mathrm{SW}}=60 \mathrm{kHz}$ | ICC2 | 6 | - | 1.4 | $\begin{gathered} 1.6 \\ \text { (Note 2) } \end{gathered}$ | mA |
| Internal IC Consumption, 1.0 nF Output Load on Pin 6, $\mathrm{F}_{\mathrm{Sw}}=100 \mathrm{kHz}$ | ICC2 | 6 | - | 2.0 | $\begin{gathered} 2.2 \\ \text { (Note 2) } \end{gathered}$ | mA |
| Internal IC Consumption, Latch-off Phase, Vcc $=6.0 \mathrm{~V}$ | ICC3 | 6 | - | 350 | - | $\mu \mathrm{A}$ |

Internal Start Up Current Source (Pin 8 biased at 50 V )

| High-Voltage Current Source, Vcc $=10$ V | IC1 | 8 | 4.5 | 7.0 | 9.0 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| High-Voltage Current Source, Vcc $=0$ | IC2 | 8 | - | 13 | - | mA |

## Drive Output

| Output Voltage Rise-Time @ CL $=1.0 \mathrm{nF}, 10-90 \%$ of <br> Output Signal | $\mathrm{T}_{\mathrm{r}}$ | 5 | - | 67 | - | ns |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage Fall-Time @ CL $=1.0 \mathrm{nF}, 10-90 \%$ of <br> Output Signal | $\mathrm{T}_{\mathrm{f}}$ | 5 | - | 28 | - | ns |
| Source Resistance | $\mathrm{R}_{\mathrm{OH}}$ | 5 | 27 | 40 | 61 | $\Omega$ |
| Sink Resistance | $\mathrm{R}_{\mathrm{OL}}$ | 5 | 5.0 | 12 | 20 | $\Omega$ |

Current Comparator (Pin 5 loaded unless otherwise noted)

| Input Bias Current @ 1.0 V Input Level on Pin 3 | $\mathrm{I}_{\mathrm{IB}}$ | 3 | - | 0.02 | - | $\mu \mathrm{A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum Internal Current Setpoint (Note 3) | $\mathrm{I}_{\text {Limit }}$ | 3 | 0.85 | 0.92 | 1.0 | V |
| Default Internal Current Setpoint for Skip Cycle Operation | $\mathrm{I}_{\text {Lskip }}$ | 3 | - | 360 | - | mV |
| Propagation Delay from Current Detection to Gate OFF <br> State | $\mathrm{T}_{\mathrm{DEL}}$ | 3 | - | 90 | 160 | ns |
| Leading Edge Blanking Duration (Note 3) | $\mathrm{T}_{\text {LEB }}$ | 3 | - | 230 | - | ns |

Internal Oscillator (Vcc = 11 V , pin 5 loaded by 1 nF )

| Oscillation Frequency, 40 kHz Version | fosc | - | 37 | 42 | 47 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillation Frequency, 60 kHz Version | fosc | - | 57 | 65 | 73 | kHz |
| Oscillation Frequency, 100 kHz Version | f Osc | - | 90 | 103 | 115 | kHz |
| Maximum Duty-Cycle | Dmax | - | 74 | 80 | 87 | $\%$ |

Feedback Section (Vcc=11 V, pin 5 unloaded)

| Internal Pull-up Resistor | Rup | 2 | - | 20 | - | $\mathrm{k} \Omega$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin 3 to Current Setpoint Division Ratio | Iratio | - | - | 3.3 | - | - |

## Skip Cycle Generation

| Default Skip Mode Level | Vskip | 1 | 1.0 | 1.2 | 1.4 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin 1 Internal Output Impedance | Zout | 1 | - | 22 | - | $\mathrm{k} \Omega$ |

1. Max value at $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$.
2. Maximum value @ $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, please see characterization curves.
3. Pin 5 loaded by 1 nF .


Figure 3. $\mathrm{V}_{\mathrm{CC}(\mathrm{off})}$ Threshold versus Temperature


Figure 5. $\mathrm{I}_{\mathrm{C}}$ Current Consumption (No Load) versus Temperature


Figure 7. HV Current Source at $\mathrm{V}_{\mathrm{Cc}}=10 \mathrm{~V}$ versus Temperature


Figure 4. $\mathrm{V}_{\mathrm{CC}(\mathrm{min})}$ Level versus Temperature


Figure 6. ICC Consumption (Loaded by 1 nF) versus Temperature


Figure 8. $\mathrm{I}_{\mathrm{C}}$ Consumption at $\mathrm{V}_{\mathrm{CC}}=8 \mathrm{~V}$ versus Temperature


Figure 9. Drive Source Resistance versus Temperature


Figure 11. Maximum Current Setpoint versus Temperature


Figure 10. Drive Sink Resistance versus Temperature

Figure 12. Frequency versus Temperature

## APPLICATION INFORMATION

## Introduction

The NCP1203 implements a standard current mode architecture where the switch-off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part-count is the key parameter, particularly in low-cost AC/DC adapters, auxiliary supplies etc. Thanks to its high-performance SmartMOS High-Voltage technology, the NCP1203 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low-pass filter and start up device. This later point emphasizes the fact that ON Semiconductor's NCP1203 does not need an external start up resistance but supplies the start up current directly from the high-voltage rail. On the other hand, more and more applications are requiring low no-load standby power, e.g. for AC/DC adapters, VCRs etc. UC384X series have a lot of difficulty to reduce the switching losses at low power levels. NCP1203 elegantly solves this problem by
skipping unwanted switching cycles at a user-adjustable power level. By ensuring that skip cycles take place at low peak current, the device ensures quiet, noise free operation. Finally, an auto-recovery output short-circuit protection (OCP) prevents from any lethal thermal runaway in overload conditions.

## Start-Up Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 4.0 mA ) is biased and charges up the Vcc capacitor. When the voltage on this Vcc capacitor reaches the VccOFF level (typically 12.8 V ), the current source turns off and no longer wastes any power. At this time, the Vcc capacitor only supplies the controller and the auxiliary supply is supposed to take over before Vcc collapses below Vcc(min). Figure 13 shows the internal arrangement of this structure:


Figure 13. The Current Source Brings $\mathrm{V}_{\mathrm{Cc}}$ Above 12.8 V and then Turns Off

Once the power supply has started, the Vcc shall be constrained below 16 V , which is the maximum rating on pin 6 . Figure 14 portrays a typical start up sequence with a Vcc regulated at 12.5 V :


Figure 14. A Typical Start Up Sequence for the NCP1203

## Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short-circuit protection. A short-circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the auxiliary voltage also decreases because it also operates in Flyback and thus duplicates the output voltage, providing the leakage inductance between windings is kept low. To account for this situation and properly protect the power supply, NCP1203 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty-cycle. The system auto-recovers when the fault condition disappears.

During the start-up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. The auxiliary voltage takes place after a few switching cycles and self-supplies the IC. In presence of a short circuit on the output, the auxiliary voltage will go down until it crosses the undervoltage
lockout level of typically 7.6 V . When this happens, NCP1203 immediately stops the switching pulses and unbias all unnecessary logical blocks. The overall consumption drops, while keeping the gate grounded, and the Vcc slowly falls down. As soon as Vcc reaches typically 4.6 V, the start up source turns-on again and a new start up
sequence occurs, bringing Vcc toward 12.8 V as an attempt to restart. If the default has gone, then the power supply normally restarts. If not, a new protective burst is initiated, shielding the SMPS from any runaway. Figure 15 portrays the typical operating signals in short circuit:


Figure 15. Typical Waveforms in Short Circuit Conditions

## Calculating the Vcc Capacitor

The Vcc capacitor can be calculated knowing the IC consumption as soon as Vcc reaches 12.8 V . Suppose that a NCP1203P60 is used and drives a MOSFET with a 30 nC total gate charge $(\mathrm{Qg})$. The total average current is thus made of Icc1 $(700 \mu \mathrm{~A})$ plus the driver current, Fsw x Qg or 1.8 mA . The total current is therefore 2.5 mA . The $\Delta \mathrm{V}$ available to fully start up the circuit (e.g. never reach the 7.6 V UVLO during power on) is $12.8-7.6=5.2 \mathrm{~V}$. We have a capacitor who then needs to supply the NCP1203 with 2.5 mA during a given time until the auxiliary supply takes over. Suppose that this time was measured at around 15 ms .

CVcc is calculated using the equation

$$
C=\frac{\Delta t \cdot i}{\Delta V \text { or }}
$$ $C \geq 7.2 \mu \mathrm{~F}$. Select a $10 \mu \mathrm{~F} / 16 \mathrm{~V}$ and this will fit.

## Skipping Cycle Mode

The NCP1203 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level (Vpin 1), the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so-called skip cycle mode, also named controlled burst operation. The power transfer now
depends upon the width of the pulse bunches (Figure 17). Suppose we have the following component values:
Lp, primary inductance $=350 \mu \mathrm{H}$
Fsw, switching frequency $=61 \mathrm{kHz}$
Ip skip $=600 \mathrm{~mA}$ (or $333 \mathrm{mV} /$ Rsense)
The theoretical power transfer is therefore:

$$
\frac{1}{2} \cdot \mathrm{Lp} \cdot \mathrm{lp} 2 \cdot \mathrm{Fsw}=3.8 \mathrm{~W}
$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms , then the total power transfer is: 3.8. $0.1=380 \mathrm{~mW}$.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:


Figure 16.

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed $1.0 \mathrm{~V} /$ Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1/3.3. The user still has the flexibility
to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. Grounding pin 1 permanently invalidates the skip cycle operation.


Figure 17. Output Pulses at Various Power Levels (X=5.0 $\mu \mathrm{s} / \mathrm{div}$ ) P1 < P2 < P3


Figure 18. The Skip Cycle Takes Place at Low Peak Currents which Guaranties Noise-Free Operation

We recommend a pin1 operation between 400 mV and 1.3 V that will fix the skip peak current level between $120 \mathrm{mV} /$ Rsense and $390 \mathrm{mV} /$ Rsense.

## Non-Latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has
disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj pin 1 level, the output pulses are disabled as long as FB is pulled below pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 9 depicts the application example:


Figure 19. Another Way of Shutting Down the IC without a Definitive Latch-Off State

## Full Latching Shutdown

Other applications require a full latching shutdown, e.g. when an abnormal situation is detected (over temp or overvoltage). This feature can easily be implemented through two external transistors wired as a discrete SCR.

When the Vcc level exceeds the zener breakdown voltage, the NPN biases the PNP and fires the equivalent SCR, permanently bringing down the FB pin. The switching pulses are disabled until the user unplugs the power supply.


Figure 20. Two Bipolars Ensure a Total Latch-Off of the SMPS in Presence of an OVP

Rhold ensures that the SCR stays on when fired. The bias current flowing through Rhold should be small enough to let the Vcc ramp up ( 12.8 V ) and down $(4.6 \mathrm{~V})$ when the SCR is fired. The NPN base can also receive a signal from a
temperature sensor. Typical bipolars can be MMBT2222 and MMBT2907 for the discrete latch. The MMBT3946 features two bipolars NPN+PNP in the same package and could also be used.

## MC33364

## Critical Conduction GreenLine ${ }^{\text {TM }}$ SMPS Controller

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Integration of the high voltage startup saves approximately 0.7 W of power compared to the value of the resistor bootstrapped circuits.

Each MC33364 features an on-board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, a CMOS driver and cycle-by-cycle current limiting.

The MC33364D1 has an internal 126 kHz frequency clamp. The MC33364D2 is available without an internal frequency clamp. The MC33364D has an internal 126 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance.

- Lossless Off-Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Operating Temperature Range $-25^{\circ}$ to $+125^{\circ} \mathrm{C}$
- Shutdown Capability
- Over Temperature Protection
- Optional/Adjustable Frequency Clamp to Limit EMI



## MC33364



This device contains 335 active transistors.

Figure 1. Representative Block Diagram


PIN DESCRIPTION

| Pin | Function | Description |
| :---: | :---: | :---: |
| 1 (1) | Zero Current Detect | The ZCD Pin ensures critical conduction mode. ZCD monitors the voltage on the auxiliary winding, during the demagnetization phase of the transformer, comparing it to an internal reference. The ZCD sets the latch for the output driver. |
| 3 (2) | Current Sense | The Current Sense Pin monitors the current in the power switch by measuring the voltage across a resistor. Leading Edge Blanking is utilized to prevent false triggering. The voltage is compared to a resistor divider connected to the Voltage Feedback Pin. A 110 mV voltage off-set is applied to compensate the natural optocoupler saturation voltage. |
| 4 (3) | Voltage Feedback | The Voltage Feedback Pin is typically connected to the collector of the optocoupler for feedback from the isolated secondary output. The Feedback is connected to the $\mathrm{V}_{\text {ref }}$ Pin via a 5 k resistor providing bias for the external optocoupler. |
| 6 (4) | $\mathrm{V}_{\text {ref }}$ | The $\mathrm{V}_{\text {ref }}$ Pin is a buffered internal 5.0 V reference with Undervoltage Lockout. |
| 8 (NA) | Frequency Clamp | The Frequency Clamp Pin ensures a minimum off-time value, typically 6.9 us. It prevents the MOSFET from restarting within a fixed (33364D1) or adjustable (33364D) delay. The minimum off-time is disabled in the 33364D2. Therefore the maximum switching frequency cannot exceed $1 /\left(T_{O N}+T_{\text {OFFmin }}\right)$. |
| 9 (5) | A GND | This pin is the ground for the internal circuitry excluding the gate drive stage. |
| 10 (5) | P GND | This pin is the ground for the gate drive stage. |
| 11 (6) | Gate Drive | The gate drive is the output to drive the gate of the power MOSFET. |
| 12 (7) | $\mathrm{V}_{\mathrm{CC}}$ | Provides the voltage for all internal circuitry including the gate drive stage and $\mathrm{V}_{\text {ref }}$. This pin has Undervoltage Lockout with hysteresis. |
| 16 (8) | Line | The Line Pin provides the initial power to the $\mathrm{V}_{\mathrm{CC}}$ pins. Internally the line pin is a high voltage current source, eliminating the need for an external startup network. |

For further information please refer to the following Application Notes;
AN1594: Critical Conduction Mode, Flyback Switching

Power Supply Using the MC33364.
AN1681: How to keep a Flyback Switch-Mode Power Supply Stable with a Critical-Mode Controller.

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage (Operating) | $\mathrm{V}_{\mathrm{CC}}$ | 16 | V |
| Line Voltage | $\mathrm{V}_{\text {Line }}$ | 700 | V |
| Current Sense, Compensation, <br> Voltage Feedback, Restart Delay and Zero Current Input Voltage | $\mathrm{V}_{\text {in } 1}$ | -1.0 to +10 | V |
| Zero Current Detect Input | $\mathrm{I}_{\text {in }}$ | $\pm 5.0$ | mA |
| Restart Diode Current | $\mathrm{I}_{\text {in }}$ | 5.0 | mA |
| Power Dissipation and Thermal Characteristics <br> D1 and D2 Suffix, Plastic Package Case 751 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> $\mathrm{D} \mathrm{Suffix} \mathrm{Plastic} \mathrm{Package} \mathrm{Case} 751 \mathrm{~B}-05$, <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $\mathrm{P}_{\mathrm{D}}$ |  |  |
| Operating Junction Temperature | $\mathrm{R}_{\theta \mathrm{JA}}$ | 450 | mW |
| Operating Ambient Temperature | $\mathrm{P}_{\mathrm{D}}$ | 178 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | $\mathrm{R}_{\theta \mathrm{JJA}}$ | 550 | mW |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{J}}=-25$ to $125^{\circ} \mathrm{C}$ )

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VOLTAGE REFERENCE |  |  |  |  |  |
| Reference Output Voltage ( $\mathrm{l}_{\text {Out }}=0 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {ref }}$ | 4.90 | 5.05 | 5.20 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 20 V ) | Regline | - | 2.0 | 50 | mV |
| Load Regulation ( $\mathrm{l}_{\text {Out }}=0 \mathrm{~mA}$ to 5.0 mA ) | Regload | - | 0.3 | 50 | mV |
| Maximum $\mathrm{V}_{\text {ref }}$ Output Current | 10 | - | 5 | - | mA |
| Reference Undervoltage Lockout Threshold | $\mathrm{V}_{\text {th }}$ | - | 4.5 | - | V |
| ZERO CURRENT DETECTOR |  |  |  |  |  |
| Input Threshold Voltage ( $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {th }}$ | 0.9 | 1.0 | 1.1 | V |
| Hysteresis ( $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\mathrm{H}}$ | - | 200 | - | mV |
| Input Clamp Voltage <br> High State ( $\mathrm{I}_{\mathrm{DET}}=3.0 \mathrm{~mA}$ ) <br> Low State ( $\mathrm{I}_{\mathrm{DET}}=-3.0 \mathrm{~mA}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | $\begin{gathered} 9.0 \\ -1.1 \end{gathered}$ | $\begin{array}{r} 10.33 \\ -0.75 \\ \hline \end{array}$ | $\begin{array}{r} 12 \\ 0.5 \end{array}$ | V |

CURRENT SENSE COMPARATOR

| Input Bias Current $\left(\mathrm{V}_{\mathrm{CS}}=0\right.$ to 2.0 V ) | $\mathrm{I}_{\mathrm{IB}}$ | -0.5 | 0.02 | 0.5 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Built In Offset | $\mathrm{V}_{\mathrm{IO}}$ | 50 | 108 | 170 | mV |
| Feedback Pin Input Range | $\mathrm{V}_{\mathrm{FB}}$ | 1.1 | 1.24 | 1.4 | V |
| Feedback Pin to Output Delay | $\mathrm{t}_{\mathrm{DLY}}$ | 100 | 232 | 400 | ns |

DRIVE OUTPUT

| Source Resistance (Drive $=0 \mathrm{~V}$, $\mathrm{V}_{\text {Gate }}=\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}$ ) <br> Sink Resistance (Drive $=\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\text {Gate }}=1.0 \mathrm{~V}$ ) | $\mathrm{R}_{\mathrm{OH}}$ $\mathrm{R}_{\mathrm{OL}}$ | $\begin{gathered} 10 \\ 5 \end{gathered}$ | $\begin{aligned} & 36 \\ & 11 \end{aligned}$ | $\begin{aligned} & 70 \\ & 25 \end{aligned}$ | $\Omega$ $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage Rise Time ( $25 \%-75 \%$ ) ( $\left.\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ | $\mathrm{t}_{\mathrm{r}}$ | - | 67 | 150 | ns |
| Output Voltage Fall Time ( $75 \%-25 \%$ ) ( $\left.\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ | $\mathrm{t}_{\mathrm{f}}$ | - | 28 | 50 | ns |
| Output Voltage in Undervoltage ( $\left.\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}, \mathrm{I}_{\text {Sink }}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{O}(\mathrm{UV})}$ | - | 0.01 | 0.03 | V |
| LEADING EDGE BLANKING |  |  |  |  |  |
| Delay to Current Sense Comparator Input $\left(\mathrm{V}_{\mathrm{FB}}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CS}}=0 \mathrm{~V} \text { to } 4.0 \mathrm{~V} \text { step, } \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ | $\mathrm{t}_{\text {PHL }}$ (in/out) | - | 250 |  | ns |
| TIMER |  |  |  |  |  |
| Watchdog Timer | $t_{\text {DLY }}$ | 200 | 360 | 700 | $\mu \mathrm{s}$ |
| UNDERVOLTAGE LOCKOUT |  |  |  |  |  |
| Startup Threshold (VCC Increasing) | $\mathrm{V}_{\text {th(on) }}$ | 14 | 15 | 16 | V |
| Minimum Operating Voltage After Turn-On (V) $\mathrm{V}_{\mathrm{CC}}$ Decreasing) | $\mathrm{V}_{\text {Shutdown }}$ | 6.5 | 7.6 | 8.5 | V |

FREQUENCY CLAMP

| Internal FC Function (pin open) | $\mathrm{f}_{\max }$ | 104 | 126 | 145 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Internal FC Function (pin grounded) | $\mathrm{f}_{\max }$ | 400 | 564 | 800 | kHz |
| Frequency Clamp Input Threshold | $\mathrm{V}_{\mathrm{th}(\mathrm{FC})}$ | 1.89 | 1.95 | 2.01 | V |
| Frequency Clamp Control Current Range (Sink) | $\mathrm{I}_{\text {Control }}$ | 30 | 70 | 110 | $\mu \mathrm{~A}$ |
| Dead Time (FC pin $=1.7 \mathrm{~V}$ ) | $\mathrm{T}_{\mathrm{d}}$ | 3.5 | 5.0 | 6.5 | $\mu \mathrm{~s}$ |

TOTAL DEVICE

| Line Startup Current $\left(\mathrm{V}_{\text {Line }}=50 \mathrm{~V}\right)\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{th}(o n)}-1.0 \mathrm{~V}\right)$ Restart Delay Time | Line <br> $t_{D L Y}$ | 5.0 | $\begin{aligned} & 8.5 \\ & 100 \end{aligned}$ | 12 | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~ms} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Pin Leakage ( $\mathrm{V}_{\text {Line }}=500 \mathrm{~V}$ ) | Line | 0.5 | 32 | 70 | $\mu \mathrm{A}$ |
| Line Startup Current ( $\mathrm{V}_{\text {CC }}=0 \mathrm{~V}, \mathrm{~V}_{\text {Line }}=50 \mathrm{~V}$ ) | 1 Line | 6.0 | 10 | 12 | mA |
| $\mathrm{V}_{\mathrm{CC}}$ Dynamic Operating Current ( $50 \mathrm{kHz}, \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ ) | ICC | 1.5 | 2.75 | 4.5 | mA |
| $\mathrm{V}_{\mathrm{CC}}$ Off State Consumption ( $\mathrm{V}_{\mathrm{CC}}=11 \mathrm{~V}$ ) | ICC Off | 300 | 544 | 800 | $\mu \mathrm{A}$ |



Figure 2. Drive Output Waveform


Figure 4. Supply Current versus Supply Voltage


Figure 6. Dead Time versus Frequency Clamp Source / Sink Current


Figure 3. Watchdog Timer Delay versus Temperature


Figure 5. Transient Thermal Resistance


Figure 7. Feedback Voltage versus Current Sense Voltage

## FUNCTIONAL DESCRIPTION

## INTRODUCTION

With the goal of reducing the size and cost of off-line power supplies, there is an ever increasing demand for an economical method of obtaining a regulated galvanically isolated dc output voltage using a control which operates
directly from the ac line. This data sheet describes a monolithic control IC that was specifically designed for power supply control with a minimal number of external components. It offers the designer a simple cost effective solution to obtain the benefits of off-line power regulation.


Figure 8. Functional Block Diagram

## Operating Description

The MC33364 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 8, note that this device does not contain an oscillator. A description of each of the functional blocks is given below.

## Zero Current Detector

The MC33364 operates as a critical conduction current mode controller, whereby the output switch conduction is initiated by the Zero Current Detector pin and terminated when the peak inductor current reaches the programmed threshold level. The ZCD pin indirectly monitors the inductor current by sensing the auxiliary winding voltage. When the voltage falls below the set threshold, 1.0 volt, the comparator resets the latch to turn on the MOSFET. There is 200 mV of hysteresis built into the comparator for noise immunity and to prevent false tripping

The ZCD pin is internally protected by a 10 volt and -0.7 volt clamp. An external resistor is necessary to limit the input current to 2 mA to protect the clamp.

Since the MC33364 implements the ZCD pin, the SMPS circuit has the following benefits:

1. A less expensive rectifier can be used on the output windings because of the zero current switching which naturally softens the diode turn-off.
2. The second benefit is the peak drain current which is limited to twice the average input current. By combining the ZCD series resistor with the pin capacitance, a drain-source valley switching can be implemented, further reducing the turn-on losses and the EMI disturbances.
3. By preventing the SMPS from entering the Continuous Conduction Mode (CCM), the MC33364 forces the system to stay a first-order device (in the lower frequency range) in any operating condition (output short, start-up, low mains). The feedback compensation network is thus considerably simplified.

## Current Sense and Feedback Inputs

The Current Sense pin and the Feedback pin are linked internally in the device via the current sense comparator. The output of the comparator is connected to the Set of the RS Latch, which turns the external MOSFET off.

The current sense operates by using a resistor, connected between the source of the MOSFET and ground, to convert the current through the inductor to a voltage. Leading Edge Blanking is implemented to prevent false triggering due to parasitics. The current sense voltage is level shifted up by 0.1 volt into the non-inverting input of the comparator. This offset accounts for the optocoupler VCEsat and allows the duty-cycle to be zero.

The maximum peak switch current is 1.15 V (the maximum voltage at the inverting input, 1.25 volts, minus 0.1 volt, the level shift) divided by the external current sense
resistance. The Current Sense Input to Drive Output propagation delay is 232 nsec typically.

The Feedback pin is internally pulled up with a 5 kOhm resistor from the 5.0 volt Vref pin. The Feedback pin uses a resistor divider to proportionally adjust the voltage into the inverting input of the comparator. The inverting input also has a 1.25 volt clamp. Typically the Feedback pin is connected to the collector of the optocoupler.

## Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 410 microseconds after the inductor current reaches zero. This time-out thus ensures the IC will restart when the demagnetization signal is lower than the internal ZCD 1V threshold or has simply been lost.

## Undervoltage Lockout

The MC33364 has a hysteretic UVLO associated with the $\mathrm{V}_{\mathrm{CC}}$ pin. During startup, $\mathrm{V}_{\mathrm{CC}}$ must rise to 15 volts to turn off the startup circuit associated with the Line pin and to enable the output drivers. The voltage at $\mathrm{V}_{\mathrm{CC}}$ must remain above 7.6 volts for the part to remain operational.

## Internal Reference

The MC33364 has an internal buffered 5.0 volt reference. The reference requires a $0.1 \mu \mathrm{~F}$ bypass capacitor for noise immunity. The reference is capable of sourcing 10 mA typically. The reference contains an independant UVLO which will disable the output drive circuitry.

## Startup Circuit and Restart Delay

A high voltage Startup Circuit is contained within the MC33364 eliminating the need for external components. The internal startup circuit operates as a constant current source to charge up the bypass capacitor on the $\mathrm{V}_{\mathrm{CC}}$ pin. The Startup Circuitry is controlled by the Restart Delay circuitry. The threshold levels of the turn on and turn off are below 4.5 volts and above 15 volts, respectively, as measured on the $\mathrm{V}_{\mathrm{CC}}$ pin.

A restart delay function is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. During a short circuit, the restart delay prevents excessive power dissipation in the primary side of the SMPS and allows time for the output to reset the fault condition. The restart delay time is approximately 100 msec .

## Output Switching Frequency Clamp

In normal operation, the MC33364 operates the flyback transformer in the critical conduction mode. The CCM is defined by the transformer ramping to a peak current value, ramping down to zero, then immediately ramping positive again. The peak current is programmed by the current sense resistor and is compared with a divided down voltage from
the feedback pin. When the output is reduced from full load to standby or no load, the switching frequency can increase dramatically to hundreds of kilohertz. Due to EMI regulations above 150 kHz , the Frequency Clamp on the MC33364D and MC33364D1 will limit the upper frequency by inserting a minimum off time.

The frequency of a switching regulator is determined by $\mathrm{f}=1 /\left(\mathrm{T}_{\text {on }}+\mathrm{T}_{\text {off }}\right)$. During light load and no load conditions, $\mathrm{T}_{\text {off }}$ is the reset time of the transformer plus dead time. At no load conditions, $\mathrm{T}_{\text {on }}$ is approximately the LEB and $\mathrm{T}_{\text {off }}$ is the programmed minimum off-time. With the addition of logic delay times, the maximum frequency when the FC pin floats is 126 kHz nominally.

The Frequency Clamp inserts a minimum off-time immediately after the driving signal goes low. If the ZCD signal comes within this minimum off-time, the information is ignored until the minimum off-time expires. By forcing the minimum off-time, the transformer will operate in the Discontinuous Mode. The next coming ZCD signal starts the latch. The MC33364 is available in three versions:

MC33364D1: the internal minimum off-time is fixed at $6.9 \mu \mathrm{sec}$ typically
MC33364D2: there is no internal minimum off-time
MC33364D: the internal minimum off-time can be either lengthened, shortened or eliminated by biasing the appropriate pin The FC pin contains a 4.0 kOhm series resistor into the non-inverting input of a comparator. The non-inverting input has a 10 volt clamp to limit overvoltage. Refer to Figure 9 for a detailed circuit of the Frequency Clamp.


NOTE: For proper operation, use either $\mathrm{R}_{\mathrm{Vcc}}$ or $\mathrm{R}_{\mathrm{gnd}}$ or let the pin float.
Figure 9. Simplified Frequency Clamp Circuit

The MC33364D has a Frequency Clamp pin which can vary the maximum frequency. If the FC pin floats, the minimum off-time is fixed at $6.9 \mu \mathrm{sec}$ typically. If the FC pin is grounded, the clamp is disabled. Sinking or sourcing a current up to $100 \mu \mathrm{~A}$ into the FC pin will vary the maximum frequency (see Figure 6). However, we do not recommend exceeding $80 \mu \mathrm{~A}$ because the high dDT/dIFC would not ensure a stable operation.

## Output

The IC contains a CMOS output driver specifically designed for direct drive of power MOSFETs. The Drive Output typical rise and fall time is 50 nS with a 1.0 nF load. Unbalanced Source and Sink capability eliminates the need for an external resistor between the IC Drive output and the Gate of the external MOSFET. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the UVLO is active. This characteristic eliminates the need for an external gate pull-down resistor.

## APPLICATION INFORMATION

## Design Example

Design an off-line Flyback converter according to the following requirements:

Output Power: $\quad 12 \mathrm{~W}$
Output: $\quad 6.0$ V @ 2 Amperes
Input voltage range: $90 \mathrm{Vac}-270 \mathrm{Vac}, 50 / 60 \mathrm{~Hz}$
The operation for the circuit shown in Figure 8 is as follows: the rectifier bridge D1-D4 and the capacitor C1 convert the ac line voltage to dc. This voltage supplies the primary winding of the transformer T1 and the startup circuit in U1 through the line pin. The primary current loop is closed by the transformer's primary winding, the TMOS switch Q1 and the current sense resistor R7. The resistors R5, R6, diode D6 and capacitor C4 create a snubber clamping network that protects Q1 from spikes on the primary winding. The network consisting of capacitor C3, diode D5 and resistor R1 provides a $\mathrm{V}_{\mathrm{CC}}$ supply voltage for U1 from the auxiliary winding of the transformer. The resistor R1 makes $\mathrm{V}_{\mathrm{CC}}$ more stable and resistant to noise. The resistor R2 reduces the current flow through the internal clamping and protection zener diode of the Zero Crossing Detector (ZCD) within U1. C3 is the decoupling capacitor of the supply voltage. The resistor R3 can provide additional bias current for the optoisolator's transistor. The diode D8 and the capacitor C5 rectify and filter the output voltage. The TL431, a programmable voltage reference, drives the primary side of the optoisolator to provide isolated feedback to the MC33364. The resistor divider consisting of R10 and R11 program the voltage of the TL431. The resistor R9 and the capacitors C7 and C8 provide frequency compensation of the feedback loop. Resistor R8 provides a current limit for the opto coupler and the TL431.

Since the critical conduction mode converter is a variable frequency system, the MC33364 has a built-in special block to reduce switching frequency in the no load condition. This block is named the "frequency clamp" block. MC33364 used in the design example has an internal frequency clamp set to 126 kHz . However, optional versions with a disabled or variable frequency clamp are available. The frequency clamp works as follows: the clamp controls the part of the switching cycle when the MOSFET switch is turned off. If this "off-time" (determined by the reset time of the transformer's core) is too short, then the frequency clamp does not allow the switch to turn-on again until the defined frequency clamp time is reached (i.e., the frequency clamp will insert a dead time).

There are several advantages of the MC33364's startup circuit. The startup circuit includes a special high voltage switch that controls the path between the rectified line voltage and the $\mathrm{V}_{\mathrm{CC}}$ supply capacitor to charge that capacitor by a limited current when the power is applied to the input. After a few switching cycles the IC is supplied from the transformer's auxiliary winding. After $\mathrm{V}_{\mathrm{CC}}$ reaches the undervoltage lockout threshold value, the startup switch is turned off by the undervoltage and the
overvoltage control circuit. Because the power supply can be shorted on the output, causing the auxiliary voltage to be zero, the MC33364 will periodically start its startup block. This mode is named "hiccup mode". During this mode the temperature of the chip rises but remains protected by the thermal shutdown block. During the power supply's normal operation, the high voltage internal MOSFET is turned off, preventing wasted power, and thereby, allowing greater circuit efficiency.
Since a bridge rectifier is used, the resulting minimum and maximum dc input voltages can be calculated:

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{in}(\min )} \mathrm{dc}=\sqrt{2} x \mathrm{~V}_{\text {in(min) }} \mathrm{ac}=(\sqrt{2})(90 \mathrm{Vac})=127 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{in}(\mu \mathrm{ax})} \mathrm{dc}=\sqrt{2} \mathrm{x} \mathrm{~V}_{\mathrm{in}(\mu \mathrm{ax})} \mathrm{ac}=(\sqrt{2})(270 \mathrm{Vac})=382 \mathrm{~V}
\end{aligned}
$$

The maximum average input current is:
$\mathrm{I}_{\text {in }}=\frac{\mathrm{P}_{\text {out }}}{\mathrm{nV} \mathrm{V}_{\text {in }(\min )}}=\frac{12 \mathrm{~W}}{0.8(127 \mathrm{~V})}=0.118 \mathrm{~A}$
where $\mathrm{n}=$ estimated circuit efficiency.
A TMOS switch with 600 V avalanche breakdown voltage is used. The voltage on the switch's drain consists of the input voltage and the flyback voltage of the transformer's primary winding. There is a ringing on the rising edge's top of the flyback voltage due to the leakage inductance of the transformer. This ringing is clamped by the RCD network. Design this clamped wave for an amplitude of 50 V below the avalanche breakdown of the TMOS device. Add another 50 V to allow a safety margin for the MOSFET. Then a suitable value of the flyback voltage may be calculated:

$$
\begin{gathered}
\mathrm{V}_{\mathrm{flbk}}=\mathrm{V}_{\text {TMOS }}-\mathrm{V}_{\text {in }(\max )}-100 \mathrm{~V}= \\
600 \mathrm{~V}-382 \mathrm{~V}-100 \mathrm{~V}=118 \mathrm{~V}
\end{gathered}
$$

Since this value is very close to the $\mathrm{V}_{\mathrm{in}(\mathrm{min})}$, set:
$\mathrm{V}_{\mathrm{flbk}}=\mathrm{V}_{\mathrm{in}(\min )}=127 \mathrm{~V}$
The $\mathrm{V}_{\text {flbk }}$ value of the duty cycle is given by:
$\partial \max =\frac{\mathrm{V}_{\mathrm{flbk}}}{\mathrm{V}_{\mathrm{flbk}}+\mathrm{V}_{\mathrm{in}(\min )}}=\frac{127 \mathrm{~V}}{[127 \mathrm{~V}+127 \mathrm{~V}]}=0.5$

The maximum input primary peak current:
$I_{p p k}=\frac{2 I_{\text {in }}}{\partial \max }=\frac{2.0(0.118 \mathrm{~A})}{0.5}=0.472 \mathrm{~A}$
Choose the desired minimum frequency $f_{\text {min }}$ of operation to be 70 kHz .
After reviewing the core sizing information provided by a core manufacturer, a EE core of size about 20 mm was chosen. Siemens' N67 magnetic material is used, which corresponds to a Philips 3C85 or TDK PC40 material.

The primary inductance value is given by:
$\mathrm{L}_{\mathrm{p}}=\frac{\partial \max \mathrm{V}_{\mathrm{in}(\mathrm{min})}}{\left(\mathrm{I}_{\mathrm{ppk}}\right)\left(\mathrm{f}_{\mathrm{min}}\right)}=\frac{0.5(127 \mathrm{~V})}{(0.472 \mathrm{~A})(70 \mathrm{kHz})}=1.92 \mathrm{mH}$
The manufacturer recommends for that magnetic core a maximum operating flux density of:
$\mathrm{B}_{\text {max }}=0.2 \mathrm{~T}$
The cross-sectional area $A_{c}$ of the EF20 core is:
$\mathrm{A}_{\mathrm{C}}=33.5 \mathrm{~mm}^{2}$
The operating flux density is given by:
$B_{\text {max }}=\frac{L_{p} I_{p p k}}{N_{p} A_{c}}$
From this equation the number of turns of the primary winding can be derived:
$n_{p}=\frac{L_{p} I_{p p k}}{B_{\max } A_{c}}$
The $A_{L}$ factor is determined by:

$$
\begin{aligned}
A_{L}=\frac{L_{p}}{n^{2} p}= & \frac{L_{p}\left(B_{\max } A_{c}\right)^{2}}{\left[L_{p}\left(I_{p p k}\right)^{2}\right]} \\
& =\frac{(0.2 \mathrm{~T})\left(33.5 \mathrm{E}-6 \mathrm{~m}^{2}\right)^{2}}{(.00192 \mathrm{H})(0.472 \mathrm{~A})^{2}}=105 \mathrm{nH}
\end{aligned}
$$

From the manufacturer's catalogue recommendation the core with an $\mathrm{A}_{\mathrm{L}}$ of 100 nH is selected. The desired number of turns of the primary winding is:
$n_{p}=\left(\frac{L_{p}}{A_{L}}\right)^{1 / 2}=\left[\frac{(0.00192 H)}{(100 n H)}\right]^{1 / 2}=139$ turns
The number of turns needed by the 6.0 V secondary is (assuming a Schottky rectifier is used):

$$
\begin{aligned}
&\left.\left.\mathrm{n}_{\mathrm{S}}=\frac{\left(\mathrm{V}_{\mathrm{S}}+\mathrm{V}_{\mathrm{fwd}}\right)(1-\partial \max ) \mathrm{n}_{\mathrm{p}}}{[\partial \max ( } \mathrm{V}_{\text {in }(\min )}\right)\right] \\
&=\frac{(6.0 \mathrm{~V}+0.3 \mathrm{~V})(1-0.5) 139}{[0.5(127 \mathrm{~V})]}=7 \text { turns }
\end{aligned}
$$

The auxiliary winding to power the control IC is 16 V and its number of turns is given by:

$$
\begin{aligned}
& \operatorname{naux}= \frac{\left(\mathrm{V}_{\mathrm{aux}}+\mathrm{V}_{\mathrm{fwd}}\right)(1-\partial \max ) \mathrm{n}_{\mathrm{p}}}{} \\
& {\left[\partial \max \left(\mathrm{~V}_{\mathrm{in}(\min )}\right)\right] } \\
&=\frac{(16 \mathrm{~V}+0.9 \mathrm{~V})(1-0.5) 139}{[0.5(127 \mathrm{~V})]}=19 \text { turns }
\end{aligned}
$$

The approximate value of rectifier capacitance needed is:
$\mathrm{C} 1=\frac{\mathrm{t}_{\text {off }}\left(\mathrm{I}_{\text {in }}\right)}{\mathrm{V}_{\text {ripple }}}=\frac{(5 \mathrm{~m} \mathrm{sec})(0.118 \mathrm{~A})}{50 \mathrm{~V}}=11.8 \mu \mathrm{~F}$
where the minimum ripple frequency is 2 times the 50 Hz line frequency and $\mathrm{t}_{\mathrm{off}}$, the discharge time of C 1 during the haversine cycle, is assumed to be half the cycle period.
Because we have a variable frequency system, all the calculations for the value of the output filter capacitors will be done at the lowest frequency, since the ripple voltage will be greatest at this frequency. When selecting the output capacitor select a capacitor with low ESR to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$
\mathrm{C} 5=\frac{\mathrm{I}_{\text {out }}}{\left({ }_{\text {min }}\right)\left(\mathrm{V}_{\text {rip }}\right)}=\frac{2 \mathrm{~A}}{(70 \mathrm{kHz})(0.1 \mathrm{~V})}=286 \mu \mathrm{~F}
$$

Determining the value of the current sense resistor (R7), one uses the peak current in the predesign consideration. Since within the IC there is a limitation of the voltage for the current sensing, which is set to 1.2 V , the design of the current sense resistor is simply given by:
$\mathrm{R} 7=\frac{\mathrm{V}_{\mathrm{CS}}}{\mathrm{I}_{\mathrm{ppk}}}=\frac{1.2 \mathrm{~V}}{0.472 \mathrm{~A}}=2.54 \Omega \approx 2.2 \Omega$
The error amplifier function is provided by a TL431 on the secondary, connected to the primary side via an optoisolator, the MOC8102.

The voltage of the optoisolator collector node sets the peak current flowing through the power switch during each cycle. This pin will be connected to the feedback pin of the MC33364, which will directly set the peak current.

Starting on the secondary side of the power supply, assign the sense current through the voltage-sensing resistor divider to be approximately 0.25 mA . One can immediately calculate the value of the lower and upper resistor:

$$
\begin{aligned}
& R_{\text {lower }}=R 11=\frac{V_{\text {ref }}(\mathrm{TL431)}}{\mathrm{I}_{\text {div }}}=\frac{2.5 \mathrm{~V}}{0.25 \mathrm{~mA}}=10 \mathrm{k} \\
& R_{\text {upper }}=\mathrm{R} 10=\frac{\mathrm{V}_{\text {out }}-\mathrm{V}_{\text {ref }}(\mathrm{TL431)}}{\mathrm{I}_{\mathrm{div}}} \\
& \quad=\frac{6.0 \mathrm{~V}-2.5 \mathrm{~V}}{0.25 \mathrm{~mA}}=14 \mathrm{k}
\end{aligned}
$$

The value of the resistor that would provide the bias current through the optoisolator and the TL431 is set by the minimum operating current requirements of the TL431. This current is minimum 1.0 mA . Assign the maximum current through the branch to be 5 mA . That makes the bias resistor value equal to:

$$
\begin{aligned}
R_{\text {bias }}=R_{S} & =\frac{\mathrm{V}_{\text {out }}-\left[\mathrm{V}_{\text {ref }}(\mathrm{TL431})+\mathrm{V}_{\mathrm{LED}}\right]}{\mathrm{I}_{\mathrm{LED}}} \\
& =\frac{6.0 \mathrm{~V}-[2.5 \mathrm{~V}+1.4 \mathrm{~V}]}{5.0 \mathrm{~mA}}=420 \Omega \approx 430 \Omega
\end{aligned}
$$

The MOC8102 has a typical current transfer ratio (CTR) of $100 \%$ with $25 \%$ tolerance. When the TL431 is full-on, 5 mA will be drawn from the transistor within the MOC8102. The transistor should be in saturated state at that time, so its collector resistor must be

$$
R_{\text {collector }}=\frac{V_{\text {ref }}-V_{\text {sat }}}{I_{\text {LED }}}=\frac{5.0 \mathrm{~V}-0.3 \mathrm{~V}}{5.0 \mathrm{~mA}}=940 \Omega
$$

Since a resistor of 5.0 k is internally connected from the reference voltage to the feedback pin of the MC33364, the external resistor can have a higher value

$$
\begin{aligned}
R_{\text {ext }}=R 3=\frac{\left(R_{\text {int }}\right)\left(R_{\text {collector }}\right)}{\left(R_{\text {int }}\right)-\left(R_{\text {collector }}\right)} & =\frac{(5.0 k)(940)}{5.0 k-940} \\
= & 1157 \Omega \approx 1200 \Omega
\end{aligned}
$$

This completes the design of the voltage feedback circuit.
In no load condition there is only a current flowing through the optoisolator diode and the voltage sense divider on the secondary side.

The load at that condition is given by:

$$
\begin{aligned}
R_{\text {noload }}= & \frac{V_{\text {out }}}{\left(I_{\text {LED }}+I_{\text {div }}\right)} \\
& =\frac{6.0 \mathrm{~V}}{(5.0 \mathrm{~mA}+0.25 \mathrm{~mA})}=1143 \Omega
\end{aligned}
$$

The output filter pole at no load is:

$$
\begin{aligned}
& \mathrm{f}_{\mathrm{pn}}=\frac{1}{\left(2 \pi \mathrm{R}_{\text {noload }} \mathrm{C}_{\text {out }}\right)} \\
& \quad=\frac{1}{(2 \pi)(1143)(300 \mu \mathrm{~F})}=0.46 \mathrm{~Hz}
\end{aligned}
$$

In heavy load condition the $\mathrm{I}_{\text {LED }}$ and $\mathrm{I}_{\text {div }}$ is negligible. The heavy load resistance is given by:

$$
R_{\text {heavy }}=\frac{V_{\text {out }}}{I_{\text {out }}}=\frac{6.0 \mathrm{~V}}{2.0 \mathrm{~A}}=3.0 \Omega
$$

The output filter pole at heavy load of this output is
$f_{p n}=\frac{1}{\left(2 \pi R_{\text {heavy }} C_{o u t}\right)}=\frac{1}{(2 \pi)(3)(300 \mu \mathrm{~F})}=177 \mathrm{~Hz}$
The gain exhibited by the open loop power supply at the high input voltage will be:

$$
A=\frac{\left(V_{\text {in max }}-V_{\text {out }}\right)^{2} N s}{\left(\left(V_{\text {in max }}\right)\left(V_{\text {error }}\right)(N p)\right)}=\frac{(382 \mathrm{~V}-6.0 \mathrm{~V})^{2}(7)}{(382 \mathrm{~V})(1.2 \mathrm{~V})(139)}
$$

$$
=15.53=23.82 \mathrm{~dB}
$$

The maximum recommended bandwidth is approximately:
$\mathrm{f}_{\mathrm{C}}=\frac{\mathrm{fs} \mathrm{min}}{5}=\frac{70 \mathrm{kHz}}{5}=14 \mathrm{kHz}$
The gain needed by the error amplifier to achieve this bandwidth is calculated at the rated load because that yields the bandwidth condition, which is:

$$
\mathrm{Gc}=20 \log \left(\frac{\mathrm{f}_{\mathrm{C}}}{f_{\mathrm{ph}}}\right)-\mathrm{A}=20 \log \left(\frac{14 \mathrm{kHz}}{177}\right)-23.82 \mathrm{~dB}
$$

$$
=14.14 \mathrm{~dB}
$$

The gain in absolute terms is:
$A_{C}=10^{(G c / 20)}=10^{(14.14 / 20)}=51$
Now the compensation circuit elements can be calculated. The output resistance of the voltage sense divider is given by the parallel combination of resistors in the divider:

$$
\begin{aligned}
& R_{\text {in }}=R_{\text {upper }}\left\|R_{\text {lower }}=10 k\right\| 14 k=5833 \Omega \\
& R 9=(A c)\left(R_{\text {in }}\right)=29.75 k \approx 30 k \\
& C 8=\frac{1}{\left[2 \pi\left(A_{c}\right)\left(R_{i n}\right)\left(f_{c}\right)\right]}=382 p F \approx 390 \mathrm{pF}
\end{aligned}
$$

The compensation zero must be placed at or below the light load filter pole:
$C 7=\frac{1}{\left[2 \pi(R 9)\left(f_{p n}\right)\right]}=11.63 \mu \mathrm{~F} \approx 10 \mu \mathrm{~F}$


Figure 10. Critical Conduction Mode Flyback Converter
CONVERTER TEST DATA

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=120 \mathrm{VAC}$ to $240 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.8 \mathrm{~A}$ | $\Delta \mathrm{~V}=50 \mathrm{mV}$ |
| Load | $\mathrm{V}_{\text {in }}=120 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.2 \mathrm{~A}$ to 0.8 A | $\Delta \mathrm{~V}=40 \mathrm{mV}$ |
|  | $\mathrm{V}_{\text {in }}=240 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.2 \mathrm{~A}$ to 0.8 A | $\Delta \mathrm{~V}=40 \mathrm{mV}$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=120 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.8 \mathrm{~A}$ | $\Delta \mathrm{~V}=290 \mathrm{mV}$ |
|  | $\mathrm{V}_{\text {in }}=240 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.8 \mathrm{~A}$ | $\Delta \mathrm{~V}=24 \mathrm{mV}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=120 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.8 \mathrm{~A}$ | $\eta=78.0 \%$ |
|  | $\mathrm{~V}_{\text {in }}=240 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.8 \mathrm{~A}$ | $\eta=79.4 \%$ |
| Power Factor | $\mathrm{V}_{\text {in }}=120 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.8 \mathrm{~A}$ | $\mathrm{Pf}=0.491$ |
|  | $\mathrm{~V}_{\text {in }}=240 \mathrm{VAC}, \mathrm{I}_{\text {out }}=0.8 \mathrm{~A}$ | $\mathrm{Pf}=0.505$ |



Ch2: 200mA/div
Figure 11. Load Regulation 120V


Figure 12. Load Regulation 240V


Figure 13. Universal Input Battery Charger

## MC33364

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC33364D1 | SO-8 | 98 Units / Rail |
| MC33364D1R2 | SO-8 Tape \& Reel | 2500 Units / Tape \& Reel |
| MC33364D2 | SO-8 | 98 Units / Rail |
| MC33364D2R2 | SO-8 Tape \& Reel | 2500 Units / Tape \& Reel |
| MC33364D | SO-16 | 48 Units / Rail |
| MC33364DR2 | SO-16 Tape \& Reel | 2500 Units / Tape \& Reel |

## High Voltage Switching Regulator

The MC33363 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on-chip 700 V/1.0 A SenseFET power switch, 450 V active off-line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16-lead dual-in-line and wide body surface mount packages.

- On-Chip 700 V, 1.0 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On-Chip 450 V Active Off-Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle-By-Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

Simplified Application


This device contains 221 active transistors.

## MC33363

## HIGH VOLTAGE OFF-LINE SWITCHING REGULATOR

## SEMICONDUCTOR

 TECHNICAL DATA

DW SUFFIX
PLASTIC PACKAGE CASE 751N (SOP-16L)


P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP-16)


## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| $\begin{array}{l}\text { Power Switch (Pin 16) } \\ \text { Drain Voltage } \\ \text { Drain Current }\end{array}$ | $V_{\text {DS }}$ | 700 | V |
| $\begin{array}{l}\text { Startup Input Voltage (Pin 1, Note 1) } \\ \text { Pin 3 = Gnd } \\ \text { Pin } 3 \leq 1000 ~\end{array}$ F to ground |  |  |  |$)$

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin }} 8=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{J}}$ is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REGULATOR (Pin 8) |  |  |  |  |  |
| Output Voltage ( $\mathrm{l} \mathrm{O}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {reg }}$ | 5.5 | 6.5 | 7.5 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to 40 V ) | Regline | - | 30 | 500 | mV |
| Load Regulation ( l = $=0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 44 | 200 | mV |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {reg }}$ | 5.3 | - | 8.0 | V |

OSCILLATOR (Pin 7)

| Frequency | fosc |  |  |  |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$ |  |  |  |  |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right)$ |  |  |  | kHz |
| $\mathrm{T}_{J}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V$)$ |  | 260 | 285 | 310 |
| $\mathrm{C}_{\mathrm{T}}=2.0 \mathrm{nF}$ |  | 255 | - | 315 |
| $\mathrm{~T}_{J}=25^{\circ} \mathrm{C}(\mathrm{V} \mathrm{VC}=20 \mathrm{~V})$ |  |  |  |  |
| $\mathrm{T}_{J}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V$)$ |  | 60 | 67.5 | 75 |
| Frequency Change with Voltage $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V$)$ |  | 59 | - | 76 |

ERROR AMPLIFIER (Pins 9, 10)

| Voltage Feedback Input Threshold | $\mathrm{V}_{\mathrm{FB}}$ | 2.52 | 2.6 | 2.68 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to $\left.40 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | Regline | - | 0.6 | 5.0 | mV |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{FB}}=2.6 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 20 | 500 | nA |
| Open Loop Voltage Gain $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{A}_{\mathrm{VOL}}$ | - | 82 | - | dB |
| Gain Bandwidth Product $\left(\mathrm{f}=100 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | GBW | - | 1.0 | - | MHz |

NOTES: 1. Maximum power dissipation limits must be observed.
2. Tested junction temperature range for the MC33363:
$\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}$
$\mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$

## MC33363

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}\right.$, $\mathrm{C}_{\text {Pin } 8}=1.0 \mu \mathrm{~F}$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{J}}$ is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER (Pins 9, 10) |  |  |  |  |  |
| Output Voltage Swing <br> High State ( Isource $=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}<2.0 \mathrm{~V}$ ) <br> Low State ( Isink $=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}>3.0 \mathrm{~V}$ ) | $\mathrm{V}_{\mathrm{OH}}$ <br> $V_{\text {OL }}$ | 4.0 | $\begin{aligned} & 5.3 \\ & 0.2 \end{aligned}$ | $\overline{-}$ | V |

OVERVOLTAGE DETECTION (Pin 11)

| Input Threshold Voltage | $\mathrm{V}_{\text {th }}$ | 2.47 | 2.6 | 2.73 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\text {in }}=2.6 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 100 | 500 | nA |

PWM COMPARATOR (Pins 7, 9)

| Duty Cycle |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum $\left(\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}\right)$ |  |  |  |  |  |
| Minimum $\left(\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\max )}$ | 48 | 50 | 52 | $\%$ |
|  | $\mathrm{DC}_{(\min )}$ | - | 0 | 0 |  |

POWER SWITCH (Pin 16)

| $\begin{aligned} & \text { Drain-Source On-State Resistance }\left(I_{\mathrm{D}}=200 \mathrm{~mA}\right) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=\mathrm{T}_{\text {low }} \text { to } T_{\text {high }} \end{aligned}$ | $\mathrm{R}_{\mathrm{DS} \text { (on) }}$ | - | $14$ | $\begin{aligned} & 17 \\ & 32 \end{aligned}$ | $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drain-Source Off-State Leakage Current ( $\mathrm{V}_{\mathrm{DS}}=700 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{D} \text { (off) }}$ | - | 0.2 | 50 | $\mu \mathrm{A}$ |
| Rise Time | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | - | ns |
| Fall Time | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | - | ns |
| OVERCURRENT COMPARATOR (Pin 16) |  |  |  |  |  |
| Current Limit Threshold ( $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}$ ) | 1 lim | 0.5 | 0.72 | 0.9 | A |
| STARTUP CONTROL (Pin 1) |  |  |  |  |  |
| $\begin{aligned} & \text { Peak Startup Current }\left(\mathrm{V}_{\mathrm{in}}=400 \mathrm{~V}\right) \\ & \mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=\left(\mathrm{V}_{\mathrm{th}(\mathrm{on})}-0.2 \mathrm{~V}\right) \end{aligned}$ | $I_{\text {start }}$ | - | $\begin{aligned} & 20 \\ & 6.0 \end{aligned}$ | - | mA |
| Off-State Leakage Current ( $\left.\mathrm{V}_{\text {in }}=50 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{D} \text { (off) }}$ | - | 40 | 200 | $\mu \mathrm{A}$ |

UNDERVOLTAGE LOCKOUT (Pin 3)

| Startup Threshold ( $\mathrm{V}_{\text {CC }}$ Increasing) | $\mathrm{V}_{\mathrm{th}(\mathrm{on})}$ | 11 | 15.2 | 18 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On | $\mathrm{V}_{\mathrm{CC}(\text { min })}$ | 7.5 | 9.5 | 11.5 | V |

TOTAL DEVICE (Pin 3)

| Power Supply Current | $I_{C C}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Startup (VCC $=10 \mathrm{~V}$, Pin 1 Open) |  | - | 0.25 | 0.5 |  |
| Operating |  | - | 3.2 | 5.0 |  |



Figure 1. Oscillator Frequency versus Timing Resistor


Figure 2. Power Switch Peak Drain Current versus Timing Resistor


Figure 3. Oscillator Charge/Discharge Current versus Timing Resistor


Figure 4. Maximum Output Duty Cycle versus Timing Resistor Ratio


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency


Figure 6. Error Amp Output Saturation Voltage versus Load Current


Figure 7. Error Amplifier Small Signal Transient Response


Figure 9. Regulator Output Voltage Change versus Source Current


Figure 11. Power Switch Drain-Source On-Resistance versus Temperature


Figure 13. Supply Current versus Supply Voltage


Figure 10. Peak Startup Current versus Power Supply Voltage


Figure 12. Power Switch Drain-Source Capacitance versus Voltage


Figure 14. DW and P Suffix Transient Thermal Resistance


Figure 15. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

PIN FUNCTION DESCRIPTION

| Pin | Function | Description |
| :---: | :---: | :---: |
| 1 | Startup Input | This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the $\mathrm{V}_{\mathrm{CC}}$ pin to ground. |
| 2 | - | This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the $\mathrm{V}_{\mathrm{CC}}$ potential on Pin 3. |
| 3 | $\mathrm{V}_{C C}$ | This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding. |
| 4, 5, 12, 13 | Ground | These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board. |
| 6 | $\mathrm{R}_{\text {T }}$ | Resistor $\mathrm{R}_{\mathrm{T}}$ connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency. |
| 7 | $\mathrm{C}_{\text {T }}$ | Capacitor $\mathrm{C}_{\top}$ connects from this pin to ground. The value selected, in conjunction with resistor $\mathrm{R}_{\mathrm{T}}$, programs the Oscillator frequency. |
| 8 | Regulator Output | This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability. |
| 9 | Compensation | This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator. |
| 10 | Voltage Feedback Input | This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 11 | Overvoltage Protection Input | This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 14, 15 | - | These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13. |
| 16 | Power Switch Drain | This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . |



Figure 17. Representative Block Diagram


Figure 18. Timing Diagram

## OPERATING DESCRIPTION

## Introduction

The MC33363 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 17 and 18.

## Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Resistor $\mathrm{R}_{\mathrm{T}}$ programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 3. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz . The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50\% limit by providing an additional charge or discharge current path to $\mathrm{C}_{\mathrm{T}}$, Figure 19. In order to increase the maximum duty cycle, a discharge current resistor $R_{D}$ is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor $\mathrm{R}_{\mathrm{C}}$ is connected from Pin 7 to the Regulator Output. Figure 4 shows an obtainable range of maximum output duty cycle versus the ratio of either $\mathrm{R}_{\mathrm{C}}$ or $\mathrm{R}_{\mathrm{D}}$ with respect to $\mathrm{R}_{\mathrm{T}}$.


Figure 19. Maximum Duty Cycle Modification

The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for $\mathrm{C}_{\mathrm{T}}$ values greater than 500 pF . For smaller values of $\mathrm{C}_{\mathrm{T}}$, refer to Figure 1. Note that resistor $\mathrm{R}_{\mathrm{T}}$ also programs the Current Limit Comparator threshold.

$$
\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}=\frac{5.4}{\mathrm{R}_{\mathrm{T}}} \quad \mathrm{f} \approx \frac{\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}}{4 \mathrm{C}_{\mathrm{T}}}
$$

## PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non-inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while $\mathrm{C}_{\mathrm{T}}$ is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When $\mathrm{C}_{\mathrm{T}}$ charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp-up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 18 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

## Current Limit Comparator and Power Switch

The MC33363 uses cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 1780 cells, of which 46 are connected to a $9.0 \Omega$ ground-referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the $450 \Omega$ resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor $\mathrm{R}_{\mathrm{T}}$. Therefore when selecting the values for $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}, \mathrm{R}_{\mathrm{T}}$ must be chosen first to set the Power Switch peak drain current, while $\mathrm{C}_{\mathrm{T}}$ is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus $\mathrm{R}_{\mathrm{T}}$ is shown in Figure 2 with the related formula below.

$$
\mathrm{I}_{\mathrm{pk}}=8.8\left(\frac{\mathrm{R}_{\mathrm{T}}}{1000}\right)-1.077
$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn-on transition is completed. The current limit propagation delay time is typically 233 ns . This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn-off.

## Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 17. It features a typical dc voltage gain of 82 dB , and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 5. The noninverting input is internally biased at $2.6 \mathrm{~V} \pm 3.1 \%$ and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of $270 \mu \mathrm{~A}$, allowing it to be easily overridden with a pull-up resistor. This is desirable in applications that require secondary side voltage sensing, Figure 20. In this application, the Voltage Feedback Input is connected to the Regulator Output. This disables the Error Amplifier by placing its output into the sink state, allowing the optocoupler transistor to directly control the PWM Comparator.

## Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side $\mathrm{V}_{\mathrm{CC}}$ voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

## Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the $\mathrm{V}_{\mathrm{CC}}$ voltage at Pin 3 and when it exceeds 14.5 V , the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

## Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33363. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off-line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor that connects from Pin 3 to ground. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold of 15.2 V , the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide an initial peak current of 20 mA , Figure 10, which decreases rapidly as $\mathrm{V}_{\mathrm{CC}}$ and the die temperature rise. The steady state current will self limit in the range of 8.0 mA with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground. The startup MOSFET is rated at a maximum of 400 V with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground, and 500 V when charging a $\mathrm{V}_{\mathrm{CC}}$ capacitor of $1000 \mu \mathrm{~F}$ or less.

## Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short-circuit protection. This output requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability.

## Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at $155^{\circ} \mathrm{C}$, the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below $145^{\circ} \mathrm{C}$. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33363 is contained in a heatsinkable plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 15 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper. Figure 22 shows a practical example of a printed circuit board layout that utilizes the copper foil as a heat dissipater. Note that a jumper was added to the layout from Pins 8 to 10 in order to enhance the copper area near the device for improved thermal conductivity. The application circuit requires two ounce copper foil in order to obtain 8.0 watts of continuous output power at room temperature.


Figure 20. 8.0 W Off-Line Converter

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=92 \mathrm{Vac}$ to $276 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}} 1.6 \mathrm{~A}$ | $\Delta=1.0 \mathrm{mV}$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=0.4 \mathrm{~A}$ to 1.6 A | $\Delta=4.0 \mathrm{mV}$ |
|  | $\mathrm{V}_{\text {in }}=230 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=0.4 \mathrm{~A}$ to 1.6 A | $\Delta=4.0 \mathrm{mV}$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=1.6 \mathrm{~A}$ | Triangular $=2.0 \mathrm{mVpp}$, Spike $=12 \mathrm{mVpp}$ |
|  | $\mathrm{V}_{\text {in }}=230 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=1.6 \mathrm{~A}$ | Triangular $=2.0 \mathrm{mVpp}$, Spike $=12 \mathrm{mVpp}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=1.6 \mathrm{~A}$ | $78.6 \% *$ |
|  | $\mathrm{~V}_{\text {in }}=230 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=1.6 \mathrm{~A}$ | $75.6 \%$ |

This data was taken with the components listed below mounted on the printed circuit board shown in Figure 22.

* With MBR2535CTL, $79.8 \%$ efficiency. PCB layout modification is required to use this rectifier.

For high efficiency and small circuit board size, the Sanyo Os-Con capacitors are recommended for C8, C9, C10 and C11.
C8, C9, C10 = Sanyo Os-Con \#6SA330M, 330 нF 6.3 V.
C11 = Sanyo Os-Con \#10SA220M, $220 \mu \mathrm{~F} 10 \mathrm{~V}$.
L1 = Coilcraft S5088-A, $5.0 \mu \mathrm{H}, 0.11 \Omega$.
T1 = Coilcraft S5502-A
Primary: 77 turns of \# 28 AWG, Pin $1=$ start, Pin $8=$ finish.
Two layers 0.002" Mylar tape.
Secondary: 5 turns of \# 22 AWG, 2 strands bifiliar wound, Pin $5=$ start, Pin $4=$ finish.
Two layers 0.002" Mylar tape.
Auxiliary: 13 turns of \# 28 AWG wound in center of bobbin, Pin $2=$ start, Pin $7=$ finish.
Two layers $0.002^{\prime \prime}$ Mylar tape.
Gap: 0.006 " total for a primary inductance ( $L_{p}$ ) of 1.0 mH .
Core and Bobbin: Coilcraft PT1950, E187, 3F3 material.
Figure 21. Converter Test Data


Figure 22. Printed Circuit Board and Component Layout (Circuit of Figure 20)

## MC33363A

## High Voltage Switching Regulator

The MC33363A is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on-chip $700 \mathrm{~V} / 1.5 \mathrm{~A}$ SenseFET power switch, 500 V active off-line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16-lead dual-in-line and wide body surface mount packages.

- Enhanced Power Capability Over MC33363
- On-Chip 700 V, 1.5 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On-Chip 500 V Active Off-Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle-By-Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown




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http://onsemi.com


PIN CONNECTIONS

(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33363ADW | SO-16W | 47 Units/Rail |
| MC33363ADWR2 | SO-16W | 1000 Tape \& Reel |
| MC33363AP | PDIP-16 | 25 Units/Rail |

Figure 1. Simplified Application

## MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Switch (Pin 16) <br> Drain Voltage <br> Drain Current | $\begin{aligned} & \mathrm{V}_{\mathrm{DS}} \\ & \mathrm{I}_{\mathrm{DS}} \end{aligned}$ | $\begin{gathered} 700 \\ 1.5 \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { A } \end{aligned}$ |
| Startup Input Voltage (Pin 1, Note 2) <br> Pin $3=$ Gnd <br> Pin $3 \leq 1000 \mu \mathrm{~F}$ to ground | $V_{\text {in }}$ | $\begin{aligned} & 400 \\ & 500 \end{aligned}$ | V |
| Power Supply Voltage (Pin 3) | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| Input Voltage Range <br> Voltage Feedback Input (Pin 10) <br> Compensation (Pin 9) <br> Overvoltage Protection Input (Pin 11) <br> $\mathrm{R}_{\mathrm{T}}(\mathrm{Pin} 6)$ <br> $\mathrm{C}_{\mathrm{T}}$ (Pin 7) | $\mathrm{V}_{\text {IR }}$ | -1.0 to $\mathrm{V}_{\text {reg }}$ | V |
| Thermal Characteristics <br> P Suffix, Dual-In-Line Case 648E <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> (Pins 4, 5, 12, 13) <br> DW Suffix, Surface Mount Case 751N <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> (Pins 4, 5, 12, 13) <br> Refer to Figures 16 and 17 for additional thermal information. | $\mathrm{R}_{\text {日JA }}$ $\mathrm{R}_{\text {өJc }}$ <br> $\mathrm{R}_{\text {日JA }}$ $\mathrm{R}_{\text {өJc }}$ | $\begin{aligned} & 80 \\ & 15 \\ & \\ & 95 \\ & 15 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -25 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin }} 8=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$,
for min/max values $T_{J}$ is the operating junction temperature range that applies (Note 3), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REGULATOR (Pin 8) |  |  |  |  |  |
| Output Voltage ( $\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {reg }}$ | 5.5 | 6.5 | 7.5 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to 40 V ) | $\mathrm{Reg}_{\text {line }}$ | - | 30 | 500 | mV |
| Load Regulation ( $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 44 | 200 | mV |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {reg }}$ | 5.3 | - | 8.0 | V |

OSCILLATOR (Pin 7)

| Frequency | fosc |  |  |  | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$ |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right)$ |  | 260 | 285 | 310 |  |
| $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V$)$ |  | 255 | - | 315 |  |
| $\mathrm{C}_{\mathrm{T}}=2.0 \mathrm{nF}$ |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}(\mathrm{V} \mathrm{CC}=20 \mathrm{~V})$ |  | 60 | 67.5 | 75 |  |
| $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V$)$ |  | 59 | - | 76 |  |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to 40 V ) | $\Delta \mathrm{f}_{\text {Osc }} / \Delta \mathrm{V}$ | - | 0.1 | 2.0 | kHz |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
2. Maximum power dissipation limits must be observed.
3. Tested junction temperature range for the MC33363A:

$$
\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C} \quad \mathrm{~T}_{\text {high }}=+125^{\circ} \mathrm{C}
$$

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin } 8}=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min/max values $T_{j}$ is the operating junction temperature range that applies (Note 4), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER (Pins 9, 10) |  |  |  |  |  |
| Voltage Feedback Input Threshold | $\mathrm{V}_{\mathrm{FB}}$ | 2.52 | 2.6 | 2.68 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | Regline | - | 0.6 | 5.0 | mV |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB}}=2.6 \mathrm{~V}$ ) | $I_{\text {IB }}$ | - | 20 | 500 | nA |
| Open Loop Voltage Gain ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | Avol | - | 82 | - | dB |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | GBW | - | 1.0 | - | MHz |
| $\begin{aligned} & \text { Output Voltage Swing } \\ & \text { High State }\left(I_{\text {Source }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}<2.0 \mathrm{~V}\right) \\ & \text { Low State }\left(I_{\text {Sink }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}>3.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ <br> $\mathrm{V}_{\mathrm{OL}}$ | 4.0 | $\begin{aligned} & 5.3 \\ & 0.2 \end{aligned}$ | $\stackrel{-}{0.35}$ | V |

## OVERVOLTAGE DETECTION (Pin 11)

| Input Threshold Voltage | $\mathrm{V}_{\text {th }}$ | 2.47 | 2.6 | 2.73 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\text {in }}=2.6 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 100 | 500 | nA |

PWM COMPARATOR (Pins 7, 9)

| Duty Cycle |  |  |  |  | $\%$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum $\left(\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\max )}$ | 48 | 50 | 52 |  |
| Minimum $\left(\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\min )}$ | - | 0 | 0 |  |

POWER SWITCH (Pin 16)

| Drain-Source On-State Resistance $\left(\mathrm{I}_{\mathrm{D}}=200 \mathrm{~mA}\right)$ | $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | - | 7.5 | 9.0 | $\Omega$ |
| $\mathrm{~T}_{J}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ |  | - | - | 20 |  |
| Drain-Source Off-State Leakage Current | $\mathrm{I}_{\mathrm{D}(\mathrm{off})}$ |  |  |  | $\mu \mathrm{A}$ |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{DS}}=700 \mathrm{~V}$ | - | 0.2 | 100 |  |  |
| $\mathrm{~T}_{J}=-25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{DS}}=65 \mathrm{~V}$ |  | - | 0.2 | 100 |  |
| Rise Time | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | - | ns |
| Fall Time | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | - | ns |

OVERCURRENT COMPARATOR (Pin 16)

| Current Limit Threshold $\left(R_{T}=13 \mathrm{k}\right)$ | $\lim _{\text {lim }}$ | 0.7 | 0.9 | 1.1 | A |
| :--- | :--- | :--- | :--- | :--- | :--- |

STARTUP CONTROL (Pin 1)

| Peak Startup Current $\left(\mathrm{V}_{\text {in }}=400 \mathrm{~V}\right)$ <br> $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ <br> $\mathrm{~V}_{\mathrm{CC}}=\left(\mathrm{V}_{\text {th(on) }}-0.2 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {start }}$ |  |  |
| :--- | :--- | :--- | :--- | :--- |
| Off-State Leakage Current $\left(\mathrm{V}_{\text {in }}=50 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}\right)$ | - | 22 |  |

UNDERVOLTAGE LOCKOUT (Pin 3)

| Startup Threshold (VCC Increasing) | $\mathrm{V}_{\mathrm{th}(\mathrm{on})}$ | 11 | 14.9 | 18 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On | $\mathrm{V}_{\mathrm{CC}(\mathrm{min})}$ | 7.5 | 9.5 | 11.5 | V |

## TOTAL DEVICE (Pin 3)

| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ |  |  | mA |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Startup (VCC $=10 \mathrm{~V}$, Pin 1 Open) |  | - | 0.27 | 0.5 |  |
| Operating |  | - | 3.4 | 5.0 |  |

4. Tested junction temperature range for the MC33363A:

$$
\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C} \quad \mathrm{~T}_{\text {high }}=+125^{\circ} \mathrm{C}
$$



Figure 2. Oscillator Frequency versus Timing Resistor


Figure 4. Oscillator Charge/Discharge Current versus Timing Resistor

Figure 3. Power Switch Peak Drain Current versus Timing Resistor


Figure 5. Maximum Output Duty Cycle versus Timing Resistor Ratio


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency


Figure 7. Error Amp Output Saturation Voltage versus Load Current

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 8. Error Amplifier Small Signal Transient Response

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 9. Error Amplifier Large Signal Transient Response


Figure 11. Peak Startup Current versus Power Supply Voltage


Figure 12. Power Switch Drain-Source On-Resistance versus Temperature


Figure 13. Power Switch Drain-Source Capacitance versus Voltage


Figure 14. Supply Current versus Supply Voltage


Figure 16. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 15. DW and P Suffix Transient Thermal Resistance


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

PIN FUNCTION DESCRIPTION

| Pin | Function | Description |
| :---: | :---: | :---: |
| 1 | Startup Input | This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the $\mathrm{V}_{\mathrm{CC}}$ pin to ground. |
| 2 | - | This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the $\mathrm{V}_{\mathrm{CC}}$ potential on Pin 3. |
| 3 | $\mathrm{V}_{C C}$ | This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding. |
| 4, 5, 12, 13 | Ground | These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board. |
| 6 | $\mathrm{R}_{\mathrm{T}}$ | Resistor $\mathrm{R}_{\mathrm{T}}$ connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency. |
| 7 | $\mathrm{C}_{\text {T }}$ | Capacitor $\mathrm{C}_{\mathrm{T}}$ connects from this pin to ground. The value selected, in conjunction with resistor $\mathrm{R}_{\mathrm{T}}$, programs the Oscillator frequency. |
| 8 | Regulator Output | This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability. |
| 9 | Compensation | This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator. |
| 10 | Voltage Feedback Input | This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 11 | Overvoltage Protection Input | This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 14, 15 | - | These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13. |
| 16 | Power Switch Drain | This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . |



Figure 18. Representative Block Diagram


Figure 19. Timing Diagram

## OPERATING DESCRIPTION

## Introduction

The MC33363A represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 18 and 19.

## Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Resistor $\mathrm{R}_{\mathrm{T}}$ programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 4. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz . The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50\% limit by providing an additional charge or discharge current path to $\mathrm{C}_{\mathrm{T}}$, Figure 20. In order to increase the maximum duty cycle, a discharge current resistor $R_{D}$ is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor $\mathrm{R}_{\mathrm{C}}$ is connected from Pin 7 to the Regulator Output. Figure 5 shows an obtainable range of maximum output duty cycle versus the ratio of either $\mathrm{R}_{\mathrm{C}}$ or $\mathrm{R}_{\mathrm{D}}$ with respect to $\mathrm{R}_{\mathrm{T}}$.


The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for $\mathrm{C}_{\mathrm{T}}$ values greater than 500 pF . For smaller values of $\mathrm{C}_{\mathrm{T}}$, refer to Figure 2. Note that resistor $\mathrm{R}_{\mathrm{T}}$ also programs the Current Limit Comparator threshold.

$$
\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}=\frac{5.4}{\mathrm{R}_{\mathrm{T}}} \quad \mathrm{f} \approx \frac{\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}}{4 \mathrm{C}_{\mathrm{T}}}
$$

## PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non-inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while $\mathrm{C}_{\mathrm{T}}$ is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When $\mathrm{C}_{\mathrm{T}}$ charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp-up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 19 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

## Current Limit Comparator and Power Switch

The MC33363A uses cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 2819 cells, of which 65 are connected to a $6.0 \Omega$ ground-referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the $450 \Omega$ resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor $\mathrm{R}_{\mathrm{T}}$. Therefore when selecting the values for $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}, \mathrm{R}_{\mathrm{T}}$ must be chosen first to set the Power Switch peak drain current, while $\mathrm{C}_{\mathrm{T}}$ is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus $\mathrm{R}_{\mathrm{T}}$ is shown in Figure 3 with the related formula below.

$$
\mathrm{I}_{\mathrm{pk}}=15.95\left(\frac{\mathrm{R}_{\mathrm{T}}}{1000}\right)-1.14
$$

Figure 20. Maximum Duty Cycle Modification

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn-on transition is completed. The current limit propagation delay time is typically 300 ns . This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn-off.

## Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 18. It features a typical dc voltage gain of 82 dB , and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 6. The noninverting input is internally biased at $2.6 \mathrm{~V} \pm 3.1 \%$ and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of $270 \mu \mathrm{~A}$, allowing it to be easily overridden with a pull-up resistor. This is desirable in applications that require secondary side voltage sensing, Figure 21. In this application, the Voltage Feedback Input is connected to the Regulator Output. This disables the Error Amplifier by placing its output into the sink state, allowing the optocoupler transistor to directly control the PWM Comparator.

## Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side $\mathrm{V}_{\mathrm{CC}}$ voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

## Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the $\mathrm{V}_{\mathrm{CC}}$ voltage at Pin 3 and when it exceeds 14.5 V , the reset signal is removed from the PWM Latch allowing operation of the

Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

## Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33363A. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off-line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor that connects from Pin 3 to ground. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold of 15.2 V , the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide an initial peak current of 20 mA , Figure 11 , which decreases rapidly as $\mathrm{V}_{\mathrm{CC}}$ and the die temperature rise. The steady state current will self limit in the range of 8.0 mA with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground. The startup MOSFET is rated at a maximum of 400 V with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground, and 500 V when charging a $\mathrm{V}_{\mathrm{CC}}$ capacitor of $1000 \mu \mathrm{~F}$ or less.

## Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short-circuit protection. This output requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability.

## Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at $155^{\circ} \mathrm{C}$, the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below $145^{\circ} \mathrm{C}$. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33363A is contained in a heatsinkable plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper. Figure 23 shows a practical example of a printed circuit board layout

## MC33363A

that utilizes the copper foil as a heat dissipater. Note that a jumper was added to the layout from Pins 8 to 10 in order to enhance the copper area near the device for improved thermal
conductivity. The application circuit requires two ounce copper foil in order to obtain 8.0 watts of continuous output power at room temperature.


Figure 21. 15 W Off-Line Converter

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=92 \mathrm{Vac}$ to $276 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}} 3.0 \mathrm{~A}$ | $\Delta=1.0 \mathrm{mV}$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=0.75 \mathrm{~A}$ to 3.0 A | $\Delta=5.0 \mathrm{mV}$ |
|  | $\mathrm{V}_{\text {in }}=230 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=0.75 \mathrm{~A}$ to 3.0 A | $\Delta=5.0 \mathrm{mV}$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}$ | Triangular $=2.0 \mathrm{mVpp}$, Spike $=32 \mathrm{mVpp}$ |
|  | $\mathrm{V}_{\text {in }}=230 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}$ | Triangular $=2.0 \mathrm{mVpp}$, Spike $=34 \mathrm{mVpp}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}$ | $76.8 \%^{*}$ |
|  | $\mathrm{~V}_{\text {in }}=230 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}$ | $76.8 \%$ |

This data was taken with the components listed below mounted on the printed circuit board shown in Figure 23.

* With MBR2535CTL, $78.8 \%$ efficiency. PCB layout modification is required to use this rectifier.

For high efficiency and small circuit board size, the Sanyo Os-Con capacitors are recommended for C8, C9, C10 and C11.
C8, C9, C10 = Sanyo Os-Con \#6SA330M, $330 \mu \mathrm{~F} 6.3 \mathrm{~V}$.
C11 = Sanyo Os-Con \#10SA220M, $220 \mu \mathrm{~F} 10 \mathrm{~V}$.
L1 = Coilcraft S5088-A, $5.0 \mu \mathrm{H}, 0.11 \Omega$.
T1 = Coilcraft U6875-A
Primary: 77 turns of \# 28 AWG, Pin $1=$ start, Pin $8=$ finish.
Two layers $0.002^{\prime \prime}$ Mylar tape.
Secondary: 5 turns of \# 22 AWG, 2 strands bifiliar wound, Pin $5=$ start, Pin $4=$ finish.
Two layers $0.002^{\prime \prime}$ Mylar tape.
Auxiliary: 13 turns of \# 28 AWG wound in center of bobbin, Pin $2=$ start, Pin $7=$ finish.
Two layers $0.002^{\prime \prime}$ Mylar tape.
Gap: $0.011^{\prime \prime}$ total for a primary inductance ( $L_{P}$ ) of $620 \mu \mathrm{H}$.
Core and Bobbin: Coilcraft PT1950, E187, 3F3 material.
Figure 22. Converter Test Data


Figure 23. Printed Circuit Board and Component Layout (Circuit of Figure 21)

## MC33363B

## High Voltage Switching Regulator

The MC33363B is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on-chip $700 \mathrm{~V} / 1.0 \mathrm{~A}$ SENSEFET power switch, 450 V active off-line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, overvoltage protection, and thermal shutdown. This device is available in a 16-lead dual-in-line and wide body surface mount packages.

- On-Chip 700 V, 1.0 A SENSEFET Power Switch
- Rectified 240 Vac Line Source Operation
- On-Chip 450 V Active Off-Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle-By-Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Over-Voltage Protection
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33363BDW | SO-16W | 47 Units/Rail |
| MC33363BDWR2 | SO-16W | 1000 Tape \& Reel |
| MC33363BP | PDIP-16 | 25 Units/Rail |

Figure 1. Simplified Application

## MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Switch (Pin 16) Drain Voltage Drain Current | $\begin{aligned} & \mathrm{V}_{\mathrm{DS}} \\ & \mathrm{I}_{\mathrm{DS}} \end{aligned}$ | $\begin{aligned} & 700 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { A } \end{aligned}$ |
| Startup Input Voltage (Pin 1, Note 2) <br> Pin $3=$ Gnd <br> Pin $3 \leq 1000 \mu \mathrm{~F}$ to ground | $V_{\text {in }}$ | $\begin{aligned} & 400 \\ & 500 \end{aligned}$ | V |
| Power Supply Voltage (Pin 3) | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| ```Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Overvoltage Protection Input (Pin 11) \(\mathrm{R}_{\mathrm{T}}\) (Pin 6) \(\mathrm{C}_{\mathrm{T}}\) (Pin 7)``` | $\mathrm{V}_{\mathrm{IR}}$ | -1.0 to $\mathrm{V}_{\text {reg }}$ | V |
| Thermal Characteristics <br> P Suffix, Dual-In-Line Case 648E <br> Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case DW Suffix, Surface Mount Case 751G Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case | $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJc }}$ | $\begin{aligned} & 80 \\ & 15 \\ & \\ & 95 \\ & 15 \\ & \hline \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -25 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin }} 8=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{J}}$ is the operating junction temperature range that applies (Note 3), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REGULATOR (Pin 8) |  |  |  |  |  |
| Output Voltage ( $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {reg }}$ | 5.5 | 6.5 | 7.5 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to 40 V ) | Regline | - | 30 | 500 | mV |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 44 | 200 | mV |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {reg }}$ | 5.3 | - | 8.0 | V |

OSCILLATOR (Pin 7)

| Frequency $\begin{aligned} \mathrm{C}_{\mathrm{T}} & =390 \mathrm{pF} \\ \mathrm{~T}_{J} & =25^{\circ} \mathrm{C}\left(\mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}\right) \\ \mathrm{T}_{J} & =\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V} \text { to } 40 \mathrm{~V}\right) \\ \mathrm{C}_{\mathrm{T}} & =2.0 \mathrm{nF} \\ \mathrm{~T}_{J} & =25^{\circ} \mathrm{C}\left(\mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}\right) \\ \mathrm{T}_{J} & =\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V} \text { to } 40 \mathrm{~V}\right) \end{aligned}$ | fosc | $\begin{aligned} & 260 \\ & 255 \\ & \\ & 60 \\ & 59 \end{aligned}$ | $285$ $67.5$ | $\begin{aligned} & 310 \\ & 315 \\ & 75 \\ & 76 \end{aligned}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to 40 V ) | $\Delta \mathrm{f}_{\mathrm{osc}} / \Delta \mathrm{V}$ | - | 0.1 | 2.0 | kHz |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
2. Maximum power dissipation limits must be observed.
3. Tested junction temperature range for the MC33363B:

$$
\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C} \quad \mathrm{~T}_{\text {high }}=+125^{\circ} \mathrm{C}
$$

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin }} 8=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min/max values $T_{J}$ is the operating junction temperature range that applies (Note 4), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER (Pins 9, 10) |  |  |  |  |  |
| Voltage Feedback Input Threshold | $\mathrm{V}_{\text {FB }}$ | 2.52 | 2.6 | 2.68 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | Regline | - | 0.6 | 5.0 | mV |
| Input Bias Current ( $\left.\mathrm{V}_{\mathrm{FB}}=2.6 \mathrm{~V}, \mathrm{~T}_{J}=0-125^{\circ} \mathrm{C}\right)$ | IIB | - | 20 | 500 | nA |
| Open Loop Voltage Gain ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | AvoL | 70 | 82 | 94 | dB |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | GBW | 0.85 | 1.0 | 1.15 | MHz |
| $\begin{aligned} & \text { Output Voltage Swing } \\ & \text { High State (l } \text { Isource }=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}<2.0 \mathrm{~V} \text { ) } \\ & \text { Low State }\left(\text { I Sink }=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}>3.0 \mathrm{~V}\right. \text { ) } \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $4.0$ | $\begin{aligned} & 5.3 \\ & 0.2 \end{aligned}$ | $\stackrel{-}{0.35}$ | V |

## OVERVOLTAGE DETECTION (Pin 11)

| Input Threshold Voltage | $\mathrm{V}_{\text {th }}$ | 2.47 | 2.6 | 2.73 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\text {in }}=2.6 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=-25-125^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 100 | 500 | nA |

PWM COMPARATOR (Pins 7, 9)

| Duty Cycle |  |  |  |  | $\%$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum $\left(V_{F B}=0 ~ V\right)$ |  |  |  |  |  |
| Minimum $\left(V_{F B}=2.7 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\max )}$ | 48 | 50 | 52 |  |

POWER SWITCH (Pin 16)

| $\begin{aligned} & \text { Drain-Source On-State Resistance }\left(\mathrm{I}_{\mathrm{D}}=200 \mathrm{~mA}\right) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{R}_{\mathrm{DS} \text { (on) }}$ | - | $15$ | $\begin{aligned} & 17 \\ & 39 \end{aligned}$ | $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drain-Source Off-State Leakage Current $V_{D S}=650 \mathrm{~V}$ | $I_{\text {(off) }}$ | - | 0.2 | 100 | $\mu \mathrm{A}$ |
| Rise Time | $t_{r}$ | - | 50 | - | ns |
| Fall Time | $t_{f}$ | - | 50 | - | ns |

OVERCURRENT COMPARATOR (Pin 16)

| Current Limit Threshold $\left(R_{T}=10 \mathrm{k}\right)$ | $\lim _{\text {lim }}$ | 0.5 | 0.72 | 0.9 | A |
| :--- | :--- | :--- | :--- | :--- | :--- |

STARTUP CONTROL (Pin 1)

| Peak Startup Current ( $\mathrm{V}_{\text {in }}=400 \mathrm{~V}$ ) (Note 5) $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=\left(\mathrm{V}_{\text {th( } \mathrm{on})}-0.2 \mathrm{~V}\right) \end{aligned}$ | $I_{\text {start }}$ | - | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 4.0 \\ & 4.0 \end{aligned}$ | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Off-State Leakage Current ( $\mathrm{V}_{\text {in }}=50 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}$ ) | $I_{D \text { (off) }}$ | - | 40 | 200 | $\mu \mathrm{A}$ |

UNDERVOLTAGE LOCKOUT (Pin 3)

| Startup Threshold (VCC Increasing) | $\mathrm{V}_{\text {th(on) }}$ | 11 | 15.2 | 18 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On | $\mathrm{V}_{\mathrm{CC}(\mathrm{min})}$ | 7.5 | 9.5 | 11.5 | V |

TOTAL DEVICE (Pin 3)

| Power Supply Current | $I_{C C}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Startup (VCC $=10 \mathrm{~V}$, Pin 1 Open) |  | - | 0.25 | 0.5 |  |
| Operating |  | - | 3.2 | 5.0 |  |

4. Tested junction temperature range for the MC33363B:
$\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C} \quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
5. The device can only guarantee to start up at high temperature below $+115^{\circ} \mathrm{C}$.


Figure 2. Oscillator Frequency versus Timing Resistor


Figure 4. Oscillator Charge/Discharge Current versus Timing Resistor


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency

Figure 3. Power Switch Peak Drain Current versus Timing Resistor


Figure 5. Maximum Output Duty Cycle versus Timing Resistor Ratio


Figure 7. Error Amp Output Saturation Voltage versus Load Current

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 8. Error Amplifier Small Signal Transient Response


Figure 10. Regulator Output Voltage
Change versus Source Current


Figure 12. Power Switch Drain-Source On-Resistance versus Temperature


Figure 13. Power Switch Drain-Source Capacitance versus Voltage

## MC33363B



Figure 14. Supply Current versus Supply Voltage


Figure 15. DW and P Suffix Transient Thermal Resistance


Figure 16. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

PIN FUNCTION DESCRIPTION

| Pin | Function | Description |
| :---: | :---: | :---: |
| 1 | Startup Input | This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the $\mathrm{V}_{\mathrm{CC}}$ pin to ground. |
| 2 | - | This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the $\mathrm{V}_{\mathrm{CC}}$ potential on Pin 3. |
| 3 | $\mathrm{V}_{C C}$ | This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding. |
| 4, 5, 12, 13 | Ground | These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board. |
| 6 | $\mathrm{R}_{\mathrm{T}}$ | Resistor $\mathrm{R}_{\mathrm{T}}$ connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency. |
| 7 | $\mathrm{C}_{\text {T }}$ | Capacitor $\mathrm{C}_{\mathrm{T}}$ connects from this pin to ground. The value selected, in conjunction with resistor $\mathrm{R}_{\mathrm{T}}$, programs the Oscillator frequency. |
| 8 | Regulator Output | This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability. |
| 9 | Compensation | This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator. |
| 10 | Voltage Feedback Input | This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 11 | Overvoltage Protection Input | This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 14, 15 | - | These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13. |
| 16 | Power Switch Drain | This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . |



Figure 18. Representative Block Diagram


Figure 19. Timing Diagram

## OPERATING DESCRIPTION

## Introduction

The MC33363B represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 18 and 19.

## Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Resistor $\mathrm{R}_{\mathrm{T}}$ programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 4. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz . The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50\% limit by providing an additional charge or discharge current path to $\mathrm{C}_{\mathrm{T}}$, Figure 20. In order to increase the maximum duty cycle, a discharge current resistor $\mathrm{R}_{\mathrm{D}}$ is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor $\mathrm{R}_{\mathrm{C}}$ is connected from Pin 7 to the Regulator Output. Figure 5 shows an obtainable range of maximum output duty cycle versus the ratio of either $R_{C}$ or $\mathrm{R}_{\mathrm{D}}$ with respect to $\mathrm{R}_{\mathrm{T}}$.


Figure 20. Maximum Duty Cycle Modification

The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for $\mathrm{C}_{\mathrm{T}}$ values greater than 500 pF . For smaller values of $\mathrm{C}_{\mathrm{T}}$, refer to Figure 2. Note that resistor $\mathrm{R}_{\mathrm{T}}$ also programs the Current Limit Comparator threshold.

$$
\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}=\frac{5.4}{\mathrm{R}_{\mathrm{T}}} \quad \mathrm{f} \approx \frac{\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}}{4 \mathrm{C}_{\mathrm{T}}}
$$

## PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non-inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while $\mathrm{C}_{\mathrm{T}}$ is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When $\mathrm{C}_{\mathrm{T}}$ charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp-up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 19 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

## Current Limit Comparator and Power Switch

The MC33363B uses cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The Power Switch is constructed as a SENSEFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 1462 cells, of which 36 are connected to a $8.1 \Omega$ ground-referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the $405 \Omega$ resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor $\mathrm{R}_{\mathrm{T}}$. Therefore when selecting the values for $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}, \mathrm{R}_{\mathrm{T}}$ must be chosen first to set the Power Switch peak drain current, while $\mathrm{C}_{\mathrm{T}}$ is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus $\mathrm{R}_{\mathrm{T}}$ is shown in Figure 3 with the related formula below.

$$
\mathrm{I}_{\mathrm{pk}}=8.8\left(\frac{\mathrm{R}_{\mathrm{T}}}{1000}\right)-1.077
$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn-on transition is completed. The current limit propagation delay time is typically 262 ns . This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn-off.

## Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 18. It features a typical dc voltage gain of 82 dB , and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 6. The noninverting input is internally biased at $2.6 \mathrm{~V} \pm 3.1 \%$ and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of $270 \mu \mathrm{~A}$, allowing it to be easily overridden with a pull-up resistor. This is desirable in applications that require secondary side voltage sensing.

## Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side $\mathrm{V}_{\mathrm{CC}}$ voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

## Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the $\mathrm{V}_{\mathrm{CC}}$ voltage at Pin 3 and when it exceeds 14.5 V , the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

## Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33363B. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off-line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor that connects from Pin 3 to ground. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold of 15.2 V , the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide a steady current of 1.7 mA , Figure 11, as $\mathrm{V}_{\mathrm{CC}}$ increases or shorted to ground. The startup MOSFET is rated at a maximum of 400 V with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground, and 500 V when charging a $\mathrm{V}_{\mathrm{CC}}$ capacitor of $1000 \mu \mathrm{~F}$ or less.

## Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short-circuit protection. This output requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability.

## Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at $150^{\circ} \mathrm{C}$, the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below $140^{\circ} \mathrm{C}$. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33363B is contained in a heatsinkable plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

## MC33365

## High Voltage Switching Regulator

The MC33365 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on-chip $700 \mathrm{~V} / 1.0 \mathrm{~A} \mathrm{SENSEFET}^{\text {TM }}$ power switch, 450 V active off-line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, bulk capacitor voltage sensing, and thermal shutdown. This device is available in a 16-lead dual-in-line package.

- On-Chip 700 V, 1.0 A SENSEFET Power Switch
- Rectified 240 Vac Line Source Operation
- On-Chip 450 V Active Off-Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle-By-Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Bulk Capacitor Voltage Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown


Figure 1. Simplified Application


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC33365P | PDIP-16 | 25 Units/Rail |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Switch (Pin 16) Drain Voltage Drain Current | $\begin{aligned} & \mathrm{V}_{\mathrm{DS}} \\ & \mathrm{I}_{\mathrm{DS}} \end{aligned}$ | $\begin{gathered} 700 \\ 1.0 \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { A } \end{aligned}$ |
| Startup Input Voltage (Pin 1, Note 1) <br> Pin $3=$ Gnd <br> Pin $3 \leq 1000 \mu \mathrm{~F}$ to ground | $\mathrm{V}_{\text {in }}$ | $\begin{aligned} & 400 \\ & 500 \end{aligned}$ | V |
| Power Supply Voltage (Pin 3) | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| ```Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Bulk OK Input (Pin 11) \(\mathrm{R}_{\mathrm{T}}\) (Pin 6) \(\mathrm{C}_{\mathrm{T}}\) (Pin 7)``` | $\mathrm{V}_{\text {IR }}$ | -1.0 to $\mathrm{V}_{\text {reg }}$ | V |
| $\begin{aligned} & \text { Thermal Characteristics } \\ & \text { P Suffix, Dual-In-Line Case 648E } \\ & \text { Thermal Resistance, Junction-to-Air } \\ & \text { Thermal Resistance, Junction-to-Case } \end{aligned}$ | $\begin{aligned} & R_{\text {}}^{\text {BJA }} \\ & R_{\theta J \mathrm{C}} \end{aligned}$ | $\begin{aligned} & 80 \\ & 15 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -25 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin }} 8=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for $\mathrm{min} / \mathrm{max}$ values $\mathrm{T}_{j}$ is the operating junction temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |

REGULATOR (Pin 8)

| Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {reg }}$ | 5.5 | 6.5 | 7.5 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V ) | Regline | - | 30 | 500 | mV |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 44 | 200 | mV |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {reg }}$ | 5.3 | - | 8.0 | V |

OSCILLATOR (Pin 7)

| Frequency | fosc |  |  |  | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$ |  |  |  |  |  |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}\left(\mathrm{V}_{C C}=20 \mathrm{~V}\right)$ |  | 260 | 285 | 310 |  |
| $\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V ) |  | 255 | - | 315 |  |
| $\mathrm{C}_{\mathrm{T}}=2.0 \mathrm{nF}$ |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}(\mathrm{V} \mathrm{CC}=20 \mathrm{~V})$ |  | 60 | 67.5 | 75 |  |
| $\mathrm{T}_{J}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to 40 V$)$ |  | 59 | - | 76 |  |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to 40 V ) | $\Delta \mathrm{f}_{\mathrm{Osc}} / \Delta \mathrm{V}$ | - | 0.1 | 2.0 | kHz |

ERROR AMPLIFIER (Pins 9, 10)

| Voltage Feedback Input Threshold | $\mathrm{V}_{\mathrm{FB}}$ | 2.52 | 2.6 | 2.68 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$ to $\left.40 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right)$ | Regline | - | 0.6 | 5.0 | mV |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{FB}}=2.6 \mathrm{~V}, \mathrm{~T}_{J}=0-125^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 20 | 500 | nA |
| Open Loop Voltage Gain $\left(\mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{A}_{\mathrm{VOL}}$ | 70 | 82 | 94 | dB |
| Gain Bandwidth Product $\left(\mathrm{f}=100 \mathrm{kHz}, \mathrm{T}_{\left.J=25^{\circ} \mathrm{C}\right)}\right.$ | GBW | 0.85 | 1.0 | 1.15 | MHz |
| Output Voltage Swing |  |  |  |  | V |
| High State $\left(\mathrm{I}_{\text {Source }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}<2.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ | 4.0 | 5.3 | - |  |
| Low State $\left(\mathrm{I}_{\text {Sink }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}>3.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 0.2 | 0.35 |  |

1. Maximum power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) $\quad\left(\mathrm{V}_{C C}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin }} 8=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{J}$ is the operating junction temperature range that applies, unless otherwise noted.)

| Characteristic |
| :--- |
| \begin{tabular}{\|l|c|c|c|c|c|c|}
\hline
\end{tabular} |
| $c \mid$ Symbol Min Typ Max Unit <br> Input Threshold Voltage $\mathrm{V}_{\mathrm{th}}$ 1.18 1.25 1.32 V <br> Input Bias Current $\left(\mathrm{V}_{\mathrm{BK}}<\mathrm{V}_{\mathrm{th}}, \mathrm{T}_{\mathrm{J}}=0-125^{\circ} \mathrm{C}\right)$ $\mathrm{I}_{\mathrm{IB}}$ - 100 500 nA <br> Source Current (Turn on after $\left.\mathrm{V}_{\mathrm{BK}}>\mathrm{V}_{\mathrm{th}}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}-125^{\circ} \mathrm{C}\right)$ $\mathrm{I}_{\mathrm{SC}}$ 39 - 53 $\mu \mathrm{~A}$ |

PWM COMPARATOR (Pins 7, 9)

| Duty Cycle |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum $\left(\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\max )}$ | 48 | 50 | 52 |  |
| Minimum $\left(\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\min )}$ | - | 0 | 0 |  |

POWER SWITCH (Pin 16)

| $\begin{aligned} & \text { Drain-Source On-State Resistance }\left(I_{\mathrm{D}}=200 \mathrm{~mA}\right) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-25^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{R}_{\mathrm{DS} \text { (on) }}$ | - | 15 | $\begin{aligned} & 17 \\ & 39 \end{aligned}$ | $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drain-Source Off-State Leakage Current $\mathrm{V}_{\mathrm{DS}}=650 \mathrm{~V}$ | $\mathrm{I}_{\mathrm{D} \text { (off) }}$ | - | 0.2 | 100 | $\mu \mathrm{A}$ |
| Rise Time | $t_{r}$ | - | 50 | - | ns |
| Fall Time | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | - | ns |

OVERCURRENT COMPARATOR (Pin 16)

| Current Limit Threshold $\left(R_{T}=10 \mathrm{k}\right)$ | $\mathrm{I}_{\mathrm{lim}}$ | 0.5 | 0.72 | 0.9 | A |
| :--- | :--- | :--- | :--- | :--- | :--- |

STARTUP CONTROL (Pin 1)

| Peak Startup Current ( $\left.\mathrm{V}_{\text {in }}=400 \mathrm{~V}\right)($ Note 2) | $\mathrm{I}_{\text {start }}$ |  |  |  | mA |
| :--- | :--- | :--- | :--- | :--- | :---: |
| $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{~V}_{\mathrm{CC}}=\left(\mathrm{V}_{\text {th(on) }}-0.2 \mathrm{~V}\right)$ |  | - | 2.0 | 4.0 |  |
| Off-State Leakage Current $\left(\mathrm{V}_{\text {in }}=50 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}\right)$ |  | - | 2.0 | 4.0 |  |

UNDERVOLTAGE LOCKOUT (Pin 3)

| Startup Threshold (VCC Increasing) | $\mathrm{V}_{\text {th(on) }}$ | 11 | 15.2 | 18 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On | $\mathrm{V}_{\mathrm{CC}(\min )}$ | 7.5 | 9.5 | 11.5 | V |

TOTAL DEVICE (Pin 3)

| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Startup (VCC $=10 \mathrm{~V}$, Pin 1 Open) |  | - | 0.25 | 0.5 | mA |
| Operating |  | - | 3.2 | 5.0 |  |

2. The device can only guarantee to start up at high temperature below $+115^{\circ} \mathrm{C}$.


Figure 2. Oscillator Frequency versus Timing Resistor


Figure 3. Power Switch Peak Drain Current versus Timing Resistor


Figure 4. Oscillator Charge/Discharge Current versus Timing Resistor


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 8. Error Amplifier Small Signal
Transient Response


Figure 5. Maximum Output Duty Cycle versus Timing Resistor Ratio


Figure 7. Error Amp Output Saturation Voltage versus Load Current

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 9. Error Amplifier Large Signal Transient Response


Figure 10. Regulator Output Voltage Change versus Source Current


Figure 12. Power Switch Drain-Source On-Resistance versus Temperature


Figure 14. Supply Current versus Supply Voltage


Figure 11. Peak Startup Current versus Power Supply Voltage


Figure 13. Power Switch Drain-Source Capacitance versus Voltage


Figure 15. P Suffix Transient Thermal Resistance


Figure 16. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

PIN FUNCTION DESCRIPTION

| Pin | Function | Description |
| :---: | :---: | :---: |
| 1 | Startup Input | This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the $\mathrm{V}_{\mathrm{CC}}$ pin to ground. |
| 2 | - | This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the $\mathrm{V}_{\mathrm{CC}}$ potential on Pin 3. |
| 3 | $\mathrm{V}_{\mathrm{CC}}$ | This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding. |
| 4, 5, 12, 13 | Gnd | These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board. |
| 6 | $\mathrm{R}_{\mathrm{T}}$ | Resistor $\mathrm{R}_{\mathrm{T}}$ connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency. |
| 7 | $\mathrm{C}_{\text {T }}$ | Capacitor $\mathrm{C}_{\mathrm{T}}$ connects from this pin to ground. The value selected, in conjunction with resistor $\mathrm{R}_{\mathrm{T}}$, programs the Oscillator frequency. |
| 8 | Regulator Output | This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability. |
| 9 | Compensation | This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator. |
| 10 | Voltage Feedback Input | This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 11 | BOK | This is the non-inverting input of the bulk capacitor voltage comparator. It has an input threshold voltage of 1.25 V . This pin is connected through a resistor divider to the bulk capacitor line voltage. |
| 14, 15 | - | These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13. |
| 16 | Power Switch Drain | This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . |



Figure 17. Representative Block Diagram


Figure 18. Timing Diagram

## OPERATING DESCRIPTION

## Introduction

The MC33365 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 17 and 18.

## Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Resistor $\mathrm{R}_{\mathrm{T}}$ programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 4. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz . The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50\% limit by providing an additional charge or discharge current path to $\mathrm{C}_{\mathrm{T}}$, Figure 19. In order to increase the maximum duty cycle, a discharge current resistor $R_{D}$ is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor $\mathrm{R}_{\mathrm{C}}$ is connected from Pin 7 to the Regulator Output. Figure 5 shows an obtainable range of maximum output duty cycle versus the ratio of either $\mathrm{R}_{\mathrm{C}}$ or $\mathrm{R}_{\mathrm{D}}$ with respect to $\mathrm{R}_{\mathrm{T}}$.


Figure 19. Maximum Duty Cycle Modification

The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for $\mathrm{C}_{\mathrm{T}}$ values greater than 500 pF . For smaller values of $\mathrm{C}_{\mathrm{T}}$, refer to Figure 2. Note that resistor $\mathrm{R}_{\mathrm{T}}$ also programs the Current Limit Comparator threshold.

$$
\mathrm{I}_{\mathrm{chg}} / \mathrm{dscg}=\frac{5.4}{\mathrm{RT}^{2}} \quad \mathrm{f} \approx \frac{\mathrm{I}_{\mathrm{chg}} / \mathrm{dscg}}{4 \mathrm{C}_{\top}}
$$

## PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non-inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while $\mathrm{C}_{\mathrm{T}}$ is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When $\mathrm{C}_{\mathrm{T}}$ charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp-up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 18 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

## Current Limit Comparator and Power Switch

The MC33365 uses cycle-by-cycle current limiting as a means of protecting the output power switch from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The Power Switch is constructed as a SENSEFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 1462 cells, of which 36 are connected to a $8.1 \Omega$ ground-referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the $405 \Omega$ resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor $\mathrm{R}_{\mathrm{T}}$. Therefore when selecting the values for $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}, \mathrm{R}_{\mathrm{T}}$ must be chosen first to set the Power Switch peak drain current, while $\mathrm{C}_{\mathrm{T}}$ is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus $\mathrm{R}_{\mathrm{T}}$ is shown in Figure 3 with the related formula below.

$$
\mathrm{I}_{\mathrm{pk}}=8.8\left(\frac{\mathrm{R}_{\mathrm{T}}}{1000}\right)-1.077
$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A . Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn-on transition is completed. The current limit propagation delay time is typically 262 ns . This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn-off.

## Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 17. It features a typical dc voltage gain of 82 dB , and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 6. The noninverting input is internally biased at $2.6 \mathrm{~V} \pm 3.1 \%$ and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of $270 \mu \mathrm{~A}$, allowing it to be easily overridden with a pull-up resistor. This is desirable in applications that require secondary side voltage sensing.

## Bulk Capacitor Voltage Comparator

In order to avoid output voltage bouncing during electricity brownout condition, a Bulk Capacitor Voltage Comparator with programmable hysteresis is included in this device. The non-inverting input, pin 11, is connected to the voltage divider comprised of $\mathrm{R}_{\text {Upper }}$ and $\mathrm{R}_{\text {Lower }}$ as shown in Figure 20 monitoring the bulk capacitor voltage level. The inverting input is connected to a threshold voltage of 1.25 V internally. As bulk capacitor voltage drops below the pre-programmed level, (Pin 11 drops below 1.25 V ), a reset signal will be generated via internal protection logic to the PWM Latch so turning off the Power Switch immediately. An internal current source controlled by the state of the comparator provides a means to program the voltage hysteresis. The following equation shows the relationship between $V_{\text {BULK }}$ levels and the voltage divider network resistors.

$$
\begin{aligned}
& \text { RUpper }=20 \times\left[\text { VBulk_H }-V_{\text {Bulk_L }}\right] \quad \text { in K Ohm } \\
& \text { RLower }=\frac{25 \times\left[\text { VBulk_H }-V_{\text {Bulk_L }}\right]}{V_{\text {Bulk_H }}-1.25} \quad \text { in K Ohm }
\end{aligned}
$$



Figure 20. Bulk OK Functional Operation

## Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the $\mathrm{V}_{\mathrm{CC}}$ voltage at Pin 3 and when it exceeds 14.5 V , the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

## Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33365. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off-line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor that connects from Pin 3 to ground. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold of 15.2 V , the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide a steady current of 1.7 mA , Figure 11, as $\mathrm{V}_{\mathrm{CC}}$ increases or shorted to ground. The startup MOSFET is rated at a maximum of 400 V with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground, and 500 V when charging a $\mathrm{V}_{\mathrm{CC}}$ capacitor of $1000 \mu \mathrm{~F}$ or less.

## Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has
short-circuit protection. This output requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability.

## Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at $150^{\circ} \mathrm{C}$, the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below $140^{\circ} \mathrm{C}$. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33365 is contained in a heatsinkable plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figure 16 shows a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

## MC33362

## High Voltage Switching Regulator

The MC33362 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 120 VAC line source. This integrated circuit features an on-chip $500 \mathrm{~V} / 2.0 \mathrm{~A}$ SenseFET power switch, 250 V active off-line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16-lead dual-in-line and wide body surface mount packages.

- On-Chip 500 V, 2.0 A SenseFET Power Switch
- Rectified 120 VAC Line Source Operation
- On-Chip 250 V Active Off-Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle-By-Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown


This device contains 221 active transistors.
Figure 1. Simplified Application

## MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Switch (Pin 16) <br> Drain Voltage <br> Drain Current | $\begin{aligned} & \mathrm{V}_{\mathrm{DS}} \\ & \mathrm{I}_{\mathrm{DS}} \end{aligned}$ | $\begin{gathered} 500 \\ 2.0 \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { A } \end{aligned}$ |
| Startup Input Voltage (Pin 1, Note 2) $\text { Pin } 3=\text { Gnd }$ <br> Pin $3 \leq 1000 \mu \mathrm{~F}$ to ground | $V_{\text {in }}$ | $\begin{aligned} & 250 \\ & 400 \end{aligned}$ | V |
| Power Supply Voltage (Pin 3) | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| ```Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Overvoltage Protection Input (Pin 11) RT(Pin 6) CT(Pin 7)``` | $\mathrm{V}_{\text {IR }}$ | -1.0 to $\mathrm{V}_{\text {reg }}$ | V |
| Thermal Characteristics <br> P Suffix, Dual-In-Line Case 648E <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> (Pins 4, 5, 12, 13) <br> DW Suffix, Surface Mount Case 751N <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> (Pins 4, 5, 12, 13) <br> Refer to Figures 16 and 17 for additional thermal information. | $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJc }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJc }}$ | $\begin{aligned} & 80 \\ & 15 \\ & \\ & 95 \\ & 15 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -25 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\mathrm{Pin} 8}=1.0 \mu \mathrm{~F}$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$,
for min/max values $T_{J}$ is the operating junction temperature range that applies (Note 3), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REGULATOR (Pin 8) |  |  |  |  |  |
| Output Voltage ( $\mathrm{I}_{0}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {reg }}$ | 5.5 | 6.5 | 7.5 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to 40 V ) | Regline | - | 30 | 500 | mV |
| Load Regulation ( $\mathrm{I}_{0}=0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 44 | 200 | mV |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {reg }}$ | 5.3 | - | 8.0 | V |

OSCILLATOR (Pin 7)


1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
2. Maximum power dissipation limits must be observed.
3. Tested junction temperature range for the MC33362:

$$
\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C} \quad \mathrm{~T}_{\text {high }}=+125^{\circ} \mathrm{C}
$$

## MC33362

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}, \mathrm{C}_{\text {Pin } 8}=1.0 \mu \mathrm{~F}\right.$, for typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min/max values $T_{J}$ is the operating junction temperature range that applies (Note 4), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER (Pins 9, 10) |  |  |  |  |  |
| Voltage Feedback Input Threshold | $\mathrm{V}_{\mathrm{FB}}$ | 2.52 | 2.6 | 2.68 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | Regline | - | 0.6 | 5.0 | mV |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB}}=2.6 \mathrm{~V}$ ) | IIB | - | 20 | 500 | nA |
| Open Loop Voltage Gain ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $A_{\text {VOL }}$ | - | 82 | - | dB |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | GBW | - | 1.0 | - | MHz |
| Output Voltage Swing <br> High State ( ${ }_{\text {source }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}<2.0 \mathrm{~V}$ ) <br> Low State ( $\mathrm{I}_{\text {Sink }}=100 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}>3.0 \mathrm{~V}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $4.0$ | $\begin{aligned} & 5.3 \\ & 0.2 \end{aligned}$ | $\stackrel{-}{0.35}$ | V |

## OVERVOLTAGE DETECTION (Pin 11)

| Input Threshold Voltage | $\mathrm{V}_{\text {th }}$ | 2.47 | 2.6 | 2.73 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\text {in }}=2.6 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 100 | 500 | nA |

PWM COMPARATOR (Pins 7, 9)

| Duty Cycle |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum $\left(\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\max )}$ | 48 | 50 | 52 | $\%$ |
| Minimum $\left(\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\min )}$ | - | 0 | 0 |  |

POWER SWITCH (Pin 16)

| Drain-Source On-State Resistance $\left(\mathrm{I}_{\mathrm{D}}=200 \mathrm{~mA}\right)$ | $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ |  |  |  | $\Omega$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | - | 4.4 | 6.0 |  |
| $\mathrm{~T}_{J}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ |  | - | - | 12 |  |
| Drain-Source Off-State Leakage Current $\left(\mathrm{V}_{\mathrm{DS}}=500 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{D}(\text { off })}$ | - | 0.2 | 50 | $\mu \mathrm{~A}$ |
| Rise Time | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | - | ns |
| Fall Time | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | - | ns |

OVERCURRENT COMPARATOR (Pin 16)

| Current Limit Threshold $\left(R_{\mathrm{T}}=10 \mathrm{k}\right)$ | $\lim _{\text {lim }}$ | 0.7 | 0.9 | 1.1 | A |
| :--- | :--- | :--- | :--- | :--- | :--- |

STARTUP CONTROL (Pin 1)

| Peak Startup Current $\left(\mathrm{V}_{\text {in }}=200 \mathrm{~V}\right)$ <br> $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ <br> $\mathrm{~V}_{\mathrm{CC}}=\left(\mathrm{V}_{\text {th }(\text { on })}-0.2 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {start }}$ |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Off-State Leakage Current $\left(\mathrm{V}_{\text {in }}=50 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}\right)$ |  | - | 55 | - |  |

UNDERVOLTAGE LOCKOUT (Pin 3)

| Startup Threshold (VCC Increasing) | $\mathrm{V}_{\mathrm{th}(\mathrm{on})}$ | 11 | 14.5 | 18 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On | $\mathrm{V}_{\mathrm{CC}(\min )}$ | 7.5 | 9.5 | 11.5 | V |

TOTAL DEVICE (Pin 3)

| Power Supply Current | $I_{C C}$ |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| Startup (VA |  |  |  |  |
| Operating | 10 V, Pin 1 Open) |  | - | 0.3 |

4. Tested junction temperature range for the MC33362:

$$
\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C} \quad \mathrm{~T}_{\text {high }}=+125^{\circ} \mathrm{C}
$$



Figure 2. Oscillator Frequency versus Timing Resistor


Figure 4. Oscillator Charge/Discharge Current versus Timing Resistor


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency


Figure 3. Power Switch Peak Drain Current versus Timing Resistor


Figure 5. Maximum Output Duty Cycle versus Timing Resistor Ratio


Figure 7. Error Amp Output Saturation Voltage versus Load Current

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 8. Error Amplifier Small Signal Transient Response


Figure 10. Regulator Output Voltage Change versus Source Current


Figure 12. Power Switch Drain-Source On-Resistance versus Temperature

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 9. Error Amplifier Large Signal Transient Response


Figure 11. Peak Startup Current versus Power Supply Voltage


Figure 13. Power Switch Drain-Source Capacitance versus Voltage


Figure 14. Supply Current versus Supply Voltage


Figure 15. DW and P Suffix Transient Thermal Resistance


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

PIN FUNCTION DESCRIPTION

| Pin | Function | Description |
| :---: | :---: | :---: |
| 1 | Startup Input | This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the $\mathrm{V}_{\mathrm{CC}}$ pin to ground. |
| 2 | - | This pin has been omitted for increased spacing between the rectified AC line voltage on Pin 1 and the $\mathrm{V}_{\mathrm{CC}}$ potential on Pin 3. |
| 3 | $\mathrm{V}_{C C}$ | This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding. |
| 4, 5, 12, 13 | Ground | These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board. |
| 6 | $\mathrm{R}_{\mathrm{T}}$ | Resistor $\mathrm{R}_{\mathrm{T}}$ connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency. |
| 7 | $\mathrm{C}_{\text {T }}$ | Capacitor $\mathrm{C}_{\mathrm{T}}$ connects from this pin to ground. The value selected, in conjunction with resistor $\mathrm{R}_{\mathrm{T}}$, programs the Oscillator frequency. |
| 8 | Regulator Output | This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability. |
| 9 | Compensation | This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator. |
| 10 | Voltage Feedback Input | This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 11 | Overvoltage Protection Input | This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output. |
| 14, 15 | - | These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13. |
| 16 | Power Switch Drain | This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 500 V and 2.0 A . |



Figure 18. Representative Block Diagram


Figure 19. Timing Diagram

## OPERATING DESCRIPTION

## Introduction

The MC33362 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 120 VAC line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 18 and 19.

## Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Resistor $\mathrm{R}_{\mathrm{T}}$ programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 4. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz . The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50\% limit by providing an additional charge or discharge current path to $\mathrm{C}_{\mathrm{T}}$, Figure 20. In order to increase the maximum duty cycle, a discharge current resistor $R_{D}$ is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor $\mathrm{R}_{\mathrm{C}}$ is connected from Pin 7 to the Regulator Output. Figure 5 shows an obtainable range of maximum output duty cycle versus the ratio of either $R_{C}$ or $R_{D}$ with respect to $R_{T}$.


Figure 20. Maximum Duty Cycle Modification

The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for $\mathrm{C}_{\mathrm{T}}$ values greater than 500 pF . For smaller values of $\mathrm{C}_{\mathrm{T}}$, refer to Figure 2. Note that resistor $\mathrm{R}_{\mathrm{T}}$ also programs the Current Limit Comparator threshold.

$$
\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}=\frac{5.4}{\mathrm{R}_{\mathrm{T}}} \quad \mathrm{f} \approx \frac{\mathrm{I}_{\mathrm{chg} / \mathrm{dscg}}}{4 \mathrm{C}_{\mathrm{T}}}
$$

## PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non-inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while $\mathrm{C}_{\mathrm{T}}$ is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When $\mathrm{C}_{\mathrm{T}}$ charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp-up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 19 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

## Current Limit Comparator and Power Switch

The MC33362 uses cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 3770 cells, of which 50 are connected to a $9.0 \Omega$ ground-referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the $450 \Omega$ resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor $\mathrm{R}_{\mathrm{T}}$. Therefore when selecting the values for $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}, \mathrm{R}_{\mathrm{T}}$ must be chosen first to set the Power Switch peak drain current, while $C_{T}$ is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus $\mathrm{R}_{\mathrm{T}}$ is shown in Figure 3 with the related formula below.

$$
\mathrm{I}_{\mathrm{pk}}=12.3\left(\frac{\mathrm{R}_{\mathrm{T}}}{1000}\right)^{-1.115}
$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 500 V and 2.0 A . Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn-on transition is completed. The current limit propagation delay time is typically 233 ns . This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn-off.

## Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 18. It features a typical dc voltage gain of 82 dB , and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 6. The noninverting input is internally biased at $2.6 \mathrm{~V} \pm 3.1 \%$ and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of $270 \mu \mathrm{~A}$, allowing it to be easily overridden with a pull-up resistor. This is desirable in applications that require secondary side voltage sensing, Figure 21. In this application, the Voltage Feedback Input is connected to the Regulator Output. This disables the Error Amplifier by placing its output into the sink state, allowing the optocoupler transistor to directly control the PWM Comparator.

## Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side $\mathrm{V}_{\mathrm{CC}}$ voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

## Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the $\mathrm{V}_{\mathrm{CC}}$ voltage at Pin 3 and when it exceeds 14.5 V , the reset signal is removed from the PWM Latch allowing operation of the

Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

## Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33362. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off-line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor that connects from Pin 3 to ground. When $\mathrm{V}_{\mathrm{CC}}$ reaches the UVLO upper threshold of 14.5 V , the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide an initial peak current of 55 mA , Figure 11, which decreases rapidly as $\mathrm{V}_{\mathrm{CC}}$ and the die temperature rise. The steady state current will self limit in the range of 12 mA with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground. The startup MOSFET is rated at a maximum of 250 V with $\mathrm{V}_{\mathrm{CC}}$ shorted to ground, and 400 V when charging a $\mathrm{V}_{\mathrm{CC}}$ capacitor of $1000 \mu \mathrm{~F}$ or less.

## Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short-circuit protection. This output requires an external bypass capacitor of at least $1.0 \mu \mathrm{~F}$ for stability.

## Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at $155^{\circ} \mathrm{C}$, the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below $145^{\circ} \mathrm{C}$. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33362 is contained in a heatsinkable plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper. Figure 23 shows a practical example of a printed circuit board layout
that utilizes the copper foil as a heat dissipater. Note that a jumper was added to the layout from Pins 8 to 10 in order to enhance the copper area near the device for improved thermal
conductivity. The application circuit requires two ounce copper foil in order to obtain 20 watts of continuous output power at room temperature.


Figure 21. 20 W Off-Line Converter

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=92 \mathrm{Vac}$ to $138 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}} 4.0 \mathrm{~A}$ | $\Delta=1.0 \mathrm{mV}$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ to 4.0 A | $\Delta=9.0 \mathrm{mV}$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=4.0 \mathrm{~A}$ | Triangular $=10 \mathrm{mVpp}$ <br> Spike $=60 \mathrm{mVpp}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\mathrm{O}}=4.0 \mathrm{~A}$ | $78.4 \%$ |

This data was taken with the components listed below mounted on the printed circuit board shown in Figure 23. For high efficiency and small circuit board size, the Sanyo Os-Con capacitors are recommended for C8, C9, C10 and C11. C8, C9, C10 = Sanyo Os-Con \#6SA330M, $330 \mu \mathrm{~F} 6.3 \mathrm{~V}$.
C11 = Sanyo Os-Con \#10SA220M, $220 \mu \mathrm{~F} 10 \mathrm{~V}$.
D7 = MBR2515L mounted on Aavid \#592502B03400 heatsink.
L1 = Coilcraft S5088-A, $5.0 \mu \mathrm{H}, 0.11 \Omega$.
T1 = Coilcraft S5069-A
Primary: 58 turns of \# 26 AWG, Pin $1=$ start, Pin $8=$ finish.
Two layers 0.002" Mylar tape.
Secondary: 4 turns of \# 18 AWG, 2 strands bifiliar wound, Pin $5=$ start, Pin $4=$ finish.
Two layers $0.002^{\prime \prime}$ Mylar tape.
Auxiliary: 10 turns of \# 26 AWG wound in center of bobbin, Pin $2=$ start, Pin $7=$ finish.
Two layers 0.002" Mylar tape.
Gap: $0.014^{\prime \prime}$ total for a primary inductance ( $L_{P}$ ) of $330 \mu \mathrm{H}$.
Core and Bobbin: Coilcraft PT1950, E187, 3F3 material.
Figure 22. Converter Test Data


Figure 23. Printed Circuit Board and Component Layout (Circuit of Figure 21)

## NCP1000, NCP1001, NCP1002

## Integrated Off-Line Switching Regulator

The NCP1000 through NCP1002 series of integrated switching regulators, combine a fixed frequency PWM controller with an integrated high voltage power switch circuit. This chip allows for simple design and minimal parts count for very low cost applications which utilize an ac input. This chip is designed to power a single ended topology, typically a discontinuous mode flyback, with secondary side sensing.

The internal high voltage switch circuit and start-up circuit can function in continuous operation over a wide range of inputs, from 85 Vac to 265 Vac , and thus can be used in any existing power system in the world. Though inexpensive, these devices include a number of features such as undervoltage lockout, over-temperature protection, bandgap reference and leading edge blanking that make them an excellent value.

## Features

- Highly Integrated Solution
- Operates Over Universal Input Voltage Range (85 Vac to 265 Vac )
- On-board 700 Volt Power Switch Circuit
- Minimal External Parts Required
- Input Undervoltage Lockout with Hysteresis
- Very Low Standby Current
- No Minimum Load Requirement
- Opto Fail-safe Shutdown Circuit


## Typical Applications

- Cell Phone Chargers
- Wall Adapters
- On-board AC-DC Converters


Figure 1. Simplified Block Diagram


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http://onsemi.com


| ORDERING INFORMATION* |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Device Package Shipping Ipk <br> Typ <br> $(A)$ Ron <br> Max <br> $(\Omega)$ <br> NCP1000P DIP-8 50 Units/Rail 0.5 18 <br> NCP1001P DIP-8 50 Units/Rail 1.0 9 <br> NCP1002P DIP-8 50 Units/Rail 1.5 6 <br> NCP1000T TO-220 50 Units/Rail 0.5 18 <br> NCP1001T TO-220 50 Units/Rail 1.0 9 <br> NCP1002T TO-220 50 Units/Rail 1.5 6 |  |  |  |  |  |

*Consult factory for additional optocoupler fail-safe latching, frequency, and current limit options.

## NCP1000, NCP1001, NCP1002

## Functional Pin Description

| Pin <br> (DIP-8) | Pin <br> (TO-220) | Function | Description |
| :---: | :---: | :---: | :--- |$|$| (T |
| :--- |
| 1 |

MAXIMUM RATINGS (Notes 1 and 2)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Switch Circuit (Pin 5) <br> Drain Voltage Range <br> Drain Current Peak During Transformer Saturation | $V_{D S}$ $l_{\mathrm{DS}(\mathrm{pk})}$ | $\begin{aligned} & -0.3 \text { to } 700 \\ & 2.0 \mathrm{I}_{\text {lim }} \operatorname{Max} \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { A } \end{aligned}$ |
| Power Supply Voltage Range (Pin 1) | $\mathrm{V}_{\text {clp }}$ | -0.3 to 10 | V |
| Feedback Input (Pin 2) <br> Voltage Range Current | $\underset{\substack{(f b) \\ \mathrm{I}_{\mathrm{fb}}}}{\mathrm{~V}^{2}}$ | $\begin{gathered} -0.3 \text { to } 10 \\ 100 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| ```Thermal Resistance P Suffix, Plastic Package Case 626 Junction to Lead Junction to Air, 2.0 Oz. Printed Circuit Copper Clad 0.36 Sq. Inch 1.0 Sq. Inch T Suffix, Plastic Package Case 314D Junction to Case Junction to Air``` | $\mathrm{R}_{\text {өJL }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 5.0 \\ & 45 \\ & 35 \\ & \\ & 2.0 \\ & 65 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -40 to 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Pins 1-3: Human Body Model 4000 V per MIL-STD-883, Method 3015.
Machine Model Method 400 V .
Pins 4, 5: Human Body Model 1000 V per MIL-STD-883, Method 3015. Machine Model Method 400 V .
Pins 4 and 5 are the HV start-up and the drain of the LDMOS device, rated only to the max rating of the part , or 700 V .
2. This device contains Latch-up protection and exceeds $\pm 200 \mathrm{~mA}$ per JEDEC Standard JESD78.

## NCP1000, NCP1001, NCP1002

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=8.6\right.$ volts, pin 2 grounded, $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ for typical values. For min/max values, $\mathrm{T}_{\mathrm{J}}$ is the operating junction temperature that applies.)

| Characteristics |
| :--- |
|  Symbol Min Typ Max Unit <br> OSCILLATOR fosc     <br> Frequency (lfb $=1.5 \mathrm{~mA}$ ) (Note 4) (Figure 7)  90 100 110 kHz <br> $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$      <br> $\mathrm{T}_{J}=0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$  85 - 115  <br> $\mathrm{~T}_{J}=-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$  75 - 115  |

PWM COMPARATOR

| Feedback Input PWM Gain $\left(T_{J}=25^{\circ} \mathrm{C}\right)\left(\mathrm{l}_{\mathrm{fb}}=1.10 \mathrm{~mA}\right.$ to 1.20 mA$)$ (Figure 2) Gain Temperature Coefficient $\left(\mathrm{T}_{J}=-40^{\circ} \mathrm{C}\right.$ to $\left.\mathrm{T}_{J}=125^{\circ} \mathrm{C}\right)$ (Note 4) | $\begin{gathered} A_{v} \\ \Delta A_{v} \end{gathered}$ | $-110$ | $\begin{gathered} -136 \\ 0.2 \end{gathered}$ | $-170$ | $\begin{gathered} \% / \mathrm{mA} \\ (\% / \mathrm{mA}) /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PWM Duty Cycle (Pin 2) Maximum ( $\mathrm{l}_{\mathrm{fb}}=0 \mathrm{~mA}$ ) Zero Duty Cycle Current | $\underset{\mathrm{I}_{\mathrm{fb}}}{\mathrm{I}_{(\max )}}$ | $\begin{aligned} & 68 \\ & 1.8 \end{aligned}$ | 72 | 74 | $\begin{gathered} \% \\ \mathrm{~mA} \end{gathered}$ |
| PWM Ramp <br> Peak <br> Valley | $\begin{aligned} & V_{\text {rpk }} \\ & V_{\text {ruly }} \end{aligned}$ | - | $\begin{aligned} & 4.1 \\ & 2.7 \end{aligned}$ |  | V |

START-UP CONTROL AND $\mathrm{V}_{\mathrm{Cc}}$ LIMITER

| Undervoltage Lockout (Figure 8) <br> $V_{c c}$ Clamp Voltage ( $\mathrm{I}_{\mathrm{CC}}=4.0 \mathrm{~mA}$ ) Start-Up Threshold (V ${ }_{\text {clp }}$ Increasing) Minimum Operating Voltage After Turn-On Hysteresis | $\mathrm{V}_{\mathrm{clp}}$ <br> $V_{\text {clp(on) }}$ <br> $\underset{\mathrm{V}_{\mathrm{Clp}(\text { min })}}{\mathrm{V}_{\mathrm{H}}}$ | $\begin{aligned} & 8.3 \\ & 8.2 \\ & 7.2 \end{aligned}$ | $\begin{gathered} 8.55 \\ 8.5 \\ 7.5 \\ 1.0 \end{gathered}$ | $\begin{aligned} & 8.9 \\ & 8.8 \\ & 8.0 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Start-Up Circuit, Pin 1 Output Current (Pin $4=50$ V) $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=8.0 \mathrm{~V} \end{aligned}$ | $\mathrm{I}_{\text {start }}$ | $\begin{aligned} & 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 3.4 \\ & 2.6 \end{aligned}$ | $\begin{aligned} & 4.2 \\ & 4.2 \end{aligned}$ | mA |
| Auto Restart ( $\mathrm{C}_{\text {Pin } 1}=47 \mu \mathrm{~F}$, Pin $4=50 \mathrm{~V}$ ) (Note 5) Duty Cycle Frequency | $\begin{aligned} & D_{\mathrm{rst}} \\ & \mathrm{f}_{\mathrm{rst}} \end{aligned}$ |  | $\begin{aligned} & 5.0 \\ & 1.2 \end{aligned}$ | 6.0 | $\begin{gathered} \% \\ \mathrm{~Hz} \end{gathered}$ |
| Start-Up Circuit Breakdown Voltage ( $1=2 \mu \mathrm{~A}$ ) (Note 5) | $\mathrm{V}_{\mathrm{BR} \text { (st) }}$ | 700 | - | - | V |
| $\begin{aligned} & \text { Start-Up Circuit Leakage Current (Pin } \left.4=700 \mathrm{~V}_{\mathrm{DC}}\right) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C} \end{aligned}$ | $l_{\text {leak }}$ |  | $\begin{aligned} & 20 \\ & 30 \end{aligned}$ | $\begin{aligned} & 40 \\ & 75 \end{aligned}$ | $\mu \mathrm{A}$ |

3. Maximum package power dissipation limits must be observed.
4. Tested junction temperature range for this device series: $T_{\text {low }}=-40^{\circ} \mathrm{C}, T_{\text {high }}=+125^{\circ} \mathrm{C}$
5. Guaranteed by design only.

## ELECTRICAL CHARACTERISTICS

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| POWER SWITCH CIRCUIT |  |  |  |  |  |
| Power Switch Circuit On-State Resistance NCP1000 ( $\mathrm{l}_{\mathrm{D}}=50 \mathrm{~mA}$ ) $\begin{aligned} & T_{J}=25^{\circ} \mathrm{C} \\ & T_{J}=125^{\circ} \mathrm{C} \text { (Note 8) } \end{aligned}$ <br> NCP1001 ( $\mathrm{I}_{\mathrm{D}}=100 \mathrm{~mA}$ ) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=125^{\circ} \mathrm{C} \text { (Note 8) } \end{aligned}$ <br> NCP1002 ( $\mathrm{I}_{\mathrm{D}}=150 \mathrm{~mA}$ ) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=125^{\circ} \mathrm{C} \text { (Note } 8 \text { ) } \end{aligned}$ | $\mathrm{R}_{\text {(on) }}$ | - - - - - - | $\begin{aligned} & 13 \\ & 24 \\ & \\ & 7.0 \\ & 14 \\ & \\ & 4.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 18 \\ & 36 \\ & \\ & 9.0 \\ & 18 \\ & \\ & 6.0 \\ & 12 \end{aligned}$ | $\Omega$ |
| Power Switch Circuit Breakdown Voltage ( $\mathrm{I}_{\mathrm{D} \text { (off) }}=100 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {(BR) }}$ | 700 | - | - | V |
| Power Switch Circuit Off-State Leakage Current (VDS $=700 \mathrm{~V}$ ) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C} \end{aligned}$ | ${ }^{\text {(off) }}$ | - | 0.25 | $\begin{aligned} & 1.0 \\ & 100 \end{aligned}$ | $\mu \mathrm{A}$ |
| ```Switching Characteristics ( \(\mathrm{V}_{\mathrm{DS}}=50 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}\) set for \(\mathrm{I}_{\mathrm{D}}=0.7 \mathrm{I}_{\text {lim }}\) ) Turn-on Time (90\% to 10\%) Turn-off Time ( \(10 \%\) to \(90 \%\) )``` | $\begin{aligned} & \mathrm{t}_{\mathrm{on}} \\ & \mathrm{t}_{\text {off }} \end{aligned}$ | - | 50 50 | - | ns |

CURRENT LIMIT AND THERMAL PROTECTION

| Current Limit Threshold ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) (Note 9) <br> NCP1000 <br> NCP1001 <br> NCP1002 | $l_{\text {lim }}$ | $\begin{aligned} & 0.42 \\ & 0.84 \\ & 1.26 \end{aligned}$ | $\begin{aligned} & 0.48 \\ & 0.96 \\ & 1.43 \end{aligned}$ | $\begin{gathered} 0.54 \\ 1.08 \\ 1.6 \end{gathered}$ | A |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Limit, Peak Switch Current NCP1000 (di/dt = $100 \mathrm{~mA} / \mu \mathrm{s}$ ) <br> NCP1001 ( $\mathrm{di} / \mathrm{dt}=200 \mathrm{~mA} / \mu \mathrm{s}$ ) <br> NCP1002 (di/dt = $300 \mathrm{~mA} / \mu \mathrm{s}$ ) | 1 lpk | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 0.500 \\ & 1.000 \\ & 1.500 \end{aligned}$ | - | A |
| Opto Fail-safe Protection (Figure 12) $\begin{aligned} & T_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=0^{\circ} \mathrm{C} \text { to } 125^{\circ} \mathrm{C} \end{aligned}$ | ${ }^{\text {Ofail }}$ | $10$ |  | $\begin{aligned} & 25 \\ & 35 \end{aligned}$ | mA |
| Propagation Delay, Current Limit Threshold to Power Switch Circuit Output (Leading Edge Blanking plus Current Limit Delay) | $t_{\text {PLH }}$ | - | 220 | - | ns |
| Thermal Protection (Note 6, 8) Shutdown (Junction Temperature Increasing) Hysteresis (Junction Temperature Decreasing) | $\begin{aligned} & \mathrm{t}_{\mathrm{sd}} \\ & \mathrm{t}_{\mathrm{H}} \end{aligned}$ | 125 | $\begin{gathered} 140 \\ 30 \end{gathered}$ | - | ${ }^{\circ} \mathrm{C}$ |

TOTAL DEVICE (Pin 1)

| Power Supply Current After UVLO Turn-On |  |  |  |
| :--- | :--- | :--- | :--- |
| Power Switch Circuit Enabled | $I_{C C 1}$ |  |  |
| NCP1000 |  | - | 1.2 |
| NCP1001 |  | 1.6 |  |
| NCP1002 |  | - | 1.4 |
| Power Switch Circuit Disabled | $I_{\text {CC2 }}$ | 0.8 | 1.6 |

6. Maximum package power dissipation limits must be observed.
7. Tested junction temperature range for this device series:
$\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} \quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
8. Guaranteed by design only.
9. Actual peak switch current is increased due to the propagation delay time and the di/dt (see Figure 16).


Figure 2. Duty Cycle vs. FB Input Current


Figure 4. Charge Time vs. $\mathrm{V}_{\mathrm{CC}}$ Capacitance


Figure 3. $\mathrm{I}_{\mathrm{Cc}}$ vs. $\mathrm{V}_{\mathrm{CC}}$


Figure 5. Startup Current vs. Startup Voltage


Figure 6. Power Switch Circuit Capacitance vs. Voltage


Figure 7. Oscillator Frequency vs. Temperature

## NCP1000, NCP1001, NCP1002



Figure 8. $\mathrm{V}_{\mathrm{CC}} / \mathrm{UVLO}$ Threshold vs.
Temperature


Figure 10. Power Switch Circuit On Resistance vs. Temperature


Figure 12. Opto Fail-safe Trigger Current vs. Temperature


Figure 9. Peak Current Limit Threshold vs. Temperature


Figure 11. Power Switch Circuit Leakage Current vs. Pin 5 Voltage


Figure 13. Zero Duty Cycle Feedback Current vs. Temperature


Figure 14. Maximum Duty Cycle Feedback Current vs. Temperature


Figure 15. On Resistance vs. Current


Figure 16. Power Switch Circuit di/dt vs. $\Delta$ lpk

## OPERATING DESCRIPTION

## Introduction

The NCP1000 thru NCP1002 represent a new higher level of integration by providing on a single monolithic chip all of the active power, control, logic, and protection circuitry required to implement a high voltage flyback or forward converter. This device series is designed for direct operation from a rectified 240 VAC line source and requires minimal external components for a complete cost sensitive converter solution. Potential markets include office automation, industrial, residential, personal computer, and consumer. A description of each of the functional blocks is given below, and the representative block diagram is shown in Figure 17.

## Oscillator

The Oscillator block consists of two comparators that alternately gate on and off a trimmed current source and current sink which are used to respectively charge and discharge an on-chip timing capacitor between two voltage levels. This configuration generates a precise linear sawtooth ramp signal that is used to pulse width modulate the MOSFET of the Power Switch circuit. During the charge of the timing capacitor, the Oscillator duty cycle output holds one input of the Driver low. This action keeps the MOSFET of the Power Switch Circuit off, thus limiting the maximum duty cycle. The Oscillator frequency is internally programmed for 100 kHz operation with a controlled charge to discharge current ratio that yields a maximum Power Switch Circuit duty cycle of $72 \%$. The Oscillator temperature characteristics are shown in Figure 7.

## PWM Comparator and Latch

The pulse width modulator (PWM) consists of a comparator with the Oscillator ramp output applied to the inverting input. The Oscillator clock output applies a set pulse to the PWM Latch when the timing capacitor reaches its peak voltage, initiating Power Switch Circuit conduction. As the timing capacitor discharges, the ramp voltage decreases to a level that is less than the Error Amplifier output, causing the PWM Comparator to reset the latch and terminate Power Switch Circuit conduction for the duration of the ramp-down period. This method of having the Oscillator set and the PWM Comparator reset the Latch prevents the possibility of multiple output pulses during a given Oscillator clock cycle. This circuit configuration is commonly referred to as double pulse suppression logic. A timing diagram is shown in Figure 18 that illustrates the behavior of the pulse width modulator.

No load operation. The pulse width modulator is designed to operate between $73 \%$ and $0 \%$ duty cycle. The ability to operate down to zero duty cycle allows for no load operation without the burden of preloads. This feature is consistent with the Blue Angle requirements, as it minimizes power
consumption while in the stand-by operation mode. For operation at no load, the output may skip cycles. This is a common occurrence for this type of control circuit. The converter will switch for several cycles, and due to delays in the output filter and feedback loop, the duty cycle will not be reduced until the output has exceeded it's regulation limit. The unit will then shut down for several cycles until the voltage is below the regulation limit, and then it will switch again. During the time that switching cycles are not present the output voltage will decay according to it's RC time constant, which is based on the output capacitance and internal loading from the regulation circuitry. During this interval, the voltage on the $\mathrm{V}_{\mathrm{CC}}$ supply will also decay. If it decays below the lower hysteretic turn off threshold, the unit will shut down and recycle. This mode of operation is not normally desirable. In order to avoid it, the time constant for the $V_{C C}$ cap and load should be equal to, or greater than the time constant of the output. If no load operation is not required, a relatively small value $(<10 \mu \mathrm{~F})$ for the $\mathrm{V}_{\mathrm{CC}}$ capacitor is acceptable.

## Feedback Input

The feedback input, pin 2, accepts the DC error signal that feeds the non-inverting input to the PWM. Pin 2 has a nominal 2.7 kOhm internal resistor to ground, which converts the optocoupler current into a voltage. Its' signal is filtered by a 7.0 kHz low pass filter which reduces high frequency noise to the input of the PWM comparator.
Typically, the photo transistor of the optocoupler is connected between $\mathrm{V}_{\mathrm{CC}}$ (pin 1) and the Feedback input (pin 2). The photo transistor is effectively a current source which is driven by the LED, which is connected to the output regulation circuit of the power supply. An external capacitor may be connected from pin 2 to ground for additional noise filtering if necessary.

When the feedback input is below the lower threshold of the ramp signal, the output of the power converter will be operating at full duty cycle. The input current vs. duty cycle transfer function is shown in Figure 2. As the voltage increases, the duty cycle will vary linearly with the change in voltage at the feedback input, between the upper and lower extremes of the ramp waveform 2.7 V to 4.1 volts. Above the upper extreme point of the ramp, the duty cycle will be zero and no power will be transmitted to the output.
The circuit should be designed such that when the output is low, the optocoupler will be off, leaving the voltage at pin 2 at ground (full duty cycle). As the output voltage increases, the optocoupler will begin to conduct, such that the voltage at pin 2 increases until the proper duty cycle is reached to maintain regulation.

Pin 2 is protected from ESD transients by a 10 volt zener diode to ground.

## Current Limit Comparator and Power Switch Circuit

The NCP1000 series uses cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Current limiting is implemented by monitoring the instantaneous output switch current during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the Oscillator ramp-down period.

The Power Switch Circuit is constructed using a SenseFET allowing a virtually lossless method of monitoring the drain current. A small number of the power MOSFET cells are used for current sensing by connecting their individual sources to a single ground referenced sense resistor, $\mathrm{R}_{\mathrm{pk}}$. The current limit comparator detects if the voltage across $R_{p k}$ exceeds the reference level that is present at the noninverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch Circuit. Figure 9 shows that this detection method yields a relatively constant current limit threshold over temperature. The high voltage Power Switch Circuit is integrated with the control logic circuitry and is designed to directly drive the converter transformer. The Power Switch Circuit is capable of switching 700 V with an associated drain current that ranges from 0.5 A to 1.5 A . Proper drain voltage snubbing during converter start-up and overload is mandatory for reliable device operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path to prevent a premature reset of the PWM Latch. A potential premature reset signal is generated each time the Power Switch Circuit is driven into conduction and appears as a narrow voltage spike across current sense resistor $\mathrm{R}_{\mathrm{pk}}$. The spike is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior that masks the current signal until the Power Switch Circuit turn-on transition is completed.

The current limit propagation delay time is typically 220 ns . This time is measured from when an overcurrent appears at the Power Switch Circuit drain, to the beginning of turn-off. Care must be taken during transformer saturation so that the maximum device current limit rating is not exceeded. To determine the peak Power Switch Circuit current at turn off, the effect of the propagation delay must be taken into account. To do this, use the appropriate Current Limit Threshold value from the electrical tables, and then add the $\Delta \mathrm{Ipk}$ based on the $\mathrm{di} / \mathrm{dt}$ from Figure 16 . The di/dt of the circuit can be calculated by the following formula:

$$
\mathrm{di} / \mathrm{dt}(\mathrm{~A} / \mu \mathrm{s})=\mathrm{V} / \mathrm{L}
$$

where:
V is the rectified, filtered input voltage (volts)
L is the primary inductance of the flyback transformer (Henries)

## High Voltage Start-Up

The NCP1000-1002 contain an internal start-up circuit that eliminates the need for external start-up components. In addition, this circuit increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses the power supplied by the auxiliary winding.

Rectified, filtered ac line voltage is connected to pin 4. An internal JFET allows current to flow from the start-up pin, to the $\mathrm{V}_{\mathrm{CC}}$ pin at a current of approximately 3.0 mA . Figure 5 shows the startup current out of pin 1 which charges the capacitor(s) connected to this pin.

The start circuit will be enhanced (conducting) when the voltage at Pin $1\left(\mathrm{~V}_{\mathrm{CC}}\right)$ is less than 7.5 volts. It will remain enhanced until the $\mathrm{V}_{\mathrm{CC}}$ voltage reaches 8.5 volts. At this point the Power Switch Circuit will be disabled, and the unit will generate voltage via the auxiliary winding to maintain proper operation of the device. Figure 4 shows the charge time for turn-on vs. $\mathrm{V}_{\mathrm{CC}}$ capacitance when the unit is initially energized.

If the $\mathrm{V}_{\mathrm{CC}}$ voltage drops below 7.5 volts (e.g. current limit mode), the start circuit will again begin conducting, and will charge up the $\mathrm{V}_{\mathrm{CC}}$ cap until the 8.5 volt limit is reached.

## $\mathrm{V}_{\mathrm{CC}}$ Limiter and Undervoltage Lockout

The undervoltage lockout (UVLO) is designed to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. It inhibits operation of the major functions of the device by disabling the Internal Bias circuitry, and assures that the Power Switch Circuit remains in its "off" state as the bias voltage is initially brought up from zero volts. When the NCP100x is in the "off" state, the High Voltage Start-up circuit is operational. The UVLO is a hysteretic switch and will hold the device in its "off" state any time that the $\mathrm{V}_{\mathrm{CC}}$ voltage is less than 7.5 volts. As the $\mathrm{V}_{\mathrm{CC}}$ increases past 7.5 volts, the NCP100x will remain off until the upper threshold of 8.6 volts is reached. At this time the power converter is enabled and will commence operation. The UVLO will allow the unit to continue to operate as long as the $\mathrm{V}_{\mathrm{CC}}$ voltage exceeds 7.5 volts. The temperature characteristics of the UVLO circuit are shown in Figure 8.

If the converter output is overloaded or shorted, the device will enter the auto restart mode. This happens when the auxiliary winding of the power transformer does not have sufficient voltage to support the $\mathrm{V}_{\mathrm{CC}}$ requirements of the chip. Once the chip is operational, if the $\mathrm{V}_{\mathrm{CC}}$ voltage falls below 7.5 volts the unit will shut down, and the High Voltage Start-up circuit will be enabled. This will charge the $\mathrm{V}_{\mathrm{CC}}$ cap up to 8.5 volts, which will clock the divide by eight counter. The divide by eight counter holds the Power Switch Circuit off. This causes the $\mathrm{V}_{\mathrm{CC}}$ cap to discharge. It will continue to discharge and recharge for eight consecutive cycles. After the eighth cycle, the unit will turn on again. If the fault remains, the unit will again cycle through the auto restart mode; if the fault has cleared the unit will begin normal operation. The auto restart mode greatly reduces the power dissipation of the power devices in the circuit and

## NCP1000, NCP1001, NCP1002

improves reliability in overload conditions. Figure 20 shows the timing waveforms in auto restart mode.

The $\mathrm{V}_{\mathrm{CC}}$ pin receives its start-up power from the high voltage start-up circuit. Once the undervoltage lockout trip point is exceeded, the high voltage start-up circuit turns off, and the $\mathrm{V}_{\mathrm{CC}}$ pin receives its power from the auxiliary winding of the power transformer. Once the converter is enabled, the $\mathrm{V}_{\mathrm{CC}}$ voltage will be clamped by the 8.6 volt limiter. Since the voltage limiter will regulate the $\mathrm{V}_{\mathrm{CC}}$ voltage at 8.6 volts, it must shunt all excess current based on the input impedance to this pin. A resistor is required between the auxiliary winding filter capacitor and the $\mathrm{V}_{\mathrm{CC}}$ pin to limit the current.

## Optocoupler Fail-safe Circuit

The NCP100x has the ability to sense an open optocoupler and protect the load in the event of a failure. This circuit operates by sensing the current in the $\mathrm{V}_{\mathrm{CC}}$ limiter, and detecting a high current which is an indication of an open optocoupler.

The $\mathrm{V}_{\mathrm{CC}}$ pin receives the output of a current source which is created by the voltage drop between the auxiliary winding and the $\mathrm{V}_{\mathrm{CC}}$ limiter across the shunt resistor. The Vcc limiter will clamp the $\mathrm{V}_{\mathrm{CC}}$ voltage to approximately 8.6 volts. Any current that is available at this pin, that is not needed for either the chip bias current, or the opto current is shunted through this limiter.

The opto fail-safe circuit operates on the premise that under an open opto condition, the opto current will all be shunted through the $\mathrm{V}_{\mathrm{CC}}$ limiter, and the output voltage (and therefore the auxiliary winding voltage) will increase. The increase in auxiliary winding voltage will cause an amplified increase in the current into the $\mathrm{V}_{\mathrm{CC}}$ pin. To detect an open opto condition, the current in the limiter is measured and if it exceeds 10 milliamps, the chip will shut down and go into burst mode operation. After a shutdown signal, the optocoupler fail-safe circuit will enable the divide-by-eight counter and attempt to restart the unit after every eight $\mathrm{V}_{\mathrm{CC}}$ cycles.

For this circuit to operate properly, the shunt resistor must be chosen prudently. There is a range of values for $\mathrm{R}_{\mathrm{S}}$ that will determine the operation of this circuit. On one extreme, a large value of $\mathrm{R}_{\mathrm{S}}$ will minimize the bias current, which will have the effect of maximizing efficiency, while reducing the response to an open optocoupler. The other extreme is the minimum value of $\mathrm{R}_{\mathrm{S}}$, which will maximize the bias current into the chip and minimize the voltage overshoot in the event of an open optocoupler.
For minimum bias current:

$$
\mathrm{Rs}_{\max }=\frac{\left(\mathrm{V}_{\mathrm{AUX}} \min -8.8 \text { volts }\right)}{\mathrm{I}_{\mathrm{CC} 1 \max }}
$$

where:
$\mathrm{V}_{\mathrm{AUXmin}}$ is the minimum expected DC voltage from the auxiliary winding.
Typically, this voltage will vary between $\pm 5 \%$ to $\pm 10 \%$ from it's nominal value.
$\mathrm{I}_{\mathrm{CC} 1 \text { max }}$ is the maximum rated bias current for the device used. This value can found in the tables on the data sheet.
For the best optocoupler fail-safe response:

$$
\mathrm{Rs}_{\min }=\frac{\left(\mathrm{V}_{\mathrm{AUX} \text { max }}-7.2 \text { volts }\right)}{1.0 \mathrm{~mA}+\mathrm{I}_{\text {trip }}}
$$

where:
$\mathrm{V}_{\text {AUXmax }}$ is the maximum expected DC voltage from the auxiliary winding.
$\mathrm{I}_{\text {trip }}$ is the minimum trip current for the optocoupler fail-safe. This information can be found in the tables under
Current Limit and Thermal Protection, as well as in Figure 12.
The value of $R_{S}$ that is used in the circuit must be between the two extreme values calculated. Setting it closer to $\mathrm{R}_{\text {Smin }}$ will optimize the optocoupler fail-safe feature, while setting it closer to the $\mathrm{R}_{\mathrm{Smax}}$ value will minimize the bias current

## Thermal Shutdown and Package

The internal Thermal Shutdown block protects the device in the event that the maximum junction temperature is exceeded. When activated, typically at $140^{\circ} \mathrm{C}$, one input of the Driver is held low to disable the Power Switch Circuit. Thermal shutdown activation is non-latching and the Power Switch Circuit is allowed resume operation when the junction temperature falls below $110^{\circ} \mathrm{C}$. The thermal shutdown feature is provided to prevent catastrophic device failures from accidental overheating. It is not intended to be used as a substitute for proper heatsinking.

The die in the 8 -pin dual-in-line package is mounted on a special heat tab copper alloy lead frame. The tab consists of pins $3,6,7,8$ is specifically designed to improve the thermal conduction from the die to the printed circuit board. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance.

The die in the 5-pin TO-220 style package is mounted directly on a copper alloy heat tab. This metal tab is exposed on the backside of the package for heatsink attachment and is electrically common to the device ground, Pin 3 . A wide variety of TO-220 style heatsinks are commercially available for enhancing the thermal performance and converter output power capability.

## NCP1000, NCP1001, NCP1002

## Applications

The TO-220 devices have a single Ground, pin 3, that serves the high current return path for the Power Switch Circuit. Do not attempt to construct a converter circuit on a wire-wrap or plug-in prototype board. In order to ensure proper device operation and stability, it is important to minimize the lead length and the associated inductance of the ground pin. This pin must connect as directly as possible
to the printed circuit ground plane and should not be bent or offset by the board layout. The Power Switch Circuit pin can be offset if additional layout creepage distance is required. Due to the potentially high rate of change in switch current, a capacitor (if used), at pin 2, should have traces as short as possible, from pin 2 and ground. This will significantly reduce the level of switching noise that can be imposed upon the feedback control signal.


Figure 17. Representative Block Diagram


Figure 18. Pulse Width Modulation Timing Diagram


Figure 19. Start-up and Normal Operation Timing Diagram

## NCP1000, NCP1001, NCP1002



Figure 20. Auto Restart Operation Timing Diagram

## APPLICATIONS INFORMATION

## APPLICATION \#1: Offline Converter Provides 5.0 Volt, 1.0 Amp Output for Small Electronic Equipment

ON Semiconductor's NCP1000 series of offline converters offers a low cost, high efficiency power source for low power, electronic equipment. It serves the same function as small, line frequency transformers, but with the added benefits of line and load regulation, transient suppression, reduction in weight, and operation across the universal input voltage range.

This kit provides a 5.0 volt, 1.0 amp output, which is derived from an input source of 85 to 265 vac , and 50 Hz to 60 Hz . This range of input voltages will allow this circuit to function virtually anywhere in the world without modification. The output is regulated and current limited, and EMI filters are included on both the input and output.

Converter Test Data

| Parameter | Conditions | Data |
| :---: | :---: | :---: |
| Line Regulation | $85 \mathrm{v} \leq$ Vin $\leq 265 \mathrm{v}$ | $\Delta \mathrm{Vo}=6.0 \mathrm{mV}$ |
| Load Regulation | $0 \mathrm{~A} \leq \mathrm{lo} \leq 1.0 \mathrm{~A}$ | $\Delta \mathrm{Vo}=8.0 \mathrm{mV}$ |
| Combined Line/ Load Regulation | $\begin{aligned} & 85 \mathrm{v} \leq \mathrm{Vin} \leq 265 \mathrm{v} \\ & .09 \mathrm{~A} \leq \mathrm{lo} \leq 1.0 \mathrm{~A} \end{aligned}$ | $\Delta \mathrm{Vo}=10 \mathrm{mV}$ |
| Output Ripple | $\mathrm{lo}=1.0 \mathrm{~A}$ | 100 mV pp |
| Input Power | $\begin{aligned} & \mathrm{V}_{\text {in }}=115 \mathrm{v}, \mathrm{lo}=1.0 \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{in}}=220 \mathrm{v}, \mathrm{lo}=1.0 \mathrm{~A} \end{aligned}$ | 7.75 watts <br> 7.88 watts |
| Power Factor | $\begin{aligned} & \mathrm{V}_{\text {in }}=115 \mathrm{v}, \mathrm{lo}=1.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=220 \mathrm{v}, \mathrm{lo}=1.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & -.57 \\ & -.49 \end{aligned}$ |
| Efficiency | $\begin{aligned} & \mathrm{V}_{\text {in }}=115 \mathrm{v}, \mathrm{lo}=1.0 \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{in}}=220 \mathrm{v}, \mathrm{lo}=1.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \eta=66 \% \\ & \eta=64 \% \end{aligned}$ |



Figure 21. Wall Adapter Schematic

For additional information on this application, please order application note AND8019/D from the Literature Distribution Center or download from our website at http://onsemi.com.

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055

## Monolithic High Voltage Gated Oscillator Power Switching Regulator

The NCP1050 through NCP1055 are monolithic high voltage regulators that enable end product equipment to be compliant with low standby power requirements. This device series combines the required converter functions allowing a simple and economical power system solution for office automation, consumer, and industrial products. These devices are designed to operate directly from a rectified AC line source. In flyback converter applications they are capable of providing an output power that ranges from 6.0 W to 40 W with a fixed AC input of $100 \mathrm{~V}, 115 \mathrm{~V}$, or 230 V , and 3.0 W to 20 W with a variable AC input that ranges from 85 V to 265 V .

This device series features an active startup regulator circuit that eliminates the need for an auxiliary bias winding on the converter transformer, fault logic with a programmable timer for converter overload protection, unique gated oscillator configuration for extremely fast loop response with double pulse suppression, power switch current limiting, input undervoltage lockout with hysteresis, thermal shutdown, and auto restart fault detection. These devices are available in an economical 8-pin dual-in-line package.

## Features

- Startup Circuit Eliminates the Need for Transformer Auxiliary Bias Winding
- Optional Auxiliary Bias Winding Override for Lowest Standby Power Applications
- Converter Output Overload and Open Loop Protection
- Auto Restart Fault Protection
- IC Thermal Fault Protection
- Unique, Dual Edge, Gated Oscillator Configuration for Extremely Fast Loop Response
- Oscillator Frequency Dithering with Controlled Slew Rate Driver for Reduced EMI
- Low Power Consumption Allowing European Blue Angel Compliance
- On-Chip 700 V Power Switch Circuit and Active Startup Circuit
- Rectified AC Line Source Operation from 85 V to 265 V
- Input Undervoltage Lockout with Hysteresis
- Oscillator Frequency Options of $44 \mathrm{kHz}, 100 \mathrm{kHz}, 136 \mathrm{kHz}$


## Typical Applications

- AC-DC Converters
- Wall Adapters
- Portable Electronic Chargers
- Low Power Standby and Keep-Alive Supplies


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


DIP-8 CASE 626
P SUFFIX
Pin: 1. $\quad V_{C C}$
2. Control Input

6-8. Ground
No Connection
Power Switch Circuit Drain

MARKING DIAGRAM


X = Current Limit (0, 1, 2, 3, 4, 5)
Z = Oscillator Frequency (A, B, C)
A = Assembly Location
WL = Wafer Lot
$\mathrm{YY}=$ Year
WW = Work Week

## ORDERING INFORMATION

See detailed ordering and shipping information on page 1110 of this data sheet.


Figure 1. Typical Application
Pin Function Description

| Pin \# | Function |  |
| :---: | :---: | :--- |
| 1 | $V_{\mathrm{CC}}$ | This is the positive supply voltage input. During startup, power is supplied to this input from <br> Pin 5. When $\mathrm{V}_{\mathrm{CC}}$ reaches $\mathrm{V}_{\mathrm{CC}}($ on), the Startup Circuit turns off and the output is allowed to <br> begin switching with 1.0 V hysteresis on the $\mathrm{V}_{\mathrm{CC}}$ pin. The capacitance connected to this pin <br> programs fault timing and frequency modulation rate. |
| 2 | Control Input | The Power Switch Circuit is turned off when a current greater than approximately $50 \mu \mathrm{~A}$ is <br> drawn out of or applied to this pin. A 10 V clamp is built onto the chip to protect the device <br> from ESD damage or overvoltage conditions. |
| $3,6,7,8$ | Ground | This pin is the control circuit and Power Switch Circuit ground. It is part of the integrated circuit <br> lead frame. |
| 4 | No Connection |  |
| 5 | Power Switch Circuit | This pin is designed to directly drive the converter transformer primary, and internally connects <br> to Power Switch Circuit and Startup Circuit. |



Figure 2. Representative Block Diagram

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055



Figure 3. Timing Diagram for Gated Oscillator with Dual Edge PWM


Figure 4. Non-Latching Fault Condition Timing Diagram

## MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Switch and Startup Circuit <br> Drain Voltage Range <br> Drain Current Peak During Transformer Saturation | $\begin{gathered} \mathrm{V}_{\mathrm{DS}} \\ \mathrm{I}_{\mathrm{DS}(\mathrm{pk})} \end{gathered}$ | $\begin{aligned} & -0.3 \text { to } 700 \\ & 2.0 \mathrm{I}_{\text {lim }} \operatorname{Max} \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { A } \end{aligned}$ |
| Power Supply/V $\mathrm{V}_{\mathrm{CC}}$ Bypass and Control Input Voltage Range Current | $\begin{aligned} & V_{I R} \\ & I_{\text {max }} \end{aligned}$ | $\begin{gathered} -0.3 \text { to } 10 \\ 100 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| ```Thermal Characteristics P Suffix, Plastic Package Case 626 Junction to Lead Junction to Air, 2.0 Oz. Printed Circuit Copper Clad 0.36 Sq. Inch 1.0 Sq. Inch``` | $\begin{aligned} & \mathrm{R}_{\theta \mathrm{JCO}} \\ & \mathrm{R}_{\theta \mathrm{AJA}} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 45 \\ & 35 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
A. This device series contains ESD protection and exceeds the following tests:

Pins 1-3: Human Body Model 2000 V per MIL-STD-883, Method 3015. Machine Model Method 400 V .
Pin 5: Human Body Model 1000 V per MIL-STD-883, Method 3015. Machine Model Method 400 V .
Pin 5 is connected to the power switch and start-up circuits, and is rated only to the max voltage of the part, or 700 V .
B. This device contains Latch-up protection and exceeds $\pm 100 \mathrm{~mA}$ per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=8.0 \mathrm{~V}$, for typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values, $\mathrm{T}_{J}$ is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |


| Frequency ( $\mathrm{V}_{\mathrm{CC}}=7.6 \mathrm{~V}$ ) $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ : <br> A Suffix Device <br> B Suffix Device <br> C Suffix Device <br> $T_{J}=T_{\text {low }}$ to $T_{\text {high }}$ <br> A Suffix Device <br> B Suffix Device <br> C Suffix Device | fosc(low) | $\begin{gathered} 38 \\ 87 \\ 119 \\ \\ 37 \\ 84 \\ 113 \end{gathered}$ | $\begin{gathered} 43 \\ 97 \\ 132 \end{gathered}$ | $\begin{gathered} 47 \\ 107 \\ 145 \\ \\ 47 \\ 107 \\ 145 \end{gathered}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency ( $\mathrm{V}_{\mathrm{CC}}=8.6 \mathrm{~V}$ ) $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ : <br> A Suffix Device <br> B Suffix Device <br> C Suffix Device <br> $\mathrm{T}_{J}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ <br> A Suffix Device <br> B Suffix Device <br> C Suffix Device | fosc(high) | $\begin{gathered} 41 \\ 93 \\ 126 \\ \\ 39 \\ 90 \\ 120 \end{gathered}$ | $\begin{gathered} 46 \\ 103 \\ 140 \\ - \\ - \end{gathered}$ | $\begin{gathered} 50 \\ 113 \\ 154 \\ \\ 50 \\ 113 \\ 154 \end{gathered}$ | kHz |
| Frequency Sweep ( $\mathrm{V}_{\mathrm{CC}}=7.6 \mathrm{~V}$ to 8.6 V, $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | \%fosc | - | 6.0 | - | \% |
| Maximum Duty Cycle | $\mathrm{D}_{(\text {max })}$ | 74 | 77 | 80 | \% |

CONTROL INPUT

| Lower Window Input Current Threshold |  |  |  |  | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Switching Enabled, Sink Current Increasing | $\mathrm{I}_{\text {off( }}$ (low) | -58 | -47 | -37 |  |
| Switching Disabled, Sink Current Decreasing | Ion(low) | -50 | -38 | -25 |  |
| Upper Window Input Current Threshold |  |  |  |  |  |
| Switching Enabled, Source Current Increasing | $\mathrm{I}_{\text {off(high }}$ | 37 | 47 | 58 |  |
| Switching Disabled, Source Current Decreasing | Ion(high) | 25 | 37 | 50 |  |
| Control Window Input Voltage |  |  |  |  | V |
| Lower ( $\mathrm{I}_{\text {sink }}=25 \mu \mathrm{~A}$ ) | $\mathrm{V}_{\text {low }}$ | 1.15 | 1.3 | 1.45 |  |
| Upper ( ${ }_{\text {source }}=25 \mu \mathrm{~A}$ ) | $V_{\text {high }}$ | 4.2 | 4.6 | 5.0 |  |

2. Tested junction temperature range for the NCP105X series:

$$
\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} \quad \mathrm{~T}_{\text {high }}=+125^{\circ} \mathrm{C}
$$

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=8.0 \mathrm{~V}$, for typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values, $\mathrm{T}_{\mathrm{J}}$ is the operating junction temperature range that applies (Note 3), unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| POWER SWITCH CIRCUIT |  |  |  |  |  |
| Power Switch Circuit On-State Resistance <br> NCP1050, NCP1051, NCP1052 ( $\left.I_{D}=50 \mathrm{~mA}\right)$ $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=125^{\circ} \mathrm{C} \end{aligned}$ <br> NCP1053, NCP1054, NCP1055 ( $\mathrm{I}_{\mathrm{D}}=100 \mathrm{~mA}$ ) $\begin{aligned} & T_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{R}_{\mathrm{DS} \text { (on) }}$ |  | $\begin{aligned} & 26 \\ & 48 \\ & \\ & 13 \\ & 24 \end{aligned}$ | $\begin{aligned} & 30 \\ & 55 \\ & \\ & 15 \\ & 28 \end{aligned}$ | $\Omega$ |
| Power Switch Circuit \& Startup Breakdown Voltage ( $\mathrm{ID}_{\text {(offi) }}=100 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{(\mathrm{BR}) \mathrm{DS}}$ | 700 | - | - | V |
| Power Switch Circuit \& Startup Circuit Off-State Leakage Current $\begin{aligned} & \left(\mathrm{V}_{\mathrm{DS}}=700 \mathrm{~V}\right) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=125^{\circ} \mathrm{C} \end{aligned}$ | l DS(off) |  | 25 15 | $\begin{aligned} & 40 \\ & 80 \end{aligned}$ | $\mu \mathrm{A}$ |
| ```Switching Characteristics ( \(\mathrm{R}_{\mathrm{L}}=50 \Omega\), \(\mathrm{V}_{\mathrm{DS}}\) set for \(\mathrm{I}_{\mathrm{D}}=0.7 \mathrm{I}_{\mathrm{lim}}\) ) Turn-on Time ( \(90 \%\) to \(10 \%\) ) Turn-off Time ( \(10 \%\) to \(90 \%\) )``` | $\begin{aligned} & \mathrm{t}_{\mathrm{on}} \\ & \mathrm{t}_{\text {off }} \end{aligned}$ | - | 45 25 | - | ns |

CURRENT LIMIT AND THERMAL PROTECTION

| Current Limit Threshold ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) (Note 6) | lim |  |  |  | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP1050 |  | 93 | 100 | 107 |  |
| NCP1051 |  | 186 | 200 | 214 |  |
| NCP1052 |  | 279 | 300 | 321 |  |
| NCP1053 |  | 372 | 400 | 428 |  |
| NCP1054 |  | 493 | 530 | 567 |  |
| NCP1055 |  | 632 | 680 | 728 |  |
| Conversion Power Deviation ( $\mathrm{J}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) (Note 7) | $\mathrm{I}^{2} \mathrm{fosc}$ | - | 0 | 10 | \% ${ }^{2} \mathrm{~Hz}$ |
| Propagation Delay, Current Limit Threshold to Power Switch Circuit Output NCP1050, NCP1051, NCP1052 <br> NCP1053, NCP1054, NCP1055 | tpLH | - | $\begin{aligned} & 125 \\ & 250 \end{aligned}$ | - | ns |
| Thermal Protection ( $\mathrm{V}_{\mathrm{CC}}=8.6 \mathrm{~V}$ ) (Note 3, 4, 5) Shutdown (Junction Temperature Increasing) Hysteresis (Junction Temperature Decreasing) | $\begin{aligned} & \mathrm{T}_{\mathrm{sd}} \\ & \mathrm{~T}_{\mathrm{H}} \end{aligned}$ | 140 | $\begin{gathered} 160 \\ 75 \end{gathered}$ | - | ${ }^{\circ} \mathrm{C}$ |

STARTUP CONTROL

| Startup/V CC Regulation <br> Startup Threshold $/ \mathrm{V}_{\mathrm{CC}}$ Regulation Peak ( $\mathrm{V}_{\mathrm{CC}}$ Increasing) Minimum Operating $/ V_{C C}$ Valley Voltage After Turn-On Hysteresis | $\mathrm{V}_{\mathrm{CC}(\text { on })}$ <br> $\mathrm{V}_{\mathrm{CC}}$ (off) $\mathrm{V}_{\mathrm{H}}$ | 8.2 7.2 | 8.6 7.6 1.0 | 9.0 8.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Undervoltage Lockout Threshold Voltage, $\mathrm{V}_{\text {CC }}$ Decreasing | $\mathrm{V}_{\mathrm{CC} \text { (reset) }}$ | 4.2 | 4.6 | 5.0 | V |
| Startup Circuit Output Current (Power Switch Circuit Output $=40 \mathrm{~V}$ ) $\begin{aligned} \mathrm{V}_{C C} & =0 \mathrm{~V} \\ \mathrm{~T}_{J} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J} & =-40 \text { to } 125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =\mathrm{V}_{\mathrm{CC}}(\text { on }) \\ \mathrm{T}_{J} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J} & =-40 \text { to } 125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\text {start }}$ | $\begin{aligned} & 5.4 \\ & 4.5 \\ & 4.6 \\ & 3.5 \end{aligned}$ | 6.2 - 5.4 | $\begin{aligned} & 7.0 \\ & 8.0 \\ & 6.2 \\ & 7.0 \end{aligned}$ | mA |
| Output Fault Condition Auto Restart <br> ( $\mathrm{V}_{\mathrm{CC}}$ Capacitor $=10 \mu \mathrm{~F}$, Power Switch Circuit Output $=40 \mathrm{~V}$ ) <br> Average Switching Duty Cycle <br> Frequency | $\begin{aligned} & D_{\mathrm{rst}} \\ & \mathrm{f}_{\mathrm{rst}} \end{aligned}$ | - | 8.0 5.0 | - | \% Hz |

3. Tested junction temperature range for the NCP105X series:

$$
\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} \quad \mathrm{~T}_{\text {high }}=+125^{\circ} \mathrm{C}
$$

4. Maximum package power dissipation limits must be observed.
5. Guaranteed by design only.
6. Adjust di/dt to reach $\mathrm{l}_{\text {lim }}$ in $4.0 \mu \mathrm{sec}$.
7. Consult factory for additional options including trim for output power accuracy.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=8.0 \mathrm{~V}$, for typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values, $\mathrm{T}_{J}$ is the operating junction temperature range that applies (Note 8), unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TOTAL DEVICE |  |  |  |  |  |
| Power Supply Current After UVLO Turn-On (Note 9) | $\mathrm{ICC1}$ |  |  |  | mA |
| Power Switch Circuit Enabled |  |  |  |  |  |
| NCP1050, NCP1051, NCP1052 |  |  |  |  |  |
| A Suffix Device |  | 0.35 | 0.47 | 0.55 |  |
| B Suffix Device |  | 0.40 | 0.52 | 0.60 |  |
| C Suffix Device |  | 0.45 | 0.56 | 0.65 |  |
| NCP1053, NCP1054, NCP1055 |  |  |  |  |  |
| A Suffix Device |  | 0.40 | 0.53 | 0.60 |  |
| B Suffix Device |  | 0.45 | 0.61 | 0.70 |  |
| C Suffix Device |  | 0.50 | 0.67 | 0.80 |  |
| Power Switch Circuit Disabled |  |  |  |  |  |
| Non-Fault Condition | $\mathrm{I}_{\text {cc2 }}$ | 0.35 | 0.45 | 0.55 |  |
| Fault Condition | ICC3 | 0.10 | 0.16 | 0.25 |  |

8. Tested junction temperature range for the NCP105X series:
$\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} \quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
9. See Non-Latching Fault Condition Timing Diagram in Figure 4.

NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055


Figure 5. Oscillator Frequency (A Suffix) versus Temperature


Figure 7. Oscillator Frequency (C Suffix) versus Temperature


Figure 9. Maximum Duty Cycle versus Temperature


Figure 6. Oscillator Frequency (B Suffix) versus Temperature


Figure 8. Frequency Sweep versus Temperature


Figure 10. Lower Window Control Input Current Thresholds versus Temperature

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055



Figure 11. Upper Window Control Input Current Thresholds versus Temperature


Figure 13. Control Input Upper Window Clamp Voltage versus Temperature


Figure 12. Control Input Lower Window Clamp Voltage versus Temperature

Figure 14. On Resistance versus Temperature


Figure 15. Power Switch and Startup Circuit Leakage Current versus Voltage


Figure 16. Power Switch and Startup Circuit Output Capacitance versus Applied Voltage

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055



Figure 17. Normalized Peak Current Limit versus Temperature


Figure 19. Supply Voltage Thresholds versus Temperature


Figure 18. Peak Current Limit Deviation versus Current Slew Rate


Figure 20. Undervoltage Lockout Threshold versus Temperature


Figure 21. Start Current versus Temperature


Figure 22. Startup Current versus Supply Voltage

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055



Figure 23. Startup Current versus Pin 5 Voltage


Figure 25. Supply Current versus Temperature (NCP1053/4/5)


Figure 24. Supply Current versus Temperature (NCP1050/1/2)


Figure 26. Supply Current in Fault Condition versus Temperature

## Introduction

The NCP105X series represents a new higher level of integration by providing on a single monolithic chip all of the active power, control, logic, and protection circuitry required to implement a high voltage flyback converter and compliance with very low standby power requirements for modern consumer electronic power supplies. This device series is designed for direct operation from a rectified 240 VAC line source and requires minimal external components for a complete cost sensitive converter solution. Potential markets include cellular phone chargers, standby power supplies for personal computers, secondary bias supplies for microprocessor keep-alive supplies and IR detectors. A description of each of the functional blocks is given below, and the representative block diagram is shown in Figure 2.

This device series features an active startup regulator circuit that eliminates the need for an auxiliary bias winding on the converter transformer, fault logic with a programmable timer for converter overload protection, unique gated oscillator configuration for extremely fast loop response with double pulse suppression, oscillator frequency dithering with a controlled slew rate driver for reduced EMI, cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, thermal shutdown, and auto restart or latched off fault detect device options. These devices are available in an economical 8-pin PDIP package.

## Oscillator

The Oscillator is a unique fixed-frequency, duty-cyclecontrolled oscillator. It charges and discharges an on chip timing capacitor to generate a precise square wave signal used to pulse width modulate the Power Switch Circuit. During the discharge of the timing capacitor, the Oscillator duty cycle output holds one input of the Driver low. This action keeps the Power Switch Circuit off, thus limiting the maximum duty cycle.

A frequency modulation feature is incorporated into the IC in order to aide in EMI reduction. Figure 3 illustrates this frequency modulation feature. The power supply voltage, $\mathrm{V}_{\mathrm{CC}}$, acts as the input to the built-in voltage controlled oscillator. As the $\mathrm{V}_{\mathrm{CC}}$ voltage is swept across its nominal operating range of 7.6 to 8.6 V , the oscillator frequency is swept across its corresponding range.

The center oscillator frequency is internally programmed for $44 \mathrm{kHz}, 100 \mathrm{kHz}$, or 136 kHz operation with a controlled charge to discharge current ratio that yields a maximum Power Switch duty cycle of $77 \%$. The Oscillator temperature characteristics are shown in Figures 5 through 9. Contact an ON Semiconductor sales representative for further information regarding frequency options.

## Control Input

The Control Input pin circuit has parallel source follower input stages with voltage clamps set at 1.3 and 4.6 V . Current sources clamp the input current through the followers at
approximately $47 \mu \mathrm{~A}$ with $10 \mu \mathrm{~A}$ hysteresis. When a source or sink current in excess of this value is applied to this input, a logic signal generated internally changes state to block power switch conduction. Since the output of the Control Input sense is sampled continuously during $\mathrm{t}_{\text {on }}$ ( $77 \%$ duty cycle), it is possible to turn the Power Switch Circuit on or off at any time within $t_{\text {on }}$. Because it does not have to wait for the next cycle (rising edge of the clock signal) to switch on, and because it does not have to wait for current limit to turn off, the circuit has a very fast transient response as shown in Figure 3.

In a typical converter application the control input current is drawn by an optocoupler. The collector of the optocoupler is connected to the Control Input pin and the emitter is connected to ground. The optocoupler LED is mounted in series with a shunt regulator (typically a TL431) at the DC output of the converter. When the power supply output is greater than the reference voltage (shunt regulator voltage plus optocoupler diode voltage drop), the optocoupler turns on, pulling down on the Control Input. The control input logic is configured for line input sensing as well.

## Turn On Latch

The Oscillator output is typically a $77 \%$ positive duty cycle square waveform. This waveform is inverted and applied to the reset input of the turn-on latch to prevent any power switch conduction during the guaranteed off time. This square wave is also gated by the output of the control section and applied to the set input of the same latch. Because of this gating action, the power switch can be activated when the control input is not asserted and the oscillator output is high.

The use of this unique gated Turn On Latch over an ordinary Gated Oscillator allows a faster load transient response. The power switch is allowed to turn on immediately, within the maximum duty cycle time period, when the control input signals a necessary change in state.

## Turn Off Latch

A Turn Off Latch feature has been incorporated into this device series to protect the power switch circuit from excessive current, and to reduce the possibility of output overshoot in reaction to a sudden load removal. If the Power Switch current reaches the specified maximum current limit, the Current Limit Comparator resets the Turn Off Latch and turns the Power Switch Circuit off. The turn off latch is also reset when the Oscillator output signal goes low or the Control Input is asserted, thus terminating output MOSFET conduction. Because of this response to control input signals, it provides a very fast transient response and very tight load regulation. The turn off latch has an edge triggered set input which ensures that the switch can only be activated once during any oscillator period. This is commonly referred to as double pulse suppression.

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055

## Current Limit Comparator and Power Switch Circuit

The Power Switch Circuit is constructed with a SENSEFET ${ }^{T M}$ in order to monitor the drain current. A portion of the current flowing through the circuit goes into a sense element, $\mathrm{R}_{\text {sense }}$. The current limit comparator detects if the voltage across $\mathrm{R}_{\text {sense }}$ exceeds the reference level that is present at its inverting input. If this level is exceeded, the comparator quickly resets the Turn Off Latch, thus protecting the Power Switch Circuit.

A Leading Edge Blanking circuit was placed in the current sensing signal path to prevent a premature reset of the Turn Off Latch. A potential premature reset signal is generated each time the Power Switch Circuit is driven into conduction and appears as a narrow voltage spike across current sense resistor $\mathrm{R}_{\text {sense }}$. The spike is due to the Power Switch Circuit gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior that masks the current signal until the Power Switch Circuit turn-on transition is completed. The current limit propagation delay time is typically 125 to 250 nanoseconds. This time is measured from when an overcurrent appears at the Power Switch Circuit drain, to the beginning of turn-off. Care must be taken during transformer saturation so that the maximum device current limit rating is not exceeded.

The high voltage Power Switch Circuit is monolithically integrated with the control logic circuitry and is designed to directly drive the converter transformer. Because the characteristics of the power switch circuit are well known, the gate drive has been tailored to control switching transitions to help limit electromagnetic interference (EMI). The Power Switch Circuit is capable of switching 700 V with an associated drain current that ranges nominally from 0.10 to 0.68 Amps.

## Startup Circuit

Rectified AC line voltage is applied to the Startup Circuit on Pin 5, through the primary winding. The circuit is self-biasing and acts as a constant current source, gated by control logic. Upon application of the AC line voltage, this circuit routes current into the supply capacitor typically connected to Pin 1. During normal operation, this capacitor is hysteretically regulated from 7.6 to 8.6 V by monitoring the supply voltage with a comparator and controlling the startup current source accordingly. This Dynamic Self-Supply (DSS) functionality offers a great deal of applications flexibility as well. The startup circuit is rated at a maximum 700 V (maximum power dissipation limits must be observed).

## Undervoltage Lockout

An Undervoltage Lockout (UVLO) comparator is included to guarantee that the integrated circuit has sufficient voltage to be fully functional. The UVLO comparator monitors the supply capacitor input voltage at Pin 1 and disables the Power Switch Circuit whenever the capacitor voltage drops below the undervoltage lockout threshold. When this level is crossed, the controller enters a new startup phase by turning the current source on. The supply voltage will then have to exceed the startup threshold in order to turn off the startup current source. Startup and normal operation of the converter are shown in Figure 3.

## Fault Logic and Timer Control

The NCP105X series has integrated Fault Logic and Timer Control circuitry for detecting application fault conditions such as open loop, overload or a short circuited output. A timer is generated by driving the supply capacitor with a known current and hysteretically regulating the supply voltage between set thresholds. The timer period starts when the supply voltage reaches the nominal upper threshold of 8.6 V and stops when the drain current of the integrated circuit draws the supply capacitor voltage down to the undervoltage lockout threshold of 7.6 V .

If, during this timer period, no feedback has been applied to the control input, the fault logic is set to indicate an abnormal condition. This may occur, for example, when the optocoupler fails or the output of the application is overloaded or completely shorted. In this case, the part will stop switching, go into a low power mode, and begin to draw down the supply capacitor to the reset threshold voltage of 4.6 V. At that time, the startup circuit will turn on again to drive the supply to the turn on threshold. Then the part will begin the cycle again, effectively sampling the control input to determine if the fault condition has been removed. This mode is commonly referred to as burst mode operation and is shown is Figure 4.
Proper selection of the supply capacitor allows successful startup with monotonically increasing output voltage, without falsely sensing a fault condition. Figure 4 shows successful startup and the evolution of the signals involved in the presence of a fault.

## Thermal Shutdown

The internal Thermal Shutdown block protects the device in the event that the maximum junction temperature is exceeded. When activated, typically at $160^{\circ} \mathrm{C}$, one input of the Driver is held low to disable the Power Switch Circuit. The Power Switch is allowed to resume operation when the junction temperature falls below $85^{\circ} \mathrm{C}$. The thermal shutdown feature is provided to prevent catastrophic device failures from accidental overheating. It is not intended to be used as a substitute for proper heatsinking.

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055

## APPLICATIONS

Two application examples have been provided in this document, and they are described in detail in this section. Figure 27 shows a Universal Input, 10 Watt Converter Application as well as a 5.5 Watt Charger Application using the NCP1053B. The Charger consists of the additional components Q1, C13, and R7 through R10, as shown. These were constructed and tested using the printed circuit board layout shown in Figure 39. The board consists of a fiberglass epoxy material (FR4) with a single side of two ounce per square foot ( $70 \mu \mathrm{~m}$ thick) copper foil. Test data from the two applications is given in Figures 28 through 38.

Both applications generate a well-regulated output voltage over a wide range of line input voltage and load current values. The charger application transitions to a constant current output if the load current is increased beyond a preset range. This can be very effective for battery charger application for portable products such as cellular telephones, personal digital assistants, and pagers. Using the NCP105X series in applications such as these offers a wide range of flexibility for the system designer.

The NCP105X application offers a low cost alternative to other applications. It uses a Dynamic Self-Supply (DSS) function to generate its own operating supply voltage such that an auxiliary transformer winding is not needed. (It also offers the flexibility to override this function with an auxiliary winding if ultra-low standby power is the designer's main concern.) This product also provides for automatic output overload, short circuit, and open loop protection by entering a programmable duty cycle burst mode of operation. This eliminates the need for expensive devices overrated for power dissipation or maximum current, or for redundant feedback loops.

The application shown in Figure 27 can be broken down into sections for the purpose of operating description. Components C1, L1 and C6 provide EMI filtering for the design, although this is very dependent upon board layout, component type, etc. D1 through D4 along with C2 provide the AC to bulk DC rectification. The NCP1053 drives the primary side of the transformer, and the capacitor, C 5 , is an integral part of the Dynamic Self-Supply. R1, C3, and D5 comprise an RCD snubber and R2 and C4 comprise a ringing damper both acting together to protect the IC from voltage transients greater than 700 volts and reduce radiated noise from the converter. Diode D6 along with C7-9, L2, C11, and C 12 rectify the transformer secondary and filter the output
to provide a tightly regulated DC output. IC3 is a shunt regulator that samples the output voltage by virtue of R5 and R6 to provide drive to the optocoupler, IC2, Light Emitting Diode (LED). C10 is used to compensate the shunt regulator. When the application is configured as a Charger, Q1 delivers additional drive to the optocoupler LED when in constant current operation by sampling the output current through R7 and R8.

## Component Selection Guidelines

Choose snubber components R1, C3, and D5 such that the voltage on pin 5 is limited to the range from 0 to 700 volts. These components protect the IC from substrate injection if the voltage was to go below zero volts, and from avalanche if the voltage was to go above 700 volts, at the cost of slightly reduced efficiency. For lower power design, a simple RC snubber as shown, or connected to ground, can be sufficient. Ensure that these component values are chosen based upon the worst-case transformer leakage inductance and worst-case applied voltage. Choose R2 and C4 for best performance radiated switching noise.

Capacitor C5 serves multiple purposes. It is used along with the internal startup circuitry to provide power to the IC in lieu of a separate auxiliary winding. It also serves to provide timing for the oscillator frequency sweep for limiting the conducted EMI emissions. The value of C 5 will also determine the response during an output fault (overload or short circuit) or open loop condition as shown in Figure 4, along with the total output capacitance.

Resistors R5 and R6 will determine the regulated output voltage along with the reference voltage chosen with IC3.
The base to emitter voltage drop of Q1 along with the value of R 7 will set the fixed current limit value of the Charger application. R9 is used to limit the base current of Q1. Component R8 can be selected to keep the current limit fixed with very low values of output voltage or to provide current limit foldback with results as shown in Figures 28 and 32. A relatively large value of R8 allows for enough output voltage to effectively drive the optocoupler LED for fixed current limit. A low value of R8, along with resistor R10, provides for a low average output power using the fault protection feature when the output voltage is very low. C13 provides for output voltage stability when the Charger application is in current limit.


T1: COOPER ELECTRONIC TECHNOLOGIES
PART \# CTX22-15348
PRIMARY: 97 turns of \#29 AWG, Pin 4 = start, Pin 5 = finish
SECONDARY: 5 turns of 0.40 mm , Pins 2 and $1=$ start, Pins 7 and $8=$ finish GAP: Designed for Total 1.24 mH Primary Inductance
CORE: TSF-7070
BOBBIN: Pins 3 and 6 Removed, EE19

[^23]| Test | Conditions | Converter Results | Charger Results |
| :---: | :---: | :---: | :---: |
| Line Regulation | $\begin{aligned} & \mathrm{V}_{\text {in }}=85-265 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{I}_{\text {out }}=190 \mathrm{~mA} \\ & \mathrm{l}_{\text {out }}=950 \mathrm{~mA} \\ & \mathrm{I}_{\text {out }}=1.91 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 1 \mathrm{mV} \\ & 1 \mathrm{mV} \\ & 2 \mathrm{mV} \end{aligned}$ |  |
|  | $\begin{aligned} \mathrm{V}_{\text {in }}=85-265 \mathrm{~V}_{\mathrm{AC}} ; & \mathrm{I}_{\text {out }} \\ \mathrm{l}_{\text {out }} & =500 \mathrm{~mA} \\ \mathrm{I}_{\text {out }} & =1.00 \mathrm{AA} \end{aligned}$ |  | $\begin{aligned} & 2 \mathrm{mV} \\ & 3 \mathrm{mV} \\ & 7 \mathrm{mV} \end{aligned}$ |
| Load Regulation | $\begin{aligned} & \mathrm{V}_{\text {in }}=85 \mathrm{~V}_{\mathrm{AC}} ; I_{\text {out }}=190 \mathrm{~mA}-1.91 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }} 110 \mathrm{~V}_{\mathrm{AC}} ; I_{\text {out }}=190 \mathrm{~mA}-1.91 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{VAC}^{\prime} I_{\text {out }}=190 \mathrm{~mA}-1.91 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=265 \mathrm{VAC}_{\mathrm{A}} ; I_{\text {out }}=190 \mathrm{~mA}-1.91 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 1 \mathrm{mV} \\ & 2 \mathrm{mV} \\ & 3 \mathrm{mV} \\ & 3 \mathrm{mV} \end{aligned}$ |  |
|  | $\begin{aligned} & \mathrm{V}_{\text {in }}=85 \mathrm{~V}_{\mathrm{AC}} ; I_{\text {out }}=100 \mathrm{~mA}-1.00 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=110 \mathrm{~V}^{\prime} ; I_{\text {out }}=100 \mathrm{~mA}-1.00 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{VA}^{\prime} ; I_{\text {out }}=100 \mathrm{~mA}-1.00 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=265 \mathrm{VAC}^{2} I_{\text {out }}=100 \mathrm{~mA}-1.00 \mathrm{~A} \end{aligned}$ |  | $\begin{gathered} 8 \mathrm{mV} \\ 9 \mathrm{mV} \\ 9 \mathrm{mV} \\ 12 \mathrm{mV} \end{gathered}$ |
| Output Ripple | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; l_{\text {out }}=1.91 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; l_{\text {out }}=1.91 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 40 \mathrm{mV}_{\mathrm{p}-\mathrm{p}} \\ & 50 \mathrm{mV} \mathrm{p}-\mathrm{p} \end{aligned}$ |  |
|  | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; l_{\text {out }}=1.00 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; l_{\text {out }}=1.00 \mathrm{~A} \end{aligned}$ |  | $\begin{aligned} & 40 \mathrm{mV}_{p-p} \\ & 50 \mathrm{mV}_{p-p} \end{aligned}$ |
| Efficiency | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{I}_{\text {out }}=1.91 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{l}_{\text {out }}=1.91 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & \hline 72.0 \% \\ & 71.2 \% \end{aligned}$ |  |
|  | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{R}_{8}=1.2 \Omega, \mathrm{I}_{\text {out }}=1.00 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; R_{8}=1.2 \Omega, \mathrm{I}_{\text {out }}=1.00 \mathrm{~A} \end{aligned}$ |  | $\begin{aligned} & \text { 52.2\% } \\ & 52.8 \% \end{aligned}$ |
|  | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{R}_{8}=0 \Omega, \mathrm{I}_{\text {out }}=1.00 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{R}_{8}=0 \Omega, \mathrm{I}_{\text {out }}=1.00 \mathrm{~A} \end{aligned}$ |  | $\begin{aligned} & \hline 65.0 \% \\ & 62.4 \% \end{aligned}$ |
| No Load Input Power | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; l_{\text {out }}=0 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; l_{\text {out }}=0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 110 \mathrm{~mW} \\ & 240 \mathrm{~mW} \end{aligned}$ | $\begin{aligned} & \hline 110 \mathrm{~mW} \\ & 190 \mathrm{~mW} \end{aligned}$ |
| Standby Output Power | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; P_{\text {in }}=1 \mathrm{~W} \\ & \mathrm{~V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; P_{\text {in }}=1 \mathrm{~W} \end{aligned}$ | 675 mW 570 mW | $\begin{aligned} & 635 \mathrm{~mW} \\ & 570 \mathrm{~mW} \end{aligned}$ |
| Short Circuit Load Input Power | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{V}_{\text {out }}=0 \mathrm{~V} \text { (Shorted) } \\ & \left.\mathrm{V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{V}_{\text {out }}=0 \mathrm{~V} \text { (Shorted }\right) \end{aligned}$ | $\begin{aligned} & 500 \mathrm{~mW} \\ & 750 \mathrm{~mW} \end{aligned}$ |  |
|  | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{R}_{8}=1.2 \Omega, \mathrm{~V}_{\text {out }}=0 \mathrm{~V} \text { (Shorted) } \\ & \mathrm{V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{R}_{8}=1.2 \Omega, \mathrm{~V}_{\text {out }}=0 \mathrm{~V} \text { (Shorted) } \end{aligned}$ |  | $\begin{aligned} & 1.05 \mathrm{~W} \\ & 1.40 \mathrm{~W} \end{aligned}$ |
|  | $\begin{aligned} & \mathrm{V}_{\text {in }}=110 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{R}_{8}=0 \Omega, \mathrm{~V}_{\text {out }}=0 \mathrm{~V} \text { (Shorted) } \\ & \mathrm{V}_{\text {in }}=230 \mathrm{~V}_{\mathrm{AC}} ; \mathrm{R}_{8}=0 \Omega, \mathrm{~V}_{\text {out }}=0 \mathrm{~V}(\text { Shorted }) \end{aligned}$ |  | $\begin{gathered} 900 \mathrm{~mW} \\ 1.25 \mathrm{~W} \end{gathered}$ |

Figure 28. Converter and Charger Test Data Summary

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055



Figure 29. Converter Line Regulation


Figure 31. Converter Load Regulation


Figure 33. Converter Load Transient Response


Figure 30. Charger Line Regulation


Figure 32. Charger Load Regulation


Figure 34. Charger Load Transient Response

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055



Figure 35. Converter Efficiency


Figure 37. Converter On/Off Line Transient Response


Figure 36. Charger Efficiency


Figure 38. Charger On/Off Line Transient Response


Figure 39. Printed Circuit Board and Component Layout

## NCP1050, NCP1051, NCP1052, NCP1053, NCP1054, NCP1055

DEVICE ORDERING INFORMATION (Note 10)

| Device (Note 11) | Package | Shipping | $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ <br> ( $\Omega$ ) | $\begin{gathered} \mathrm{I}_{\mathrm{pk}} \\ (\mathrm{~mA}) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: |
| NCP1050PZZZ | DIP-8 | 50 Units/Rail | 30 | 100 |
| NCP1051PZZZ |  |  |  | 200 |
| NCP1052PZZZ |  |  |  | 300 |
| NCP1053PZZZ |  |  | 15 | 400 |
| NCP1054PZZZ |  |  |  | 530 |
| NCP1055PZZZ |  |  |  | 680 |

10. Consult factory for additional optocoupler fail-safe latching, frequency, current limit and line input options.
11. $\mathrm{ZZZ}=$ Oscillator Frequency in $\mathrm{kHz}(44,100$ or 136)

## MC33368

## High Voltage GreenLine ${ }^{T M}$ Power Factor Controller

The MC33368 is an active power factor controller that functions as a boost preconverter in off-line power supply applications. MC33368 is optimized for low power, high density power supplies requiring a minimum board area, reduced component count and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the $\mathrm{V}_{\mathrm{CC}}$ supply voltage and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer and cycle-by-cycle current limiting.

- Lossless Off-Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer


## ON Semiconductor

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MARKING
DIAGRAMS

PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33368D | SO-16 | 48 Units/Rail |
| MC33368DR2 | SO-16 | 2500 Tape \& Reel |
| MC33368P | DIP-16 | 25 Units/Rail |

Representative Block Diagram


This device contains 240 active transistors.

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage (Transient) | $V_{\text {CC }}$ | 20 | V |
| Power Supply Voltage (Operating) | $V_{C C}$ | 16 | V |
| Line Voltage | $V_{\text {Line }}$ | 500 | V |
| Current Sense, Multiplier, Compensation, Voltage Feedback, Restart Delay and Zero Current Input Voltage | $V_{\text {in1 }}$ | -1.0 to +10 | V |
| LEB Input, Frequency Clamp Input | $\mathrm{V}_{\text {in2 }}$ | -1.0 to +20 | V |
| Zero Current Detect Input | $1{ }_{\text {in }}$ | $\pm 5.0$ | mA |
| Restart Diode Current | $\mathrm{l}_{\text {in }}$ | 5.0 | mA |
| Power Dissipation and Thermal Characteristics P Suffix, Plastic Package Case 648 Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{AJA}} \end{gathered}$ | $\begin{aligned} & 1.25 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751K Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{JJA}} \end{gathered}$ | $\begin{aligned} & 450 \\ & 178 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -25 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=14.5 \mathrm{~V}\right.$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{J}}=-25$ to $+125^{\circ} \mathrm{C}$ )

| Characteristic |
| :--- |
| Symbol |
| ERROR AMPLIFIER |
|  Min Typ Max Unit  <br> Input Bias Current $\left(\mathrm{V}_{\mathrm{FB}}=5.0 \mathrm{~V}\right)$ $\mathrm{I}_{\mathrm{IB}}$ - 0 1.0 $\mu \mathrm{~A}$ <br> Input Offset Voltage $\left(\mathrm{V}_{\mathrm{Comp}}=3.0 \mathrm{~V}\right)$ $\mathrm{V}_{\mathrm{IO}}$ - 2.0 50 mV <br> Transconductance $\left(\mathrm{V}_{\mathrm{Comp}}=3.0 \mathrm{~V}\right)$ $\mathrm{g}_{\mathrm{m}}$ 30 51 80 $\mu \mathrm{mho}$ <br> Output Source $\left(\mathrm{V}_{\mathrm{FB}}=4.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{Comp}}=3.0 \mathrm{~V}\right)$ $\mathrm{I}_{\mathrm{O}}$ 9.0 17.5 30 $\mu \mathrm{~A}$ <br> Output Sink $\left(\mathrm{V}_{\mathrm{FB}}=5.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{Comp}}=3.0 \mathrm{~V}\right)$ $\mathrm{I}_{\mathrm{O}}$ 9.0 17.5 30  |

OVERVOLTAGE COMPARATOR

| Voltage Feedback Input Threshold | $\mathrm{V}_{\mathrm{FB}(\mathrm{OV})}$ | $1.07 \mathrm{~V}_{\mathrm{FB}}$ | $1.084 \mathrm{~V}_{\mathrm{FB}}$ | $1.1 \mathrm{~V}_{\mathrm{FB}}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Propagation Time to Output | $\mathrm{T}_{\mathrm{P}}$ | - | 705 | - | ns |

## MULTIPLIER

| Input Bias Current, $\mathrm{V}_{\text {Mult }}\left(\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}\right)$ | 1 IB | - | -0.2 | -1.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Threshold, $\mathrm{V}_{\text {comp }}$ | $\left.\mathrm{V}_{\text {th( }} \mathrm{M}\right)$ | 1.8 | 2.1 | 2.4 | V |
| Dynamic Input Voltage Range Multiplier Input Compensation | $V_{\text {Mult }}$ <br> $V_{\text {Comp }}$ | $\begin{gathered} 0 \text { to } 2.5 \\ \mathrm{~V}_{\text {th }(\mathrm{M})} \text { to } \\ \left(\mathrm{V}_{\mathrm{hh}(\mathrm{M})}+1.0\right) \\ \hline \end{gathered}$ | $\begin{gathered} 0 \text { to } 3.5 \\ V_{\text {th }(M)} \text { to } \\ \left(\mathrm{V}_{\mathrm{th}(\mathrm{M})}+2.0\right) \\ \hline \end{gathered}$ | - | V |
| $\left.\begin{array}{l} \text { Multiplier Gain }\left(\mathrm{V}_{\text {Mult }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {Comp }}=\mathrm{V}_{\text {th }(\mathrm{M})}+1.0 \mathrm{~V}\right) \\ {\left[\mathrm{K}=\frac{\mathrm{V}_{\mathrm{CS}} \text { Threshold }}{\mathrm{V}_{\text {Mult }}\left(\mathrm{V}_{\text {Comp }}-\mathrm{V}_{\text {th }(\mathrm{M})}\right)}\right.} \end{array}\right] .$ | K | 0.25 | 0.51 | 0.75 | 1/V |

VOLTAGE REFERENCE

| Voltage Reference $\left(\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {ref }}$ | 4.95 | 5.0 | 5.05 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 16 V$)$ | Reg $_{\text {line }}$ | - | 5.0 | 100 | mV |
| Load Regulation ( $\left.\mathrm{I}_{\mathrm{O}}=0-5.0 \mathrm{~mA}\right)$ | Reg $_{\text {load }}$ | - | 5.0 | 100 | mV |
| Total Output Variation Over Line, Load and Temperature | $\mathrm{V}_{\text {ref }}$ | 4.8 | - | 5.2 | V |
| Maximum Output Current | $\mathrm{I}_{\mathrm{O}}$ | 5.0 | 10 | - | mA |
| Reference Undervoltage Lockout Threshold | $\mathrm{V}_{\mathrm{th}}$ | - | 4.5 | - | V |

## ZERO CURRENT DETECTOR

| Input Threshold Voltage $\left(\mathrm{V}_{\text {in }}\right.$ Increasing) | $\mathrm{V}_{\mathrm{th}}$ | 1.0 | 1.2 | 1.4 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Hysteresis $\left(\mathrm{V}_{\text {in }}\right.$ Decreasing) | $\mathrm{V}_{\mathrm{H}}$ | 100 | 200 | 300 | mV |
| Delay to Output | $\mathrm{T}_{\mathrm{pd}}$ | - | 127 | - | ns |

CURRENT SENSE COMPARATOR

| Input Bias Current $\left(\mathrm{V}_{\mathrm{CS}}=0\right.$ to 2.0 V$)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 0.2 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage ( $\left.\mathrm{V}_{\text {Mult }}=-0.2 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{IO}}$ | - | 4.0 | 50 | mV |
| Maximum Current Sense Input Threshold $\left(\mathrm{V}_{\text {Comp }}=5.0 \mathrm{~V}\right.$, <br> $\left.\mathrm{V}_{\text {Mult }}=5.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {th(max }}$ | 1.3 | 1.5 | 1.8 | V |
| Delay to Output <br> $\left(\mathrm{V}_{\text {LEB }}=12 \mathrm{~V}, \mathrm{~V}_{\text {Comp }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {Mult }}=5.0 \mathrm{~V}\right)$ <br> $\left(\mathrm{V}_{\mathrm{CS}}=0\right.$ to 5.0 V Step, $\left.\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ | $\mathrm{t}_{\text {PHL(in/out) }}$ | 50 | 270 | 425 | ns |

## FREQUENCY CLAMP

| Frequency Clamp Input Threshold | $\mathrm{V}_{\text {th(FC) }}$ | 1.9 | 2.0 | 2.1 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Frequency Clamp Capacitor Reset Current $\left(\mathrm{V}_{\mathrm{FC}}=0.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {reset }}$ | 0.5 | 1.7 | 4.0 | mA |
| Frequency Clamp Disable Voltage | $\mathrm{V}_{\mathrm{DFC}}$ | - | 7.3 | 8.0 | V |

## MC33368

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{C C}=14.5 \mathrm{~V}\right.$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{J}}=-25$ to $+125^{\circ} \mathrm{C}$ )

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| DRIVE OUTPUT |  |  |  |  |  |
| Source Resistance (Current Sense $\left.=0 \mathrm{~V}, \mathrm{~V}_{\text {Gate }}=\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}\right)$ | $\mathrm{R}_{\mathrm{OH}}$ | 4.0 | 8.6 | 20 | $\Omega$ |
| Sink Resistance (Current Sense $\left.=3.0 \mathrm{~V}, \mathrm{~V}_{\text {Gate }}=1.0 \mathrm{~V}\right)$ | $\mathrm{R}_{\mathrm{OL}}$ | 4.0 | 7.2 | 20 |  |
| Output Voltage Rise Time $(25 \%-75 \%)\left(\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ | $\mathrm{t}_{\mathrm{r}}$ | - | 55 | 200 | ns |
| Output Voltage Fall Time $(75 \%-25 \%)\left(\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ | $\mathrm{t}_{\mathrm{f}}$ | - | 70 | 200 | ns |
| Output Voltage in Undervoltage $\left(\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}, \mathrm{I}_{\text {Sink }}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{O}(\mathrm{UV})}$ | - | 0.01 | 0.25 | V |

## LEADING EDGE BLANKING

| Input Bias Current | $\mathrm{I}_{\text {bias }}$ | - | 0.1 | 0.5 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Threshold (as Offset from $\mathrm{V}_{\mathrm{CC}}$ ) $\left(\mathrm{V}_{\text {LEB }}\right.$ Increasing) | $\mathrm{V}_{\text {LEB }}$ | 1.0 | 2.25 | 2.75 | V |
| Hysteresis ( $\mathrm{V}_{\text {LEB }}$ Decreasing) | $\mathrm{V}_{\mathrm{H}}$ | 100 | 270 | 500 | mV |

UNDERVOLTAGE LOCKOUT

| Startup Threshold ( $\mathrm{V}_{\mathrm{CC}}$ Increasing) | $\mathrm{V}_{\text {th }(o n)}$ | 11.5 | 13 | 14.5 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On ( $\mathrm{V}_{\mathrm{CC}}$ Decreasing) | $\mathrm{V}_{\text {Shutdown }}$ | 7.0 | 8.5 | 10 | V |
| Hysteresis | $\mathrm{V}_{\mathrm{H}}$ | - | 4.5 | - | V |

TIMER

| Watchdog Timer | $\mathrm{I}_{\text {DLY }}$ | 180 | 385 | 800 | $\mu \mathrm{~s}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Restart Timer Threshold | $\mathrm{V}_{\text {th(restart })}$ | 1.5 | 2.3 | 3.0 | V |
| Restart Pin Output Current $\left(\mathrm{V}_{\text {restart }}=0 \mathrm{~V}, \mathrm{~V}_{\text {ref }}=5.0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {restart }}$ | 3.1 | 5.2 | 7.1 | mA |

TOTAL DEVICE

| Line Startup Current $\left(\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}, \mathrm{~V}_{\text {Line }}=50 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{SU}}$ | 5.0 | 16 | 25 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Line Operating Current $\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {th(on }}, \mathrm{V}_{\text {Line }}=50 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{OP}}$ | 3.0 | 12.9 | 20 | mA |
| $\mathrm{~V}_{\mathrm{CC}}$ Dynamic Operating Current $\left(50 \mathrm{kHz}, \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ | $\mathrm{I}_{\mathrm{CC}}$ | - | 5.3 | 8.5 | mA |
| $\mathrm{~V}_{\mathrm{CC}}$ Static Operating Current $\left(\mathrm{I}_{\mathrm{O}}=0\right)$ |  | - | 3.0 | - |  |
| Line Pin Leakage $\left(\mathrm{V}_{\text {Line }}=500 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {Line }}$ | - | 30 | 80 | $\mu \mathrm{~A}$ |



Figure 1. Current Sense Input Threshold versus Multiplier Input


Figure 3. Reference Voltage versus Temperature


Figure 2. Current Sense Input Threshold versus Multiplier Input, Expanded View


Figure 4. Overvoltage Comparator Input Threshold versus Temperature


Figure 5. Error Amplifier Transconductance and Phase versus Frequency


Figure 6. Error Amplifier Transient Response


Figure 7. Quickstart Charge Current versus Temperature


Figure 8. Watchdog Timer Delay versus Temperature


Figure 9. Drive Output Waveform


Figure 10. Supply Current versus Supply Voltage


Figure 11. Transient Thermal Resistance


Figure 12. Low Load Detection Response Waveform

## FUNCTIONAL DESCRIPTION

## INTRODUCTION

With the goal of exceeding the requirements of legislation on line current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple cost effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 13.


Figure 13. Uncorrected Power Factor Circuit
This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 14 . Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.


Figure 14. Uncorrected Power Factor Input Waveforms
Power factor correction can be achieved with the use of either a passive or active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing with the boost converter being the most popular topology. Since active input circuits operate at a frequency much higher than that
of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

## Operating Description

The MC33368 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 15, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

## Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage-to-current gain ( $\mathrm{g}_{\mathrm{m}} \approx 50 \mu \mathrm{mhos}$ ). The noninverting input is internally biased at $5.0 \mathrm{~V} \pm 2.0 \%$. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is $-1.0 \mu \mathrm{~A}$ which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R2. The Error Amplifier output is internally connected to the Multiplier and is pinned out (Pin 4) for external loop compensation. Typically, the bandwidth is set below 20 Hz so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amplifier monitors the average output voltage of the converter over several line cycles resulting in a fixed Drive Output on-time. The amplifier output stage can sink and source $11.5 \mu \mathrm{~A}$ of current and is capable of swinging from 1.7 to 5.0 V , assuring that the Multiplier can be driven over its entire dynamic range.

Note that by using a transconductance type amplifier, the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of the Voltage Feedback pin by the Error Amplifier and Overvoltage Comparator.

## Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to $1.08 \mathrm{~V}_{\text {ref }}$. In order to prevent false tripping during normal operation, the value of the output filter capacitor C3 must be large enough to keep the peak-to-peak ripple less than $16 \%$ of the average dc output.

## Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 5 with respect to ground while the Error Amplifier output at Pin 4 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 1. Note that both inputs are extremely linear over a wide dynamic range, 0 to 3.2 V for Pin 5 and 2.5 to 4.0 V for Pin 4. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET on-time to track the input line voltage, thus making the preconverter load appear to be resistive.

$$
\text { Pin } 6 \text { Threshold } \approx 0.55\left(\mathrm{~V}_{\operatorname{Pin} 4}-\mathrm{V}_{\operatorname{Pin} 3}\right) \mathrm{V}_{\operatorname{Pin} 5}
$$

## Zero Current Detector

The MC33368 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on-time by setting the $\mathrm{R}_{\mathrm{S}}$ Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn-on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.2 V . To prevent false tripping, 200 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 10 V clamp prevents input overvoltage breakdown while the lower -0.7 V clamp prevents substrate injection. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps to 5.0 mA or less.

## Current Sense Comparator and RS Latch

The Current Sense Comparator $\mathrm{R}_{\mathrm{S}}$ Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R7 in series with the source of output switch. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 6 where:

$$
I_{\mathrm{pk}}=\frac{\text { Pin } 6 \text { Threshold }}{\text { R7 }}
$$

Abnormal operating conditions occur when the preconverter is running at extremely low line or if output voltage sensing is lost. Under these conditions, the Current

Sense Comparator threshold will be internally clamped to 1.5 V . Therefore, the maximum peak switch current is:

$$
\mathrm{I}_{\mathrm{pk}(\max )}=\frac{1.5 \mathrm{~V}}{\mathrm{R7}}
$$

With the component values shown in Figure 15, the Current Sense Comparator threshold, at the peak of the haversine, varies from 110 mV at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns .

## Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than $385 \mu$ s after the inductor current reaches zero.

## Undervoltage Lockout and Quickstart

The MC33368 has a 5.0 V internal reference brought out to Pin 1 and capable of sourcing 10 mA typically. It also contains an Undervoltage Lockout (UVLO) circuit which suppresses the Gate output at Pin 11 if the $\mathrm{V}_{\mathrm{CC}}$ supply voltage drops below 8.5 V typical.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C 1 will be discharged, holding the Error Amplifier output below the Multiplier's threshold. This will prevent Drive Output switching and delay bootstraping of capacitor C4 by diode D6. If Pin 4 does not reach the multiplier threshold before C 4 discharges below the lower SMPS UVLO threshold, the converter will hiccup and experience a significant startup delay. The Quickstart circuit is designed to precharge C 1 to 1.7 V . This level is slightly below the Pin 4 Multiplier threshold, allowing immediate Drive Output switching.

## Restart Delay

A restart delay pin is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. When power is first applied, there is no startup delay, but subsequent cycling of the $\mathrm{V}_{\mathrm{CC}}$ voltage will result in delay times that are programmed by an external resistor and capacitor. The Restart Delay, Pin 2, is a high impedance, so that an external capacitor can provide delay times as long as several seconds.

If the SMPS output is short circuited, the transformer winding, which provides the $\mathrm{V}_{\mathrm{CC}}$ voltage to the control IC and the MC33368, will be unable to sustain $\mathrm{V}_{\mathrm{CC}}$ to the control circuits. The restart delay capacitor at Pin 2 of the MC33368 prevents the high voltage startup transistor within the IC from maintaining the voltage on C 4 . After $\mathrm{V}_{\mathrm{CC}}$ drops below the UVLO threshold in the SMPS, the SMPS switching transistors are held off for the time programmed by the values of the restart capacitor (C9) and resistor (R8). In this manner, the SMPS switching transistors are operated
at very low duty cycles, preventing their destruction. If the short circuit fault is removed, the power supply system will turn on by itself in a normal startup mode after the restart delay has timed out.

## Output Switching Frequency Clamp

In normal operation, the MC33368 operates the boost inductor in the critical mode. That is, the inductor current ramps to a peak value, ramps down to zero, then immediately begins ramping positive again. The peak current is programmed by the multiplier output within the IC. As the input voltage haversine declines to near zero, the output switch on-time becomes constant, rather than going to zero because of the small integrated dc voltage at Pin 5 caused by C2, R3 and R5. Because of this, the average line current does not exactly follow the line voltage near the zero crossings. The Output Switching Frequency Clamp remedies this situation to improve power factor and minimize EMI generated in this operating region. The values of R10 and C7, as shown in Figure 15, program a minimum off-time in the frequency clamp which overrides the zero current detect signal, forcing a minimum off-time. This allows discontinuous conduction operation of the boost inductor in the zero crossing region, and the average line current more nearly follows the voltage. The Output Switching Frequency Clamp function can be disabled by connecting the FC input, Pin 13, to the $\mathrm{V}_{\mathrm{CC}}$ supply Pin 12.

For best results, the minimum off-time, determined by the values of R10 and C7, should be chosen so that $t_{s(\min )}=t_{(o n)}$ $+\mathrm{t}_{(\text {off }) \mathrm{fc}}$. Output drive is inhibited when the voltage at the frequency clamp input is less than 2.0 V . When the output drive is high, C 7 is discharged through an internal $100 \mu \mathrm{~A}$ current source. When the output drive switches low, C7 is charged through R10. The drive output is inhibited until the voltage across C7 reaches 2.0 V , establishing a minimum off-time where:

$$
\mathrm{t}_{\text {(off)fc }}=-\mathrm{R} 10 \mathrm{C} 7 \log _{\mathrm{e}}\left[1-\left(\frac{2}{\mathrm{~V}_{\mathrm{CC}}}\right)\right]
$$

## Output

The IC contains a CMOS output driver that was specifically designed for direct drive of power MOSFETs. The Gate Output is capable of up to $\pm 1500 \mathrm{~mA}$ peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Gate Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull-down resistor. The totem-pole output has been optimized to minimize cross-conduction current during high speed operation.

Table 1. Design Equations

| Calculation | Formula | Notes |
| :---: | :---: | :---: |
| Converter Output Power | $\mathrm{P}_{\mathrm{O}}=\mathrm{V}_{\mathrm{O}} \mathrm{l}_{\mathrm{O}}$ | Calculate the maximum required output power. |
| Peak Indicator Current | $\mathrm{I}_{\mathrm{L}(\mathrm{pk})}=\frac{2 \sqrt{2} \mathrm{P}_{\mathrm{O}}}{\eta \mathrm{Vac}_{(\mathrm{LL})}}$ | Calculated at the minimum required ac line voltage for output regulation. Let the efficiency $\eta=0.92$ for low line operation. |
| Inductance | $\mathrm{L}_{\mathrm{P}}=\frac{\mathrm{t}\left(\frac{\mathrm{~V}_{\mathrm{O}}}{\sqrt{2}}-\mathrm{Vac}_{(\mathrm{LL})}\right) \eta \mathrm{Vac}_{(\mathrm{LL})}{ }^{2}}{\sqrt{2} \mathrm{~V}_{\mathrm{O}} \mathrm{P}_{\mathrm{O}}}$ | Let the switching cycle $\mathrm{t}=40 \mu \mathrm{~s}$ for universal input ( 85 to 265 Vac ) operation and $20 \mu \mathrm{~s}$ for fixed input ( 92 to 138 Vac , or 184 to 276 Vac ) operation. |
| Switch On-Time | $\mathrm{t}_{(\mathrm{on})}=\frac{2 \mathrm{P}_{\mathrm{O}} \mathrm{~L}_{\mathrm{P}}}{\eta \mathrm{Vac}^{2}}$ | In theory, the on-time $t_{(o n)}$ is constant. In practice, $t_{(o n)}$ tends to increase at the ac line zero crossings due to the charge on capacitor C 5 . Let $\mathrm{Vac}=\mathrm{Vac}_{(\mathrm{LL})}$ for initial $t_{\text {(on) }}$ and $t_{\text {(off) }}$ calculations. |
| Switch Off-Time | $t_{\text {(off) }}=\frac{t^{t} \text { on) }}{\frac{V_{O}}{\sqrt{2} \operatorname{Vac}\|\operatorname{Sin} \theta\|}-1}$ | The off-time $t_{\text {(off) }}$ is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta $(\theta)$ represents the angle of the ac line voltage. |
| Minimum Switch Off-Time | ${ }^{\mathrm{t}}{ }_{(\mathrm{off})_{\text {min }}}=\frac{\mathrm{L}_{\mathrm{P}} \mathrm{I}_{\mathrm{L}(\mathrm{pk})}}{\mathrm{V}_{\mathrm{O}}}$ | The off-time is at a minimum at ac line crossings. This equation is used to calculate $t_{\text {(off) }}$ as Theta approaches zero. |
| Delay Time | $t_{d}=-R 10 C 7 \ln \left(\frac{v_{C C}-2}{V_{C C}}\right)$ | The delay time is used to override the minimum off-time at the ac line zero crossings by programming the Frequency Clamp with C7 and R10. |
| Switching Frequency | $f=\frac{1}{t_{(\text {on })}+t_{(\text {off })}}$ | The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, $\mathrm{t}_{(\text {off })}$ approaches zero producing an increase in switching frequency. |
| Peak Switch Current | $\mathrm{R7}=\frac{\mathrm{V}_{\text {CS }}}{\mathrm{I}_{\mathrm{L}(\mathrm{pk})}}$ | Set the current sense threshold $\mathrm{V}_{\mathrm{CS}}$ to 1.0 V for universal input ( 85 to 265 Vac ) operation and to 0.5 V for fixed input ( 92 to 138 Vac , or 184 to 276 Vac ) operation. Note that $\mathrm{V}_{\mathrm{CS}}$ must be less than 1.4 V . |
| Multiplier Input Voltage | $V_{M}=\frac{\operatorname{Vac} \sqrt{2}}{\left(\frac{R 5}{R 3}+1\right)}$ | Set the multiplier input voltage $\mathrm{V}_{\mathrm{M}}$ to 3.0 V at high line. Empirically adjust $\mathrm{V}_{\mathrm{M}}$ for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line. |
| Converter Output Voltage | $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\text {ref }}\left(\frac{R 2}{R 1}+1\right)-I_{I B} R 1$ | The $I_{I B}$ R1 error term can be minimized with a divider current in excess of $100 \mu \mathrm{~A}$. |
| Converter Output Peak-to-Peak Ripple Voltage | $\Delta \mathrm{V}_{\mathrm{O}(\mathrm{pp})}=\mathrm{I}_{\mathrm{L}(\mathrm{pk})} \sqrt{\left(\frac{1}{2 \pi f_{\mathrm{ac}} \mathrm{C} 3}\right)^{2}+E S R^{2}}$ | The calculated peak-to-peak ripple must be less than $16 \%$ of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator Text. ESR is the equivalent series resistance of C3. |
| Error Amplifier Bandwidth | $\mathrm{BW}=\frac{\mathrm{g}_{\mathrm{m}}}{2 \pi \mathrm{C} 1}$ | The bandwidth is typically set to 20 Hz . When operating at high ac line, the value of C 1 may need to be increased. |

NOTE: The following converter characteristics must be chosen:
$\mathrm{V}_{\mathrm{O}}=$ Desired output voltage. $\quad \mathrm{Vac}_{(\mathrm{LL})}=\mathrm{AC}$ RMS minimum required operating line voltage for output regulation.
$\mathrm{I}_{\mathrm{O}}=$ Desired output current. $\quad \Delta \mathrm{V}_{\mathrm{O}}=$ Converter output peak-to-peak ripple voltage.
Vac = AC RMS operating line voltage.


Power Factor Controller Test Data

| AC Line Input |  |  |  |  |  |  |  |  | DC Output |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Current Harmonic Distortion (\% $\mathrm{I}_{\text {fund }}$ ) |  |  |  |  | $\mathrm{V}_{0}(\mathrm{pp})$ | $\mathrm{V}_{0}$ | 10 | Po | n(\%) |
| $\mathrm{V}_{\text {rms }}$ | Pin | PF | $I_{\text {fund }}$ | THD | 2 | 3 | 5 | 7 |  |  |  |  |  |
| 90 | 79.7 | 0.999 | 0.89 | 0.5 | 0.15 | 0.09 | 0.06 | 0.09 | 3.0 | 244.4 | 0.31 | 76.01 | 95.4 |
| 100 | 79.3 | 0.998 | 0.79 | 0.5 | 0.14 | 0.09 | 0.08 | 0.10 | 3.0 | 242.9 | 0.31 | 75.54 | 95.3 |
| 110 | 78.9 | 0.997 | 0.72 | 0.5 | 0.16 | 0.13 | 0.08 | 0.10 | 3.0 | 242.9 | 0.31 | 75.30 | 95.4 |
| 120 | 78.5 | 0.996 | 0.66 | 0.5 | 0.15 | 0.12 | 0.08 | 0.13 | 3.0 | 243.0 | 0.31 | 75.57 | 96.3 |
| 130 | 78.1 | 0.994 | 0.60 | 0.5 | 0.14 | 0.12 | 0.07 | 0.14 | 3.0 | 243.0 | 0.31 | 75.57 | 96.7 |
| 138 | 77.8 | 0.991 | 0.57 | 0.5 | 0.15 | 0.14 | 0.08 | 0.14 | 3.0 | 243.0 | 0.31 | 75.57 | 97.1 |

Heatsink = AAVID Engineering Inc., 590302B03600, or 593002B03400
Figure 15. 80 W Power Factor Controller


Power Factor Controller Test Data

| AC Line Input |  |  |  |  |  |  |  |  | DC Output |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {rms }}$ | Pin | PF | $\mathrm{I}_{\text {fund }}$ | Current Harmonic Distortion (\% $\mathrm{l}_{\text {fund }}$ ) |  |  |  |  | $\mathrm{V}_{0(\mathrm{pp})}$ | $\mathrm{V}_{0}$ | 10 | $\mathrm{P}_{0}$ | n (\%) |
|  |  |  |  | THD | 2 | 3 | 5 | 7 |  |  |  |  |  |
| 90 | 190.4 | 0.995 | 2.11 | 5.8 | 0.16 | 0.32 | 0.24 | 0.80 | 3.6 | 398.0 | 0.44 | 175.9 | 92.4 |
| 120 | 192.1 | 0.997 | 1.60 | 3.2 | 0.08 | 0.17 | 0.07 | 0.30 | 3.6 | 398.9 | 0.44 | 177.1 | 92.2 |
| 138 | 192.7 | 0.997 | 1.40 | 0.9 | 0.08 | 0.24 | 0.03 | 0.15 | 3.6 | 402.3 | 0.45 | 179.0 | 92.9 |
| 180 | 194.3 | 0.995 | 1.08 | 0.9 | 0.04 | 0.18 | 0.04 | 0.08 | 3.6 | 409.1 | 0.45 | 182.9 | 94.1 |
| 240 | 189.3 | 0.983 | 0.80 | 0.7 | 0.08 | 0.21 | 0.08 | 0.06 | 3.6 | 407.0 | 0.45 | 181.1 | 95.7 |
| 268 | 186.3 | 0.972 | 0.71 | 0.6 | 0.11 | 0.32 | 0.10 | 0.10 | 3.6 | 406.2 | 0.44 | 180.4 | 96.8 |

Heatsink = AAVID Engineering Inc., 590302B03600
Figure 16. 175 W Universal Input Power Factor Controller


An RFI filter is required for best performance when connecting the preconverter directly to the ac line. The filter attenuates the level of high frequency switching that appears on the ac line current waveform. Figures 15 and 16 work well with commercially available two stage filters such as the Delta Electronics 03DPCG6. Shown above is a single stage test filter that can easily be constructed with four ac line rated capacitors and a common-mode transformer. Coilcraft CMT3-28-2 was used to test Figures 15 and 16. It has a minimum inductance of 28 mH and a maximum current rating of 2.0 A . Coilcraft CMT4-17-9 was used to test Figure 19. It has a minimum inductance of 17 mH and a maximum current rating of 9.0 A . Circuit conversion efficiency $\eta(\%)$ was calculated without the power loss of the RFI filter.

Figure 17. Power Factor Test Setup


Figure 18. On/Off Control


Figure 19. 400 W Power Factor Controller


Figure 20. Printed Circuit Board and Component Layout (Circuits of Figures 15 and 16)

## Power Factor Controllers

The MC34262/MC33262 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off-line power converter applications. These integrated circuits feature an internal startup timer for stand-alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle-by-cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual-in-line and surface mount plastic packages.

- Overvoltage Comparator Eliminates Runaway Output Voltage
- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2\% Internal Bandgap Reference
- Totem Pole Output with High State Clamp
- Undervoltage Lockout with 6.0 V of Hysteresis
- Low Startup and Operating Current
- Supersedes Functionality of SG3561 and TDA4817


## Simplified Block Diagram



MC34262
MC33262

## POWER FACTOR CONTROLLERS

## SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626


D SUFFIX PLASTIC PACKAGE

CASE 751
(SO-8)

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| MC34262D | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-8 |
| MC34262P |  |  |
| MC33262D | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | SO-8 |
| MC33262P |  |  |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Total Power Supply and Zener Current | $\left(\mathrm{I}_{\mathrm{CC}}+\mathrm{I}_{\mathrm{Z}}\right)$ | 30 | mA |
| Output Current, Source or Sink (Note 1) | 10 | 500 | mA |
| Current Sense, Multiplier, and Voltage Feedback Inputs | $\mathrm{V}_{\text {in }}$ | -1.0 to +10 | V |
| Zero Current Detect Input High State Forward Current Low State Reverse Current | $\mathrm{l}_{\text {in }}$ | $\begin{array}{r} 50 \\ -10 \end{array}$ | mA |
| Power Dissipation and Thermal Characteristics P Suffix, Plastic Package, Case 626 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air <br> D Suffix, Plastic Package, Case 751 Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $R_{\text {日JA }}$ | $\begin{aligned} & 800 \\ & 100 \\ & 450 \\ & 178 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 3) MC34262 <br> MC33262 | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+85 \\ -40 \text { to }+105 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$ (Note 2), for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER |  |  |  |  |  |
| Voltage Feedback Input Threshold $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\mathrm{V} \mathrm{CC}=12 \mathrm{~V} \text { to } 28 \mathrm{~V}) \end{aligned}$ | $V_{\text {FB }}$ | $\begin{gathered} 2.465 \\ 2.44 \end{gathered}$ | $2.5$ | $\begin{gathered} 2.535 \\ 2.54 \end{gathered}$ | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to $\left.28 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | Regline | - | 1.0 | 10 | mV |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ ) | $1 I_{B}$ | - | -0.1 | -0.5 | $\mu \mathrm{A}$ |
| Transconductance ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{gm}_{\mathrm{m}}$ | 80 | 100 | 130 | $\mu \mathrm{mho}$ |
| Output Current <br> Source ( $\mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) <br> Sink ( $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) | 10 | - | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | - | $\mu \mathrm{A}$ |
| Output Voltage Swing <br> High State ( $\mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) <br> Low State ( $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) | $\mathrm{V}_{\mathrm{OH}(e a)}$ <br> $\mathrm{V}_{\mathrm{OL}(\mathrm{ea})}$ | $\begin{gathered} 5.8 \\ - \end{gathered}$ | $\begin{aligned} & 6.4 \\ & 1.7 \end{aligned}$ | $2.4$ | V |

OVERVOLTAGE COMPARATOR

| Voltage Feedback Input Threshold | $\mathrm{V}_{\mathrm{FB}(\mathrm{OV})}$ | $1.065 \mathrm{~V}_{\mathrm{FB}}$ | $1.08 \mathrm{~V}_{\mathrm{FB}}$ | $1.095 \mathrm{~V}_{\mathrm{FB}}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |

## MULTIPLIER

| Input Bias Current, Pin $3\left(\mathrm{~V}_{\mathrm{FB}}=0 \mathrm{~V}\right.$ ) | IB | - | -0.1 | -0.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Threshold, Pin 2 | $\mathrm{V}_{\mathrm{th}(\mathrm{M})}$ | $1.05 \mathrm{~V}_{\text {OL(EA) }}$ | 1.2 $\mathrm{V}_{\text {OL(EA) }}$ | - | V |
| Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2) | $\begin{aligned} & \mathrm{V}_{\text {Pin } 3} \\ & \mathrm{~V}_{\text {Pin } 2} \end{aligned}$ | $\begin{gathered} 0 \text { to } 2.5 \\ V_{\text {th }(M)} \text { to } \\ \left(\mathrm{V}_{\mathrm{th}(\mathrm{M})}+1.0\right) \end{gathered}$ | $\begin{gathered} 0 \text { to } 3.5 \\ \mathrm{~V}_{\mathrm{th}(\mathrm{M}} \mathrm{to} \\ \left(\mathrm{~V}_{\mathrm{th}(\mathrm{M})}+1.5\right) \end{gathered}$ |  | V |
| Multiplier Gain ( $\left.\left.\mathrm{V}_{\text {Pin } 3}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {Pin } 2}=\mathrm{V}_{\text {th( }} \mathrm{M}\right)+1.0 \mathrm{~V}\right)$ (Note 4) | K | 0.43 | 0.65 | 0.87 | 1/V |

ZERO CURRENT DETECTOR

| Input Threshold Voltage ( $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\text {th }}$ | 1.33 | 1.6 | 1.87 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Hysteresis ( $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\mathrm{H}}$ | 100 | 200 | 300 | mV |
| Input Clamp Voltage |  |  |  |  | V |
| High State (l $\mathrm{I}_{\mathrm{DET}}=+3.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {IH }}$ | 6.1 | 6.7 | - |  |
| Low State (IDET $=-3.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {IL }}$ | 0.3 | 0.7 | 1.0 |  |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$ (Note 2), for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CURRENT SENSE COMPARATOR |  |  |  |  |  |
| Input Bias Current ( $\mathrm{V}_{\text {Pin } 4}=0 \mathrm{~V}$ ) | $I_{\text {IB }}$ | - | -0.15 | -1.0 | $\mu \mathrm{A}$ |
| Input Offset Voltage ( $\left.\mathrm{V}_{\text {Pin } 2}=1.1 \mathrm{~V}, \mathrm{~V}_{\text {Pin } 3}=0 \mathrm{~V}\right)$ | $\mathrm{V}_{10}$ | - | 9.0 | 25 | mV |
| Maximum Current Sense Input Threshold (Note 5) | $\mathrm{V}_{\mathrm{th}(\text { max })}$ | 1.3 | 1.5 | 1.8 | V |
| Delay to Output | $\mathrm{t}_{\text {PHL }}$ (in/out) | - | 200 | 400 | ns |
| DRIVE OUTPUT |  |  |  |  |  |
| $\begin{array}{cl} \text { Output Voltage } & \left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right) \\ \text { Low State } & (\text { ISink }=20 \mathrm{~mA}) \\ & (\text { ISink }=200 \mathrm{~mA}) \\ \text { High State } & (\text { ISource }=20 \mathrm{~mA}) \\ & \text { (ISource }=200 \mathrm{~mA}) \end{array}$ | $\mathrm{V}_{\mathrm{OL}}$ <br> $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & - \\ & 9.8 \\ & 7.8 \end{aligned}$ | $\begin{gathered} 0.3 \\ 2.4 \\ 10.3 \\ 8.4 \end{gathered}$ | $\begin{aligned} & 0.8 \\ & 3.3 \\ & - \end{aligned}$ | V |
| Output Voltage ( $\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}$ ) <br> High State ( $\mathrm{I}_{\text {Source }}=20 \mathrm{~mA}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ ) | $\mathrm{V}_{\mathrm{O}(\text { max })}$ | 14 | 16 | 18 | V |
| Output Voltage Rise Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ ) | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | 120 | ns |
| Output Voltage Fall Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ ) | $t_{f}$ | - | 50 | 120 | ns |
| Output Voltage with UVLO Activated $\left(\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}, \mathrm{I}_{\text {Sink }}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {O(UVLO) }}$ | - | 0.1 | 0.5 | V |

RESTART TIMER

| Restart Time Delay | $t_{\text {DLY }}$ | 200 | 620 | - | $\mu \mathrm{s}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNDERVOLTAGE LOCKOUT |  |  |  |  |  |
| Startup Threshold (VCC Increasing) | $V_{\text {th(on) }}$ | 11.5 | 13 | 14.5 | V |
| Minimum Operating Voltage After Turn-On ( $\mathrm{V}_{\mathrm{CC}}$ Decreasing) | $\mathrm{V}_{\text {Shutdown }}$ | 7.0 | 8.0 | 9.0 | V |
| Hysteresis | $\mathrm{V}_{\mathrm{H}}$ | 3.8 | 5.0 | 6.2 | V |

TOTAL DEVICE

| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ |  |  | mA |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Startup $\left(\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}\right)$ |  | - | 0.25 | 0.4 |  |
| Operating |  | - | 6.5 | 12 |  |
| Dynamic Operating $\left(50 \mathrm{kHz}, \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}\right)$ |  | - | 9.0 | 20 |  |
| Power Supply Zener Voltage $\left(\mathrm{I}_{\mathrm{CC}}=25 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{Z}}$ | 30 | 36 | - | V |

NOTES: 1. Maximum package power dissipation limits must be observed. 2. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the startup threshold before setting to 12 V .
3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34262 $=-40^{\circ} \mathrm{C}$ for MC33262
$\mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$ for MC34262
$=+105^{\circ} \mathrm{C}$ for MC33262
4. $\mathrm{K}=\frac{\text { Pin } 4 \text { Threshold }}{\mathrm{V}_{\text {Pin } 3}\left(\mathrm{~V}_{\text {Pin 2 }}-\mathrm{V}_{\text {th }}(\mathrm{M})\right)}$
5. This parameter is measured with $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$, and $\mathrm{V}_{\text {Pin } 3}=3.0$

Figure 21. Current Sense Input Threshold versus Multiplier Input


Figure 22. Current Sense Input Threshold versus Multiplier Input, Expanded View



Figure 25. Error Amp Transconductance and Phase versus Frequency


Figure 24. Overvoltage Comparator Input Threshold versus Temperature


Figure 26. Error Amp Transient Response


Figure 27. Quickstart Charge Current versus Temperature


Figure 28. Restart Timer Delay versus Temperature


Figure 29. Zero Current Detector Input Threshold Voltage versus Temperature


Figure 31. Drive Output Waveform


100 ns/DIV

Figure 33. Supply Current versus Supply Voltage


Figure 30. Output Saturation Voltage versus Load Current


Figure 32. Drive Output Cross Conduction


Figure 34. Undervoltage Lockout Thresholds versus Temperature


## FUNCTIONAL DESCRIPTION

## Introduction

With the goal of exceeding the requirements of legislation on line-current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple, cost-effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 15.

Figure 35. Uncorrected Power Factor Circuit


This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 16. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

Power factor correction can be achieved with the use of either a passive or an active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing, with the boost converter being the most popular topology, Figure 17. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to
appear resistive to the ac line, thus significantly reducing the harmonic current content.

Figure 36. Uncorrected Power Factor Input Waveforms


The MC34262, MC33262 are high performance, critical conduction, current-mode power factor controllers specifically designed for use in off-line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the ac line current sinusoidal and in phase with the line voltage.

## Operating Description

The MC34262, MC33262 contain many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 19, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. The reasons for these differences will become apparent in the following discussion. A description of each of the functional blocks is given below.

Figure 37. Active Power Factor Correction Preconverter


## Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage-to-current gain. The amplifier features a typical gm of $100 \mu \mathrm{mhos}$ (Figure 5). The noninverting input is internally biased at $2.5 \mathrm{~V} \pm 2.0 \%$ and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is $-0.5 \mu \mathrm{~A}$, which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor $\mathrm{R}_{2}$. The Error Amp output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz , so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amp monitors the average output voltage of the converter over several line cycles. The Error Amp output stage was designed to have a relatively constant transconductance over temperature. This allows the designer to define the compensated bandwidth over the intended operating temperature range. The output stage can sink and source $10 \mu \mathrm{~A}$ of current and is capable of swinging from 1.7 V to 6.4 V , assuring that the Multiplier can be driven over its entire dynamic range.

A key feature to using a transconductance type amplifier, is that the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of of the Voltage Feedback Input pin by the Error Amplifier and by the Overvoltage Comparator.

## Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to $1.08 \mathrm{~V}_{\text {ref }}$. In order to prevent false tripping during normal operation, the value of the output filter capacitor $C_{3}$ must be large enough to keep the peak-to-peak ripple less than $16 \%$ of the average dc output. The Overvoltage Comparator input to Drive Output turn-off propagation delay is typically 400 ns. A comparison of startup overshoot without and with the Overvoltage Comparator circuit is shown in Figure 23.

## Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac full wave rectified haversines are monitored at Pin 3
with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. The Multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0 V to 3.2 V for Pin 3, and 2.0 V to 3.75 V for Pin 2, Figure 1. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line, Figure 18. This has the effect of forcing the MOSFET on-time to track the input line voltage, resulting in a fixed Drive Output on-time, thus making the preconverter load appear to be resistive to the ac line. An approximation of the Current Sense Comparator threshold can be calculated from the following equation. This equation is accurate only under the given test condition stated in the electrical table.

$$
\mathrm{V}_{\mathrm{CS}} \text {, Pin } 4 \text { Threshold } \approx 0.65\left(\mathrm{~V}_{\text {Pin } 2}-\mathrm{V}_{\mathrm{th}(\mathrm{M})}\right) \mathrm{V}_{\text {Pin } 3}
$$

A significant reduction in line current distortion can be attained by forcing the preconverter to switch as the ac line voltage crosses through zero. The forced switching is achieved by adding a controlled amount of offset to the Multiplier and Current Sense Comparator circuits. The equation shown below accounts for the built-in offsets and is accurate to within ten percent. Let $\mathrm{V}_{\mathrm{th}(\mathrm{M})}=1.991 \mathrm{~V}$

$$
\begin{gathered}
V_{\text {CS }} \text {, Pin } 4 \text { Threshold }=0.544\left(V_{\text {Pin 2 }}-V_{\text {th }}(\mathrm{M})\right) \mathrm{V}_{\text {Pin } 3} \\
+0.0417\left(\mathrm{~V}_{\text {Pin 2 }}-\mathrm{V}_{\text {th }(\mathrm{M})}\right)
\end{gathered}
$$

## Zero Current Detector

The MC34262 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on-time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn-on until the inductor current reaches zero, the output rectifier reverse recovery time becomes less critical, allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous, thus limiting the peak switch to twice the average input current.
The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.4 V . To prevent false tripping, 200 mV of hysteresis is provided. Figure 9 shows that the thresholds are well-defined over temperature. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Current limit protection of the lower clamp transistor is provided in the event that the input pin is accidentally shorted to ground. The Zero Current Detector input to Drive Output turn-on propagation delay is typically 320 ns .

Figure 38. Inductor Current and MOSFET Gate Voltage Waveforms


## Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor $\mathrm{R}_{7}$ in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 4 where:

$$
\left.\mathrm{I}_{\mathrm{L}(\mathrm{pk}}\right)=\frac{\text { Pin } 4 \text { Threshold }}{\mathrm{R}_{7}}
$$

Abnormal operating conditions occur during preconverter startup at extremely high line or if output voltage sensing is lost. Under these conditions, the Multiplier output and Current Sense threshold will be internally clamped to 1.5 V . Therefore, the maximum peak switch current is limited to:

$$
\mathrm{I}_{\mathrm{pk}(\max )}=\frac{1.5 \mathrm{~V}}{\mathrm{R}_{7}}
$$

An internal RC filter has been included to attenuate any high frequency noise that may be present on the current waveform. This filter helps reduce the ac line current distortion especially near the zero crossings. With the component values shown in Figure 20, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac . The Current Sense Input to Drive Output turn-off propagation delay is typically less than 200 ns .

## Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand-alone applications. The Timer provides a means to
automatically start or restart the preconverter if the Drive Output has been off for more than $620 \mu$ s after the inductor current reaches zero. The restart time delay versus temperature is shown in Figure 8.

## Undervoltage Lockout and Quickstart

An Undervoltage Lockout comparator has been incorporated to guarantee that the IC is fully functional before enabling the output stage. The positive power supply terminal $\left(\mathrm{V}_{\mathrm{CC}}\right)$ is monitored by the UVLO comparator with the upper threshold set at 13 V and the lower threshold at 8.0 V . In the stand-by mode, with $\mathrm{V}_{\mathrm{CC}}$ at 7.0 V , the required supply current is less than 0.4 mA . This large hysteresis and low startup current allow the implementation of efficient bootstrap startup techniques, making these devices ideally suited for wide input range off-line preconverter applications. An internal 36 V clamp has been added from $\mathrm{V}_{\mathrm{CC}}$ to ground to protect the IC and capacitor $\mathrm{C}_{4}$ from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter. The supply current, startup, and operating voltage characteristics are shown in Figures 13 and 14.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor $\mathrm{C}_{1}$ will be discharged, holding the error amp output below the Multiplier threshold. This will prevent Drive Output switching and delay bootstrapping of capacitor $\mathrm{C}_{4}$ by diode $\mathrm{D}_{6}$. If Pin 2 does not reach the multiplier threshold before $\mathrm{C}_{4}$ discharges below the lower UVLO threshold, the converter will "hiccup" and experience a significant startup delay. The Quickstart circuit is designed to precharge $\mathrm{C}_{1}$ to 1.7 V , Figure 7 . This level is slightly below the Pin 2 Multiplier threshold, allowing immediate Drive Output switching and bootstrap operation when $\mathrm{C}_{4}$ crosses the upper UVLO threshold.

## Drive Output

The MC34262/MC33262 contain a single totem-pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to $\pm 500 \mathrm{~mA}$ peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull-down resistor. The totem-pole output has been optimized to minimize cross-conduction current during high speed operation. The addition of two $10 \Omega$ resistors, one in series with the source output transistor and one in series with the sink output transistor, helps to reduce the cross-conduction current and radiated noise by limiting the output rise and fall time. A 16 V clamp has been incorporated into the output stage to limit the high state $\mathrm{V}_{\mathrm{OH}}$. This prevents rupture of the MOSFET gate when $\mathrm{V}_{\mathrm{CC}}$ exceeds 20 V .

## APPLICATIONS INFORMATION

The application circuits shown in Figures 19, 20 and 21 reveal that few external components are required for a complete power factor preconverter. Each circuit is a peak detecting current-mode boost converter that operates in critical conduction mode with a fixed on-time and variable off-time. A major benefit of critical conduction operation is that the current loop is inherently stable, thus eliminating the need for ramp compensation. The application in Figure 19 operates over an input voltage range of 90 Vac to 138 Vac and provides an output power of $80 \mathrm{~W}(230 \mathrm{~V}$ at 350 mA ) with an associated power factor of approximately
0.998 at nominal line. Figures 20 and 21 are universal input preconverter examples that operate over a continuous input voltage range of 90 Vac to 268 Vac. Figure 20 provides an output power of $175 \mathrm{~W}(400 \mathrm{~V}$ at 440 mA$)$ while Figure 21 provides $450 \mathrm{~W}(400 \mathrm{~V}$ at 1.125 A$)$. Both circuits have an observed worst-case power factor of approximately 0.989 . The input current and voltage waveforms of Figure 20 are shown in Figure 22 with operation at 115 Vac and 230 Vac. The data for each of the applications was generated with the test set-up shown in Figure 24.

Table 1. Design Equations

| Notes | Calculation | Formula |
| :---: | :---: | :---: |
| Calculate the maximum required output power. | Required Converter Output Power | $\mathrm{P}_{\mathrm{O}}=\mathrm{V}_{\mathrm{O}} \mathrm{l}_{0}$ |
| Calculated at the minimum required ac line voltage for output regulation. Let the efficiency $\eta=0.92$ for low line operation. | Peak Inductor Current | $\mathrm{L}_{\mathrm{L}(\mathrm{pk})}=\frac{2 \sqrt{2} \mathrm{P}_{\mathrm{O}}}{\eta \operatorname{Vac}_{(\mathrm{LL})}}$ |
| Let the switching cycle $t=40 \mu$ s for universal input ( 85 to 265 Vac ) operation and $20 \mu \mathrm{~s}$ for fixed input ( 92 to 138 Vac , or 184 to 276 Vac ) operation. | Inductance | $\mathrm{L}_{\mathrm{P}}=\frac{\mathrm{t}\left(\frac{\mathrm{~V}_{\mathrm{O}}}{\sqrt{2}}-\mathrm{Vac}_{(\mathrm{LL})}\right) \eta \operatorname{Vac}_{(\mathrm{LL})}{ }^{2}}{\sqrt{2} \mathrm{~V}_{\mathrm{O}} \mathrm{P}_{\mathrm{O}}}$ |
| In theory the on-time $\mathrm{t}_{\mathrm{on}}$ is constant. In practice $\mathrm{t}_{\mathrm{on}}$ tends to increase at the ac line zero crossings due to the charge on capacitor $\mathrm{C}_{5}$. Let $\mathrm{Vac}=\mathrm{Vac}_{(\mathrm{LL})}$ for initial $\mathrm{t}_{\mathrm{on}}$ and $\mathrm{t}_{\text {off }}$ calculations. | Switch On-Time | $\mathrm{t}_{\mathrm{on}}=\frac{2 \mathrm{P}_{\mathrm{O}} \mathrm{LP}}{\eta \mathrm{Vac}^{2}}$ |
| The off-time $t_{\text {off }}$ is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta ( $\theta$ ) represents the angle of the ac line voltage. | Switch Off-Time | $\mathrm{t}_{\mathrm{off}}=\frac{\mathrm{t}_{\mathrm{on}}}{\frac{\mathrm{~V}_{\mathrm{O}}}{\sqrt{2} \mathrm{Vac}\|\operatorname{Sin} \theta\|}-1}$ |
| The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, $t_{\text {off }}$ approaches zero producing an increase in switching frequency. | Switching Frequency | $f=\frac{1}{t_{\text {on }}+t_{\text {off }}}$ |
| Set the current sense threshold $\mathrm{V}_{\mathrm{CS}}$ to 1.0 V for universal input ( 85 Vac to 265 Vac ) operation and to 0.5 V for fixed input ( 92 Vac to 138 Vac , or 184 Vac to 276 Vac ) operation. Note that $\mathrm{V}_{\mathrm{CS}}$ must be <1.4 V. | Peak Switch Current | $\mathrm{R}_{7}=\frac{\mathrm{V}_{\mathrm{CS}}}{\mathrm{I}_{\mathrm{L}(\mathrm{pk})}}$ |
| Set the multiplier input voltage $\mathrm{V}_{\mathrm{M}}$ to 3.0 V at high line. Empirically adjust $\mathrm{V}_{\mathrm{M}}$ for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line. | Multiplier Input Voltage | $V_{M}=\frac{\operatorname{Vac} \sqrt{2}}{\left(\frac{R_{5}}{R_{3}}+1\right)}$ |
| The $I_{\mathrm{IB}} \mathrm{R}_{1}$ error term can be minimized with a divider current in excess of $50 \mu \mathrm{~A}$. | Converter Output Voltage | $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\text {ref }}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)-\mathrm{I}_{\mathrm{IB}} \mathrm{R}_{2}$ |
| The calculated peak-to-peak ripple must be less than $16 \%$ of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator text. ESR is the equivalent series resistance of $\mathrm{C}_{3}$ | Converter Output Peak to Peak Ripple Voltage | $\Delta \mathrm{V}_{\mathrm{O}(\mathrm{pp})}=\mathrm{I}_{\mathrm{O}} \sqrt{\left(\frac{1}{2 \pi \mathrm{f}_{\mathrm{ac}} \mathrm{C}_{3}}\right)^{2}+\mathrm{ESR}^{2}}$ |
| The bandwidth is typically set to 20 Hz . When operating at high ac line, the value of $\mathrm{C}_{1}$ may need to be increased. (See Figure 25) | Error Amplifier Bandwidth | $\mathrm{BW}=\frac{\mathrm{gm}}{2 \pi \mathrm{C}_{1}}$ |

The following converter characteristics must be chosen:

$$
\begin{array}{cc}
\mathrm{V}_{\mathrm{O}}-\text { Desired output voltage } & \mathrm{Vac}-\mathrm{AC} \text { RMS line voltage } \\
\mathrm{I}_{\mathrm{O}}-\text { Desired output current } & \mathrm{Vac}_{(\mathrm{LL})}-\mathrm{AC} R \mathrm{RMS} \text { low line voltage } \\
\Delta \mathrm{V}_{\mathrm{O}}-\text { Converter output peak-to-peak ripple voltage }
\end{array}
$$

Figure 39. 80 W Power Factor Controller


Power Factor Controller Test Data

| AC Line Input |  |  |  |  |  |  |  |  | DC Output |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Current Harmonic Distortion (\% $l_{\text {fund }}$ ) |  |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {rms }}$ | $\mathrm{P}_{\text {in }}$ | PF | $\mathrm{I}_{\text {fund }}$ | THD | 2 | 3 | 5 | 7 | $\mathrm{V}_{\mathrm{O}(\mathrm{pp})}$ | $\mathrm{V}_{0}$ | 10 | Po | $\eta(\%)$ |
| 90 | 85.9 | 0.999 | 0.93 | 2.6 | 0.08 | 1.6 | 0.84 | 0.95 | 4.0 | 230.7 | 0.350 | 80.8 | 94.0 |
| 100 | 85.3 | 0.999 | 0.85 | 2.3 | 0.13 | 1.0 | 1.2 | 0.73 | 4.0 | 230.7 | 0.350 | 80.8 | 94.7 |
| 110 | 85.1 | 0.998 | 0.77 | 2.2 | 0.10 | 0.58 | 1.5 | 0.59 | 4.0 | 230.7 | 0.350 | 80.8 | 94.9 |
| 120 | 84.7 | 0.998 | 0.71 | 3.0 | 0.09 | 0.73 | 1.9 | 0.58 | 4.1 | 230.7 | 0.350 | 80.8 | 95.3 |
| 130 | 84.4 | 0.997 | 0.65 | 3.9 | 0.12 | 1.7 | 2.2 | 0.61 | 4.1 | 230.7 | 0.350 | 80.8 | 95.7 |
| 138 | 84.1 | 0.996 | 0.62 | 4.6 | 0.16 | 2.4 | 2.3 | 0.60 | 4.1 | 230.7 | 0.350 | 80.8 | 96.0 |

This data was taken with the test set-up shown in Figure 24.
T = Coilcraft N2881-A
Primary: 62 turns of \# 22 AWG
Secondary: 5 turns of \# 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: $0.072^{\prime \prime}$ total for a primary inductance (Lp) of $320 \mu \mathrm{H}$
Heatsink = AAVID Engineering Inc. 590302B03600, or 593002B03400

Figure 40. 175 W Universal Input Power Factor Controller


Power Factor Controller Test Data

| AC Line Input |  |  |  |  |  |  |  |  | DC Output |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Current Harmonic Distortion (\% $l_{\text {fund }}$ ) |  |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {rms }}$ | $\mathrm{P}_{\text {in }}$ | PF | $\mathrm{I}_{\text {fund }}$ | THD | 2 | 3 | 5 | 7 | $\mathrm{V}_{\text {O(pp) }}$ | $\mathrm{V}_{\mathrm{O}}$ | 10 | Po | $\eta$ (\%) |
| 90 | 193.3 | 0.991 | 2.15 | 2.8 | 0.18 | 2.6 | 0.55 | 1.0 | 3.3 | 402.1 | 0.44 | 176.9 | 91.5 |
| 120 | 190.1 | 0.998 | 1.59 | 1.6 | 0.10 | 1.4 | 0.23 | 0.72 | 3.3 | 402.1 | 0.44 | 176.9 | 93.1 |
| 138 | 188.2 | 0.999 | 1.36 | 1.2 | 0.12 | 1.3 | 0.65 | 0.80 | 3.3 | 402.1 | 0.44 | 176.9 | 94.0 |
| 180 | 184.9 | 0.998 | 1.03 | 2.0 | 0.10 | 0.49 | 1.2 | 0.82 | 3.4 | 402.1 | 0.44 | 176.9 | 95.7 |
| 240 | 182.0 | 0.993 | 0.76 | 4.4 | 0.09 | 1.6 | 2.3 | 0.51 | 3.4 | 402.1 | 0.44 | 176.9 | 97.2 |
| 268 | 180.9 | 0.989 | 0.69 | 5.9 | 0.10 | 2.3 | 2.9 | 0.46 | 3.4 | 402.1 | 0.44 | 176.9 | 97.8 |

This data was taken with the test set-up shown in Figure 24.
T = Coilcraft N2880-A
Primary: 78 turns of \# 16 AWG
Secondary: 6 turns of \# 18 AWG
Core: Coilcraft PT4215, EE 42-15
Gap: 0.104 " total for a primary inductance ( $L_{P}$ ) of $870 \mu \mathrm{H}$
Heatsink = AAVID Engineering Inc. 590302B03600

Figure 41. 450 W Universal Input Power Factor Controller


Power Factor Controller Test Data

| AC Line Input |  |  |  |  |  |  |  |  | DC Output |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Current Harmonic Distortion (\% $\mathrm{I}_{\text {fund }}$ ) |  |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {rms }}$ | $\mathrm{P}_{\text {in }}$ | PF | $1_{\text {fund }}$ | THD | 2 | 3 | 5 | 7 | $\mathrm{V}_{\mathrm{O}(\mathrm{pp})}$ | $\mathrm{V}_{\mathrm{O}}$ | 10 | Po | $\eta(\%)$ |
| 90 | 489.5 | 0.990 | 5.53 | 2.2 | 0.10 | 1.5 | 0.25 | 0.83 | 8.8 | 395.5 | 1.14 | 450.9 | 92.1 |
| 120 | 475.1 | 0.998 | 3.94 | 2.5 | 0.12 | 0.29 | 0.62 | 0.52 | 8.8 | 395.5 | 1.14 | 450.9 | 94.9 |
| 138 | 470.6 | 0.998 | 3.38 | 2.1 | 0.06 | 0.70 | 1.1 | 0.41 | 8.8 | 395.5 | 1.14 | 450.9 | 95.8 |
| 180 | 463.4 | 0.998 | 2.57 | 4.1 | 0.21 | 2.0 | 1.6 | 0.71 | 8.9 | 395.5 | 1.14 | 450.9 | 97.3 |
| 240 | 460.1 | 0.996 | 1.91 | 4.8 | 0.14 | 4.3 | 2.2 | 0.63 | 8.9 | 395.5 | 1.14 | 450.9 | 98.0 |
| 268 | 459.1 | 0.995 | 1.72 | 5.8 | 0.10 | 5.0 | 2.5 | 0.61 | 8.9 | 395.5 | 1.14 | 450.9 | 98.2 |

This data was taken with the test set-up shown in Figure 24.
T = Coilcraft P3657-A
Primary: 38 turns Litz wire, 1300 strands of \#48 AWG, Kerrigan-Lewis, Chicago, IL
Secondary: 3 turns of \# 20 AWG
Core: Coilcraft PT4220, EE 42-20
Gap: $0.180^{\prime \prime}$ total for a primary inductance (Lp) of $190 \mu \mathrm{H}$
Heatsink $=$ AAVID Engineering Inc. 604953 B04000 Extrusion

Figure 42. Power Factor Corrected Input Waveforms
(Figure 20 Circuit)


Figure 43. Output Voltage Startup Overshoot
(Figure 20 Circuit)


Figure 44. Power Factor Test Set-Up


An RFI filter is required for best performance when connecting the preconverter directly to the ac line. The filter attenuates the level of high frequency switching that appears on the ac line current waveform. Figures 19 and 20 work well with commercially available two stage filters such as the Delta Electronics 03DPCG5. Shown above is a single stage test filter that can easily be constructed with four ac line rated capacitors and a common-mode transformer. Coilcraft CMT3-28-2 was used to test Figures 19 and 20. It has a minimum inductance of 28 mH and a maximum current rating of 2.0 A . Coilcraft CMT4-17-9 was used to test Figure 21. It has a minimum inductance of 17 mH and a maximum current rating of 9.0 A. Circuit conversion efficiency $\eta(\%)$ was calculated without the power loss of the RFI filter.

Figure 45. Error Amp Compensation


The Error Amp output is a high impedance node and is susceptible to noise pickup. To minimize pickup, compensation capacitor $\mathrm{C}_{1}$ must be connected as close to Pin 2 as possible with a short, heavy ground returning directly to $\operatorname{Pin} 6$. When operating at high ac line, the voltage at Pin 2 may approach the lower threshold of the Multiplier, $\approx 2.0 \mathrm{~V}$. If there is excessive ripple on Pin 2, the Multiplier will be driven into cut-off causing circuit instability, high distortion and poor power factor. This problem can be eliminated by increasing the value of $C_{1}$.

Figure 46. Current Waveform Spike Suppression

A narrow turn-on spike is usually present on the leading edge of the current waveform and can cause circuit instability. The MC34262 provides an internal RC filter with a time constant of 220 ns . An additional external RC filter may be required in universal input applications that are above 200 W . It is suggested that the external filter be placed directly at the Current Sense Input and have a time constant that approximates the spike duration.


Figure 47. Negative Current Waveform Spike Suppression


A negative turn-off spike can be observed on the trailing edge of the current waveform. This spike is due to the parasitic inductance of resistor $\mathrm{R}_{7}$, and if it is excessive, it can cause circuit instability. The addition of Schottky diode $D_{1}$ can effectively clamp the negative spike. The addition of the external RC filter shown in Figure 26 may provide sufficient spike attenuation.

Figure 48. Printed Circuit Board and Component Layout
(Circuits of Figures 15 and 16)


## MC33260

## GreenLine ${ }^{\text {TM }}$ Compact Power Factor Controller: Innovative Circuit for Cost Effective Solutions

The MC33260 is a controller for Power Factor Correction preconverters meeting international standard requirements in electronic ballast and off-line power conversion applications. Designed to drive a free frequency discontinuous mode, it can also be synchronized and in any case, it features very effective protections that ensure a safe and reliable operation.

This circuit is also optimized to offer extremely compact and cost effective PFC solutions. While it requires a minimum number of external components, the MC33260 can control the follower boost operation that is an innovative mode allowing a drastic size reduction of both the inductor and the power switch. Ultimately, the solution system cost is significantly lowered.

Also able to function in a traditional way (constant output voltage regulation level), any intermediary solutions can be easily implemented. This flexibility makes it ideal to optimally cope with a wide range of applications.

## General Features

- Standard Constant Output Voltage or "Follower Boost" Mode
- Switch Mode Operation: Voltage Mode
- Latching PWM for Cycle-by-Cycle On-Time Control
- Constant On-Time Operation That Saves the Use of an Extra Multiplier
- Totem Pole Output Gate Drive
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Improved Regulation Block Dynamic Behavior
- Synchronization Capability
- Internally Trimmed Reference Current Source


## Safety Features

- Overvoltage Protection: Output Overvoltage Detection
- Undervoltage Protection: Protection Against Open Loop
- Effective Zero Current Detection
- Accurate and Adjustable Maximum On-Time Limitation
- Overcurrent Protection
- ESD Protection on Each Pin


## TYPICAL APPLICATION



## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com
MARKING DIAGRAMS


DIP-8 P SUFFIX CASE 626


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33260P | Plastic DIP-8 | 50 Units/Rail |
| MC33260D | SO-8 | 98 Units/Rail |
| MC33260DR2 | SO-8 | 2500 Tape \& Reel |

BLOCK DIAGRAM


MAXIMUM RATINGS

| Rating | $\begin{aligned} & \text { Pin \# } \\ & \text { DIP-8 } \end{aligned}$ | $\begin{aligned} & \text { Pin \# } \\ & \text { SO-8 } \end{aligned}$ | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gate Drive Current* Source Sink | 7 | 5 | $\mathrm{I}_{\mathrm{O}}$ (Source) $\mathrm{I}_{\text {(Sink) }}$ | $\begin{gathered} -500 \\ 500 \end{gathered}$ | mA |
| $\mathrm{V}_{\text {CC }}$ Maximum Voltage | 8 | 6 | $(\mathrm{Vcc})_{\text {max }}$ | 16 | V |
| Input Voltage |  |  | $\mathrm{V}_{\text {in }}$ | -0.3 to +10 | V |
| Power Dissipation and Thermal Characteristics <br> P Suffix, DIP Package <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ <br> Thermal Resistance Junction to Air |  |  | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{JJA}} \end{gathered}$ | $\begin{aligned} & 600 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature |  |  | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature |  |  | $\mathrm{T}_{\text {A }}$ | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right.$ for typical values, $\mathrm{T}_{J}=-40$ to $105^{\circ} \mathrm{C}$ for min $/ \mathrm{max}$ values unless otherwise noted.)

| Characteristic | Pin \# <br> DIP-8 | Pin \# <br> SO-8 | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## GATE DRIVE SECTION

| ```Gate Drive Resistor Source Resistor @ IDrive = 100 mA Sink Resistor @ IDrive= 100 mA``` | 7 | 5 | ROL $\mathrm{R}_{\mathrm{OH}}$ | $\begin{gathered} 10 \\ 5 \end{gathered}$ | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | 35 25 | $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Gate Drive Voltage Rise Time (From 3.0 V Up to 9.0 V) (Note 1) | 7 | 5 | $t_{r}$ | - | 50 | - | ns |
| Output Voltage Falling Time (From 9.0 V Down to 3.0 V ) (Note 1) | 7 | 5 | $t_{f}$ | - | 50 | - | ns |

## OSCILLATOR SECTION

| Maximum Oscillator Swing | 3 | 1 | $\Delta \mathrm{V}_{\mathrm{T}}$ | 1.4 | 1.5 | 1.6 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Charge Current @ $\mathrm{I}_{\text {FB }}=100 \mu \mathrm{~A}$ | 3 | 1 | $I_{\text {charge }}$ | 87.5 | 100 | 112.5 | $\mu \mathrm{A}$ |
| Charge Current @ $\mathrm{I}_{\mathrm{FB}}=200 \mu \mathrm{~A}$ | 3 | 1 | $\mathrm{I}_{\text {charge }}$ | 350 | 400 | 450 | $\mu \mathrm{A}$ |
| Ratio Multiplier Gain Over Maximum Swing <br> $@ I_{F B}=100 \mu \mathrm{~A}$ | 3 | 1 | $\mathrm{K}_{\text {osc }}$ | 5600 | 6400 | 7200 | 1/(V.A) |
| Ratio Multiplier Gain Over Maximum Swing <br> @ $\mathrm{I}_{\mathrm{FB}}=200 \mu \mathrm{~A}$ | 3 | 1 | $\mathrm{K}_{\text {osc }}$ | 5600 | 6400 | 7200 | 1/(V.A) |
| Average Internal Oscillator Pin Capacitance Over Oscillator Maximum Swing ( $\mathrm{C}_{\mathrm{T}}$ Voltage Varying From 0 Up to 1.5 V ) (Note 2) | 3 | 1 | $\mathrm{C}_{\text {int }}$ | 10 | 15 | 20 | pF |
| Discharge Time ( $\mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}$ ) | 3 | 1 | $\mathrm{T}_{\text {disch }}$ | - | 0.5 | 1.0 | $\mu \mathrm{s}$ |

## REGULATION SECTION

| Regulation High Current Reference | 1 | 7 | $\mathrm{I}_{\text {reg-H }}$ | 192 | 200 | 208 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ratio (Regulation Low Current Reference) $/ I_{\text {reg-H }}$ | 1 | 7 | $\mathrm{I}_{\text {reg-L }} / I_{\text {reg-H }}$ | 0.965 | 0.97 | 0.98 | - |
| $\mathrm{V}_{\text {control }}$ Impedance | 1 | 7 | $\mathrm{Z}_{\mathrm{Vcontrol}}$ | - | 300 | - | $\mathrm{k} \Omega$ |
| Feedback Pin Clamp Voltage $@ \mathrm{I}_{\mathrm{FB}}=100 \mu \mathrm{~A}$ | 1 | 7 | $\mathrm{~V}_{\mathrm{FB}-100}$ | 1.5 | 2.1 | 2.5 | V |
| Feedback Pin Clamp Voltage @ $\mathrm{I}_{\mathrm{FB}}=200 \mu \mathrm{~A}$ | 1 | 7 | $\mathrm{~V}_{\mathrm{FB}-200}$ | 2.0 | 2.6 | 3.0 | V |

NOTE: $\mathrm{I}_{\mathrm{FB}}$ is the current that is drawn by the Feedback Input pin.

1. 1.0 nF being connected between the pin 7 and ground for DIP-8, between Pin 5 and ground for SO-8.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right.$ for typical values, $\mathrm{T}_{J}=-40$ to $105^{\circ} \mathrm{C}$ for $\mathrm{min} / \mathrm{max}$ values unless otherwise noted.)

| Characteristic | Pin \# <br> DIP-8 | Pin \# <br> SO-8 | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## CURRENT SENSE SECTION

| Zero Current Detection Comparator Threshold | 4 | 2 | $\mathrm{V}_{\text {ZCD-th }}$ | -90 | -60 | -30 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Negative Clamp Level ( $\mathrm{I}_{\text {CS-pin }}=-1.0 \mathrm{~mA}$ ) | 4 | 2 | $\mathrm{Cl}-$ neg | - | -0.7 | - | V |
| Bias Current @ Vcs = V ${ }_{\text {ZCD-th }}$ | 4 | 2 | $\mathrm{l}_{\mathrm{b}-\mathrm{cs}}$ | -0.2 | - | - | $\mu \mathrm{A}$ |
| Propagation Delay (Vcs > V $\mathrm{ZCD-th}$ ) to Gate Drive High | 7 | 5 | $\mathrm{T}_{\mathrm{ZCD}}$ | - | 500 | - | ns |
| Current Sense Pin Internal Current Source | 4 | 2 | locp | 192 | 205 | 218 | $\mu \mathrm{A}$ |
| Leading Edge Blanking Duration |  |  | $\tau_{\text {LEB }}$ | - | 400 | - | ns |
| OverCurrent Protection Propagation Delay (Vcs < $\mathrm{V}_{\mathrm{ZcD}-\mathrm{th}}$ to Gate Drive Low) | 7 | 5 | T OCP | 100 | 160 | 240 | ns |

## SYNCHRONIZATION SECTION

| Synchronization Threshold |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIP-8 | 5 | - | $\mathrm{V}_{\text {sync-th }}$ | 0.8 | 1.0 | 1.2 | V |
| SO-8 | - | 3 | $\mathrm{~V}_{\text {sync-th }}$ | 0.8 | 1.0 | 1.4 | V |
| Negative Clamp Level ( $\mathrm{I}_{\text {sync }}=-1.0 \mathrm{~mA}$ ) | 5 | 3 | $\mathrm{Cl}-$ neg | - | -0.7 | - | V |
| Minimum Off-Time | 7 | 5 | $\mathrm{~T}_{\text {off }}$ | 1.5 | 2.1 | 2.7 | $\mu \mathrm{~s}$ |
| Minimum Required Synchronization Pulse Duration | 5 | 3 | $\mathrm{~T}_{\text {sync }}$ | - | - | 0.5 | $\mu \mathrm{~s}$ |

## OVERVOLTAGE PROTECTION SECTION

| OverVoltage Protection High Current Threshold and $I_{\text {reg-H }}$ Difference | 1 | 7 | $\mathrm{I}_{\text {OVP-H }}{ }^{-1} \mathrm{Ireg}-\mathrm{H}$ | 8.0 | 13 | 18 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OverVoltage Protection Low Current Threshold and $\mathrm{I}_{\text {reg-H }}$ Difference | 1 | 7 | lovp-L-Ireg-H | 0 | - | - | - |
| Ratio (lovp-H/lovp-L) | 1 | 7 | lovp-H/love-L | 1.02 | - | - | - |
| Propagation Delay ( $\mathrm{I}_{\mathrm{FB}}>110 \% \mathrm{I}_{\text {ref }}$ to Gate Drive Low) | 7 | 5 | Tovp | - | 500 | - | ns |

UNDERVOLTAGE PROTECTION SECTION

| Ratio (UnderVoltage Protection Current <br> Threshold) $/ I_{\text {reg-H }}$ | 1 | 7 | $I_{U V P /} / I_{\text {reg-H }}$ | 12 | 14 | 16 | $\%$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay (I $\mathrm{I}_{\mathrm{FB}}<12 \% \mathrm{I}_{\text {ref }}$ to Gate Drive Low) | 7 | 5 | $T_{\text {UVP }}$ | - | 500 | - | ns |

THERMAL SHUTDOWN SECTION

| Thermal Shutdown Threshold | 7 | 5 | $\mathrm{~T}_{\text {stdwn }}$ | - | 150 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Hysteresis | 7 | 5 | $\Delta \mathrm{~T}_{\text {stdwn }}$ | - | 30 | - | ${ }^{\circ} \mathrm{C}$ |

$\mathrm{V}_{\mathrm{cc}}$ UNDERVOLTAGE LOCKOUT SECTION

| Start-Up Threshold | 8 | 6 | $V_{\text {stup-th }}$ | 9.7 | 11 | 12.3 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Disable Voltage After Threshold Turn-On | 8 | 6 | $V_{\text {disable }}$ | 7.4 | 8.5 | 9.6 | V |

TOTAL DEVICE

| Power Supply Current | 8 | 6 | $I_{C C}$ |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Start-Up $\left(V_{C C}=5 \mathrm{~V}\right.$ with $\mathrm{V}_{\mathrm{CC}}$ Increasing $)$ |  |  |  | - | 0.1 | 0.25 | mA |
| Operating @ $\mathrm{I}_{\mathrm{FB}}=200 \mu \mathrm{~A}$ |  |  |  |  |  |  |  |

Vcs is the Current Sense Pin Voltage and $\mathrm{I}_{\mathrm{FB}}$ is the Feedback Pin Current

Pin Numbers are Relevant to the DIP-8 Version


Figure 1. Regulation Block Output versus Feedback Current


Figure 3. Maximum Oscillator Swing versus Temperature


Figure 5. Oscillator Charge Current versus Feedback Current


Figure 2. Regulation Block Output versus Feedback Current


Figure 4. Feedback Input Voltage versus Feedback Current


Figure 6. Oscillator Charge Current versus Temperature


Figure 7. Oscillator Charge Current versus Temperature


Figure 9. On-Time versus Feedback Current


Figure 11. $\left(l_{\text {ovpH }} / I_{\text {ref }}\right),\left(I_{\text {ovpL }} / I_{\text {ref }}\right),\left(I_{\text {regL }} / I_{\text {ref }}\right)$ versus Temperature


Figure 8. On-Time versus Feedback Current


Figure 10. Internal Current Sources versus Temperature


Figure 12. Undervoltage Ratio versus Temperature

Pin Numbers are Relevant to the DIP-8 Version


Figure 13. Current Sense Threshold versus Temperature


Figure 15. Oscillator Pin Internal Capacitance


Figure 17. Gate Drive Cross Conduction


Figure 14. Circuit Consumption versus Supply Voltage


Figure 16. Gate Drive Cross Conduction


Figure 18. Gate Drive Cross Conduction

PIN FUNCTION DESCRIPTION

| Pin No. DIP-8 | Pin No. SO-8 | Function | Description |
| :---: | :---: | :---: | :---: |
| 1 | 7 | Feedback Input | This pin is designed to receive a current that is proportional to the preconverter output voltage. This information is used for both the regulation and the overvoltage and undervoltage protections. The current drawn by this pin is internally squared to be used as oscillator capacitor charge current. |
| 2 | 8 | $\mathrm{V}_{\text {control }}$ | This pin makes available the regulation block output. The capacitor connected between this pin and ground, adjusts the control bandwidth. It is typically set below 20 Hz to obtain a nondistorted input current. |
| 3 | 1 | Oscillator Capacitor $\left(\mathrm{C}_{\mathrm{T}}\right)$ | The circuit uses an on-time control mode. This on-time is controlled by comparing the $\mathrm{C}_{\boldsymbol{T}}$ voltage to the $\mathrm{V}_{\text {control }}$ voltage. $\mathrm{C}_{\boldsymbol{T}}$ is charged by the squared feedback current. |
| 4 | 2 | Zero Current Detection Input | This pin is designed to receive a negative voltage signal proportional to the current flowing through the inductor. This information is generally built using a sense resistor. The Zero Current Detection prevents any restart as long as the pin 4 voltage is below $(-60 \mathrm{mV})$. This pin is also used to perform the peak current limitation. The overcurrent threshold is programmed by the resistor connected between the pin and the external current sense resistor. |
| 5 | 3 | Synchronization Input | This pin is designed to receive a synchronization signal. For instance, it enables to synchronize the PFC preconverter to the associated SMPS. If not used, this pin must be grounded. |
| 6 | 4 | Ground | This pin must be connected to the preregulator ground. |
| 7 | 5 | Gate Drive | The gate drive current capability is suited to drive an IGBT or a power MOSFET. |
| 8 | 6 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the IC. The circuit turns on when $\mathrm{V}_{\mathrm{CC}}$ becomes higher than 11 V , the operating range after start-up being 8.5 V up to 16 V . |

APPLICATION SCHEMATIC


## FUNCTIONAL DESCRIPTION Pin Numbers are Relevant to the DIP-8 Version <br> OPERATION DESCRIPTION

## INTRODUCTION

The need of meeting the requirements of legislation on line current harmonic content, results in an increasing demand for cost effective solutions to comply with the Power Factor regulations. This data sheet describes a monolithic controller specially designed for this purpose.

Most off-line appliances use a bridge rectifier associated to a huge bulk capacitor to derive raw dc voltage from the utility ac line.


Figure 19. Typical Circuit Without PFC
This technique results in a high harmonic content and in poor power factor ratios. In effect, the simple rectification technique draws power from the mains when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike. Consequently, a poor power factor (in the range of $0.5-0.7$ ) is generated, resulting in an apparent input power that is much higher than the real power.


Figure 20. Line Waveforms Without PFC
Active solutions are the most popular way to meet the legislation requirements. They consist of inserting a PFC pre-regulator between the rectifier bridge and the bulk capacitor. This interface is, in fact, a step-up SMPS that outputs a constant voltage while drawing a sinusoidal current from the line.


Figure 21. PFC Preconverter
The MC33260 was developed to control an active solution with the goal of increasing its robustness while lowering its global cost.

The MC33260 is optimized to just as well drive a free running as a synchronized discontinuous voltage mode.

It also features valuable protections (overvoltage and undervoltage protection, overcurrent limitation, ...) that make the PFC preregulator very safe and reliable while requiring very few external components. In particular, it is able to safely face any uncontrolled direct charges of the output capacitor from the mains which occur when the output voltage is lower than the input voltage (start-up, overload, ...).
In addition to the low count of elements, the circuit can control an innovative mode named "Follower Boost" that permits to significantly reduce the size of the preconverter inductor and power MOSFET. With this technique, the output regulation level is not forced to a constant value, but can vary according to the a.c. line amplitude and to the power. The gap between the output voltage and the ac line is then lowered, what allows the preconverter inductor and power MOSFET size reduction. Finally, this method brings a significant cost reduction.

A description of the functional blocks is given below.

## REGULATION SECTION

Connecting a resistor between the output voltage to be regulated and the pin 1, a feedback current is obtained. Typically, this current is built by connecting a resistor between the output voltage and the pin 1 . Its value is then given by the following equation:

$$
I_{\text {pin1 }}=\frac{V_{0}-V_{\text {pin1 }}}{R_{0}}
$$

where:
$\mathrm{R}_{\mathrm{O}}$ is the feedback resistor,
$\mathrm{V}_{\mathrm{o}}$ is the output voltage,
$\mathrm{V}_{\mathrm{pin} 1}$ is the pin 1 clamp value.
The feedback current is compared to the reference current so that the regulation block outputs a signal following the characteristic depicted in Figure 22. According to the power and the input voltage, the output voltage regulation level varies between two values $\left(\mathrm{V}_{\mathrm{o}}\right)_{\text {regL }}$ and $\left(\mathrm{V}_{\mathrm{o}}\right)_{\text {regH }}$ corresponding to the $I_{\text {regL }}$ and $I_{\text {regH }}$ levels.


Figure 22. Regulation Characteristic
The feedback resistor must be chosen so that the feedback current should equal the internal current source $I_{\text {regH }}$ when the output voltage exceeds the chosen upper regulation voltage $\left[\left(\mathrm{V}_{\mathrm{o}}\right)_{\text {regH }}\right]$. Consequently:

## Pin Numbers are Relevant to the DIP-8 Version

$$
\mathrm{R}_{\mathrm{O}}=\frac{\left(\mathrm{V}_{\mathrm{o}}\right)_{\mathrm{regH}}-\mathrm{V}_{\mathrm{pin} 1}}{\mathrm{I}_{\mathrm{reg}}}
$$

In practice, $\mathrm{V}_{\text {pin1 }}$ is small compared to $\left(\mathrm{V}_{\mathrm{o}}\right)_{\text {regH }}$ and this equation can be simplified as follows ( $\mathrm{I}_{\mathrm{regH}}$ being also replaced by its typical value $200 \mu \mathrm{~A}$ ):

$$
\mathrm{R}_{\mathrm{o}} \approx 5 \times\left(\mathrm{V}_{\mathrm{o}}\right)_{\mathrm{regH}}<\mathrm{k}^{>}
$$

The regulation block output is connected to the pin 2 through a $300 \mathrm{k} \Omega$ resistor. The pin 2 voltage $\left(\mathrm{V}_{\text {control }}\right)$ is compared to the oscillator sawtooth for PWM control.

An external capacitor must be connected between pin 2 and ground, for external loop compensation. The bandwidth is typically set below 20 Hz so that the regulation block output should be relatively constant over a given ac line cycle. This integration that results in a constant on-time over the ac line period, prevents the mains frequency output ripple from distorting the ac line current.

## OSCILLATOR SECTION

The oscillator consists of three phases:

- Charge Phase: The oscillator capacitor voltage grows up linearly from its bottom value (ground) until it exceeds $\mathrm{V}_{\text {control }}$ (regulation block output voltage). At that moment, the PWM latch output gets low and the oscillator discharge sequence is set.
- Discharge Phase: The oscillator capacitor is abruptly discharged down to its valley value $(0 \mathrm{~V})$.
- Waiting Phase: At the end of the discharge sequence, the oscillator voltage is maintained in a low state until the PWM latch is set again.


The oscillator charge current is dependent on the feedback current ( $\mathrm{I}_{\mathrm{o}}$ ). In effect

$$
I_{\text {charge }}=2 \times \frac{I_{0}^{2}}{I_{\text {ref }}}
$$

where:
$\mathrm{I}_{\text {charge }}$ is the oscillator charge current,
$\mathrm{I}_{0}$ is the feedback current (drawn by pin 1),
$\mathrm{I}_{\mathrm{ref}}$ is the internal reference current $(200 \mu \mathrm{~A})$.
So, the oscillator charge current is linked to the output voltage level as follows:

$$
I_{\text {charge }}=\frac{2 \times\left\langle v_{0}-v_{\text {pin1 }}\right\rangle^{2}}{R_{0}^{2} \times I_{\text {ref }}}
$$

where:
$\mathrm{V}_{\mathrm{o}}$ is the output voltage,
$\mathrm{R}_{\mathrm{O}}$ is the feedback resistor,
$\mathrm{V}_{\text {pin1 }}$ is the pin 1 clamp voltage.
In practice, $\mathrm{V}_{\text {pin1 }}$ that is in the range of 2.5 V , is very small compared to $\mathrm{V}_{\mathrm{o}}$. The equation can then be simplified by neglecting $\mathrm{V}_{\mathrm{pin} 1}$ :

$$
I_{\text {charge }} \approx \frac{2 \times \mathrm{V}_{0}^{2}}{\mathrm{R}_{\mathrm{o}}^{2} \times \mathrm{I}_{\mathrm{ref}}}
$$

It must be noticed that the oscillator terminal (pin 3) has an internal capacitance ( $\mathrm{C}_{\mathrm{int}}$ ) that varies versus the pin 3 voltage. Over the oscillator swing, its average value typically equals $15 \mathrm{pF}(\min 10 \mathrm{pF}$, max 20 pF ).

The total oscillator capacitor is then the sum of the internal and external capacitors.

$$
C_{\mathrm{pin3}}=\mathrm{C}_{\mathrm{T}}+\mathrm{C}_{\mathrm{int}}
$$

## PWM LATCH SECTION

The MC33260 operates in voltage mode: the regulation block output ( $\mathrm{V}_{\text {control }}$ - pin 2 voltage) is compared to the oscillator sawtooth so that the gate drive signal (pin 7) is high until the oscillator ramp exceeds $\mathrm{V}_{\text {control }}$.

The on-time is then given by the following equation:

$$
t_{\text {on }}=\frac{C_{\text {pin3 }} \times V_{\text {control }}}{I_{c h}}
$$

where:
$t_{\text {on }}$ is the on-time,
$\mathrm{C}_{\mathrm{pin} 3}$ is the total oscillator capacitor (sum of the internal and external capacitor),
$\mathrm{I}_{\text {charge }}$ is the oscillator charge current (pin 3 current),
$\mathrm{V}_{\text {control }}$ is the pin 2 voltage (regulation block output).
Consequently, replacing $\mathrm{I}_{\text {charge }}$ by the expression given in the Oscillator Section:

$$
\mathrm{t}_{\mathrm{on}}=\frac{\mathrm{R}_{\mathrm{o}}^{2} \times \mathrm{I}_{\mathrm{ref}} \times \mathrm{C}_{\mathrm{pin} 3} \times \mathrm{V}_{\text {control }}}{2 \times \mathrm{V}_{\mathrm{o}}^{2}}
$$

One can notice that the on-time depends on $V_{o}$ (preconverter output voltage) and that the on-time is maximum when Vcontrol is maximum (1.5 V typically).
At a given $\mathrm{V}_{\mathrm{o}}$, the maximum on-time is then expressed by the following equation:

$$
\left\langle\mathrm{t}_{\mathrm{on}}\right\rangle \max =\frac{\mathrm{C}_{\text {pin3 }} \times \mathrm{R}_{\mathrm{o}}^{2} \times \mathrm{I}_{\text {ref }} \times\left\langle\mathrm{V}_{\text {control }}\right\rangle_{\max }}{2 \times \mathrm{V}_{\mathrm{o}}^{2}}
$$

This equation can be simplified replacing

$$
\left\{2 /\left[\left(\mathrm{V}_{\text {contro }}\right)_{\max }{ }^{*} \mathrm{I}_{\text {ref }}\right]\right\} \text { by } \mathrm{K}_{\text {osc }}
$$

## Refer to Electrical Characteristics, Oscillator Section.

 Then:$$
\left\langle\mathrm{t}_{\mathrm{on}}\right\rangle \max =\frac{\mathrm{C}_{\mathrm{pin} 3} \times \mathrm{R}_{\mathrm{o}}^{2}}{\mathrm{~K}_{\mathrm{osc}} \times \mathrm{V}_{\mathrm{O}}^{2}}
$$

This equation shows that the maximum on-time is inversely proportional to the squared output voltage. This

## Pin Numbers are Relevant to the DIP-8 Version

property is used for follower boost operation (refer to Follower Boost section).

## CURRENT SENSE BLOCK

The inductor current is converted into a voltage by inserting a ground referenced resistor $\left(\mathrm{R}_{\mathrm{cs}}\right)$ in series with the input diodes bridge (and the input filtering capacitor). Therefore a negative voltage proportional to the inductor current is built:

$$
\mathrm{V}_{\mathrm{cs}}=-\left\langle\mathrm{R}_{\mathrm{cs}} \times \mathrm{I}_{\mathrm{L}}\right\rangle
$$

where:
$\mathrm{I}_{\mathrm{L}}$ is the inductor current,
$\mathrm{R}_{\mathrm{cs}}$ is the current sense resistor,
$\mathrm{V}_{\mathrm{cs}}$ is the measured $\mathrm{R}_{\mathrm{cs}}$ voltage.


Figure 24. Current Sensing
The negative signal $\mathrm{V}_{\text {cs }}$ is applied to the current sense through a resistor $\mathrm{R}_{\mathrm{OCP}}$. The pin is internally protected by a negative clamp $(-0.7 \mathrm{~V})$ that prevents substrate injection.

As long as the pin 4 voltage is lower than $(-60 \mathrm{mV})$, the Current Sense comparator resets the PWM latch to force the gate drive signal low state. In that condition, the power MOSFET cannot be on.

During the on-time, the pin 4 information is used for the overcurrent limitation while it serves the zero current detection during the off time.

## Zero Current Detection

The Zero Current Detection function guarantees that the MOSFET cannot turn on as long as the inductor current hasn't reached zero (discontinuous mode).

The pin 4 voltage is simply compared to the $(-60 \mathrm{mV})$ threshold so that as long as $\mathrm{V}_{\mathrm{cs}}$ is lower than this threshold, the circuit gate drive signal is kept in low state. Consequently, no power MOSFET turn on is possible until the inductor current is measured as smaller than $\left(60 \mathrm{mV} / \mathrm{R}_{\mathrm{cs}}\right)$ that is, the inductor current nearly equals zero.


Figure 25. Current Sense Block

## Overcurrent Protection

During the power switch conduction (i.e. when the Gate Drive pin voltage is high), a current source is applied to the pin 4. A voltage drop $\mathrm{V}_{\mathrm{OCP}}$ is then generated across the resistor $\mathrm{R}_{\mathrm{OCP}}$ that is connected between the sense resistor and the Current Sense pin (refer to Figure 25). So, instead of $\mathrm{V}_{\mathrm{cs}}$, the sum $\left(\mathrm{V}_{\mathrm{cs}}+\mathrm{V}_{\mathrm{OCP}}\right)$ is compared to $(-60 \mathrm{mV})$ and the maximum permissible current is the solution of the following equation:

$$
-\left\langle\mathrm{R}_{\mathrm{CS}} \times \mathrm{lpk}_{\max }\right\rangle+\mathrm{V}_{\mathrm{OCP}}=-60 \mathrm{mV}
$$

where:
$\mathrm{Ipk}_{\text {max }}$ is maximum allowed current,
$\mathrm{R}_{\mathrm{cs}}$ is the sensing resistor.
The overcurrent threshold is then:

$$
\mathrm{Ipk}_{\max }=\frac{\left\langle\mathrm{R}_{\mathrm{OCP}} \times \mathrm{I} \mathrm{OCP}\right\rangle+60 \times 10^{-3}}{\mathrm{R}_{\mathrm{CS}}}
$$

where:
$\mathrm{R}_{\mathrm{OCP}}$ is the resistor connected between the pin and the sensing resistor $\left(\mathrm{R}_{\mathrm{cs}}\right)$,
$\mathrm{I}_{\mathrm{OCP}}$ is the current supplied by the Current Sense pin when the gate drive signal is high (power switch conduction phase). I
Practically, the $\mathrm{V}_{\mathrm{OCP}}$ offset is high compared to 60 mV and the precedent equation can be simplified. The maximum current is then given by the following equation:

$$
\mathrm{lpk}_{\max } \approx \frac{\mathrm{R}_{\mathrm{OCP}}{ }^{<\mathrm{k}^{>}}}{\mathrm{R}_{\mathrm{CS}} \Omega^{\prime}} \times 0.205^{<\mathrm{A}^{>}}
$$

Consequently, the $\mathrm{R}_{\mathrm{OCP}}$ resistor can program the OCP level whatever the $\mathrm{R}_{\mathrm{cs}}$ value is. This gives a high freedom in the choice of $\mathrm{R}_{\mathrm{cs}}$. In particular, the inrush resistor can be utilized.

Pin Numbers are Relevant to the DIP-8 Version


Figure 26. PWM Latch

A LEB (Leading Edge Blanking) has been implemented. This circuitry disconnects the Current Sense comparator from pin 4 and disables it during the 400 first ns of the power switch conduction. This prevents the block from reacting on the current spikes that generally occur at power switch turn on. Consequently, proper operation does not require any filtering capacitor on pin 4.

## PROTECTIONS

## OCP (Overcurrent Protection)

Refer to Current Sense Block.

## OVP (Overvoltage Protection)

The feedback current ( $\mathrm{I}_{0}$ ) is compared to a threshold current $\left(\mathrm{I}_{\mathrm{ovpH}}\right)$. If it exceeds this value, the gate drive signal is maintained low until this current gets lower than a second level ( $\mathrm{I}_{\mathrm{ovpL}}$ ).


Figure 27. Internal Current Thresholds
So, the OVP upper threshold is:

$$
\mathrm{V}_{\mathrm{ovpH}}=\mathrm{V}_{\mathrm{pin} 1}+\left(\mathrm{R}_{\mathrm{o}} \times \mathrm{I}_{\mathrm{ovpH}}\right)
$$

where:
$\mathrm{R}_{\mathrm{o}}$ is the feedback resistor that is connected between pin 1 and the output voltage,
$\mathrm{I}_{\text {ovp-H }}$ is the internal upper OVP current threshold,
$\mathrm{V}_{\mathrm{pin} 1}$ is the pin 1 clamp voltage.

Practically, $\mathrm{V}_{\mathrm{pin} 1}$ that is in the range of 2.5 V , can be neglected. The equation can then be simplified:

$$
\mathrm{V}_{\mathrm{ovpH}}=\mathrm{R}_{\mathrm{o}}<_{\mathrm{M} \Omega^{>} \times \mathrm{I}_{\mathrm{ovpH}}}^{<\mu \mathrm{A}^{>}<_{\mathrm{V}}>}
$$

On the other hand, the OVP low threshold is:

$$
\mathrm{v}_{\mathrm{ovpL}}=\mathrm{V}_{\mathrm{pin} 1}+\left(\mathrm{R}_{\mathrm{o}} \times \mathrm{I}_{\mathrm{ovpL}}\right)
$$

where $\mathrm{I}_{\text {ovp-L }}$ is the internal low OVP current threshold. Consequently, $\mathrm{V}_{\text {pin1 }}$ being neglected:

$$
\mathrm{V}_{\mathrm{ovpL}}=\mathrm{R}_{\mathrm{o}}{ }^{<} \mathrm{M} \Omega^{>} \times \mathrm{I}_{\mathrm{ovpL}}{ }^{<} \mu \mathrm{A}^{>}<_{\mathrm{V}}{ }^{>}
$$

The OVP hysteresis prevents erratic behavior.
$\mathrm{I}_{\mathrm{ovpL}}$ is guaranteed to be higher than IregH (refer to parameters specification). This ensures that the OVP function doesn't interfere with the regulation one.

## UVP (Undervoltage Protection)

This function detects when the feedback current is lower than $14 \%$ of $\mathrm{I}_{\text {ref }}$. In this case, the PWM latch is reset and the power switch is kept off.

This protection is useful to:

- Protect the preregulator from working in too low mains conditions.
- To detect the feedback current absence (in case of a nonproper connection for instance).
The UVP threshold is:

$$
\mathrm{V}_{\mathrm{uvp}} \approx \mathrm{~V}_{\mathrm{pin} 1}+\left(\mathrm{R}_{\mathrm{o}}^{<} \mathrm{M}^{>} \times \mathrm{I}_{\mathrm{uvp}}{ }^{<} \mu \mathrm{A}^{>}\right)(\mathrm{V})
$$

Practically ( $\mathrm{V}_{\mathrm{pin} 1}$ being neglected),

$$
\mathrm{V}_{\mathrm{uvp}}=\mathrm{R}_{\mathrm{o}}^{<} \mathrm{M}^{>} \times \mathrm{I}_{\mathrm{uvp}}{ }^{<} \mu \mathrm{A}^{><}{ }_{\mathrm{V}}{ }^{>}
$$

## Maximum On-Time Limitation

As explained in PWM Latch, the maximum on-time is accurately controlled.

## Pin Protection

All the pins are ESD protected.

Pin Numbers are Relevant to the DIP-8 Version

In particular, a 11 V zener diode is internally connected between the terminal and ground on the following pins:

Feedback, $V_{\text {control }}$, Oscillator, Current Sense, and Synchronization.


Figure 28. Synchronization Arrangement

## SYNCHRONIZATION BLOCK

The MC33260 features two modes of operation:

- Free Running Discontinuous Mode: The power switch is turned on as soon as there is no current left in the inductor (Zero Current Detection). This mode is simply obtained by grounding the synchronization terminal (pin 5).
- Synchronization Mode: This mode is set as soon as a signal crossing the 1 V threshold, is applied to the pin 5. In this case, operation in free running can only be recovered after a new circuit start-up. In this mode, the power switch cannot turn on before the two following conditions are fulfilled.
- Still, the zero current must have been detected.
- The precedent turn on must have been followed by (at least) one synchronization raising edge crossing the 1 V threshold.
In other words, the synchronization acts to prolong the power switch off time.

Consequently, a proper synchronized operation requires that the current cycle (on-time + inductor demagnetization) is shorter than the synchronization period. Practically, the inductor must be chosen accordingly. Otherwise, the system will keep working in free running discontinuous mode. Figure 33 illustrates this behavior.

It must be noticed that whatever the mode is, a $2 \mu \mathrm{~s}$ minimum off-time is forced. This delay limits the switching frequency in light load conditions.

## OUTPUT SECTION

The output stage contains a totem pole optimized to minimize the cross conduction current during high speed
operation. The gate drive is kept in a sinking mode whenever the Undervoltage Lockout is active. The rise and fall times have been controlled to typically equal 50 ns while loaded by 1 nF .

## REFERENCE SECTION

An internal reference current source ( $\mathrm{I}_{\text {ref }}$ ) is trimmed to be $\pm 4 \%$ accurate over the temperature range (the typical value is $200 \mu \mathrm{~A}$ ). $\mathrm{I}_{\text {ref }}$ is the reference used for the regulation ( $\mathrm{I}_{\mathrm{regH}}$ $=\mathrm{I}_{\mathrm{ref}}$ ).

## UNDERVOLTAGE LOCKOUT SECTION

An Undervoltage Lockout comparator has been implemented to guarantee that the integrated circuit is operating only if its supply voltage $\left(\mathrm{V}_{\mathrm{CC}}\right)$ is high enough to enable a proper working. The UVLO comparator monitors the pin 8 voltage and when it exceeds 11 V , the device gets active. To prevent erratic operation as the threshold is crossed, 2.5 V of hysteresis is provided.

The circuit off state consumption is very low: in the range of $100 \mu \mathrm{~A} @ \mathrm{~V}_{\mathrm{CC}}=5 \mathrm{~V}$. This consumption varies versus $\mathrm{V}_{\mathrm{CC}}$ as the circuit presents a resistive load in this mode.

## THERMAL SHUTDOWN

An internal thermal circuitry is provided to disable the circuit gate drive and then to prevent it from oscillating, if the junction temperature exceeds $150^{\circ} \mathrm{C}$ typically.

The output stage is again enabled when the temperature drops below $120^{\circ} \mathrm{C}$ typically ( $30^{\circ} \mathrm{C}$ hysteresis).

## Pin Numbers are Relevant to the DIP-8 Version

FOLLOWER BOOST
Traditional PFC preconverters provide the load with a fixed and regulated voltage that generally equals 230 V or 400 V according to the mains type (U.S., European, or universal).

In the "Follower Boost" operation, the preconverter output regulation level is not fixed but varies linearly versus the ac line amplitude at a given input power.


Figure 29. Follower Boost Characteristics
This technique aims at reducing the gap between the output and the input voltages to minimize the boost efficiency degradation.

## Follower Boost Benefits

The boost presents two phases:

- The on-time during which the power switch is on. The inductor current grows up linearly according to a slope $\left(\mathrm{V}_{\text {in }} / \mathrm{L}_{\mathrm{p}}\right)$, where $\mathrm{V}_{\text {in }}$ is the instantaneous input voltage and $\mathrm{L}_{\mathrm{p}}$ the inductor value.
- The off-time during which the power switch is off. The inductor current decreases linearly according the slope $\left(V_{o}-V_{i n}\right) / L_{p}$, where $V_{o}$ is the output voltage. This sequence that terminates when the current equals zero, has a duration that is inversely proportional to the gap between the output and input voltages. Consequently, the off-time duration becomes longer in follower boost.
Consequently, for a given peak inductor current, the longer the off time, the smaller power switch duty cycle and then its conduction dissipation. This is the first benefit of this technique: the MOSFET on-time losses are reduced.

The increase of the off time duration also results in a switching frequency diminution (for a given inductor value). Given that in practise, the boost inductor is selected big enough to limit the switching frequency down to an acceptable level, one can immediately see the second benefit
of the follower boost: it allows the use of smaller, lighter and cheaper inductors compared to traditional systems.
Finally, this technique utilization brings a drastic system cost reduction by lowering the size and then the cost of both the inductor and the power switch.


Figure 30. Off-Time Duration Increase

## Follower Boost Implementation

In the MC33260, the on-time is differently controlled according to the feedback current level. Two areas can be defined:

- When the feedback current is higher than $\mathrm{I}_{\text {regL }}$ (refer to regulation section), the regulation block output ( $\mathrm{V}_{\text {control }}$ ) is modulated to force the output voltage to a desired value.
- On the other hand, when the feedback current is lower than $\mathrm{I}_{\text {regL }}$, the regulation block output and therefore, the on-time are maximum. As explained in PWM Latch Section, the on-time is then inversely proportional to the output voltage square. The Follower Boost is active in these conditions in which the on-time is simply limited by the output voltage level. Note: In this equation, the feedback pin voltage ( $\mathrm{V}_{\mathrm{pin} 1}$ ) is neglected compared to the output voltage (refer to the PWM Latch Section).

$$
\mathrm{t}_{\text {on }}=\left\langle\mathrm{t}_{\mathrm{on}}\right\rangle \max =\frac{\mathrm{C}_{\mathrm{pin} 3} \times \mathrm{R}_{\mathrm{o}}^{2}}{\mathrm{~K}_{\mathrm{osc}} \times \mathrm{V}_{\mathrm{o}}^{2}}
$$

where:
$\mathrm{C}_{\mathrm{pin} 3}$ is the total oscillator capacitor (sum of the internal and external capacitors $-\mathrm{C}_{\mathrm{int}}+\mathrm{C}_{\mathrm{T}}$ ),
$\mathrm{K}_{\mathrm{osc}}$ is the ratio (oscillator swing over oscillator gain),
$\mathrm{V}_{\mathrm{o}}$ is the output voltage,
$\mathrm{R}_{\mathrm{O}}$ is the feedback resistor.

## Pin Numbers are Relevant to the DIP-8 Version

On the other hand, the boost topology has its own rule that dictates the on-time necessary to deliver the required power:

$$
\mathrm{t}_{\mathrm{on}}=\frac{4 \times \mathrm{L}_{\mathrm{p}} \times \mathrm{P}_{\mathrm{in}}}{\mathrm{~V}_{\mathrm{pk}}^{2}}
$$

where:
$\mathrm{V}_{\mathrm{pk}}$ is the peak ac line voltage,
$\mathrm{L}_{\mathrm{p}}$ is the inductor value,
$P_{\text {in }}$ is the input power.
Combining the two equations, one can obtain the Follower Boost equation:

$$
\mathrm{V}_{\mathrm{o}}=\frac{\mathrm{R}_{0}}{2} \times \sqrt{\frac{\mathrm{C}_{\mathrm{pin} 3}}{\mathrm{~K}_{\mathrm{osc}} \times \mathrm{L}_{\mathrm{p}} \times P_{\mathrm{in}}}} \times \mathrm{V}_{\mathrm{pk}}
$$

Consequently, a linear dependency links the output voltage to the ac line amplitude at a given input power.


Figure 31. Follower Boost Characteristics
The behavior of the output voltage is depicted in Figures 31 and 32. In particular, Figure 31 illustrates how the output voltage converges to a stable equilibrium level. First, at a given ac line voltage, the on-time is dictated by the power demand. Then, the follower boost characteristic makes correspond one output voltage level to this on-time. Combining these two laws, it appears that the power level forces the output voltage.

One can notice that the system is fully stable:

- If an output voltage increase makes it move away from its equilibrium value, the on-time will immediately diminish according to the follower boost law. This will result in a delivered power decrease. Consequently, the supplied power being too low, the output voltage will decrease back,
- In the same way, if the output voltage decreases, more power will be transferred and then the output voltage will increase back.


Figure 32. Follower Boost Output Voltage

## Mode Selection

The operation mode is simply selected by adjusting the oscillator capacitor value. As shown in Figure 32, the output voltage first has an increasing linear characteristic versus the ac line magnitude and then is clamped down to the regulation value. In the traditional mode, the linear area must be rejected. This is achieved by dimensioning the oscillator capacitor so that the boost can deliver the maximum power while the output voltage equals its regulation level and this, whatever the given input voltage. Practically, that means that whatever the power and input voltage conditions are, the follower boost would generate output voltages values higher than the regulation level, if there was no regulation block.
In other words, if $\left(\mathrm{V}_{\mathrm{o}}\right)_{\text {regL }}$ is the low output regulation level:

$$
\left\langle V_{o}\right\rangle_{\text {regL }} \leq \frac{R_{0}}{2} \times \sqrt{\frac{C_{T}+C_{i n t}}{K_{o s c} \times L_{p} \times\left\langle P_{i n}\right\rangle \max }} \times V_{p k}
$$

Consequently,
$\mathrm{C}_{\mathrm{T}} \geq-\mathrm{C}_{\mathrm{int}}+\frac{4 \times \mathrm{K}_{\mathrm{osc}} \times \mathrm{L}_{\mathrm{p}} \times\left\langle\mathrm{P}_{\mathrm{in}}\right\rangle \max \times\left\langle\mathrm{V}_{\mathrm{o}}\right\rangle_{\mathrm{regL}}^{2}}{\mathrm{R}_{\mathrm{o}}^{2} \times \mathrm{V}_{\mathrm{pk}}^{2}}$
Using $\mathrm{I}_{\text {regL }}$ (regulation block current reference), this equation can be simplified as follows:

$$
\mathrm{C}_{\mathrm{T}} \geq-\mathrm{C}_{\mathrm{int}}+\frac{4 \times \mathrm{K}_{\mathrm{osc}} \times \mathrm{L}_{\mathrm{p}} \times\left\langle\mathrm{P}_{\mathrm{in}}\right\rangle \max \times \mathrm{I}_{\mathrm{regL}}^{2}}{\mathrm{~V}_{\mathrm{pk}}^{2}}
$$

In the Follower Boost case, the oscillator capacitor must be chosen so that the wished characteristics are obtained.

Consequently, the simple choice of the oscillator capacitor enables the mode selection.


Figure 33. Typical Waveforms

MAIN DESIGN EQUATIONS (Note 1)

| rms Input Current (lac) $\mathrm{I}_{\mathrm{ac}}=\frac{\mathrm{P}_{\mathrm{o}}}{\eta \times \mathrm{V}_{\mathrm{ac}}}$ | $\eta$ (preconverter efficiency) is generally in the range of $90-95 \%$. |
| :---: | :---: |
| Maximum Inductor Peak Current ((1 $\left.\mathrm{l}_{\mathrm{pk}}\right)$ max $)$ : $\left(\mathrm{I}_{\mathrm{pk}}\right) \max =\frac{2 \times \sqrt{2} \times\left(\mathrm{P}_{\mathrm{o}}\right) \max }{\eta \times V_{\mathrm{acLL}}}$ | $\left(\mathrm{I}_{\mathrm{pk}}\right) \mathrm{max}$ is the maximum inductor current. |
| Output Voltage Peak to Peak $100 \mathrm{~Hz}(120 \mathrm{~Hz})$ Ripple (( $\Delta \mathrm{Vo}) \mathrm{pk}-\mathrm{pk})$ : $\left(\Delta V_{o}\right)_{p k-p k}=\frac{P_{0}}{2 \pi \times f_{a c} \times C_{o} \times V_{o}}$ | $\mathrm{fac}_{\text {ac }}$ is the ac line frequency ( 50 or 60 Hz ) |
| $\begin{aligned} & \text { Inductor Value ( } \left.\mathrm{L}_{\mathrm{p}}\right): \\ & \mathrm{L}_{\mathrm{p}}=\frac{2 \times \mathrm{t} \times\left(\frac{\mathrm{V}_{\mathrm{o}}}{\sqrt{2}}-\mathrm{V}_{\mathrm{acLL}}\right) \times \mathrm{V}_{\mathrm{acLL}}{ }^{2}}{\mathrm{~V}_{\mathrm{o}} \times \mathrm{V}_{\mathrm{acLL}} \times\left(\mathrm{I}_{\mathrm{pk}}\right) \max } \end{aligned}$ | $t$ is the maximum switching period. ( $\mathrm{t}=40 \mu \mathrm{~s}$ ) for universal mains operation and ( $\mathrm{t}=20 \mu \mathrm{~s}$ ) for narrow range are generally used. |
| Maximum Power MOSFET Conduction Losses (( $\mathrm{p}_{\mathrm{on}}$ )max): $\left(\mathrm{P}_{\mathrm{on}}\right) \max \approx \frac{1}{3} \times(\text { Rds }) \mathrm{on} \times\left(\mathrm{I}_{\mathrm{pk}}\right) \max ^{2} \times\left[1-\frac{1.2 \times \mathrm{V}_{\mathrm{acLL}}}{\mathrm{~V}_{\mathrm{o}}}\right]$ | (Rds)on is the MOSFET drain source on-time resistor. <br> In Follower Boost, the ratio $\left(\mathrm{V}_{\text {acLL }} / \mathrm{V}_{0}\right)$ is higher. The on-time MOSFET losses are then reduced |
| Maximum Average Diode Current ( $\left(\mathrm{I}_{\mathrm{d}}\right)$ : $\left(I_{\mathrm{d}}\right) \max =\frac{\left(\mathrm{P}_{\mathrm{o}}\right) \max }{\left(\mathrm{V}_{\mathrm{o}}\right) \min }$ | The Average Diode Current depends on the power and on the output voltage. |
| Current Sense Resistor Losses ( $\mathrm{pR}_{\mathrm{cs}}$ ): $\mathrm{pR}_{\mathrm{cs}}=\frac{1}{6} \times(\mathrm{Rds}) \mathrm{on} \times\left(\mathrm{I}_{\mathrm{pk}}\right)^{2} \max$ | This formula indicates the required dissipation capability for $\mathrm{R}_{\text {cs }}$ (current sense resistor). |
| Over Current Protection Resistor ( $\mathrm{R}_{\mathrm{OCP}}$ ): $\mathrm{R}_{\mathrm{OCP}} \approx \frac{\mathrm{R}_{\mathrm{cs}} \times\left(\mathrm{I}_{\mathrm{pk}}\right) \max }{0.205}$ | The overcurrent threshold is adjusted by ROCP at a given $\mathrm{R}_{\mathrm{cs}}$. <br> $\mathrm{R}_{\mathrm{cs}}$ can be a preconverter inrush resistor |
| Oscillator External Capacitor Value ( $\mathrm{C}_{\mathrm{T}}$ ): <br> -Traditional Operation $\mathrm{C}_{\mathrm{T}} \geq-\mathrm{C}_{\mathrm{int}}+\frac{2 \times \mathrm{K}_{\mathrm{osc}} \times \mathrm{L}_{\mathrm{p}} \times\left(\mathrm{P}_{\mathrm{in}}\right) \max \times \mathrm{I}_{\mathrm{regL}}^{2}}{\mathrm{~V}_{\mathrm{ac}}^{2}}$ <br> - Follower Boost: $v_{o}=\frac{R_{0}}{2} \times \sqrt{\frac{C_{T}+C_{i n t}}{K_{o s c} \times L_{p} \times P_{i n}}} \times v_{p k}$ | The Follower Boost characteristic is adjusted by the $\mathrm{C}_{\mathrm{T}}$ choice. <br> The Traditional Mode is also selected by $\mathrm{C}_{\mathrm{T}}$. $\mathrm{C}_{\text {int }}$ is the oscillator pin internal capacitor. |
| Feedback Resistor ( $\mathrm{R}_{\mathrm{o}}$ ): $R_{O}=\frac{\left(V_{0}\right)_{\mathrm{reg}}-V_{F B}}{I_{\text {regH }}} \approx \frac{V_{0}}{200}$ | The output voltage regulation level is adjusted by $\mathrm{R}_{0}$. |

Note 1. The preconverter design requires the following characteristics specification:

- $\left(\mathrm{V}_{0}\right)_{\text {reg }}$ : desired output voltage regulation level
$-\left(\Delta \mathrm{V}_{0}\right)_{\text {pk-pk }}$ : admissible output peak to peak ripple voltage
- $P_{0}$ : desired output power
$-\mathrm{V}_{\mathrm{ac}}$ : ac rms operating line voltage
- $\mathrm{V}_{\mathrm{acLL}}$ : minimum ac rms operating line voltage
- $V_{F B}$ : feedback pin voltage


L1: Coilcraft N2881 - A (primary: 62 turns of \# 22 AWG - Secondary: 5 turns of \# 22 AWG Core: Coilcraft PT2510, EE 25 Gap: $0.072^{\prime \prime}$ total for a primary inductance (Lp) of $320 \mu \mathrm{H}$ )

Figure 34. 80 W Wide Mains Power Factor Corrector

POWER FACTOR CONTROLLER TEST DATA*

| AC Line Input |  |  |  |  |  |  |  |  |  | DC Output |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Current Harmonic Distortion (\% $\mathrm{I}_{\text {fund }}$ ) |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{V}_{\text {rms }}$ <br> (V) | $P_{\text {in }}$ <br> (W) | $\begin{aligned} & \text { PF } \\ & (-) \end{aligned}$ | Ifund (mA) | THD | H2 | H3 | H5 | H7 | H9 | $\mathrm{V}_{0}$ <br> (V) | $\Delta V_{0}$ <br> (V) | $\begin{gathered} \mathrm{I}_{0} \\ (\mathrm{~mA}) \end{gathered}$ | $P_{0}$ <br> (W) | $\begin{gathered} \eta \\ (\%) \end{gathered}$ |
| 90 | 88.2 | 0.991 | 990 | 8.1 | 0.07 | 5.9 | 4.3 | 1.5 | 1.7 | 181 | 31.2 | 440 | 79.6 | 90.2 |
| 110 | 86.3 | 0.996 | 782 | 7.0 | 0.05 | 2.7 | 5.7 | 1.1 | 0.8 | 222 | 26.4 | 360 | 79.9 | 92.6 |
| 135 | 85.2 | 0.995 | 642 | 8.2 | 0.03 | 1.5 | 6.8 | 1.1 | 1.5 | 265 | 20.8 | 300 | 79.5 | 93.3 |
| 180 | 87.0 | 0.994 | 480 | 9.5 | 0.16 | 4.0 | 6.5 | 3.1 | 4.0 | 360 | 16.0 | 225 | 81.0 | 93.1 |
| 220 | 84.7 | 0.982 | 385 | 15 | 0.5 | 8.4 | 7.8 | 5.3 | 1.9 | 379 | 14.0 | 210 | 79.6 | 94.4 |
| 240 | 85.3 | 0.975 | 359 | 16.5 | 0.7 | 9.0 | 7.8 | 7.4 | 3.8 | 384 | 14.0 | 210 | 80.6 | 94.5 |
| 260 | 84.0 | 0.967 | 330 | 18.8 | 0.7 | 11.0 | 7.0 | 9.0 | 4.0 | 392 | 13.2 | 205 | 80.4 | 95.7 |

[^24]

Figure 35. Circuit Supply Voltage

## MC33260 V Cc SUPPLY VOLTAGE

In some applications, the arrangement shown in Figure 35 must be implemented to supply the circuit. A start-up resistor is connected between the rectified voltage (or one-half wave) to charge the MC33260 $\mathrm{V}_{\mathrm{CC}}$ up to its start-up threshold (11 V typically). The MC33260 turns on and the $\mathrm{V}_{\mathrm{CC}}$ capacitor $\left(\mathrm{C}_{\mathrm{pin} 8}\right)$ starts to be charged by the PFC transformer auxiliary winding. A resistor, $r$ (in the range of $22 \Omega$ ) and a 15 V zener should be added to protect the circuit from excessive voltages.

When the PFC preconverter is loaded by an SMPS, the MC33260 should preferably be supplied by the SMPS itself. In this configuration, the SMPS starts first and the PFC gets active when the MC33260 $\mathrm{V}_{\mathrm{CC}}$ supplied by the power supply, exceeds the device start-up level. With this configuration, the PFC preconverter doesn't require any auxiliary winding and finally a simple coil can be used.

## PCB LAYOUT

The connections of the oscillator and $\mathrm{V}_{\text {control }}$ capacitors should be as short as possible.


Figure 36. Preconverter loaded by a Flyback SMPS: MC33260 VCC Supply

## MC33349

## Lithium Battery Protection Circuit for One Cell Battery Packs

The MC33349 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of a one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit detection, and a low current standby mode when the cell is discharged. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack.

- Internally Trimmed Charge and Discharge Voltage Limits
- Discharge Current Limit Detection
- Low Current Standby Mode when Cells are Discharged
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in a Low Profile Surface Mount Package


Figure 1. Typical One Cell Smart Battery Pack

## (a)

## ON Semiconductor ${ }^{\text {w }}$

 http://onsemi.com

## PIN CONNECTIONS



ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1170 of this data sheet.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (Pin 5 to Pin 6) | $\mathrm{V}_{\mathrm{DD}}$ | -0.3 to 12 | V |
| Input Voltage |  |  |  |
| P- Pin Voltage (Pin 5 to Pin 2) | $\mathrm{V}_{\mathrm{P}-}$ | $\mathrm{V}_{\mathrm{DD}}-28$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| Ct Pin (Pin 4 to Pin 6) | $\mathrm{V}_{\mathrm{Ct}}$ | $\mathrm{Gnd}-0.3$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| Output Voltage |  |  |  |
| CO Pin Voltage (Pin 3 to Pin 2) | $\mathrm{V}_{\mathrm{CO}}$ | $\mathrm{V}_{\mathrm{DD}}-28$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| DO Pin Voltage (Pin 1 to Pin 6) | $\mathrm{V}_{\mathrm{DO}}$ | $\mathrm{Gnd}-0.3$ to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | 150 | mW |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to 125 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{C}_{\mathrm{t}}=0.01 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating junction temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit | Note 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VOLTAGE SENSING |  |  |  |  |  |  |
| Cell Charging Cutoff (Pin 5 to Pin 6) Overvoltage Threshold, $\mathrm{V}_{\mathrm{DD}}$ Increasing $\begin{aligned} & \text {-3, -4 Suffix } \\ & -7 \text { Suffix } \end{aligned}$ <br> Overvoltage Hysteresis $\mathrm{V}_{\mathrm{DD}}$ Decreasing | $V_{D E T 1}$ $\mathrm{V}_{\mathrm{HYS}}$ | $\begin{aligned} & 4.2 \\ & 4.3 \\ & 150 \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.25 \\ & 4.35 \\ & 200 \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.3 \\ & 4.4 \\ & 250 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{mV} \end{gathered}$ | B |
| Cell Discharging Cutoff (Pin 5 to Pin 6) Undervoltage Threshold, $\mathrm{V}_{\mathrm{DD}}$ Decreasing | $\mathrm{V}_{\text {DET2 }}$ | 2.437 | 2.5 | 2.563 | V | C |
| Overvoltage Delay Time ( $\mathrm{C}_{\mathrm{t}}=0.01 \mu \mathrm{~F}, \mathrm{~V} D=3.6 \mathrm{~V}$ to 4.5 V ) | ${ }^{\text {( }}$ (EET1) | 55 | 80 | 105 | ms | B |
| Undervoltage Delay Time ( $\mathrm{V}_{\mathrm{DD}}=3.6 \mathrm{~V}$ to 2.4 V ) | ${ }^{\text {t }}$ (DET2) | 7.0 | 10 | 13 | ms | C |

## CURRENT SENSING

| Excess Current Threshold (Detect rising edge of P - pin voltage) $\begin{aligned} & -3,-7 \text { Suffix } \\ & -4 \text { Suffix } \end{aligned}$ | $V_{\text {DET3 }}$ | $\begin{gathered} 170 \\ 45 \end{gathered}$ | $\begin{gathered} 200 \\ 75 \end{gathered}$ | $\begin{aligned} & 230 \\ & 105 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ | D |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Short Protection Voltage ( $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ ) | $\mathrm{V}_{\text {SHORT }}$ | $V_{D D}-1.1$ | $V_{D D}-0.8$ | $\mathrm{V}_{\mathrm{DD}}-0.5$ | V | D |
| Current Limit Delay Time ( $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ ) | ${ }^{\mathrm{t}}$ (DET3) ${ }^{\mathrm{t}}$ (SHORT) | $9.0$ | $\begin{aligned} & 13 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 17 \\ & 50 \end{aligned}$ | $\begin{aligned} & \mathrm{ms} \\ & \mu \mathrm{~s} \end{aligned}$ | D D |
| Reset Resistance for Short Protection | $\mathrm{R}_{\text {SHORT }}$ | 50 | 100 | 150 | $\mathrm{k} \Omega$ | D |

## OUTPUTS

| CO Nch On Voltage $\left(\mathrm{I}_{\mathrm{O}}=50 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DD}}=4.4 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{ol} 1}$ | - | 0.2 | 0.5 | V | E |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| CO Pch On Voltage $\left(\mathrm{I}_{\mathrm{O}}=-50 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DD}}=3.9 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{oh} 1}$ | 3.4 | 3.8 | - | V | F |
| DO Nch On Voltage $\left(\mathrm{I}_{\mathrm{O}}=50 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DD}}=2.4 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{ol} 2}$ | - | 0.2 | 0.5 | V | G |
| DO Pch On Voltage $\left(\mathrm{I}_{\mathrm{O}}=-50 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{DD}}=3.9 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{oh} 2}$ | 3.4 | 3.7 | - | V | H |

TOTAL DEVICE

| Operating Input Voltage | $\mathrm{V}_{\mathrm{DD}}$ | 1.5 | - | 10 | V | A |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current | $\mathrm{I}_{\text {cell }}$ |  |  |  |  |  |
| Operating (VD $\left.=3.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{P}-}=0 \mathrm{~V}\right)$ | - | 3.0 | 6.0 | $\mu \mathrm{~A}$ | I |  |
| Standby (VD $=2.0 \mathrm{~V}$ ) |  | - | 0.3 | 0.6 | $\mu \mathrm{~A}$ | I |
| Minimum Operating Cell Voltage for Zero Volt Charging <br> (Pin 5 to Pin 2) | $\mathrm{V}_{\mathrm{ST}}$ | - | - | 1.2 | V | A |

1. Indicates test circuits shown on next page.


Figure 2. Test Circuit Schematics


Figure 3. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

| Pin | Symbol | Description |
| :---: | :---: | :--- |
| 1 | DO | This output connects to the gate of the discharge MOSFET allowing it to enable or disable battery pack <br> discharging. |
| 2 | $\mathrm{P}-$ | This pin monitors cell discharge current. <br> The excess current detector sets when the combined voltage drop of the charge MOSFET and the discharge <br> MOSFET exceeds the discharge current limit threshold voltage, $\mathrm{V}_{(\text {(DET3) }}$. The short circuit detector activates when <br> $\mathrm{V}_{(\mathrm{P}-)}$ is pulled within 0.8 V of the cell voltage by a short circuit. |
| 3 | CO | This output connects to the gate of the charge MOSFET allowing it to enable or disable battery pack charging. |
| 4 | $\mathrm{C}_{\mathrm{t}}$ | This pin connects to the external capacitor for setting the output delay of the overvoltage detector (VD1). |
| 5 | $\mathrm{~V}_{\text {cell }}$ | This input connects to the positive terminal of the cell for voltage monitoring and provides operating bias for the <br> integrated circuit. |
| 6 | Gnd | This is the ground pin of the IC. |

TYPICAL CHARACTERISTICS


Figure 4. Overvoltage Threshold vs Temperature MC33349N-3X


Figure 6. Excess Current Threshold vs Temperature MC33349N-3X / MC33349N-7X


Figure 8. Output Delay of Overvoltage vs Temperature MC33349N-3X


Figure 5. Undervoltage Threshold vs Temperature MC33349N-3X / MC33349N-7X


Figure 7. Short Protection Voltage vs Temperature MC33349N-3X


Figure 9. Output Delay of Undervoltage vs Temperature
MC33349N-3X / MC33349N-7X


Figure 10. Output Delay of Excess Current vs Temperature MC33349N-3X


Figure 12. Overvoltage Threshold Hysteresis vs Temperature MC33349N-3X / MC33349N-7X


Figure 14. Standby Current vs Temperature MC33349N-3X


Figure 11. Output Delay of Short Circuit Detector vs Temperature MC33349N-3X


Figure 13. Operating Current
vs Temperature
MC33349N-3X


Figure 15. Cout Nch Driver On Voltage (Vol1)
vs Temperature
MC33349N-3X


Figure 16. Cout Pch Driver On Voltage (Voh1) vs Temperature MC33349N-3X


Figure 18. Dout Pch Driver On Voltage (Voh2) vs Temperature MC33349N-3X


Figure 17. Dout Nch Driver On Voltage (Vol2) vs Temperature MC33349N-3X


Figure 19. Short Protection Delay Time vs Capacitance C2 MC33349N-3X


Figure 20. Excess Current Delay Time vs $\mathrm{V}_{\mathrm{DD}}$ MC33349N-3X


Figure 21. Excess Current Threshold vs
External Resistance R2
MC33349N-3X / MC33349N-7X


Figure 22. Overvoltage Threshold vs External Resistance R1 MC33349N-3X

## OPERATING DESCRIPTION

## VD1 / Over-Charge Detector

VD1 monitors the voltage at the $\mathrm{V}_{\text {CELL }}$ pin $\left(\mathrm{V}_{\mathrm{DD}}\right)$. When it exceeds the over-charge detector threshold, $\mathrm{V}_{\mathrm{DET} 1}$. VD1 senses an over-charging condition, the CO pin goes to a "Low" level, and the external charge control, Nch-MOSFET turns off.

Resetting VD1 allows resumption of the charging process. VD1 resets under two conditions, thus, making the CO pin level "High." The first case occurs when the cell voltage drops below " $\mathrm{V}_{\mathrm{DET1}}-\mathrm{V}_{\mathrm{HYS} 1}$." ( $\mathrm{V}_{\mathrm{HYS}}$ is typically 200 mV ). In the second case, disconnecting the charger from the battery pack can reset VD1 after $\mathrm{V}_{\mathrm{DD}}$ drops between "V $V_{\text {DET1 }}$ " and " $V_{\text {DET1 }}-V_{\text {HYS1 }}$ ".

After detecting over-charge, connecting a load to the battery pack allows load current to flow through the parasitic diode of the external charge control FET. The CO level goes "High" when the cell voltage drops below $\mathrm{V}_{\text {DET1 }}$ due to load current draw through the parasitic diode.

An external capacitor connected between the Gnd pin and Ct pin sets the output delay time for over-charge detection. The external capacitor sets up a delay time from the moment of over-charge detection to the time CO outputs a signal, which enables the charge control FET to turn off. If the voltage fault occurs within the time delay window. CO will not turn off the charge control FET. The output delay time can be calculated as follows:

$$
{ }^{\mathrm{t} V D E T 1} 1[\mathrm{sec}]=\left(\mathrm{Ct}[\mathrm{~F}] \times(\mathrm{VDD}[\mathrm{~V}]-0.7) /\left(0.48 \times 10^{-6}\right)\right.
$$

A level shifter incorporated in a buffer driver for the CO pin drives the "Low" level of CO pin to the $\mathrm{P}-$ pin voltage. A CMOS buffer sets the "High" level of CO pin to $V_{D D}$.

## VD2 / Over-Discharge Detector

VD2 monitors the voltage at the $\mathrm{V}_{\text {CELL }}$ pin ( $\mathrm{V}_{\mathrm{DD}}$ ). When it drops below the over-discharge detector threshold, $\mathrm{V}_{\text {DET2 }}$, VD2 senses an over-discharge condition, the DO
pin goes to a "Low" level, and the external discharge control Nch MOSFET turns off. The IC enters a low current standby mode after detection of an over-discharged voltage by VD2. Supply current then reduces to approximately $0.3 \mu \mathrm{~A}$. During standby mode, only the charger detector operates.

VD2 can only reset after connecting the pack to a charger. While $\mathrm{V}_{\mathrm{DD}}$ remains under the over-discharge detector threshold, $\mathrm{V}_{\text {DET2 }}$, discharge current can flow through the parasitic diode of the external discharge control FET. The DO level goes "High" when the cell voltage rises above $\mathrm{V}_{\text {DET2 }}$ due to the charging current through the parasitic diode. Connecting a charger to the battery pack will instantly set DO "High" if this causes $V_{\text {DD }}$ to rise above $V_{\text {DET2 }}$.
When cell voltage equals zero, one can charge the battery pack if the voltage is greater than the minimum charge voltage, $\mathrm{V}_{\mathrm{ST}}$.

Output delay time for the over-discharge detection ( $\mathrm{t}_{\text {VDET2 }}$ ) is fixed internally. If the voltage fault occurs within the time delay window, DO will not turn off the discharge control FET.
A CMOS buffer sets the output of the DO pin to a "High" level of $\mathrm{V}_{\mathrm{DD}}$ and a "Low" level of Gnd.

## VD3 / Excess Current Detector, Short Circuit Detector

Both the excess current detector and the short circuit detector can work when the two control FET's are on. When the voltage at the P - pin rises to a value between the short circuit protection voltage, $\mathrm{V}_{\text {SHORT }}$, and the excess current threshold, $\mathrm{V}_{\mathrm{DET}}$, the excess current detector operates. Increasing $\mathrm{V}_{(\mathrm{P}-)}$ higher than $\mathrm{V}_{\text {SHORT }}$ enables the short circuit detector. The DO pin then goes to a "Low" level, and the external discharge control Nch MOSFET turns off.

Output delay time for excess current detection ( $\mathrm{t}_{\mathrm{VDET}}$ ) is fixed internally. If the excess current fault occurs within the time delay window, DO will not turn off the discharge control FET. However, when the short circuit protector is
enabled, DO can turn off the discharge control FET. Its delay time would be approximately $5 \mu \mathrm{~s}$.

The P-pin has a built-in pull down resistor, typically $100 \mathrm{k} \Omega$, which connects to the Gnd pin. Once an excess current or short circuit fault is removed, the internal resistor pulls $\mathrm{V}_{(\mathrm{P}-)}$ to the Gnd pin potential. Therefore, the voltage from P - to Gnd drops below the current detection thresholds and DO turns the external MOSFET back on.

## -NOTE-

If $\mathrm{V}_{\mathrm{DD}}$ voltage is higher than the over-discharge voltage threshold, $\mathrm{V}_{\mathrm{DET}}$, when excess current is detected the IC will not enter a standby mode. However, if $\mathrm{V}_{\mathrm{DD}}$ is below $\mathrm{V}_{\text {DET2 }}$ when excess current is detected, the IC will enter a standby mode. This will not occur when the short circuit detector activates.


Figure 23. Timing Diagram / Operational Description


Figure 24. Typical Application Circuit

## Technical Notes

R1 and C1 will stabilize a supply voltage to the MC33349. A recommended R1 value is less than $1 \mathrm{k} \Omega$. A larger value of R1 leads to higher detection voltage because of shoot through current into the IC.
R2 and C2 stabilize P - pin voltage. Larger R2 values could possibly disable reset from over-discharge by connecting a charger. Recommended values are less than $1 \mathrm{k} \Omega$. After an over-charge detection even connecting a battery pack to a system could probably not allow a system to draw load current if one uses a larger R2C2 time constant. The recommended C 2 value is less than $1 \mu \mathrm{~F}$.
R1 and R2 can operate as a current limiter against setting cell reverse direction or for applying excess charging voltage to the IC and battery pack. Smaller R1 and R2 values may cause excessive power consumption over the specified power dissipation rating. Therefore $\mathrm{R} 1+\mathrm{R} 2$ should be more than $1 \mathrm{k} \Omega$.
The time constants R1C1 and R2C2 must have a relation as follows:
$\mathrm{R} 1 \mathrm{C} 1 \leq \mathrm{R} 2 \mathrm{C} 2$
If the R1C1 time constant for the Vcell pin is larger than the R2C2 time constant for the $\mathrm{P}-$ pin, the IC might enter a standby mode after detecting excess current. This was noted in the operating description of the current detectors.

## MC33349

ORDERING INFORMATION

| Device | Overvoltage <br> Threshold (V) | Undervoltage <br> Threshold (V) | Current Limit <br> Threshold (V) | Marking | Reel Size | Tape width | Quantity |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MC33349N-3R1 | 4.25 | 2.5 | 0.2 | $A 1 x^{*}$ |  |  |  |
| MC33349N-4R1 | 4.25 | 2.5 | 0.075 | $A 2 x^{*}$ | $7{ }^{\prime \prime}$ | 8 mm | 3000 |
| MC33349N-7R1 | 4.35 | 2.5 | 0.2 | $A 0 x x^{*}$ |  |  |  |

*"xx" denotes the date code marking.
Consult factory for information on other threshold values.

## NCP800

## Lithium Battery Protection Circuit for One Cell Battery Packs

The NCP800 resides in a lithium battery pack where the battery cell continuously powers it. In order to maintain cell operation within specified limits, this protection circuit senses cell voltage and discharge current, and correspondingly controls the state of two, N-channel, MOSFET switches. These switches reside in series with the negative terminal of the cell and the negative terminal of the battery pack. During a fault condition, the NCP800 open circuits the pack by turning off one of these MOSFET switches, which disconnects the current path.

- Internally Trimmed Precision Charge and Discharge Voltage Limits
- Discharge Current Limit Detection
- Automatic Reset from Discharge Current Faults
- Low Current Standby State when Cells are Discharged
- Available in a Low Profile Surface Mount Package


Figure 1. Typical One Cell Smart Battery Pack This device contains 169 transistors.


## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP800SN1T1 | TSOP-6 | 3000 Units/Rail |



Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

| Pin | Symbol | Description |
| :---: | :---: | :--- |
| 1 | DO | This output connects to the gate of the discharge MOSFET allowing it to enable or disable battery pack discharging. |
| 2 | P- | This pin monitors cell discharge current. The excess current detector sets when the combined voltage drop of the <br> charge MOSFET and the discharge MOSFET exceeds the discharge current limit threshold voltage, V(DET). The <br> short circuit detector activates when V(P-) is pulled within typically 0.85 V of the $\mathrm{V}_{\text {cell }}$ Voltage. The CO driver is level <br> shifted to the voltage at this pin. |
| 3 | CO | This output connects to the gate of the charge MOSFET switch Q1 allowing it to enable or disable battery pack <br> charging. |
| 4 | $\mathrm{C}_{t}$ | This pin connects to the external capacitor for setting the output delay of the overvoltage detector (VD1). |
| 5 | $\mathrm{~V}_{\text {cell }}$ | This input connects to the positive terminal of the cell for voltage monitoring and provides operating bias for the <br> integrated circuit. |
| 6 | Gnd | This is the ground pin of the IC. |

MAXIMUM RATINGS

| Ratings | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (Pin 5 to Pin 6) | $\mathrm{V}_{\mathrm{DD}}$ | -0.3 to 12 | V |
| $\begin{array}{l}\text { Input Voltage } \\ \text { Charge Gate Drive Common/Current Limit (Pin 5 to Pin 2) } \\ \text { Overvoltage Delay Capacitor (Pin 4 to Pin 6) }\end{array}$ |  |  | V |
| $\begin{array}{l}\text { Output Voltage } \\ \text { CO Pin Voltage (Pin 3 to Pin 2) } \\ \text { DO Pin Voltage (Pin 1 to Pin 6) }\end{array}$ | V (pin5) +0.3 to V (pin 5) -8 |  |  |
| 0.3 to 12 |  |  |  |$)$

1. This device contains ESD protection:

Human Body Model 2000 V.
Machine Model Method 200 V .
ELECTRICAL CHARACTERISTICS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VOLTAGE SENSING |  |  |  |  |  |
| Overvoltage Threshold, $\mathrm{V}_{\mathrm{DD}}$ Increasing (Note 2) Overvoltage Hysteresis VDD Decreasing | $\begin{aligned} & \mathrm{V}_{\mathrm{DET} 1} \\ & \mathrm{~V}_{\mathrm{HYS} 1} \end{aligned}$ | $\begin{array}{r} 4.30 \\ 150 \\ \hline \end{array}$ | $\begin{aligned} & 4.35 \\ & 200 \end{aligned}$ | $\begin{aligned} & 4.40 \\ & 250 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{mV} \end{gathered}$ |
| Overvoltage Delay Time $\begin{aligned} & \mathrm{C}_{\mathrm{t}}=560 \mathrm{pF} \\ & \mathrm{C}_{\mathrm{t}}=0.01 \mu \mathrm{~F} \end{aligned}$ | tDET1 |  | $\begin{gathered} 4 \\ 75 \end{gathered}$ | $6$ | ms |
| Undervoltage Threshold, $\mathrm{V}_{\mathrm{DD}}$ Decreasing | $\mathrm{V}_{\text {DET2 }}$ | 2.437 | 2.5 | 2.563 | V |
| Undervoltage Delay Time ( $\mathrm{V}_{\mathrm{DD}}=3.6 \mathrm{~V}$ to 2.4 V ) | $t_{\text {DET2 }}$ | 7.0 | 11 | 13 | ms |

## CURRENT SENSING

| Excess Current Threshold (Detect rising edge of P - pin voltage) (Note 3) | $\mathrm{V}_{\text {DET3 }}$ | 170 | 200 | 230 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Short Protection Voltage ( $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ ) | $\mathrm{V}_{\text {SHORT }}$ | $V_{D D}-1.1$ | $\mathrm{V}_{\mathrm{DD}}-0.85$ | $V_{D D}-0.5$ | V |
| Current Limit Delay Time ( $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ ) | tDET3 tshort | $9.0$ | $\begin{aligned} & 14 \\ & 10 \end{aligned}$ | $17$ | $\begin{aligned} & \mathrm{ms} \\ & \mu \mathrm{~s} \end{aligned}$ |
| Reset Resistance | $\mathrm{R}_{\text {SHORT }}$ | 50 | 100 | 150 | $\mathrm{k} \Omega$ |

## OUTPUTS

| Charge Gate Drive Output Low (Pin 3 to Pin 2) $\left(\mathrm{V}_{\mathrm{DD}}=4.4 \mathrm{~V}, \mathrm{Io}=50 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{011}$ | - | 0.16 | 0.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Charge Gate Drive Output High (Pin 5 to Pin 3) ( $\mathrm{V}_{\mathrm{DD}}=3.9 \mathrm{~V}, \mathrm{lo}=-50 \mu \mathrm{~A}$ ) | $\mathrm{V}_{\text {oh1 }}$ | 3.4 | 3.8 | - | V |
| Discharge Gate Drive Output Low (Pin 1 to Pin 6) $\left(\mathrm{V}_{\mathrm{DD}}=2.4 \mathrm{~V}, \mathrm{lo}=50 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\text {ol2 }}$ | - | 0.1 | 0.5 | V |
| Discharge Gate Drive Output High (Pin 5 to Pin 1) $\left(\mathrm{V}_{\mathrm{DD}}=3.9 \mathrm{~V}, \mathrm{lo}=-50 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\text {oh2 }}$ | 3.4 | 3.8 | - | V |

TOTAL DEVICE

| Supply Current | $\mathrm{I}_{\text {cell }}$ |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Operating $\left(\mathrm{V}_{\mathrm{DD}}=3.9 \mathrm{~V}, \mathrm{VP}-=0 \mathrm{~V}\right)$ |  | 2.0 | 4.0 | 6.0 | $\mu \mathrm{~A}$ |
| Standby $\left(\mathrm{V}_{\mathrm{DD}}=2.0 \mathrm{~V}\right)$ | - | 0.3 | 0.6 | $\mu \mathrm{~A}$ |  |
| Operating Voltage | $\mathrm{V}_{\mathrm{DD}}$ | 1.5 | - | 10 | V |

2. Consult factory about other Overvoltage Threshold Options.
3. Consult factory about other Excess Current Threshold Options.


Figure 3. Overvoltage Threshold vs. Temperature


Figure 5. Excess Current Threshold vs. Temperature


Figure 7. Output Delay of Overvoltage vs. Temperature


Figure 4. Undervoltage Threshold vs. Temperature


Figure 6. Short Protection Threshold vs. Temperature


Figure 8. Output Delay of Undervoltage vs. Temperature


Figure 9. Output Delay of Excess Current vs. Temperature

Figure 11. Overvoltage Threshold Hysteresis vs. Temperature


Figure 13. Standby Current vs. Temperature


Figure 10. Output Delay of Short Circuit Detector vs. Temperature


Figure 12. Operating Current vs. Temperature

Figure 14. Cout $_{\text {Nch }}$ Driver On Voltage vs. Temperature


Figure 15. $\mathrm{D}_{\text {out }}$ Nch Driver On Voltage vs. Temperature


Figure 17. Dout Pch Driver On Voltage vs. Temperature



Figure 19. Excess Current Delay Time vs. $V_{\text {DD }}$


Figure 16. Cout $_{\text {Pch }}$ Driver On Voltage vs.

Temperature


Figure 18. Short Protection Delay Time vs. Capacitance $\mathrm{C}_{2}$


Figure 20. Excess Current Threshold vs. External Resistance R2


Figure 21. Overvoltage Threshold vs. External Resistance R1

## OPERATING DESCRIPTION

## VD1 / Over-Charge Detector

VD1 monitors the voltage at the $\mathrm{V}_{\text {CELL }}$ pin $\left(\mathrm{V}_{\mathrm{DD}}\right)$. When it exceeds the over-charge detector threshold, $\mathrm{V}_{\mathrm{DET1}}$. VD1 senses an over-charging condition, the CO pin goes to a "Low" level, and the external charge control, Nch-MOSFET turns off.

Resetting VD1 allows resumption of the charging process. VD1 resets under two conditions, thus, making the CO pin level "High." The first case occurs when the cell voltage drops below "V $\mathrm{V}_{\mathrm{DET} 1}-\mathrm{V}_{\mathrm{HYS1}}$." ( $\mathrm{V}_{\mathrm{HYS}}$ is typically 200 mV ). In the second case, disconnecting the charger from the battery pack can reset VD1 after $\mathrm{V}_{\mathrm{DD}}$ drops between " $V_{\text {DETI }}$ " and " $\mathrm{V}_{\text {DET1 }}-\mathrm{V}_{\text {HYSI }}$ ".

After detecting over-charge, connecting a load to the battery pack allows load current to flow through the parasitic diode of the external charge control FET. The CO level goes "High" when the cell voltage drops below $\mathrm{V}_{\text {DET1 }}$ due to load current draw through the parasitic diode.

An external capacitor connected between the Gnd pin and Ct pin sets the output delay time for over-charge detection. The external capacitor sets up a delay time from the moment of over-charge detection to the time CO outputs a signal, which enables the charge control FET to turn off. If the voltage fault occurs within the time delay window. CO will not turn off the charge control FET. The output delay time can be calculated as follows:

$$
{ }^{\mathrm{t}} \mathrm{DET} 1[\mathrm{sec}]=\left(\mathrm{Ct}[\mathrm{~F}] \times(\mathrm{VDD}[\mathrm{~V}]-0.7) /\left(0.48 \times 10^{-6}\right)\right.
$$

A level shifter incorporated in a buffer driver for the CO pin drives the "Low" level of CO pin to the $\mathrm{P}-$ pin voltage. A CMOS buffer sets the "High" level of CO pin to $\mathrm{V}_{\mathrm{DD}}$.

## VD2 / Over-Discharge Detector

VD2 monitors the voltage at the $\mathrm{V}_{\text {CELL }}$ pin $\left(\mathrm{V}_{\mathrm{DD}}\right)$. When it drops below the over-discharge detector threshold, $\mathrm{V}_{\text {DET2 }}, \mathrm{VD} 2$ senses an over-discharge condition, the DO pin goes to a "Low" level, and the external discharge control

Nch MOSFET turns off. The IC enters a low current standby mode after detection of an over-discharged voltage by VD2. Supply current then reduces to approximately $0.3 \mu \mathrm{~A}$. During standby mode, only the charger detector operates.
VD2 can only reset after connecting the pack to a charger. While $\mathrm{V}_{\mathrm{DD}}$ remains under the over-discharge detector threshold, $\mathrm{V}_{\mathrm{DET} 2}$, discharge current can flow through the parasitic diode of the external discharge control FET. The DO level goes "High" when the cell voltage rises above $\mathrm{V}_{\text {DET2 }}$ due to the charging current through the parasitic diode. Connecting a charger to the battery pack will instantly set DO "High" if this causes $\mathrm{V}_{\mathrm{DD}}$ to rise above $\mathrm{V}_{\text {DET2 }}$.
Output delay time for the over-discharge detection ( $\mathrm{t}_{\text {DET2 }}$ ) is fixed internally. If the voltage fault occurs within the time delay window, DO will not turn off the discharge control FET.
A CMOS buffer sets the output of the DO pin to a "High" level of $\mathrm{V}_{\mathrm{DD}}$ and a "Low" level of Gnd.

## VD3 / Excess Current Detector, Short Circuit Detector

Both the excess current detector and the short circuit detector can work when the two control FET's are on. When the voltage at the $\mathrm{P}-$ pin rises to a value between the short circuit protection voltage, $\mathrm{V}_{\text {SHORT }}$, and the excess current threshold, $\mathrm{V}_{\mathrm{DET3}}$, the excess current detector operates. Increasing $\mathrm{V}_{(\mathrm{P}-)}$ higher than $\mathrm{V}_{\text {SHORT }}$ enables the short circuit detector. The DO pin then goes to a "Low" level, and the external discharge control Nch MOSFET turns off.
Output delay time for excess current detection ( $\mathrm{t}_{\text {DET3 }}$ ) is fixed internally. If the excess current fault occurs within the time delay window, DO will not turn off the discharge control FET. However, when the short circuit protector is enabled, DO can turn off the discharge control FET. Its delay time is approximately $10 \mu \mathrm{~s}$.
The P-pin has a built-in pull down resistor, typically $100 \mathrm{k} \Omega$, which connects to the Gnd pin. Once an excess current or short circuit fault is removed, the internal resistor
pulls $\mathrm{V}_{(\mathrm{P}-)}$ to the Gnd pin potential. Therefore, the voltage from P - to Gnd drops below the current detection thresholds and DO turns the external MOSFET back on.
NOTE: If $\mathrm{V}_{\mathrm{DD}}$ voltage is higher than the over-discharge voltage threshold, $\mathrm{V}_{\mathrm{DET}}$, when excess current is detected
the IC will not enter a standby mode. However, if $\mathrm{V}_{\mathrm{DD}}$ is below $\mathrm{V}_{\text {DET2 }}$ when excess current is detected, the IC will enter a standby mode. This will not occur when the short circuit detector activates.


Figure 22. Timing Diagram / Operational Description


Figure 23. Typical Application Circuit

## Technical Notes

R 1 and C 1 will stabilize a supply voltage to the NCP800. A recommended R1 value is less than $1 \mathrm{k} \Omega$. A larger value of R1 leads to higher detection voltage because of shoot through current into the IC.
R2 and C2 stabilize P - pin voltage. Larger R2 values could possibly disable reset from over-discharge by connecting a charger. Recommended values are less than $1 \mathrm{k} \Omega$. After an over-charge detection even connecting a battery pack to a system could probably not allow a system to draw load current if one uses a larger R2C2 time constant. The recommended C2 value is less than $1 \mu \mathrm{~F}$.
R1 and R2 can operate as a current limiter against setting cell reverse direction or for applying excess charging voltage to the IC and battery pack. Smaller R1 and R2 values may cause excessive power consumption over the specified power dissipation rating. Therefore $\mathrm{R} 1+\mathrm{R} 2$ should be more than $1 \mathrm{k} \Omega$.
The time constants R1C1 and R2C2 must have a relation as follows:
$\mathrm{R} 1 \mathrm{C} 1 \leq \mathrm{R} 2 \mathrm{C} 2$
If the R1C1 time constant for the Vcell pin is larger than the R2C2 time constant for the $\mathrm{P}-$ pin, the IC might enter a standby mode after detecting excess current. This was noted in the operating description of the current detectors.

## Advanced Information <br> Lithium Battery Protection Circuit for Three Battery Packs

The MC33351A is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of three cell rechargeable battery packs. The MC33351A is specifically designed to be placed in a lithium battery pack where the battery cells continuously power it. In order to maintain cell operation within specified limits, the protection circuit senses cell voltages, and discharge current, and correspondingly controls the state of two P-channel MOSFET switches. These switches are connected in series with the positive terminal of the third cell and the positive terminal of the battery pack. During a fault condition, the MC33351A open circuits the pack by turning off one of these MOSFET switches.

## Features

- Selectable Charge Interrupt Voltage Sensing Mode for Precise Cell Voltage Measurements
- Programmable Overvoltage Delay
- Choice of Discharge Current Limit Sensing Elements consisting of either Low-Side Resistor or High-Side MOSFET Switches
- Programmable Discharge Current Limit Threshold and Shutdown Delay
- Selectable Cell Voltage Balancing
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Package

Typical Three Cell Smart Battery Pack


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com

| A | $=$ Assembly Location |
| :--- | :--- |
| WL, L | $=$ Wafer Lot |
| YY, Y | $=$ Year |
| WW,W | $=$ Work Week |

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC33351ADTB-1 | TSSOP-20 | 75 Units/Rail |
| MC33351ADTB-1R2 | TSSOP-20 | 2500 Tape/Reel |

Smart Battery Pack with Low-Side Discharge Current Sensing, Charge Interrupt Voltage Sensing, and Cell Voltage Balancing


Figure 1. Control Logic Inputs from Microcontroller Output Ports

Smart Battery Pack with High-Side Discharge Current Sensing


Figure 2.

[^25]MAXIMUM RATINGS

| Ratings | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage (Measured with respect to Ground, Pin 13) <br> Cell 1/Vc (Pin 15) <br> Cell 2 (Pin 12) <br> Cell 3 (Pin 18) <br> Vcc/ High Side Discharge Current Limit (Pin 16) <br> Charge Inhibit Input (Pin 1) <br> Discharge Inhibit Input (Pin 2) <br> Overvoltage Shutdown Delay (Pin 3) <br> Discharge Current Limit Shutdown Delay (Pin 4) <br> Low-Side Discharge Current Limit Input (Pin 5) <br> Voltage Sampling Mode Select (Pin 6) <br> Discharge Gate Drive Output (Pin 7) <br> Charge Gate Drive Common (Pin 8) <br> Charge Gate Drive Output (Pin 9) <br> Undervoltage Fault Output (Pin 10) <br> High-Side Current Limit Threshold (Pin 11) | $V_{\text {IR }}$ | $\begin{aligned} & 7.5 \\ & 10 \\ & 18 \\ & 20 \\ & 7.5 \\ & 7.5 \\ & 7.5 \\ & 20 \\ & 7.5 \\ & 7.5 \\ & 18 \\ & 20 \\ & 18 \\ & 20 \\ & 7.5 \end{aligned}$ | V |
| Cell Balancing Current (Note 1) <br> Balance 3, Source Current (Pin 19) <br> Balance 1, Balance 2 Sink Current (Pin 20, 14) | $\mathrm{l}_{\text {bal }}$ | $\begin{aligned} & 50 \\ & 50 \end{aligned}$ | mA |
| Undervoltage Fault Output Sink Current (Pin 10) | $\mathrm{fflt}^{\text {flt }}$ | 10 | mA |
| Thermal Resistance, Junction-to-Air DTB Suffix, TSSOP Plastic Package, Case 948E DW Suffix, SO-20L Plastic Package, Case 751D | $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 135 \\ & 105 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature (Note 1) | $\mathrm{T}_{\mathrm{J}}$ | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {cell } 3}(\operatorname{Pin} 18)=10.5 \mathrm{~V}, \mathrm{~V}_{\text {cell } 2}(\right.$ Pin 12$)=7.0 \mathrm{~V}, \mathrm{~V}_{\text {cell } 1}($ Pin 15$)=3.5 \mathrm{~V}$,
$\mathrm{C}_{\text {dly }}($ Pin 4$)=1000 \mathrm{pF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ )

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VOLTAGE SENSING |  |  |  |  |  |
| Cell Charging Cutoff (Pin 15 to 13,12 to 15,18 to 12) <br> Overvoltage Threshold, $\mathrm{V}_{\text {Cell }}$ Increasing <br> MC33351A-1 <br> Overvoltage Hysteresis, $\mathrm{V}_{\text {Cell }}$ Decreasing <br> Delay <br> One Overvoltage Sample (Pin 3 = Gnd) <br> Two Consecutive Overvoltage Samples (Pin $3=\mathrm{Vc}$ ) | $\begin{gathered} \mathrm{V}_{\mathrm{th}(\mathrm{OV})} \\ \mathrm{V}_{\mathrm{H}} \\ \mathrm{t}_{\mathrm{dly}(\mathrm{OV})} \end{gathered}$ | $\begin{gathered} 4.207 \\ 50 \\ 0 \\ 0 \\ 1.0 \end{gathered}$ | $125$ | $\begin{gathered} 4.293 \\ 200 \\ \\ 1.2 \\ 2.3 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{mV} \\ \mathrm{~s} \\ \mathrm{~s} \end{gathered}$ |
| Cell Discharging Cutoff MC33351A-1 <br> Undervoltage Threshold, $\mathrm{V}_{\text {Cell }}$ Decreasing  | $\mathrm{V}_{\text {th }}(\mathrm{UV})$ | 2.185 | 2.3 | 2.415 | V |
| Input Bias Current During Cell Voltage Sampling | $I_{\text {IB }}$ | - | 28 | - | $\mu \mathrm{A}$ |
| Cell Voltage Sampling Rate | ${ }^{\text {t }}$ (smpl) | - | 1.0 | - | s |
| Charge Interrupt Input Voltage Range (Pin 6) Enabled Disabled | $\mathrm{V}_{\text {th(Intrrpt }}$ | - | $\begin{gathered} \left(\mathrm{V}_{\mathrm{c}} / 2+0.2 \text { to } \mathrm{V}_{\mathrm{c}}\right) \\ \left(0 \text { to } \mathrm{V}_{\mathrm{c}} / 2-0.2\right) \end{gathered}$ | - | V |
| Enabled Charge Interrupt Time | $t_{\text {Intrip }}$ | - | 20 | - | ms |

NOTE: 1 Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {cell } 3}(\right.$ Pin 18 $)=10.5 \mathrm{~V}, \mathrm{~V}_{\text {cell } 2}($ Pin 12$)=7.0 \mathrm{~V}, \mathrm{~V}_{\text {cell } 1}($ Pin 15$)=3.5 \mathrm{~V}$,
$\mathrm{C}_{\text {dly }}($ Pin 4$)=1000 \mathrm{pF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ )

| $\mid$ Characteristic |
| :--- |
|  Symbol Min Typ Max UnitCELL VOLTAGE BALANCING $R_{\text {DS(on) }}$    <br> Internal Balancing MOSFET On-Resistance  - 100 - <br> Balance 3, (Pin 19)  - 50 - <br> Balance 1, Balance 2 (Pin 20, 14)     |

CURRENT SENSING

| High-Side Discharge Current Limit (Pin 16 to Pin 8) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Threshold Voltage | $\mathrm{V}_{\text {th(HSdschg }}$ |  |  |  |  |
| $\mathrm{R}_{\text {pin } 11}=1.0 \mathrm{M} \Omega$ |  | 200 | 280 | 380 | mV |
| $\mathrm{R}_{\text {pin } 11}=2.0 \mathrm{M} \Omega$ |  | 100 | 170 | 230 | mV |
| Delay |  |  |  |  |  |
| Overcurrent Detect ( $\mathrm{V}_{\text {sense }}=250 \mathrm{mV}$ ) | $\mathrm{t}_{\text {dly }}$ (HSdschg) | 2.5 |  | 6.0 | ms |
| Short Circuit Detect ( $\mathrm{V}_{\text {sense }}=1.0 \mathrm{~V}$ ) |  | 0.0 |  | 2.5 | ms |
| Low-Side Discharge Current Limit (Pin 13 to Pin 5) |  |  |  |  |  |
| Delay |  |  |  |  |  |
| Overcurrent Detect ( $\mathrm{V}_{\text {sense }}=50 \mathrm{mV}$ ) | $\mathrm{t}_{\text {dly }}$ (LSdschg) | 2.5 |  | 6.0 | ms |
| Short Circuit Detect ( $\mathrm{V}_{\text {sense }}=200 \mathrm{mV}$ ) |  | 0.3 |  | 0.4 | ms |

LOGIC

| Charge and Discharge Inhibit Inputs (Pin 1, 2) <br> Threshold Voltage <br> Propagation Delay to Respective Gate Drive Output | $\begin{gathered} \mathrm{V}_{\text {th(inhbt) }} \\ \mathrm{t}_{\mathrm{PL} / \mathrm{H}} \end{gathered}$ | - | $\begin{aligned} & \mathrm{V}_{\mathrm{c}} / 2 \\ & 100 \end{aligned}$ | - | V $\mu \mathrm{S}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Undervoltage Fault Output (Pin 10) <br> Low State Sink Resistance <br> Off State Leakage Current $\left(V_{\text {drain }}=16 \mathrm{~V}\right)$ <br> Detection Delay Time Before Discharge MOSFET Turn Off (Note 2) |  | - | $\begin{gathered} 100 \\ 100 \\ 16 \end{gathered}$ | - | $\begin{gathered} \Omega \\ \mathrm{nA} \\ \mathrm{~s} \end{gathered}$ |
| Charge and Discharge Gate Drive Outputs (Pin 9, 7) <br> High State Source Resistance <br> Low State Sink Resistance | $\mathrm{R}_{\mathrm{DS} \text { (source) }}$ $\mathrm{R}_{\mathrm{DS} \text { (sink) }}$ | - | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | - | $\Omega$ |

TOTAL DEVICE

| Average Cell Current | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\quad$Operating $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right)$ <br> Sleepmode (VC $=6.0 \mathrm{~V})$ |  | - | 15 | 20 | $\mu \mathrm{~A}$ |
| Minimum Operating Cell Voltage | $\mathrm{V}_{\mathrm{CC}}$ |  |  | 500 | nA |
| Cell 1 Voltage |  | 1.5 | 1.8 | - | V |
| Cell 2, or Cell 3 Voltage |  | 0.7 | 0.8 | - |  |

[^26]
## MC33351A



Figure 3. Over Voltage Threshold versus Temperature


Figure 5. Undervoltage Threshold versus Temperature


Figure 7. Discharge Current (High Side) Threshold versus Temperature (R11 = 1.5 mOhms )


Figure 4. Charge ON Voltage Threshold versus Temperature


Figure 6. Discharge Current (Low Side) versus Temperature


Figure 8. Discharge Current (High Side) versus Resistance

## MC33351A




Figure 11. Discharge Current Limit Shutdown Delay versus Capacitance

PIN FUNCTION DESCRIPTION

| Pin <br> No. | Function | Description |
| :---: | :---: | :---: |
| 1 | Charge Inhibit Input | A logic low level at this input will disable battery pack charging. A 10 k internal pull-up resistor connects from this pin to $\mathrm{V}_{\mathrm{C}}$. |
| 2 | Discharge Inhibit Input | A logic low level at this input will disable battery pack discharging. A 10 k internal pull-up resistor connects from this pin to $\mathrm{V}_{\mathrm{C}}$. Also, connecting this pin to 3.0 V above $\mathrm{V}_{\mathrm{C}}$ the internal logic is held in reset state and both MOSFET switches are turned on. |
| 3 | Overvoltage Shutdown Delay | This input controls the required number of cell overvoltage events that must be detected before charge switch Q1 is turned off. With a logic level low at this input, charge switch Q1 turns off after a single overvoltage event is detected. With a logic level high, charge switch Q1 turns off after two successive overvoltage events are detected. |
| 4 | Discharge Current Limit Shutdown Delay | A capacitor connects from this pin to ground and is used to program a time delay from when the discharge current limit is exceeded to when discharge switch Q2 is turned off. |
| 5 | Low-Side Discharge Current Limit Input | This pin is used to monitor the load induced voltage drop that appears across current sensing resistor $\mathrm{R}_{\lim (\mathrm{LS})}$. This voltage drop is sensed by pins 13 and 5 . |
| 6 | Charge Interrupt Mode Select | The logic level that is applied to this input determines if the charge current will be interrupted during the cell voltage sampling period. The charge current is interrupted when this input is connected to $\mathrm{V}_{\mathrm{C}}$, and not interrupted when connected to ground, pin 13. |
| 7 | Discharge Gate Drive Output | This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging. |
| 8 | Charge and Discharge Gate Drive Common | This pin provides a gate turn-off path for charge switch Q1. The charge switch source and the battery pack positive terminal connect to this point. |
| 9 | Charge Gate Drive Output | This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging. |
| 10 | Undervoltage Fault Output | This is an open drain output that is active low when an undervoltage fault limit has been exceeded. Discharge switch Q2 will turn off 16 seconds after the Fault goes low. |
| 11 | High-Side Discharge Current Limit Threshold | A resistor connects from this pin to ground and is used to program the high-side discharge current limit threshold. The programmed threshold voltage is sensed by pins 16 and 8. |
| 12 | Cell 2 | This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and the negative terminal of Cell 3. |
| 13 | Ground | This is the protection IC ground and all voltage ratings are with respect to this pin. |
| 14 | Balance 2 | This pin is used if cell balancing is desired. It connects to the drain of an internal N-channel MOSFET and is active low during the balancing of Cell 2. |
| 15 | Cell $1 / \mathrm{V}_{\mathrm{C}}$ | This is a multi-function pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2 . This pin also provides bias for the internal logic. |
| 16 | $\mathrm{V}_{\mathrm{CC}} /$ High-Side Discharge Current Limit | This is a multi-function pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 3 and to provide positive supply voltage for the protection IC. This pin can also be used for high-side discharge current limit protection by monitoring the load induced voltage drop that appears across the on-resistance of switches Q2 and diode of Q1. This voltage drop is sensed by pins 16 and 8 . |
| 17 | NC | No Connection |
| 18 | Cell 3 | This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 3 and $\mathrm{V}_{\mathrm{CC}}$. |
| 19 | Balance 3 | This pin is used if cell balancing is desired. It connects to the drain of an internal P-channel MOSFET and is active high during the balancing of Cell 3. |
| 20 | Balance 1 | This pin is used if cell balancing is desired. It connects to the drain of an internal $N$-channel MOSFET and is active low during the balancing of Cell 1. |

PROTECTION CIRCUIT OPERATING MODE TABLE

|  |  | Outputs |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | MOSFET Switches <br> (Note 3) |  | Cell <br> Balancing |
| Input Conditions <br> Cell Status | Circuit Operation <br> Battery Pack Status | Charge <br> Q1 | Discharge <br> Q2 | Balancing <br> Outputs |

CELL CHARGING/DISCHARGING

| Storage or Nominal Operation: <br> No current or voltage faults | Both Charge MOSFET Q1 and Discharge MOSFET <br> Q2 are on. The battery pack is available for charging <br> or discharging. | On | On |
| :--- | :--- | :--- | :--- |

CELL CHARGING FAULT/RESET

| Charge Voltage Limit Fault: <br> $\mathrm{V}_{\text {Cell }} \geq \mathrm{V}_{\text {th(ov) }}$ for $\mathrm{t}_{\text {dly (OV) }}$ $\mathrm{t}_{\mathrm{dly}(\mathrm{OV})}=$ <br> 0 to 1.2 s , Pin 3 to 13 <br> 1.0 to 2.1 s , Pin 3 to 15 | Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal hysteresis voltage is generated when the overvoltage cell is sensed. The shutdown delay is programmable for either one or two successive overvoltage events by the state of Pin 3 . The battery pack is available for discharging. | On to Off | On | Active |
| :---: | :---: | :---: | :---: | :---: |
| Charge Voltage Limit Reset: <br> $\mathrm{V}_{\text {Cell }}<\left(\mathrm{V}_{\text {th }(\mathrm{OV})}-\mathrm{V}_{\mathrm{H}}\right)$ for 1.2 s | Charge MOSFET Q1 will turn on when the voltage across the overvoltage cell falls sufficiently to overcome the internal hysteresis voltage. This can be accomplished by applying a load to the battery pack. | Off to On | On | Active |

CELL DISCHARGING FAULT/RESET

| Discharge Current Limit Fault: <br> $\mathrm{V}_{\text {Pin } 16} \geq\left(\mathrm{V}_{\text {Pin } 8}+\mathrm{Vth}_{\text {(HS dschg) }}\right.$ <br> for $t_{\text {dly }}$ (HS dschg) or <br> $\mathrm{V}_{\text {Pin } 5} \geq\left(\mathrm{V}_{\text {Pin } 13}+\mathrm{V}_{\text {th }(\text { LS dschg })}\right.$ <br> for $\mathrm{t}_{\text {dly }}$ (LS dschg) | Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $\mathrm{V}_{\text {Pin 16 }}$ exceeds $\mathrm{V}_{\text {Pin } 8}$ by $\approx \mathrm{V}_{\mathrm{TH} \text { (HSdschrg) }}$. A discharge current limit fault can be activated by either high-side or a low-side current sensing methods. The battery pack is available for charging. | On | On to Off | Active |
| :---: | :---: | :---: | :---: | :---: |
| Discharge Current Limit Reset: $\begin{aligned} & V_{\text {Pin } 16}-V_{\text {Pin } 8}<V_{T H(H S d s c h r g)} \\ & V_{\text {Pin } 5}-V_{\text {Pin } 13}<V_{T H(L S d s c h r g)} \end{aligned}$ | The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{\text {Pin } 16}$ no longer exceeds $\mathrm{V}_{\text {Pin } 8}$ by 2.0 V . This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. | On | Off to On | Active |
| Discharge Voltage Limit Fault: $\mathrm{V}_{\text {Cell }} \leq \mathrm{V}_{\mathrm{th}(\mathrm{UV})} \text { for } 2.1 \mathrm{~s}$ | Undervoltage Fault Output (Pin 10) is driven low after two successive undervoltage events are detected. After a 16 second delay, discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging. | On | On to Off after 16 s | Disabled |
| Discharge Voltage Limit Reset: $V_{\text {Pin } 8}>\left(V_{\text {Pin 16 }}+0.6 \mathrm{~V}\right)$ | The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $\mathrm{V}_{\text {Pin } 8}$ exceeds $\mathrm{V}_{\text {Pin } 16}$ by 0.6 V . This can be accomplished by connecting the battery pack to the charger. | On | Off to On | Active |
| FAULTY CELL |  |  |  |  |
| Simultaneous Charge and Discharge Voltage Limit Faults | This condition can happen if there is a defective cell in the battery pack. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2 , or 3 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty ( $<1.5 \mathrm{~V}$ ) the protection circuit logic will not function and the battery pack cannot be charged. | Cycles <br> Cell 1 Good <br> Disabled Cell 1 Faulty | Cycles Cell 1 Good <br> Disabled Cell 1 Faulty | Cycles <br> Cell 1 Good <br> Disabled Cell 1 Faulty |

NOTE: 3 Charge switch Q1 and discharge switch Q2 can be selectively turned off via the appropriate inhibit input except during the sleepmode state.

## INTRODUCTION

The demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Today's most attractive chemistries include lithium-polymer, lithium-ion, and lithium-metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium-based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event.

The MC33351A features internally-fixed cell voltage limits, programmable cell voltage balancing, low operating current, a virtually zero current sleepmode state, and requires few external components.

## OPERATING DESCRIPTION

The MC33351A is specifically designed to be placed in the battery pack where it can be continuously powered from three lithium cells. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and discharge current, and correspondingly controls the state of two P-channel MOSFET switches. These switches, Q1 and Q2, are placed within the series path of the positive terminal of cell 3 and the positive terminal of the battery pack. For lowside current limit sense, a resistor is placed within the series path of the negative terminal of Cell 1 and the negative terminal of the battery pack. This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that a programmed voltage or current limit for any cell has been exceeded.

A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 1.

## Voltage Sensing

Individual cell voltage sensing is accomplished by the use of the Cell Selector in conjunction with the Floating Over/Under Voltage Detector and Reference block. The Cell Selector applies the voltage of each cell across an internal resistor divider string. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Selector is gated on for a 4.0 ms period at a fixed one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across each cell, thus extending the useful battery pack capacity.


Figure 12. Simplified Smart Battery Pack
Cell Sensing Sequence

| Polling <br> Sequence | Time <br> $(\mathbf{m s})$ | Cell <br> Sensed | Tested <br> Limit |
| :---: | :---: | :---: | :---: |
| 1 | 0.25 | Cell 1 | Overvoltage |
| 2 | 0.25 | Cell 2 | Overvoltage |
| 3 | 0.25 | Cell 3 | Overvoltage |
| 4 | 0.25 | Cell 1 | Undervoltage |
| 5 | 0.25 | Cell 2 | Undervoltage |
| 6 | 0.25 | Cell 3 | Undervoltage |

By incorporating this polling technique with a single floating comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.


Figure 13. Cell Voltage Limit Sampling

## vs. Programming

The cell charge and discharge voltage limits are controlled by the values selected for the internal resistor divider string. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition on the first cell that exceeds the pre-set overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal current source pull-up is then applied to the lower tap of the divider when the overvoltage cell is again sensed. This creates an input hysteresis voltage with divider resistors R1 and R2. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across the highest voltage cell falls below the hysteresis level, charge MOSFET Q1 will turn on and the current source pull-up will turn off. The battery pack will now be available for charging or discharging.

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition on the first cell that falls below the designed undervoltage limit. After an undervoltage cell is detected, undervoltage fault output goes low and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load after 16 seconds. The protection circuit will now enter a low current sleepmode state drawing less than 15.0 nA typically, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. An alternate method of turning discharge MOSFET Q2 can be employed using $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$ as shown in Figures 1 and 2. Recommended value of $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$ of $5.1 \mathrm{k} \Omega$ and $22 \mu \mathrm{fd}$ respectively generates a time delay of 110 $\pm 10 \%$ milliseconds.

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 8 exceeds Pin 16 by 0.6 V , discharge MOSFET Q2 will be turned on. The battery pack will now be available for charging or discharging.

## Cell Voltage Balancing

With series connected cells, successive charge and discharge cycles can result in a significant difference in cell voltage with a corresponding degradation of battery pack
capacity. Figure 13 illustrates the operation of an unbalanced three cell pack. As the cells become unbalanced, the full battery pack capacity is not realized. This is due to the requirement that charging must terminate when the highest voltage cell reaches the overvoltage limit, and discharging must terminate when the lowest voltage cell reaches the undervoltage limit. By employing a method of keeping the cell voltages equal, each of the cells can be charged and discharged to their specified limits, thus attaining the maximum possible capacity.


Figure 14. Unbalanced Battery Pack Operation
The MC33351A contains a Cell Voltage Balancing Logic circuit that controls three internal MOSFETs. These MOSFETs are connected to an external transistor and resistor combination across the individual cells. The circuit samples the voltage of each cell during the polling period. If all of the cells are below the programmed overvoltage fault limit, no cell balancing takes place. If one or more cells reach the overvoltage fault limit, a specific latch is set for each cell. At the end of the polling period, charge MOSFET Q1 is turned off and the latches are interrogated. If all of the latches were set, no cell balancing takes place. If one, two, or three latches were set, the required cell balancing MOSFETs are then activated. The overvoltage cells are discharged to the pre-set level. As each cell attains this level, the balancing MOSFETs successively turn off. Upon completion of cell balancing, charge MOSFET Q1 is turned on. Cell voltage balancing can be active during charging and discharging, but is disabled during the low current sleepmode state.

## Test Mode

A test option is provided to speed up device and battery pack testing. By connecting Pin 2 to 3.0 V above $V_{C}$ the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the Control Logic becomes active and the cell are polled within 4.0 ms .

## Discharge Current Sensing

Discharge current limit protection can be selectively added to the battery pack with the addition of a sense resistor $\mathrm{R}_{\mathrm{lim}(\mathrm{dschg})}$ on the Low-Side or by monitoring the voltage drop across the series FETs on the High-Side.
Sense resistor - low-side
The sense resistor $\mathrm{R}_{\mathrm{lim}(\mathrm{dschg})}$ is placed in series with the negative terminal of Cell 1 and the negative terminal of the battery pack, Refer to Figure 1.

As the battery pack discharges, Pins 5 and 13 sense the voltage drop across $\mathrm{R}_{\text {Lim(dschg) }}$.

A discharge current limit fault is detected if the voltage at Pin 5 is greater than Pin 13 by $\mathbf{5 0} \mathbf{m V}$ for more than 3.0 ms . The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$
\mathrm{I}_{\mathrm{Lim}(\mathrm{dschg})}=\frac{\mathrm{V}_{\text {th(dschg) }}}{\mathrm{R}_{\mathrm{Lim}(\mathrm{dschg})}}=\frac{50 \mathrm{mV}}{\mathrm{R}_{\mathrm{Lim}(\mathrm{dschg})}}
$$

## Voltage across FETs - high-side

A $1 \mathrm{M} \Omega$ or $2 \mathrm{M} \Omega$ resistor connected from pin\# 11 to ground is used to program the high-side discharge current limit threshold.

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 16 no longer exceeds Pin 8 by approximately 2.0 V, the Sense Enable
circuit will turn on discharge MOSFET Q2. Discharge current sensing can be disabled by connecting Pin 16 to Pin 8.

The discharge current protection circuit contains a built in response delay of 3.0 ms . This helps to prevent fault activation when the battery pack is subjected to pulsed currents during charging or discharging.

## Battery Pack Application

Each of the application figures show a capacitor labeled $\mathrm{C}_{\mathrm{I}}$ that connects directly across the battery pack terminals, and two resistors labeled $\mathrm{R}_{\mathrm{g}}$ that are placed in series with the charge and discharge gate drive outputs. These components prevent excessive currents from flowing into the MC33351A when the battery pack terminals are shorted or arced and are mandatory. Capacitor $C_{I}$ is $\boldsymbol{a} 1.0 \mu \boldsymbol{F} \pm \mathbf{2 0 \%}$ ceramic leaded or surface mount type. It must be placed directly across the battery pack plus and minus terminals with extremely short lead lengths $(\leq 1 / 16$ ") and as close to the IC as possible. The gate drive output resistors for both Q1 and Q2 are $10 k \Omega \pm 5.0 \%$ carbon film type.
In applications where inordinately low leakage MOSFETs are used, the protection circuit may take several seconds to reset from an overcurrent fault after the load is removed. If desired, this situation can be remedied by providing a small leakage path for charging $\mathrm{C}_{\mathrm{I}}$, thus allowing Pin 8 to rapidly rise, so that it no longer exceeds Pin 16 by approximately 2.0 V . A $4.7 \mathrm{M} \Omega$ resistor placed across the MOSFET switches accomplishes this task with a minimum increase in cell discharge current when the battery pack is connected to the load.

Upon assembly of the battery pack, it is imperative that Cell 1 be connected first so that $V_{c}$ is properly biased. The remaining cells can then be connected in any order. This assembly method prevents forward biasing the protection IC substrate which can result in overheating and non-functionality.

MC33351A

MC33351A - Cell Voltage versus Undervoltage Fault


## MC33340, MC33342

## Battery Fast Charge Controllers

The MC33340 and MC33342 are monolithic control IC's that are specifically designed as fast charge controllers for Nickel Cadmium ( NiCd ) and Nickel Metal Hydride (NiMH) batteries. These devices feature negative slope voltage detection as the primary means for fast charge termination. Accurate detection is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. An additional secondary backup termination method can be selected that consists of either a programmable time or temperature limit. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout with hysteresis. Fast charge holdoff time is the only difference between the MC33340 and the MC33342. The MC33340 has a typical holdoff time of 177 seconds and the MC33342 has a typical holdoff time of 708 seconds.

- Negative Slope Voltage Detection with 4.0 mV Sensitivity
- Accurate Zero Current Battery Voltage Sensing
- High Noise Immunity with Synchronous VFC/Logic
- Programmable 1 to 4 Hour Fast Charge Time Limit
- Programmable Over/Under Temperature Detection
- Battery Over and Undervoltage Fast Charge Protection
- Power Supply Input Undervoltage Lockout with Hysteresis
- Operating Voltage Range of 3.25 V to 18 V
- 177 seconds Fast Change Hold-off Time (MC33340)
- 708 seconds Fast Change Hold-off Time (MC33342)


This device contains 2,512 active transistors.

## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com

|  |  | MARKING DIAGRAMS |
| :---: | :---: | :---: |
| $\operatorname{cin}_{8}^{-}$ | PDIP-8P SUFFIXCASE 626 |  |
|  |  | MC3334×P |
|  |  | - AWL |
|  |  | 『एすV |
|  | D SUFFIX CASE 751 |  |
|  |  |  |
|  |  |  |
| $x$ | $=0$ or 2 |  |
| A | = Assembly Location |  |
| WL, L | = Wafer Lot |  |
| $Y Y, Y=$ Year |  |  |
| WW, W= Work Week |  |  |

PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33340D | SO-8 | 98 Units/Rail |
| MC33340DR2 | SO-8 | 2500 Tape \& Reel |
| MC33340P | PDIP-8 | 50 Units/Rail |
| MC33342D | SO-8 | 98 Units/Rail |
| MC33342DR2 | SO-8 | 2500 Tape \& Reel |
| MC33342P | PDIP-8 | 50 Units/Rail |

Figure 1. Simplified Block Diagram

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage (Pin 8) | $\mathrm{V}_{\mathrm{CC}}$ | 18 | V |
| Input Voltage Range <br> Time/Temperature Select (Pins 5, 6, 7) Battery Sense, (Note 2) (Pin 1) | $\mathrm{V}_{\mathrm{IR}(\mathrm{t} T)}$ <br> $\mathrm{V}_{\mathrm{IR} \text { (sen) }}$ | $\begin{gathered} -1.0 \text { to } \mathrm{V}_{C C} \\ -1.0 \text { to } \mathrm{V}_{\mathrm{CC}}+0.6 \text { or }-1.0 \text { to } 10 \\ \hline \end{gathered}$ | V |
| $\mathrm{V}_{\text {sen }}$ Gate Output (Pin 2) <br> Voltage <br> Current | $\mathrm{V}_{\mathrm{O} \text { (gate) }}$ <br> $\mathrm{l}_{\mathrm{O}(\mathrm{gate})}$ | $\begin{aligned} & 20 \\ & 50 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Fast/Trickle Output (Pin 3) Voltage Current | $\begin{aligned} & \mathrm{V}_{\mathrm{O}(\mathrm{FT})} \\ & \mathrm{l}_{\mathrm{O}(\mathrm{FTT})} \end{aligned}$ | $\begin{aligned} & 20 \\ & 50 \end{aligned}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Thermal Resistance, Junction-to-Air P Suffix, DIP Plastic Package, Case 626 <br> D Suffix, SO-8 Plastic Package, Case 751 | $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 100 \\ & 178 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 3) | $\mathrm{T}_{\mathrm{A}}$ | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method $3015 \quad$ Machine Model Method 400 V
ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BATTERY SENSE INPUT (Pin 1) |  |  |  |  |  |
| Input Sensitivity for - $\Delta \mathrm{V}$ Detection | $-\Delta \mathrm{V}_{\text {th }}$ | - | -4.0 | - | mV |
| Overvoltage Threshold | $\mathrm{V}_{\text {th }}(\mathrm{OV})$ | 1.9 | 2.0 | 2.1 | V |
| Undervoltage Threshold | $\mathrm{V}_{\mathrm{th}(\mathrm{UV})}$ | 0.95 | 1.0 | 1.05 | mV |
| Input Bias Current | $\mathrm{I}_{\mathrm{B}}$ | - | 10 | - | nA |
| Input Resistance | $\mathrm{R}_{\text {in }}$ | - | 6.0 | - | $\mathrm{M} \Omega$ |

TIME/TEMPERATURE INPUTS (Pins 5, 6, 7)

| Programing Inputs $\left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}\right)$ <br> Input Current <br> Input Current Matching | $\mathrm{I}_{\text {in }}$ <br> $\Delta \mathrm{l}_{\text {in }}$ | -24 | -30 | -36 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage, Over and Under Temperature Comparators | $\mathrm{V}_{1 \mathrm{O}}$ | - | 5.0 | - | mV |
| Under Temperature Comparator Hysteresis (Pin 5) | $\mathrm{V}_{\mathrm{H}(\mathrm{T})}$ | - | 44 | - | mV |
| Temperature Select Threshold | $\mathrm{V}_{\mathrm{th}(\mathrm{t})}$ | - | $\mathrm{V}_{\mathrm{CC}}-0.7$ | - | V |

## INTERNAL TIMING

| Internal Clock Oscillator Frequency | fosc | - | 760 | - | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \mathrm{V}_{\text {sen }} \text { Gate Output (Pin 2) } \\ & \text { Gate Time } \\ & \text { Gate Repetition Rate } \end{aligned}$ | $\mathrm{t}_{\text {gate }}$ | - | $\begin{gathered} 33 \\ 1.38 \end{gathered}$ | - | $\begin{gathered} \mathrm{ms} \\ \mathrm{~s} \end{gathered}$ |
| $\begin{aligned} & \text { Fast Charge Holdoff from }-\Delta V \text { Detection } \\ & \text { MC33340 } \\ & \text { MC33342 } \end{aligned}$ | thold | - | $\begin{aligned} & 177 \\ & 708 \end{aligned}$ | - | s |
| $\mathrm{V}_{\text {sen }}$ GATE OUTPUT (Pin 2) |  |  |  |  |  |
| Off-State Leakage Current ( $\mathrm{V}_{\mathrm{O}}=20 \mathrm{~V}$ ) | $\mathrm{l}_{\text {off }}$ | - | 10 | - | nA |
| Low State Saturation Voltage ( $\mathrm{I}_{\text {sink }}=10 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{OL}}$ | - | 1.2 | - | V |

## FAST/TRICKLE OUTPUT (Pin 3)

| Off-State Leakage Current ( $\mathrm{V}_{\mathrm{O}}=20 \mathrm{~V}$ ) | $\mathrm{I}_{\text {off }}$ | - | 10 | - | nA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low State Saturation Voltage ( $\mathrm{l}_{\text {sink }}=10 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{OL}}$ | - | 1.0 | - | V |
| UNDERVOLTAGE LOCKOUT (Pin 8) |  |  |  |  |  |
| Start-Up Threshold ( $\mathrm{V}_{\mathrm{CC}}$ Increasing, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {th(on) }}$ | - | 3.0 | 3.25 | V |
| Turn-Off Threshold ( $\mathrm{V}_{\mathrm{CC}}$ Decreasing, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {th(off) }}$ | 2.75 | 2.85 | - | V |

TOTAL DEVICE (Pin 8)

| Power Supply Current (Pins 5, 6, 7 Open) | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Start-Up $\left(\mathrm{V}_{\mathrm{CC}}=2.9 \mathrm{~V}\right)$ |  | - | 0.65 | 2.0 | mA |
| Operating $\left(\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}\right)$ |  | - | 0.61 | 2.0 |  |

2. Whichever voltage is lower.
3. Tested junction temperature range for the MC33340/342: $\quad T_{\text {low }}=-25^{\circ} \mathrm{C} \quad \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$


Figure 2. Battery Sense Input Thresholds versus Temperature


Figure 4. Temperature Select Threshold Voltage versus Temperature


Figure 6. Undervoltage Lockout Thresholds versus Temperature


Figure 3. Oscillator Frequency versus Temperature


Figure 5. Saturation Voltage versus Sink Current $\mathrm{V}_{\text {sen }}$ Gate and Fast/Trickle Outputs

Figure 7. Supply Current versus Supply Voltage

## INTRODUCTION

Nickel Cadmium and Nickel Metal Hydride batteries require precise charge termination control to maximize cell capacity and operating time while preventing overcharging. Overcharging can result in a reduction of battery life as well as physical harm to the end user. Since most portable applications require the batteries to be charged rapidly, a primary and usually a secondary or redundant charge sensing technique is employed into the charging system. It is also desirable to disable rapid charging if the battery voltage or temperature is either too high or too low. In order to address these issues, an economical and flexible fast charge controller was developed.

The MC33340/342 contains many of the building blocks and protection features that are employed in modern high performance battery charger controllers that are specifically designed for Nickel Cadmium and Nickel Metal Hydride batteries. The device is designed to interface with either primary or secondary side regulators for easy implementation of a complete charging system. A representative block diagram in a typical charging application is shown in Figure 8.

The battery voltage is monitored by the $\mathrm{V}_{\text {sen }}$ input that internally connects to a voltage to frequency converter and
counter for detection of a negative slope in battery voltage. A timer with three programming inputs is available to provide backup charge termination. Alternatively, these inputs can be used to monitor the battery pack temperature and to set the over and under temperature limits also for backup charge termination.
Two active low open collector outputs are provided to interface this controller with the external charging circuit. The first output furnishes a gating pulse that momentarily interrupts the charge current. This allows an accurate method of sampling the battery voltage by eliminating voltage drops that are associated with high charge currents and wiring resistances. Also, any noise voltages generated by the charging circuitry are eliminated. The second output is designed to switch the charging source between fast and trickle modes based upon the results of voltage, time, or temperature. These outputs normally connect directly to a linear or switching regulator control circuit in non-isolated primary or secondary side applications. Both outputs can be used to drive optoisolators in primary side applications that require galvanic isolation. Figure 9 shows the typical charge characteristics for NiCd and NiMh batteries.


Figure 8. Typical Battery Charging Application


Figure 9. Typical Charge Characteristics for NiCd and NiMh Batteries

## OPERATING DESCRIPTION

The MC33340/342 starts up in the fast charge mode when power is applied to $\mathrm{V}_{\mathrm{CC}}$. A change to the trickle mode can occur as a result of three possible conditions. The first is if the $\mathrm{V}_{\text {sen }}$ input voltage is above 2.0 V or below 1.0 V . Above 2.0 V indicates that the battery pack is open or disconnected, while below 1.0 V indicates the possibility of a shorted or defective cell. The second condition is when the MC33340/342 detects a fully charged battery by measuring a negative slope in battery voltage. The MC33340/342 recognize a negative voltage slope after the preset holdoff time ( $\mathrm{t}_{\text {hold }}$ ) has elapsed during a fast charge cycle. This indicates that the battery pack is fully charged. The third condition is either due to the battery pack being out of a programmed temperature range, or that the preset timer period has been exceeded.

There are three conditions that will cause the controller to return from trickle to fast charge mode. The first is if the $\mathrm{V}_{\text {sen }}$ input voltage moved to within the 1.0 to 2.0 V range from initially being either too high or too low. The second is if the battery pack temperature moved to within the programmed temperature range, but only from initially being too cold. Third is by cycling $\mathrm{V}_{\mathrm{CC}}$ off and then back on causing the internal logic to reset. A concise description of the major circuit blocks is given below.

## Negative Slope Voltage Detection

A representative block diagram of the negative slope voltage detector is shown in Figure 10. It includes a Synchronous Voltage to Frequency Converter, a Sample Timer, and a Ratchet Counter. The $\mathrm{V}_{\text {sen }}$ pin is the input for the Voltage to Frequency Converter (VFC), and it connects to the rechargeable battery pack terminals through a
resistive voltage divider. The input has an impedance of approximately $6.0 \mathrm{M} \Omega$ and a maximum voltage range of -1.0 V to $\mathrm{V}_{\mathrm{CC}}+0.6 \mathrm{~V}$ or 0 V to 10 V , whichever is lower. The 10 V upper limit is set by an internal zener clamp that provides protection in the event of an electrostatic discharge. The VFC is a charge-balanced synchronous type which generates output pulses at a rate of $\mathrm{F}_{\mathrm{V}}=\mathrm{V}_{\text {sen }}(24 \mathrm{kHz})$.

The Sample Timer circuit provides a 95 kHz system clock signal (SCK) to the VFC. This signal synchronizes the $\mathrm{F}_{\mathrm{V}}$ output to the other Sample Timer outputs used within the detector. At 1.38 second intervals the $\mathrm{V}_{\text {sen }}$ Gate output goes low for a 33 ms period. This output is used to momentarily interrupt the external charging power source so that a precise voltage measurement can be taken. As the $\mathrm{V}_{\text {sen }}$ Gate goes low, the internal Preset control line is driven high for 11 ms . During this time, the battery voltage at the $\mathrm{V}_{\text {sen }}$ input is allowed to stabilize and the previous $\mathrm{F}_{\mathrm{V}}$ count is preloaded. At the Preset high-to-low transition, the Convert line goes high for 22 ms . This gates the $\mathrm{F}_{\mathrm{V}}$ pulses into the ratchet counter for a comparison to the preloaded count. Since the Convert time is derived from the same clock that controls the VFC, the number of $F_{V}$ pulses is independent of the clock frequency. If the new sample has more counts than were preloaded, it becomes the new peak count and the cycle is repeated 1.38 seconds later. If the new sample has two fewer counts, a less than peak voltage event has occurred, and a register is initialized. If two successive less than peak voltage events occur, the $-\Delta \mathrm{V}$ 'AND' gate output goes high and the Fast/Trickle output is latched in a low state, signifying that the battery pack has reached full charge status.

## MC33340, MC33342

Negative slope voltage detection starts after 60 ms have elapsed in the fast charge mode. This does not affect the Fast/Trickle output until the holdoff time ( $\mathrm{t}_{\text {hold }}$ ) has elapsed during the fast charge mode. Two scenarios then exist. Trickle mode holdoff is implemented to ignore any initial drop in voltage that may occur when charging batteries that have been stored for an extended time period. If the negative slope voltage detector senses that initial drop during the holdoff time, and the input voltage rises as the battery charges, the Fast/Trickle output will remain open. However, if the negative slope voltage detector senses a negative drop
in voltage during the holdoff time and the input voltage never rises above that last detected level, the Fast/Trickle output will latch into a low state. The negative slope voltage detector has a maximum resolution of 2.0 V divided by 1023 , or 1.955 mV per count with an uncertainty of $\pm 1.0$ count. This yields a detection range of 1.955 mV to 5.865 mV . In order to obtain maximum sensing accuracy, the $\mathrm{R} 2 / \mathrm{R} 1$ voltage divider must be adjusted so that the $\mathrm{V}_{\text {sen }}$ input voltage is slightly less than 2.0 V when the battery pack is fully charged. Voltage variations due to temperature and cell manufacturing must be considered.


Figure 10. Negative Slope Voltage Detector

## Fast Charge Timer

A programmable backup charge timer is available for fast charge termination. The timer is activated by the Time/Temp Select comparator, and is programmed from the $\mathrm{t} 1 / \mathrm{T}_{\text {ref }}$ High, $\mathrm{t} 2 / \mathrm{T}_{\text {sen }}$, and $\mathrm{t} 3 / \mathrm{T}_{\text {ref }}$ Low inputs. If one or more of these inputs is allowed to go above $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$ or is left open, the comparator output will switch high, indicating that the timer feature is desired. The three inputs allow one of seven possible fast charge time limits to be selected. The programmable time limits, rounded to the nearest whole minute, are shown in Figure 11.

## Over/Under Temperature Detection

A backup over/under temperature detector is available and can be used in place of the timer for fast charge termination. The timer is disabled by the Time/Temp Select comparator when each of the three programming inputs are held below $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$.

Temperature sensing is accomplished by placing a negative temperature coefficient (NTC) thermistor in thermal contact with the battery pack. The thermistor connects to the $t 2 / \mathrm{T}_{\text {sen }}$ input which has a $30 \mu \mathrm{~A}$ current source pull-up for developing a temperature dependent voltage. The temperature limits are set by a resistor that connects from the $\mathrm{t} 1 / \mathrm{T}_{\text {ref }}$ High and the $\mathrm{t} 3 / \mathrm{T}_{\text {ref }}$ Low inputs to ground. Since all three inputs contain matched $30 \mu \mathrm{~A}$ current source pull-ups, the required programming resistor values are identical to that of the thermistor at the desired over and under trip temperature. The temperature window detector is composed of two comparators with a common input that connects to the $\mathrm{t} 2 / \mathrm{T}_{\text {sen }}$ input.

The lower comparator senses the presence of an under temperature condition. When the lower temperature limit is exceeded, the charger is switched to the trickle mode. The comparator has 44 mV of hysteresis to prevent erratic
switching between the fast and trickle modes as the lower temperature limit is crossed. The amount of temperature rise to overcome the hysteresis is determined by the thermistor's rate of resistance change or sensitivity at the under temperature trip point. The required resistance change is:

$$
\Delta \mathrm{R}\left(\mathrm{~T}_{\text {Low }} \rightarrow \mathrm{T}_{\text {High }}\right)=\frac{\mathrm{V}_{\mathrm{H}(\mathrm{~T})}}{\mathrm{I}_{\text {in }}}=\frac{44 \mathrm{mV}}{30 \mu \mathrm{~A}}=1.46 \mathrm{k}
$$

The resistance change approximates a thermal hysteresis of $2^{\circ} \mathrm{C}$ with a $10 \mathrm{k} \Omega$ thermistor operating at $0^{\circ} \mathrm{C}$. The under temperature fast charge inhibit feature can be disabled by biasing the $\mathrm{t} 3 / \mathrm{T}_{\text {ref }}$ Low input to a voltage that is greater than that present at $\mathrm{t} 2 / \mathrm{T}_{\text {sen }}$, and less than $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$. Under extremely cold conditions, it is possible that the thermistor resistance can become too high, allowing the $\mathrm{t} 2 / \mathrm{T}_{\text {sen }}$ input to go above $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$, and activate the timer. This condition can be prevented by placing a resistor in parallel with the thermistor. Note that the time/temperature threshold of $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$ is a typical value at room temperature. Refer to the Electrical Characteristics table and to Figure 4 for additional information.

The upper comparator senses the presence of an over temperature condition. When the upper temperature limit is exceeded, the comparator output sets the Over Temperature Latch and the charger is switched to trickle mode. Once the latch is set, the charger cannot be returned to fast charge, even after the temperature falls below the limit. This feature prevents the battery pack from being continuously temperature cycled and overcharged. The latch can be reset
by removing and reconnecting the battery pack or by cycling the power supply voltage.

If the charger does not require either the time or temperature backup features, they can both be easily disabled. This is accomplished by biasing the $\mathrm{t} 3 / \mathrm{T}_{\text {ref }}$ Low input to a voltage greater than $\mathrm{t} 2 / \mathrm{T}_{\text {sen }}$, and by grounding the $\mathrm{t} 1 / \mathrm{T}_{\text {ref }}$ High input. Under these conditions, the Time/Temp Select comparator output is low, indicating that the temperature mode is selected, and that the $t 2 / T_{\text {sen }}$ input is biased within the limits of an artificial temperature window.

Charging of battery packs that are used in portable power tool applications typically use temperature as the only means for fast charge termination. The MC33340/342 can be configured in this manner by constantly resetting the $-\Delta \mathrm{V}$ detection logic. This is accomplished by biasing the $\mathrm{V}_{\text {sen }}$ input to $\approx 1.5 \mathrm{~V}$ from a two resistor divider that is connected between the positive battery pack terminal and ground. The $\mathrm{V}_{\text {sen }}$ Gate output is also connected to the $\mathrm{V}_{\text {sen }}$ input. Now, each time that the Sample Timer causes the $\mathrm{V}_{\text {sen }}$ output to go low, the $\mathrm{V}_{\text {sen }}$ input will be pulled below the undervoltage threshold of 1.0 V . This causes a reset of the $-\Delta \mathrm{V}$ logic every 1.38 seconds, thus disabling detection.

## Operating Logic

The order of events in the charging process is controlled by the logic circuitry. Each event is dependent upon the input conditions and the chosen method of charge termination. A table summary containing all of the possible operating modes is shown in Figure 12.

| $\qquad$ | Programming Inputs |  |  | Time Limit Fast Charge (Minutes) |
| :---: | :---: | :---: | :---: | :---: |
|  | $\begin{gathered} \mathrm{t} 3 / \mathrm{T}_{\text {ref }} \text { Low } \\ \text { (Pin 5) } \end{gathered}$ | t2/T sen <br> (Pin 6) | $t 1 / T_{\text {ref }}$ High (Pin 7) |  |
| Time | Open | Open | Open | 283 |
| Time | Open | Open | Gnd | 247 |
| Time | Open | Gnd | Open | 212 |
| Time | Open | Gnd | Gnd | 177 |
| Time | Gnd | Open | Open | 141 |
| Time | Gnd | Open | Gnd | 106 |
| Time | Gnd | Gnd | Open | 71 |
| Temperature | 0 V to $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$ | 0 V to $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$ | 0 V to $\mathrm{V}_{\mathrm{CC}}-0.7 \mathrm{~V}$ | Timer Disabled |

Figure 11. Fast Charge Backup Termination Time/Temperature Limit

| Input Condition | Controller Operation |
| :---: | :---: |
| $\mathrm{V}_{\text {sen }}$ Input Voltage: <br> $>1.0 \mathrm{~V}$ and $<2.0 \mathrm{~V}$ | The divided down battery pack voltage is within the fast charge voltage range. The charger switches from trickle to fast charge mode as $\mathrm{V}_{\text {sen }}$ enters this voltage range, and a reset pulse is then applied to the timer and the over temperature latch. |
| $>1.0 \mathrm{~V}$ and $<2.0 \mathrm{~V}$ with two consecutive $-\Delta \mathrm{V}$ events detected after 160 s $<1.0 \mathrm{~V}$ or $>2.0 \mathrm{~V}$ | The battery pack has reached full charge and the charger switches from fast to a latched trickle mode. A reset pulse must be applied for the charger to switch back to the fast mode. The reset pulse occurs when entering the 1.0 V to 2.0 V window for $\mathrm{V}_{\text {sen }}$ or when $\mathrm{V}_{\mathrm{CC}}$ rises above 3.0 V . |
|  | The divided down battery pack voltage is outside of the fast charge voltage range. The charger switches from fast to trickle mode. |
| Timer Backup: Within time limit Beyond time limit | The timer has not exceeded the programmed limit. The charger will be in fast charge mode if $\mathrm{V}_{\text {sen }}$ and $\mathrm{V}_{\mathrm{CC}}$ are within their respective operating limits. |
|  | The timer has exceeded the programmed limit. The charger switches from fast to a latched trickle mode. |
| Temperature Backup: Within limits | The battery pack temperature is within the programmed limits. The charger will be in fast charge mode if $V_{\text {sen }}$ and $V_{C C}$ are within their respective operating limits. |
| Below lower limit | The battery pack temperature is below the programmed lower limit. The charger will stay in trickle mode until the lower temperature limit is exceeded. When exceeded, the charger will switch from trickle to fast charge mode. |
| Above upper limit | The battery pack temperature has exceeded the programmed upper limit. The charger switches from fast to a latched trickle mode. A reset signal must be applied and then released for the charger to switch back to the fast charge mode. The reset pulse occurs when entering the 1.0 V to 2.0 V window for $\mathrm{V}_{\text {sen }}$ or when $\mathrm{V}_{\mathrm{Cc}}$ rises above 3.0 V . |
| Power Supply Voltage: <br> $\mathrm{V}_{\mathrm{CC}}>3.0 \mathrm{~V}$ and $<18 \mathrm{~V}$ $\mathrm{V}_{\mathrm{CC}}>0.6 \mathrm{~V} \text { and }<2.8 \mathrm{~V}$ | This is the nominal power supply operating voltage range. The charger will be in fast charge mode if $\mathrm{V}_{\text {sen }}$, and temperature backup or timer backup are within their respective operating limits. |
|  | The undervoltage lockout comparator will be activated and the charger will be in trickle mode. A reset signal is applied to the timer and over temperature latch. |

Figure 12. Controller Operating Mode Table

## Testing

Under normal operating conditions, it would take 283 minutes to verify the operation of the 34 stage ripple counter used in the timer. In order to significantly reduce the test time, three digital switches were added to the circuitry and are used to bypass selected divider stages. Entering each of the test modes without requiring additional package pins or affecting normal device operation proved to be challenging. Refer to the timer functional block diagram in Figure 13.

Switch 1 bypasses 19 divider stages to provide a 524,288 times speedup of the clock. This switch is enabled when the $\mathrm{V}_{\text {sen }}$ input falls below 1.0 V . Verification of the programmed fast charge time limit is accomplished by measuring the propagation delay from when the $\mathrm{V}_{\text {sen }}$ input falls below 1.0 V , to when the $\mathrm{F} / \mathrm{T}$ output changes from a high-to-low state. The 71, 106, 141, 177, 212, 247 and 283 will now correspond to $8.1,12.1,16.2,20.2,24.3,28.3$ and 32.3 ms delays. It is possible to enter this test mode during operation if the equivalent battery pack voltage was to fall below 1.0 V . This will not present a problem since the device would normally switch from fast to trickle mode under these
conditions, and the relatively short variable time delay would be transparent to the user.
Switch 2 bypasses 11 divider stages to provide a 2048 times speedup of the clock. This switch is necessary for testing the 19 stages that were bypassed when switch 1 was enabled. Switch 2 is enabled when the $\mathrm{V}_{\text {sen }}$ input falls below 1.0 V and the $\mathrm{t} / \mathrm{T}_{\text {ref }}$ High input is biased at -100 mV . Verification of the 19 stages is accomplished by measuring a nominal propagation delay of 338.8 ms from when the $\mathrm{V}_{\text {sen }}$ input falls below 1.0 V , to when the $\mathrm{F} / \mathrm{T}$ output changes from a high-to-low state.
Switch 3 is a dual switch consisting of sections "A" and "B". Section "A" bypasses 5 divider stages to provide a 32 times speedup of the $\mathrm{V}_{\text {sen }}$ gate signal that is used in sampling the battery voltage. This speedup allows faster test verification of two successive $-\Delta V$ events. Section "B" bypasses 11 divider stages to provide a 2048 speedup of the trickle mode holdoff timer. Switches 3A and 3B are both activated when the $t 1 / T_{\text {ref }}$ High input is biased at -100 mV with respect to Pin 4.


Figure 13. Timer Functional Block Diagram


This application combines the MC33340/342 with an adjustable three terminal regulator to form an isolated secondary side battery charger. Regulator IC2 operates as a constant current source with R7 setting the fast charge level. The trickle charge level is set by R5. The R2/R1 divider should be adjusted so that the $\mathrm{V}_{\text {sen }}$ input is less than 2.0 V when the batteries are fully charged. The printed circuit board shown below will accept the several TO-220 style heatsinks for IC2 and are all manufactured by AAVID Engineering Inc.

Figure 14. Line Isolated Linear Regulator Charger

| AAVID \# | $\theta_{\mathrm{SA}}{ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| :---: | :---: |
| 592502B03400 | 24.0 |
| 593002B03400 | 14.0 |
| 590302B03600 | 9.2 |


(Top View)

(Bottom View)

Figure 15. Printed Circuit Board and Component Layout
(Circuit of Figure 14)


The MC33340/342 can be combined with any of the devices in the UC3842 family of current mode controllers to form a switch mode battery charger. In this example, optocouplers OC1 and OC2 are used to provide isolated control signals to the UC3842. During battery voltage sensing, OC2 momentarily grounds the Output/Compensation pin, effectively turning off the charger. When fast charge termination is reached, OC1 turns on, and grounds the lower side of R3. This reduces the peak switch current threshold of the Current Sense Comparator to a programmed trickle current level. For additional converter design information, refer to the UC3842 and UC3844 device family data sheets.

Figure 16. Line Isolated Switch Mode Charger

## MC33340, MC33342



The MC33340/342 can be used to control the MC34166 or MC34167 power switching regulators to produce an economical and efficient fast charger. These devices are capable of operating continuously in current limit with an input voltage range of 7.5 to 40 V . The typical charging current for the MC34166 and MC34167 is 4.3 A and 6.5 A respectively. Resistors R2 and R1 are used to set the battery pack fast charge float voltage. If precise float voltage control is not required, components R1, R2, R3 and C1 can be deleted, and Pin 1 must be grounded. The trickle current level is set by resistor R4. It is recommended that a redundant charge termination method be employed for end user protection. This is especially true for fast charger systems. For additional converter design information, refer to the MC34166 and MC34167 data sheets.

Figure 17. Switch Mode Fast Charger

## Power Supply Battery Charger Regulation Control Circuit

The MC33341 is a monolithic regulation control circuit that is specifically designed to close the voltage and current feedback loops in power supply and battery charger applications. This device features the unique ability to perform source high-side, load high-side, source low-side and load low-side current sensing, each with either an internally fixed or externally adjustable threshold. The various current sensing modes are accomplished by a means of selectively using the internal differential amplifier, inverting amplifier, or a direct input path. Positive voltage sensing is performed by an internal voltage amplifier. The voltage amplifier threshold is internally fixed and can be externally adjusted in all low-side current sensing applications. An active high drive output is provided to directly interface with economical optoisolators for isolated output power systems. This device is available in 8-lead dual-in-line and surface mount packages.

- Differential Amplifier for High-Side Source and Load Current Sensing
- Inverting Amplifier for Source Return Low-Side Current Sensing
- Non-Inverting Input Path for Load Low-Side Current Sensing
- Fixed or Adjustable Current Threshold in All Current Sensing Modes
- Positive Voltage Sensing in All Current Sensing Modes
- Fixed Voltage Threshold in All Current Sensing Modes
- Adjustable Voltage Threshold in All Low-Side Current Sensing Modes
- Output Driver Directly Interfaces with Economical Optoisolators
- Operating Voltage Range of 2.3 V to 16 V

Representative Block Diagram


This device contains 114 active transistors.

## MC33341

## POWER SUPPLY BATTERY CHARGER REGULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA


P SUFFIX PLASTIC PACKAGE CASE 626


D SUFFIX PLASTIC PACKAGE

CASE 751
(SO-8)

PIN CONNECTIONS

(Top View)

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| MC33341D | $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-8 |
| MC33341P |  | Plastic DIP |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage (Pin 7) | $\mathrm{V}_{\mathrm{CC}}$ | 16 | V |
| Voltage Range <br> Current Sense Input A (Pin 1) <br> Current Threshold Adjust (Pin 2) <br> Compensation (Pin 3) <br> Voltage Sense Input (Pin 5) <br> Current Sense Input B/Voltage Threshold Adjust (Pin 6) <br> Drive Output (Pin 8) | $\mathrm{V}_{\mathrm{IR}}$ | -1.0 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Drive Output Source Current (Pin 8) | $I_{\text {Source }}$ | 50 | mA |
| Thermal Resistance, Junction-to-Air P Suffix, DIP Plastic Package, Case 626 D Suffix, SO-8 Plastic Package, Case 751 | $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 100 \\ & 178 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature (Note 1) | $\mathrm{T}_{J}$ | -25 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |


| High-Side Source and Load Sensing Pin 1 to Pin 6 (Pin $1>1.6$ V) Internally Fixed Threshold Voltage (Pin $2=\mathrm{V}_{\mathrm{CC}}$ ) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ <br> Externally Adjusted Threshold Voltage (Pin $2=0 \mathrm{~V}$ ) <br> Externally Adjusted Threshold Voltage (Pin $2=200 \mathrm{mV}$ ) | $\mathrm{V}_{\mathrm{th}(\mathrm{IHS})}$ | $\begin{gathered} 187 \\ 183 \\ - \end{gathered}$ | $\begin{gathered} 197 \\ - \\ 10 \\ 180 \end{gathered}$ | $\begin{gathered} 207 \\ 211 \\ - \end{gathered}$ | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low-Side Load Sensing Pin 1 to Pin 4 (Pin $1=0 \mathrm{~V}$ to 0.8 V ) Internally Fixed Threshold Voltage (Pin $2=\mathrm{V}_{\mathrm{CC}}$ ) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ <br> Externally Adjusted Threshold Voltage (Pin $2=0 \mathrm{~V}$ ) <br> Externally Adjusted Threshold Voltage (Pin $2=200 \mathrm{mV}$ ) | $\mathrm{V}_{\text {th( }}$ LIS + ) | $\begin{gathered} 194 \\ 192 \\ \end{gathered}$ | $\begin{gathered} 200 \\ - \\ 10 \\ 180 \end{gathered}$ | $\begin{gathered} 206 \\ 208 \\ - \end{gathered}$ | mV |
| Low-Side Source Return Sensing Pin 1 to 4 (Pin $1=0 \mathrm{~V}$ to -0.2 V ) Internally Fixed Threshold Voltage (Pin $2=\mathrm{V}_{\mathrm{CC}}$ ) $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}$ <br> Externally Adjusted Threshold Voltage (Pin $2=0 \mathrm{~V}$ ) <br> Externally Adjusted Threshold Voltage (Pin $2=200 \mathrm{mV}$ ) | $\mathrm{V}_{\text {th( }}$ LSS-) | $\begin{gathered} -195 \\ -193 \\ - \end{gathered}$ | $\begin{gathered} -201 \\ - \\ -10 \\ -180 \end{gathered}$ | $\begin{gathered} -207 \\ -209 \\ - \end{gathered}$ | mV |
| Current Sense Input A (Pin 1) <br> Input Bias Current, High-Side Source and Load Sensing (Pin $2=0 \mathrm{~V}$ to $\mathrm{V}_{\text {Pin } 6} \mathrm{~V}$ ) <br> Input Bias Current, Low-Side Load Sensing (Pin $2=0 \mathrm{~V}$ to 0.8 V ) <br> Input Resistance, Low-Side Source Return Sensing (Pin $2=-0.6 \mathrm{~V}$ to 0 V ) | $\mathrm{I}_{\mathrm{IB}(\mathrm{A} H \mathrm{~S})}$ <br> $I_{\text {IB(A LS }+)}$ <br> $\mathrm{R}_{\text {in( } \mathrm{A} \text { LS-) }}$ |  | 40 <br> 10 <br> 10 | - | $\mu \mathrm{A}$ <br> nA <br> $\mathrm{k} \Omega$ |
| Current Sense Input B/Voltage Threshold Adjust (Pin 6) Input Bias Current <br> High-Side Source and Load Current Sensing (Pin $6>2.0 \mathrm{~V}$ ) Voltage Threshold Adjust (Pin 6 < 1.2 V ) | $\mathrm{IIB}_{(\mathrm{B})}$ | - | $\begin{gathered} 20 \\ 100 \end{gathered}$ |  | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{nA} \end{aligned}$ |
| Current Sense Threshold Adjust (Pin 2) Input Bias Current | $\mathrm{I}_{\mathrm{B}(1 \mathrm{th})}$ | - | 10 | - | nA |
| Transconductance, Current Sensing Inputs to Drive Output | $\mathrm{gm}_{\text {(1) }}$ | - | 6.0 | - | mhos |

NOTE: 1. Tested ambient temperature range for the MC33341: $\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$.

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DIFFERENTIAL AMPLIFIER DISABLE LOGIC (Pins 1, 6) |  |  |  |  |  |
| Logic Threshold Voltage Pin 1 (Pin $6=0 \mathrm{~V}$ ) |  |  |  |  | V |
| Enabled, High-Side Source and Load Current Sensing | $\mathrm{V}_{\text {th( }(\mathrm{IHS})}$ | - | $\geq 1.7$ | - |  |
| Disabled, Low-Side Load and Source Return Current Sensing | $\mathrm{V}_{\text {th( }}$ (LS) | - | $\leq 1.3$ | - |  |

## VOLTAGE SENSING (Pins 5, 6)

| Positive Sensing Pin 5 to Pin 4 | $\mathrm{V}_{\mathrm{th}(\mathrm{V})}$ |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Internally Fixed Threshold Voltage |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.186 | 1.210 | 1.234 | V |
| $\mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ |  | 1.174 | - | 1.246 | V |
| Externally Adjusted Threshold Voltage (Pin $6=0 \mathrm{~V})$ | - | 40 | - | mV |  |
| Externally Adjusted Threshold Voltage (Pin 6=1.2 V) |  | - | 1.175 | - | V |
| Voltage Sense, Input Bias Current (Pin 5) | $\mathrm{I}_{\mathrm{IB}(\mathrm{V})}$ | - | 10 | - | nA |
| Transconductance, Voltage Sensing Inputs to Drive Output | $\mathrm{g}_{\mathrm{m}(\mathrm{V})}$ | - | 7.0 | - | mhos |

## DRIVE OUTPUT (Pin 8)

| High State Source Voltage $\left(I_{\text {Source }}=10 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ | - | $\mathrm{V}_{\mathrm{CC}}-0.8$ | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| High State Source Current $($ Pin $8=0 \mathrm{~V})$ | $\mathrm{I}_{\text {Source }}$ | 15 | 20 | - | mA |

TOTAL DEVICE (Pin 7)

| Operating Voltage Range | $\mathrm{V}_{\mathrm{CC}}$ | 2.5 to 15 | 2.3 to 15 | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power Supply Current $\left(\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{CC}}$ | - | 300 | 600 | $\mu \mathrm{~A}$ |

NOTE: 1. Tested ambient temperature range for the $\mathrm{MC} 33341: \mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$.

## PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
| :---: | :--- | :--- |
| 1 | Current Sense Input A | This multi-mode current sensing input can be used for either source high-side, load high-side, <br> source-return low-side, or load low-side sensing. It is common to a Differential Amplifier, Inverting <br> Amplifier, and a Noninverting input path. Each of these sensing paths indirectly connect to the <br> current sense input of the Transconductance Amplifier. This input is connected to the high potential <br> side of a current sense resistor when used in source high-side, load high-side, or load low-side <br> current sensing modes. In source return low-side current sensing mode, this pin connects to the low <br> potential side of a current sense resistor. |
| 2 | Current Threshold Adjust | The current sense threshold can be externally adjusted over a range of 0 V to 200 mV with respect <br> to Pin 4, or internally fixed at 200 mV by connecting Pin 2 to VCc. |
| 3 | Compensation | This pin is connected to a high impedance node within the transconductance amplifier and is made <br> available for loop compensation. It can also be used as an input to directly control the Drive Output. <br> An active low at this pin will force the Drive Output into a high state. |
| 4 | Ground | This pin is the regulation control IC ground. The control threshold voltages are with respect to this <br> pin. |
| 5 | Voltage Sense Input | This is the voltage sensing input of the Transconductance Amplifier. It is normally connected to the <br> power supply/battery charger output through a resistor divider. The input threshold is controlled by <br> Pin 6. |
| 6 | Current Sense Input B/ <br> Voltage Threshold Adjust | This is a dual function input that is used for either high-side current sensing, or as a voltage <br> threshold adjustment for Pin 5. This input is connected to the low potential side of a current sense <br> resistor when used in source high-side or load high-side current sensing modes. In all low-side <br> current sensing modes, Pin 6 is available as a voltage threshold adjustment for Pin 5. The threshold <br> can be externally adjusted over a range of 0 V to 1.2 V with respect to Pin 4, or internally fixed at <br> 1.2 V by connecting Pin 6 to VCc. |
| 7 | VCC | This is the positive supply voltage for the regulation control IC. The typical operating voltage range is <br> 2.3 V to 15 V with respect to Pin 4. |
| 8 | Drive Output | This is a source-only output that normally connects to a linear or switching regulator control circuit. <br> This output is capable of 15 mA, allowing it to directly drive an optoisolator in primary side control <br> applications where galvanic isolation is required. |



Threshold Change versus Temperature


Figure 3. Closed-Loop Voltage Sensing Input versus Voltage Threshold Adjust


Figure 2. Current Sensing Threshold Change versus Temperature


Figure 4. Closed-Loop Current Sense Input B versus Current Threshold Adjust


Figure 6. Closed-Loop Current Sensing Input A versus Current Threshold Adjust


Figure 7. Bode Plot Voltage Sensing Inputs to Drive Output


Figure 9. Transconductance Voltage Sensing Inputs to Drive Output


Figure 11. Drive Output High State Source Saturation versus Load Current


Figure 8. Bode Plot Current Sensing Inputs to Drive Output


Figure 10. Transconductance Current Sensing Inputs to Drive Output


Figure 12. Supply Current versus Supply Voltage

## INTRODUCTION

Power supplies and battery chargers require precise control of output voltage and current in order to prevent catastrophic damage to the system load. Many present day power sources contain a wide assortment of building blocks and glue devices to perform the required sensing for proper regulation. Typical feedback loop circuits may consist of a voltage and current amplifier, level shifting circuitry, summing circuitry and a reference. The MC33341 contains all of these basic functions in a manner that is easily adaptable to many of the various power source-load configurations.

## OPERATING DESCRIPTION

The MC33341 is an analog regulation control circuit that is specifically designed to simultaneously close the voltage and current feedback loops in power supply and battery charger applications. This device can control the feedback loop in either constant-voltage or constant-current mode with automatic crossover. A concise description of the integrated circuit blocks is given below. Refer to the block diagram in Figure 13.

## Transconductance Amplifier

A quad input transconductance amplifier is used to control the feedback loop. This amplifier has separate voltage and current channels, each with a sense and a threshold input. Within a given channel, if the sense input level exceeds that of the threshold input, the amplifier output is driven high. The channel with the largest difference between the sense and threshold inputs will set the output source current of the amplifier and thus dominate control of the feedback loop. The amplifier output appears at Pin 8 and is a source-only type that is capable of 15 mA .

A high impedance node within the transconductance amplifier is made available at Pin 3 for loop compensation. This pin can sink and source up to $10 \mu \mathrm{~A}$ of current. System stability is achieved by connecting a capacitor from Pin 3 to ground. The Compensation Pin signal is out of phase with respect to the Drive Output. By actively clamping Pin 3 low, the Drive Output is forced into a high state. This, in effect, will shutdown the power supply or battery charger, by forcing the output voltage and current regulation threshold down towards zero.

## Voltage Sensing

The voltage that appears across the load is monitored by the noninverting $\mathrm{V}_{\text {sen }}$ input of the transconductance amplifier. This voltage is resistively scaled down and connected to Pin 5. The threshold at which voltage regulation occurs is set by the level present at the inverting $\mathrm{V}_{\text {th }}$ input of the transconductance amplifier. This level is controlled by Pin 6. In source high-side and load high-side current sensing modes, Pin 6 must be connected to the low potential side of current sense resistor $\mathrm{R}_{\mathrm{S}}$. Under these conditions, the voltage regulation threshold is internally fixed at 1.2 V. In source return low-side and load low-side
current sensing modes, Pin 6 is available, and can be used to lower the regulation threshold of Pin 5. This threshold can be externally adjusted over a range of 0 V to 1.2 V with respect to the IC ground at Pin 4.

## Current Sensing

Current sensing is accomplished by monitoring the voltage that appears across sense resistor $\mathrm{R}_{\mathrm{S}}$, level shifting it with respect to Pin 4 if required, and applying it to the noninverting $\mathrm{I}_{\text {sen }}$ input of the transconductance amplifier. In order to allow for maximum circuit flexibility, there are three methods of current sensing, each with different internal paths.
In source high-side (Figures 13 and 14) and load high-side (Figures 17 and 18) current sensing, the Differential Amplifier is active with a gain of 1.0. Pin 1 connects to the high potential side of current sense resistor $\mathrm{R}_{\mathrm{S}}$ while Pin 6 connects to the low side. Logic circuitry is provided to disable the Differential Amplifier output whenever low-side current sensing is required. This circuit clamps the Differential Amplifier output high which disconnects it from the $I_{\text {sen }}$ input of the Transconductance Amplifier. This happens if Pin 1 is less than 1.2 V or if Pin 1 is less than Pin 6.
With source return low-side current sensing (Figures 15 and 16), the Inverting Amplifier is active with a gain of -1.0 . Pin 1 connects to the low potential side of current sense resistor $\mathrm{R}_{\mathrm{S}}$ while Pin 4 connects to the high side. Note that a negative voltage appears across $\mathrm{R}_{\mathrm{S}}$ with respect to Pin 4.
In load low-side current sensing (Figures 19 and 20) a Noninverting input path is active with a gain of 1.0. Pin 1 connects to the high potential side of current sense resistor $\mathrm{R}_{\mathrm{S}}$ while Pin 4 connects to the low side. The Noninverting input path lies from Pin 1, through the Inverting Amplifier input and feedback resistors R, to the cathode of the output diode. With load low-side current sensing, Pin 1 will be more positive than Pin 4, forcing the Inverting Amplifier output low. This causes the diode to be reverse biased, thus preventing the output stage of the amplifier from loading the input signal that is flowing through the feedback resistors.
The regulation threshold in all of the current sensing modes is internally fixed at 200 mV with Pin 2 connected to $\mathrm{V}_{\mathrm{CC}}$. Pin 2 can be used to externally adjust the threshold over a range of 0 to 200 mV with respect to the IC ground at Pin 4.

## Reference

An internal band gap reference is used to set the 1.2 V voltage threshold and 200 mV current threshold. The reference is initially trimmed to a $\pm 1.0 \%$ tolerance at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and is guaranteed to be within $\pm 2.0 \%$ over an ambient operating temperature range of $-25^{\circ}$ to $85^{\circ} \mathrm{C}$.

## Applications

Each of the application circuits illustrate the flexibility of this device. The circuits shown in Figures 13 through 20 contain an optoisolator connected from the Drive Output at

Pin 8 to ground. This configuration is shown for ease of understanding and would normally be used to provide an isolated control signal to a primary side switching regulator controller. In non-isolated, primary or secondary side applications, a load resistor can be placed from Pin 8 to ground. This resistor will convert the Drive Output current to a voltage for direct control of a regulator.

In applications where excessively high peak currents are possible from the source or load, the load induced voltage
drop across $\mathrm{R}_{\mathrm{S}}$ could exceed 1.6 V. Depending upon the current sensing configuration used, this will result in forward biasing of either the internal $\mathrm{V}_{\mathrm{CC}}$ clamp diode, Pin 6, or the device substrate, Pin 1. Under these conditions, input series resistor R3 is required. The peak input current should be limited to 20 mA . Excessively large values for R3 will degrade the current sensing accuracy. Figure 21 shows a method of bounding the voltage drop across $\mathrm{R}_{\mathrm{S}}$ without sacrificing current sensing accuracy.


The above figure shows the MC33341 configured for source high-side current sensing allowing a common ground path between Load - and Source Return -. The Differential Amplifier inputs, Pins 1 and 6, are used to sense the load induced voltage drop that appears across resistor $\mathrm{R}_{\mathrm{S}}$. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6 . Resistor R3 is required in applications where a high peak level of reverse current is possible if the source inputs are shorted. The resistor value should be chosen to limit the input current of the internal $\mathrm{V}_{\mathrm{Cc}}$ clamp diode to less than 20 mA . Excessively large values for R 3 will degrade the current sensing accuracy.

$$
\begin{aligned}
\mathrm{V}_{\text {reg }} & =\mathrm{V}_{\mathrm{th}(\mathrm{~V})}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & \mathrm{I}_{\mathrm{reg}} & =\frac{\mathrm{V}_{\mathrm{th}(\mathrm{IHS})}^{\mathrm{R}_{\mathrm{S}}}}{} \\
& =1.2\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & & =\frac{0.2}{\mathrm{R}_{\mathrm{S}}}
\end{aligned}
$$

$$
\mathrm{R} 3=\frac{\left(\mathrm{I}_{\mathrm{pk}} \mathrm{R}_{\mathrm{S}}\right)-0.6}{0.02}
$$

Figure 13. Source High-Side Current Sensing with Internally Fixed Voltage and Current Thresholds


The above figure shows the MC33341 configured for source high-side current sensing with an externally adjustable current threshold. Operation of this circuit is similar to that of Figure 13. The current regulation threshold can be adjusted over a range of 0 V to 200 mV with respect to Pin 4.

$$
\begin{array}{rlr}
\mathrm{V}_{\mathrm{reg}} & =\mathrm{V}_{\mathrm{th}(\mathrm{~V})}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) \quad \mathrm{I}_{\mathrm{reg}}=\frac{\mathrm{V}_{\mathrm{th}(\mathrm{Pin} 2)}}{\mathrm{R}_{\mathrm{S}}} \\
& =1.2\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & \mathrm{R} 3=\frac{\left(\mathrm{I}_{\mathrm{pk}} \mathrm{R}_{\mathrm{S}}\right)-0.6}{0.02}
\end{array}
$$

Figure 14. Source High-Side Current Sensing with Externally Adjustable Current and Internally Fixed Voltage Thresholds


The above figure shows the MC33341 configured for source return low-side current sensing allowing a common power path between Source + and Load + . This configuration is especially suited for negative output applications where a common ground path, Source + to Load + , is desired. The Inverting Amplifier inputs, Pins 1 and 4, are used to sense the load induced voltage drop that appears across resistor $\mathrm{R}_{\mathrm{S}}$. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6 . Resistor R3 is required in applications where high peak levels of inrush current are possible. The resistor value should be chosen to limit the negative substrate current to less than 20 mA . Excessively large values for R3 will degrade the current sensing accuracy.

$$
\begin{aligned}
\mathrm{V}_{\text {reg }} & =\mathrm{V}_{\text {th( } \mathrm{V})}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & \mathrm{I}_{\mathrm{reg}} & =\frac{\mathrm{V}_{\text {th( }(\mathrm{LS}-)}}{\mathrm{R}_{\mathrm{S}}} \\
& =1.2\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & & =\frac{-0.2}{\mathrm{R}_{\mathrm{S}}}
\end{aligned}
$$

Figure 15. Source Return Low-Side Current Sensing with Internally Fixed Current and Voltage Thresholds


The above figure shows the MC33341 configured for source return low-side current sensing with externally adjustable voltage and current thresholds. Operation of this circuit is similar to that of Figure 15. The respective voltage and current regulation threshold can be adjusted over a range of 0 to 1.6 V and 0 V to 200 mV with respect to Pin 4.

$$
V_{\text {reg }}=V_{\text {th(Pin } 6)}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) \quad \mathrm{I}_{\text {reg }}=-\frac{\mathrm{V}_{\text {th(Pin 2) }}}{\mathrm{R}_{\mathrm{S}}} \quad \mathrm{R} 3=\frac{\left(\mathrm{I}_{\mathrm{pk}} \mathrm{R}_{\mathrm{S}}\right)-0.6}{0.02}
$$

Figure 16. Source Return Low-Side Current Sensing with Externally Adjustable Current and Voltage Thresholds


The above figure shows the MC33341 configured for load high-side current sensing allowing common paths for both power and ground, between the source and load. The Differential Amplifier inputs, Pins 1 and 6, are used to sense the load induced voltage drop that appears across resistor $\mathrm{R}_{\mathrm{S}}$. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of load current are possible from the battery or load bypass capacitor. The resistor value should be chosen to limit the input current of the internal $\mathrm{V}_{\mathrm{CC}}$ clamp diode to less than 20 mA . Excessively large values for R3 ill degrade the current sensing accuracy.

$$
\begin{array}{rlrl}
V_{\mathrm{reg}} & =\mathrm{V}_{\mathrm{th}(\mathrm{~V})}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & \mathrm{I}_{\mathrm{reg}} & =\frac{\mathrm{V}_{\mathrm{th}(I \mathrm{HS})}}{\mathrm{R}_{\mathrm{S}}} \\
& =1.2\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & =\frac{0.2}{\mathrm{R}_{\mathrm{S}}} & \mathrm{R} 3=\frac{\left(\mathrm{I}_{\mathrm{pk}} \mathrm{R}_{\mathrm{S}}\right)-0.6}{0.02} \\
\end{array}
$$

Figure 17. Load High-Side Current Sensing with Internally Fixed Current and Voltage Thresholds


The above figure shows the MC33341 configured for load high-side current sensing with an externally adjustable current threshold. Operation of this circuit is similar to that of Figure 17. The current regulation threshold can be adjusted over a range of 0 V to 200 mV with respect to Pin 4.

$$
\begin{aligned}
\mathrm{V}_{\mathrm{reg}} & =\mathrm{V}_{\mathrm{th}(\mathrm{~V})}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) \quad \mathrm{I}_{\mathrm{reg}}=\frac{\mathrm{V}_{\mathrm{th}(\mathrm{Pin} 2)}}{\mathrm{R}_{\mathrm{S}}} \\
& =1.2\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right)
\end{aligned} \quad \mathrm{R} 3=\frac{\left(\mathrm{I}_{\mathrm{pk}} \mathrm{R}_{\mathrm{S}}\right)-0.6}{0.02}
$$

Figure 18. Load High-Side Current Sensing with Externally Adjustable Current and Internally Fixed Voltage Thresholds


The above figure shows the MC33341 configured for load low-side current sensing allowing common paths for both power and ground, between the source and load. The Noninverting input paths, Pins 1 and 4, are used to sense the load induced voltage drop that appears across resistor $\mathrm{R}_{\mathrm{S}}$. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of load current are possible from the battery or load bypass capacitor. The resistor value should be chosen to limit the negative substratecurrent to less than 20 mA . Excessively large values for R3 will degrade the current sensing accuracy.

$$
\begin{array}{rlrl}
V_{\text {reg }} & =V_{\text {th }(V)}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & \mathrm{I}_{\mathrm{reg}} & =\frac{\mathrm{V}_{\mathrm{th}(\mathrm{ILS}+)}}{\mathrm{R}_{\mathrm{S}}} \\
& =1.2\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right) & & \mathrm{R} 3=\frac{\left(\mathrm{I}_{\mathrm{pk}} \mathrm{R}_{\mathrm{S}}\right)-0.6}{0.02} \\
\mathrm{R}_{\mathrm{S}}
\end{array}
$$

Figure 19. Load Low-Side Current Sensing with Internally Fixed Current and Voltage Thresholds


The above figure shows the MC33341 configured for load low-side current sensing with an externally adjustable voltage and current threshold. Operation of this circuit is similar to that of Figure 19. The respective voltage and current regulation threshold can be adjusted over a range of 0 to 1.2 V and 0 V to 200 mV , with respect to Pin 4.

$$
\mathrm{V}_{\mathrm{reg}}=\mathrm{V}_{\mathrm{th}(\operatorname{Pin} 6)}\left(\frac{\mathrm{R} 2}{\mathrm{R} 1}+1\right)
$$

$$
I_{\text {reg }}=\frac{V_{\text {th(Pin 2) }}}{R_{S}}
$$

$$
\mathrm{R} 3=\frac{\left(\mathrm{I}_{\mathrm{pk}} \mathrm{R}_{\mathrm{S}}\right)-0.6}{0.02}
$$

Figure 20. Load Low-Side Current Sensing with Externally Adjustable Current and Voltage Thresholds

## MC33341



NOTE: An excessive load induced voltage across $R_{S}$ can occur if either the source input or load output is shorted. This voltage can easily be bounded with the addition of the diodes shown without degrading the current sensing accuracy. This bounding technique can be used in any of the MC33341 applications where high peak currents are anticipated.

Figure 21. Current Sense Resistor Bounding


NOTE: Multiple outputs can be controlled by summing the error signal into a common optoisolator. The converter output with the largest voltage or current error will dominate control of the feedback loop.

Figure 22. Multiple Output Current and Voltage Regulation


Figure 23. 10 V/1.0 A Constant-Voltage Constant-Current Regulator


Figure 23 shows the MC33341 configured as a source high-side constant-voltage constant-current regulator. The regulator is designed for an output voltage of 10 V at 1.0 A . Figure 24 shows the regulator's output characteristics as the load is varied. Source return low-side, load high-side, and load low-side configurations will each exhibit a nearly identical load regulation characteristic. A heatsink is required for the MTP2955 series pass element.

Figure 24. Output Load Regulation


Figure 25 shows that the MC33341 can be configured as a high-side constant-current constant-voltage switch mode charger. This circuit operates as a step down converter. With a nominal input voltage and output load current as stated above, the switching frequency is approximately 28 kHz with and an associated conversion efficiency of 86 percent. The switching frequency will vary with changes in input voltage and load current.

Figure 25. Constant-Current Constant-Voltage Switch Mode Charger

## NCP1500

## Advance Information Dual Mode PWM/Linear BUCK Converter

The NCP1500 is a dual mode converter that operates as either a pulse width modulated (PWM) buck converter or as a linear regulator. The converter automatically transitions between the two modes. The converter operates as a PWM when a synchronization signal is present at the sync input. The converter operates as a linear regulator in the absence of a synchronization signal. The PWM mode offers excellent performance at normal to heavy loads at the sacrifice of output ripple voltage. The linear mode offers excellent noise rejection at the sacrifice of system efficiency. The user is able to select which mode will give the best performance for a given operating condition. Internal protection features include thermal shutdown with hysteresis and cycle-by-cycle current limit in the PWM mode. Additionally, the converter transitions into PFM mode at very light loads if a synchronization signal is present and an output over voltage condition is detected.

## PWM Features

- Current Mode Control with Cycle-by-Cycle Current Limit
- Nominal Synchronization Frequency of 270 to 630 kHz
- Built-in Slope Compensation


## Linear Regulator Features

- Low Output Noise


## Overall Features

- Thermal Shutdown with Hysteresis
- Digitally Programmable Output Voltage Between 4 Voltages: $1.0,1.3,1.5$, and 1.8
- Fast Transient Response
- Input Voltage Range From 2.7 V to 5.4 V
- Space Saving Micro8 Package
- Low Shutdown Current of $0.18 \mu \mathrm{~A}$ Typical

Typical Applications

- Baseband Supplies for Portable Handsets
- PDAs
- Supplies for DSP Circuitry

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MARKING DIAGRAM


A = Assembly Location
Y = Year
W = Work Week

## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP1500DMR2 | Micro8 | 4000 Tape/Reel |

[^27]

Figure 1. Typical Operating Circuit

PIN FUNCTION DESCRIPTIONS

| Pin \# | Symbol | Pin Description |
| :---: | :---: | :--- |
| 1 | SHD | Device is placed in shutdown when SHD is driven low. In shutdown mode, the internal MOSFET and output <br> are turned off. Driven to high for normal operation. This pin is floating internally and needs to be tied to a <br> fixed source externally. |
| 2 | SYN | External Synchronization Clock Signal Input. If a clock signal is present at this pin, the device will go into <br> PWM mode. If SYN is driven low, the device operates in linear mode. |
| 3 | $\mathrm{~V}_{\mathrm{O}}$ | Connected to internal voltage divider for feedback. |
| 4 | LX | Pin for the connection between the drain of the internal P-MOSFET and the external inductor. |
| 5 | $\mathrm{~V}_{\text {IN }}$ | Voltage Supply Input. Bypass with $10 \mu \mathrm{~F}$ capacitor. |
| 6 | GND | Ground. |
| 7 | CB1 | Control Bit 1 Input for output voltage level selection. Internally pulled low. |
| 8 | CB0 | Control Bit 0 Input for output voltage level selection. Internally pulled low. |

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply (Pin 5) | $\mathrm{V}_{\mathrm{IN}}$ | -0.3 to 6.0 | V |
| Input/Output Pins <br> Pin 1-4 \& Pin 7-8 | $\mathrm{V}_{\text {IO }}$ | -0.3 to 6.0 | V |
| Thermal Characteristics <br> Micro8 Plastic Package <br> Thermal Resistance Junction to Air |  |  |  |
| Operating Junction Temperature Range | $\mathrm{R}_{\theta \mathrm{JA}}$ | 240 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to +140 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\pm 2.0 \mathrm{kV}$ per JEDEC standard: JESD22-A114.
Machine Model (MM) $\pm 200$ V per JEDEC standard: JESD22-A115.
2. Latch-up Current Maximum Rating: $\pm 150 \mathrm{~mA}$ per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{IN}}=3.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=1.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, $\mathrm{Fsyn}=600 \mathrm{kHz} 50 \%$ Duty Cycle sinewave with $\mathrm{V}_{\mathrm{H}}=2.0 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{L}}=0 \mathrm{~V}$ for PWM mode; $\mathrm{T}_{\mathrm{A}}=-40$ to $85^{\circ} \mathrm{C}$ for Min/Max values, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Voltage Range | $\mathrm{V}_{\text {IN }}$ | 2.7 | - | 5.4 | V |
| Main FET Leakage Current (Pins 5 to 4) | LEAK | - |  |  | $\mu \mathrm{A}$ |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |  |  | 0.06 | 0.3 |  |

## Mode Selection Pin

| SYN "H" Input Voltage | $V_{S Y N H}$ | 1.3 | - | - |
| :--- | :---: | :---: | :---: | :---: |
| SYN "L" Input Voltage | $\mathrm{V}_{\text {SYNL }}$ | - | V |  |
| SYN "H" Input Current | $I_{\text {SYNH }}$ | - | - | 1.1 |
| SYN "L" Input Current | $I_{\text {SYNL }}$ | -0.5 | 0 | 0.5 |
| External Synchronization Frequency | $F_{\text {SYNC }}$ | 270 | - | - |

## Output Level Selection Pins

| CB "H" Input Voltage Threshold | $\mathrm{V}_{\mathrm{CBH}}$ | 0.85 | - | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| CB "L" Input Voltage Threshold | $\mathrm{V}_{\mathrm{CBL}}$ | - | - | 0.65 | V |
| CB "H" Input Current | $\mathrm{I}_{\mathrm{CBH}}$ | - | 0.1 | - | $\mu \mathrm{A}$ |
| CB "L" Input Current | $\mathrm{I}_{\mathrm{CBL}}$ | - | 0 | - | $\mu \mathrm{A}$ |

## Shutdown Pin

| SHD "H" Input Voltage Threshold | $\mathrm{V}_{\text {SHDH }}$ | 0.56 | - | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| SHD "L" Input Voltage Threshold | $\mathrm{V}_{\text {SHDL }}$ | - | - | 0.29 | V |
| SHD "H" Input Current | $\mathrm{I}_{\text {SHDH }}$ | - | 0.1 | - | $\mu \mathrm{A}$ |
| SHD "L" Input Current | $\mathrm{I}_{\text {SHDL }}$ | - | 0 | - | $\mu \mathrm{A}$ |

PWM Mode

| $\begin{gathered} \text { Output Voltage }\left(\mathrm{l}_{\mathrm{OUT}}=10 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ \text { CB0, CB1 }=(\mathrm{H}, \mathrm{H}) \\ \text { CB0, CB1 }=(\mathrm{H}, \mathrm{~L}) \\ \text { CB0, CB1 }=(\mathrm{L}, \mathrm{~L}) \\ \text { CB0, CB1 }=(\mathrm{L}, \mathrm{H}) \end{gathered}$ | $\mathrm{V}_{\text {OUT0 }}$ | $\begin{gathered} 0.95 \\ 1.235 \\ 1.425 \\ 1.71 \end{gathered}$ | $\begin{aligned} & 1.0 \\ & 1.3 \\ & 1.5 \\ & 1.8 \end{aligned}$ | $\begin{gathered} 1.05 \\ 1.365 \\ 1.575 \\ 1.89 \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Variation of Output Voltage <br> (Line (2.7-5.4 V), Load ( $15-300 \mathrm{~mA}$ ) and Temperature $\left(\mathrm{T}_{\mathrm{A}}=-40\right.$ to $85^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{V}_{\text {out }}$ | - | +/-5\% | - | $\mathrm{V}_{\text {outo }}$ |
| Minimum On-Time | $\mathrm{TON}_{\text {MIN }}$ | - | 210 | - | nsec |
| Internal PFET ON-Resistance ( $\mathrm{ILX}_{\text {l }}=400 \mathrm{~mA}, \mathrm{~V}_{\text {IN }}=2.0 \mathrm{~V}$ ) | $\mathrm{R}_{\mathrm{DS}(\mathrm{ON}) \text { _P }}$ | - | 0.65 | 1.2 | $\Omega$ |
| Main Output Switch Current Limit | lıIM | - | 800 | - | mA |

## Linear Regulator Mode (Lx shorted to Vo)

| $\begin{aligned} & \text { Output Voltage }\left(l_{\text {out }}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \text { CB0, CB1 }=(\mathrm{H}, \mathrm{H}) \\ & \mathrm{CBO}, \mathrm{CB} 1=(\mathrm{H}, \mathrm{~L}) \\ & \mathrm{CBO}, \mathrm{CB} 1=(\mathrm{L}, \mathrm{~L}) \\ & \mathrm{CBO}, \mathrm{CB1}=(\mathrm{L}, \mathrm{H}) \end{aligned}$ | $\mathrm{V}_{\text {out0 }}$ | $\begin{gathered} 0.95 \\ 1.235 \\ 1.425 \\ 1.71 \end{gathered}$ | $\begin{aligned} & 1.0 \\ & 1.3 \\ & 1.5 \\ & 1.8 \end{aligned}$ | $\begin{gathered} 1.05 \\ 1.365 \\ 1.575 \\ 1.89 \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage (Line (2.7-5.4 V), Load ( $0-10 \mathrm{~mA}$ ), and Temperature $\left(\mathrm{T}_{\mathrm{A}}=-40\right.$ to $\left.85^{\circ} \mathrm{C}\right)$ ) | $\Delta \mathrm{V}_{\text {out }}$ | - | +/-5\% | - | $\mathrm{V}_{\text {out0 }}$ |
| Startup Current Load in Linear Mode | ISTART $_{\text {LIN }}$ | 80 | - | - | mA |

Over Voltage Protection

| Output Over-Voltage Threshold in PWM Mode | VO $_{\text {PFM }}$ | - | +5.0 | +10 | $\%$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## Total Device

| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Standby (SHD tied low, $\mathrm{V}_{\mathrm{IN}}=3.6 \mathrm{~V}$, SYN tied low) $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $25^{\circ} \mathrm{C}$ |  | - | 0.18 | 0.5 |  |
| $\mathrm{T}_{\mathrm{A}}=26^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |  | - | - | 15 |  |
| PWM Mode (SHD tied high, $\mathrm{V}_{\mathrm{IN}}=3.6 \mathrm{~V}, \mathrm{~V}_{\text {out }}=1.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{CB} 0}=\mathrm{V}_{\mathrm{CB} 1}=0 \mathrm{~V}$, SYN @ $600 \mathrm{kHz} / 50 \%$ duty cycle, $\mathrm{I}_{\text {out }}=0 \mathrm{~mA}$ ) |  | - | 96 | 150 |  |
| Linear Mode (SHD tied high, $\mathrm{V}_{\mathrm{IN}}=3.6 \mathrm{~V}, \mathrm{~V}_{\text {out }}=1.5 \mathrm{~V}$, SYN tied low, $\left.\mathrm{I}_{\text {out }}=0 \mathrm{~mA}\right)$ |  | - | 30 | 70 |  |



| Component | Value | Manufacturer |
| :--- | :---: | :---: |
| C1, C2 | $10 \mu \mathrm{~F}, 6.3 \mathrm{~V}$ | TDK, C3216X5R0J106M |
| L | $15 \mu \mathrm{H}$ | Cooper, SD12-150 <br> SD20-150 <br> Coilcraft, D01606T-153 |

Figure 2. Typical Circuit with the Internal Schematic

## DETAILED OPERATING DESCRIPTION

## Introduction

The NCP1500 is a dual mode regulator intended for use in baseband supplies for portable equipment. Its unique features provide power to the baseband circuitry while, at the same time save valuable battery energy. When the handset is idle, the user can activate the linear regulator function. In this mode, the regulator provides a regulated low current, low noise output voltage keeping the baseband circuit biased. When the handset is in its normal operating mode, the regulator synchronizes to the baseband clock and turns into a switching regulator. This allows the regulator to provide efficient power to the baseband circuit.

## Operating Description

## Synchronization Protocol and Mode Selection

The NCP1500 has a SYNC input. The device operates at a fixed switch frequency determined by the frequency of the synchronization signal applied. The part automatically operates in PWM mode after synchronization pulses are present for several cycles, regardless of the pulse width. The NCP1500 will output 2 pulses when a sync signal is present. The first is a PWM pulse. This pulse 'sets' a latch that initiates output switch conduction. The width of this pulse controls the minimum on time in PWM mode. The second signal is a slope compensation ramp. A ramp signal is generated. This signal is summed with the current information before being fed into the PWM comparator. The purpose of this circuit is to provide stable operation at output switch duty cycles in excess of $50 \%$. The device automatically switches to linear mode when the SYNC signal is removed for approximately $6.0 \mu \mathrm{sec}$. It is recommended that the sync signal be externally pulled low to enable the linear mode. Pulling the pin high or open may cause portions of the circuit to remain active, increasing the total current consumption of the IC. The threshold level of the SYNC signal is typically 1.3 V . The duty cycle of the sync signal must be within 20 to $80 \%$.


Figure 3. Timing Diagram of the SYNC Signal

Figure 3 shows the waveform when the SYNC signal is applied. After several cycles, the MODE select changes and PWM operation is activated with the internal clock signal.

## Reference/Shutdown

The NCP1500 uses an internal reference, typically at 0.8 V . An external shutdown pin is provided. When this pin is pulled low, the reference and other circuitry are disabled, placing the part into a low quiescent current standby mode. In this mode, the pass device is off and the output voltage will be zero. The typical standby current is $0.18 \mu \mathrm{~A}$.

## Error Amplifier/Output Voltage Program

A fully compensated error amplifier is provided inside the NCP1500. No external circuitry is required to stabilize the operation of the NCP1500. The error amplifier provides an error signal to both the PWM circuit and the linear regulator circuit. The output of the error amplifier is directly connected to the linear regulator control circuit. However, the output of the error amplifier is connected first to a subtraction circuit before going to the input of the PWM comparator. The subtraction circuit is activated only during an over current condition. During this condition, a signal proportional to the amount of over current is subtracted from the error amplifier signal. This subtraction results in a lower signal applied to the PWM comparator, thus lowering the output duty cycle.
The output voltage is digitally programmable up to four voltages. Two program pins are provided to accomplish this task. The program pins control a mux, which switch a bank of resistors. The appropriate resistor bank is switched to the error amplifier input, depending on the program input. The following truth table can be used to program the output voltage:

| CB0 | CB1 | Output Voltage |
| :---: | :---: | :---: |
| 0 | 0 | 1.5 |
| 0 | 1 | 1.8 |
| 1 | 0 | 1.3 |
| 1 | 1 | 1.0 |

Both program pins are internally pulled low. Thus, if the input pins are left open, the output voltage will be 1.5 V .

## PWM Section

The PWM section consists of a PWM comparator, set dominant latch, slope compensation circuit, current sense circuit, and current limit circuit.

The NCP1500 operates as a current mode regulator in PWM mode. In this mode, a PWM pulse from the synchronization section initiates the output switch conduction. Output switch conduction is terminated when the peak inductor current reaches a threshold level established by the error amplifier. The output switch conduction duty cycle is allowed to go to $100 \%$ to increase transient load response when going from light load to heavy load.

A reset dominant latch is provided in the NCP1500. A 3 input OR gate controls the reset pin. Any one of the 3 inputs will terminate output switch conduction. Once terminated, output switch conduction cannot begin again until the next PWM pulse. Additionally, the output switch will not conduct until all 3 inputs reset to the same level. This means that the output can start to skip cycles or change to a 'PFM' mode of operation. One of the OR gate inputs can cause this

PFM mode, the over voltage detect input. Output switch conduction can begin at the next PWM cycle after the OVP input is reset.
Current mode controllers can exhibit an instability at duty cycles over $50 \%$. A slope compensation circuit is provided inside the NCP1500 to overcome the potential instability. Slope compensation consists of a ramp signal generated by the synchronization block and adding this to the current signal. The summed signal is then applied to the PWM comparator.
A current limit feature is provided in the PWM mode only. The current limit is set to allow peak switch current in excess of 800 mA . It is implemented as a cycle-by-cycle current limit. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction. An error signal is generated upon sensing an over-current condition. This signal is subtracted from the error amplifier output. This in turn reduces the PWM comparison threshold voltage, thus limiting the output duty cycle.


Figure 4. PWM Waveforms During Normal Operation

## Linear Mode Operation

The NCP1500 operates as a linear regulator if the synchronization signal is absent. The part is designed to provide up to 50 mA nominally in this mode. Transients of up to 100 mA can be accommodated if the thermal impact is low. The main output is in series with an external inductor. This can cause a lag in the transient response of the device
when going from light load to heavy load. A bypass transistor is incorporated to release the energy stored in the inductor in order to avoid oscillation within the operation range. ${ }^{\mathrm{PP}}$
The following figure shows the transient step load response of the NCP1500 in this mode of operation. NOTE: PP - Patent Pending


Figure 5. Load Transient Response in Linear Mode

## Over Voltage Protection

NCP1500 has an overvoltage protection circuit that protects the output during the PWM mode. Normally, in PWM mode, the output switch will conduct at the onset of every synchronization pulse. The minimum output duty cycle is $3 \%$. The output voltage will rise at minimum duty cycle and a light load or no load condition is present at the output. If the output rises more than $5 \%$ of the programmed
voltage, an overvoltage comparator will trip. This signal will reset the PWM latch and hold it in a reset condition until the output voltage decays below its threshold. The output will then be allowed to switch at the next synchronization pulse. This type of operation is usually referred to as PFM or skip mode operation.
The following figure is a simulation of the regulator during this condition:


Figure 6. Waveforms of PFM Mode Operation During Over Voltage

## Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event at the maximum junction temperature is exceeded. When activated, typically at $150^{\circ} \mathrm{C}$, the PWM latch is reset and the linear regulator control circuitry is disabled. The thermal shutdown circuit is designed with $25^{\circ} \mathrm{C}$ of hysteresis. This means that the

PWM latch and the regulator control circuitry cannot be re-enabled until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended as a substitute for proper heatsinking. The NCP1500 is contained in the Micro8 package.


Figure 7. Power-Up and Power-Down Sequence

## APPLICATIONS INFORMATION



Figure 8. Efficiency in Linear Mode Operation vs. Input Voltage (IOUT $=10 \mathrm{~mA}$ )


Figure 10. Output Voltage vs. Output Current in PWM Mode


Figure 9. Output Voltage vs. Output Current in LDO Mode


Figure 11. PWM Efficiency

Table 3. Efficiency Measurement in PWM Mode

| $V_{\text {OUT }}$ <br> (V) | $\begin{aligned} & V_{\mathbf{I N}} \\ & \text { (V) } \end{aligned}$ | $\mathrm{I}_{\text {OUt ( }}(\mathrm{mA})$ |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | 1 | 5 | 10 | 20 | 30 | 40 | 60 | 80 | 100 | 200 | 300 |
| 1.5 | 2.5 | 44\% | 75\% | 82\% | 86\% | 87\% | 88\% | 88\% | 88\% | 90\% | 84\% | 80\% |
|  | 3.0 | 44\% | 68\% | 76\% | 82\% | 84\% | 85\% | 86\% | 86\% | 86\% | 83\% | 80\% |
|  | 3.6 | 49\% | 62\% | 71\% | 79\% | 80\% | 83\% | 83\% | 84\% | 84\% | 82\% | 80\% |
|  | 4.2 | 51\% | 64\% | 66\% | 75\% | 77\% | 80\% | 81\% | 82\% | 82\% | 82\% | 79\% |
| 1.8 | 2.5 | 48\% | 79\% | 86\% | 90\% | 90\% | 91\% | 91\% | 91\% | 91\% | 87\% | 84\% |
|  | 3.0 | 41\% | 73\% | 80\% | 85\% | 88\% | 88\% | 89\% | 89\% | 89\% | 86\% | 84\% |
|  | 3.6 | 45\% | 64\% | 76\% | 83\% | 84\% | 86\% | 86\% | 87\% | 87\% | 85\% | 84\% |
|  | 4.2 | 52\% | 63\% | 71\% | 78\% | 81\% | 83\% | 84\% | 85\% | 85\% | 85\% | 83\% |

NOTE: See figure 1 for circuit configuration.
$\mathrm{C}_{\text {in }}=\mathrm{C}_{\text {out }}=\mathrm{C} 3216 \mathrm{X} 5 \mathrm{R} 106 \mathrm{M}$
L = D01606T-153

## CS5361

## Battery Charger Buck Controller

The CS5361 is a high voltage step down controller that provides a simple way to build a battery charger suited for various types of batteries. With an operating range of up to 30 V , it can be used to charge a multiple number of cells from a DC voltage, as is supplied by high AC-DC adapter voltages. Proprietary $\mathrm{I}^{2}$ architecture ensures full control over both Average and Peak charging currents. Independent voltage loop allows for precision regulation of the battery voltage. Average current outer control loop provides tight regulation and easy loop compensation while pulse by pulse inner control provides for fast response.

The CS5361 is designed to provide a high performance, full-featured battery charger that is simple to use. A 4.2 V reference with $0.8 \%$ tolerance can be used to implement $1.0 \%$ accurate output voltages. It also features an additional pulse-by-pulse current limit input to allow for fast output current control.

The CS5361 operates over a 7.0 V to 30 V range and is available in a 16 lead surface mount narrow body.

## Features

- Switching Regulator Controller
- Synchronous Buck Regulator Topology for High Efficiency
- Top Side P-Channel Allows High Input Voltage and Requires No Charge Pump
- Pulse-by-Pulse Inner Control Loop for Fast Response
- Programmable Peak Current Limit
- True Current Soft Start
- Clamped Gate-to-Source Voltage
- Oscillator
- Constant Frequency Design
- 100 kHz to 500 kHz Adjustable Frequency
- System Power Management
- Programmable UVLO
- $2.0 \mu \mathrm{~A}$ Sleep Mode Current (Typical)
- Bias Mode Uses Top Switch to Connect Battery to Load
$-4.2 \mathrm{~V} \pm 0.8 \%$ Reference Output
- Thermal Shutdown

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CNO-16

PIN CONNECTIONS AND MARKING DIAGRAM


A =Assembly Location
YY, Y = Year
WW, W = Work Week

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5361GD16 | SO-16 | 48 Units/Rail |
| CS5361GDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, 16.8 V/2.0 A Four Cell Lithium-Ion Battery Charger with High Side Current Sensing

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance: <br> Junction-to-Case, R $\mathrm{R}_{\text {JJ }}$ Junction-to-Ambient, R ${ }_{\theta J \mathrm{JA}}$ |  | $\begin{gathered} 28 \\ 115 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\mathrm{CC}}$ | 30 V | -0.3 V | N/A | 2.0 A Peak <br> 50 mA DC |
| Positive Current Sense Input | IS+ | 30 V | -0.3 V | 1.0 mA | 1.0 mA |
| Negative Current Sense Input | IS- | 30 V | -0.3 V | 1.0 mA | 1.0 mA |
| Shutdown and UVLO Input | Enable/UVLO | 6.0 V | -0.3 V | 1.0 mA | 10 mA |
| Average Current Loop Set Point | $\mathrm{I}_{\text {AVG }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Peak Current Loop Set Point | IPEAK | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Input | $V_{\text {FB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Reference Voltage Input | $\mathrm{V}_{\text {REF(IN) }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Loop Compensation Pin | $\mathrm{V}_{\text {COMP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| High-Side FET Driver | GATE(H) | 30 V | $\begin{aligned} & -0.3 \mathrm{~V} \\ & -2.0 \mathrm{~V} \text { for } 50 \mathrm{~ns} \end{aligned}$ | 2.0 A Peak <br> 200 mA DC | 2.0 A Peak <br> 200 mA DC |
| Low-Side FET Driver | GATE(L) | 15 V | $\begin{gathered} -0.3 \mathrm{~V} \\ -2.0 \mathrm{~V} \text { for } 50 \mathrm{~ns} \end{gathered}$ | 2.0 A Peak <br> 200 mA DC | 2.0 A Peak <br> 200 mA DC |
| Current Loop Compensation Pin | $I_{\text {comp }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Power Ground | PGND | 0 V | 0 V | 2.0 A Peak <br> 200 mA DC | N/A |
| Logic Ground | LGND | 0 V | 0 V | 200 mA DC | N/A |
| Reference Voltage Output | $\mathrm{V}_{\text {REF }}$ | 6.0 V | -0.3 V | 50 mA | 50 mA |
| Oscillator Pin | OSC | 6.0 V | -0.3 V | 10 mA | 10 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<115^{\circ} \mathrm{C} ; 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<30 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=\right.$ $1.0 \mathrm{nF}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}, \mathrm{CV}_{\mathrm{CC}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {ICOMP }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Voltage Error Amplifier |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.1 | 0.27 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {COMP }}$ Source Current | $\mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V}$ to 3.3 V ; $\mathrm{V}_{\mathrm{FB}}=0.9 \mathrm{~V}$ | 68 | 100 | 170 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {COMP }}$ Sink Current | $\mathrm{V}_{\mathrm{COMP}}=0.5 \mathrm{~V}$ to 3.3 V ; $\mathrm{V}_{\mathrm{FB}}=1.1 \mathrm{~V}$ | 60 | 100 | 160 | $\mu \mathrm{A}$ |
| Open Loop DC Gain | Note 2 | 60 | 80 | 100 | dB |
| Transconductance (Gm) | - | 0.6 | 1.2 | 2.1 | $\mathrm{mA} / \mathrm{V}$ |
| Output Impedance | Note 2 | 1.4 | 8.3 | 47.6 | $\mathrm{M} \Omega$ |
| PSRR @ 1.0 kHz | Note 2 | 60 | 85 | - | dB |
| CMRR @ 1.0 kHz | Note 2 | 80 | 110 | - | dB |
| Input Voltage Offset | 1.0 V to 5.0 V | -5.0 | - | 6.5 | mV |
| $\mathrm{V}_{\text {COMP }}$ Max Voltage | $\mathrm{V}_{\mathrm{REF}(\mathrm{IN})}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=3.2 \mathrm{~V}$ | 3.9 | 5.0 | 6.5 | V |
| $\mathrm{V}_{\text {COMP }}$ Min Voltage | $\mathrm{V}_{\mathrm{REF}(\mathrm{IN})}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=3.4 \mathrm{~V}$ | - | 0.1 | 0.2 | V |

GATE(H) and GATE(L)

| High Voltage (AC) | Note 2 | $\mathrm{V}_{C C}-0.5$ | $\mathrm{V}_{\mathrm{CC}}$ | - | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Note 2 | - | 0 | 0.5 | V |
| Rise Time | $\begin{aligned} & \text { For } \mathrm{V}_{\mathrm{CC}}>10 \mathrm{~V} \text { : Note } 2 \\ & 1.0 \mathrm{~V}<\mathrm{GATE}(\mathrm{~L})<3.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CC}}-8.0 \mathrm{~V}<\mathrm{GATE}(\mathrm{H})<\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V} \text {; } \\ & \text { For } 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<10 \mathrm{~V}: \\ & 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{L})<\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}, \\ & 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{H})<\mathrm{V}_{\mathrm{CC}} 1.0 \mathrm{~V} \end{aligned}$ | - | 40 | 80 | ns |
| Fall Time | $\begin{aligned} & \text { For } \mathrm{V}_{\mathrm{CC}}>10 \mathrm{~V} \text { : Note } 2 \\ & 3.0 \mathrm{~V}>\operatorname{GATE}(\mathrm{L})>1.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CC}}-1.0 \mathrm{~V}>\operatorname{GATE}(\mathrm{H})<\mathrm{V}_{\mathrm{CC}}-8.0 \mathrm{~V} \text {; } \\ & \text { For } 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<10 \mathrm{~V}: \\ & \mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}>\operatorname{GATE}(\mathrm{L})<1.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CC}}-1.0 \mathrm{~V}>\operatorname{GATE}(\mathrm{H})>1.0 \mathrm{~V} \end{aligned}$ | - | 40 | 80 | ns |
| GATE(H) to GATE(L) Delay | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}-\operatorname{GATE}(\mathrm{H})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{~L})>2.0 \mathrm{~V} \\ & \text { Note } 2 \end{aligned}$ | 40 | 80 | 110 | ns |
| GATE(L) to GATE(H) Delay | $\begin{aligned} & \operatorname{GATE}(\mathrm{L})<2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}-\operatorname{GATE}(\mathrm{H})>2.0 \mathrm{~V} \\ & \text { Note } 2 \end{aligned}$ | 15 | 60 | 80 | ns |
| GATE(L) Clamp to GND | - | 4.0 | 5.0 | 6.0 | V |
| GATE(H) Clamp to V ${ }_{\text {CC }}$ | - | -15 | -12 | -10 | V |
| GATE(H) Sleep Clamp | $\mathrm{I}_{\text {GATE(H) }}=100 \mu \mathrm{~A}$ | - | $\mathrm{V}_{\mathrm{CC}}-0.7$ | $\mathrm{V}_{C C}-1.0$ | V |
| GATE(L) Resistance to GND | - | 20 | 50 | 100 | k $\Omega$ |
| GATE(H) Bias Clamp | $\mathrm{I}_{\mathrm{GATE}(\mathrm{H})}=10 \mu \mathrm{~A}$ to GND in Bias mode | 13 | 16 | 20 | V |
| GATE(H) Bias Current | $\operatorname{GATE}(\mathrm{H})=\mathrm{V}_{\mathrm{CC}}-5.0 \mathrm{~V}$ | 3.0 | 10 | 20 | $\mu \mathrm{A}$ |

2. Guaranteed by design, not $100 \%$ production tested.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<115^{\circ} \mathrm{C} ; 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<30 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=\right.$ $1.0 \mathrm{nF}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}, \mathrm{CV}_{\mathrm{CC}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {ICOMP }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillator |  |  |  |  |  |
| Switching Frequency | $960 \mathrm{k} \Omega$ from OSC to GND | 80 | 100 | 120 | kHz |
| Switching Frequency | $330 \mathrm{k} \Omega$ from OSC to GND | 240 | 300 | 360 | kHz |
| Switching Frequency | $185 \mathrm{k} \Omega$ from OSC to GND | 420 | 500 | 635 | kHz |
| Bias Threshold Positive | - | 2.5 | 2.75 | 3.0 | V |
| Bias Threshold Negative | - | 2.25 | 2.5 | 2.75 | V |
| Bias Threshold Hysteresis | - | 150 | 250 | 350 | mV |
| Bias Input Current | OSC $=5.0 \mathrm{~V}$ | - | - | 1.0 | $\mu \mathrm{A}$ |

## Average Current Error Amplifier

| $\mathrm{I}_{\text {AVG }}$ Bias Current | $\mathrm{I}_{\mathrm{AVG}}=0 \mathrm{~V}$ | - | 0.2 | 1.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $I_{\text {comp }}$ Source Current | $\mathrm{I}_{\text {COMP }}=0.5 \mathrm{~V}$ to 3.3 V | 18 | 25 | 32 | $\mu \mathrm{A}$ |
| $I_{\text {comp }}$ Sink Current | $\mathrm{I}_{\text {COMP }}=0.5 \mathrm{~V}$ to 3.3 V | 18 | 25 | 32 | $\mu \mathrm{A}$ |
| Set Point | $\begin{aligned} & I_{\mathrm{AVG}}=0.25 \mathrm{~V}, 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<24 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{AVG}}=2.5 \mathrm{~V}, 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<24 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 90 \end{aligned}$ | $\begin{gathered} 10 \\ 100 \end{gathered}$ | $\begin{gathered} 16.5 \\ 110 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Open Loop DC Gain | Note 3 | 60 | 80 | 100 | dB |
| Transconductance (Gm) | Note 3 | 0.2 | 0.3 | 0.7 | $\mathrm{mA} / \mathrm{V}$ |
| Output Impedance | Note 3 | 5.0 | 33 | 143 | $\mathrm{M} \Omega$ |
| PSRR @ 1.0 kHz | Note 3 | 60 | 80 | - | dB |
| $I_{\text {comp }}$ Max Voltage | $\mathrm{V}_{\mathrm{I}(\mathrm{AVG})}=3.3 \mathrm{~V}, \mathrm{IS}+=\mathrm{IS}-=0 \mathrm{~V}$ | 3.9 | 5.0 | 6.5 | V |
| ICOMP Min Voltage | $\mathrm{V}_{\mathrm{I}(\mathrm{AVG})}=0 \mathrm{~V}, \mathrm{IS}+=0.2 \mathrm{~V}$, IS- $=0 \mathrm{~V}$ | - | 0.1 | 0.2 | V |

## Current Sense Amplifier

| IS+, IS- Bias Current | IS- = IS+ = 0 V to $\mathrm{V}_{\text {CC }}(20 \mathrm{~V}$ max $)$ | -5.0 | 1.0 | 5.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset | IS- = 0 to $\mathrm{V}_{\mathrm{CC}}$ | -8.0 | - | 7.0 | mV |
| DC Gain | IS- = 1.0 V to $\mathrm{V}_{C C}$ | 23 | 25 | 27 | V/V |
| Gain Bandwidth (-3.0 dB) | Note 3 | 3.5 | 5.5 | - | MHz |
| Propagation Delay | Note 3 | - | 70 | 105 | ns |
| PSRR @ 1.0 kHz | Note 3 | 60 | 85 | - | dB |
| CMRR @ 1.0 kHz | Note 3 | 80 | 100 | - | dB |
| Input Common Mode Range | - | 0 | - | $\mathrm{V}_{\text {cc }}$ | V |
| Input Differential Mode Range | Note 3 | 0 | - | 125 | mV |

## Peak Current Comparator

| Set Point | I PEAK = 3.0 V, Duty Cycle =50\% | 90 | 100 | 110 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| I PEAK Bias Current | I PEAK $=0 \mathrm{~V}$ | - | 0.3 | 1.0 | $\mu \mathrm{~A}$ |

3. Guaranteed by design, not $100 \%$ production tested.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<115^{\circ} \mathrm{C} ; 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<30 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=\right.$ $1.0 \mathrm{nF}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}, \mathrm{CV}_{\mathrm{CC}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {ICOMP }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PWM Comparator |  |  |  |  |  |
| Transient Response | Note 4 | - | 50 | - | ns |
| ICOMP Input Resistance | - | 200 | 500 | 800 | $\Omega$ |
| Slope Compensation | Note 4 | 0.8 | 1.0 | 1.2 | V |
| Oscillator Duty Cycle | Note 4 | 85 | 90 | 95 | \% |
| Minimum Pulse Width | Note 4 | - | 150 | 200 | ns |

Enable/UVLO Management

| Enable Input Threshold | - | 2.25 | 2.5 | 2.75 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Resistance | Note 4 | 10 | 50 | 80 | $\mathrm{k} \Omega$ |
| Input Bias Current | $\mathrm{V}_{\text {ENABLE/UVLO }}=2.75 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{~A}$ |

Reference Output

| $V_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{I}_{\mathrm{V}(\mathrm{REF})}<1.0 \mathrm{~mA}$ | 4.166 | 4.2 | 4.234 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\text {REF }}$ Short Circuit Current | $\mathrm{V}_{\mathrm{REF}}=0 \mathrm{~V}$ | 3.0 | 6.0 | 10 | mA |

## Thermal Protection

| Over Temperature Trip Point | Note 4 | 125 | 150 | 175 | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Thermal Shutdown Hysteresis | Note 4 | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

General Electrical Specifications

| $V_{C C}$ Operating Current <br> (Non-Switching) | $\mathrm{V}_{\text {COMP }}=\mathrm{I}_{\mathrm{COMP}}=0 \mathrm{~V}$ | - | 17 | 30 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{CC}}$ Sleep Current | $\mathrm{ENABLE} / \mathrm{UVLO}=0 \mathrm{~V} ; 7.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ;$ <br> $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 2.0 | 5.0 | $\mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{CC}}$ Bias Mode Current | ENABLE/UVLO $=0 \mathrm{~V}$ | - | 50 | 75 | $\mu \mathrm{~A}$ |

4. Guaranteed by design, not $100 \%$ production tested.

CS5361

PACKAGE PIN DESCRIPTION

| Package Pin \# |  |  |
| :---: | :---: | :---: |
| SO-16 | Pin Symbol | Function |
| 1 | ENABLE/UVLO | Shutdown input. Connect to $\mathrm{V}_{\mathbb{I N}}$ through a resistor divider to program minimum operating voltage. Pull below 2.5 V to shut down the IC. |
| 2 | OSC | Oscillator pin. Place resistor to GND to set the switching frequency. Enters bias mode when pulled above 2.75 V and the ENABLE/UVLO Input is low (PFET turned ON). |
| 3 | $\mathrm{V}_{\text {REF(IN) }}$ | Reference input of the voltage error amplifier. Connect to the built-in or external reference. |
| 4 | LGND | Logic Ground. IC Substrate Connection. |
| 5 | $\mathrm{I}_{\text {COMP }}$ | Current feedback compensation network. |
| 6 | $\mathrm{V}_{\text {REF }}$ | 4.2 V Reference output voltage. Capable of sourcing 3.0 mA . |
| 7 | $\mathrm{I}_{\text {AVG }}$ | Average current control loop input. Voltage at this pin sets average output current. |
| 8 | $\mathrm{V}_{\text {COMP }}$ | Voltage feedback compensation network. |
| 9 | $\mathrm{V}_{\mathrm{FB}}$ | Voltage feedback pin. Connect a resistor divider between output and this pin to set output voltage. |
| 10 | $I_{\text {PEAK }}$ | Peak current control loop input. This input is used to set peak value of the inductor ripple current. This pin can override average current loop setting. It can be used for fast current control. |
| 11 | IS- | Negative input of the current sense amplifier. |
| 12 | IS+ | Positive input of the current sense amplifier. |
| 13 | PGND | Power Ground. |
| 14 | GATE(L) | Low-Side FET Driver. This pin is capable of delivering peak currents of 1.0 A. |
| 15 | $\mathrm{V}_{\mathrm{CC}}$ | Input power supply pin or $\mathrm{V}_{\text {CC }}$ bias. |
| 16 | GATE(H) | High-Side FET Driver. This pin is capable of delivering peak currents of 1.0 A. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## Overview

The CS5361 battery charger controller has been designed with the flexibility to charge several types of batteries, such as Lithium Ion, Nickel Cadmium, Nickel Metal Hydride and Lead Acid. The differences in chemistry between different battery types result in differing charge requirements

Lithium Ion batteries are charged with a constant voltage, current limit supply. When the battery voltage is low, the charger operates in constant current mode. When the battery voltage reaches 4.2 V , the current begins to taper off and the charger enters into constant voltage mode until the current essentially reaches zero. Nickel Cadmium and Nickel Metal Hydride batteries can be charged with a constant current profile. Lead Acid batteries are charged with a constant voltage, current limiting supply or with a constant-current supply.

For a battery charger with the capability to charge all those battery types, at least two operation modes are required: constant current mode and constant voltage mode. Synchronous operation enables designs with greater than $94 \%$ efficiency to be realized.

## Control Method

## 1. Current Control

$I^{2}$ control scheme is employed to regulate the charging current. The sense resistor senses the inductor current. A low offset, high speed Current Sense amplifier with rail-to-rail inputs amplifies the voltage across the sense resistor. The output of the amplifier ( $\mathrm{I}_{\text {SENSE }}$ ), which is proportional to the inductor current, is used as feedback for two control loops. The DC level is used by the outer loop and is fed to the Average Current Error Amplifier. The Error Amplifier compares $\mathrm{I}_{\text {SENSE }}$ to an externally set reference voltage $\mathrm{I}_{\mathrm{AVG}}$ and generates a PWM control voltage $\mathrm{I}_{\text {COMP. }}$ Charger designers can use the $\mathrm{I}_{\text {COMP }}$ pin to design the compensation for the Average Current Amplifier. The current ripple is used as the ramp signal of the PWM comparator. $\mathrm{I}^{2}$ control has inherent compensation for duty cycle in response to line voltage or load changes. Changes in line and load conditions affect the inductor current. Because the ramp signal of the PWM comparator is generated from the inductor current, the duty cycle can be adjusted on a pulse by pulse basis. Since the fast PWM control loop handles transient response, a high gain, low bandwidth error amplifier can be used to improve DC accuracy, stability and noise immunity.


Figure 3. ${ }^{\mathbf{2}}$ Control Scheme

## 2. Voltage Control

Current mode voltage control method is used to regulate the voltage. The $\mathrm{V}_{\mathrm{FB}}$ pin monitors the battery voltage. A resistor divider is used to scale the voltage down to the reference level set at the $\mathrm{V}_{\text {REF(IN) }}$ pin. CS5361 provides a $4.2 \mathrm{~V} \pm 0.8 \%$ reference voltage which can obviate the need for a resistor network if charging a single 4.2 V cell. $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{REF}(\mathrm{IN})}$ are the two inputs of the Voltage Error Amplifier. The output $\mathrm{V}_{\text {COMP }}$ is compared with the ramp signal, which is generated from the inductor current, to adjust the duty cycle. Similar to $\mathrm{I}_{\text {COMP, }} \mathrm{V}_{\text {COMP }}$ provides user with compensation capability.

## Start-Up

CS5361 provides a controlled startup of regulator output current and voltage through the Error Amplifiers and external compensation networks. The capacitor at the $\mathrm{I}_{\text {COMP }}$ output provides true current soft start. As the capacitor charges up, the Average Current Error Amplifier signal increases. The output current of the regulator ramps up in a controlled manner. The compensation network at $\mathrm{V}_{\text {COMP }}$ has the similar function, which will prevent instantaneous switching of the output voltage.

## Oscillator

The battery charger controller is designed for constant frequency operation. The user can adjust the switching frequency from 100 kHz to 500 kHz by connecting a resistor from the OSC pin to GND. This function simplifies the
selection of external components and allows the user freedom to choose switching frequency.

## Gate Drivers GATE(H) and GATE(L)

In synchronous buck operation, $\operatorname{GATE}(\mathrm{H})$ and GATE(L) drive the high-side P -channel MOSFET and the low-side N -channel MOSFET respectively. The advantage of this circuit is that no charge pump is required. The low-side FET (the synchronous rectifier) behaves like a diode but has a smaller voltage drop and improves the efficiency. A 60 ns nonoverlap dead time is added between the time when the high-side FET is turned off and when the synchronous rectifier is turned on, and vice versa. This function effectively prevents crowbar currents during switching transitions.

## Gate Voltage Clamps

Internal clamps prevent driving the external power MOSFET gate voltages to levels higher than required for complete enhancement. This improves converter efficiency by reducing gate rise time, fall time, and the losses associated with the charge and discharge of gate capacitance.

## Bias Mode

When the battery is fully charged, the charger can be shut down externally by pulling the ENABLE/UVLO pin low. When the part is off and the OSC pin is pulled above 2.75 V , the charger will enter into Bias Mode. In Bias mode, the high-side PFET turns on and connect the battery to the load so that the battery starts discharging to the load.

## 100\% Duty Cycle

The maximum duty cycle of the CS5361 is $100 \%$. This feature is useful when the input voltage is marginally higher than the output voltage. If the battery voltage is very close to the input line voltage, the controller will simply go to $100 \%$ duty cycle.

## Slope Compensation

In both current and voltage controls, the sensed inductor current signal is used as the ramp of the PWM comparator to afford fast response to line and load variations. An artificial ramp signal with negative slope generated by the oscillator is added to the two negative inputs ( $\mathrm{V}_{\text {COMP }}$ and $\mathrm{I}_{\text {COMP }}$ ) of the PWM comparator to be compared with the ramp generated by the inductor current. The output of the PWM comparator is used to control the duty cycle. This method helps stabilize the system over the whole operation duty cycle range as well as minimize response time to output current changes.

## Error Amplifier Compensation

The outputs of the Average Current Error Amplifier and the Voltage Error Amplifier are available to users. Users have the freedom to design the compensation network to improve the dynamic characteristics such as transient response time, over/undershoot, and loop stability.

## Enable/Under-Voltage Lockout

The input voltage of the charger must remain above a certain level in order to work. Control is required to ensure that the charger will not start to operate without sufficient voltage. Under-Voltage Lockout provides this protection with a comparator, which compares the input to 2.5 V . The output of the comparator enables the charger's reference voltage, which in turn controls startup of the charger. The comparator's output also controls the high-side MOSFET so that the batteries will power the load when the charger is shut off. This pin also provides the function of manual shutdown by bringing the pin below 2.5 V . Chip current in the shutdown mode is only $2.0 \mu \mathrm{~A}$.

## Peak Current Control

The Peak Current Buffer Amplifier compares the current control signal (the output of the Average Current Error Amplifier) with a preset reference voltage, which can be set externally at pin IPEAK. When output of the Error Amplifier exceeds the limit, the output of the Peak Current Buffer Amplifier goes low and clamps current control signal. Therefore, the peak current control can override the average current control. In laptop computer systems, fast reducing the charge current is required to prevent overloading the input supply when the computer switches into active mode from sleep mode. On the other hand, a trickle charging mode is required in many battery chargers either to prevent over-discharged or fully charged cells from being damaged by constant-current charging. The current for trickle charging is usually much lower than that of constant-current charging. The Peak Current Control can be utilized to implement trickle charging mode without changing the setting of the average charging current.

## Input Current Limiting

An input current limiting function can be implemented externally using a dual op-amp, a sense resistor and several resistors and capacitors. The first op-amp is configured into a differential amplifier. The second op-amp compares the amplified input current signal with a reference voltage. The output is used to clamp the $\mathrm{I}_{\text {COMP }}$ pin voltage when input current exceeds the limit. See Figure 9 for detailed implementation.


Figure 4. Key Operation Waveforms

## DESIGN GUIDELINES

## 1. Selection of the Output Inductor

The value of the output inductor can be calculated based on the inductor ripple current requirement:

$$
\begin{equation*}
\mathrm{L}=(1.0-\mathrm{D}) \times \frac{\mathrm{TS}_{\mathrm{S}} \mathrm{VUT}}{\Delta \mathrm{I}_{\mathrm{L}}} \tag{52}
\end{equation*}
$$

where $\mathrm{V}_{\text {OUT }}$ is the output voltage; $\mathrm{T}_{\mathrm{S}}$ is the period of one switching cycle; $\Delta \mathrm{I}_{\mathrm{L}}$ is the peak-to-peak inductor ripple current given by design specification; and D is the duty cycle. Because both duty cycle and the output voltage change during charging operation, the designer should determine the maximum product of $(1.0-\mathrm{D})$ and $\mathrm{V}_{\text {OUT }}$ to calculate the inductance. The peak inductor current is given by:

$$
\begin{equation*}
\mathrm{I}, \mathrm{PEAK}=\mathrm{I}_{\mathrm{O}}+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2.0} \tag{53}
\end{equation*}
$$

The peak current should not saturate the core of the inductor.

## 2. Selection of Output Capacitor

Both the output voltage ripple and the inductor current ripple determine the value of the output capacitance. The required minimum is given by:

$$
\begin{equation*}
\mathrm{C}=0.125 \times \frac{\Delta \mathrm{l}_{\mathrm{L} T \mathrm{~S}}}{\Delta \mathrm{~V}_{\mathrm{OUT}}} \tag{54}
\end{equation*}
$$

The capacitor ESR (Equivalent Series Resistance) of the capacitor also needs to be small enough to meet the ripple requirement.

$$
\begin{equation*}
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{l}_{\mathrm{L}}} \tag{55}
\end{equation*}
$$

If the ESR obtained from the above equation is smaller than the ESR specified in the capacitor manufacturer's data
sheet; several capacitors should be paralleled. The number of capacitors is determined by:

$$
\begin{equation*}
\text { Number of Capacitors }=\frac{\text { ESRPER CAP }}{\text { ESRMAX }} \tag{56}
\end{equation*}
$$

## 3. Design of Resistor Divider for Voltage Sensing

Because the internal reference voltage is 4.2 V , which is equal to the voltage of one Lithium Ion battery cell, we have:

$$
\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}=\frac{1.0}{\text { Cell Count }}
$$

The maximum input bias current of the Voltage Error Amplifier is $1.0 \mu \mathrm{~A}$, the resistor divider current should be much higher than that to ensure that there is sufficient bias current. For 4-cell charger, the output voltage is 16.8 V . If we choose $\mathrm{R} 1+\mathrm{R} 2=100 \mathrm{k} \Omega$, then

$$
\frac{16.8 \mathrm{~V}}{100 \mathrm{k} \Omega}=168 \mu \mathrm{~A} \gg 1.0 \mu \mathrm{~A}
$$

Therefore,

$$
\begin{equation*}
\mathrm{R} 2=\frac{100 \mathrm{k} \Omega}{\text { Cell Count }}, \mathrm{R} 1=100 \mathrm{k} \Omega-\mathrm{R} 2 \tag{57}
\end{equation*}
$$

R1 and R2 must be $\pm 0.1 \%$ precise resistors to meet the $\pm 1.0 \%$ overall charge voltage accuracy.

## 4. Design of Resistor Divider for Enable/Under-Voltage Lockout

The resistor divider should be so designed that the controller can be enabled at the required minimum input voltage.

$$
\frac{\mathrm{R} 4}{\mathrm{R} 3+\mathrm{R} 4}=\frac{2.5 \mathrm{~V}}{\mathrm{~V}_{\mathrm{IN}, \mathrm{MIN}}}
$$

The maximum bias current for this pin is also $1.0 \mu \mathrm{~A}$. The sum of R3 and R4 can also be chosen as $100 \mathrm{k} \Omega$, so

$$
\begin{equation*}
\mathrm{R} 4=\frac{100 \mathrm{k} \Omega \times 2.5 \mathrm{~V}}{\mathrm{VIN}, \mathrm{MIN}}, \mathrm{R} 3=100 \mathrm{k} \Omega-\mathrm{R} 4 \tag{58}
\end{equation*}
$$

## 5. Selection of Current Sense Resistor and Resistor Divider for Current Setting

The tolerance of the current sense resistor affects the accuracy of current regulation, so a sense resistor with $\pm 1.0 \%$ tolerance should be used. Since the Current Sense Amplifier is a high-speed, low voltage rail-to-rail amplifier, the value of the current sensing resistor should satisfy the following condition:

$$
\text { IPEAK } \times \text { RSENSE } \leq 125 \mathrm{mV}
$$

where 125 mV is the differential mode input range of the Current Sense Amplifier.

Therefore,

$$
\begin{equation*}
\text { RSENSE } \leq \frac{125 \mathrm{mV}}{\text { IPEAK }} \tag{59}
\end{equation*}
$$

After the value of current sense resistor is determined, the resistor divider for current setting can be designed.

$$
\frac{\mathrm{R} 6}{\mathrm{R} 5+\mathrm{R} 6}=\mathrm{IOUT} \times \text { RSENSE } \times \frac{25}{4.2 \mathrm{~V}}
$$

where IOUT is the target value of the output current.
The maximum bias current of the Current Error Amplifier is 1.0 mA . The voltage across the resistor divider is 4.2 V . If we choose $R 5+R 6=10 \mathrm{k} \Omega$, we have

$$
\frac{42}{10 \mathrm{k} \Omega}=420 \mu \mathrm{~A} \gg 1.0 \mu \mathrm{~A}
$$

Therefore,

$$
\begin{gather*}
\mathrm{R} 6=10 \mathrm{k} \Omega \times 25 \times \mathrm{IOUT} \times \frac{\mathrm{RSENSE}}{4.2 \mathrm{~V}},  \tag{60}\\
\mathrm{R} 5=10 \mathrm{k} \Omega-\mathrm{R} 6
\end{gather*}
$$

## 6. Design of Average Current Compensation Network

As mentioned before, there are two feedback loops in the $I^{2}$ control scheme. The slow outer loop provides tight regulation and easy loop compensation. The fast inner loop handles the transient response on a pulse-by-pulse basis. The design of the compensation network is based on the control-to-output transfer function with closed inner current feedback loop. In this case, "control" is the output of the Average Current Error Amplifier ( $\mathrm{I}_{\mathrm{COMP}}$ ) and "output" is the inductor current.

The approximate control-to-output transfer function for the Buck converter is given by:

$$
\begin{equation*}
\frac{\mathrm{I}_{\mathrm{L}}}{\mathrm{ICOMP}} \approx \frac{1.0+\mathrm{sC} \times(\mathrm{ESR}+\mathrm{R})}{\mathrm{R}_{\mathrm{l}}(1.0+\mathrm{sCR})\left[1.0+\mathrm{s} /\left(\omega_{\mathrm{n}} \mathrm{Q}\right)+\mathrm{s}^{2} / \omega_{\mathrm{n}}{ }^{2}\right]} \tag{61}
\end{equation*}
$$

where $R_{I}$ is the current sense gain, $\omega$ n is half of the switching frequency and

$$
\begin{equation*}
\mathrm{Q}=\frac{1.0}{\pi[(1.0+\mathrm{Se} / \mathrm{Sn}) \times(1.0-\mathrm{D})-0.5]} \tag{62}
\end{equation*}
$$

where Se is the slope of the external ramp signal and Sn is the inductor current up slope.

The transfer function is a third-order system with a double pole at half of the switching frequency and a low frequency pole. Because ESR of the output capacitor is usually very small compared to load resistor R , the zero and the low frequency pole can cancel out each other. The system degrades to second-order.

The compensation design for such a system becomes very easy. A single integrator pole gives the system high DC gain and makes it crossover with -1.0 slope. The Bode plot of the
closed loop control-to-output transfer function without and with compensation is shown in Figure 5.


Figure 5. Bode Plot of Control-to-Output Transfer Function

If a transconductance amplifier is used as the error amplifier, the integrator pole can be implemented by connecting a capacitor from the amplifier output to the ground. The compensation gain is given by:

$$
\begin{equation*}
\mathrm{F}_{\mathrm{C}}(\mathrm{~s})=\frac{\mathrm{G}}{(\mathrm{sCCOMP})} \tag{63}
\end{equation*}
$$

where G is the transconductance of the amplifier.
The total loop gain is

$$
\mathrm{T}(\mathrm{~s})=\frac{\mathrm{G}}{\mathrm{R}_{\boldsymbol{l}} \times \mathrm{sCCOMP}\left[1.0+\mathrm{s} /\left(\omega_{\mathrm{n}} \mathrm{Q}\right)+\mathrm{s}^{2} / \omega_{\mathrm{n}}^{2}\right]} \text { (64) }
$$

The value of the compensation capacitor $\mathrm{C}_{\text {COMP }}$ can be calculated if the crossover frequency is known. Generally, the crossover frequency should be chosen well below the switching frequency.

We can choose

$$
\mathrm{f} C O=1 / 6 \times \mathrm{fs}
$$

So

$$
\begin{equation*}
\mathrm{CCOMP}=\frac{\mathrm{G}}{\mathrm{R}_{\boldsymbol{l}} \times 2.0 \pi \mathrm{fCO}} \tag{65}
\end{equation*}
$$

## 7. Design of Voltage Compensation Network

For voltage, "control" is referred to the output of the Voltage Error Amplifier ( $\mathrm{V}_{\mathrm{COMP}}$ ) and "output" is the output voltage. The control-to-output transfer function with closed current loop is given by:
$\frac{V_{\text {OUT }}}{\mathrm{V}_{\mathrm{COMP}}} \approx \frac{\mathrm{R}(1.0+\mathrm{sC} \times \mathrm{ESR})}{\mathrm{R}_{\mathrm{l}}(1.0+\mathrm{sCR})\left[1.0+\mathrm{s} /\left(\omega_{\mathrm{n}} \mathrm{Q}\right)+\mathrm{s}^{2} / \omega_{\mathrm{n}}{ }^{2}\right]}$
Compare the above expression with equation (60), the transfer function of current mode voltage control has same poles as I ${ }^{2}$ control. The difference is the zero. For $\mathrm{I}^{2}$ control, the zero is determined by both ESR of the output capacitor and the load resistor and can be cancel out the low frequency pole. But for current mode voltage control, the zero is a high frequency ESR zero. The low frequency pole cannot be cancelled. So the system is third-order. The Bode plot of the control-to-output transfer function with closed current loop is illustrated in Figure 6


Figure 6. Bode Plot
For a transconductance error amplifier, a possible compensation network is shown in Figure 7. The compensation network has two poles and one zero.


Figure 7. Compensation Network
The compensation gain is given by:
$F(s)=\frac{G \times(1.0+\mathrm{sR} 1 \mathrm{C} 1)}{(\mathrm{C} 1+\mathrm{C} 2) \times \mathrm{s}[1.0+\mathrm{sR1C1C2} /(\mathrm{C} 1+\mathrm{C} 2)]}$
The integrator pole will give the system high DC gain. Use the zero to compensate the excessive phase delay caused by the low frequency pole of the control-to-output transfer function. The other pole of the compensation network should be placed around the ESR zero to make sure the amplitude decrease fast after the 0 dB crossover.


Figure 8. Additional Application Diagram, 16.8 V/2.0 A Four Cell Lithium-Ion Battery Charger with Low Side Current Sensing


Figure 9. Additional Application Diagram, 16.8 V/2.0 A Four Cell Lithium-Ion Battery Charger with High Side Current Sensing and Input Current Limiting

## Single-Cell Lithium Ion Battery Charge Controller

The NCP1800 is a constant current, constant voltage (CCCV) lithium ion battery charge controller. The external sense resistor sets the full charging current, and the termination current is $10 \%$ of the full charge current $(0.1 \mathrm{C})$. The voltage is regulated at $\pm 1 \%$ during the final charge stage. There is virtually zero drain on the battery when the input power is removed.

## Features

- Integrated Voltage and Programmable Current Regulation
- Integrated Cell Conditioning for Deeply Discharged Cell
- Integrated End of Charge Detection
- Better than 1\% Voltage Regulation
- Charger Status Output for LED or Host Processor Interface
- Charge Interrupt Input
- Safety Shutoff for Removal of Battery
- Blocking Diode Not Required with PNP Transistor
- Adjustable Charge Current Limit
- Input Over and Under Voltage Lockout
- Micro8 Package


## Applications

- Cellular Phones, PDAs
- Handheld Equipments
- Battery Operated Portable Devices


Figure 1. Typical Application
This device contains 1015 transistors.


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP1800DM41R2 | Micro8 | 4000 Units/Reel |
| NCP1800DM42R2 | Micro8 | 4000 Units/Reel |



Figure 2. NCP1800 Internal Block Diagram

PIN FUNCTION DESCRIPTIONS

| Pin | Symbol |  |
| :---: | :---: | :--- |
| 1 | ISNS | This is one of the inputs to the current regulator and the end-of-charge comparator. |
| 2 | ISEL | A resistor from this pin to ground pin sets the full charging current regulation level. |
| 3 | COMP/DIS | This is a multifunction pin that is used for compensation and can be used to interrupt charge with an <br> open drain/collector output from a microcontroller. When this pin is pulled to ground, the charge <br> current is interrupted. |
| 4 | GND | This is the ground pin of the IC. |
| 5 | VSNS | This is an input that is used to sense battery voltage and is the other input to the current regulator. It <br> also serves as the input to the battery overvoltage comparator. |
| 6 | CFLG | An open drain output that indicates the battery charging status. |
| 7 | VCC | This is a multifunction pin that powers the device and senses for over and undervoltage conditions. |
| 8 | OUT | This is a current source driver for the pass transistor. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 16 | V |
| Voltage Range for: VSNS Input ISNS Input COMP/DIS Input ISEL Input CFLG Output Out Output | - | $\begin{aligned} & -0.3 \text { to } 6.0 \\ & -0.3 \text { to } 6.0 \\ & -0.3 \text { to } 6.0 \\ & -0.3 \text { to } 6.0 \\ & -0.3 \text { to } 6.0 \\ & -0.3 \text { to } V_{C C} \end{aligned}$ | V |
| OUT Sink Current | 10 | 20 | mA |
| Thermal Resistance, Junction to Air | $\mathrm{R}_{\text {өJA }}$ | 240 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -20 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -20 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\leq 2.0 \mathrm{kV}$ per JEDEC standard: JESD22-A114.
Machine Model (MM) $\leq 200$ V per JEDEC standard: JESD22-A115.
2. Latch-up Current Maximum Rating: $\leq 150 \mathrm{~mA}$ per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$ for typical values, $-20^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ for min/max values, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Supply Voltage (Note 3) | $\mathrm{V}_{\mathrm{CC}}$ | 2.5 | - | 16 | V |
| Input Supply Current | ICC | - | 140 | 250 | $\mu \mathrm{A}$ |
| $\begin{array}{ll}\text { Regulated Output Voltage } & \text { NCP1800DM41 } \\ & \text { NCP1800DM42 }\end{array}$ | $V_{\text {REG }}$ | $\begin{aligned} & 4.059 \\ & 4.158 \end{aligned}$ | $\begin{aligned} & 4.1 \\ & 4.2 \end{aligned}$ | $\begin{aligned} & \hline 4.141 \\ & 4.242 \end{aligned}$ | V |
| Full-Charge Current Reference Voltage $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{SNS}}<4.2 \mathrm{~V}, \mathrm{R}_{\text {ISEL }}=60 \mathrm{~K} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{FCHG}}$ | 220 | 240 | 260 | mV |
| Full-Charge Current Reference Voltage Temperature Coefficient $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{SNS}}<4.2 \mathrm{~V}, \mathrm{R}_{\text {ISEL }}=60 \mathrm{~K} \Omega$ | TCV FCHG | - | -0.163 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| Pre-Charge Current Reference Voltage $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{SNS}}<3.0 \mathrm{~V}, \mathrm{R}_{\text {ISEL }}=60 \mathrm{~K} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{PCHG}}$ | 13.2 | 24 | 34.8 | mV |
| Pre- Charge Current Reference Voltage Temperature Coefficient $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{SNS}}<3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{ISEL}}=60 \mathrm{~K} \Omega$ | TCV ${ }_{\text {PCHG }}$ | - | -0.180 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| $\begin{array}{ll}\text { Pre-Charge Threshold Voltage } & \text { NCP1800DM41 } \\ & \text { NCP1800DM42 }\end{array}$ | $\mathrm{V}_{\text {PCTH }}$ | $\begin{aligned} & \hline 2.78 \\ & 2.85 \end{aligned}$ | $\begin{gathered} 2.93 \\ 3.0 \end{gathered}$ | $\begin{aligned} & 3.08 \\ & 3.15 \end{aligned}$ | V |
| $\mathrm{V}_{\text {CC }}$ Under Voltage Lockout Voltage | $\mathrm{V}_{\text {UVLO }}$ | 3.43 | 3.56 | 3.69 | V |
| Hysteresis of $\mathrm{V}_{\mathrm{CC}}$ Under Voltage Lockout ( $\mathrm{V}_{\text {UVLO }}$ ), $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 90 | 150 | 195 | mV |
| Hysteresis of $\mathrm{V}_{\mathrm{CC}}$ Under Voltage Lockout Voltage ( $\mathrm{V}_{\text {UVLO }}$ ) Temperature Coefficient | - | - | 0.261 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| End-of-Charge Voltage Reference $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{SNS}}>4.2 \mathrm{~V}, \mathrm{R}_{\mathrm{ISEL}}=60 \mathrm{~K} \Omega$ | $\mathrm{V}_{\text {EOC }}$ | 20 | 24 | 28 | mV |
| End-of-Charge Voltage Reference Temperature Coefficient $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{SNS}}>4.2 \mathrm{~V}, \mathrm{R}_{\text {ISEL }}=60 \mathrm{~K} \Omega$ | TCV ${ }_{\text {EOC }}$ | - | -0.160 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| Charge Disable Threshold Voltage ( $\mathrm{I}_{\text {comp }}=100 \mu \mathrm{~A}$ min.) | $\mathrm{V}_{\text {CDIS }}$ | - | - | 0.08 | V |
| $\mathrm{V}_{\text {CC }}$ Over Voltage Lockout | V OVLO | 6.95 | 7.20 | 7.45 | V |
| Hysteresis of $\mathrm{V}_{\mathrm{CC}}$ Over Voltage Lockout ( $\mathrm{V}_{\text {OVLO }}$ ), $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 90 | 150 | 180 | mV |
| Hysteresis of $\mathrm{V}_{\text {CC }}$ Over Voltage Lockout (V $\mathrm{V}_{\text {VLO }}$ ) Temperature Coefficient | - | - | 0.39 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| V | $\mathrm{V}_{\text {SovLO }}$ | $\begin{aligned} & 4.3 \\ & 4.4 \end{aligned}$ | $\begin{aligned} & 4.4 \\ & 4.5 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 4.6 \end{aligned}$ | V |

3. See the "External Adaptor Power Supply Voltage Selection" section of the application note to determine the minimum voltage of the charger power supplies.

ELECTRICAL CHARACTERISTICS (continued)
( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for typical values, $-20^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ for min/max values, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Hysteresis of $\mathrm{V}_{\text {SNS }}$ Over Voltage Lockout ( $\mathrm{V}_{\text {SOVLO }}$ ), $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 40 | 70 | 100 | mV |
| Hysteresis of $\mathrm{V}_{\text {SNS }}$ Over Voltage Lockout ( $\mathrm{V}_{\text {SOVLO }}$ ) Temperature Coefficient $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | - | 0.52 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| Full Charge Current Range with $\mathrm{R}_{\text {SNS }}=0.4 \Omega$ | $\mathrm{I}_{\text {REG1 }}$ | 600 | - | 1000 | mA |
| Full Charge Current Range with $\mathrm{R}_{\text {SNS }}=0.8 \Omega$ | $\mathrm{I}_{\mathrm{REG} 2}$ | 300 | - | 600 | mA |
| $\begin{aligned} & \text { Battery Drain Current }\left(\mathrm{V}_{\mathrm{SNS}}+\mathrm{I}_{\mathrm{SNS}}\right) \\ & \mathrm{V}_{\mathrm{CC}}=\mathrm{Ground}, \mathrm{~V}_{\mathrm{SNS}}=4.2 \mathrm{~V} \end{aligned}$ | IBDRN | - | - | 0.5 | $\mu \mathrm{A}$ |
| CFLG Pin Output Low Voltage (CFLG = LOW, $\mathrm{I}_{\text {CFLG }}=5.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {CFLGL }}$ | - | - | 0.35 | V |
| CFLG Pin Leakage Current (CFLG = HIGH) | $\mathrm{I}_{\text {CFLGH }}$ | - | - | 0.1 | $\mu \mathrm{A}$ |



Figure 3. Pre-Charge Threshold Voltage versus Input Supply Voltage


Figure 5. Pre-Charge Current Reference Voltage versus Battery Voltage



Figure 4. Pre-Charge Current Reference Voltage versus Input Supply Voltage


Figure 6. Full-Charge Current Reference Voltage versus Battery Voltage


Figure 9. Battery Drain Current versus Battery Voltage


Figure 11. Full-Charge Current versus Current Programming Resistor


Figure 8. End of Charge Reference Voltage versus Input Supply Voltage


Figure 10. Pre-Charge Current versus Current Programming Resistor


Figure 12. $\mathrm{V}_{\mathrm{EOC}} / \mathrm{V}_{\mathrm{FCHG}}$ versus Current Programming Resistor


Figure 13. Input Supply Current versus Input Supply Voltage


Figure 14. NCP1800 State Machine Diagram


Figure 15. NCP1800 Charging Operational Flow Chart


Figure 16. Typical Charging Algorithm

| Conditions |  |
| :---: | :---: |
| CFLG Pin  <br> Pre-Charge, Full-Charge and <br> Final Charge High-Z <br> End-of-Charge, Trickle Charge <br> and Faults Low |  |

## Operation Descriptions

The NCP1800 is a linear lithium ion (Li-ion) battery charge controller and provides the necessary control functions for charging $\mathrm{Li}-\mathrm{ion}$ batteries precisely and safely. It features the constant current and constant voltage method (CCCV) of charging.

## Conditioning and Pre-charge Phase

The NCP1800 initiates a charging cycle upon toggling the COMP/DIS to LOW or application of the valid external power source (i.e. $\mathrm{V}_{\mathrm{UVLO}}<\mathrm{V}_{\mathrm{CC}}<\mathrm{V}_{\mathrm{OVLO}}$ ) with the Li-ion battery present or when the Li-ion battery is inserted. Before a charge cycle can begin, the battery conditions are verified to be within safe limits. The battery will not be charged when its voltage is less than 0.9 V or higher than $\mathrm{V}_{\text {SOVLO }}$.

Li-ion batteries can be easily damaged when fast charged from a completely discharged state. Also, a fully discharged Li-ion battery may indicate an abnormal battery condition. With the built-in safety features of the NCP1800, the Li-ion battery pre-charges (Pre-Charge Phase) at $10 \%$ of the full rated charging current $\left(\mathrm{I}_{\mathrm{REG}}\right)$ when the battery voltage is lower than $\mathrm{V}_{\text {PCTH }}$ and the CFLG pin is HIGH. Typically, the battery voltage reaches $\mathrm{V}_{\text {PCTH }}$ in a few minutes and then the Full Charge phase begins.

## Full Charge (Current Regulation) Phase

When the battery voltage reaches $\mathrm{V}_{\mathrm{PCTH}}$, the NCP1800 begins fast charging the battery with full rate charging current $\mathrm{I}_{\text {REG }}$. The NCP1800 monitors the charging current at the $I_{\text {SNS }}$ input pin by the voltage drop across a current sense resistor, $\mathrm{R}_{\text {SNS }}$, and the charging current is maintained at $I_{\text {REG }}$ by the pass transistor throughout the full charge phase.
$\mathrm{I}_{\text {REG }}$ is determined by $\mathrm{R}_{\text {SNS }}$ and $\mathrm{R}_{\text {ISEL }}$ with the following formula:

$$
\begin{gathered}
\text { IREG }=\frac{(1.19 \times 12 \mathrm{k})}{(\mathrm{RISEL} \times \mathrm{RSNS})} \\
\text { And with } \mathrm{R}_{\mathrm{ISEL}}=60 \mathrm{k} \text { and } \mathrm{R}_{\mathrm{SNS}}=0.4 \Omega, \mathrm{I}_{\mathrm{REG}}=0.6 \mathrm{~A} .
\end{gathered}
$$

Since the external P channel MOSFET or PNP transistor is used to regulate the current to charge the battery and operates in linear mode as a linear regulator, power is dissipated in the pass transistor. Designing with a very well regulated external adaptor (e.g. $5.1 \mathrm{~V} \pm 1 \%$ ) can help to minimize the heat dissipation in the pass transistor. Care must be taken in heat sink designing in enclosed environments such as inside the battery operated portables or cellular phones.

The Full Charge phase continues until the battery voltage reaches $V_{\text {REG }}$. The NCP1800 comes in two options with $\mathrm{V}_{\text {REG }}$ thresholds of 4.1 and 4.2 V .

## Final Charge (Voltage Regulation) Phase

Once the battery voltage reaches $\mathrm{V}_{\mathrm{REG}}$, the pass transistor is controlled to regulate the voltage across the battery and the Final Charge phase (constant voltage mode) begins. Once the charger is in the Final Charge phase, the charger maintains a regulated voltage and the charging current will begin to decrease and is dependent on the state of the charge of the battery. As the battery approaches a fully charged condition, the charge current falls to a very low value.

## Trickle Charge Phase

During the Final Charge phase, the charging current continues to decrease and the NCP1800 monitors the charging current through the current sense resistor $\mathrm{R}_{\text {SNS }}$. When the charging current decreases to such a level that $\mathrm{I}_{\text {SNS }}$ $<0.1 \mathrm{X}_{\mathrm{REG}}$, the CFLG pin is set to LOW and the Trickle Charge phase begins. The charger stays in the Trickle Charge phase until any fault modes are detected or the COMP/DIS pin is pulled low to start over the charging cycle.


Figure 17. Typical Application Circuit with PNP Transistor


Figure 18. Typical Application Circuit with P Channel MOSFET

## Selecting External Components

## External Adaptor Power Supply Voltage Selection

Since the NCP1800 is using a linear, charging algorithm, the efficiency is lower. Adapter voltage selection must be done carefully in order to minimize the heat dissipation. In general, the power supply input voltage should be around 5.0 to 6.0 V . The minimum input voltage should be chosen to minimize the heat dissipation in the system. Excessively high input voltages can cause too much heat dissipation and will complicate the thermal design in applications like cellular phones. With the overvoltage protection feature of the NCP1800, input voltages higher than 7.0 V will activate the overvoltage protection circuit and disconnect the power supply input to the battery and other circuitry.

For applications with the MBT35200,

$$
\begin{aligned}
\mathrm{V}_{\mathrm{IN}(\min )>}> & \text { Li-ion regulated voltage, } \\
& \mathrm{V}_{\mathrm{REG}}+\max \mathrm{V}_{\mathrm{CE}}(\text { sat })+\text { voltage drop of RSNS } \\
> & 4.2 \mathrm{~V}+0.15 \mathrm{~V}+(0.6 \mathrm{~A})(0.4 \Omega) \\
= & 4.59 \mathrm{~V} \simeq 4.6 \mathrm{~V},
\end{aligned}
$$

(there is no blocking diode required with PNP)
For applications with the NTGS3441T1,

$$
\begin{aligned}
\mathrm{V}_{\mathrm{IN}(\min )}> & \text { Li-ion regulated voltage }, \\
& \mathrm{V}_{\mathrm{REG}}+(0.6 \mathrm{~A})\left(\mathrm{RDS}_{\mathrm{DS}(\mathrm{ON}))}\right. \\
& +\mathrm{V}_{\mathrm{F}} \text { of Schottky Diode }+ \text { voltage drop of RSNS } \\
> & 4.2 \mathrm{~V}+(0.6 \mathrm{~A})(100 \mathrm{~m} \Omega)+0.38 \mathrm{~V} \\
& +(0.6 \mathrm{~A})(0.4 \Omega)=4.88 \mathrm{~V} \simeq 4.9 \mathrm{~V}
\end{aligned}
$$

Therefore, with the PMOS application, if the output voltage accuracy is $5 \%$, then a typ. $5.2 \mathrm{~V} \pm 5 \%$ output voltage adaptor must be used.

And for a very good regulated adaptor of accuracy 1\%, 5.0 $\mathrm{V} \pm 1 \%$ output voltage adaptor can then be used. It is obvious that if tighter tolerance adaptors are used, heat dissipation can be minimized by using lower nominal voltage adaptors.

## Pass Element Selection

The pass element used with the NCP1800 can either be a PNP transistor or a P channel MOSFET. The type and size of the pass transistor is determined by input-output
differential voltage, charging current, current sense resistor and the type of blocking diode used.
The selected pass element must satisfy the following criteria:

Drop across pass element $=$

$$
\mathrm{VIN}_{\mathrm{IN}}(\min )-\text { Li-ion regulated voltage }-\mathrm{V}_{\mathrm{F}}-\mathrm{I}_{\mathrm{REG}} \times \text { RSNS }
$$

With:

$$
\begin{aligned}
\mathrm{V}_{\mathrm{IN}(\min )} & =5.0 \mathrm{~V} \\
\mathrm{~V}_{\mathrm{REG}} & =4.2 \mathrm{~V} \\
\mathrm{I} \mathrm{REG} & =0.6 \mathrm{~A} \\
\mathrm{R} \text { SNS } & =0.4 \Omega
\end{aligned}
$$

Dropout across pass element $=$

$$
5.0 \mathrm{~V}-4.2 \mathrm{~V}-0.38 \mathrm{~V}-(0.6 \mathrm{~A})(0.4 \Omega)=0.18 \mathrm{~V}
$$

When using p-channel MOSFET's, max. $\mathrm{R}_{\mathrm{DS}(\text { on })}$ should be less than $(0.18 \mathrm{~V}) /(0.6 \mathrm{~A})=0.3 \Omega$ at 0.6 A . And in PNP applications, as the blocking diode is not required, the blocking diode forward voltage drop must be neglected in the calculation.

## External Output Capacitor

Any good quality output filter can be used, independent of the capacitor's minimum ESR. However, a $10 \mu \mathrm{~F}$ tantalum capacitor or electrolytic capacitor is recommended at the output to suppress fast ramping spikes at the $\mathrm{V}_{\text {SNS }}$ input and to ensure stability for 1.0 A at full range. The capacitor should be mounted with the shortest possible lead or track length to the VSNS and GND pins.

## Current Sense Resistor

The charging current can be set by the value of the current sense resistor as in the previous formula. Proper de-rating is advised when selecting the power dissipation rating of the resistor. If necessary, $\mathrm{R}_{\text {ISEL }}$ can also be changed for proper selection of the $\mathrm{R}_{\mathrm{SNS}}$ values. Take note of the recommended full-charge current ranges specified in the electrical characteristics section. Also notice the effect of RISEL on the accuracy of pre-charge current and end-of-charge detection as noted in Figures 10 and 12, respectively.

NCP345

## Over Voltage Protection IC

The NCP345 over-voltage protection circuit (OVP) protects sensitive electronic circuitry from over-voltage transients and power supply faults when used in conjunction with an external P -channel FET. The device is designed to sense an over-voltage condition and quickly disconnect the input voltage supply from the load before any damage can occur. The OVP consists of a precise voltage reference, a comparator with hysteresis, control logic, and a MOSFET gate driver. The OVP is designed on a robust BiCMOS process and is intended to withstand voltage transients up to 30 V .

The device is optimized for applications that have an external AC/DC adapter or car accessory charger to power the product and/or recharge the internal batteries. The nominal over-voltage threshold is 6.85 V so it is suitable for single cell Li-Ion applications as well as $3 / 4$ cell NiCD/NiMH applications.

## Features

- Over-Voltage Turn-Off Time of less than $1.0 \mu \mathrm{sec}$
- Accurate Voltage Threshold of 6.85 V (nominal)
- Under-Voltage Lockout Protection
- CNTRL Input Compatible with 1.8 V Logic Levels


## Typical Applications

- Cellular Phones
- Digital Cameras
- Portable Computers and PDAs
- Portable CD and other Consumer Electronics

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


THIN SOT23-5 SN SUFFIX CASE 483

PIN CONNECTIONS \& MARKING DIAGRAM


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP345SNT1 | Thin <br> SOT23-5 | $3000 / 7^{\prime \prime}$ Reel |



Figure 1. Simplified Application Diagram


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTIONS

| Pin \# | Symbol | Pin Description |
| :---: | :---: | :--- |
| 1 | OUT | This signal drives the gate of a P-channel MOSFET. It is controlled by the voltage level on IN or the logic state <br> of the CNTTRL input. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of $\mathrm{V}_{\text {CC }}$ in <br> less than $1.0 \mu$ sec provided that gate and stray capacitance is less than 12 nF. |
| 2 | GND | Circuit Ground |

TRUTH TABLE

| IN | CNTRL | OUT |
| :---: | :---: | :---: |
| $<\mathrm{V}_{\text {th }}$ | L | GND |
| $<\mathrm{V}_{\text {th }}$ | H | VCC |
| $>\mathrm{V}_{\text {th }}$ | L | VCC |
| $>\mathrm{V}_{\text {th }}$ | H | VCC |

ABSOLUTE MAXIMUM RATINGS ${ }^{*}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$ unless otherwise noted.)

| Rating | Pin | Symbol | Min | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OUT voltage to GND | 1 | $\mathrm{V}_{\mathrm{O}}$ | -0.3 | 30 | V |
| Input and CNTRL pin voltage to GND | $\begin{aligned} & 4 \\ & 3 \end{aligned}$ | $V_{\text {input }}$ <br> $V_{\text {CNTRL }}$ | $\begin{aligned} & -0.3 \\ & -0.3 \end{aligned}$ | $\begin{aligned} & 30 \\ & 13 \end{aligned}$ | V |
| $\mathrm{V}_{\text {CC }}$ Maximum Range | 5 | $\mathrm{V}_{\text {CC(max }}$ | -0.3 | 30 | V |
| Maximum Power Dissipation at $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ | - | $\mathrm{P}_{\mathrm{D}}$ | - | 0.216 | W |
| Thermal Resistance Junction to Air | - | $\mathrm{R}_{\text {өJA }}$ | - | 300 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Junction Temperature | - | $\mathrm{T}_{\mathrm{J}}$ | - | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | - | $\mathrm{T}_{\text {A }}$ | -40 | 85 | ${ }^{\circ} \mathrm{C}$ |
| $V_{\text {CNTRL }}$ Operating Voltage | 3 | - | 0 | 5.0 | V |
| Storage Temperature Range | - | $\mathrm{T}_{\text {stg }}$ | -65 | 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD performance (HBM) $\dagger$ | all | - | 2.5 | - | kV |

* Maximum Ratings are those values beyond which damage to the device may occur.
$\dagger$ Human body model (HBM): MIL STD 883C Method $3015-7$, ( $R=1500$ ohms, $C=100 \mathrm{pf}, \mathrm{F}=3$ pulses delay 1 s ).

ELECTRICAL CHARACTERISTICS
(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$, unless otherwise noted.)

| Characteristic | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ Operating Voltage Range | $\mathrm{V}_{\mathrm{CC} \text { (opt) }}$ | 5 | 3.0 | 4.8 | 25 | V |
| Supply Current ( $\mathrm{I}_{\text {CC }}+\mathrm{I}_{\text {Input }} ; \mathrm{V}_{\text {CC }}=6.0 \mathrm{~V}$ Steady State) | - | 4,5 | - | 0.75 | 1.0 | mA |
| Input Threshold ( $\mathrm{V}_{\text {Input }}$ connected to $\mathrm{V}_{\mathrm{CC}} ; \mathrm{V}_{\text {Input }}$ increasing) | $\mathrm{V}_{\text {Th }}$ | 4 | 6.70 | 6.85 | 7.05 | V |
| Input Hysteresis ( $\mathrm{V}_{\text {Input }}$ connected to $\mathrm{V}_{\mathrm{CC}} ; \mathrm{V}_{\text {Input }}$ decreasing) | $\mathrm{V}_{\text {Hyst }}$ | 4 | 50 | 100 | 200 | mV |
| Input Impedance ( Input = $\mathrm{V}_{\text {Th }}$ ) | $\mathrm{R}_{\text {in }}$ | 4 | 70 | 150 | - | $\mathrm{k} \Omega$ |
| CNTRL Voltage High | $\mathrm{V}_{\text {ih }}$ | 3 | 1.5 | - | - | V |
| CNTRL Voltage Low | $\mathrm{V}_{\mathrm{il}}$ | 3 | - | - | 0.5 | V |
| CNTRL Current High ( $\mathrm{V}_{\text {ih }}=5.0 \mathrm{~V}$ ) | $\mathrm{l}_{\text {ih }}$ | 3 | - | 95 | 200 | $\mu \mathrm{A}$ |
| CNTRL Current Low ( $\mathrm{V}_{\mathrm{il}}=0.5 \mathrm{~V}$ ) | $\mathrm{l}_{\mathrm{il}}$ | 3 | - | 10 | 20 | $\mu \mathrm{A}$ |
| Under Voltage Lockout ( $\mathrm{V}_{\mathrm{CC}}$ decreasing) | $\mathrm{V}_{\text {Lock }}$ | 3 | 2.5 | 2.8 | 3.0 | V |
| Output Sink Current ( $\left.\mathrm{V}_{\text {CC }}<\mathrm{V}_{\text {Th }}, \mathrm{V}_{\text {OUT }}=1.0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {Sink }}$ | 1 | 10 | 33 | 50 | $\mu \mathrm{A}$ |
| Output Voltage High ( $\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$; $\mathrm{I}_{\text {Source }}=10 \mathrm{~mA}$ ) <br> Output Voltage High $\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}\right.$; $\left.\mathrm{I}_{\text {Source }}=0.25 \mathrm{~mA}\right)$ <br> Output Voltage High $\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}\right.$; $\left.\mathrm{I}_{\text {Source }}=0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {oh }}$ | 1 | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}-1.0 \\ \mathrm{~V}_{\mathrm{CC}}-0.25 \\ \mathrm{~V}_{\mathrm{CC}}-0.1 \end{gathered}$ | - | - | V |
| $\begin{aligned} & \text { Output Voltage Low } \\ & \text { (Input }<6.5 \mathrm{~V} ; \mathrm{I}_{\text {Sink }}=0 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{CNTRL}=0 \mathrm{~V} \text { ) } \end{aligned}$ | $\mathrm{V}_{\text {ol }}$ | 1 | - | - | 0.1 | V |
| Turn ON Delay - Input ( $\mathrm{V}_{\text {Input }}$ connected to $\mathrm{V}_{\mathrm{CC}} ; \mathrm{V}_{\text {Input }}$ step down signal from 8.0 to 6.0 V ; measured to $50 \%$ point of OUT)* | ToN IN | 1 | - | - | 10 | $\mu \mathrm{sec}$ |
| Turn OFF Delay - Input ( $\mathrm{V}_{\text {Input }}$ connected to $\mathrm{V}_{\mathrm{CC}} ; \mathrm{V}_{\text {Input }}$ step up signal from 6.0 to $8.0 \mathrm{~V} ; \mathrm{C}_{\mathrm{L}}=12 \mathrm{nF}$ Output $>\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}$ ) | Toff IN | 1 | - | 0.5 | 1.0 | $\mu \mathrm{sec}$ |
| Turn ON Delay - CNTRL (CNTRL step down signal from 2.0 to 0.5 V ; measured to $50 \%$ point of OUT)* | Ton Ct | 1 | - | - | 10 | $\mu \mathrm{sec}$ |
| Turn OFF Delay - CNTRL (CNTRL step up signal from 0.5 to 2.0 V ; $\mathrm{C}_{\mathrm{L}}=12 \mathrm{nF}$ Output $>\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}$ ) | T OFF CT | 1 | - | 1.0 | 2.0 | $\mu \mathrm{sec}$ |

*Turn ON Delay is guaranteed by design.


Figure 3. Typical $\mathrm{V}_{\text {th }}$ Threshold Variation vs. Temperature


Figure 4. Typical OUT Sink Current vs. Temperature $\mathrm{V}_{\text {in }}<\mathrm{V}_{\text {th }}, \mathrm{V}_{\text {out }}=1 \mathrm{~V}$


Figure 5. Typical Supply Current vs. Temperature
$I_{c c}+I_{i n}, V_{c c}=6 \mathrm{~V}$


Figure 6. Typical Turn-off Time CNTRL to VLOAD


Figure 7. Typical Turn-on Time CNTRL to VLOAD

## APPLICATION INFORMATION



Figure 8.

## Introduction

In many electronic products, an external AC/DC wall adapter is used to convert the AC line voltage into a regulated DC voltage or a current limited source. Line surges or faults in the adapter may result in over-voltage events that can damage sensitive electronic components within the product. This is becoming more critical as the operating voltages of many integrated circuits have been lowered due to advances in sub-micron silicon lithography. In addition, portable products with removable battery packs pose special problems since the pack can be removed at any time. If the user removes a pack in the middle of charging, a large transient voltage spike can occur which can damage the product. Finally, damage can result if the user plugs in the wrong adapter into the charging jack. The challenge of the product designer is to improve the robustness of the design and avoid situations where the product can be damaged due to un-expected, but unfortunately, likely events that will occur as the product is used.

## Circuit Overview

To address these problems, the protection system above has been developed consisting of the NCP345 Over Voltage Protection IC and a P-channel MOSFET switch such as the MGSF3441. The NCP345 monitors the input voltage and will not turn on the MOSFET unless the input voltage is within a safe operating window that has an upper limit of 7.05 V. A zener diode can be placed in parallel to the load to provide for secondary protection during the brief time that it takes for the NCP345 to detect the over-voltage fault and disconnect the MOSFET. The decision to use this secondary diode is a function of the charging currents expected, load capacitance across the battery, and the desired protection
voltage by analyzing the $\mathrm{dV} / \mathrm{dT}$ rise that occurs during the brief time it takes to turn-off the MOSFET. For battery powered applications, a low-forward voltage Schottky diode such as the MBRM120LT3 can be placed in series with the MOSFET to block the body diode of the MOSFET and prevent shorting the battery out if the input is accidentally shorted to ground. This provides additional voltage margin at the load since there is a small forward drop across this diode that reduces the voltage at the load.

When the protection circuit turns off the MOSFET, there can be a sudden rise in the input voltage of the device. This transient can be quite large depending on the impedance of the supply and the current being drawn from the supply at the time of an over-voltage event. This inductive spike can be clamped with a zener diode from IN to ground. This diode breakdown voltage should be well above the worst case supply voltage provided from the AC/DC adapter or Cigarette Lighter Adapter (CLA), since the zener is only intended to clamp the transient. The NCP345 is designed so that the IN and $\mathrm{V}_{\mathrm{CC}}$ pin can safely protect up to 25 V and withstand transients to 30 V . Since these spikes can be very narrow in duration, it is important to use a high bandwidth probe and oscilloscope when prototyping the product to verify the operation of the circuit under all the transient conditions. A similar problem can result due to contact bounce as the DC source is plugged into the product.
For portable products it is normal to have a capacitor to ground in parallel with the battery. If the product has a battery pack that is easily removable during charging, this scenario should be analyzed. Under that situation, the charging current will go into the capacitor and the voltage may rise rapidly depending on the capacitor value, the charging current and the power supply response time.

## Normal Operation

Figure 1 illustrates a typical configuration. The external adapter provides power to the protection system so the circuitry is only active when the adapter is connected. The OVP monitors the voltage from the charger and if the voltage exceeds a nominal voltage of 6.85 V , the OUT signal drives the gate of the MOSFET to within 1.0 V of VCC, thus turning off the FET and disconnecting the source from the load. The nominal time it takes to drive the gate to this state is 400 nsec ( 1.0 usec maximum for gate capacitance of $<12 \mathrm{nF}$ ). Typical turn off performance using the CNTRL input can be seen in Figure 6. The CNTRL input can also be used to interrupt charging and allow the microcontroller to measure the cell voltage under a normal condition to get a more accurate measure of the battery voltage. Once the over voltage is removed, the NCP345 will turn on the MOSFET. The turn on circuitry is designed to turn on the MOSFET more gradually to limit the in-rush current. Typical turn-on
performance is illustrated using the MGSF3441 in Figure 7. This characteristic is a function of the threshold of the MOSFET and will vary depending on the device characteristics such as the gate capacitance.

The OVP has an under voltage lockout (UVLO) circuit which disables the gate driver circuit until the UVLO senses that the VCC voltage is above 2.6 V . Once the UVLO has released the gate driver circuit, the OUT signal will stay high until the voltage on the IN is sensed. If the input voltage to IN is less than 6.85 V nominal, then the OUT signal will be driven LOW and the FET will be turned on so the source can be connected to the load.

There are three events that will cause the OVP to drive the gate of the FET to a HIGH state.

- Voltage on VCC falls below the UVLO threshold
- Voltage on IN rises above 6.85 V (nominal)
- CNTRL input is driven to a logic High


# INFORMATION FOR USING THE THIN SOT23-5 SURFACE MOUNT PACKAGE MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS 

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


THIN SOT23-5

## THIN SOT23-5 POWER DISSIPATION

The power dissipation of the Thin SOT23-5 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $\mathrm{T}_{\mathrm{J}(\max )}$, the maximum rated junction temperature of the die, $\mathrm{R}_{\theta \mathrm{JA}}$, the thermal resistance from the device junction to ambient, and the operating temperature, $\mathrm{T}_{\mathrm{A}}$. Using the values provided on the data sheet for the Thin SOT23-5 package, $\mathrm{P}_{\mathrm{D}}$ can be calculated as follows:

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $\mathrm{T}_{\mathrm{A}}$ of $25^{\circ} \mathrm{C}$, one can calculate the power dissipation of the device which in this case is 400 milliwatts.

$$
P_{D}=\frac{150^{\circ} \mathrm{C}-25^{\circ} \mathrm{C}}{300^{\circ} \mathrm{C} / \mathrm{W}}=417 \text { milliwatts }
$$

The $300^{\circ} \mathrm{C} / \mathrm{W}$ for the Thin SOT23-5 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 417 milliwatts.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be $100^{\circ} \mathrm{C}$ or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of $10^{\circ} \mathrm{C}$.
- The soldering temperature and time shall not exceed $260^{\circ} \mathrm{C}$ for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be $5^{\circ} \mathrm{C}$ or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.
*Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.


## CS51411, CS51412, CS51413, CS51414

### 1.5 A, 260 kHz and 520 kHz, Low Voltage Buck Regulators with External Bias or Synchronization Capability

The CS5141X products are 1.5 A buck regulator ICs. These devices are fixed-frequency operating at 260 kHz and 520 kHz . The regulators use the $V^{2 \mathrm{TM}}$ control architecture to provide unmatched transient response, the best overall regulation and the simplest loop compensation for today's high-speed logic. These products accommodate input voltages from 4.5 V to 40 V .

The CS51411 and CS51413 contain synchronization circuitry. The CS51412 and CS51414 have the option of powering the controller from an external 3.3 V to 6.0 V supply in order to improve efficiency, especially in high input voltage, light load conditions.

The on-chip NPN transistor is capable of providing a minimum of 1.5 A of output current, and is biased by an external "boost" capacitor to ensure saturation, thus minimizing on-chip power dissipation. Protection circuitry includes thermal shutdown, cycle-by-cycle current limiting and frequency foldback. The CS51411 and CS51413 are functionally pin-compatible with the LT1375. The CS51412 and CS51414 are functionally pin-compatible with the LT1376.

## Features

- $\mathrm{V}^{2}$ Architecture Provides Ultra-Fast Transient Response, Improved Regulation and Simplified Design
- $2.0 \%$ Error Amp Reference Voltage Tolerance
- Switch Frequency Decrease of 4:1 in Short Circuit Conditions Reduces Short Circuit Power Dissipation
- BOOST Lead Allows "Bootstrapped" Operation to Maximize Efficiency
- Sync Function for Parallel Supply Operation or Noise Minimization
- Shutdown Lead Provides Power-Down Option
- $85 \mu \mathrm{~A}$ Quiescent Current During Power-Down
- Thermal Shutdown
- Soft Start
- Pin-Compatible with LT1375 and LT1376


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http://onsemi.com



| X... | $=$ Specific Device Code |
| :--- | :--- |
| A | $=$ Assembly Location |
| WL, L | $=$ Wafer Lot |
| YY, Y | $=$ Year |
| WW, W | $=$ Work Week |

## PIN CONNECTIONS



ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1277 of this data sheet.

## PRODUCT SELECTION GUIDE

| Part Number | Frequency | Temperature Range | Bias/Sync |
| :---: | :---: | :---: | :---: |
| CS51411E | 260 kHz | $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | Sync |
| CS51411G | 260 kHz | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | Sync |
| CS51412E | 260 kHz | $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | Bias |
| CS51412G | 260 kHz | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | Bias |
| CS51413E | 520 kHz | $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | Sync |
| CS51413G | 520 kHz | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | Sync |
| CS51414E | 520 kHz | $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ | Bias |
| CS51414G | 520 kHz | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ | Bias |



Figure 1. Application Diagram, 4.5 V-16 V to 3.3 V @ 1.0 A Converter

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :--- | :---: | :---: |
| Operating Junction Temperature Range, $\mathrm{T}_{J}$ |  | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Damage Threshold (Human Body Model) |  | 2.0 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## CS51411, CS51412, CS51413, CS51414

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | $\mathbf{V}_{\text {Max }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IN }}$ | 40 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | 4.0 A |
| BOOST | 40 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | 100 mA |
| $\mathrm{~V}_{\text {SW }}$ | 40 V | $-0.6 \mathrm{~V} /-1.0 \mathrm{~V}, \mathrm{t}<50 \mathrm{~ns}$ | 4.0 A | 10 mA |
| $\mathrm{~V}_{\mathrm{C}}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| SHDNB | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| SYNC | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| BIAS | 7.0 V | -0.3 V | 1.0 mA | 50 mA |
| $\mathrm{~V}_{\text {FB }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| GND | 7.0 V | -0.3 V | 50 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}\right.$ (CS51411E/2E/3E/4E); $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}(\mathrm{CS51411E/2E/3E/4E)} \mathrm{;}$ $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ (CS51411G/2G/3G/4G), $4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{IN}}<40 \mathrm{~V}$; unless otherwise specified.)

| $\|c\| c\|c\| c\|c\| c\|c\|$ |
| :--- |
| Characteristic |
| Oscillator |
| \begin{tabular}{\|l|c|c|c|c|c|}
\hline
\end{tabular} |
| Operating Frequency |

## PWM Comparator

| Slope Compensation Voltage | CS51411/CS51412, Fix $\mathrm{V}_{\mathrm{FB}}, \Delta \mathrm{V}_{\mathrm{C}} / \Delta \mathrm{T}_{\mathrm{ON}}$ | 8.0 | 17 | 26 | $\mathrm{mV} / \mu \mathrm{s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | CS51413/CS51414 | 25 | 50 | 75 | $\mathrm{mV} / \mu \mathrm{s}$ |
| Minimum Output Pulse Width | CS51411/CS51412, $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\mathrm{SW}}$ | - | 150 | 300 | ns |
|  | CS51413/CS51414, $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\mathrm{SW}}$ | - | - | 230 | ns |

## Power Switch

| Current Limit | $\mathrm{V}_{\mathrm{FB}}>0.36 \mathrm{~V}$ | 1.6 | 2.3 | 3.0 | A |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Foldback Current | $\mathrm{V}_{\mathrm{FB}}<0.29 \mathrm{~V}$ | 0.9 | 1.5 | 2.1 | A |
| Saturation Voltage | $\mathrm{I}_{\mathrm{OUT}}=1.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{BOOST}}=\mathrm{V}_{\mathrm{IN}}+2.5 \mathrm{~V}$ | 0.4 | 0.7 | 1.0 | V |
| Current Limit Delay | Note 2 | - | 120 | 160 | ns |

## Error Amplifier

| Internal Reference Voltage | - | 1.244 | 1.270 | 1.296 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Reference PSRR | Note 2 | - | 40 | - | dB |
| FB Input Bias Current |  | - | 0.02 | 0.1 | $\mu \mathrm{~A}$ |
| Output Source Current | $\mathrm{V}_{\mathrm{C}}=1.270 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.0 \mathrm{~V}$ | 15 | 25 | 35 | $\mu \mathrm{~A}$ |
| Output Sink Current | $\mathrm{V}_{\mathrm{C}}=1.270 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.0 \mathrm{~V}$ | 15 | 25 | 35 | $\mu \mathrm{~A}$ |
| Output High Voltage | $\mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V}$ | 1.39 | 1.46 | 1.53 | V |
| Output Low Voltage | $\mathrm{V}_{\mathrm{FB}}=2.0 \mathrm{~V}$ | 5.0 | 20 | 60 | mV |
| Unity Gain Bandwidth | Note 2 | - | 500 | - | kHz |
| Open Loop Amplifier Gain | Note 2 | - | 70 | - | dB |
| Amplifier Transconductance | Note 2 | - | 6.4 | - | $\mathrm{mA} / \mathrm{V}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}\right.$ (CS51411E/2E/3E/4E); $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}(\mathrm{CS51411E/2E/3E/4E)} \mathrm{;}$ $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ (CS51411G/2G/3G/4G), $4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{IN}}<40 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Sync |  |  |  |  |  |
| Sync Frequency Range | CS51411/CS51412 | 305 | - | 470 | kHz |
| Sync Frequency Range | CS51413/CS51414 | 575 | - | 880 | kHz |
| Sync Pin Bias Current | $\begin{aligned} & \mathrm{V}_{\mathrm{SYNC}}=0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{SYNC}}=5.0 \mathrm{~V} \end{aligned}$ | $250$ | $\begin{aligned} & 0.1 \\ & 360 \end{aligned}$ | $\begin{aligned} & 0.2 \\ & 460 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Sync Threshold Voltage | - | 1.0 | 1.5 | 1.9 | V |

## Shutdown

| Shutdown Threshold Voltage |  | 1.0 | 1.3 | 1.6 | V |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Shutdown Pin Bias Current | $\mathrm{V}_{\text {SHDNB }}=0 \mathrm{~V}$ | 0.14 | 5.00 | 35 | $\mu \mathrm{~A}$ |

## Thermal Shutdown

| Overtemperature Trip Point | Note 3 | 175 | 185 | 195 | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Thermal Shutdown Hysteresis | Note 3 | - | 42 | - | ${ }^{\circ} \mathrm{C}$ |

General

| Quiescent Current | $\mathrm{I}_{\mathrm{SW}}=0 \mathrm{~A}$ | 3.0 | 4.0 | 6.25 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Shutdown Quiescent Current | $\mathrm{V}_{\text {SHDNB }}=0 \mathrm{~V}$ | 8.0 | 20 | 85 | $\mu \mathrm{~A}$ |
| Boost Operating Current | $\mathrm{V}_{\text {BOOST }}-\mathrm{V}_{\mathrm{SW}}=2.5 \mathrm{~V}$ | 6.0 | 15 | 40 | $\mathrm{~mA} / \mathrm{A}$ |
| Minimum Boost Voltage | Note 3 | - | - | 2.5 | V |
| Start up Voltage |  | 2.2 | 3.3 | 4.4 | V |
| Minimum Output Current | - | - | 7.0 | 12 | mA |

3. Guaranteed by design, not $100 \%$ tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| SO-8 |  | PIN SYMBOL |

PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| SO-8 | PIN SYMBOL | FUNCTION |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control

The CS5141X family of buck regulators provides leading edge technology, a high level of integration and high operating frequencies allowing the layout of a switch-mode power supply in a very small board area. These devices are based on the proprietary $\mathrm{V}^{2}$ control architecture. $\mathrm{V}^{2}$ control uses the output voltage and its ripple as the ramp signal, providing an ease of use not generally associated with voltage or current mode control. Improved line regulation, load regulation and very fast transient response are also major advantages.


Figure 3. Buck Converter with $\mathrm{V}^{2}$ Control.
As shown in Figure 3, there are two voltage feedback paths in $\mathrm{V}^{2}$ control, namely FFB (Fast Feedback) and SFB(Slow Feedback). In FFB path, the feedback voltage connects directly to the PWM comparator. This feedback path carries the ramp signal as well as the output DC voltage. Artificial ramp derived from oscillator is added to the feedback signal to improve stability. The other feedback path SFB connects the feedback voltage to the error amplifier whose output $\mathrm{V}_{\mathrm{C}}$ feeds to the other input of the PWM comparator. In a constant frequency mode, the oscillator signal sets the output latch and turns on the switch S1. This starts a new switch cycle. The ramp signal, composed of both artificial ramp and output ripple, eventually comes across the $\mathrm{V}_{\mathrm{C}}$ voltage, and consequently resets the latch to turn off the switch. The switch S 1 will turn on again at the beginning of the next switch cycle. In a buck converter, the output ripple is determined by the ripple
current of the inductor L1 and the ESR (equivalent series resistor) of the output capacitor C 1.
The slope compensation signal is a fixed voltage ramp provided by the oscillator. Adding this signal eliminates subharmonic oscillation associated with the operation at duty cycle greater than $50 \%$. The artificial ramp also ensures the proper PWM function when the output ripple voltage is inadequate. The slope compensation signal is properly sized to serve it purposes without sacrificing the transient response speed.
Under load and line transient, not only the ramp signal changes, but more significantly the DC component of the feedback voltage varies proportionally to the output voltage. FFB path connects both signals directly to the PWM comparator. This allows instant modulation of the duty cycle to counteract any output voltage deviations. The transient response time is independent of the error amplifier bandwidth. This eliminates the delay associated with error amplifier and greatly improves the transient response time. The error amplifier is used here to ensure excellent DC accuracy.

## Error Amplifier

The CS5141X has a transconductance error amplifier, whose non-inverting input is connected to an Internal Reference Voltage generated from the on-chip regulator. The inverting input connects to the $\mathrm{V}_{\mathrm{FB}}$ pin. The output of the error amplifier is made available at the $\mathrm{V}_{\mathrm{C}}$ pin. A typical frequency compensation requires only a $0.1 \mu \mathrm{~F}$ capacitor connected between the $\mathrm{V}_{\mathrm{C}}$ pin and ground, as shown in Figure 1. This capacitor and error amplifier's output resistance (approximately $8.0 \mathrm{M} \Omega$ ) create a low frequency pole to limit the bandwidth. Since $V^{2}$ control does not require a high bandwidth error amplifier, the frequency compensation is greatly simplified.
The $\mathrm{V}_{\mathrm{C}}$ pin is clamped below Output High Voltage. This allows the regulator to recover quickly from over current or short circuit conditions.

## Oscillator and Sync Feature (CS51411 and CS51413 only)

The on-chip oscillator is trimmed at the factory and requires no external components for frequency control. The high switching frequency allows smaller external components to be used, resulting in a board area and cost savings. The tight frequency tolerance simplifies magnetic components selection. The switching frequency is reduced to $25 \%$ of the nominal value when the $\mathrm{V}_{\mathrm{FB}}$ pin voltage is below Frequency Foldback Threshold. In short circuit or over-load conditions, this reduces the power dissipation of the IC and external components.
An external clock signal can sync CS51411/CS51414 to a higher frequency. The rising edge of the sync pulse turns on the power switch to start a new switching cycle, as shown in Figure 4. There is approximately $0.5 \mu$ s delay between the
rising edge of the sync pulse and rising edge of the $\mathrm{V}_{\mathrm{SW}}$ pin voltage. The sync threshold is TTL logic compatible, and duty cycle of the sync pulses can vary from $10 \%$ to $90 \%$. The frequency foldback feature is disabled during the sync mode.


Figure 4. A CS51411 Buck Regulator is Synced by an External 350 kHz Pulse Signal

## Power Switch and Current Limit

The collector of the built-in NPN power switch is connected to the $\mathrm{V}_{\text {IN }}$ pin, and the emitter to the $\mathrm{V}_{\text {SW }}$ pin. When the switch turns on, the $\mathrm{V}_{\mathrm{SW}}$ voltage is equal to the $\mathrm{V}_{\mathrm{IN}}$ minus switch Saturation Voltage. In the buck regulator, the $\mathrm{V}_{\mathrm{SW}}$ voltage swings to one diode drop below ground when the power switch turns off, and the inductor current is commutated to the catch diode. Due to the presence of high pulsed current, the traces connecting the $\mathrm{V}_{\text {SW }}$ pin, inductor and diode should be kept as short as possible to minimize the noise and radiation. For the same reason, the input capacitor should be placed close to the $\mathrm{V}_{\text {IN }}$ pin and the anode of the diode.

The saturation voltage of the power switch is dependent on the switching current, as shown in Figure 5.


Figure 5. The Saturation Voltage of the Power Switch Increases with the Conducting Current

Members of the CS5141X family contain pulse-by-pulse current limiting to protect the power switch and external components. When the peak of the switching current reaches the Current Limit, the power switch turns off after the Current Limit Delay. The switch will not turn on until the next switching cycle. The current limit threshold is independent of switching duty cycle. The maximum load current, given by the following formula under continuous conduction mode, is less than the Current Limit due to the ripple current.

$$
\mathrm{IO}(\mathrm{MAX})=\mathrm{I}_{\mathrm{LI}} \mathrm{M}-\frac{\mathrm{V}_{\mathrm{O}}\left(\mathrm{~V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{O}}\right)}{2(\mathrm{~L})\left(\mathrm{V}_{\mathrm{IN}}\right)\left(\mathrm{f}_{\mathrm{S}}\right)}
$$

where:
$\mathrm{f}_{\mathrm{S}}=$ switching frequency,
$\mathrm{I}_{\mathrm{LIM}}=$ current limit threshold,
$\mathrm{V}_{\mathrm{O}}=$ output voltage,
$\mathrm{V}_{\mathrm{IN}}=$ input voltage,
$\mathrm{L}=$ inductor value.
When the regulator runs under current limit, the subharmonic oscillation may cause low frequency oscillation, as shown in Figure 6. Similar to current mode control, this oscillation occurs at the duty cycle greater than $50 \%$ and can be alleviated by using a larger inductor value. The current limit threshold is reduced to Foldback Current when the FB pin falls below Foldback Threshold. This feature protects the IC and external components under the power up or over-load conditions.


Figure 6. The Regulator in Current Limit

## BOOST Pin

The BOOST pin provides base driving current for the power switch. A voltage higher than $\mathrm{V}_{\text {IN }}$ provides required headroom to turn on the power switch. This in turn reduces IC power dissipation and improves overall system efficiency. The BOOST pin can be connected to an external boost-strapping circuit which typically uses a $0.1 \mu \mathrm{~F}$ capacitor and a 1N914 or 1N4148 diode, as shown in Figure 1. When the power switch is turned on, the voltage on the BOOST pin is equal to

$$
\mathrm{V}_{\mathrm{BOOST}}=\mathrm{V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{O}}-\mathrm{V}_{\mathrm{F}}
$$

where:
$\mathrm{V}_{\mathrm{F}}=$ diode forward voltage.
The anode of the diode can be connected to any DC voltage other than the regulated output voltage. However, the maximum voltage on the BOOST pin shall not exceed 40 V .

As shown in Figure 7, the BOOST pin current includes a constant 7.0 mA pre-driver current and base current proportional to switch conducting current. A detailed discussion of this current is conducted in Thermal Consideration section. A $0.1 \mu \mathrm{~F}$ capacitor is usually adequate for maintaining the Boost pin voltage during the on time.


Figure 7. The Boost Pin Current Includes 7.0 mA Pre-Driver Current and Base Current when the Switch is Turned On. The Beta Decline of the Power Switch Further Increases the Base Current at High Switching Current

BIAS Pin (CS51412 and CS51414 Only)
The BIAS pin allows a secondary power supply to bias the control circuitry of the IC. The BIAS pin voltage should be between 3.3 V and 6.0 V . If the BIAS pin voltage falls below that range, use a diode to prevent current drain from the BIAS pin. Powering the IC with a voltage lower than the regulator's input voltage reduces the IC power dissipation and improves energy transfer efficiency.

## Shutdown

The internal power switch will not turn on until the $\mathrm{V}_{\mathrm{IN}}$ pin rises above the Start Up Voltage. This ensures no switching until adequate supply voltage is provided to the IC.

The IC enters a sleep mode when the SHDNB pin is pulled below Shutdown Threshold Voltage. In the sleep mode, the power switch keeps open and the supply current reduces to Shutdown Quiescent Current. This pin has internal pull-up current. So when this pin is not used, leave the SHDNB pin open.

## Start-Up

During power up, the regulator tends to quickly charge up the output capacitors to reach voltage regulation. This gives
rise to an excessive in-rush current which can be detrimental to the inductor, IC and catch diode. In $\mathrm{V}^{2}$ control, the compensation capacitor provides Soft Start with no need for extra pin or circuitry. During the power up, the Output Source Current of the error amplifier charges the compensation capacitor which forces $\mathrm{V}_{\mathrm{C}}$ pin and thus output voltage ramp up gradually. The Soft Start duration can be calculated by

$$
\mathrm{TSS}=\frac{\mathrm{V}_{\mathrm{C}} \times \mathrm{C}_{\mathrm{COMP}}}{\mathrm{I}_{\text {SOURCE }}}
$$

where:
$\mathrm{V}_{\mathrm{C}}=\mathrm{V}_{\mathrm{C}}$ pin steady-state voltage, which is approximately equal to error amplifier's reference voltage.
$\mathrm{C}_{\mathrm{COMP}}=$ Compensation capacitor connected to the $\mathrm{V}_{\mathrm{C}}$ pin $I_{\text {SOURCE }}=$ Output Source Current of the error amplifier.
Using a $0.1 \mu \mathrm{~F} \mathrm{C}_{\mathrm{COMP}}$, the calculation shows a $\mathrm{T}_{\mathrm{SS}}$ over 5.0 ms which is adequate to avoid any current stresses. Figure 8 shows the gradual rise of the $\mathrm{V}_{\mathrm{C}}, \mathrm{V}_{\mathrm{O}}$ and envelope of the $\mathrm{V}_{\mathrm{SW}}$ during power up. There is no voltage over-shoot after the output voltage reaches the regulation. If the supply voltage rises slower than the $\mathrm{V}_{\mathrm{C}}$ pin, output voltage may over-shoot.


Figure 8. The Power Up Transition of CS5141X Regulator

## Short Circuit

When the $\mathrm{V}_{\mathrm{FB}}$ pin voltage drops below Foldback Threshold, the regulator reduces the peak current limit by $40 \%$ and switching frequency to $1 / 4$ of the nominal frequency. These features are designed to protect the IC and external components during over load or short circuit conditions. In those conditions, peak switching current is clamped to the current limit threshold. The reduced switching frequency significantly increases the ripple current, and thus lowers the DC current. The short circuit can cause the minimum duty cycle to be limited by Minimum Output Pulse Width. The foldback frequency reduces the minimum duty cycle by extending the switching cycle. This protects the IC from overheating, and also limits the power that can be transferred to the output. The current limit
foldback effectively reduces the current stress on the inductor and diode. When the output is shorted, the DC current of the inductor and diode can approach the current limit threshold. Therefore, reducing the current limit by $40 \%$ can result in an equal percentage drop of the inductor and diode current. The short circuit waveforms are captured in Figure 9, and the benefit of the foldback frequency and current limit is self-evident.


Figure 9. In Short Circuit, the Foldback Current and Foldback Frequency Limit the Switching Current to Protect the IC, Inductor and Catch Diode

## Thermal Considerations

A calculation of the power dissipation of the IC is always necessary prior to the adoption of the regulator. The current drawn by the IC includes quiescent current, pre-driver current, and power switch base current. The quiescent current drives the low power circuits in the IC, which include comparators, error amplifier and other logic blocks. Therefore, this current is independent of the switching current and generates power equal to

$$
W_{Q}=V_{I N} \times I_{Q}
$$

where:
$\mathrm{I}_{\mathrm{Q}}=$ quiescent current.
The pre-driver current is used to turn on/off the power switch and is approximately equal to 12 mA in worst case. During steady state operation, the IC draws this current from the Boost pin when the power switch is on and then receives it from the $\mathrm{V}_{\text {IN }}$ pin when the switch is off. The pre-driver current always returns to the $\mathrm{V}_{\mathrm{SW}}$ pin. Since the pre-driver current goes out to the regulator's output even when the power switch is turned off, a minimum load is required to prevent overvoltage in light load conditions. If the Boost pin voltage is equal to $\mathrm{V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{O}}$ when the switch is on, the power dissipation due to pre-driver current can be calculated by

$$
\mathrm{W}_{\mathrm{DRV}}=12 \mathrm{~mA} \times\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{O}}+\frac{\mathrm{V}_{\mathrm{O}}^{2}}{\mathrm{~V}_{\mathrm{IN}}}\right)
$$

The base current of a bipolar transistor is equal to collector current divided by beta of the device. Beta of 60 is used here
to estimate the base current. The Boost pin provides the base current when the transistor needs to be on. The power dissipated by the IC due to this current is

$$
W_{\mathrm{BASE}}=\frac{\mathrm{V}_{\mathrm{O}^{2}}}{\mathrm{~V}_{\mathrm{IN}}} \times \frac{\mathrm{IS}}{60}
$$

where:
$\mathrm{I}_{\mathrm{S}}=\mathrm{DC}$ switching current.
When the power switch turns on, the saturation voltage and conduction current contribute to the power loss of a non-ideal switch. The power loss can be quantified as

$$
\mathrm{W}_{\mathrm{SAT}}=\frac{\mathrm{v}_{\mathrm{O}}}{\mathrm{v}_{\text {IN }}} \times \mathrm{IS}_{\mathrm{S}} \times \mathrm{v}_{\text {SAT }}
$$

where:
$\mathrm{V}_{\mathrm{SAT}}=$ saturation voltage of the power switch which is shown in Figure 5.
The switching loss occurs when the switch experiences both high current and voltage during each switch transition. This regulator has a 30 ns turn-off time and associated power loss is equal to

$$
W_{S}=\frac{\mathrm{IS} \times \mathrm{V}_{\mathrm{IN}}}{2} \times 20 \mathrm{~ns} \times \mathrm{fS}
$$

The turn-on time is much shorter and thus turn-on loss is not considered here.

The total power dissipated by the IC is sum of all the above

$$
W_{I C}=W_{Q}+W_{D R V}+W_{B A S E}+W_{S A T}+W_{S}
$$

The IC junction temperature can be calculated from the ambient temperature, IC power dissipation and thermal resistance of the package. The equation is shown as follows,

$$
T_{J}=W_{I C} \times R_{\theta J A}+T_{A}
$$

The maximum IC junction temperature shall not exceed $125^{\circ} \mathrm{C}$ to guarantee proper operation and avoid any damages to the IC.

## Minimum Load Requirement

As pointed out in the previous section, a minimum load is required for this regulator due to the pre-driver current feeding the output. Placing a resistor equal to $\mathrm{V}_{\mathrm{O}}$ divided by 12 mA should prevent any voltage overshoot at light load conditions. Alternatively, the feedback resistors can be valued properly to consume 12 mA current.

## COMPONENT SELECTION

## Input Capacitor

In a buck converter, the input capacitor witnesses pulsed current with an amplitude equal to the load current. This pulsed current and the ESR of the input capacitors determine the $\mathrm{V}_{\text {IN }}$ ripple voltage, which is shown in Figure 10. For $\mathrm{V}_{\mathrm{IN}}$ ripple, low ESR is a critical requirement for the input capacitor selection. The pulsed input current possesses a significant AC component, which is absorbed by the input
capacitors. The RMS current of the input capacitor can be calculated using:

$$
I_{R M S}=I_{O} \sqrt{D(1-D)}
$$

where:
$\mathrm{D}=$ switching duty cycle which is equal to $\mathrm{V}_{\mathrm{O}} / \mathrm{V}_{\mathrm{IN}}$.
$\mathrm{I}_{\mathrm{O}}=$ load current.


Figure 10. Input Voltage Ripple in a Buck Converter
To calculate the RMS current, multiply the load current with the constant given by Figure 11 at each duty cycle. It is a common practice to select the input capacitor with an RMS current rating more than half the maximum load current. If multiple capacitors are paralleled, the RMS current for each capacitor should be the total current divided by the number of capacitors.


Figure 11. Input Capacitor RMS Current can be Calculated by Multiplying Y Value with Maximum Load Current at any Duty Cycle
Selecting the capacitor type is determined by each design's constraint and emphasis. The aluminum electrolytic capacitors are widely available at lowest cost. Their ESR and ESL (equivalent series inductor) are relatively high. Multiple capacitors are usually paralleled to achieve lower ESR. In addition, electrolytic capacitors usually need to be paralleled with a ceramic capacitor for filtering high frequency noises. The OS-CON are solid aluminum electrolytic capacitors, and therefore has a much lower ESR. Recently, the price of the OS-CON capacitors has dropped significantly so that it is now feasible to use them for some low cost designs. Electrolytic capacitors are physically large, and not used in applications where the size, and especially height is the major concern.

Ceramic capacitors are now available in values over $10 \mu \mathrm{~F}$. Since the ceramic capacitor has low ESR and ESL, a single ceramic capacitor can be adequate for both low frequency and high frequency noises. The disadvantage of ceramic capacitors are their high cost. Solid tantalum capacitors can have low ESR and small size. However, the reliability of the tantalum capacitor is always a concern in the application where the capacitor may experience surge current.

## Output Capacitor

In a buck converter, the requirements on the output capacitor are not as critical as those on the input capacitor. The current to the output capacitor comes from the inductor and thus is triangular. In most applications, this makes the RMS ripple current not an issue in selecting output capacitors.

The output ripple voltage is the sum of a triangular wave caused by ripple current flowing through ESR, and a square wave due to ESL. Capacitive reactance is assumed to be
small compared to ESR and ESL. The peak to peak ripple current of the inductor is:

$$
\mathrm{IP}-\mathrm{P}=\frac{\mathrm{V}_{\mathrm{O}}\left(\mathrm{~V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{O}}\right)}{\left(\mathrm{V}_{\mathrm{IN}}\right)(\mathrm{L})\left(\mathrm{fS}_{\mathrm{S}}\right)}
$$

$\mathrm{V}_{\text {RIPPLE(ESR) }}$, the output ripple due to the ESR, is equal to the product of $\mathrm{I}_{\mathrm{P}-\mathrm{P}}$ and ESR. The voltage developed across the ESL is proportional to the di/dt of the output capacitor. It is realized that the $\mathrm{di} / \mathrm{dt}$ of the output capacitor is the same as the di/dt of the inductor current. Therefore, when the switch turns on, the di/dt is equal to $\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{O}}\right) / \mathrm{L}$, and it becomes $\mathrm{V}_{\mathrm{O}} / \mathrm{L}$ when the switch turns off. The total ripple voltage induced by ESL can then be derived from

$$
\mathrm{V}_{\mathrm{RIPPLE}(E S L)}=\operatorname{ESL}\left(\frac{\mathrm{V}_{\mathrm{IN}}}{\mathrm{~L}}\right)+\operatorname{ESL}\left(\frac{\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{O}}}{\mathrm{~L}}\right)=\operatorname{ESL}\left(\frac{\mathrm{V}_{\text {IN }}}{\mathrm{L}}\right)
$$

The total output ripple is the sum of the $V_{\text {RIPPLE(ESR) }}$ and $V_{\text {RIPPLE(ESR) }}$.


Figure 12. The Output Voltage Ripple Using Two $10 \mu \mathrm{~F}$ Ceramic Capacitors in Parallel


Figure 13. The Output Voltage Ripple Using One $100 \mu \mathrm{~F}$ POSCAP Capacitor


Figure 14. The Output Voltage Ripple Using One $100 \mu$ F OS-CON


Figure 15. The Output Voltage Ripple Using One $100 \mu \mathrm{~F}$ Tantalum Capacitor
Figure 12 to Figure 15 show the output ripple of a 5.0 V to $3.3 \mathrm{~V} / 500 \mathrm{~mA}$ regulator using $22 \mu \mathrm{H}$ inductor and various capacitor types. At the switching frequency, the low ESR and ESL make the ceramic capacitors behave capacitively as shown in Figure 12. Additional paralleled ceramic capacitors will further reduce the ripple voltage, but inevitably increase the cost. "POSCAP", manufactured by SANYO, is a solid electrolytic capacitor. The anode is sintered tantalum and the cathode is a highly conductive polymerized organic semiconductor. TPC series, featuring low ESR and low profile, is used in the measurement of Figure 13. It is shown that POSCAP presents a good balance of capacitance and ESR, compared with a ceramic capacitor. In this application, the low ESR generates less than 5.0 mV of ripple and the ESL is almost unnoticeable. The ESL of the through-hole OS-CON capacitor give rise to the inductive impedance. It is evident from Figure 14 which shows the
step rise of the output ripple on the switch turn-on and large spike on the switch turn-off. The ESL prevents the output capacitor from quickly charging up the parasitic capacitor of the inductor when the switch node is pulled below ground through the catch diode conduction. This results in the spike associated with the falling edge of the switch node. The D package tantalum capacitor used in Figure 15 has the same footprint as the POSCAP, but doubles the height. The ESR of the tantalum capacitor is apparently higher than the POSCAP. The electrolytic and tantalum capacitors provide a low-cost solution with compromised performance. The reliability of the tantalum capacitor is not a serious concern for output filtering because the output capacitor is usually free of surge current and voltage.

## Diode Selection

The diode in the buck converter provides the inductor current path when the power switch turns off. The peak reverse voltage is equal to the maximum input voltage. The peak conducting current is clamped by the current limit of the IC. The average current can be calculated from:

$$
\mathrm{ID}(\mathrm{AVG})=\frac{\mathrm{IO}\left(\mathrm{~V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{O}}\right)}{\mathrm{V}_{\mathrm{IN}}}
$$

The worse case of the diode average current occurs during maximum load current and maximum input voltage. For the diode to survive the short circuit condition, the current rating of the diode should be equal to the Foldback Current Limit. See Table 4 for schottky diodes from ON Semiconductor which are suggested for CS5141X regulator.
height, output ripple, EMI, saturation and cost. Lower inductor values are chosen to reduce the physical size of the inductor. Higher value cuts down the ripple current, core losses and allows more output current. For most applications, the inductor value falls in the range between $2.2 \mu \mathrm{H}$ and $22 \mu \mathrm{H}$. The saturation current ratings of the inductor shall not exceed the $\mathrm{I}_{\mathrm{L}(\mathrm{PK})}$, calculated according to

$$
\mathrm{I}_{\mathrm{L}(\mathrm{PK})}=\mathrm{I}_{\mathrm{O}}=+\frac{\mathrm{V}_{\mathrm{O}}\left(\mathrm{~V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{O}}\right)}{2(\mathrm{fS})(\mathrm{L})\left(\mathrm{V}_{\mathrm{IN}}\right)}
$$

The DC current through the inductor is equal to the load current. The worse case occurs during maximum load current. Check the vendor's spec to adjust the inductor value under current loading. Inductors can lose over $50 \%$ of inductance when it nears saturation.

The core materials have a significant effect on inductor performance. The ferrite core has benefits of small physical size, and very low power dissipation. But be careful not to operate these inductors too far beyond their maximum ratings for peak current, as this will saturate the core. Powered Iron cores are low cost and have a more gradual saturation curve. The cores with an open magnetic path, such as rod or barrel, tend to generate high magnetic field radiation. However, they are usually cheap and small. The cores providing a close magnetic loop, such as pot-core and toroid, generate low electro-magnetic interference (EMI).
There are many magnetic component vendors providing standard product lines suitable for CS5141X. Table 5 lists three vendors, their products and contact information.

## Inductor Selection

When choosing inductors, one might have to consider maximum load current, core and copper losses, component

Table 4.

| Part Number | V ${ }_{\text {BREAKDOWN }}(\mathrm{V})$ | Itaverage (A) | $\mathrm{V}_{(\mathrm{F})}(\mathrm{V}) \mathrm{@l}_{\text {IVERAGE }}$ | Package |
| :---: | :---: | :---: | :---: | :---: |
| 1N5817 | 20 | 1.0 | 0.45 | Axial Lead |
| 1N5818 | 30 | 1.0 | 0.55 | Axial Lead |
| 1N5819 | 40 | 1.0 | 0.6 | Axial Lead |
| MBR0520 | 20 | 0.5 | 0.385 | SOD-123 |
| MBR0530 | 30 | 0.5 | 0.43 | SOD-123 |
| MBR0540 | 40 | 0.5 | 0.53 | SOD-123 |
| MBRS120 | 20 | 1.0 | 0.55 | SMB |
| MBRS130 | 30 | 1.0 | 0.395 | SMB |
| MBRS140 | 40 | 1.0 | 0.6 | SMB |

Table 5.


Figure 16. Additional Application Diagram, 5.0 V-12 V to -5.0 V/400 mA Inverting Converter


Figure 17. Additional Application Diagram, 12 V to 5.0 V/1.0 A Buck Converter using the BIAS Pin

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package | Shipping |
| :--- | :---: | :---: | :---: |
| CS51411ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS51411EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |
| CS51412ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51412EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51413ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS51413EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51414ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51414EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51411GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51411GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51412GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51412GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51413GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51413GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51414GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51414GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 45 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 165 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## LM2574

### 0.5 A, Adjustable Output Voltage, Step-Down Switching Regulator

The LM2574 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 0.5 A load with excellent line and load regulation. These devices are available in fixed output voltages of $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, $12 \mathrm{~V}, 15 \mathrm{~V}$, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2574 are offered by several different inductor manufacturers.

Since the LM2574 converter is a switch-mode power supply, its efficiency is significantly higher in comparison with popular three-terminal linear regulators, especially with higher input voltages. In most cases, the power dissipated by the LM2574 regulator is so low, that the copper traces on the printed circuit board are normally the only heatsink needed and no additional heatsinking is required.

The LM2574 features include a guaranteed $\pm 4 \%$ tolerance on output voltage within specified input voltages and output load conditions, and $\pm 10 \%$ on the oscillator frequency ( $\pm 2 \%$ over $0^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ ). External shutdown is included, featuring $60 \mu \mathrm{~A}$ (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

## Features

- 3.3 V, 5.0 V, $12 \mathrm{~V}, 15 \mathrm{~V}$, and Adjustable Output Versions
- Adjustable Version Output Voltage Range, 1.23 to $37 \mathrm{~V} \pm 4 \%$ max over Line and Load Conditions
- Guaranteed 0.5 A Output Current
- Wide Input Voltage Range: 4.75 to 40 V
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection


## Applications

- Simple and High-Efficiency Step-Down (Buck) Regulators
- Efficient Pre-regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converters (Buck-Boost)
- Negative Step-Up Converters
- Power Supply for Battery Chargers


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


PDIP-8 N SUFFIX CASE 626

## PIN CONNECTIONS



* No internal connection, but should be soldered to PC board for best heat transfer.


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1301 of this data sheet. section on page 1301 of this data sheet.

## LM2574

Typical Application (Fixed Output Voltage Versions)

(4) (6) (5)

Representative Block Diagram and Typical Application


NOTE: Pin numbers in ( ) are for the SO-16W package.
Figure 1. Block Diagram and Typical Application

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur).

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Maximum Supply Voltage | $V_{\text {in }}$ | 45 | V |
| ON/OFF Pin Input Voltage | - | $-0.3 \mathrm{~V} \leq \mathrm{V} \leq+\mathrm{V}_{\text {in }}$ | V |
| Output Voltage to Ground (Steady State) | - | -1.0 | V |
| DW Suffix, Plastic Package Case 751G Max Power Dissipation Thermal Resistance, Junction-to-Air | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{AJA}} \end{gathered}$ | Internally Limited 145 | $\begin{gathered} \text { W } \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| N Suffix, Plastic Package Case 626 Max Power Dissipation Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | $\begin{gathered} \text { Internally Limited } \\ 100 \\ 5.0 \end{gathered}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ | ${ }^{\circ} \mathrm{C}$ |
| Minimum ESD Rating <br> (Human Body Model: C = $100 \mathrm{pF}, \mathrm{R}=1.5 \mathrm{k} \Omega$ ) | - | 2.0 | kV |
| Lead Temperature (Soldering, 10 seconds) | - | 260 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | TJ | 150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics).

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Supply Voltage | $\mathrm{V}_{\text {in }}$ | 40 | V |

SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 16)
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $\mathrm{V}_{\text {in }}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, and Adjustable version, $\mathrm{V}_{\text {in }}=25 \mathrm{~V}$ for the 12 V version, $\mathrm{V}_{\text {in }}=30 \mathrm{~V}$ for the 15 V version. $\mathrm{I}_{\text {Load }}=100 \mathrm{~mA}$. For typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{J}}$ is the operating junction temperature range that applies [Note 2], unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LM2574-3.3 ([Note 1] Test Circuit Figure 16) |  |  |  |  |  |
| Output Voltage ( $\left.\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=100 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right)$ | $V_{\text {out }}$ | 3.234 | 3.3 | 3.366 | V |
| $\begin{aligned} & \text { Output Voltage }\left(4.75 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 0.5 \mathrm{~A}\right) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $V_{\text {out }}$ | $\begin{aligned} & 3.168 \\ & 3.135 \end{aligned}$ | $3.3$ | $\begin{aligned} & 3.432 \\ & 3.465 \end{aligned}$ | V |
| Efficiency ( $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}$ ) | $\eta$ | - | 72 | - | \% |

LM2574-5 ([Note 1] Test Circuit Figure 16)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=100 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 4.9 | 5.0 | 5.1 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(7.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 0.5 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 4.8 | 5.0 | 5.2 |  |
| $\mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 4.75 |  | 5.25 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}\right)$ | $\eta$ | - | 77 | - | $\%$ |

LM2574-12 ([Note 1] Test Circuit Figure 16)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{I}_{\text {Load }}=100 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 11.76 | 10 | 12.24 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(15 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 0.5 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 11.52 | 12 | 12.48 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 11.4 | - | 12.6 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=15 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}\right)$ | $\eta$ | - | 88 | - | $\%$ |

LM2574-15 ([Note 1] Test Circuit Figure 16)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=30 \mathrm{~V}, \mathrm{I}_{\text {Load }}=100 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 14.7 | 15 | 15.3 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(18 \mathrm{~V}<\mathrm{V}_{\text {in }}<40 \mathrm{~V}, 0.1 \mathrm{~A}<\mathrm{I}_{\text {Load }}<0.5 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 14.4 | 15 | 15.6 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 14.25 |  | 15.75 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=18 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}\right)$ | $\eta$ | - | 88 | - | $\%$ |

LM2574 ADJUSTABLE VERSION ([Note 1] Test Circuit Figure 16)

| Feedback Voltage $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=100 \mathrm{~mA}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{FB}}$ | 1.217 | 1.23 | 1.243 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Feedback Voltage $7.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.1 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 0.5 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0$ | $\mathrm{~V}_{\mathrm{FBT}}$ |  |  |  | V |
| V |  |  |  |  |  |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 1.193 | 1.23 | 1.267 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 1.18 |  | 1.28 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}\right)$ | $\eta$ | - | 77 | - | $\%$ |

1. External components such as the catch diode, inductor, input and output capacitors can affect the switching regulator system performance. When the LM2574 is used as shown in the Figure 16 test circuit, the system performance will be as shown in the system parameters section of the Electrical Characteristics.
2. Tested junction temperature range for the LM 2574 : $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$.

SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 16)
ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise specified, $\mathrm{V}_{\text {in }}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, and
Adjustable version, $\mathrm{V}_{\text {in }}=25 \mathrm{~V}$ for the 12 V version, $\mathrm{V}_{\text {in }}=30 \mathrm{~V}$ for the 15 V version. $\mathrm{I}_{\text {Load }}=100 \mathrm{~mA}$. For typical values $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$, for $\mathrm{min} / \mathrm{max}$ values $\mathrm{T}_{\mathrm{J}}$ is the operating junction temperature range that applies [Note 2], unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## ALL OUTPUT VOLTAGE VERSIONS

| $\begin{aligned} & \text { Feedback Bias Current } \mathrm{V}_{\text {out }}=5.0 \mathrm{~V} \text { (Adjustable Version Only) } \\ & \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{l}_{\mathrm{b}}$ |  |  | $\begin{aligned} & 100 \\ & 200 \end{aligned}$ | nA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillator Frequency (Note 3) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=0 \text { to }+125^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{f}_{0}$ | $47$ | $\begin{aligned} & 52 \\ & 52 \end{aligned}$ | $\begin{aligned} & 58 \\ & 63 \end{aligned}$ | kHz |
| $\begin{aligned} & \text { Saturation Voltage ( } \left.\mathrm{l}_{\text {out }}=0.5 \mathrm{~A},[\text { Note } 4]\right) \\ & \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {sat }}$ |  |  | $\begin{aligned} & 1.2 \\ & 1.4 \end{aligned}$ | V |
| Max Duty Cycle ("on") (Note 5) | DC | 93 | 98 | - | \% |
| Current Limit Peak Current (Notes 3 and 4) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\mathrm{CL}}$ | $\begin{gathered} 0.7 \\ 0.65 \end{gathered}$ |  | $\begin{aligned} & 1.6 \\ & 1.8 \end{aligned}$ | A |
| ```Output Leakage Current (Notes 6 and 7), TJ=25}\mp@subsup{}{}{\circ}\textrm{C Output = 0 V Output =-1.0 V``` | IL |  | $\begin{aligned} & 0.6 \\ & 10 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 30 \end{aligned}$ | mA |
| $\begin{aligned} & \text { Quiescent Current (Note 6) } \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | ${ }^{1}$ |  |  | $\begin{gathered} 9.0 \\ 11 \end{gathered}$ | mA |
| $\begin{aligned} & \text { Standby Quiescent Current (ON/OFF Pin = } 5.0 \mathrm{~V} \text { ("off")) } \\ & \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\text {stby }}$ |  |  | $\begin{aligned} & 200 \\ & 400 \end{aligned}$ | $\mu \mathrm{A}$ |
| ON/OFF Pin Logic Input Level $\begin{aligned} \mathrm{V}_{\text {out }} & =0 \mathrm{~V} \\ \mathrm{~T}_{J} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J} & =-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ <br> Nominal Output Voltage $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{IH}}$ $\mathrm{V}_{\mathrm{IL}}$ | $\begin{aligned} & 2.2 \\ & 2.4 \end{aligned}$ | $\begin{gathered} 1.4 \\ - \\ 1.2 \end{gathered}$ | $\begin{aligned} & 1.0 \\ & 0.8 \end{aligned}$ | V |
| ON/OFF $\mathrm{P}_{\text {in }}$ Input Current ON/OFF $\mathrm{P}_{\text {in }}=5.0 \mathrm{~V}$ ("off"), $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ON/OFF $\mathrm{P}_{\text {in }}=0 \mathrm{~V}$ ("on"), $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\begin{aligned} & I_{\mathrm{IH}} \\ & I_{\mathrm{IL}} \end{aligned}$ | - | $\begin{gathered} 15 \\ 0 \end{gathered}$ | $\begin{aligned} & 30 \\ & 5.0 \end{aligned}$ | $\mu \mathrm{A}$ |

1. External components such as the catch diode, inductor, input and output capacitors can affect the switching regulator system performance. When the LM2574 is used as shown in the Figure 16 test circuit, the system performance will be as shown in the system parameters section of the Electrical Characteristics.
2. Tested junction temperature range for the LM 2574 : $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$.
3. The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately $40 \%$ from the nominal output voltage. This self protection feature lowers the average power dissipation of the IC by lowering the minimum duty cycle from $5 \%$ down to approximately $2 \%$.
4. Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to the output pin.
5. Feedback (Pin 4) removed from output and connected to 0 V .
6. Feedback (Pin 4) removed from output and connected to 12 V for the Adjustable, 3.3 V , and 5.0 V versions, and 25 V for the 12 V and 15 V versions, to force the output transistor OFF.
7. $\mathrm{V}_{\mathrm{in}}=40 \mathrm{~V}$.

## LM2574

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 16)


Figure 2. Normalized Output Voltage


Figure 4. Dropout Voltage


Figure 6. Quiescent Current


Figure 3. Line Regulation


Figure 5. Current Limit


Figure 7. Standby Quiescent Current

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 16) (continued)


Figure 8. Oscillator Frequency


Figure 10. Minimum Operating Voltage


Figure 12. Continuous Mode Switching Waveforms $\mathrm{V}_{\text {out }}=5.0 \mathrm{~V}, 500 \mathrm{~mA}$ Load Current, $\mathrm{L}=330 \mu \mathrm{H}$


Figure 9. Switch Saturation Voltage


Figure 11. Feedback Pin Current


Figure 13. Discontinuous Mode Switching Waveforms $\mathrm{V}_{\text {out }}=5.0 \mathrm{~V}, 100 \mathrm{~mA}$ Load Current, $\mathrm{L}=100 \mu \mathrm{H}$

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 16) (continued)

$200 \mu \mathrm{~s} /$ DIV
A: Output Voltage, $50 \mathrm{mV} / \mathrm{DIV}$, AC Coupled
B: 100 mA to 500 mA Load Pulse
Figure 14. 500 mA Load Transient Response for Continuous Mode Operation, $\mathrm{L}=330 \mu \mathrm{H}, \mathrm{C}_{\text {out }}=300 \mu \mathrm{~F}$

$200 \mu \mathrm{~s} / \mathrm{DIV}$
A: Output Voltage, $50 \mathrm{mV} / \mathrm{DIV}, \mathrm{AC}$ Coupled
B: 50 mA to 250 mA Load Pulse
Figure 15. $\mathbf{2 5 0 \mathrm { mA } \text { Load Transient Response for }}$ Discontinuous Mode Operation, $L=68 \mu \mathrm{H}, \mathrm{C}_{\text {out }}=470 \mu \mathrm{~F}$

Fixed Output Voltage Versions


NOTE: Pin numbers in ( ) are for the SO-16W package.
Figure 16. Test Circuit and Layout Guidelines

## PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 16, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible.

For best results, single-point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 7 (emitter of the internal switch) of the LM2574 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2574 regulator.

PIN FUNCTION DESCRIPTION

| Pin |  |  |  |
| :---: | :---: | :---: | :--- |
| SO-16W | PDIP-8 | Symbol |  |
| 12 | 5 | $V_{\text {in }}$ | This pin is the positive input supply for the LM2574 step-down switching regulator. In order to <br> minimize voltage transients and to supply the switching currents needed by the regulator, a <br> suitable input bypass capacitor must be present ( $C_{\text {in }}$ in Figure 1). |
| 14 | 7 | Output | This is the emitter of the internal switch. The saturation voltage $\mathrm{V}_{\text {sat of this output switch is }}^{\text {typically 1.0 V. It should be kept in mind that the PCB area connected to this pin should be kept }}$ <br> to a minimum in order to minimize coupling to sensitive circuitry. |
| 4 | 2 | Sig Gnd | Circuit signal ground pin. See the information about the printed circuit board layout. |

## DESIGN PROCEDURE

## Buck Converter Basics

The LM2574 is a "Buck" or Step-Down Converter which is the most elementary forward-mode converter. Its basic schematic can be seen in Figure 17.

The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$
\mathrm{I}_{\mathrm{L}(\mathrm{on})}=\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \mathrm{t}_{\text {on }}}{\mathrm{L}}
$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.


Figure 17. Basic Buck Converter
The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by the catch diode. Current now flows through the catch diode thus maintaining the load
current loop. This removes the stored energy from the inductor. The inductor current during this time is:

$$
I_{L(\text { off })}=\frac{\left(V_{\text {out }}-V_{D}\right) t_{\text {off }}}{L}
$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

$$
\mathrm{d}=\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{~T}} \text {, where } \mathrm{T} \text { is the period of switching. }
$$

For the buck converter with ideal components, the duty cycle can also be described as:

$$
\mathrm{d}=\frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}}
$$

Figure 18 shows the buck converter idealized waveforms of the catch diode voltage and the inductor current.


Figure 18. Buck Converter Idealized Waveforms

Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

| Procedure | Example |
| :---: | :---: |
| Given Parameters: <br> $\mathrm{V}_{\text {out }}=$ Regulated Output Voltage (3.3 V, 5.0 V, 12 V or 15 V ) <br> $\mathrm{V}_{\text {in(max })}=$ Maximum Input Voltage <br> $I_{\text {Load }(\max )}=$ Maximum Load Current | Given Parameters: $\begin{aligned} & V_{\text {out }}=5.0 \mathrm{~V} \\ & \mathrm{~V}_{\text {in }(\max )}=15 \mathrm{~V} \\ & \mathrm{I}_{\text {Load }(\max )}=0.4 \mathrm{~A} \end{aligned}$ |
| 1. Controller IC Selection <br> According to the required input voltage, output voltage and current, select the appropriate type of the controller IC output voltage version. | 1. Controller IC Selection <br> According to the required input voltage, output voltage, current polarity and current value, use the LM2574-5 controller IC. |
| 2. Input Capacitor Selection ( $\mathrm{C}_{\mathrm{in}}$ ) <br> To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+\mathrm{V}_{\text {in }}$ and ground pin Gnd. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. | 2. Input Capacitor Selection ( $\mathrm{C}_{\text {in }}$ ) <br> A $22 \mu \mathrm{~F}, 25 \mathrm{~V}$ aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing. |
| 3. Catch Diode Selection (D1) <br> A. Since the diode maximum peak current exceeds the regulator maximum load current, the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2574 to be able to withstand a continuous output short. <br> B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. | 3. Catch Diode Selection (D1) <br> A. For this example the current rating of the diode is 1.0 A . <br> B. Use a 20 V 1 N 5817 Schottky diode, or any of the suggested fast recovery diodes shown in Table 1. |
| 4. Inductor Selection (L1) <br> A. According to the required working conditions, select the correct inductor value using the selection guide from Figures 19 to 23. <br> B. From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code. <br> C. Select an appropriate inductor from the several different manufacturers part numbers listed in Table 2. The designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows: $I_{p(\max )}=I_{\text {Load }(\max )}+\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \mathrm{t}_{\text {on }}}{2 \mathrm{~L}}$ <br> where $t_{o n}$ is the "on" time of the power switch and $t_{\text {on }}=\frac{V_{\text {out }}}{V_{\text {in }}} \times \frac{1.0}{f_{\text {osc }}}$ <br> For additional information about the inductor, see the inductor section in the "EXTERNAL COMPONENTS" section of this data sheet. | 4. Inductor Selection (L1) <br> A. Use the inductor selection guide shown in Figure 20. <br> B. From the selection guide, the inductance area intersected by the 15 V line and 0.4 A line is 330 . <br> C. Inductor value required is $330 \mu \mathrm{H}$. From Table 2, choose an inductor from any of the listed manufacturers. |

Procedure (Fixed Output Voltage Version) (continued) In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

| Procedure | Example |
| :---: | :---: |
| 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ ) <br> A. Since the LM2574 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately $1 \%$ of the output voltage) a value between $100 \mu \mathrm{~F}$ and $470 \mu \mathrm{~F}$ is recommended. <br> B. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8.0 V is appropriate, and a 10 V or 16 V rating is recommended. | 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ ) <br> A. $\mathrm{C}_{\text {out }}=100 \mu \mathrm{~F}$ to $470 \mu \mathrm{~F}$ standard aluminium electrolytic. <br> B. Capacitor voltage rating $=20 \mathrm{~V}$. |

## Procedure (Adjustable Output Version: LM2574-ADJ)

| Procedure | Example |
| :---: | :---: |
| Given Parameters: <br> $\mathrm{V}_{\text {out }}=$ Regulated Output Voltage <br> $\mathrm{V}_{\text {in(max) }}=$ Maximum DC Input Voltage <br> $I_{\text {Load(max) }}=$ Maximum Load Current | Given Parameters: $\begin{aligned} & \mathrm{V}_{\text {out }}=24 \mathrm{~V} \\ & \mathrm{~V}_{\text {in }(\max )}=40 \mathrm{~V} \\ & \mathrm{~L}_{\text {Load }(\max )}=0.4 \mathrm{~A} \end{aligned}$ |
| 1. Programming Output Voltage <br> To select the right programming resistor R1 and R2 value (see Figure 2) use the following formula: $V_{\text {out }}=V_{\text {ref }}\left(1.0+\frac{R 2}{R 1}\right) \quad \text { where } V_{\text {ref }}=1.23 \mathrm{~V}$ <br> Resistor R1 can be between $1.0 \mathrm{k} \Omega$ and $5.0 \mathrm{k} \Omega$. (For best temperature coefficient and stability with time, use $1 \%$ metal film resistors). $\mathrm{R} 2=\mathrm{R} 1\left(\frac{\mathrm{~V}_{\text {out }}}{\mathrm{V}_{\text {ref }}}-1.0\right)$ | 1. Programming Output Voltage (selecting R1 and R2) Select R1 and R2 : $\begin{gathered} V_{\text {out }}=1.23\left(1.0+\frac{R 2}{R 1}\right) \text { Select } R 1=1.0 \mathrm{k} \Omega \\ R 2=R 1\left(\frac{V_{\text {out }}}{V_{\text {ref }}}-1.0\right)=1.0 \mathrm{k}\left(\frac{10 \mathrm{~V}}{1.23 \mathrm{~V}}-1.0\right) \\ R 2=18.51 \mathrm{k} \Omega \text {, choose a } 18.7 \mathrm{k} \Omega \text { metal film resistor. } \end{gathered}$ |
| 2. Input Capacitor Selection ( $\mathrm{C}_{\mathrm{in}}$ ) <br> To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+\mathrm{V}_{\text {in }}$ and ground pin Gnd. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. For additional information see input capacitor section in the "EXTERNAL COMPONENTS" section of this data sheet. | 2. Input Capacitor Selection ( $\mathrm{C}_{\mathrm{in}}$ ) <br> A $22 \mu \mathrm{~F}$ aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing. |

3. Catch Diode Selection (D1)
A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2574 to be able to withstand a continuous output short.
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

## 3. Catch Diode Selection (D1)

A. For this example, a 1.0 A current rating is adequate.
B. Use a 50 V MBR150 Schottky diode or any suggested fast recovery diodes in Table 1.

Procedure (Adjustable Output Version: LM2574-ADJ)

| Procedure |
| :--- |
| 4. Inductor Selection (L1) |
| A. Use the following formula to calculate the inductor Volt x |
| microsecond $[\mathrm{V} \times \mu \mathrm{s}]$ constant: |
| $\mathrm{E} \times T=\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}} \times \frac{10^{6}}{\mathrm{~F}[\mathrm{~Hz}]}[\mathrm{V} \times \mu \mathrm{s}]$ |

B. Match the calculated $\mathrm{E} \times \mathrm{T}$ value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 23. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle.
C. Next step is to identify the inductance region intersected by the ExT value and the maximum load current value on the horizontal axis shown in Figure 27.
D. From the inductor code, identify the inductor value. Then select an appropriate inductor from Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of $1.15 \times \mathrm{I}_{\text {Load }}$. The inductor current rating can also be determined by calculating the inductor peak current:

$$
\mathrm{I}_{\mathrm{p}(\max )}=\mathrm{I}_{\mathrm{Load}(\max )}+\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \mathrm{t}_{\mathrm{on}}}{2 \mathrm{~L}}
$$

where $t_{\text {on }}$ is the "on" time of the power switch and

$$
t_{\text {on }}=\frac{V_{\text {out }}}{V_{\text {in }}} \times \frac{1.0}{f_{\text {osc }}}
$$

For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.

## 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ )

A. Since the LM2574 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values.

For stable operation, the capacitor must satisfy the following requirement:

$$
C_{\text {out }} \geq 13,300 \frac{V_{\text {in }}^{\text {(max }}}{}[[\mu F]
$$

B. Capacitor values between $10 \mu \mathrm{~F}$ and $2000 \mu \mathrm{~F}$ will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields.
C. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8.0 V is appropriate, and a 10 V or 16 V rating is recommended.

## 4. Inductor Selection (L1)

A. Calculate $\mathrm{E} \times \mathrm{T}[\mathrm{V} \times \mu \mathrm{s}]$ constant :

$$
E \times T=(40-24) \times \frac{24}{40} \times \frac{1000}{52}=105[V \times \mu s]
$$

B. $\mathrm{E} \times \mathrm{T}=185[\mathrm{~V} \times \mu \mathrm{s}]$
C. $I_{\text {Load }(\max )}=0.4 \mathrm{~A}$

Inductance Region $=1000$
D. Proper inductor value $=1000 \mu \mathrm{H}$ Choose the inductor from Table 2.

## 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ )

A.

$$
C_{\text {out }} \geq 13,300 \times \frac{40}{24 \times 1000}=22.2 \mu \mathrm{~F}
$$

To achieve an acceptable ripple voltage, select $C_{\text {out }}=100 \mu \mathrm{~F}$ electrolytic capacitor.

## LM2574

## LM2574 Series Buck Regulator Design Procedures (continued)

Indicator Value Selection Guide (For Continuous Mode Operation)


Figure 19. LM2574-3.3


Figure 21. LM2574-12


Figure 20. LM2574-5


Figure 22. LM2574-15


Figure 23. LM2574-ADJ

Table 1. Diode Selection Guide gives an overview about through-hole diodes for an effective design. Device listed in bold are available from ON Semiconductor

| $\mathbf{V}_{\mathbf{R}}$ | 1.0 Amp Diodes |  |
| :---: | :---: | :---: |
|  | Schottky | Fast Recovery |
| 20 V | 1N5817 <br> MBR120P |  |
| 30 V | 1N5818 <br> MBR130P | 1N5819 <br> MBR140P |
| 40 V | MUR110 <br> (rated to 100 V) |  |
| 50 V | MBR150 |  |
| 60 V | MBR160 |  |

Table 2. Inductor Selection Guide

| Inductor <br> Value | Pulse Engineering | Tech 39 | Renco | NPI |
| :---: | :---: | :---: | :---: | :---: |
| $68 \mu \mathrm{H}$ | $*$ | 55258 SN | RL-1284-68 | NP5915 |
| $100 \mu \mathrm{H}$ | $*$ | 55308 SN | RL-1284-100 | NP5916 |
| $150 \mu \mathrm{H}$ | 52625 | 55356 SN | RL-1284-150 | NP5917 |
| $220 \mu \mathrm{H}$ | 52626 | 55406 SN | RL-1284-220 | NP5918/5919 |
| $330 \mu \mathrm{H}$ | 52627 | 55454 SN | RL-1284-330 | NP5920/5921 |
| $470 \mu \mathrm{H}$ | 52628 | $*$ | RL-1284-470 | NP5922 |
| $680 \mu \mathrm{H}$ | 52629 | 55504 SN | RL-1284-680 | NP5923 |
| $1000 \mu \mathrm{H}$ | 52631 | 55554 SN | RL-1284-1000 | $*$ |
| $1500 \mu \mathrm{H}$ | $*$ | $*$ | RL-1284-1500 | $*$ |
| $2200 \mu \mathrm{H}$ | $*$ | RL-1284-2200 | $*$ |  |

*: Contact Manufacturer

Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

| Pulse Engineering Inc. | Phone <br> Fax | $+1-619-674-8100$ <br> $+1-619-674-8262$ |
| :--- | :--- | :--- |
| Pulse Engineering Inc. Europe | Phone <br> Fax | $+353-9324-107$ <br> $+353-9324-459$ |
| Renco Electronics Inc. | Phone <br> Fax | $+1-516-645-5828$ <br> $+1-516-586-5562$ |
| Tech 39 | Phone <br> Fax | $+33-1-4115-1681$ <br> $+33-1-4709-5051$ |
| NPI/APC | Phone <br> Fax | $+44-634-290-588$ |

## EXTERNAL COMPONENTS

## Input Capacitor ( $\mathrm{C}_{\text {in }}$ ) The Input Capacitor Should Have a Low ESR

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin, to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below $-25^{\circ} \mathrm{C}$ larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

## RMS Current Rating of $C_{\text {in }}$

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequences of operating an electrolytic capacitor beyond the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$
\mathrm{I}_{\mathrm{rms}}>1.2 \times \mathrm{dx} \mathrm{I}_{\text {Load }}
$$

where $d$ is the duty cycle, for a continuous mode buck regulator

$$
\mathrm{d}=\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{~T}}=\frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}}
$$

and $d=\frac{t_{\text {on }}}{T}=\frac{\left|V_{\text {out }}\right|}{\left|V_{\text {out }}\right|+V_{\text {in }}}$ for a buck-boost regulator.

## Output Capacitor ( $\mathrm{C}_{\text {out }}$ )

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak-to-peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value. Standard aluminium electrolytics could be adequate for some applications but for quality design, low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors, such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher
voltage ratings may be needed to provide low ESR values, that are required for low output ripple voltage.

## The Output Capacitor Requires an ESR Value that has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low (below $0.03 \Omega$ ), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

## At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 times at $-25^{\circ} \mathrm{C}$ and as much as 10 times at $-40^{\circ} \mathrm{C}$. Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$. They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about $10 \%$ or $20 \%$ of the total capacitance. The output capacitor should have at least $50 \%$ higher RMS ripple current rating at 52 kHz than the peak-to-peak inductor ripple current.

## Catch Diode <br> Locate the Catch Diode Close to the LM2574

The LM2574 is a step-down buck converter, it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2574 using short leads and short printed circuit traces to avoid EMI problems.

## Use a Schottky or a Soft Switching Ultra-Fast Recovery Diode

Since the rectifier diodes are very significant source of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications ( 5.0 V and lower). Another choice could be Fast-Recovery, or Ultra-Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast-recovery diode with soft recovery characteristics can better fulfill some quality, low noise design requirements. Table 1 provides a list of suitable diodes for the LM2574 regulator. Standard $50 / 60 \mathrm{~Hz}$ rectifier diodes, such as the 1 N 4001 series or 1 N 5400 series are NOT suitable.

## Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design have a great influence on the reliability of the overall power supply.

Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) problems.

## Continuous and Discontinuous Mode of Operation

The LM2574 step-down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 24 and Figure 25). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2574 regulator was added to this data sheet (Figures 19 through 23). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 0.2 A ) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak-to-peak
current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.

## Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the amount of EMI (Electro-Magnetic Interference) shielding that the core must provide. There are many different styles of inductors available, such as pot core, E-core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not contained within the core.

When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E-core (closed magnetic structure) should be used in such applications.

## Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the dc resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2574 internal switch into cycle-by-cycle current limit, thus reducing the dc output load current. This can also result in overheating of the inductor and/or the LM2574. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.


HORIZONTAL TIME BASE: $5.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 24. Continuous Mode Switching Current Waveforms


HORIZONTAL TIME BASE: $5.0 \mu \mathrm{~s} /$ DIV
Figure 25. Continuous Mode Switching Current Waveforms

## GENERAL RECOMMENDATIONS

## Output Voltage Ripple and Transients Source of the Output Ripple

Since the LM2574 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from $0.5 \%$ to $3 \%$ of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

## Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 26). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimize these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.


HORIZONTAL TIME BASE: $5.0 \mu \mathrm{~s} / \mathrm{DIV}$

Figure 26. Output Ripple Voltage Waveforms

## Minimizing the Output Ripple

In order to minimize the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter $(20 \mu \mathrm{H}, 100 \mu \mathrm{~F})$, that can be added to the output (see Figure 35) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 26 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 34.

The upper waveform is from the normal unfiltered output of the converter, while the lower waveform shows the output ripple voltage filtered by an additional LC filter.

## Heatsinking and Thermal Considerations

The LM2574 is available in both 8-pin DIP and SO-16L packages. When used in the typical application the copper lead frame conducts the majority of the heat from the die, through the leads, to the printed circuit copper. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor.

For the best thermal performance, wide copper traces should be used and all ground and unused pins should be soldered to generous amounts of printed circuit board copper, such as a ground plane. Large areas of copper provide the best transfer of heat to the surrounding air. One exception to this is the output (switch) pin, which should not have large areas of copper in order to minimize coupling to sensitive circuitry.

Additional improvement in heat dissipation can be achieved even by using of double sided or multilayer boards which can provide even better heat path to the ambient. Using a socket for the 8-pin DIP package is not recommended because socket represents an additional thermal resistance, and as a result the junction temperature will be higher.

Since the current rating of the LM2574 is only 0.5 A , the total package power dissipation for this switcher is quite low, ranging from approximately 0.1 W up to 0.75 W under varying conditions. In a carefully engineered printed circuit board, the through-hole DIP package can easily dissipate up to 0.75 W , even at ambient temperatures of $60^{\circ} \mathrm{C}$, and still keep the maximum junction temperature below $125^{\circ} \mathrm{C}$.

## Thermal Analysis and Design

The following procedure must be performed to determine the operating junction temperature. First determine:

1. $\mathrm{P}_{\mathrm{D}(\max )}$ - maximum regulator power dissipation in the application.
2. $\mathrm{T}_{\mathrm{A}(\max )}$ - maximum ambient temperature in the application.
3. $\mathrm{T}_{\mathrm{J}(\max )}$ - maximum allowed junction temperature $\left(125^{\circ} \mathrm{C}\right.$ for the LM2574). For a conservative design, the maximum junction temperature should not exceed $110^{\circ} \mathrm{C}$ to assure safe operation. For every additional $+10^{\circ} \mathrm{C}$ temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $R_{\theta \mathrm{JC}}$ - package thermal resistance junction-case.
5. $\mathrm{R}_{\theta \mathrm{JA}}$ - package thermal resistance junction-ambient.
(Refer to Absolute Maximum Ratings on page 1279 of this data sheet or $R_{\theta J C}$ and $R_{\theta J \mathrm{~A}}$ values).

The following formula is to calculate the approximate total power dissipated by the LM2574:

$$
P_{D}=\left(V_{\text {in }} \times I_{Q}\right)+d \times I_{\text {Load }} \times V_{\text {sat }}
$$

where $d$ is the duty cycle and for buck converter

$$
\mathrm{d}=\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{~T}}=\frac{\mathrm{V}_{\mathrm{O}}}{\mathrm{~V}_{\mathrm{in}}},
$$

$\mathrm{I}_{\mathrm{Q}}$ (quiescent current) and $\mathrm{V}_{\text {sat }}$ can be found in the LM2574 data sheet,
$\mathrm{V}_{\text {in }}$ is minimum input voltage applied,
$\mathrm{V}_{\mathrm{O}}$ is the regulator output voltage,
$\mathrm{I}_{\text {Load }}$ is the load current.


Figure 27. Inverting Buck-Boost Develops -12 V

The dynamic switching losses during turn-on and turn-off can be neglected if a proper type catch diode is used. The junction temperature can be determined by the following expression:

$$
T_{J}=\left(R_{\theta J A}\right)\left(P_{D}\right)+T_{A}
$$

where $\left(R_{\theta J A}\right)\left(P_{D}\right)$ represents the junction temperature rise caused by the dissipated power and $\mathrm{T}_{\mathrm{A}}$ is the maximum ambient temperature.

## Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still. At higher power levels the thermal resistance decreases due to the increased air current activity.
Other factors are trace width, total printed circuit copper area, copper thickness, single- or double-sided, multilayer board, the amount of solder on the board or even color of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat. Some of them, like the catch diode or the inductor will generate some additional heat.

## ADDITIONAL APPLICATIONS

## Inverting Regulator

An inverting buck-boost regulator using the LM2574-12 is shown in Figure 27. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.
In this example the LM2574-12 is used to generate a -12 V output. The maximum input voltage in this case cannot exceed 28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V .

This circuit configuration is able to deliver approximately 0.1 A to the output when the input voltage is 8.0 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V , because the buck-boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck-boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck-boost inverting regulator can also require a larger amount of startup input current, even for light loads. This may overload an input power source with a current limit less than 0.6 A .

Because of the relatively high startup currents required by this inverting regulator topology, the use of a delayed startup or an undervoltage lockout circuit is recommended.

While using a delayed startup arrangement, the input capacitor can charge up to a higher voltage before the switch-mode regulator begins to operate.

The high input current needed for startup is now partially supplied by the input capacitor $\mathrm{C}_{\mathrm{in}}$.

## Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L1 or the output capacitor $\mathrm{C}_{\text {out }}$.

The output capacitor values must be larger than what is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of $\mu \mathrm{F}$ ).

The recommended range of inductor values for the inverting converter design is between $68 \mu \mathrm{H}$ and $220 \mu \mathrm{H}$. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.


Figure 28. Inverting Buck-Boost Regulator with Delayed Startup

The following formula is used to obtain the peak inductor current:

$$
\begin{aligned}
& \mathrm{I}_{\text {peak }} \approx \frac{\mathrm{I}_{\text {Load }}\left(\mathrm{V}_{\text {in }}+\left|\mathrm{V}_{\mathrm{O}}\right|\right)}{\mathrm{V}_{\mathrm{in}}}+\frac{\mathrm{V}_{\text {in }} \times \mathrm{t}_{\mathrm{on}}}{2 \mathrm{~L}_{1}} \\
& \text { where } \\
& \mathrm{t}_{\mathrm{on}}=\frac{\left|\mathrm{V}_{\mathrm{O}}\right|}{\mathrm{V}_{\mathrm{in}}+\left|\mathrm{V}_{\mathrm{O}}\right|} \times \frac{1.0}{f_{\mathrm{osc}}} \text {, and } \mathrm{f}_{\mathrm{osc}}=52 \mathrm{kHz} .
\end{aligned}
$$

Under normal continuous inductor current operating conditions, the worst case occurs when $\mathrm{V}_{\mathrm{in}}$ is minimal.

It has been already mentioned above, that in some situations, the delayed startup or the undervoltage lockout features could be very useful. A delayed startup circuit applied to a buck-boost converter is shown in Figure 28. Figure 34 in the "Undervoltage Lockout" section describes an undervoltage lockout feature for the same converter topology.

With the inverting configuration, the use of the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin requires some level shifting techniques. This is caused
by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin threshold voltage (1.3 V approximately) has to be related to the negative output voltage level. There are many different possible shutdown methods, two of them are shown in Figures 29 and 30.


NOTE: This picture does not show the complete circuit.
Figure 29. Inverting Buck-Boost Regulator Shutdown Circuit Using an Optocoupler


NOTE: This picture does not show the complete circuit.
Figure 30. Inverting Buck-Boost Regulator Shutdown Circuit Using a PNP Transistor

## Negative Boost Regulator

This example is a variation of the buck-boost topology and it is called negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

The circuit in Figure 31 shows the negative boost configuration. The input voltage in this application ranges from -5.0 to -12 V and provides a regulated -12 V output. If the input voltage is greater than -12 V , the output will rise above -12 V accordingly, but will not damage the regulator.


Figure 31. Negative Boost Regulator

## Design Recommendations:

The same design rules as for the previous inverting buck-boost converter can be applied. The output capacitor $\mathrm{C}_{\text {out }}$ must be chosen larger than what would be required for a standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of $\mu \mathrm{F}$ ). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

Another important point is that these negative boost converters cannot provide any current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

## Delayed Startup

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of startup current. In such cases, if the input power source is limited, this delayed startup feature becomes very useful.

To provide a time delay between the time when the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 32 can be used. As the input voltage is applied, the capacitor C 1 charges up, and the voltage across the resistor R2 falls down. When the voltage on the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin falls below the threshold value 1.3 V , the regulator starts up. Resistor R1 is included to limit the maximum voltage applied to the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin. It reduces the power supply noise sensitivity, and also limits the capacitor C 1 discharge current, but its use is not mandatory.

When a high 50 Hz or $60 \mathrm{~Hz}(100 \mathrm{~Hz}$ or 120 Hz respectively) ripple voltage exists, a long delay time can cause some problems by coupling the ripple into the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin, the regulator could be switched periodically on and off with the line (or double) frequency.


NOTE: This picture does not show the complete circuit.
Figure 32. Delayed Startup Circuitry

## Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 33 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck-boost converter is shown in Figure 34. Resistor R3 pulls the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level, which is determined by the following expression:


NOTE: This picture does not show the complete circuit.
Figure 33. Undervoltage Lockout Circuit for Buck Converter

## LM2574



NOTE: This picture does not show the complete circuit (see Figure 27).
Figure 34. Undervoltage Lockout Circuit for Buck-Boost Converter

## Adjustable Output, Low-Ripple Power Supply

A 0.5 A output current capability power supply that features an adjustable output voltage is shown in Figure 35.
This regulator delivers 0.5 A into 1.2 to 35 V output. The input voltage ranges from roughly 3.0 to 40 V . In order to achieve a 10 or more times reduction of output ripple, an additional $\mathrm{L}-\mathrm{C}$ filter is included in this circuit.


Figure 35. 1.2 to 35 V Adjustable 500 mA Power Supply with Low Output Ripple

The LM2574-5 Step-Down Voltage Regulator with 5.0 V @ 0.5 A Output Power Capability. Typical Application With Through-Hole PC Board Layout


Figure 36. Schematic Diagram of the LM2574-5 Step-Down Converter


NOTE: Not to scale.
Figure 37. PC Board Layout Component Side


NOTE: Not to scale.
Figure 38. PC Board Layout Copper Side

The LM2574-ADJ Step-Down Voltage Regulator with 5.0 V @ 0.5 A Output Power Capability Typical Application With Through-Hole PC Board Layout


Figure 39. Schematic Diagram of the 5.0 V @ 0.5 A Step-Down Converter Using the LM2574-ADJ (An additional LC filter is included to achieve low output ripple voltage)


NOTE: Not to scale.
Figure 40. PC Board Layout Component Side


NOTE: Not to scale.
Figure 41. PC Board Layout Copper Side

## References

- Marty Brown "Practical Switching Power Supply Design", Academic Press, Inc., San Diego 1990
- Ray Ridley "High Frequency Magnetics Design", Ridley Engineering, Inc. 1995


## LM2574

ORDERING INFORMATION

| Device | Nominal Output Voltage | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| LM2574DW－ADJ | 1．23 V to 37 V | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | SO－16W | 47 Units／Rail |
| LM2574DW－ADJR2 |  |  | SO－16W | 1000 Units／Tape \＆Reel |
| LM2574N－ADJ |  |  | PDIP－8 | 50 Units／Rail |
| LM2574N－3．3 | 3.3 V |  | PDIP－8 | 50 Units／Rail |
| LM2574N－5 | 5.0 V |  | PDIP－8 | 50 Units／Rail |
| LM2574N－12 | 12 V |  | PDIP－8 | 50 Units／Rail |
| LM2574N－15 | 15 V |  | PDIP－8 | 50 Units／Rail |

MARKING DIAGRAMS

SO－16W DW SUFFIX CASE 751G

16

2574DW－ADJ
AWL
－YYWW
昭昭昭昭

PDIP－8
N SUFFIX
CASE 626


A＝Assembly Location
WL＝Wafer Lot
YY＝Year
WW＝Work Week

## LM2575

### 1.0 A, Adjustable Output Voltage, Step-Down Switching Regulator

The LM2575 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 1.0 A load with excellent line and load regulation. These devices are available in fixed output voltages of $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, $12 \mathrm{~V}, 15 \mathrm{~V}$, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2575 are offered by several different inductor manufacturers.

Since the LM2575 converter is a switch-mode power supply, its efficiency is significantly higher in comparison with popular three-terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated by the LM2575 regulator is so low, that no heatsink is required or its size could be reduced dramatically.

The LM2575 features include a guaranteed $\pm 4 \%$ tolerance on output voltage within specified input voltages and output load conditions, and $\pm 10 \%$ on the oscillator frequency ( $\pm 2 \%$ over $0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ ). External shutdown is included, featuring $80 \mu \mathrm{~A}$ typical standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

## Features

- 3.3 V, 5.0 V, $12 \mathrm{~V}, 15 \mathrm{~V}$, and Adjustable Output Versions
- Adjustable Version Output Voltage Range of 1.23 V to $37 \mathrm{~V} \pm 4 \%$ Maximum Over Line and Load Conditions
- Guaranteed 1.0 A Output Current
- Wide Input Voltage Range: 4.75 V to 40 V
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- Moisture Sensitivity Level (MSL) Equals 1


## Applications

- Simple and High-Efficiency Step-Down (Buck) Regulators
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converters (Buck-Boost)
- Negative Step-Up Converters
- Power Supply for Battery Chargers

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


Heatsink surface connected to Pin 3


TO-220
T SUFFIX
CASE 314D

Pin 1. $V_{\text {in }}$
2. Output
3. Ground
4. Feedback
5. $\overline{\mathrm{ON}} / \mathrm{OFF}$

$D^{2}$ PAK D2T SUFFIX CASE 936A

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1325 of this data sheet. section on page 1325 of this data sheet.

## Typical Application (Fixed Output Voltage Versions)



Representative Block Diagram and Typical Application


This device contains 162 active transistors.
Figure 1. Block Diagram and Typical Application

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Maximum Supply Voltage | $\mathrm{V}_{\text {in }}$ | 45 | V |
| ON/OFF Pin Input Voltage | - | $-0.3 \mathrm{~V} \leq \mathrm{V} \leq+\mathrm{V}_{\text {in }}$ | V |
| Output Voltage to Ground (Steady-State) | - | -1.0 | V |
| Power Dissipation <br> Case 314B and 314D (TO-220, 5-Lead) <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case <br> Case 936A (D²PAK) <br> Thermal Resistance, Junction-to-Ambient (Figure 34) <br> Thermal Resistance, Junction-to-Case | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJc }}$ | Internally Limited 65 5.0 Internally Limited 70 5.0 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{w} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{w} \end{gathered}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Minimum ESD Rating (Human Body Model: $\mathrm{C}=100 \mathrm{pF}, \mathrm{R}=1.5 \mathrm{k} \Omega$ ) | - | 3.0 | kV |
| Lead Temperature (Soldering, 10 s ) | - | 260 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | TJ | 150 | ${ }^{\circ} \mathrm{C}$ |

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Supply Voltage | $\mathrm{V}_{\text {in }}$ | 40 | V |

## SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 14)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $\mathrm{V}_{\text {in }}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, and Adjustable version, $\mathrm{V}_{\text {in }}=25 \mathrm{~V}$ for the 12 V version, and $\mathrm{V}_{\text {in }}=30 \mathrm{~V}$ for the 15 V version. $\mathrm{I}_{\text {Load }}=200 \mathrm{~mA}$. For typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{J}$ is the operating junction temperature range that applies [Note 2], unless otherwise noted.)
Characteristics

|  | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| LM2575-3.3 ([Note 1] Test Circuit Figure 14) |  |  |  |  |  |
| Output Voltage $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.2 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 3.234 | 3.3 | 3.366 | V |
| Output Voltage $\left(4.75 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 1.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 3.168 | 3.3 | 3.432 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 3.135 | - | 3.465 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=1.0 \mathrm{~A}\right)$ | $\eta$ | - | 75 | - | $\%$ |

LM2575-5 ([Note 1] Test Circuit Figure 14)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.2 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 4.9 | 5.0 | 5.1 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(8.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 1.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 4.8 | 5.0 | 5.2 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 4.75 | - | 5.25 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=1.0 \mathrm{~A}\right)$ | $\eta$ | - | 77 | - | $\%$ |

LM2575-12 ([Note 1] Test Circuit Figure 14)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.2 \mathrm{~A}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 11.76 | 12 | 12.24 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(15 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 1.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 11.52 | 12 | 12.48 |  |
| $\mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 11.4 | - | 12.6 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=15 \mathrm{~V}, \mathrm{I}_{\text {Load }}=1.0 \mathrm{~A}\right)$ | $\eta$ | - | 88 | - | $\%$ |

LM2575-15 ([Note 1] Test Circuit Figure 14)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=30 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.2 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 14.7 | 15 | 15.3 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(18 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 1.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 14.4 | 15 | 15.6 |  |
| $\mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 14.25 | - | 15.75 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=18 \mathrm{~V}, \mathrm{I}_{\text {Load }}=1.0 \mathrm{~A}\right)$ | $\eta$ | - | 88 | - | $\%$ |

LM2575 ADJUSTABLE VERSION ([Note 1] Test Circuit Figure 14)

| Feedback Voltage $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.2 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{FB}}$ | 1.217 | 1.23 | 1.243 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Feedback Voltage $\left(8.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.2 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 1.0 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{FB}}$ |  |  |  |  |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 1.193 | 1.23 | 1.267 | V |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 1.18 | - | 1.28 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=1.0 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}\right)$ | $\eta$ | - | 77 | - | $\%$ |

1. External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2575 is used as shown in the Figure 14 test circuit, system performance will be as shown in system parameters section.
2. Tested junction temperature range for the LM2575: $\quad \mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} \quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$

## DEVICE PARAMETERS

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $\mathrm{V}_{\text {in }}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, and Adjustable version, $\mathrm{V}_{\text {in }}=25 \mathrm{~V}$ for the 12 V version, and $\mathrm{V}_{\text {in }}=30 \mathrm{~V}$ for the 15 V version. $\mathrm{I}_{\text {Load }}=200 \mathrm{~mA}$. For typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{J}$ is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

ALL OUTPUT VOLTAGE VERSIONS

| $\begin{aligned} & \text { Feedback Bias Current (Vout }=5.0 \mathrm{~V} \text { [Adjustable Version Only] }) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{l}_{\mathrm{b}}$ |  | 25 | $\begin{aligned} & 100 \\ & 200 \end{aligned}$ | nA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillator Frequency [Note 3] $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=0 \text { to }+125^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{f}_{\text {osc }}$ | $\begin{aligned} & - \\ & 47 \\ & 47 \end{aligned}$ | $52$ | $\begin{aligned} & 58 \\ & 63 \end{aligned}$ | kHz |
| $\begin{aligned} & \text { Saturation Voltage ( } \text { lout }=1.0 \mathrm{~A}[\text { Note } 4] \text { ) } \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {sat }}$ | - | 1.0 | $\begin{aligned} & 1.2 \\ & 1.3 \end{aligned}$ | V |
| Max Duty Cycle ("on") [Note 5] | DC | 94 | 98 | - | \% |
| Current Limit (Peak Current [Notes 4 and 3]) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $\mathrm{I}_{\text {CL }}$ | $\begin{aligned} & 1.7 \\ & 1.4 \end{aligned}$ | 2.3 | $\begin{aligned} & 3.0 \\ & 3.2 \end{aligned}$ | A |
| Output Leakage Current [Notes 6 and 7 ], $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ $\begin{aligned} & \text { Output }=0 \mathrm{~V} \\ & \text { Output }=-1.0 \mathrm{~V} \end{aligned}$ | L | - |  | $\begin{aligned} & 2.0 \\ & 20 \end{aligned}$ | mA |
| Quiescent Current [Note 6] $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{l}_{\mathrm{Q}}$ | - | 5.0 | $\begin{gathered} 9.0 \\ 11 \end{gathered}$ | mA |
| Standby Quiescent Current (ON/OFF Pin =5.0 V ("off")) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\text {stby }}$ | - | 80 | $\begin{aligned} & 200 \\ & 400 \\ & \hline \end{aligned}$ | $\mu \mathrm{A}$ |
| ON/OFF Pin Logic Input Level (Test Circuit Figure 14) $\begin{aligned} \mathrm{V}_{\text {out }} & =0 \mathrm{~V} \\ \mathrm{~T}_{J} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J} & =-40 \text { to }+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {out }} & =\text { Nominal Output Voltage } \\ \mathrm{T}_{J} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J} & =-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{IH}}$ $\mathrm{V}_{\mathrm{IL}}$ | 2.2 2.4 | 1.4 - 1.2 | $\begin{aligned} & 1.0 \\ & 0.8 \end{aligned}$ | V |
| ON/OFF Pin Input Current (Test Circuit Figure 14) ON/OFF Pin $=5.0 \mathrm{~V}$ ("off"), $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ $\overline{O N} / O F F$ Pin $=0 \mathrm{~V}$ ("on"), $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\begin{aligned} & I_{\mathrm{IH}} \\ & I_{\mathrm{IL}} \end{aligned}$ | - | 15 0 |  | $\mu \mathrm{A}$ |

3. The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately $40 \%$ from the nominal output voltage. This self protection feature lowers the average dissipation of the IC by lowering the minimum duty cycle from $5 \%$ down to approximately $2 \%$.
4. Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to output pin.
5. Feedback (Pin 4) removed from output and connected to 0 V .
6. Feedback (Pin 4) removed from output and connected to +12 V for the Adjustable, 3.3 V , and 5.0 V versions, and +25 V for the 12 V and 15 V versions, to force the output transistor "off".
7. $\mathrm{V}_{\mathrm{in}}=40 \mathrm{~V}$.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 14)


Figure 2. Normalized Output Voltage


Figure 4. Switch Saturation Voltage


Figure 6. Dropout Voltage


Figure 3. Line Regulation


Figure 5. Current Limit


Figure 7. Quiescent Current


Figure 8. Standby Quiescent Current


Figure 10. Oscillator Frequency


Figure 12. Switching Waveforms


Figure 9. Standby Quiescent Current


Figure 11. Feedback Pin Current


Figure 13. Load Transient Response


Adjustable Output Voltage Versions


Where $\mathrm{V}_{\text {ref }}=1.23 \mathrm{~V}$, R1
between $1.0 \mathrm{k} \Omega$ and $5.0 \mathrm{k} \Omega$
Figure 14. Typical Test Circuit

## PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 14, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. For best results, single-point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 2 (emitter of the internal switch) of the LM2575 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2575 regulator.

PIN FUNCTION DESCRIPTION

| Pin | Symbol | Description (Refer to Figure 1) |
| :---: | :---: | :--- |
| 1 | $V_{\text {in }}$ | This pin is the positive input supply for the LM2575 step-down switching regulator. In order to minimize <br> voltage transients and to supply the switching currents needed by the regulator, a suitable input bypass <br> capacitor must be present (C in in Figure 1). |
| 2 | Output | This is the emitter of the internal switch. The saturation voltage $V_{\text {sat }}$ of this output switch is typically 1.0 V . <br> It should be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to <br> minimize coupling to sensitive circuitry. |
| 3 | Gnd | Circuit ground pin. See the information about the printed circuit board layout. |
| 4 | Feedback | This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the <br> internal resistor divider network R2, R1 and applied to the non-inverting input of the internal error amplifier. <br> In the Adjustable version of the LM2575 switching regulator this pin is the direct input of the error amplifier <br> and the resistor network R2, R1 is connected externally to allow programming of the output voltage. |
| 5 | ON/OFF | It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total <br> input supply current to approximately 80 $\mu \mathrm{A}$. The input threshold voltage is typically 1.4 V . Applying a <br> voltage above this value (up to + $+\mathrm{V}_{\text {in }}$ ) shuts the regulator off. If the voltage applied to this pin is lower than <br> 1.4 V or if this pin is connected to ground, the regulator will be in the "on" condition. |

## DESIGN PROCEDURE

## Buck Converter Basics

The LM2575 is a "Buck" or Step-Down Converter which is the most elementary forward-mode converter. Its basic schematic can be seen in Figure 15.

The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$
\mathrm{I}_{\mathrm{L}(\mathrm{on})}=\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \mathrm{t}_{\text {on }}}{\mathrm{L}}
$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.


Figure 15. Basic Buck Converter

The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by catch dioded. Current now flows through the catch diode thus maintaining the load current loop. This removes the stored energy from the inductor. The inductor current during this time is:

$$
I_{L(\text { off })}=\frac{\left(v_{\text {out }}-V_{D}\right) t_{\text {off }}}{L}
$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

$$
\mathrm{d}=\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{~T}} \text {, where } \mathrm{T} \text { is the period of switching. }
$$

For the buck converter with ideal components, the duty cycle can also be described as:

$$
\mathrm{d}=\frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}}
$$

Figure 16 shows the buck converter idealized waveforms of the catch diode voltage and the inductor current.


Figure 16. Buck Converter Idealized Waveforms

Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

| Procedure |
| :--- |
| Given Parameters: <br> $V_{\text {out }}=$ Regulated Output Voltage $(3.3 \mathrm{~V}, 5.0 \mathrm{~V}, 12 \mathrm{~V}$ or 15 V$)$ <br> $\mathrm{V}_{\text {in(max) }}=$ Maximum DC Input Voltage <br> $\mathrm{I}_{\text {Load(max) }}=$ Maximum Load Current |
| 1. Controller IC Selection |
| According to the required input voltage, output voltage and |
| current, select the appropriate type of the controller IC output |
| voltage version. |

## 3. Catch Diode Selection (D1)

A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.
4. Inductor Selection (L1)
A. According to the required working conditions, select the correct inductor value using the selection guide from Figures 17 to 21.
B. From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code.
C. Select an appropriate inductor from the several different manufacturers part numbers listed in Table 1 or Table 2. When using Table 2 for selecting the right inductor the designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows:

$$
\begin{aligned}
& \text { ws: } \\
& I_{p(\text { max })}=I_{\text {Load (max })}+\frac{\left(V_{\text {in }}-V_{\text {out }}\right) t_{\text {on }}}{2 L}
\end{aligned}
$$

where $\mathrm{t}_{\mathrm{on}}$ is the "on" time of the power switch and

$$
t_{\text {on }}=\frac{V_{\text {out }}}{V_{\text {in }}} \times \frac{1}{f_{\text {osc }}}
$$

For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.

1. Controller IC Selection

According to the required input voltage, output voltage, current polarity and current value, use the LM2575-5 controller IC
2. Input Capacitor Selection ( $\mathrm{C}_{\text {in }}$ )

A $47 \mu \mathrm{~F}, 25 \mathrm{~V}$ aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing.
3. Catch Diode Selection (D1)
A. For this example the current rating of the diode is 1.0 A .
B. Use a 30 V 1 N 5818 Schottky diode, or any of the suggested fast recovery diodes shown in the Table 4.
4. Inductor Selection (L1)
A. Use the inductor selection guide shown in Figures 17 to 21 .
B. From the selection guide, the inductance area intersected by the 20 V line and 0.8 A line is L330.
C. Inductor value required is $330 \mu \mathrm{H}$. From the Table 1 or Table 2, choose an inductor from any of the listed manufacturers.

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Procedure (Fixed Output Voltage Version) (continued)In order to simplify the switching regulator design, a step-by-step design procedure and example is provided.

| Procedure | Example |
| :---: | :---: |
| 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ ) <br> A. Since the LM2575 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-2-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately $1 \%$ of the output voltage) a value between $100 \mu \mathrm{~F}$ and $470 \mu \mathrm{~F}$ is recommended. <br> B. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8 V is appropriate, and a 10 V or 16 V rating is recommended. | 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ ) <br> A. $\mathrm{C}_{\text {out }}=100 \mu \mathrm{~F}$ to $470 \mu \mathrm{~F}$ standard aluminium electrolytic. <br> B. Capacitor voltage rating $=16 \mathrm{~V}$. |

## Procedure (Adjustable Output Version: LM2575-Adj)

| Procedure | Example |
| :---: | :---: |
| Given Parameters: <br> $\mathrm{V}_{\text {out }}=$ Regulated Output Voltage <br> $V_{\text {in(max) }}=$ Maximum DC Input Voltage <br> $I_{\text {Load(max) }}=$ Maximum Load Current | Given Parameters: $\begin{aligned} & V_{\text {out }}=8.0 \mathrm{~V} \\ & \mathrm{~V}_{\text {in }(\max )}=12 \mathrm{~V} \\ & I_{\text {Load }(\max )}=1.0 \mathrm{~A} \end{aligned}$ |
| 1. Programming Output Voltage <br> To select the right programming resistor R1 and R2 value (see Figure 14) use the following formula: $V_{\text {out }}=V_{\text {ref }}\left(1+\frac{R 2}{R 1}\right) \text { where } V_{\text {ref }}=1.23 \mathrm{~V}$ <br> Resistor R1 can be between 1.0 k and $5.0 \mathrm{k} \Omega$. (For best temperature coefficient and stability with time, use $1 \%$ metal film resistors). $\mathrm{R} 2=\mathrm{R} 1\left(\frac{\mathrm{~V}_{\text {out }}}{\mathrm{V}_{\text {ref }}}-1\right)$ | 1. Programming Output Voltage (selecting R1 and R2) Select R1 and R2: $\begin{aligned} & \mathrm{V}_{\text {out }}=1.23\left(1+\frac{\mathrm{R} 2}{\mathrm{R} 1}\right) \text { Select } \mathrm{R} 1=1.8 \mathrm{k} \Omega \\ & \mathrm{R} 2=\mathrm{R} 1\left(\frac{\mathrm{~V}_{\text {out }}}{\mathrm{V}_{\text {ref }}}-1\right)=1.8 \mathrm{k}\left(\frac{8.0 \mathrm{~V}}{1.23 \mathrm{~V}}-1\right) \end{aligned}$ <br> $R 2=9.91 \mathrm{k} \Omega$, choose a 9.88 k metal film resistor. |
| 2. Input Capacitor Selection ( $\mathrm{C}_{\text {in }}$ ) <br> To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+\mathrm{V}_{\text {in }}$ and ground pin Gnd This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value. <br> For additional information see input capacitor section in the "External Components" section of this data sheet. | 2. Input Capacitor Selection ( $\mathrm{C}_{\text {in }}$ ) A $100 \mu \mathrm{~F}$ aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing. |
| 3. Catch Diode Selection (D1) <br> A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short. <br> B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage. | 3. Catch Diode Selection (D1) <br> A. For this example, a 3.0 A current rating is adequate. <br> B. Use a 20 V 1 N 5820 or MBR320 Schottky diode or any suggested fast recovery diode in the Table 4. |

Procedure (Adjustable Output Version: LM2575-Adj) (continued)

| Procedure |
| :--- |
| 4. Inductor Selection (L1) |
| A. Use the following formula to calculate the inducto |
| microsecond $[\mathrm{V} \times \mu \mathrm{s}]$ constant: |
| $E \mathrm{E} \times T=\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {on }}} \times \frac{10^{6}}{\mathrm{~F}[\mathrm{~Hz}]}[\mathrm{V} \times \mu \mathrm{s}]$ |

B. Match the calculated $\mathrm{E} \times \mathrm{T}$ value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 21. This $\mathrm{E} \times \mathrm{T}$ constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle.
C. Next step is to identify the inductance region intersected by the $E \times T$ value and the maximum load current value on the horizontal axis shown in Figure 21.
D. From the inductor code, identify the inductor value. Then select an appropriate inductor from the Table 1 or Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of $1.15 \times \mathrm{I}_{\text {Ioad }}$. The inductor current rating can also be determined by calculating the inductor peak current:

$$
I_{p(\max )}=I_{\text {Load }(\max )}+\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \mathrm{t}_{\text {on }}}{2 \mathrm{~L}}
$$

where $t_{o n}$ is the "on" time of the power switch and

$$
t_{\text {on }}=\frac{V_{\text {out }}}{V_{\text {in }}} \times \frac{1}{f_{\text {osc }}}
$$

For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.

## 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ )

A. Since the LM2575 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-2-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values.

For stable operation, the capacitor must satisfy the following requirement:

$$
C_{\text {out }} \geq 7.785 \frac{V_{\text {in }(\max )}}{V_{\text {out }} \times L[\mu \mathrm{H}]}[\mu \mathrm{F}]
$$

B. Capacitor values between $10 \mu \mathrm{~F}$ and $2000 \mu \mathrm{~F}$ will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields.
C. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8 V is appropriate, and a 10 V or 16 V rating is recommended.

## 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ )

A.

$$
C_{\text {out }} \geq 7.785 \frac{12}{8.220}=53 \mu \mathrm{~F}
$$

To achieve an acceptable ripple voltage, select $\mathrm{C}_{\text {out }}=100 \mu \mathrm{~F}$ electrolytic capacitor.

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INDUCTOR VALUE SELECTION GUIDE


Figure 17. LM2575-3.3


Figure 19. LM2575-12


Figure 18. LM2575-5.0


Figure 20. LM2575-15


Figure 21. LM2575-Adj

NOTE: This Inductor Value Selection Guide is applicable for continuous mode only.

## LM2575

Table 1. Inductor Selection Guide

| Inductor Code | Inductor Value | Pulse Eng | Renco | AIE | Tech 39 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L100 | $100 \mu \mathrm{H}$ | PE-92108 | RL2444 | 415-0930 | 77308 BV |
| L150 | $150 \mu \mathrm{H}$ | PE-53113 | RL1954 | 415-0953 | 77358 BV |
| L220 | $220 \mu \mathrm{H}$ | PE-52626 | RL1953 | 415-0922 | 77408 BV |
| L330 | $330 \mu \mathrm{H}$ | PE-52627 | RL1952 | 415-0926 | 77458 BV |
| L470 | $470 \mu \mathrm{H}$ | PE-53114 | RL1951 | 415-0927 | - |
| L680 | $680 \mu \mathrm{H}$ | PE-52629 | RL1950 | 415-0928 | 77508 BV |
| H150 | $150 \mu \mathrm{H}$ | PE-53115 | RL2445 | 415-0936 | 77368 BV |
| H220 | $220 \mu \mathrm{H}$ | PE-53116 | RL2446 | 430-0636 | 77410 BV |
| H330 | $330 \mu \mathrm{H}$ | PE-53117 | RL2447 | 430-0635 | 77460 BV |
| H470 | $470 \mu \mathrm{H}$ | PE-53118 | RL1961 | 430-0634 | - |
| H680 | $680 \mu \mathrm{H}$ | PE-53119 | RL1960 | 415-0935 | 77510 BV |
| H1000 | $1000 \mu \mathrm{H}$ | PE-53120 | RL1959 | 415-0934 | 77558 BV |
| H1500 | $1500 \mu \mathrm{H}$ | PE-53121 | RL1958 | 415-0933 | - |
| H2200 | $2200 \mu \mathrm{H}$ | PE-53122 | RL2448 | 415-0945 | 77610 BV |

Table 2. Inductor Selection Guide

| Inductance | Current | Schott |  | Renco |  | Pulse Engineering |  | Coilcraft |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $(\mu \mathrm{H})$ | (A) | THT | SMT | THT | SMT | THT | SMT | SMT |
|  | 0.32 | 67143940 | 67144310 | RL-1284-68-43 | RL1500-68 | PE-53804 | PE-53804-S | DO1608-68 |
|  | 0.58 | 67143990 | 67144360 | RL-5470-6 | RL1500-68 | PE-53812 | PE-53812-S | DO3308-683 |
|  | 0.99 | 67144070 | 67144450 | RL-5471-5 | RL1500-68 | PE-53821 | PE-53821-S | DO3316-683 |
|  | 1.78 | 67144140 | 67144520 | RL-5471-5 | - | PE-53830 | PE-53830-S | DO5022P-683 |
|  | 0.48 | 67143980 | 67144350 | RL-5470-5 | RL1500-100 | PE-53811 | PE-53811-S | DO3308-104 |
| 100 | 0.82 | 67144060 | 67144440 | RL-5471-4 | RL1500-100 | PE-53820 | PE-53820-S | DO3316-104 |
|  | 1.47 | 67144130 | 67144510 | RL-5471-4 | - | PE-53829 | PE-53829-S | DO5022P-104 |
|  | 0.39 | - | 67144340 | RL-5470-4 | RL1500-150 | PE-53810 | PE-53810-S | DO3308-154 |
| 150 | 0.66 | 67144050 | 67144430 | RL-5471-3 | RL1500-150 | PE-53819 | PE-53819-S | DO3316-154 |
|  | 1.20 | 67144120 | 67144500 | RL-5471-3 | - | PE-53828 | PE-53828-S | DO5022P-154 |
|  | 0.32 | 67143960 | 67144330 | RL-5470-3 | RL1500-220 | PE-53809 | PE-53809-S | DO3308-224 |
| 220 | 0.55 | 67144040 | 67144420 | RL-5471-2 | RL1500-220 | PE-53818 | PE-53818-S | DO3316-224 |
|  | 1.00 | 67144110 | 67144490 | RL-5471-2 | - | PE-53827 | PE-53827-S | DO5022P-224 |
|  | 0.42 | 67144030 | 67144410 | RL-5471-1 | RL1500-330 | PE-53817 | PE-53817-S | DO3316-334 |
| 330 | 0.80 | 67144100 | 67144480 | RL-5471-1 | - | PE-53826 | PE-53826-S | DO5022P-334 |

NOTE: Table 1 and Table 2 of this Indicator Selection Guide shows some examples of different manufacturer products suitable for design with the LM2575.

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Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

| Pulse Engineering Inc. | Phone <br> Fax | $+1-619-674-8100$ <br> $+1-619-674-8262$ |
| :--- | :--- | :--- |
| Pulse Engineering Inc. Europe | Phone <br> Fax | +3539324107 <br> +3539324459 |
| Renco Electronics Inc. | Phone <br> Fax | $+1-516-645-5828$ <br> $+1-516-586-5562$ |
| AIE Magnetics | Phone <br> Fax | $+1-813-347-2181$ |
| Coilcraft Inc. | Phone <br> Fax | $+1-708-322-2645$ <br> $+1-708-639-1469$ |
| Coilcraft Inc., Europe | Phone <br> Fax | +441236730595 <br> +441236730627 |
| Tech 39 | Phone <br> Fax | +3384252626 <br> +3384252610 |
| Schott Corp. | Phone <br> Fax | $+1-612-475-1173$ <br> $+1-612-475-1786 ~$ |

Table 4. Diode Selection Guide gives an overview about both surface-mount and through-hole diodes for an effective design. Device listed in bold are available from ON Semiconductor.

| $\mathrm{V}_{\mathrm{R}}$ | Schottky |  |  |  | Ultra-Fast Recovery |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1.0 A |  | 3.0 A |  | 1.0 A |  | 3.0 A |  |
|  | SMT | THT | SMT | THT | SMT | THT | SMT | THT |
| 20 V | SK12 | 1N5817 SR102 | $\begin{gathered} \text { SK32 } \\ \text { MBRD320 } \end{gathered}$ | 1N5820 MBR320 SR302 | MURS120T3 | $\begin{aligned} & \text { MUR120 } \\ & \text { 11DF1 } \\ & \text { HER102 } \end{aligned}$ | MURS320T3 | MUR320 30WF10 MUR420 |
| 30 V | $\begin{gathered} \hline \text { MBRS130LT3 } \\ \text { SK13 } \end{gathered}$ | 1N5818 SR103 11DQ03 | $\begin{gathered} \hline \text { SK33 } \\ \text { MBRD330 } \end{gathered}$ | 1N5821 MBR330 SR303 31DQ03 |  |  |  |  |
| 40 V | $\begin{gathered} \hline \text { MBRS140T3 } \\ \text { SK14 } \\ \text { 10BQ040 } \\ \text { 10MQ040 } \end{gathered}$ | 1N5819 SR104 11DQ04 | $\begin{gathered} \text { MBRS340T3 } \\ \text { MBRD340 } \\ \text { 30WQ04 } \\ \text { SK34 } \end{gathered}$ | 1N5822 MBR340 SR304 31DQ04 | 10BF10 |  | MURD320 |  |
| 50 V | $\begin{gathered} \hline \text { MBRS150 } \\ \text { 10BQ050 } \end{gathered}$ | MBR150 SR105 11DQ05 | $\begin{gathered} \hline \text { MBRD350 } \\ \text { SK35 } \\ \text { 30WQ05 } \end{gathered}$ | MBR350 SR305 11DQ05 |  |  | $\begin{aligned} & \text { 31DF1 } \\ & \text { HER302 } \end{aligned}$ |  |

## EXTERNAL COMPONENTS

## Input Capacitor ( $\mathrm{C}_{\text {in }}$ ) The Input Capacitor Should Have a Low ESR

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below $-25^{\circ} \mathrm{C}$ larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

## RMS Current Rating of $C_{\text {in }}$

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequence of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$
\mathrm{I}_{\mathrm{rms}}>1.2 \times \mathrm{dx} \mathrm{I}_{\text {Load }}
$$

where d is the duty cycle, for a buck regulator

$$
\mathrm{d}=\frac{\mathrm{t}_{\text {on }}}{\mathrm{T}}=\frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}}
$$

and $d=\frac{t_{\text {on }}}{T}=\frac{\left|V_{\text {out }}\right|}{\left|V_{\text {out }}\right|+V_{\text {in }}}$ for a buck-boost regulator.

## Output Capacitor ( $\mathrm{C}_{\text {out }}$ )

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak-to-peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value. Standard aluminium electrolytics could be adequate for some applications but for quality design low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher voltage ratings may be needed to provide low ESR values that are required for low output ripple voltage.

## The Output Capacitor Requires an ESR Value That Has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low (below $0.05 \Omega$ ), there is a possibility of an unstable feedback
loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

## At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 times at $-25^{\circ} \mathrm{C}$ and as much as 10 times at $-40^{\circ} \mathrm{C}$. Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$. They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about $10 \%$ or $20 \%$ of the total capacitance. The output capacitor should have at least $50 \%$ higher RMS ripple current rating at 52 kHz than the peak-to-peak inductor ripple current.

## Catch Diode <br> Locate the Catch Diode Close to the LM2575

The LM2575 is a step-down buck converter; it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2575 using short leads and short printed circuit traces to avoid EMI problems.

## Use a Schottky or a Soft Switching Ultra-Fast Recovery Diode

Since the rectifier diodes are very significant source of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.
They provide the best efficiency especially in low output voltage applications ( 5.0 V and lower). Another choice could be Fast-Recovery, or Ultra-Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast-recovery diode with soft recovery characteristics can better fulfill a quality, low noise design requirements. Table 4 provides a list of suitable diodes for the LM2575 regulator. Standard $50 / 60 \mathrm{~Hz}$ rectifier diodes such as the 1N4001 series or 1N5400 series are NOT suitable.

## Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design has a great influence on the reliability of the overall power supply.
Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) problems.

## Continuous and Discontinuous Mode of Operation

The LM2575 step-down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 22 and Figure 23). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2575 regulator was added to this data sheet (Figures 17 through 21). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 200 mA ) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak-to-peak current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.


HORIZONTAL TIME BASE: $5.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 22. Continuous Mode Switching Current Waveforms

## Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the
amount of EMI (Electro-Magnetic Interference) shielding that the core must provide. The inductor selection guide covers different styles of inductors, such as pot core, E-core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is completely contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not completely contained within the core.

When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E-core (closed magnetic structure) should be used in such applications.

## Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the dc resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2575 internal switch into cycle-by-cycle current limit, thus reducing the dc output load current. This can also result in overheating of the inductor and/or the LM2575. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.


Figure 23. Discontinuous Mode Switching Current Waveforms

## GENERAL RECOMMENDATIONS

## Output Voltage Ripple and Transients Source of the Output Ripple

Since the LM2575 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from $0.5 \%$ to $3 \%$ of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

## Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 24). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimize these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.


HORIZONTAL TIME BASE: $10 \mu \mathrm{~s} /$ DIV
Figure 24. Output Ripple Voltage Waveforms

## Minimizing the Output Ripple

In order to minimize the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter $(20 \mu \mathrm{H}, 100 \mu \mathrm{~F})$, that can be added to the output (see Figure 33) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 24 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 33.

The upper waveform is from the normal unfiltered output of the converter, while the lower waveform shows the output ripple voltage filtered by an additional LC filter.

## Heatsinking and Thermal Considerations The Through-Hole Package TO-220

The LM2575 is available in two packages, a $5-$ pin TO-220(T, TV) and a 5 -pin surface mount $\mathrm{D}^{2} \mathrm{PAK}(\mathrm{D} 2 \mathrm{~T})$. There are many applications that require no heatsink to keep the LM2575 junction temperature within the allowed operating range. The TO-220 package can be used without a heatsink for ambient temperatures up to approximately $50^{\circ} \mathrm{C}$ (depending on the output voltage and load current). Higher ambient temperatures require some heatsinking, either to the printed circuit (PC) board or an external heatsink.

## The Surface Mount Package D²PAK and its Heatsinking

The other type of package, the surface mount $\mathrm{D}^{2} \mathrm{PAK}$, is designed to be soldered to the copper on the PC board. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least $0.4 \mathrm{in}^{2}$ (or $100 \mathrm{~mm}^{2}$ ) and ideally should have 2 or more square inches ( $1300 \mathrm{~mm}^{2}$ ) of 0.0028 inch copper. Additional increasing of copper area beyond approximately $3.0 \mathrm{in}^{2}\left(2000 \mathrm{~mm}^{2}\right)$ will not improve heat dissipation significantly. If further thermal improvements are needed, double sided or multilayer PC boards with large copper areas should be considered.

## Thermal Analysis and Design

The following procedure must be performed to determine whether or not a heatsink will be required. First determine:

1. $\mathrm{P}_{\mathrm{D}(\max )}$ maximum regulator power dissipation in the application.
2. $\mathrm{T}_{\mathrm{A}(\max )}$ maximum ambient temperature in the application.
3. $\mathrm{T}_{\mathrm{J}(\max )}$ maximum allowed junction temperature $\left(125^{\circ} \mathrm{C}\right.$ for the LM2575). For a conservative design, the maximum junction temperature should not exceed $110^{\circ} \mathrm{C}$ to assure safe operation. For every additional $10^{\circ} \mathrm{C}$ temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $\mathrm{R}_{\theta \mathrm{JC}}$ package thermal resistance junction-case. 5. $\mathrm{R}_{\theta \mathrm{JA}}$ package thermal resistance junction-ambient. (Refer to Absolute Maximum Ratings in this data sheet or $R_{\theta J C}$ and $R_{\theta J \mathrm{~A}}$ values).

The following formula is to calculate the total power dissipated by the LM2575:

$$
P_{D}=\left(V_{\text {in }} \times I_{Q}\right)+d \times I_{\text {Load }} \times V_{\text {sat }}
$$

where $d$ is the duty cycle and for buck converter

$$
\mathrm{d}=\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{~T}}=\frac{\mathrm{V}_{\mathrm{O}}}{\mathrm{~V}_{\mathrm{in}}}
$$

$\mathrm{I}_{\mathrm{Q}} \quad$ (quiescent current) and $\mathrm{V}_{\text {sat }}$ can be found in the LM2575 data sheet,
$\mathrm{V}_{\text {in }}$ is minimum input voltage applied,
$\mathrm{V}_{\mathrm{O}}$ is the regulator output voltage,
$\mathrm{I}_{\text {Load }}$ is the load current.
The dynamic switching losses during turn-on and turn-off can be neglected if proper type catch diode is used.

## Packages Not on a Heatsink (Free-Standing)

For a free-standing application when no heatsink is used, the junction temperature can be determined by the following expression:

$$
T_{J}=\left(R_{\theta J A}\right)\left(P_{D}\right)+T_{A}
$$

where $\left(R_{\theta J A}\right)\left(P_{D}\right)$ represents the junction temperature rise caused by the dissipated power and $\mathrm{T}_{\mathrm{A}}$ is the maximum ambient temperature.

## Packages on a Heatsink

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, than a heatsink is required. The junction temperature will be calculated as follows:

$$
T_{J}=P_{D}\left(R_{\theta J A}+R_{\theta C S}+R_{\theta S A}\right)+T_{A}
$$

where $\quad R_{\theta J C}$ is the thermal resistance junction-case, $\mathrm{R}_{\theta C S}$ is the thermal resistance case-heatsink, $\mathrm{R}_{\theta \mathrm{SA}}$ is the thermal resistance heatsink-ambient.
If the actual operating temperature is greater than the selected safe operating junction temperature, then a larger heatsink is required.

## Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still.
Other factors are trace width, total printed circuit copper area, copper thickness, single- or double-sided, multilayer board, the amount of solder on the board or even color of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat.


Figure 25. Inverting Buck-Boost Regulator Using the LM2575-12 Develops -12 V @ 0.35 A

## ADDITIONAL APPLICATIONS

## Inverting Regulator

An inverting buck-boost regulator using the LM2575-12 is shown in Figure 25. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2575-12 is used to generate a -12 V output. The maximum input voltage in this case cannot exceed +28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V .

This circuit configuration is able to deliver approximately 0.35 A to the output when the input voltage is 12 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V , because the buck-boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.
Since the switch currents in this buck-boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck-boost inverting regulator can also require a larger amount of startup input current, even for light loads. This may overload an input power source with a current limit less than 1.5 A .

Such an amount of input startup current is needed for at least 2.0 ms or more. The actual time depends on the output voltage and size of the output capacitor.
Because of the relatively high startup currents required by this inverting regulator topology, the use of a delayed startup or an undervoltage lockout circuit is recommended.

Using a delayed startup arrangement, the input capacitor can charge up to a higher voltage before the switch-mode regulator begins to operate.

The high input current needed for startup is now partially supplied by the input capacitor $\mathrm{C}_{\mathrm{in}}$.

## Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L1 or the output capacitor $\mathrm{C}_{\text {out }}$.

The output capacitor values must be larger than is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of $\mu \mathrm{F}$ ).

The recommended range of inductor values for the inverting converter design is between $68 \mu \mathrm{H}$ and $220 \mu \mathrm{H}$. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

The following formula is used to obtain the peak inductor current:

$$
\begin{gathered}
\mathrm{I}_{\text {peak }} \approx \frac{\mathrm{I}_{\mathrm{Load}}\left(\mathrm{~V}_{\text {in }}+\left|\mathrm{V}_{\mathrm{O}}\right|\right)}{\mathrm{V}_{\text {in }}}+\frac{\mathrm{V}_{\text {in }} \times \mathrm{t}_{\mathrm{on}}}{2 \mathrm{~L}_{1}} \\
\text { where } \mathrm{t}_{\mathrm{on}}=\frac{\left|\mathrm{V}_{\mathrm{O}}\right|}{\mathrm{V}_{\mathrm{in}}+\left|\mathrm{V}_{\mathrm{O}}\right|} \times \frac{1}{f_{\mathrm{osc}}}, \text { and } \mathrm{f}_{\mathrm{osc}}=52 \mathrm{kHz} .
\end{gathered}
$$

Under normal continuous inductor current operating conditions, the worst case occurs when $\mathrm{V}_{\mathrm{in}}$ is minimal.

Note that the voltage appearing across the regulator is the absolute sum of the input and output voltage, and must not exceed 40 V .


Figure 26. Inverting Buck-Boost Regulator with Delayed Startup

It has been already mentioned above, that in some situations, the delayed startup or the undervoltage lockout features could be very useful. A delayed startup circuit applied to a buck-boost converter is shown in Figure 26. Figure 32 in the "Undervoltage Lockout" section describes an undervoltage lockout feature for the same converter topology.


NOTE: This picture does not show the complete circuit.
Figure 27. Inverting Buck-Boost Regulator Shut Down Circuit Using an Optocoupler

With the inverting configuration, the use of the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin threshold voltage (1.4 V approximately) has to be related to the negative output voltage level. There are many different possible shut down methods, two of them are shown in Figures 27 and 28.


NOTE: This picture does not show the complete circuit.
Figure 28. Inverting Buck-Boost Regulator Shut Down Circuit Using a PNP Transistor

## Negative Boost Regulator

This example is a variation of the buck-boost topology and is called a negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.
The circuit in Figure 29 shows the negative boost configuration. The input voltage in this application ranges from -5.0 V to -12 V and provides a regulated -12 V output.

If the input voltage is greater than -12 V , the output will rise above -12 V accordingly, but will not damage the regulator.


Figure 29. Negative Boost Regulator

## Design Recommendations:

The same design rules as for the previous inverting buck-boost converter can be applied. The output capacitor $\mathrm{C}_{\text {out }}$ must be chosen larger than would be required for a standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of $\mu \mathrm{F}$ ). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

Another important point is that these negative boost converters cannot provide current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

## Delayed Startup

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of startup current. In such cases, if the input power source is limited, this delayed startup feature becomes very useful.

To provide a time delay between the time the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 30 can be used. As the input voltage is applied, the capacitor C 1 charges up, and the voltage across the resistor R 2 falls down. When the voltage on the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin falls below the threshold value 1.4 V , the regulator starts up. Resistor R1 is included to limit the maximum voltage applied to the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin, reduces the power supply noise sensitivity, and also limits the capacitor C1 discharge current, but its use is not mandatory.

When a high 50 Hz or $60 \mathrm{~Hz}(100 \mathrm{~Hz}$ or 120 Hz respectively) ripple voltage exists, a long delay time can
cause some problems by coupling the ripple into the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin, the regulator could be switched periodically on and off with the line (or double) frequency.


NOTE: This picture does not show the complete circuit.
Figure 30. Delayed Startup Circuitry

## Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 31 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck-boost converter is shown in Figure 32. Resistor R3 pulls the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level, which is determined by the following expression:

$$
\mathrm{v}_{\mathrm{th}} \approx \mathrm{~V}_{\mathrm{Z} 1}+\left(1+\frac{\mathrm{R} 2}{\mathrm{R} 1}\right) \mathrm{v}_{\mathrm{BE}}(\mathrm{Q} 1)
$$



NOTE: This picture does not show the complete circuit.
Figure 31. Undervoltage Lockout Circuit for Buck Converter

## LM2575



NOTE: This picture does not show the complete circuit.
Figure 32. Undervoltage Lockout Circuit for Buck-Boost Converter

## Adjustable Output, Low-Ripple Power Supply

A 1.0 A output current capability power supply that features an adjustable output voltage is shown in Figure 33.
This regulator delivers 1.0 A into 1.2 V to 35 V output. The input voltage ranges from roughly 8.0 V to 40 V . In order to achieve a 10 or more times reduction of output ripple, an additional $\mathrm{L}-\mathrm{C}$ filter is included in this circuit.


Figure 33. Adjustable Power Supply with Low Ripple Voltage


Figure 34. D2PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

THE LM2575-5.0 STEP-DOWN VOLTAGE REGULATOR WITH 5.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT


Figure 35. Schematic Diagram of the LM2575-5.0 Step-Down Converter


NOTE: Not to scale.
Figure 36. Printed Circuit Board Component Side


NOTE: Not to scale.
Figure 37. Printed Circuit Board Copper Side

THE LM2575-ADJ STEP-DOWN VOLTAGE REGULATOR WITH 8.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT


Figure 38. Schematic Diagram of the 8.0 V @ 1.0 V Step-Down Converter Using the LM2575-Adj
(An additional LC filter is included to achieve low output ripple voltage)


NOTE: Not to scale.
Figure 39. PC Board Component Side


NOTE: Not to scale.
Figure 40. PC Board Copper Side

## References

- National Semiconductor LM2575 Data Sheet and Application Note
- National Semiconductor LM2595 Data Sheet and Application Note
- Marty Brown "Practical Switching Power Supply Design", Academic Press, Inc., San Diego 1990
- Ray Ridley "High Frequency Magnetics Design", Ridley Engineering, Inc. 1995


## LM2575

ORDERING INFORMATION

| Device | Nominal Output Voltage | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| LM2575TV-ADJ | 1.23 V to 37 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-220 (Vertical Mount) | 50 Units/Rail |
| LM2575T-ADJ |  |  | TO-220 (Straight Lead) |  |
| LM2575D2T-ADJ |  |  | $\mathrm{D}^{2}$ PAK (Surface Mount) |  |
| LM2575D2T-ADJR4 |  |  | D²PAK (Surface Mount) |  |
| LM2575TV-3.3 | 3.3 V |  | TO-220 (Vertical Mount) |  |
| LM2575T-3.3 |  |  | TO-220 (Straight Lead) |  |
| LM2575D2T-3.3 |  |  | D²PAK (Surface Mount) |  |
| LM2575D2T-3.3R4 |  |  | D2PAK (Surface Mount) |  |
| LM2575TV-5 | 5.0 V |  | TO-220 (Vertical Mount) |  |
| LM2575T-5 |  |  | TO-220 (Straight Lead) |  |
| LM2575D2T-5 |  |  | D²PAK (Surface Mount) |  |
| LM2575D2T-5R4 |  |  | D²PAK (Surface Mount) | 800 Tape \& Reel |
| LM2575TV-12 |  |  | TO-220 (Vertical Mount) | 50 Units/Rail |
| LM2575T-12 |  |  | TO-220 (Straight Lead) |  |
| LM2575D2T-12 |  |  | D2PAK (Surface Mount) |  |
| LM2575D2T-12R4 |  |  | D2PAK (Surface Mount) |  |
| LM2575TV-15 | 15 V |  | TO-220 (Vertical Mount) |  |
| LM2575T-15 |  |  | TO-220 (Straight Lead) |  |
| LM2575D2T-15 |  |  | D²PAK (Surface Mount) |  |
| LM2575D2T-15R4 |  |  | D2PAK (Surface Mount) |  |

## MARKING DIAGRAMS



[^28]
## LM2576

### 3.0 A, 15 V, Step-Down Switching Regulator

The LM2576 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step-down switching regulator (buck converter). All circuits of this series are capable of driving a 3.0 A load with excellent line and load regulation. These devices are available in fixed output voltages of $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, $12 \mathrm{~V}, 15 \mathrm{~V}$, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimized for use with the LM2576 are offered by several different inductor manufacturers.

Since the LM2576 converter is a switch-mode power supply, its efficiency is significantly higher in comparison with popular three-terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated is so low that no heatsink is required or its size could be reduced dramatically.

A standard series of inductors optimized for use with the LM2576 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

The LM2576 features include a guaranteed $\pm 4 \%$ tolerance on output voltage within specified input voltages and output load conditions, and $\pm 10 \%$ on the oscillator frequency ( $\pm 2 \%$ over $0^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ ). External shutdown is included, featuring $80 \mu \mathrm{~A}$ (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

## Features

- 3.3 V, 5.0 V, $12 \mathrm{~V}, 15 \mathrm{~V}$, and Adjustable Output Versions
- Adjustable Version Output Voltage Range, 1.23 to $37 \mathrm{~V} \pm 4 \%$ Maximum Over Line and Load Conditions
- Guaranteed 3.0 A Output Current
- Wide Input Voltage Range
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- Moisture Sensitivity Level (MSL) Equals 1


## Applications

- Simple High-Efficiency Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converter (Buck-Boost)
- Negative Step-Up Converters
- Power Supply for Battery Chargers

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


Heatsink surface connected to Pin 3


Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1349 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 1349 of this data sheet.

## LM2576

Typical Application (Fixed Output Voltage Versions)


Figure 1. Block Diagram and Typical Application

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Maximum Supply Voltage | $V_{\text {in }}$ | 45 | V |
| ON/OFF Pin Input Voltage | - | $-0.3 \mathrm{~V} \leq \mathrm{V} \leq+\mathrm{V}_{\text {in }}$ | V |
| Output Voltage to Ground (Steady-State) | - | -1.0 | V |
| Power Dissipation <br> Case 314B and 314D (TO-220, 5-Lead) <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case <br> Case 936A ( $D^{2}$ PAK) <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | Internally Limited 65 5.0 Internally Limited 70 5.0 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Minimum ESD Rating (Human Body Model: $\mathrm{C}=100 \mathrm{pF}, \mathrm{R}=1.5 \mathrm{k} \Omega)$ | - | 2.0 | kV |
| Lead Temperature (Soldering, 10 seconds) | - | 260 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | TJ | 150 | ${ }^{\circ} \mathrm{C}$ |

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Supply Voltage | $\mathrm{V}_{\text {in }}$ | 40 | V |

## SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 15)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $\mathrm{V}_{\text {in }}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, and Adjustable version, $\mathrm{V}_{\text {in }}=25 \mathrm{~V}$ for the 12 V version, and $\mathrm{V}_{\text {in }}=30 \mathrm{~V}$ for the 15 V version. $\mathrm{I}_{\text {Load }}=500 \mathrm{~mA}$. For typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{J}$ is the operating junction temperature range that applies [Note 2], unless otherwise noted.)
Characteristics

|  | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| LM2576-3.3 ([Note 1] Test Circuit Figure 15) |  |  |  |  |  |
| Output Voltage $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 3.234 | 3.3 | 3.366 | V |
| Output Voltage $\left(6.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.5 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 3.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 3.168 | 3.3 | 3.432 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 3.135 | - | 3.465 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=3.0 \mathrm{~A}\right)$ | $\eta$ | - | 75 | - | $\%$ |

LM2576-5 ([Note 1] Test Circuit Figure 15)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 4.9 | 5.0 | 5.1 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(8.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.5 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 3.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 4.8 | 5.0 | 5.2 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 4.75 | - | 5.25 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=3.0 \mathrm{~A}\right)$ | $\eta$ | - | 77 | - | $\%$ |

LM2576-12 ([Note 1] Test Circuit Figure 15)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 11.76 | 12 | 12.24 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(15 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.5 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 3.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 11.52 | 12 | 12.48 |  |
| $\mathrm{~T}_{\mathrm{J}}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 11.4 | - | 12.6 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=15 \mathrm{~V}, \mathrm{I}_{\text {Load }}=3.0 \mathrm{~A}\right)$ | $\eta$ | - | 88 | - | $\%$ |

LM2576-15 ([Note 1] Test Circuit Figure 15)

| Output Voltage $\left(\mathrm{V}_{\text {in }}=30 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 14.7 | 15 | 15.3 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage $\left(18 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.5 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 3.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 14.4 | 15 | 15.6 |  |
| $\mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 14.25 | - | 15.75 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=18 \mathrm{~V}, \mathrm{I}_{\text {Load }}=3.0 \mathrm{~A}\right)$ | $\eta$ | - | 88 | - | $\%$ |

LM2576 ADJUSTABLE VERSION ([Note 1] Test Circuit Figure 15)

| Feedback Voltage $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=0.5 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {out }}$ | 1.217 | 1.23 | 1.243 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Feedback Voltage $\left(8.0 \mathrm{~V} \leq \mathrm{V}_{\text {in }} \leq 40 \mathrm{~V}, 0.5 \mathrm{~A} \leq \mathrm{I}_{\text {Load }} \leq 3.0 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {out }}$ |  |  |  | V |
| $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  | 1.193 | 1.23 | 1.267 |  |
| $\mathrm{~T}_{J}=-40$ to $+125^{\circ} \mathrm{C}$ |  | 1.18 | - | 1.28 |  |
| Efficiency $\left(\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\text {Load }}=3.0 \mathrm{~A}, \mathrm{~V}_{\text {out }}=5.0 \mathrm{~V}\right)$ | $\eta$ | - | 77 | - | $\%$ |

1. External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576 is used as shown in the Figure 15 test circuit, system performance will be as shown in system parameters section.
2. Tested junction temperature range for the LM2576: $\quad T_{\text {low }}=-40^{\circ} \mathrm{C} \quad \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$

## DEVICE PARAMETERS

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $\mathrm{V}_{\text {in }}=12 \mathrm{~V}$ for the $3.3 \mathrm{~V}, 5.0 \mathrm{~V}$, and Adjustable version, $\mathrm{V}_{\text {in }}=25 \mathrm{~V}$ for the 12 V version, and $\mathrm{V}_{\text {in }}=30 \mathrm{~V}$ for the 15 V version. $\mathrm{I}_{\text {Load }}=500 \mathrm{~mA}$. For typical values $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{J}$ is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

ALL OUTPUT VOLTAGE VERSIONS

| $\begin{aligned} & \text { Feedback Bias Current (Vout }=5.0 \mathrm{~V} \text { [Adjustable Version Only] }) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{Ib}_{\mathrm{b}}$ | - | 25 | $\begin{aligned} & 100 \\ & 200 \end{aligned}$ | nA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillator Frequency [Note 3] $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=0 \text { to }+125^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $\mathrm{f}_{\text {osc }}$ | $\begin{aligned} & 47 \\ & 42 \end{aligned}$ | 52 | $\begin{aligned} & 58 \\ & 63 \end{aligned}$ | kHz |
| $\begin{aligned} & \text { Saturation Voltage ( } \text { lout }=3.0 \mathrm{~A}[\text { Note } 4] \text { ) } \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {sat }}$ | - | 1.5 | $\begin{aligned} & 1.8 \\ & 2.0 \end{aligned}$ | V |
| Max Duty Cycle ("on") [Note 5] | DC | 94 | 98 | - | \% |
| Current Limit (Peak Current [Notes 3 and 4]) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | ICL | 4.2 3.5 | 5.8 | $\begin{aligned} & 6.9 \\ & 7.5 \end{aligned}$ | A |
| Output Leakage Current [Notes 6 and 7 ], $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ $\begin{aligned} & \text { Output }=0 \mathrm{~V} \\ & \text { Output }=-1.0 \mathrm{~V} \end{aligned}$ | $l_{L}$ | - |  | $\begin{aligned} & 2.0 \\ & 20 \end{aligned}$ | mA |
| Quiescent Current [Note 6] $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\mathrm{Q}}$ | - | 5.0 | $\begin{gathered} 9.0 \\ 11 \end{gathered}$ | mA |
| Standby Quiescent Current (ON/OFF Pin =5.0 V ("off")) $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\text {stby }}$ | - | 80 | $\begin{aligned} & 200 \\ & 400 \end{aligned}$ | $\mu \mathrm{A}$ |
| ON/OFF Pin Logic Input Level (Test Circuit Figure 15) $\begin{aligned} \mathrm{V}_{\text {out }} & =0 \mathrm{~V} \\ \mathrm{~T}_{J} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J} & =-40 \text { to }+125^{\circ} \mathrm{C} \\ \mathrm{~V}_{\text {out }} & =\text { Nominal Output Voltage } \\ \mathrm{T}_{J} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{J} & =-40 \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{IH}}$ $\mathrm{V}_{\mathrm{IL}}$ | $\begin{aligned} & 2.2 \\ & 2.4 \end{aligned}$ | 1.4 - 1.2 | $\begin{aligned} & - \\ & \\ & 1.0 \\ & 0.8 \end{aligned}$ | V |
| ON/OFF Pin Input Current (Test Circuit Figure 15) ON/OFF Pin =5.0 V ("off"), $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ $\overline{\mathrm{ON}} / \mathrm{OFF}$ Pin $=0 \mathrm{~V}$ ("on"), $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\begin{aligned} & I_{I H} \\ & I_{I L} \end{aligned}$ | - | 15 0 | $\begin{aligned} & 30 \\ & 5.0 \end{aligned}$ | $\mu \mathrm{A}$ |

3. The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately $40 \%$ from the nominal output voltage. This self protection feature lowers the average dissipation of the IC by lowering the minimum duty cycle from $5 \%$ down to approximately $2 \%$.
4. Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to output pin.
5. Feedback (Pin 4) removed from output and connected to 0 V .
6. Feedback (Pin 4) removed from output and connected to +12 V for the Adjustable, 3.3 V , and 5.0 V versions, and +25 V for the 12 V and 15 V versions, to force the output transistor "off".
7. $\mathrm{V}_{\mathrm{in}}=40 \mathrm{~V}$.

## LM2576

## TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 15)



Figure 2. Normalized Output Voltage


Figure 4. Dropout Voltage


Figure 6. Quiescent Current


Figure 3. Line Regulation


Figure 5. Current Limit


Figure 7. Standby Quiescent Current

## LM2576

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 15)


Figure 8. Standby Quiescent Current


Figure 10. Oscillator Frequency


Figure 9. Switch Saturation Voltage


Figure 11. Minimum Operating Voltage


Figure 12. Feedback Pin Current

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 15)


Figure 13. Switching Waveforms


Figure 14. Load Transient Response

[^29]
## LM2576

Fixed Output Voltage Versions


Figure 15. Typical Test Circuit

## PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 15, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible.

For best results, single-point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 2 (emitter of the internal switch) of the LM2576 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2576 regulator.

PIN FUNCTION DESCRIPTION

| Pin | Symbol | Description (Refer to Figure 1) |
| :---: | :---: | :--- |
| 1 | $\mathrm{~V}_{\text {in }}$ | This pin is the positive input supply for the LM2576 step-down switching regulator. In order to minimize voltage <br> transients and to supply the switching currents needed by the regulator, a suitable input bypass capacitor must be <br> present ( $\mathrm{C}_{\text {in }}$ in Figure 1). |
| 2 | Output | This is the emitter of the internal switch. The saturation voltage $\mathrm{V}_{\text {sat }}$ of this output switch is typically 1.5 V. It should <br> be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to minimize coupling <br> to sensitive circuitry. |
| 3 | Gnd | Circuit ground pin. See the information about the printed circuit board layout. |
| 4 | Feedback | This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the internal resistor <br> divider network R2, R1 and applied to the non-inverting input of the internal error amplifier. In the Adjustable version <br> of the LM2576 switching regulator this pin is the direct input of the error amplifier and the resistor network R2, R1 is <br> connected externally to allow programming of the output voltage. |
| 5 | ON/OFF | It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total input supply <br> current to approximately 80 $\mu \mathrm{A}$. The threshold voltage is typically 1.4 V . Applying a voltage above this value (up to <br> +V $\mathrm{V}_{\text {in }}$ ) shuts the regulator off. If the voltage applied to this pin is lower than 1.4 V or if this pin is left open, the <br> regulator will be in the "on" condition. |

## DESIGN PROCEDURE

## Buck Converter Basics

The LM2576 is a "Buck" or Step-Down Converter which is the most elementary forward-mode converter. Its basic schematic can be seen in Figure 16.

The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$
\mathrm{I}_{\mathrm{L}(\mathrm{on})}=\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \mathrm{t}_{\text {on }}}{\mathrm{L}}
$$

During this "on" period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the "off" period.


Figure 16. Basic Buck Converter
The next period is the "off" period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by the catch diode. The current now flows through the catch diode thus maintaining the load current loop. This removes the stored energy from the inductor. The inductor current during this time is:

$$
\mathrm{I}_{\mathrm{L}(\text { off })}=\frac{\left(\mathrm{V}_{\text {out }}-\mathrm{V}_{\mathrm{D}}\right) \mathrm{t}_{\text {off }}}{\mathrm{L}}
$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

$$
\mathrm{d}=\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{~T}} \text {, where } \mathrm{T} \text { is the period of switching. }
$$

For the buck converter with ideal components, the duty cycle can also be described as:

$$
\mathrm{d}=\frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}}
$$

Figure 17 shows the buck converter, idealized waveforms of the catch diode voltage and the inductor current.


Figure 17. Buck Converter Idealized Waveforms

Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step-by-step design procedure and some examples are provided.

| Procedure |
| :--- |
| Given Parameters: <br> $V_{\text {out }}=$ Regulated Output Voltage $(3.3 \mathrm{~V}, 5.0 \mathrm{~V}, 12 \mathrm{~V}$ or 15 V$)$ <br> $\mathrm{V}_{\text {in(max) }}=$ Maximum Input Voltage <br> $\mathrm{I}_{\text {Load(max) }}=$ Maximum Load Current |
| 1. Controller IC Selection |
| According to the required input voltage, output voltage and |
| current, select the appropriate type of the controller IC output |
| voltage version. |

3. Catch Diode Selection (D1)
A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2576 to be able to withstand a continuous output short
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.
4. Catch Diode Selection (D1)
A. For this example the current rating of the diode is 3.0 A .
B. Use a 20 V 1 N 5820 Schottky diode, or any of the suggested fast recovery diodes shown in Table 1.
5. Inductor Selection (L1)
A. Use the inductor selection guide shown in Figures 19.
B. From the selection guide, the inductance area intersected by the 15 V line and 3.0 A line is L 100 .
C. Inductor value required is $100 \mu \mathrm{H}$. From Table 2, choose an inductor from any of the listed manufacturers.

## LM2576

Procedure (Fixed Output Voltage Version) (continued)In order to simplify the switching regulator design, a step-by-step design procedure and some examples are provided.

| Procedure | Example |
| :---: | :---: |
| 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ ) <br> A. Since the LM2576 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately $1 \%$ of the output voltage) a value between $680 \mu \mathrm{~F}$ and $2000 \mu \mathrm{~F}$ is recommended. <br> B. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8.0 V is appropriate, and a 10 V or 16 V rating is recommended. | 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ ) <br> A. $\mathrm{C}_{\text {out }}=680 \mu \mathrm{~F}$ to $2000 \mu \mathrm{~F}$ standard aluminium electrolytic. <br> B. Capacitor voltage rating $=20 \mathrm{~V}$. |

Procedure (Adjustable Output Version: LM2576-ADJ)

| Procedure |
| :--- |
| Given Parameters: <br> $\mathrm{V}_{\text {out }}=$ Regulated Output Voltage <br> $\mathrm{V}_{\text {in }(\max )}=$ Maximum DC Input Voltage |
| $\mathrm{I}_{\text {Load }(\max )}=$ Maximum Load Current |

Resistor R1 can be between 1.0 k and $5.0 \mathrm{k} \Omega$. (For best temperature coefficient and stability with time, use $1 \%$ metal film resistors).

$$
\mathrm{R} 2=\mathrm{R} 1\left(\frac{\mathrm{~V}_{\text {out }}}{\mathrm{V}_{\text {ref }}}-1.0\right)
$$

## 2. Input Capacitor Selection ( $\mathrm{C}_{\text {in }}$ )

To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+\mathrm{V}_{\text {in }}$ and ground pin Gnd This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value.

For additional information see input capacitor section in the "Application Hints" section of this data sheet.
3. Catch Diode Selection (D1)
A. Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2576 to be able to withstand a continuous output short.
B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.
B. Use a 30 V 1 N 5821 Schottky diode or any suggested fast recovery diode in the Table 1.

Procedure (Adjustable Output Version: LM2576-ADJ) (continued)

| Procedure |
| :--- |
| 4. Inductor Selection (L1) |
| A. Use the following formula to calculate the inducto |
| microsecond $[\mathrm{V} \times \mu \mathrm{s}]$ constant: |
| $E \mathrm{E} \times \mathrm{T}=\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}} \times \frac{10^{6}}{\mathrm{~F}[\mathrm{~Hz}]}[\mathrm{V} \times \mu \mathrm{s}]$ |

B. Match the calculated $\mathrm{E} \times \mathrm{T}$ value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 22. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle.
C. Next step is to identify the inductance region intersected by the $\mathrm{E} \times \mathrm{T}$ value and the maximum load current value on the horizontal axis shown in Figure 25.
D. From the inductor code, identify the inductor value. Then select an appropriate inductor from Table 2.
The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of $1.15 \times \mathrm{I}_{\text {Load }}$. The inductor current rating can also be determined by calculating the inductor peak current:

$$
I_{p(\max )}=I_{\text {Load }(\max )}+\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {out }}\right) \mathrm{t}_{\text {on }}}{2 \mathrm{~L}}
$$

where $t_{o n}$ is the "on" time of the power switch and

$$
t_{\text {on }}=\frac{V_{\text {out }}}{V_{\text {in }}} \times \frac{1.0}{f_{\text {osc }}}
$$

For additional information about the inductor, see the inductor section in the "External Components" section of this data sheet.

## 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ )

A. Since the LM2576 is a forward-mode switching regulator with voltage mode control, its open loop 2-pole-1-zero frequency characteristic has the dominant pole-pair determined by the output capacitor and inductor values.

For stable operation, the capacitor must satisfy the following requirement:

$$
C_{\text {out }} \geq 13,300 \frac{V_{\text {in }(\text { max })}}{V_{\text {out }} \times L[\mu H]}[\mu \mathrm{F}]
$$

B. Capacitor values between $10 \mu \mathrm{~F}$ and $2000 \mu \mathrm{~F}$ will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields.
C. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8.0 V is appropriate, and a 10 V or 16 V rating is recommended.

## Example

4. Inductor Selection (L1)
A. Calculate $\mathrm{E} \times \mathrm{T}[\mathrm{V} \times \mu \mathrm{s}]$ constant:

$$
E \times T=(25-8.0) \times \frac{8.0}{25} \times \frac{1000}{52}=80[V \times \mu \mathrm{s}]
$$

B. $\mathrm{E} \times \mathrm{T}=80[\mathrm{~V} \times \mu \mathrm{s}]$
C. $I_{\text {Load }(\max )}=2.5 \mathrm{~A}$

Inductance Region $=\mathrm{H} 150$
D. Proper inductor value $=150 \mu \mathrm{H}$ Choose the inductor from Table 2.

## 5. Output Capacitor Selection ( $\mathrm{C}_{\text {out }}$ )

A.

$$
C_{\text {out }} \geq 13,300 \times \frac{25}{8 \times 150}=332.5 \mu \mathrm{~F}
$$

To achieve an acceptable ripple voltage, select $\mathrm{C}_{\text {out }}=680 \mu \mathrm{~F}$ electrolytic capacitor.

## LM2576

## LM2576 Series Buck Regulator Design Procedures (continued)

Indicator Value Selection Guide (For Continuous Mode Operation)


Figure 18. LM2576-3.3


Figure 20. LM2576-12


Figure 19. LM2576-5


Figure 21. LM2576-15


Figure 22. LM2576-ADJ

Table 1. Diode Selection Guide

| $\mathrm{V}_{\mathrm{R}}$ | Schottky |  |  |  | Fast Recovery |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 3.0 A |  | 4.0-6.0 A |  | 3.0 A |  | 4.0-6.0 A |  |
|  | Through Hole | Surface Mount | Through Hole | Surface Mount | Through Hole | Surface Mount | Through Hole | Surface Mount |
| 20 V | $\begin{gathered} \text { 1N5820 } \\ \text { MBR320P } \\ \text { SR302 } \end{gathered}$ | SK32 | $\begin{aligned} & \text { 1N5823 } \\ & \text { SR502 } \\ & \text { SB520 } \end{aligned}$ |  | MUR320 <br> 31DF1 <br> HER302 <br> (all diodes <br> rated <br> to at least <br> 100 V ) | MURS320T3 MURD320 30WF10 (all diodes rated to at least 100 V) | MUR420 <br> HER602 <br> (all diodes <br> rated <br> to at least <br> 100 V ) | MURD620CT <br> 50WF10 <br> (all diodes rated to at least 100 V) |
| 30 V | $\begin{gathered} \text { 1N5821 } \\ \text { MBR330 } \\ \text { SR303 } \\ \text { 31DQ03 } \end{gathered}$ | $\begin{gathered} \text { SK33 } \\ \text { 30WQ03 } \end{gathered}$ | 1N5824 <br> SR503 <br> SB530 | 50WQ03 |  |  |  |  |
| 40 V | 1N5822 MBR340 SR304 31DQ04 | $\begin{gathered} \text { SK34 } \\ \text { 30WQ04 } \\ \text { MBRS340T3 } \\ \text { MBRD340 } \end{gathered}$ | $\begin{aligned} & \text { 1N5825 } \\ & \text { SR504 } \\ & \text { SB540 } \end{aligned}$ | $\begin{aligned} & \text { MBRD640CT } \\ & \text { 50WQ04 } \end{aligned}$ |  |  |  |  |
| 50 V | $\begin{gathered} \text { MBR350 } \\ \text { 31DQ05 } \\ \text { SR305 } \end{gathered}$ | $\begin{gathered} \text { SK35 } \\ \text { 30WQ05 } \end{gathered}$ | SB550 | 50WQ05 |  |  |  |  |
| 60 V | $\begin{gathered} \text { MBR360 } \\ \text { DQ06 } \\ \text { SR306 } \end{gathered}$ | MBRS360T3 MBRD360 | 50SQ080 | MBRD660CT |  |  |  |  |

NOTE: Diodes listed in bold are available from ON Semiconductor.

Table 2. Inductor Selection by Manufacturer's Part Number

| Inductor Code | Inductor Value | Tech 39 | Schott Corp. | Pulse Eng. | Renco |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L47 | $47 \mu \mathrm{H}$ | 77212 | 67126980 | PE-53112 | RL2442 |
| L68 | $68 \mu \mathrm{H}$ | 77262 | 67126990 | PE-92114 | RL2443 |
| L100 | $100 \mu \mathrm{H}$ | 77312 | 67127000 | PE-92108 | RL2444 |
| L150 | $150 \mu \mathrm{H}$ | 77360 | 67127010 | PE-53113 | RL1954 |
| L220 | $220 \mu \mathrm{H}$ | 77408 | 67127020 | PE-52626 | RL1953 |
| L330 | $330 \mu \mathrm{H}$ | 77456 | 67127030 | PE-52627 | RL1952 |
| L470 | $470 \mu \mathrm{H}$ | * | 67127040 | PE-53114 | RL1951 |
| L680 | $680 \mu \mathrm{H}$ | 77506 | 67127050 | PE-52629 | RL1950 |
| H150 | $150 \mu \mathrm{H}$ | 77362 | 67127060 | PE-53115 | RL2445 |
| H220 | $220 \mu \mathrm{H}$ | 77412 | 67127070 | PE-53116 | RL2446 |
| H330 | $330 \mu \mathrm{H}$ | 77462 | 67127080 | PE-53117 | RL2447 |
| H470 | $470 \mu \mathrm{H}$ | * | 67127090 | PE-53118 | RL1961 |
| H680 | $680 \mu \mathrm{H}$ | 77508 | 67127100 | PE-53119 | RL1960 |
| H1000 | $1000 \mu \mathrm{H}$ | 77556 | 67127110 | PE-53120 | RL1959 |
| H1500 | $1500 \mu \mathrm{H}$ | * | 67127120 | PE-53121 | RL1958 |
| H2200 | $2200 \mu \mathrm{H}$ | * | 67127130 | PE-53122 | RL2448 |

NOTE: *Contact Manufacturer

Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

| Pulse Engineering, Inc. | Phone <br> Fax | $+1-619-674-8100$ <br> $+1-619-674-8262$ |
| :--- | :--- | :--- |
| Pulse Engineering, Inc. Europe | Phone <br> Fax | $+353-9324-107$ <br> $+353-9324-459$ |
| Renco Electronics, Inc. | Phone <br> Fax | $+1-516-645-5828$ <br> $+1-516-586-5562$ |
| Tech 39 | Phone <br> Fax | $+33-1-4115-1681$ <br> $+33-1-4709-5051$ |
|  | Phone <br> Fax | $+1-612-475-1173$ <br> $+1-612-475-1786$ |

## EXTERNAL COMPONENTS

## Input Capacitor ( $\mathrm{C}_{\text {in }}$ ) <br> The Input Capacitor Should Have a Low ESR

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin, to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below $-25^{\circ} \mathrm{C}$ larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

## RMS Current Rating of $C_{\text {in }}$

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequence of operating an electrolytic capacitor beyond the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$
I_{\mathrm{rms}}>1.2 \times \mathrm{dx} \mathrm{I}_{\text {Load }}
$$

where d is the duty cycle, for a buck regulator

$$
\mathrm{d}=\frac{\mathrm{t}_{\text {on }}}{\mathrm{T}}=\frac{\mathrm{V}_{\text {out }}}{\mathrm{V}_{\text {in }}}
$$

and $d=\frac{t_{\text {on }}}{T}=\frac{\left|V_{\text {out }}\right|}{\left|V_{\text {out }}\right|+V_{\text {in }}}$ for a buck-boost regulator.

## Output Capacitor (Cout)

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak-to-peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value. Standard aluminium electrolytics could be adequate for some applications but for quality design, low ESR types are recommended.
An aluminium electrolytic capacitor's ESR value is related to many factors such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher voltage ratings may be needed to provide low ESR values that, are required for low output ripple voltage.

## The Output Capacitor Requires an ESR Value That Has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically $1 \%$ to $2 \%$ of the output voltage. But if the selected capacitor's ESR is extremely low (below $0.05 \Omega$ ), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

## At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below $-25^{\circ} \mathrm{C}$. The ESR rises dramatically at cold temperatures and typically rises 3 times at $-25^{\circ} \mathrm{C}$ and as much as 10 times at $-40^{\circ} \mathrm{C}$. Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below $-25^{\circ} \mathrm{C}$. They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about $10 \%$ or $20 \%$ of the total capacitance. The output capacitor should have at least $50 \%$ higher RMS ripple current rating at 52 kHz than the peak-to-peak inductor ripple current.

## Catch Diode

## Locate the Catch Diode Close to the LM2576

The LM2576 is a step-down buck converter; it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2576 using short leads and short printed circuit traces to avoid EMI problems.

## Use a Schottky or a Soft Switching Ultra-Fast Recovery Diode

Since the rectifier diodes are very significant sources of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications ( 5.0 V and lower). Another choice could be Fast-Recovery, or Ultra-Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast-recovery diode with soft recovery characteristics can better fulfill some quality, low noise design requirements. Table 1 provides a list of suitable diodes for the LM2576 regulator. Standard $50 / 60 \mathrm{~Hz}$ rectifier diodes, such as the 1N4001 series or 1N5400 series are NOT suitable.

## Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design has a great influence on the reliability of the overall power supply.

Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) problems.

## Continuous and Discontinuous Mode of Operation

The LM2576 step-down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 23 and Figure 24). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output
ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2576 regulator was added to this data sheet (Figures 18 through 22). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 300 mA ) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak-to-peak current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.


Figure 23. Continuous Mode Switching Current Waveforms

## Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the amount of EMI (Electro-Magnetic Interference) shielding that the core must provide. The inductor selection guide covers different styles of inductors, such as pot core, E-core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not contained within the core.

When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E-core (closed magnetic structure) should be used in such applications.

## Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the DC resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2576 internal switch into cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the
inductor and/or the LM2576. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.


HORIZONTAL TIME BASE: $5.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 24. Discontinuous Mode Switching Current Waveforms

## GENERAL RECOMMENDATIONS

## Output Voltage Ripple and Transients Source of the Output Ripple

Since the LM2576 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from $0.5 \%$ to $3 \%$ of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

## Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 25). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimize these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.


Figure 25. Output Ripple Voltage Waveforms

## Minimizing the Output Ripple

In order to minimize the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter ( 20 $\mu \mathrm{H}, 100 \mu \mathrm{~F}$ ), that can be added to the output (see Figure 34) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 25 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 34.

The lower waveform is from the normal unfiltered output of the converter, while the upper waveform shows the output ripple voltage filtered by an additional LC filter.

## Heatsinking and Thermal Considerations The Through-Hole Package TO-220

The LM2576 is available in two packages, a 5-pin TO-220(T, TV) and a 5-pin surface mount D ${ }^{2}$ PAK (D2T). Although the TO-220(T) package needs a heatsink under most conditions, there are some applications that require no heatsink to keep the LM2576 junction temperature within the allowed operating range. Higher ambient temperatures require some heat sinking, either to the printed circuit (PC) board or an external heatsink.

## The Surface Mount Package D²PAK and its Heatsinking

The other type of package, the surface mount $\mathrm{D}^{2} \mathrm{PAK}$, is designed to be soldered to the copper on the PC board. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least $0.4 \mathrm{in}^{2}$ (or $260 \mathrm{~mm}^{2}$ ) and ideally should have 2 or more square inches ( $1300 \mathrm{~mm}^{2}$ ) of 0.0028 inch copper. Additional increases of copper area
beyond approximately $6.0 \mathrm{in}^{2}\left(4000 \mathrm{~mm}^{2}\right)$ will not improve heat dissipation significantly. If further thermal improvements are needed, double sided or multilayer PC boards with large copper areas should be considered. In order to achieve the best thermal performance, it is highly recommended to use wide copper traces as well as large areas of copper in the printed circuit board layout. The only exception to this is the OUTPUT (switch) pin, which should not have large areas of copper (see page 1333 'PCB Layout Guideline').

## Thermal Analysis and Design

The following procedure must be performed to determine whether or not a heatsink will be required. First determine:

1. $\mathrm{P}_{\mathrm{D}(\max )}$ maximum regulator power dissipation in the application.
2. $\mathrm{T}_{\mathrm{A}(\max )}$ maximum ambient temperature in the application.
3. $\mathrm{T}_{\mathrm{J}(\max )}$ maximum allowed junction temperature $\left(125^{\circ} \mathrm{C}\right.$ for the LM2576). For a conservative design, the maximum junction temperature should not exceed $110^{\circ} \mathrm{C}$ to assure safe operation. For every additional $+10^{\circ} \mathrm{C}$ temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $\mathrm{R}_{\theta \mathrm{JC}}$ package thermal resistance junction-case.
5. $\mathrm{R}_{\theta \mathrm{JA}}$ package thermal resistance junction-ambient.
(Refer to Absolute Maximum Ratings on page 1327 of this data sheet or $R_{\theta J C}$ and $R_{\theta J \mathrm{~A}}$ values).

The following formula is to calculate the approximate total power dissipated by the LM2576:

$$
P_{D}=\left(V_{\text {in }} \times I_{Q}\right)+d \times I_{\text {Load }} \times V_{\text {sat }}
$$

where $d$ is the duty cycle and for buck converter

$$
\mathrm{d}=\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{~T}}=\frac{\mathrm{V}_{\mathrm{O}}}{\mathrm{~V}_{\mathrm{in}}}
$$

$\mathrm{I}_{\mathrm{Q}} \quad$ (quiescent current) and $\mathrm{V}_{\text {sat }}$ can be found in the LM2576 data sheet,
$\mathrm{V}_{\mathrm{in}}$ is minimum input voltage applied,
$\mathrm{V}_{\mathrm{O}}$ is the regulator output voltage,
$\mathrm{I}_{\text {Load }}$ is the load current.
The dynamic switching losses during turn-on and turn-off can be neglected if proper type catch diode is used.

## Packages Not on a Heatsink (Free-Standing)

For a free-standing application when no heatsink is used, the junction temperature can be determined by the following expression:

$$
T_{J}=\left(R_{\theta J A}\right)\left(P_{D}\right)+T_{A}
$$

where $\left(R_{\theta J A}\right)\left(P_{D}\right)$ represents the junction temperature rise caused by the dissipated power and $\mathrm{T}_{\mathrm{A}}$ is the maximum ambient temperature.

## Packages on a Heatsink

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, than a heatsink is required. The junction temperature will be calculated as follows:

$$
T_{J}=P_{D}\left(R_{\theta J A}+R_{\theta C S}+R_{\theta S A}\right)+T_{A}
$$

where $\quad R_{\theta J C}$ is the thermal resistance junction-case, $\mathrm{R}_{\theta C S}$ is the thermal resistance case-heatsink, $\mathrm{R}_{\theta S A}$ is the thermal resistance heatsink-ambient.
If the actual operating temperature is greater than the selected safe operating junction temperature, then a larger heatsink is required.

## Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still.

Other factors are trace width, total printed circuit copper area, copper thickness, single- or double-sided, multilayer board, the amount of solder on the board or even color of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat.


Figure 26. Inverting Buck-Boost Develops -12 V

## ADDITIONAL APPLICATIONS

## Inverting Regulator

An inverting buck-boost regulator using the LM2576-12 is shown in Figure 26. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2576-12 is used to generate a -12 V output. The maximum input voltage in this case cannot exceed +28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V .

This circuit configuration is able to deliver approximately 0.7 A to the output when the input voltage is 12 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V , because the buck-boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck-boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck-boost inverting regulator can also require a larger amount of start-up input current, even for light loads. This may overload an input power source with a current limit less than 5.0 A.

Such an amount of input start-up current is needed for at least 2.0 ms or more. The actual time depends on the output voltage and size of the output capacitor.

Because of the relatively high start-up currents required by this inverting regulator topology, the use of a delayed start-up or an undervoltage lockout circuit is recommended.

Using a delayed start-up arrangement, the input capacitor can charge up to a higher voltage before the switch-mode regulator begins to operate.

The high input current needed for start-up is now partially supplied by the input capacitor $\mathrm{C}_{\mathrm{in}}$.

It has been already mentioned above, that in some situations, the delayed start-up or the undervoltage lockout features could be very useful. A delayed start-up circuit applied to a buck-boost converter is shown in Figure 27, Figure 33 in the "Undervoltage Lockout" section describes an undervoltage lockout feature for the same converter topology.

## Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L1 or the output capacitor $\mathrm{C}_{\text {out }}$.

The output capacitor values must be larger than what is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of $\mu \mathrm{F}$ ).

The recommended range of inductor values for the inverting converter design is between $68 \mu \mathrm{H}$ and $220 \mu \mathrm{H}$. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

The following formula is used to obtain the peak inductor current:

$$
\begin{gathered}
\mathrm{I}_{\text {peak }} \approx \frac{\mathrm{I}_{\text {Load }}\left(\mathrm{V}_{\text {in }}+\left|\mathrm{V}_{\mathrm{O}}\right|\right)}{\mathrm{V}_{\text {in }}}+\frac{\mathrm{V}_{\text {in }} \times \mathrm{t}_{\text {on }}}{2 \mathrm{~L}_{1}} \\
\text { where } \mathrm{t}_{\mathrm{on}}=\frac{\left|\mathrm{V}_{\mathrm{O}}\right|}{\mathrm{V}_{\text {in }}+\left|\mathrm{V}_{\mathrm{O}}\right|} \times \frac{1.0}{f_{\mathrm{osc}}}, \text { and } \mathrm{f}_{\mathrm{osc}}=52 \mathrm{kHz} .
\end{gathered}
$$

Under normal continuous inductor current operating conditions, the worst case occurs when $\mathrm{V}_{\mathrm{in}}$ is minimal.


Figure 27. Inverting Buck-Boost Regulator with Delayed start-up


NOTE: This picture does not show the complete circuit.
Figure 28. Inverting Buck-Boost Regulator Shutdown Circuit Using an Optocoupler

With the inverting configuration, the use of the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin threshold voltage (1.3 V approximately) has to be related to the negative output voltage level. There are many different possible shut down methods, two of them are shown in Figures 28 and 29.


NOTE: This picture does not show the complete circuit.
Figure 29. Inverting Buck-Boost Regulator Shutdown Circuit Using a PNP Transistor

## Negative Boost Regulator

This example is a variation of the buck-boost topology and it is called negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

The circuit in Figure 30 shows the negative boost configuration. The input voltage in this application ranges from -5.0 V to -12 V and provides a regulated -12 V output. If the input voltage is greater than -12 V , the output will rise above -12 V accordingly, but will not damage the regulator.


Figure 30. Negative Boost Regulator

## Design Recommendations:

The same design rules as for the previous inverting buck-boost converter can be applied. The output capacitor $\mathrm{C}_{\text {out }}$ must be chosen larger than would be required for a what standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of $\mu \mathrm{F}$ ). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

Another important point is that these negative boost converters cannot provide current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

## Delayed Start-up

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of start-up current. In such cases, if the input power source is limited, this delayed start-up feature becomes very useful.

To provide a time delay between the time when the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 31 can be used. As the input voltage is applied, the capacitor C 1 charges up, and the voltage across the resistor R2 falls down. When the voltage on the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin falls below the threshold value 1.3 V , the regulator starts up. Resistor R1 is included to limit the maximum voltage applied to the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin. It reduces the power supply noise sensitivity, and also limits the capacitor C1 discharge current, but its use is not mandatory.

When a high 50 Hz or $60 \mathrm{~Hz}(100 \mathrm{~Hz}$ or 120 Hz respectively) ripple voltage exists, a long delay time can cause some problems by coupling the ripple into the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin, the regulator could be switched periodically on and off with the line (or double) frequency.


NOTE: This picture does not show the complete circuit.
Figure 31. Delayed Start-up Circuitry

## Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 32 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck-boost converter is shown in Figure 33. Resistor R3 pulls the $\overline{\mathrm{ON}} / \mathrm{OFF}$ pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level with respect to the ground Pin 3, which is determined by the following expression:

$$
\mathrm{V}_{\mathrm{th}} \approx \mathrm{~V}_{\mathrm{Z} 1}+\left(1.0+\frac{\mathrm{R} 2}{\mathrm{R} 1}\right) \mathrm{V}_{\mathrm{BE}}(\mathrm{Q} 1)
$$



NOTE: This picture does not show the complete circuit.
Figure 32. Undervoltage Lockout Circuit for Buck Converter

The following formula is used to obtain the peak inductor current:

$$
I_{\text {peak }} \approx \frac{I_{\text {Load }}\left(V_{\text {in }}+\left|V_{\mathrm{O}}\right|\right)}{V_{\text {in }}}+\frac{\mathrm{v}_{\text {in }} \times \mathrm{t}_{\text {on }}}{2 \mathrm{~L}_{1}}
$$

where $\mathrm{t}_{\mathrm{on}}=\frac{\left|\mathrm{V}_{\mathrm{O}}\right|}{\mathrm{V}_{\mathrm{in}}+\left|\mathrm{V}_{\mathrm{O}}\right|} \times \frac{1.0}{f_{\text {Osc }}}$, and $\mathrm{f}_{\text {osc }}=52 \mathrm{kHz}$.

Under normal continuous inductor current operating conditions, the worst case occurs when $\mathrm{V}_{\text {in }}$ is minimal.


NOTE: This picture does not show the complete circuit.
Figure 33. Undervoltage Lockout Circuit for Buck-Boost Converter

## Adjustable Output, Low-Ripple Power Supply

A 3.0 A output current capability power supply that features an adjustable output voltage is shown in Figure 34.
This regulator delivers 3.0 A into 1.2 V to 35 V output. The input voltage ranges from roughly 3.0 V to 40 V . In order to achieve a 10 or more times reduction of output ripple, an additional $\mathrm{L}-\mathrm{C}$ filter is included in this circuit.


Figure 34. 1.2 to 35 V Adjustable 3.0 A Power Supply with Low Output Ripple

THE LM2576-5 STEP-DOWN VOLTAGE REGULATOR WITH 5.0 V @ 3.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT


Figure 35. Schematic Diagram of the LM2576-5 Step-Down Converter


NOTE: Not to scale.
Figure 36. Printed Circuit Board Layout Component Side


NOTE: Not to scale.
Figure 37. Printed Circuit Board Layout Copper Side

THE LM2576-ADJ STEP-DOWN VOLTAGE REGULATOR WITH 8.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH-HOLE PC BOARD LAYOUT


Figure 38. Schematic Diagram of the $8.0 \mathrm{~V} @ 3.0 \mathrm{~A}$ Step-Down Converter Using the LM2576-ADJ


## References

- National Semiconductor LM2576 Data Sheet and Application Note
- National Semiconductor LM2595 Data Sheet and Application Note
- Marty Brown "Practical Switching Power Supply Design", Academic Press, Inc., San Diego 1990
- Ray Ridley "High Frequency Magnetics Design", Ridley Engineering, Inc. 1995


## LM2576

ORDERING INFORMATION

| Device | Nominal Output Voltage | Operating <br> Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| LM2576TV-ADJ | 1.23 V to 37 V | $\mathrm{T}_{J}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | TO-220 (Vertical Mount) | 50 Units/Rail |
| LM2576T-ADJ |  |  | TO-220 (Straight Lead) |  |
| LM2576D2T-ADJ |  |  | D²PAK (Surface Mount) |  |
| LM2576D2T-ADJR4 |  |  | D²PAK (Surface Mount) | 2500 Tape \& Reel |
| LM2576TV-3.3 | 3.3 V |  | TO-220 (Vertical Mount) | 50 Units/Rail |
| LM2576T-3.3 |  |  | TO-220 (Straight Lead) |  |
| LM2576D2T-3.3 |  |  | D2PAK (Surface Mount) |  |
| LM2576D2TR4-3.3 |  |  | D2PAK (Surface Mount) | 2500 Tape \& Reel |
| LM2576TV-5 | 5.0 V |  | TO-220 (Vertical Mount) | 50 Units/Rail |
| LM2576T-5 |  |  | TO-220 (Straight Lead) |  |
| LM2576D2T-5 |  |  | D²PAK (Surface Mount) |  |
| LM2576D2TR4-5 |  |  | D2PAK (Surface Mount) | 2500 Tape \& Reel |
| LM2576TV-12 | 12 V |  | TO-220 (Vertical Mount) | 50 Units/Rail |
| LM2576T-12 |  |  | TO-220 (Straight Lead) |  |
| LM2576D2T-12 |  |  | D2PAK (Surface Mount) |  |
| LM2576TV-15 | 15 V |  | TO-220 (Vertical Mount) | 50 Units/Rail |
| LM2576T-15 |  |  | TO-220 (Straight Lead) |  |
| LM2576D2T-15 |  |  | D2PAK (Surface Mount) |  |

## MARKING DIAGRAMS


xxx = 3.3, $5.0,12,15$, or ADJ
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

## CS2001

### 1.2 A Switching Regulator, and 5.0 V , 100 mA Linear Regulator with RESET

The CS2001 is a smart power supply ASIC utilized in automotive airbag systems. It contains a current-mode switching regulator with a 1.2 A on-chip switch and a $5.0 \mathrm{~V}, 100 \mathrm{~mA}$ linear regulator. The linear output capacitor must be $3.3 \mu \mathrm{~F}$ or greater with an ESR in the range of $100 \mathrm{~m} \Omega$ to $1.0 \Omega$. If the ESR of the cap is less than $100 \mathrm{~m} \Omega$, a series resistor must be used. The switcher can be configured in either a boost or flyback topology. The boost topology produces energy reserve voltage VER which is externally adjustable ( 25 V maximum) through the resistor divider connected to the $\mathrm{V}_{\mathrm{FB}}$ pin. In the event of fault conditions that produce $\mathrm{V}_{\mathrm{FB}}$ either open or shorted, the switcher is shut down.

Under normal operating conditions $\left(\mathrm{V}_{\mathrm{BAT}}>8.0 \mathrm{~V}\right)$, the current loading on the linear regulator is directed through $\mathrm{V}_{\text {BAT }}$. A low battery or loss of battery condition switches the supply for the linear regulator from $\mathrm{V}_{\text {BAT }}$ to VER and shuts down the switcher using the ASIC's internal "smartswitch." This switchover feature minimizes the power dissipation in both the linear and switcher output devices and saves the cost of using a larger inductor.

The NERD (No Energy Reserve Detected) pin is a dual function output. If V OUT is not in regulation, it provides a Power On Reset function whose time interval is externally adjustable with the capacitor. This interval can be seen on the RESETB pin, which allows for clean power-up and power-down of the microprocessor. Once $\mathrm{V}_{\text {OUT }}$ is in regulation, the logic level of the NERD output (usually low) indicates to the microprocessor whether or not the VER pin is connected.

A switched-capacitor voltage tripler accepts input voltage VER and produces output voltage $\mathrm{V}_{\mathrm{CHG}}$ (typically VER +8.0 V ). This voltage is used in the system to drive high-side FETs.

This part is capable of withstanding a 50 V peak transient voltage. The linear regulator will not shut down during this event.

## Features

- Linear Regulator $5.0 \mathrm{~V} \pm 2 \%$ @ 100 mA
- Switching Regulator 1.2 A Peak Internal Switch
- Voltage Tripler
- Smart Functions
- Smartswitch
- RESET
- Energy Reserve Status
- Protection
- Overtemperature
- Current Limit
- 50 V Peak Transient Capability
- Internally Fused Leads in SO-20L Package

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS2001YDWF20 | SO-20L | 37 Units/Rail |
| CS2001YDWFR20 | SO-20L | 1000 Tape \& Reel |



Figure 1. Application Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| $V_{\text {BAT }}$ |  | -0.5 to 25 | V |
| VER |  | -0.5 to 25 | V |
| $\mathrm{V}_{\text {OUT }}$ |  | -0.5 to 7.0 | V |
| Digital Input/Output Voltage |  | -0.5 to 7.0 | V |
| Peak Transient Voltage (36 V Load Dump @ 14 V Battery Voltage) |  | 50 | V |
| Storage Temperature Range |  | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Junction to Free Air Thermal Impedance |  | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| ESD Susceptibility (Human Body Model) |  | 4.0 | kV |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{A}}$ |  | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{J}$ |  | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BAT}} \leq 16 \mathrm{~V}, 8.0 \mathrm{~V} \leq \mathrm{VER} \leq 25 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{V}(\mathrm{OUT})} \leq 100 \mathrm{~mA}$,
$\mathrm{T}_{\text {TEST }}=-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Linear Regulator |  |  |  |  |  |
| Output Voltage | Output Driven from VBAT, VER $=25 \mathrm{~V}$ <br> Output Driven from VER, $\mathrm{V}_{\mathrm{BAT}}=0 \mathrm{~V}$ | $\begin{aligned} & 4.9 \\ & 4.9 \end{aligned}$ | - | $\begin{aligned} & 5.1 \\ & 5.1 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Regulator Bias Current (from $\mathrm{V}_{\mathrm{BAT}}$ ) | $\begin{aligned} & \mathrm{I}_{\mathrm{V}(\mathrm{BAT})} @ \mathrm{I}_{\mathrm{V}(\mathrm{OUT})}=-100 \mathrm{~mA}, \\ & \mathrm{SWSD}=4.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=16 \mathrm{~V}, \mathrm{VER}=25 \mathrm{~V} \\ & \mathrm{~T}=-40^{\circ} \mathrm{C} \\ & \mathrm{~T}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}=125^{\circ} \mathrm{C} \end{aligned}$ | - | - | $\begin{aligned} & 8.0 \\ & 7.0 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Regulator Bias Current (from VER) | $\begin{aligned} & \mathrm{I}_{\mathrm{VER}} @ \mathrm{I}_{\mathrm{V}(\mathrm{OUT})}=-100 \mathrm{~mA}, \\ & \mathrm{SWSD}=4.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=0 \mathrm{~V}, \mathrm{VER}=25 \mathrm{~V} \\ & \mathrm{~T}=-40^{\circ} \mathrm{C} \\ & \mathrm{~T}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}=125^{\circ} \mathrm{C} \end{aligned}$ | - | - | $\begin{aligned} & 11 \\ & 9.0 \\ & 8.0 \end{aligned}$ | mA <br> mA <br> mA |
| Dropout Voltage $\mathrm{V}_{\text {BAT }}$ - $\mathrm{V}_{\text {OUT }}$ | $\mathrm{VER}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{V} \text { (OUT) }}=-100 \mathrm{~mA}$ (Probe Only) | - | - | 1.5 | V |
| Dropout Voltage VER - V ${ }_{\text {OUT }}$ | $\mathrm{V}_{\text {BAT }}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{OUT})}=-100 \mathrm{~mA}$ | - | - | 1.5 | V |
| Smart Switch Threshold $V_{B A T}$ to VER | $\mathrm{VER}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{V} \text { (OUT })}=-50 \mathrm{~mA}$ | 6.5 | - | 8.0 | V |
| Smart Switch Threshold Hysteresis | $\mathrm{VER}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{V} \text { (OUT) }}=-50 \mathrm{~mA}$ | 0.5 | - | 1.0 | V |
| $\mathrm{V}_{\text {OUT }}$ Output Noise | $\begin{aligned} \mathrm{V}_{\mathrm{BAT}} & =16 \mathrm{~V}, \mathrm{VER}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{OUT})}=-1.0 \mathrm{~mA}, \\ \mathrm{C} & =10 \mu \mathrm{~F}, \mathrm{ESR} \end{aligned}=0.5 \Omega \mathrm{l}$ | - | - | 0.05 | V |
| Line Regulation | - | - | - | 0.025 | V |
| Load Regulation | - | - | - | 0.025 | V |
| Output Current Limit | - | 120 | - | - | mA |


| Switching Regulator $\quad$ VER $=25 \mathrm{~V}, \mathrm{IV}_{\mathrm{V} \text { (OUT) }}=\mathbf{- 1 . 0 ~ m A}$ |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Switching Frequency | $\mathrm{C}_{\text {PUMP }} 270 \mathrm{pF}, \mathrm{R}_{\text {l(BIAS })}=30.1 \mathrm{k} \Omega$ | 135 | 150 | 165 | kHz |
| Pump Drive Current | $\Delta \mathrm{l}_{\mathrm{V}(\mathrm{BAT})}$ for $0 \mathrm{~A} \leq \mathrm{I}_{\mathrm{V}(\mathrm{SW})} \leq 1.2 \mathrm{~A}$ | - | - | 50 | mA |
| Switch Saturation Voltage | $\mathrm{I}_{\mathrm{V}(\mathrm{SW})}=1.2 \mathrm{~A}$ | - | - | 1.6 | V |
| Output Current Limit | - | 1.2 | - | 2.4 | A |
| $\mathrm{V}_{\mathrm{FB}}$ Regulation | - | 1.238 | 1.27 | 1.303 | V |
| $\mathrm{V}_{\text {FB }}$ Input Current | $\mathrm{V}_{\text {FB }}$ Above Short Low Detection Level | - | - | 1.0 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{FB}}$ Input Shorted Low Detection Level | - | 200 | 250 | 300 | mV |
| Cpump Short Detection Threshold | - | 200 | 250 | 300 | mV |
| Maximum Duty Cycle | - | 80 | - | 95 | \% |
| $\mathrm{V}_{\text {SW }}$ Leakage Current | $\mathrm{I}_{\mathrm{V}(\mathrm{SW})} @ \mathrm{~V}_{\text {SW }}=50 \mathrm{~V}, \mathrm{SWSD}=\mathrm{V}_{\text {OUT }}$ | - | - | 100 | $\mu \mathrm{A}$ |


| Voltage Tripler $\quad \mathrm{V}_{\mathrm{BAT}}=16 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{OUT})}=\mathbf{- 1 . 0 ~ m A , ~} \mathrm{C}_{\text {CHG }}=1.5 \mu \mathrm{~F}$ |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage Clamp $\mathrm{V}_{\mathrm{CHG}}-\mathrm{VER}$ | $\begin{aligned} & \mathrm{VER}=8.0 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{CHG})}=-30 \mu \mathrm{~A} \\ & \mathrm{VER}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{CHG})}=-90 \mu \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 6.25 \\ & 6.25 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.0 \end{aligned}$ | $\begin{aligned} & 13 \\ & 13 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Initial Charge Time | $\begin{aligned} & \mathrm{C}_{\mathrm{CHG}}=0.15 \mu \mathrm{~F}, \mathrm{VER}=8.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CHG}}=14.25 \mathrm{~V} \end{aligned}$ | - | - | 30 | ms |
| Maximum Output Voltage Clamp $V_{\text {CHG }}$ | - | 25 | 32.5 | 40 | V |
| Output Voltage Clamp $\mathrm{V}_{\text {CHG }}$ | $\mathrm{VER}=28 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{CHG})}=0 \mu \mathrm{~A}$ | 25 | 32.5 | 40 | V |
| Short Circuit Path Current Limit VER to $\mathrm{V}_{\mathrm{CHG}}$ | - | - | - | 3.0 | mA |

ELECTRICAL CHARACTERISTICS (continued) $\left(8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BAT}} \leq 16 \mathrm{~V}, 8.0 \mathrm{~V} \leq \mathrm{VER} \leq 25 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{V}(\mathrm{OUT})} \leq 100 \mathrm{~mA}\right.$,
$\mathrm{T}_{\text {TEST }}=-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RESETB OUTPUT | $\mathrm{V}_{\text {BAT }}=0 \mathrm{~V}$ |  |  |  |  |
| High Threshold | $\mathrm{V}_{\text {OUT }}$ Increasing | 4.525 | 4.75 | 4.85 | V |
| Low Threshold | V OUT Decreasing | 4.5 | 4.65 | 4.825 | V |
| Hysteresis | - | 25 | 100 | 200 | mV |
| Output Low Voltage | $\mathrm{V}_{\text {OUT }}=1.0 \mathrm{~V}, \mathrm{I}_{\text {RESETB }}=100 \mu \mathrm{~A}$ <br> $\mathrm{I}_{\text {RESETB }}=1.0 \mathrm{~mA}, \mathrm{~V}_{\text {OUT }}=4.5 \mathrm{~V}$ | - | - | $\begin{aligned} & 0.5 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Pull-Up Resistor | RESETB $=1.0 \mathrm{~V}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |

SWSD Input $\quad \mathrm{V}_{\mathrm{BAT}}=16 \mathrm{~V}, \mathrm{VER}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{OUT})}=\mathbf{- 1 . 0} \mathrm{mA}$

| High Threshold | - | - | - | $0.7 \times \mathrm{V}_{\text {OUT }}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Low Threshold | - | $0.3 \times \mathrm{V}_{\text {OUT }}$ | - | - | V |
| Input Impedance | Referenced to Ground | 10 | 20 | 40 | $\mathrm{k} \Omega$ |

NERD OUTPUT $\quad V_{B A T}=16 \mathrm{~V}, \mathrm{I}_{\mathrm{V}(\mathrm{OUT})}=\mathbf{- 1 . 0} \mathrm{mA}, \mathrm{C}_{\text {NERD }}=0.47 \mu \mathrm{~F}$

| VER Detection Voltage | - | 1.5 | - | 6.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Low Voltage | $I_{\text {NERD }}=1.0 \mathrm{~mA}, \mathrm{~V}_{\text {OUT }}=4.5 \mathrm{~V}$ | - | - | 0.5 | V |
| Pull-Up Current | NERD $=0.5 \mathrm{~V}$ | 30 | 40 | 50 | $\mu \mathrm{~A}$ |
| Power On Delay |  | 6.25 | 8.5 | 11 | ms |
| Clamping Voltage (Low) | VER Present | 1.0 | 1.25 | 1.5 | V |
| Clamping Voltage (High) | VER Not Present | 3.5 | 3.75 | 4.0 | V |

## General

| VER Load Current | $\mathrm{VER}=25 \mathrm{~V}, \mathrm{~V}$ BAT $=16 \mathrm{~V}, \mathrm{IV}(\mathrm{OUT})=-100 \mathrm{~mA}$ |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | $\mathrm{~T}=-40^{\circ} \mathrm{C}$ | - | - | 5.0 | mA |
|  | $\mathrm{~T}=25^{\circ} \mathrm{C}$ | - | - | 5.0 | mA |
|  | $\mathrm{~T}=125^{\circ} \mathrm{C}$ | - | - | 4.0 | mA |
| Thermal Shutdown | (Guaranteed by Design) | 160 | - | 210 | ${ }^{\circ} \mathrm{C}$ |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-20L | PIN SYMBOL | FUNCTION |
| 1 | VER | Energy reserve input. |
| 2 | $V_{\text {BAT }}$ | Battery input. |
| 3 | $V_{F B}$ | Charge PUMP control voltage input. |
| 4 | GND1 | Ground. |
| 5 | GND2 | Ground. |
| 6 | GND3 | Ground. |
| 7 | GND4 | Ground. |
| 8 | $\mathrm{V}_{\text {SW }}$ | Charge PUMP switch collector. |
| 9 | SWSD | Charge PUMP shutdown input. |
| 10 | COMP | Charge PUMP compensation pin. |
| 11 | $\mathrm{C}_{\text {PUMP }}$ | Charge PUMP timing cap input. |
| 12 | $\mathrm{I}_{\text {BIAS }}$ | Reference current resistor pin. |

PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-20L | PIN SYMBOL | FUNCTION |
| 13 | $\mathrm{V}_{\text {CHG }}$ | Switched cap voltage tripler output. |
| 14 | GND5 | Ground. |
| 15 | GND6 | Ground. |
| 16 | GND7 | Ground. |
| 17 | GND8 | Ground. |
| 18 | NERD | No energy reserve detected output. |
| 19 | RESETB | Reset output. |
| 20 | $\mathrm{V}_{\text {OUT }}$ | Linear regulator output. |



Figure 2. Block Diagram

## CIRCUIT DESCRIPTION

Figure 3 is an oscilloscope waveform showing the charge pump collector voltage, collector current and the charge pump timing capacitor during normal operation with $\mathrm{I}_{\mathrm{VER}}=30 \mathrm{~mA}$.


Figure 4 is an oscilloscope waveform showing the voltage tripler output and the energy reserve input during power up.


Figure 4. Startup with $\mathrm{R}_{\mathrm{V}(\mathrm{CHG})}=510 \mathrm{k}$

Figure 3. Typical Operation with $\mathrm{I}_{\mathrm{VER}}=30 \mathrm{~mA}$

PACKAGE THERMAL DATA

| Parameter |  | SO-20L | Unit |
| :--- | :---: | :---: | :---: |
| $\mathrm{R}_{\text {®JC }}$ | Typical | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5111

### 1.4 A Switching Regulator with 5.0 V, 100 mA Linear Regulator with Watchdog, RESET and ENABLE

The CS5111 is a dual output power supply integrated circuit. It contains a $5.0 \mathrm{~V} \pm 2 \%, 100 \mathrm{~mA}$ linear regulator, a watchdog timer, a linear output voltage monitor to provide a Power On Reset (POR) and a 1.4 A current mode PWM switching regulator.

The 5.0 V linear regulator is comprised of an error amplifier, reference, and supervisory functions. It has low internal supply current consumption and provides 1.2 V (typical) dropout voltage at maximum load current.

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal. If a correct watchdog signal is not received within the externally programmable time, a reset signal is issued.

The externally programmable active reset circuit operates correctly for an output voltage $\left(\mathrm{V}_{\mathrm{LIN}}\right)$ as low as 1.0 V . During power up, or if the output voltage shifts below the regulation limit, $\overline{\text { RESET }}$ toggles low and remains low for the duration of the delay after proper output voltage regulation is restored. Additionally a reset pulse is issued if the correct watchdog is not received within the programmed time. Reset pulses continue until the correct watchdog signal is received. The reset pulse width and frequency, as well as the Power On Reset delay, are set by one external RC network.

The current mode PWM switching regulator is comprised of an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator, and a 1.4 A output power switch with anti-saturation control. The switching regulator can be configured in a variety of topologies.

The CS5111 is load dump capable and has protection circuitry which includes overvoltage shutdown, current limit on the linear and switcher outputs, and an overtemperature limiter.

## Features

- Linear Regulator
$-5.0 \mathrm{~V} \pm 2 \%$ @ 100 mA
- Switching Regulator
- 1.4 A Peak Internal Switch
- 120 kHz Maximum Switching Frequency
- 5.0 V to 26 V Operating Supply Range
- Smart Functions
- Watchdog
- $\overline{\text { RESET }}$
- $\overline{\text { ENABLE }}$
- Protection
- Overvoltage
- Overtemperature
- Current Limit
- 54 V Peak Transient Capability
- Internally Fused Leads in SO-24L Package


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5111YDWF24 | SO-24L | 31 Units/Rail |
| CS5111YDWFR24 | SO-24L | 1000 Tape \& Reel |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| Logic Inputs/Outputs (ENABLE, SELECT, WDI, RESET) | -0.3 to $\mathrm{V}_{\mathrm{LIN}}$ | V |
| $V_{\text {LIN }}$ | -0.3 to 10 |  |
| $\mathrm{V}_{\mathrm{IN}}, \mathrm{V}_{\text {REG }}:$ <br> DC Input Voltage Peak Transient Voltage (40 V Load Dump @ $14 \mathrm{~V} \mathrm{~V}_{\mathrm{IN}}$ ) | $\begin{aligned} & -0.3 \text { to } 26 \\ & -0.3 \text { to } 54 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| $\mathrm{V}_{\text {SW }}$ Peak Transient Voltage | 54 | V |
| $\mathrm{C}_{\text {OSC }}, \mathrm{C}_{\text {Delay }}, \mathrm{COMP}$, $\mathrm{V}_{\mathrm{FB} 1}, \mathrm{~V}_{\text {FB2 }}$ | -0.3 to $\mathrm{V}_{\text {LIM }}$ | V |
| Power Dissipation | Internally Limited | - |
| $\mathrm{V}_{\text {LIN }}$ Output Current | Internally Limited | - |
| $V_{\text {SW }}$ Output Current | Internally Limited | - |
| RESET Output Sink Current | 5.0 | mA |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| ESD Susceptibility (Machine Model) | 200 | V |
| Storage Temperature | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $5.0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 26 \mathrm{~V}$ and $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, \mathrm{C}_{\text {OUT }}=100 \mu \mathrm{~F}(\mathrm{ESR} \leq 8.0 \Omega)$,
$C_{\text {Delay }}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{BIAS}}=64.9 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{OSC}}=390 \mathrm{pF}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| General |  |  |  |  |  |
| $I_{\text {IN }}$ Off Current | $6.6 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}, \mathrm{I}_{\text {SW }}=0 \mathrm{~A}$ | - | - | 2.0 | mA |
| $\mathrm{I}_{\mathrm{IN}}$ On Current | $6.6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}, \mathrm{I}_{\text {SW }}=1.4 \mathrm{~A}$ | - | 30 | 70 | mA |
| IREG Current | $\mathrm{I}_{\text {LIN }}=100 \mathrm{~mA}, 6.6 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$ | - | - | 6.0 | mA |
| Thermal Limit | Guaranteed by Design | 160 | - | 210 | ${ }^{\circ} \mathrm{C}$ |

5.0 V Regulator Section

| VIIN Output Voltage | $\begin{aligned} & 6.6 \mathrm{~V} \leq \mathrm{V}_{\text {REG }} \leq 26 \mathrm{~V}, \\ & 1.0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{LIN}} \leq 100 \mathrm{~mA} \end{aligned}$ | 4.9 | 5.0 | 5.1 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\left(\mathrm{V}_{\text {REG }}-\mathrm{V}_{\text {LIN }}\right) @ \mathrm{I}$ LIN $=100 \mathrm{~mA}$ | - | 1.2 | 1.5 | V |
| Overvoltage Shutdown | - | 30 | 34 | 38 | V |
| Line Regulation | $6.6 \mathrm{~V} \leq \mathrm{V}_{\text {REG }} \leq 26 \mathrm{~V}$, $\mathrm{L}_{\text {LIN }}=5.0 \mathrm{~mA}$ | - | 5.0 | 25 | mV |
| Load Regulation | $\mathrm{V}_{\text {REG }}=19 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\text {LIN }} \leq 100 \mathrm{~mA}$ | - | 5.0 | 25 | mV |
| Current Limit | $6.6 \mathrm{~V} \leq \mathrm{V}_{\text {REG }} \leq 26 \mathrm{~V}$ | 120 | - | - | mA |
| DC Ripple Rejection | $14 \mathrm{~V} \leq \mathrm{V}_{\mathrm{REG}} \leq 24 \mathrm{~V}$ | 60 | 75 | - | dB |

RESET Section

| Low Threshold ( $\mathrm{V}_{\text {RTL }}$ ) | $\mathrm{V}_{\text {LIN }}$ Decreasing | 4.05 | 4.25 | 4.45 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High Threshold (VRTH) | $\mathrm{V}_{\text {LIN }}$ Increasing | 4.2 | 4.45 | 4.7 | V |
| Hysteresis | $\mathrm{V}_{\text {RTH }}-\mathrm{V}_{\text {RTL }}$ | 140 | 190 | 240 | mV |
| Active High | $\mathrm{V}_{\text {LIN }}>\mathrm{V}_{\text {RTH }}, \mathrm{I}_{\text {RESET }}=-25 \mu \mathrm{~A}$ | $\mathrm{V}_{\text {LIN }}-0.5$ | - | - | V |
| Active Low | $\mathrm{V}_{\mathrm{LIN}}=1.0 \mathrm{~V}, 10 \mathrm{k} \Omega$ Pull-Up from RESET to $\mathrm{V}_{\mathrm{LIN}}$ $\mathrm{V}_{\text {LIN }}=4.0 \mathrm{~V}, \mathrm{I}_{\text {RESET }}=1.0 \mathrm{~mA}$ |  |  | $\begin{aligned} & 0.4 \\ & 0.7 \end{aligned}$ | V V |
| Delay | Invalid WDI | 6.25 | 8.78 | 11 | ms |
| Power On Delay | $\mathrm{V}_{\text {LIN }}$ Crossing $\mathrm{V}_{\text {RTH }}$ | 6.25 | - | - | ms |

Watchdog Input (WDI)

| VIH | Peak WDI Needed to Activate RESET | - | - | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VIL | - | 0.8 | - | - | V |
| Hysteresis | Note 2 | 25 | 50 | - | mV |
| Pull-Up Resistor | WDI $=0 \mathrm{~V}$ | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| Low Threshold | - | 6.25 | 8.78 | 11 | ms |
| Floating Input Voltage | - | 3.5 | - | - | V |
| WDI Pulse Width | - | - | - | 5.0 | $\mu \mathrm{s}$ |

## Switcher Section

| Minimum Operating Input Voltage | - | - | - | 5.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Switching Frequency | Refer to Figure 5 | 80 | 95 | 110 | kHz |
| Switch Saturation Voltage | $\mathrm{I}_{\mathrm{SW}}=1.4 \mathrm{~A}$ | 0.7 | 1.1 | 1.6 | V |
| Output Current Limit | - | 1.4 | - | 2.5 | A |
| Max Switching Frequency | $\mathrm{V}_{\mathrm{SW}}=7.5 \mathrm{~V}$ with $50 \Omega$ Load, Refer to Figure 5 | 120 | - | - | kHz |

[^30]ELECTRICAL CHARACTERISTICS (continued) ( $5.0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 26 \mathrm{~V}$ and $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{OUT}}=100 \mu \mathrm{~F}(\mathrm{ESR} \leq 8.0 \Omega)$, $C_{\text {Delay }}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{BIAS}}=64.9 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{OSC}}=390 \mathrm{pF}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Switcher Section (continued)

| $\mathrm{V}_{\mathrm{FB} 1}$ Regulation Voltage | - | 1.206 | 1.25 | 1.294 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FB} 2}$ Regulation Voltage | - | 1.206 | 1.25 | 1.294 | V |
| $\mathrm{~V}_{\mathrm{FB} 1}, \mathrm{~V}_{\mathrm{FB} 2}$ Input Current | $\mathrm{V}_{\mathrm{FB} 1}=\mathrm{V}_{\mathrm{FB} 2}=5.0 \mathrm{~V}$ | - | - | 1.0 | $\mu \mathrm{~A}$ |
| Oscillator Charge Current | $\mathrm{C}_{\mathrm{OSC}}=0 \mathrm{~V}$ | 35 | 40 | 45 | $\mu \mathrm{~A}$ |
| Oscillator Discharge Current | $\mathrm{C}_{\mathrm{OSC}}=\mathrm{V} 40$ | 270 | 320 | 370 | $\mu \mathrm{~A}$ |
| $\mathrm{C}_{\text {Delay }}$ Charge Current | $\mathrm{C}_{\mathrm{Delay}}=0 \mathrm{~V}$ | 35 | 40 | 45 | $\mu \mathrm{~A}$ |
| Switcher Max Duty Cycle | $\mathrm{V}_{\mathrm{SW}}=5.0 \mathrm{~V}$ with $50 \Omega$ Load, <br> $\mathrm{V}_{\mathrm{FB} 1}=\mathrm{V}_{\mathrm{FB} 2}=1.0 \mathrm{~V}$ | 72 | 85 | 95 | $\%$ |
| Current Sense Amp Gain | $\mathrm{I}_{\mathrm{SW}}=2.3 \mathrm{~A}$ | - | 7.0 | - | $\mathrm{V} / \mathrm{V}$ |
| Error Amp DC Gain |  | - | - | 67 | - |
| Error Amp Transconductance |  | - | 2700 | - | $\mu \mathrm{A} / \mathrm{V}$ |

## ENABLE Input

| VIL | - | 0.8 | 1.24 | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| VIH | - | - | 1.3 | 2.0 | V |
| Hysteresis | - | - | 60 | - | mV |
| Input Impedance | - | 10 | 20 | 40 | $\mathrm{k} \Omega$ |

## Select Input

| VIL (Selects $\mathrm{V}_{\mathrm{FB} 1}$ ) | $4.9 \leq \mathrm{V}_{\mathrm{LIN}} \leq 5.1$ | 0.8 | 1.25 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{VIH}\left(\right.$ Selects $\left.\mathrm{V}_{\mathrm{FB} 2}\right)$ | $4.9 \leq \mathrm{V}_{\mathrm{LIN}} \leq 5.1$ | - | 1.25 | 2.0 | V |
| SELECT Pull-Up | $\mathrm{SELECT}=0 \mathrm{~V}$ | 10 | 24 | 50 | $\mathrm{k} \Omega$ |
| Floating Input Voltage |  | 3.5 | 4.5 | - | V |

## PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-24L | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{IN}}$ | Supply voltage. |
| 2, 3 | NC | No connection. |
| 4 | $\mathrm{V}_{\text {SW }}$ | Collector of NPN power switch for switching regulator section. |
| 5, 6, 7, 8, 17, 18, 19, 20 | GND | Connected to the heat removing leads. |
| 9 | $\mathrm{V}_{\text {FB1 }}$ | Feedback input voltage 1 (referenced to 1.25 V ). |
| 10 | $\mathrm{V}_{\text {FB2 }}$ | Feedback input voltage 2 (referenced to 1.25 V ). |
| 11 | SELECT | Logic level input that selects either $\mathrm{V}_{\mathrm{FB} 1}$ or $\mathrm{V}_{\mathrm{FB} 2}$. An open selects $\mathrm{V}_{\mathrm{FB} 2}$. Connect to GND to select $\mathrm{V}_{\mathrm{FB} 1}$. |
| 12 | COMP | Output of the transconductance error amplifier. |
| 13 | Cosc | A capacitor connected to GND sets the switching frequency. Refer to Figure 5. |
| 14 | WDI | Watchdog input. Active on falling edge. |
| 15 | $\mathrm{C}_{\text {Delay }}$ | A capacitor connected to GND sets the Power On Reset and Watchdog time. |
| 16 | RESET | RESET output. Active low if $\mathrm{V}_{\text {LIN }}$ is below the regulation limit. If watchdog timeout is reached, a reset pulse train is issued. |

PIN FUNCTION DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| SO-24L | PIN SYMBOL |  |
| 21 | I BIAS | A resistor connected to GND sets internal bias currents as well as the Cosc and <br> C Delay $^{\text {charge currents. }}$ |
| 22 | V LIN | Regulated 5.0 V output from the linear regulator section. |
| 23 | V $_{\text {REG }}$ | Input voltage to the linear regulator and the internal supply circuitry. |
| 24 | ENABLE | Logic level input to shut down the switching regulator. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. 5.0 V Regulator Bias Current vs. Load Current


Figure 4. Switch Saturation Voltage


Figure 3. Supply Current vs. Switch Current


Figure 5. Oscillator Frequency (kHz) vs. $\mathrm{C}_{\text {Osc }}(\mathrm{pF})$, Assuming $\mathrm{R}_{\mathrm{BIAS}}=64.9 \mathrm{k} \Omega$

## CIRCUIT DESCRIPTION



Figure 6. Block Diagram of 5.0 V Linear Regulator Portion of the CS5111

### 5.0 V LINEAR REGULATOR

The 5.0 V linear regulator consists of an error amplifier, bandgap voltage reference, and a composite pass transistor.

The 5.0 V linear regulator circuitry is shown in Figure 6. When an unregulated voltage greater than 6.6 V is applied to the $\mathrm{V}_{\text {REG }}$ input, a 5.0 V regulated DC voltage will be present at $\mathrm{V}_{\mathrm{LIN}}$. For proper operation of the 5.0 V linear regulator, the $\mathrm{I}_{\text {BIAS }}$ lead must have a $64.9 \mathrm{k} \Omega$ pull down resistor to ground. A $100 \mu \mathrm{~F}$ or larger capacitor with an ESR < $8.0 \Omega$ must be connected between $\mathrm{V}_{\text {LIN }}$ and ground. To operate the 5.0 V linear regulator as an independent regulator (i.e. separate from the switching supply), the input voltage must be tied to the $\mathrm{V}_{\text {REG }}$ lead.

As the voltage at the $\mathrm{V}_{\text {REG }}$ input is increased, $\mathrm{Q}_{1}$ is turned on. $\mathrm{Q}_{1}$ provides base drive for $\mathrm{Q}_{2}$ which in turn provides base current for $Q_{3}$. As $Q_{3}$ is turned on, the output voltage, $\mathrm{V}_{\mathrm{LIN}}$, begins to rise as $\mathrm{Q}_{3}$ 's output current charges the output capacitor, CoUT. Once $\mathrm{V}_{\text {LIN }}$ rises to a certain level, the error amplifier becomes biased and provides the appropriate amount of base current to $\mathrm{Q}_{1}$. The error amplifier monitors the scaled output voltage via an internal voltage divider, $\mathrm{R}_{2}$ through $\mathrm{R}_{5}$, and compares it to the bandgap voltage reference. The error amplifier output or error signal is an output current equal to the error amplifier's input differential voltage times the transconductance of the amplifier. Therefore, the error amplifier varies the base current to $Q_{1}$, which provides bias to $Q_{2}$ and $Q_{3}$, based on the difference between the reference voltage and the scaled $\mathrm{V}_{\mathrm{LIN}}$ output voltage.

## CONTROL FUNCTIONS

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal which it expects to see within an externally programmable time (see Figure 7).

The watchdog time is given by:

$$
\text { tWDI }=1.353 \times \text { CDelayRBIAS }^{2}
$$

Using $C_{\text {Delay }}=0.1 \mu \mathrm{~F}$ and $\mathrm{R}_{\text {BIAS }}=64.9 \mathrm{k} \Omega$ gives a time ranging from 6.25 ms to 11 ms assuming ideal components. Based on this, the software must be written so that the watchdog arrives at least every 6.25 ms . In practice, the tolerance of $\mathrm{C}_{\text {Delay }}$ and $\mathrm{R}_{\text {BIAS }}$ must be taken into account when calculating the minimum watchdog time ( $\mathrm{t}_{\mathrm{WDI}}$ ).


Figure 7. Timing Diagram for Normal Regulator Operation

If a correct watchdog signal is not received within the specified time a reset pulse train is issued until the correct watchdog signal is received. The nominal reset signal in this case is a 5 volt square wave with a $50 \%$ duty cycle as shown in Figure 8.


A: Watchdog waiting for low-going transition on WDI B: $\overline{R E S E T}$ stays low for twol time

Figure 8. Timing Diagram When WDI Fails to Appear Within the Preset Time Interval, twDI

The $\overline{\text { RESET }}$ signal frequency is given by:

$$
\mathrm{fRESET}=\frac{1}{2(\mathrm{tWDI})}
$$

The Power On Reset (POR) and low voltage $\overline{\text { RESET }}$ use the same circuitry and issue a reset when the linear output voltage is below the regulation limit. After $\mathrm{V}_{\text {LIN }}$ rises above the minimum specified value, $\overline{\text { RESET }}$ remains low for a fixed period tPOR as shown in Figures 9 and 10.


Figure 9. The Power On Reset Time Interval ( $\mathrm{t}_{\mathrm{POR}}$ ) Begins When VIIN Rises Above 4.45 V (Typical)


Figure 10. RESET Signal Is Issued Whenever $\mathrm{V}_{\text {LIN }}$ Falls Below 4.25 V (Typical)

The POR delay ( $\mathrm{t}_{\mathrm{POR}}$ ) is given by:

$$
\text { tPOR }=1.353 \times \text { CDelayRBIAS }
$$

## CURRENT MODE PWM SWITCHING CIRCUITRY

The current mode PWM switching voltage regulator contains an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator and a 1.4 A output power switch with antisaturation control. The switching regulator and external components, connected in a boost configuration, are shown in Figure 11.

The switching regulator begins operation when $V_{\text {REG }}$ and $\mathrm{V}_{\text {IN }}$ are raised above 5 volts. $\mathrm{V}_{\text {REG }}$ is required since the switching supply's control circuitry is powered through $\mathrm{V}_{\mathrm{LIN}}$. $\mathrm{V}_{\text {IN }}$ supplies the base drive to the switcher output transistor.

The output transistor turns on when the oscillator starts to charge the capacitor on Cosc. The output current will develop a voltage drop across the internal sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$. This voltage drop produces a proportional voltage at the output of the current sense amplifier, which is compared to the output of the error amplifier. The error amplifier generates an output voltage which is proportional to the difference between the scaled down output boost voltage $\left(\mathrm{V}_{\mathrm{FB} 1}\right.$ or $\left.\mathrm{V}_{\mathrm{FB} 2}\right)$ and the internal bandgap voltage reference. Once the current sense amplifier output exceeds the error amplifier's output voltage, the output transistor is turned off.

The energy stored in the inductor during the output transistor on time is transferred to the load when the output transistor is turned off. The output transistor is turned back
on at the next rising edge of the oscillator. On a cycle by cycle basis, the current mode controller in a discontinuous mode of operation charges the inductor to the appropriate amount of energy, based on the energy demand of the load. Figure 12 shows the typical current and voltage waveforms for a boost supply operating in the discontinuous mode.
2. The switching regulator can be disabled by providing a logic high at the $\overline{\text { ENABLE input. }}$
3. The boost output voltage can be controlled dynamically by the feedback select input. If select is open, $\mathrm{V}_{\mathrm{FB} 2}$ is selected. If select is low, then $\mathrm{V}_{\mathrm{FB} 1}$ is selected.

## Notes:

1. Refer to Figure 5 to determine oscillator frequency.


Figure 11. Block Diagram of the 1.4 A Current Mode Control Switching Regulator Portion of the CS5111 in a Boost Configuration


Figure 12. Voltage and Current Waveforms for Boost Topology in CS5111

## PROTECTION CIRCUITRY

If the input voltage at $\mathrm{V}_{\text {REG }}$ is increased above the overvoltage threshold, the drive to the linear and switcher output transistors is shut off. Therefore, $\mathrm{V}_{\text {LIN }}$ is disabled and $\mathrm{V}_{\mathrm{SW}}$ can not be pulled low.

The current out of $\mathrm{V}_{\text {LIN }}$ is sensed in order to limit excessive power dissipation in the linear output transistor over the output range of 0 V to regulation. Also, the current into $\mathrm{V}_{\mathrm{SW}}$ is sensed in order to provide the current limit function in the switcher output transistor.

If the die temperature is increased above $160^{\circ} \mathrm{C}$, either due to excessive ambient temperature or excessive power dissipation, the drive to the linear output transistor is reduced proportionally with increasing die temperature. Therefore, $\mathrm{V}_{\text {LIN }}$ will decrease with increasing die temperature above $160^{\circ} \mathrm{C}$. Since the switcher control circuitry is powered through $\mathrm{V}_{\mathrm{LIN}}$, the switcher performance, including current limit, will be affected by the decrease in $\mathrm{V}_{\text {LIN }}$.

## APPLICATION NOTES

## DESIGN PROCEDURE FOR BOOST TOPOLOGY

This section outlines a procedure for designing a boost switching power supply operating in the discontinuous mode.

## Step 1

Determine the output power required by the load.
POUT = IOUTVOUT

## Step 2

Choose COSC based on the target oscillator frequency with an external resistor value, $\mathrm{R}_{\text {BIAS }}=64.9 \mathrm{k} \Omega$ (See Figure 5).

## Step 3

Next select the output voltage feedback sense resistor divider as follows (Figure 13).

For $\mathrm{V}_{\mathrm{FB} 1}$ active, choose a value for $\mathrm{R}_{1}$ and then solve for $R_{E Q}$ where:

$$
\begin{equation*}
R_{E Q}=\frac{R_{1}}{\frac{V_{O U T}}{V_{F B 1}}-1} \tag{2}
\end{equation*}
$$

For $\mathrm{V}_{\mathrm{FB} 2}$ active, find:

$$
\begin{equation*}
V_{\mathrm{FB} 1}=\operatorname{VOUT}\left(\frac{\mathrm{R}_{\mathrm{EQ}}}{\mathrm{R}_{1}+\mathrm{R}_{\mathrm{EQ}}}\right) \tag{3}
\end{equation*}
$$

and then calculate $\mathrm{R}_{2}$ where:

$$
\begin{equation*}
\mathrm{R}_{2}=\frac{\mathrm{V}_{\mathrm{R} 2}}{\mathrm{I}_{\mathrm{R} 2}}=\frac{\mathrm{V}_{\mathrm{FB} 1}-\mathrm{V}_{\mathrm{FB}} 2}{\mathrm{~V}_{\mathrm{FB} 1} / \mathrm{R}_{\mathrm{EQ}}} \tag{4}
\end{equation*}
$$

Then find $\mathrm{R}_{3}$, where:

$$
\begin{equation*}
R_{3}=R_{E Q}-R_{2} \tag{5}
\end{equation*}
$$



Figure 13. Feedback Sense Resistor Divider Connected Between V

## Step 4

Determine the maximum on time at the minimum oscillator frequency and $\mathrm{V}_{\text {IN }}$. For discontinuous operation, all of the stored energy in the inductor is transferred to the load prior to the next cycle. Since the current through the inductor cannot change instantaneously and the inductance is constant, a volt-second balance exists between the on time and off time. The voltage across the inductor during the on cycle is $\mathrm{V}_{\text {IN }}$ and the voltage across the inductor during the off cycle is $\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}$. Therefore:

$$
\begin{equation*}
\text { VINtON }=(\text { VOUT }- \text { VIN }) \text { tOFF } \tag{6}
\end{equation*}
$$

where the maximum on time is:

## Step 5

Calculate the maximum inductance allowed for discontinuous operation:

$$
\begin{equation*}
\mathrm{L}(\mathrm{MAX})=\frac{\mathrm{f} \mathrm{SW}(\mathrm{MIN}) \mathrm{VIN}^{2}(\mathrm{MIN}) \mathrm{tON}^{2}(\mathrm{MAX})}{2 \mathrm{POUT} / \eta} \tag{8}
\end{equation*}
$$

where $\eta=$ efficiency.
Usually $\eta=0.75$ is a good starting point. The IC's power dissipation should be calculated after the peak current has been determined in Step 6. If the efficiency is less than originally assumed, decrease the efficiency and recalculate the maximum inductance and peak current.

## Step 6

Determine the peak inductor current at the minimum inductance, minimum $\mathrm{V}_{\text {IN }}$ and maximum on time to make sure the inductor current doesn't exceed 1.4 A.

$$
\begin{equation*}
\mathrm{IPK}=\frac{\mathrm{VIN}_{\mathrm{IN}}(\mathrm{MIN}) \mathrm{TON}(\mathrm{MAX})}{\mathrm{L}(\mathrm{MIN})} \tag{9}
\end{equation*}
$$

## Step 7

Determine the minimum output capacitance and maximum ESR based on the allowable output voltage ripple.

$$
\begin{align*}
\operatorname{COUT}(\mathrm{MIN}) & =\frac{\mathrm{IPK}}{8 \mathrm{f} \Delta \mathrm{~V}_{\text {RIPPLE }}}  \tag{10}\\
\mathrm{ESR}(\mathrm{MIN}) & =\frac{\Delta \mathrm{V}_{\text {RIPPLE }}}{\mathrm{IPK}} \tag{11}
\end{align*}
$$

In practice, it is normally necessary to use a larger capacitance value to obtain a low ESR. By placing capacitors in parallel, the equivalent ESR can be reduced.

## Step 8

Compensate the feedback loop to guarantee stability under all operating conditions. To do this, we calculate the modulator gain and the feedback resistor network attenuation and set the gain of the error amplifier so that the overall loop gain is 0 dB at the crossover frequency, $\mathrm{f}_{\mathrm{CO}}$. In addition, the gain slope should be $-20 \mathrm{~dB} /$ decade at the crossover frequency.

The low frequency gain of the modulator (i.e. error amplifier output to output voltage) is:

$$
\begin{equation*}
\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{~V}_{\mathrm{EA}}}=\frac{\mathrm{IPK}(\mathrm{MAX})}{\mathrm{V}_{\mathrm{EA}(\mathrm{MAX})}} \sqrt{\frac{\mathrm{R}_{\mathrm{LOADLf}}}{2}} \tag{12}
\end{equation*}
$$

where:

$$
\operatorname{IPK}(\mathrm{MAX})=\frac{\mathrm{V}_{\mathrm{EA}(\mathrm{MAX}) / \mathrm{GCSA}}}{\mathrm{RS}}=\frac{2.4 \mathrm{~V} / 7}{150 \mathrm{~m} \Omega}=2.3 \mathrm{~A} \text { (13) }
$$

The $\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{EA}}$ transfer function has a pole at:

$$
\begin{equation*}
f_{p}=1 /\left(\pi R_{\text {LOADCOUT }}\right) \tag{14}
\end{equation*}
$$

and a zero due to the output capacitor's ESR at:

$$
\begin{equation*}
f_{Z}=1 /(2 \pi E S R(C O U T)) \tag{15}
\end{equation*}
$$

Since the error amplifier reference voltage is 1.25 V , the output voltage must be divided down or attenuated before being applied to the input of the error amplifier. The feedback resistor divider attenuation is:

$$
\frac{1.25 \mathrm{~V}}{\mathrm{VOUT}}
$$

The error amplifier in the CS5111 is an operational transconductance amplifier (OTA), with a gain given by:
GOTA = gmZOUT
where:

$$
\begin{equation*}
\mathrm{gm}=\frac{\Delta \mathrm{l}_{\mathrm{OUT}}}{\Delta \mathrm{~V}_{\mathrm{IN}}} \tag{17}
\end{equation*}
$$

For the CS5111, gm $=2700 \mu \mathrm{~A} / \mathrm{V}$ typical.
One possible error amplifier compensation scheme is shown in Figure 14. This gives the error amplifier a gain plot as shown in Figure 15.

For the error amplifier gain shown in Figure 15, a low frequency pole is generated by the error amplifier output impedance and $\mathrm{C}_{1}$. This is shown by the line AB with a $-20 \mathrm{~dB} /$ decade slope in Figure 15. The slope changes to zero at point B due to the zero at:

$$
\begin{equation*}
f_{Z}=1 /\left(2 \pi R_{4} C_{1}\right) \tag{18}
\end{equation*}
$$



Figure 14. RC Network Used to Compensate the Error Amplifier (OTA)

A pole at point C :

$$
\begin{equation*}
f_{p}=1 /\left(\pi R_{4} C_{2}\right) \tag{19}
\end{equation*}
$$

offsets the zero set by the ESR of the output capacitors.
An alternative scheme uses a single capacitor as shown in Figure 16 , to roll the gain off at a relatively low frequency.

## Step 9

Finally the watchdog timer period and Power on Reset time is determined by:

$$
\begin{equation*}
\text { tDelay }=1.353 \times \text { CDelay } R_{\text {BIAS }} \tag{20}
\end{equation*}
$$



Figure 15. Bode Plot of Error Amplifier (OTA) Gain and Modulator Gain Added to the Feedback Resistor Divider Attenuation

CS5111


Figure 16. A Typical Application Diagram with External Components Configured in a Boost Topology

## LINEAR REGULATOR OUTPUT CURRENT VS. INPUT VOLTAGE



Figure 17. The Shaded Area Shows the Safe Operating Area of the CS5111 as a Function of $\mathrm{I}_{\mathrm{LIN}}, \mathrm{V}_{\text {REG }}$, and $\Theta_{\mathrm{JA}}$. Refer to Table 4 for Typical Loads and Voltages.

Table 4.

| $\mathbf{V}_{\mathbf{R E G}}(\mathbf{V})$ | $\mathbf{V}_{\mathbf{I N}}(\mathbf{V})$ | $\mathbf{I}_{\text {LIN }}(\mathbf{m A})$ | Linear Power <br> Dissipation $(\mathbf{W})$ | Worst Case Switcher <br> Power Available <br> $\left(\Theta_{\mathbf{J A}}=55^{\circ} \mathbf{C} / \mathbf{W}\right)(\mathbf{W})$ | Worst Case Switcher <br> Power Available <br> $\left(\Theta_{\mathbf{J A}}=\mathbf{3 5} \mathbf{C} / \mathbf{W}\right)(\mathbf{W})$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 20 | 14 | 25 | 0.44 | 0.74 | 1.42 |
| 20 | 14 | 50 | 0.83 | 0.35 | 1.03 |
| 20 | 14 | 75 | 1.22 | ${ }^{*}$ | 0.64 |
| 20 | 14 | 100 | 1.60 | ${ }^{*}$ | 0.26 |
| 25 | 14 | 25 | 0.60 | 0.58 | 1.26 |
| 25 | 14 | 50 | 1.11 | $*$ | 0.75 |
| 25 | 14 | 75 | 1.62 | $*$ | 0.24 |
| 25 | 14 | 100 | 2.14 | $*$ |  |

*Subjecting the CS5111 to these conditions will exceed the maximum total power that the part can handle, thereby forcing it into thermal limit.

PACKAGE THERMAL DATA

| Parameter |  | SO-24L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5112

### 1.4 A Switching Regulator with 5.0 V, 100 mA Linear Regulator with Watchdog, RESET and ENABLE

The CS5112 is a dual output power supply integrated circuit. It contains a $5.0 \mathrm{~V} \pm 2 \%, 100 \mathrm{~mA}$ linear regulator, a watchdog timer, a linear output voltage monitor to provide a Power On Reset (POR) and a 1.4 A current mode PWM switching regulator.

The 5.0 V linear regulator is comprised of an error amplifier, reference, and supervisory functions. It has low internal supply current consumption and provides 1.2 V (typical) dropout voltage at maximum load current.

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal. If a correct watchdog signal is not received within the externally programmable time, a reset signal is issued.

The externally programmable active reset circuit operates correctly for an output voltage $\left(\mathrm{V}_{\mathrm{LIN}}\right)$ as low as 1.0 V . During power up, or if the output voltage shifts below the regulation limit, RESET toggles low and remains low for the duration of the delay after proper output voltage regulation is restored. Additionally a reset pulse is issued if the correct watchdog is not received within the programmed time. Reset pulses continue until the correct watchdog signal is received. The reset pulse width and frequency, as well as the Power On Reset delay, are set by one external RC network.

The current mode PWM switching regulator is comprised of an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator, and a 1.4 A output power switch with anti-saturation control. The switching regulator can be configured in a variety of topologies.

The CS5112 is load dump capable and has protection circuitry which includes current limit on the linear and switcher outputs, and an overtemperature limiter.

## Features

- Linear Regulator
- $5.0 \mathrm{~V} \pm 2 \%$ @ 100 mA
- Switching Regulator
- 1.4 A Peak Internal Switch
- 120 kHz Maximum Switching Frequency
- 5.0 V to 26 V Operating Supply Range
- Smart Functions
- Watchdog
- RESET
- $\overline{\text { ENABLE }}$
- Protection
- Overtemperature
- Current Limit
- Internally Fused Leads in SO-24L Package


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5112YDWF24 | SO-24L | 31 Units/Rail |
| CS5112YDWFR24 | SO-24L | 1000 Tape \& Reel |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| Logic Inputs/Outputs (ENABLE, SELECT, WDI, RESET) | -0.3 to $\mathrm{V}_{\text {LIN }}$ | V |
| $\mathrm{V}_{\text {LIN }}$ | -0.3 to 10 |  |
| $\mathrm{V}_{\mathrm{IN}}, \mathrm{V}_{\text {REG }}:$ <br> DC Input Voltage Peak Transient Voltage ( 26 V Load Dump @ 14 V VIN ) | $\begin{aligned} & -0.3 \text { to } 26 \\ & -0.3 \text { to } 40 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| $\mathrm{V}_{\text {SW }}$ Peak Transient Voltage | 54 | V |
| $\mathrm{C}_{\text {OSC }}, \mathrm{C}_{\text {Delay }}$, COMP, $\mathrm{V}_{\mathrm{FB} 1}, \mathrm{~V}_{\text {FB2 }}$ | -0.3 to $\mathrm{V}_{\text {LIM }}$ | V |
| Power Dissipation | Internally Limited | - |
| $\mathrm{V}_{\text {LIN }}$ Output Current | Internally Limited | - |
| $\mathrm{V}_{\text {SW }}$ Output Current | Internally Limited | - |
| RESET Output Sink Current | 5.0 | mA |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| ESD Susceptibility (Machine Model) | 200 | V |
| Storage Temperature | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(5.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}\right.$ and $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{OUT}}=100 \mu \mathrm{~F}(\mathrm{ESR} \leq 8.0 \Omega)$,
$C_{\text {Delay }}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{BIAS}}=64.9 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{OSC}}=390 \mathrm{pF}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| General |  |  |  |  |  |
| $I_{\text {IN }}$ Off Current | $6.6 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 26 \mathrm{~V}$, $\mathrm{I}_{\text {SW }}=0 \mathrm{~A}$ | - | - | 2.0 | mA |
| $\mathrm{I}_{\mathrm{IN}}$ On Current | $6.6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$, $\mathrm{I}_{\text {SW }}=1.4 \mathrm{~A}$ | - | 30 | 70 | mA |
| $\mathrm{I}_{\text {REG }}$ Current | $\mathrm{I}_{\text {LIN }}=100 \mathrm{~mA}, 6.6 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 26 \mathrm{~V}$ | - | - | 6.0 | mA |
| Thermal Limit | Guaranteed by Design | 160 | - | 210 | ${ }^{\circ} \mathrm{C}$ |

5.0 V Regulator Section

| $\mathrm{V}_{\text {LIN }}$ Output Voltage | $6.6 \mathrm{~V} \leq \mathrm{V}_{\text {REG }} \leq 26 \mathrm{~V}$, <br> $1.0 \mathrm{~mA} \leq \mathrm{I}_{\text {LIN }} \leq 100 \mathrm{~mA}$ | 4.9 | 5.0 | 5.1 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Dropout Voltage | $\left(\mathrm{V}_{\text {REG }}-\mathrm{V}_{\mathrm{LIN}}\right) @ \mathrm{I}_{\mathrm{LIN}}=100 \mathrm{~mA}$ | - | 1.2 | 1.5 | V |
| Line Regulation | $6.6 \mathrm{~V} \leq \mathrm{V}_{\text {REG }} \leq 26 \mathrm{~V}, \mathrm{I}_{\text {LIN }}=5.0 \mathrm{~mA}$ | - | 5.0 | 25 | mV |
| Load Regulation | $\mathrm{V}_{\text {REG }}=19 \mathrm{~V}, 1.0 \mathrm{~mA} \leq \mathrm{I}_{\text {LIN }} \leq 100 \mathrm{~mA}$ | - | 5.0 | 25 | mV |
| Current Limit | $6.6 \mathrm{~V} \leq \mathrm{V}_{\text {REG }} \leq 26 \mathrm{~V}$ | 120 | - | - | mA |
| DC Ripple Rejection | $14 \mathrm{~V} \leq \mathrm{V}_{\text {REG }} \leq 24 \mathrm{~V}$ | 60 | 75 | - | dB |

## RESET Section

| Low Threshold ( $\mathrm{V}_{\text {RTL }}$ ) | $V_{\text {LIN }}$ Decreasing | 4.05 | 4.25 | 4.45 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| High Threshold (VRTH) | $V_{\text {LIN }}$ Increasing | 4.2 | 4.45 | 4.7 | V |
| Hysteresis | $\mathrm{V}_{\text {RTH }}-\mathrm{V}_{\text {RTL }}$ | 140 | 190 | 240 | mV |
| Active High | $\mathrm{V}_{\text {LIN }}>\mathrm{V}_{\text {RTH }}, \mathrm{I}_{\text {RESET }}=-25 \mu \mathrm{~A}$ | $\mathrm{V}_{\mathrm{LIN}}-0.5$ | - | - | V |
| Active Low | $\mathrm{V}_{\mathrm{LIN}}=1.0 \mathrm{~V}, 10 \mathrm{k} \Omega$ Pull-Up from RESET to $\mathrm{V}_{\text {LIN }}$ $\mathrm{V}_{\mathrm{LIN}}=4.0 \mathrm{~V}, \mathrm{I}_{\mathrm{RESET}}=1.0 \mathrm{~mA}$ |  |  | $\begin{aligned} & \hline 0.4 \\ & 0.7 \end{aligned}$ | V <br> V |
| Delay | Invalid WDI | 6.25 | 8.78 | 11 | ms |
| Power On Delay | $V_{\text {LIN }}$ Crossing V ${ }_{\text {RTH }}$ | 6.25 | - | - | ms |

## Watchdog Input (WDI)

| VIH | Peak WDI Needed to Activate RESET | - | - | 2.0 | V |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| VIL |  |  |  |  |  |  |
| Hysteresis | Note 2 | 0.8 | - | - | V |  |
| Pull-Up Resistor | WDI = 0 V | 25 | 50 | - | mV |  |
| Low Threshold |  | - | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| Floating Input Voltage | - | 6.25 | 8.78 | 11 | ms |  |
| WDI Pulse Width | - | - | - | - | V |  |

Switcher Section

| Minimum Operating Input Voltage | - | - | - | 5.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Switching Frequency | Refer to Figure 5 | 80 | 95 | 110 | kHz |
| Switch Saturation Voltage | $\mathrm{I}_{\mathrm{SW}}=1.4 \mathrm{~A}$ | 0.7 | 1.1 | 1.6 | V |
| Output Current Limit | - | 1.4 | - | 2.5 | A |
| Max Switching Frequency | $\mathrm{V}_{\mathrm{SW}}=7.5 \mathrm{~V}$ with $50 \Omega$ Load, Refer to Figure 5 | 120 | - | - | kHz |
| $\mathrm{V}_{\mathrm{FB} 1}$ Regulation Voltage | - | 1.206 | 1.25 | 1.294 | V |

2. Guaranteed by design, not $100 \%$ tested in productions.

## CS5112

ELECTRICAL CHARACTERISTICS (continued) ( $5.0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 26 \mathrm{~V}$ and $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}$, $\mathrm{C}_{\text {OUT }}=100 \mu \mathrm{~F}$ (ESR $\leq 8.0 \Omega$ ), $C_{\text {Delay }}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{BIAS}}=64.9 \mathrm{k} \Omega, \mathrm{C}_{\text {OSC }}=390 \mathrm{pF}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Switcher Section (continued)

| $\mathrm{V}_{\mathrm{FB} 2}$ Regulation Voltage | - | 1.206 | 1.25 | 1.294 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FB} 1}, \mathrm{~V}_{\mathrm{FB} 2}$ Input Current | $\mathrm{V}_{\mathrm{FB} 1}=\mathrm{V}_{\mathrm{FB} 2}=5.0 \mathrm{~V}$ | - | - | 1.0 | $\mu \mathrm{~A}$ |
| Oscillator Charge Current | $\mathrm{C}_{\mathrm{OSC}}=0 \mathrm{~V}$ | 35 | 40 | 45 | $\mu \mathrm{~A}$ |
| Oscillator Discharge Current | $\mathrm{C}_{\mathrm{OSC}}=\mathrm{V} 40$ | 270 | 320 | 370 | $\mu \mathrm{~A}$ |
| $\mathrm{C}_{\text {Delay }}$ Charge Current | $\mathrm{C}_{\mathrm{Delay}}=0 \mathrm{~V}$ | 35 | 40 | 45 | $\mu \mathrm{~A}$ |
| Switcher Max Duty Cycle | $\mathrm{V}_{\mathrm{SW}}=5.0 \mathrm{~V}$ with $50 \Omega$ Load, <br> $\mathrm{V}_{\mathrm{FB} 1}=\mathrm{V}_{\mathrm{FB} 2}=1.0 \mathrm{~V}$ | 72 | 85 | 95 | $\%$ |
| Current Sense Amp Gain | $\mathrm{I}_{\mathrm{SW}}=2.3 \mathrm{~A} \quad-$ | - | 7.0 | - | $\mathrm{V} / \mathrm{V}$ |
| Error Amp DC Gain |  | - | 67 | - | dB |
| Error Amp Transconductance |  | - | 2700 | - | $\mu \mathrm{A} / \mathrm{V}$ |

ENABLE Input

| VIL | - | 0.8 | 1.24 | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| VIH | - | - | 1.3 | 2.0 | V |
| Hysteresis | - | - | 60 | - | mV |
| Input Impedance | - | 10 | 20 | 40 | $\mathrm{k} \Omega$ |

## Select Input

| VIL (Selects $\mathrm{V}_{\mathrm{FB} 1}$ ) | $4.9 \leq \mathrm{V}_{\mathrm{LIN}} \leq 5.1$ | 0.8 | 1.25 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{VIH}\left(\right.$ Selects $\left.\mathrm{V}_{\mathrm{FB} 2}\right)$ | $4.9 \leq \mathrm{V}_{\mathrm{LIN}} \leq 5.1$ | - | 1.25 | 2.0 | V |
| SELECT Pull-Up | $\mathrm{SELECT}=0 \mathrm{~V}$ | 10 | 24 | 50 | $\mathrm{k} \Omega$ |
| Floating Input Voltage |  | 3.5 | 4.5 | - | V |

## PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-24L | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\text {IN }}$ | Supply voltage. |
| 2, 3 | NC | No connection. |
| 4 | $\mathrm{V}_{\text {SW }}$ | Collector of NPN power switch for switching regulator section. |
| 5, 6, 7, 8, 17, 18, 19, 20 | GND | Connected to the heat removing leads. |
| 9 | $\mathrm{V}_{\mathrm{FB} 1}$ | Feedback input voltage 1 (referenced to 1.25 V ). |
| 10 | $\mathrm{V}_{\text {FB2 }}$ | Feedback input voltage 2 (referenced to 1.25 V ). |
| 11 | SELECT | Logic level input that selects either $\mathrm{V}_{\mathrm{FB} 1}$ or $\mathrm{V}_{\mathrm{FB} 2}$. An open selects $\mathrm{V}_{\mathrm{FB} 2}$. Connect to GND to select $\mathrm{V}_{\mathrm{FB} 1}$. |
| 12 | COMP | Output of the transconductance error amplifier. |
| 13 | Cosc | A capacitor connected to GND sets the switching frequency. Refer to Figure 5. |
| 14 | WDI | Watchdog input. Active on falling edge. |
| 15 | $\mathrm{C}_{\text {Delay }}$ | A capacitor connected to GND sets the Power On Reset and Watchdog time. |
| 16 | RESET | RESET output. Active low if $\mathrm{V}_{\text {LIN }}$ is below the regulation limit. If watchdog timeout is reached, a reset pulse train is issued. |
| 21 | $I_{\text {BIAS }}$ | A resistor connected to GND sets internal bias currents as well as the Cosc and $\mathrm{C}_{\text {Delay }}$ charge currents. |

PIN FUNCTION DESCRIPTION (continued)

| PACKAGE PIN \# | FUNCTION |  |
| :---: | :---: | :--- |
| SO-24L |  |  |
| 22 | $V_{\text {LIN }}$ | Regulated 5.0 V output from the linear regulator section. |
| 23 | $\mathrm{~V}_{\text {REG }}$ | Input voltage to the linear regulator and the internal supply circuitry. |
| 24 | ENABLE | Logic level input to shut down the switching regulator. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. 5.0 V Regulator Bias Current vs. Load Current


Figure 4. Switch Saturation Voltage


Figure 3. Supply Current vs. Switch Current


Figure 5. Oscillator Frequency (kHz) vs. $\mathrm{C}_{\mathrm{OsC}}(\mathrm{pF})$, Assuming $\mathrm{R}_{\mathrm{BIAS}}=64.9 \mathrm{k} \Omega$

## CIRCUIT DESCRIPTION



Figure 6. Block Diagram of 5.0 V Linear Regulator Portion of the CS5112

### 5.0 V LINEAR REGULATOR

The 5.0 V linear regulator consists of an error amplifier, bandgap voltage reference, and a composite pass transistor.

The 5.0 V linear regulator circuitry is shown in Figure 6. When an unregulated voltage greater than 6.6 V is applied to the $\mathrm{V}_{\text {REG }}$ input, a 5.0 V regulated DC voltage will be present at $\mathrm{V}_{\mathrm{LIN}}$. For proper operation of the 5.0 V linear regulator, the $\mathrm{I}_{\text {BIAS }}$ lead must have a $64.9 \mathrm{k} \Omega$ pull down resistor to ground. A $100 \mu \mathrm{~F}$ or larger capacitor with an ESR < $8.0 \Omega$ must be connected between $\mathrm{V}_{\text {LIN }}$ and ground. To operate the 5.0 V linear regulator as an independent regulator (i.e. separate from the switching supply), the input voltage must be tied to the $\mathrm{V}_{\text {REG }}$ lead.

As the voltage at the $\mathrm{V}_{\text {REG }}$ input is increased, $\mathrm{Q}_{1}$ is turned on. $\mathrm{Q}_{1}$ provides base drive for $\mathrm{Q}_{2}$ which in turn provides base current for $Q_{3}$. As $Q_{3}$ is turned on, the output voltage, $\mathrm{V}_{\mathrm{LIN}}$, begins to rise as $\mathrm{Q}_{3}$ 's output current charges the output capacitor, CoUT. Once $\mathrm{V}_{\text {LIN }}$ rises to a certain level, the error amplifier becomes biased and provides the appropriate amount of base current to $\mathrm{Q}_{1}$. The error amplifier monitors the scaled output voltage via an internal voltage divider, $\mathrm{R}_{2}$ through $\mathrm{R}_{5}$, and compares it to the bandgap voltage reference. The error amplifier output or error signal is an output current equal to the error amplifier's input differential voltage times the transconductance of the amplifier. Therefore, the error amplifier varies the base current to $Q_{1}$, which provides bias to $Q_{2}$ and $Q_{3}$, based on the difference between the reference voltage and the scaled $\mathrm{V}_{\mathrm{LIN}}$ output voltage.

## CONTROL FUNCTIONS

The watchdog timer circuitry monitors an input signal (WDI) from the microprocessor. It responds to the falling edge of this watchdog signal which it expects to see within an externally programmable time (see Figure 7).

The watchdog time is given by:

$$
\text { tWDI }=1.353 \times \text { CDelayRBIAS }^{2}
$$

Using $C_{\text {Delay }}=0.1 \mu \mathrm{~F}$ and $\mathrm{R}_{\text {BIAS }}=64.9 \mathrm{k} \Omega$ gives a time ranging from 6.25 ms to 11 ms assuming ideal components. Based on this, the software must be written so that the watchdog arrives at least every 6.25 ms . In practice, the tolerance of $\mathrm{C}_{\text {Delay }}$ and $\mathrm{R}_{\text {BIAS }}$ must be taken into account when calculating the minimum watchdog time ( $\mathrm{t}_{\mathrm{WDI}}$ ).


Figure 7. Timing Diagram for Normal Regulator Operation

If a correct watchdog signal is not received within the specified time a reset pulse train is issued until the correct watchdog signal is received. The nominal reset signal in this case is a 5 volt square wave with a $50 \%$ duty cycle as shown in Figure 8.


A: Watchdog waiting for low-going transition on WDI
B: $\overline{R E S E T}$ stays low for twol time
Figure 8. Timing Diagram When WDI Fails to Appear Within the Preset Time Interval, twDI

The $\overline{\text { RESET }}$ signal frequency is given by:

$$
\mathrm{fRESET}=\frac{1}{2(\mathrm{tWDI})}
$$

The Power On Reset (POR) and low voltage $\overline{\text { RESET }}$ use the same circuitry and issue a reset when the linear output voltage is below the regulation limit. After $\mathrm{V}_{\text {LIN }}$ rises above the minimum specified value, $\overline{\text { RESET }}$ remains low for a fixed period $t_{\text {POR }}$ as shown in Figures 9 and 10.


Figure 9. The Power On Reset Time Interval ( $\mathrm{t}_{\mathrm{POR}}$ ) Begins When V ${ }_{\text {LIN }}$ Rises Above 4.45 V (Typical)


Figure 10. RESET Signal Is Issued Whenever $\mathrm{V}_{\text {LIN }}$ Falls Below 4.25 V (Typical)

The POR delay ( $\mathrm{t}_{\mathrm{POR}}$ ) is given by:

$$
\text { tPOR }=1.353 \times \text { CDelay }_{\text {RIAS }}
$$

## CURRENT MODE PWM SWITCHING CIRCUITRY

The current mode PWM switching voltage regulator contains an error amplifier with selectable feedback inputs, a current sense amplifier, an adjustable oscillator and a 1.4 A output power switch with antisaturation control. The switching regulator and external components, connected in a boost configuration, are shown in Figure 11.

The switching regulator begins operation when $V_{\text {REG }}$ and $\mathrm{V}_{\text {IN }}$ are raised above 5 volts. $\mathrm{V}_{\text {REG }}$ is required since the switching supply's control circuitry is powered through $\mathrm{V}_{\text {LIN }} . \mathrm{V}_{\text {IN }}$ supplies the base drive to the switcher output transistor.

The output transistor turns on when the oscillator starts to charge the capacitor on $\mathrm{C}_{\text {OSC }}$. The output current will develop a voltage drop across the internal sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$. This voltage drop produces a proportional voltage at the output of the current sense amplifier, which is compared to the output of the error amplifier. The error amplifier generates an output voltage which is proportional to the difference between the scaled down output boost voltage ( $\mathrm{V}_{\mathrm{FB} 1}$ or $\mathrm{V}_{\mathrm{FB} 2}$ ) and the internal bandgap voltage reference. Once the current sense amplifier output exceeds the error amplifier's output voltage, the output transistor is turned off.

The energy stored in the inductor during the output transistor on time is transferred to the load when the output transistor is turned off. The output transistor is turned back
on at the next rising edge of the oscillator. On a cycle by cycle basis, the current mode controller in a discontinuous mode of operation charges the inductor to the appropriate amount of energy, based on the energy demand of the load. Figure 12 shows the typical current and voltage waveforms for a boost supply operating in the discontinuous mode.
2. The switching regulator can be disabled by providing a logic high at the $\overline{\text { ENABLE input. }}$
3. The boost output voltage can be controlled dynamically by the feedback select input. If select is open, $\mathrm{V}_{\mathrm{FB} 2}$ is selected. If select is low, then $\mathrm{V}_{\mathrm{FB} 1}$ is selected.

## Notes:

1. Refer to Figure 5 to determine oscillator frequency.


Figure 11. Block Diagram of the 1.4 A Current Mode Control Switching Regulator Portion of the CS5112 in a Boost Configuration


Figure 12. Voltage and Current Waveforms for Boost Topology in CS5112

## PROTECTION CIRCUITRY

The current out of $\mathrm{V}_{\mathrm{LIN}}$ is sensed in order to limit excessive power dissipation in the linear output transistor over the output range of 0 V to regulation. Also, the current into $\mathrm{V}_{\mathrm{SW}}$ is sensed in order to provide the current limit function in the switcher output transistor.

If the die temperature is increased above $160^{\circ} \mathrm{C}$, either due to excessive ambient temperature or excessive power dissipation, the drive to the linear output transistor is reduced proportionally with increasing die temperature. Therefore, $\mathrm{V}_{\text {LIN }}$ will decrease with increasing die temperature above $160^{\circ} \mathrm{C}$. Since the switcher control circuitry is powered through $\mathrm{V}_{\mathrm{LIN}}$, the switcher performance, including current limit, will be affected by the decrease in $\mathrm{V}_{\text {LIN }}$.

## APPLICATION NOTES

## DESIGN PROCEDURE FOR BOOST TOPOLOGY

This section outlines a procedure for designing a boost switching power supply operating in the discontinuous mode.

## Step 1

Determine the output power required by the load.
POUT = IOUTVOUT

## Step 2

Choose COSC based on the target oscillator frequency with an external resistor value, $\mathrm{R}_{\text {BIAS }}=64.9 \mathrm{k} \Omega$ (See Figure 5).

## Step 3

Next select the output voltage feedback sense resistor divider as follows (Figure 13).

For $\mathrm{V}_{\mathrm{FB} 1}$ active, choose a value for $\mathrm{R}_{1}$ and then solve for $R_{E Q}$ where:

$$
\begin{equation*}
R_{E Q}=\frac{R_{1}}{\frac{V_{O U T}}{V_{F B 1}}-1} \tag{2}
\end{equation*}
$$

For $\mathrm{V}_{\mathrm{FB} 2}$ active, find:

$$
\begin{equation*}
V_{F B 1}=V_{O U T}\left(\frac{R_{E Q}}{R_{1}+R_{E Q}}\right) \tag{3}
\end{equation*}
$$

and then calculate $\mathrm{R}_{2}$ where:

$$
\begin{equation*}
\mathrm{R}_{2}=\frac{\mathrm{V}_{\mathrm{R} 2}}{\mathrm{I}_{\mathrm{R} 2}}=\frac{\mathrm{V}_{\mathrm{FB} 1}-\mathrm{V}_{\mathrm{FB} 2}}{\mathrm{~V}_{\mathrm{FB} 1} / \mathrm{R}_{\mathrm{EQ}}} \tag{4}
\end{equation*}
$$

Then find $\mathrm{R}_{3}$, where:

$$
\begin{equation*}
R_{3}=R_{E Q}-R_{2} \tag{5}
\end{equation*}
$$



Figure 13. Feedback Sense Resistor Divider Connected Between V

## Step 4

Determine the maximum on time at the minimum oscillator frequency and $\mathrm{V}_{\text {IN }}$. For discontinuous operation, all of the stored energy in the inductor is transferred to the load prior to the next cycle. Since the current through the inductor cannot change instantaneously and the inductance is constant, a volt-second balance exists between the on time and off time. The voltage across the inductor during the on cycle is $\mathrm{V}_{\text {IN }}$ and the voltage across the inductor during the off cycle is $\mathrm{V}_{\text {OUT }}-\mathrm{V}_{\text {IN }}$. Therefore:

$$
\begin{equation*}
\text { VINtON }=(\text { VOUT }- \text { VIN }) \text { tOFF } \tag{6}
\end{equation*}
$$

where the maximum on time is:

## Step 5

Calculate the maximum inductance allowed for discontinuous operation:

$$
\begin{equation*}
\mathrm{L}(\mathrm{MAX})=\frac{\mathrm{fSW}(\mathrm{MIN}) \mathrm{VIN}^{2}(\mathrm{MIN}) \mathrm{tON}^{2}(\mathrm{MAX})}{2 \mathrm{POUT} / \eta} \tag{8}
\end{equation*}
$$

where $\eta=$ efficiency.
Usually $\eta=0.75$ is a good starting point. The IC's power dissipation should be calculated after the peak current has been determined in Step 6. If the efficiency is less than originally assumed, decrease the efficiency and recalculate the maximum inductance and peak current.

## Step 6

Determine the peak inductor current at the minimum inductance, minimum $\mathrm{V}_{\text {IN }}$ and maximum on time to make sure the inductor current doesn't exceed 1.4 A.

$$
\begin{equation*}
\mathrm{IPK}=\frac{\mathrm{VIN}_{\mathrm{IN}}(\mathrm{MIN}) \mathrm{tON}(\mathrm{MAX})}{\mathrm{L}_{(\mathrm{MIN})}} \tag{9}
\end{equation*}
$$

## Step 7

Determine the minimum output capacitance and maximum ESR based on the allowable output voltage ripple.

$$
\begin{align*}
\operatorname{COUT}(\mathrm{MIN}) & =\frac{\mathrm{IPK}}{8 \mathrm{~V} \text { VIPPLE }}  \tag{10}\\
\mathrm{ESR}_{(\mathrm{MIN})} & =\frac{\Delta \mathrm{V}_{\text {RIPPLE }}}{\mathrm{IPK}} \tag{11}
\end{align*}
$$

In practice, it is normally necessary to use a larger capacitance value to obtain a low ESR. By placing capacitors in parallel, the equivalent ESR can be reduced.

## Step 8

Compensate the feedback loop to guarantee stability under all operating conditions. To do this, we calculate the modulator gain and the feedback resistor network attenuation and set the gain of the error amplifier so that the overall loop gain is 0 dB at the crossover frequency, $\mathrm{f}_{\mathrm{CO}}$. In addition, the gain slope should be $-20 \mathrm{~dB} /$ decade at the crossover frequency.
The low frequency gain of the modulator (i.e. error amplifier output to output voltage) is:

$$
\begin{equation*}
\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{~V}_{\mathrm{EA}}}=\frac{\mathrm{IPK}(\mathrm{MAX})}{\mathrm{V}_{\mathrm{EA}(\mathrm{MAX})}} \sqrt{\frac{\mathrm{R}_{\mathrm{LOADLf}}}{2}} \tag{12}
\end{equation*}
$$

where:

$$
\operatorname{IPK}(\mathrm{MAX})=\frac{\mathrm{VEA}_{\mathrm{E}(\mathrm{MAX}) / \mathrm{GCSA}}}{\mathrm{RS}}=\frac{2.4 \mathrm{~V} / 7}{150 \mathrm{~m} \Omega}=2.3 \mathrm{~A}(13)
$$

The $\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{EA}}$ transfer function has a pole at:

$$
\begin{equation*}
f_{p}=1 /\left(\pi R_{\text {LOADCOUT }}\right) \tag{14}
\end{equation*}
$$

and a zero due to the output capacitor's ESR at:

$$
\begin{equation*}
f_{\mathrm{Z}}=1 /(2 \pi E S R(C O U T)) \tag{15}
\end{equation*}
$$

Since the error amplifier reference voltage is 1.25 V , the output voltage must be divided down or attenuated before being applied to the input of the error amplifier. The feedback resistor divider attenuation is:

$$
\frac{1.25 \mathrm{~V}}{\mathrm{~V}_{\mathrm{OUT}}}
$$

The error amplifier in the CS5112 is an operational transconductance amplifier (OTA), with a gain given by:
GOTA = gmZOUT
where:

$$
\begin{equation*}
\mathrm{gm}=\frac{\Delta \mathrm{l}_{\mathrm{OUT}}}{\Delta \mathrm{~V}_{\mathrm{IN}}} \tag{17}
\end{equation*}
$$

For the CS5112, gm $=2700 \mu \mathrm{~A} / \mathrm{V}$ typical.
One possible error amplifier compensation scheme is shown in Figure 14. This gives the error amplifier a gain plot as shown in Figure 15.

For the error amplifier gain shown in Figure 15, a low frequency pole is generated by the error amplifier output impedance and $\mathrm{C}_{1}$. This is shown by the line AB with a $-20 \mathrm{~dB} /$ decade slope in Figure 15. The slope changes to zero at point $B$ due to the zero at:

$$
\begin{equation*}
f_{z}=1 /\left(2 \pi R_{4} C_{1}\right) \tag{18}
\end{equation*}
$$



Figure 14. RC Network Used to Compensate the Error Amplifier (OTA)

A pole at point C :

$$
\begin{equation*}
f_{p}=1 /\left(\pi R_{4} C_{2}\right) \tag{19}
\end{equation*}
$$

offsets the zero set by the ESR of the output capacitors.
An alternative scheme uses a single capacitor as shown in Figure 16, to roll the gain off at a relatively low frequency.

## Step 9

Finally the watchdog timer period and Power on Reset time is determined by:

$$
\begin{equation*}
\text { tDelay }=1.353 \times \text { CDelay RBIAS } \tag{20}
\end{equation*}
$$



Figure 15. Bode Plot of Error Amplifier (OTA) Gain and Modulator Gain Added to the Feedback Resistor Divider Attenuation


Figure 16. A Typical Application Diagram with External Components Configured in a Boost Topology

## CS5112

## Linear regulator output current vs. Input voltage



Figure 17. The Shaded Area Shows the Safe Operating Area of the CS5112 as a Function of $I_{\text {LIN }}, V_{\text {REG }}$, and $\Theta_{\text {JA. }}$. Refer to Table 5 for Typical Loads and Voltages.

Table 5.

| $\mathbf{V}_{\mathbf{R E G}}(\mathbf{V})$ | $\mathbf{V}_{\mathbf{I N}}(\mathbf{V})$ | $\mathbf{I}_{\text {LIN }}(\mathbf{m A})$ | Linear Power <br> Dissipation $(\mathbf{W})$ | Worst Case Switcher <br> Power Available <br> $\left(\Theta_{\mathbf{J A}}=55^{\circ} \mathbf{C} / \mathbf{W}\right)(\mathbf{W})$ | Worst Case Switcher <br> Power Available <br> $\left(\Theta_{\mathbf{J A}}=\mathbf{3 5} \mathbf{C} / \mathbf{W}\right)(\mathbf{W})$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 20 | 14 | 25 | 0.44 | 0.74 | 1.42 |
| 20 | 14 | 50 | 0.83 | 0.35 | 1.03 |
| 20 | 14 | 75 | 1.22 | ${ }^{*}$ | 0.64 |
| 20 | 14 | 100 | 1.60 | ${ }^{*}$ | 0.26 |
| 25 | 14 | 25 | 0.60 | 0.58 | 1.26 |
| 25 | 14 | 50 | 1.11 | $*$ | 0.75 |
| 25 | 14 | 75 | 1.62 | $*$ | 0.24 |
| 25 | 14 | 100 | 2.14 | $*$ |  |

*Subjecting the CS5112 to these conditions will exceed the maximum total power that the part can handle, thereby forcing it into thermal limit.

PACKAGE THERMAL DATA

| Parameter |  | SO-24L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\Theta J C}$ | Typical | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5171, CS5172, CS5173, CS5174

### 1.5 A 280 kHz/560 kHz Boost Regulators

The CS5171/2/3/4 products are $280 \mathrm{kHz} / 560 \mathrm{kHz}$ switching regulators with a high efficiency, 1.5 A integrated switch. These parts operate over a wide input voltage range, from 2.7 V to 30 V . The flexibility of the design allows the chips to operate in most power supply configurations, including boost, flyback, forward, inverting, and SEPIC. The ICs utilize current mode architecture, which allows excellent load and line regulation, as well as a practical means for limiting current. Combining high frequency operation with a highly integrated regulator circuit results in an extremely compact power supply solution. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback controls for either positive or negative voltage regulation. These parts are pin-to-pin compatible with LT1372/1373.

| Part Number | Frequency | Feedback Voltage Polarity |
| :---: | :---: | :---: |
| CS5171 | 280 kHz | positive |
| CS5172 | 280 kHz | negative |
| CS5173 | 560 kHz | positive |
| CS5174 | 560 kHz | negative |

## Features

- Integrated Power Switch: 1.5 A Guaranteed
- Wide Input Range: 2.7 V to 30 V
- High Frequency Allows for Small Components
- Minimum External Components
- Easy External Synchronization
- Built in Overcurrent Protection
- Frequency Foldback Reduces Component Stress During an Overcurrent Condition
- Thermal Shutdown with Hysteresis
- Regulates Either Positive or Negative Output Voltages
- Shut Down Current: $50 \mu \mathrm{~A}$ Maximum
- Pin-to-Pin Compatible with LT1372/1373
- Wide Ambient Temperature Range
- Industrial Grade: $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$
- Commercial Grade: $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$


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## PIN CONNECTIONS AND MARKING DIAGRAM


$x \quad=1,2,3$, or 4
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1402 of this data sheet.


Figure 1. Applications Diagram

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Junction Temperature Range, $\mathrm{T}_{J}$ |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\text {STORAGE }}$ |  | Reflow (Note 1) | 230 Peak |
| Lead Temperature Soldering: |  | ${ }^{\circ} \mathrm{C}$ |  |
| ESD, Human Body Model |  | 1.2 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\text {CC }}$ | 30 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | 200 mA |
| Shutdown/Sync | SS | 30 V | -0.3 V | 1.0 mA | 1.0 mA |
| Loop Compensation | $\mathrm{V}_{\text {C }}$ | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Voltage Feedback Input | FB <br> (CS5171/3 only) | 10 V | -0.3 V | 1.0 mA | 1.0 mA |
| Negative Feedback Input <br> (transient, 10 ms ) | NFB <br> (CS5172/4 only) | -10 V | 10 V | 1.0 mA | 1.0 mA |
| Test Pin | Test | 6.0 V | -0.3 V | 1.0 mA | 4 A |
| Power Ground | PGND | 0.3 V | -0.3 V | 1.0 mA |  |
| Analog Ground | AGND | 0 V | 0 V | $\mathrm{~N} / \mathrm{A}$ | 10 mA |
| Switch Input | $\mathrm{V}_{\text {SW }}$ | 40 V | -0.3 V | 10 mA | 10 mA |

ELECTRICAL CHARACTERISTICS (2.7 V< $\mathrm{V}_{\mathrm{CC}}<30 \mathrm{~V}$; Industrial Grade: $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$; Commercial Grade: $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$; $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$; For all CS5171/2/3/4 specifications unless otherwise stated.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- |

Positive and Negative Error Amplifiers

| FB Reference Voltage (CS5171/3 only) | $\mathrm{V}_{\mathrm{C}}$ tied to FB ; measure at FB | 1.246 | 1.276 | 1.300 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NFB Reference Voltage (CS5172/4 only) | $\mathrm{V}_{\mathrm{C}}=1.25 \mathrm{~V}$ | -2.55 | -2.45 | -2.35 | V |
| FB Input Current (CS5171/3 only) | $\mathrm{FB}=\mathrm{V}_{\text {REF }}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| NFB Input Current (CS5172/4 only) | $N F B=N V_{\text {REF }}$ | -16 | -10 | -5.0 | $\mu \mathrm{A}$ |
| FB Reference Voltage Line Regulation (CS5171/3 only) | $V_{C}=F B$ | - | 0.01 | 0.03 | \%/V |
| NFB Reference Voltage Line Regulation (CS5172/4 only) | $\mathrm{V}_{\mathrm{C}}=1.25 \mathrm{~V}$ | - | 0.01 | 0.05 | \%/V |
| Positive Error Amp Transconductance | $\mathrm{I}_{\mathrm{VC}}= \pm 25 \mu \mathrm{~A}$ | 300 | 550 | 800 | $\mu \mathrm{Mho}$ |
| Negative Error Amp Transconductance | $\mathrm{IVC}= \pm 5 \mu \mathrm{~A}$ | 115 | 160 | 225 | $\mu \mathrm{Mho}$ |
| Positive Error Amp Gain | Note 2 | 200 | 500 | - | V/V |
| Negative Error Amp Gain | Note 2 | 100 | 180 | 320 | V/V |
| $\mathrm{V}_{\mathrm{C}}$ Source Current | $\mathrm{FB}=1.0 \mathrm{~V}$ or $\mathrm{NFB}=-1.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=1.25 \mathrm{~V}$ | 25 | 50 | 90 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{C}}$ Sink Current | $\mathrm{FB}=1.5 \mathrm{~V}$ or $\mathrm{NFB}=-3.1 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=1.25 \mathrm{~V}$ | 200 | 625 | 1500 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{C}}$ High Clamp Voltage | $\begin{aligned} & \mathrm{FB}=1.0 \mathrm{~V} \text { or } \mathrm{NFB}=-1.9 \mathrm{~V} ; \\ & \mathrm{V}_{\mathrm{C}} \text { sources } 25 \mu \mathrm{~A} \end{aligned}$ | 1.5 | 1.7 | 1.9 | V |
| $\mathrm{V}_{\mathrm{C}}$ Low Clamp Voltage | $\mathrm{FB}=1.5 \mathrm{~V}$ or $\mathrm{NFB}=-3.1 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}$ sinks $25 \mu \mathrm{~A}$ | 0.25 | 0.50 | 0.65 | V |
| $\mathrm{V}_{\mathrm{C}}$ Threshold | Reduce $\mathrm{V}_{\mathrm{C}}$ from 1.5 V until switching stops | 0.75 | 1.05 | 1.30 | V |

## Oscillator

| Base Operating Frequency | $\mathrm{CS} 5171 / 2, \mathrm{FB}=1 \mathrm{~V}$ or NFB $=-1.9 \mathrm{~V}$ | 230 | 280 | 310 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Reduced Operating Frequency | $\mathrm{CS} 5171 / 2, \mathrm{FB}=0 \mathrm{~V}$ or NFB $=0 \mathrm{~V}$ | 30 | 52 | 120 | kHz |
| Maximum Duty Cycle | $\mathrm{CS} 5171 / 2$ | 90 | 94 | - | $\%$ |
| Base Operating Frequency | $\mathrm{CS} 5173 / 4, \mathrm{FB}=1 \mathrm{~V}$ or NFB $=-1.9 \mathrm{~V}$ | 460 | 560 | 620 | kHz |
| Reduced Operating Frequency | $\mathrm{CS5173/4} ,\mathrm{FB} \mathrm{=0} \mathrm{~V} \mathrm{or} \mathrm{NFB} \mathrm{=} \mathrm{~V}$ | 60 | 104 | 160 | kHz |
| Maximum Duty Cycle | $\mathrm{CS5173/4}$ | 82 | 90 | - | $\%$ |
| NFB Frequency Shift Threshold | Frequency drops to reduced operating <br> frequency | -0.80 | -0.65 | -0.50 | V |
| FB Frequency Shift Threshold | Frequency drops to reduced operating <br> frequency | 0.36 | 0.40 | 0.44 | V |

## Sync/ Shutdown

| Sync Range | CS5171/2 | 320 | - | 500 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Sync Range | CS5173/4 | 640 | - | 1000 | kHz |
| Sync Pulse Transition Threshold | Rise time $=20 \mathrm{~ns}$ | 2.5 | - | - | V |
| SS Bias Current | $\mathrm{SS}=0 \mathrm{~V}$ | -15 | -3.0 | - | $\mu \mathrm{A}$ |
|  | $\mathrm{SS}=3.0 \mathrm{~V}$ | - | 3.0 | 8.0 | $\mu \mathrm{~A}$ |
| Shutdown Threshold |  | 0.50 | 0.85 | 1.20 | V |
| Shutdown Delay | $2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 12 \mathrm{~V}$ | 12 | 80 | 350 | $\mu \mathrm{~s}$ |
|  | $12 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}} \leq 30 \mathrm{~V}$ | 12 | 36 | 200 | $\mu \mathrm{~s}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

## CS5171, CS5172, CS5173, CS5174

ELECTRICAL CHARACTERISTICS (continued) (2.7 $\mathrm{V}<\mathrm{V}_{\mathrm{CC}}<30 \mathrm{~V}$; Industrial Grade: $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$; Commercial Grade: $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$; $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$; For all CS5171/2/3/4 specifications unless otherwise stated.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Switch |  |  |  |  |  |
| Switch Saturation Voltage | $\begin{aligned} & \text { I SWITCH }=1.5 \mathrm{~A}, \text { Note } 3 \\ & \text { IsWITCH }=1.0 \mathrm{~A}, 0 \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C} \\ & \text { I SWITCH }=1.0 \mathrm{~A},-40 \leq \mathrm{T}_{\mathrm{A}} \leq 0^{\circ} \mathrm{C} \text {, Note } 3 \\ & \text { I } \end{aligned}$ | - - - - | $\begin{gathered} 0.8 \\ 0.55 \\ 0.75 \\ 0.09 \end{gathered}$ | $\begin{gathered} 1.4 \\ 1.00 \\ 1.30 \\ 0.45 \end{gathered}$ | $\begin{aligned} & V \\ & V \\ & V \\ & V \end{aligned}$ |
| Switch Current Limit | 50\% duty cycle, Note 3 80\% duty cycle, Note 3 | $\begin{aligned} & 1.6 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 1.7 \end{aligned}$ | $\begin{aligned} & 2.4 \\ & 2.2 \end{aligned}$ | $\begin{aligned} & \text { A } \\ & \text { A } \end{aligned}$ |
| Minimum Pulse Width | $\mathrm{FB}=0 \mathrm{~V}$ or $\mathrm{NFB}=0 \mathrm{~V}, \mathrm{I}_{\text {SW }}=4.0 \mathrm{~A}$, Note 3 | 200 | 250 | 300 | ns |
| $\Delta \mathrm{l}_{\mathrm{CC}} / \Delta \mathrm{IV} \mathrm{V}_{\text {SW }}$ | $\begin{aligned} & 2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 12 \mathrm{~V}, 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{SW}} \leq 1.0 \mathrm{~A} \\ & 12 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}} \leq 30 \mathrm{~V}, 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{SW}} \leq 1.0 \mathrm{~A} \\ & 2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 12 \mathrm{~V}, 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{SW}} \leq 1.5 \mathrm{~A}, \\ & \text { Note } 3 \\ & 12 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}} \leq 30 \mathrm{~V}, 10 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{SW}} \leq 1.5 \mathrm{~A}, \\ & \text { Note } 3 \end{aligned}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \end{aligned}$ | $\begin{gathered} 10 \\ - \\ 17 \\ - \end{gathered}$ | $\begin{gathered} 30 \\ 100 \\ 30 \\ 100 \end{gathered}$ | mA/A <br> mA/A <br> mA/A <br> mA/A |
| Switch Leakage | $\mathrm{V}_{\mathrm{SW}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=0 \mathrm{~V}$ | - | 2.0 | 100 | $\mu \mathrm{A}$ |
| General |  |  |  |  |  |
| Operating Current | $\mathrm{I}_{\text {sw }}=0$ | - | 5.5 | 8.0 | mA |
| Shutdown Mode Current | $\begin{aligned} & \mathrm{V}_{\mathrm{C}}<0.8 \mathrm{~V}, \mathrm{SS}=0 \mathrm{~V}, 2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 12 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{C}}<0.8 \mathrm{~V}, \mathrm{SS}=0 \mathrm{~V}, 12 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 30 \mathrm{~V} \end{aligned}$ | - | $12$ | $\begin{gathered} 60 \\ 100 \end{gathered}$ | $\mu \mathrm{A}$ |
| Minimum Operation Input Voltage | $\mathrm{V}_{\text {SW }}$ switching, maximum $\mathrm{I}_{\mathrm{SW}}=10 \mathrm{~mA}$ | - | 2.45 | 2.70 | V |
| Thermal Shutdown | Note 3 | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Hysteresis | Note 3 | - | 25 | - | ${ }^{\circ} \mathrm{C}$ |

3. Guaranteed by design, not $100 \%$ tested in production.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |
| :---: | :---: | :---: |
| 8 LEAD SO NARROW | Pin Symbol | Function |
| 1 | $\mathrm{V}_{\mathrm{C}}$ | Loop compensation pin. The $\mathrm{V}_{\mathrm{C}}$ pin is the output of the error amplifier and is used for loop compensation, current limit and soft start. Loop compensation can be implemented by a simple RC network as shown in the application diagram on page 1383 as R1 and C1. |
| 2 (CS5171/3 only) | FB | Positive regulator feedback pin. This pin senses a positive output voltage and is referenced to 1.276 V . When the voltage at this pin falls below 0.4 V , chip switching frequency reduces to $20 \%$ of the nominal frequency. |
| $\begin{aligned} & 2 \text { (CS5172/4 only) } \\ & 3 \text { (CS5171/3 only) } \end{aligned}$ | Test | These pins are connected to internal test logic and should either be left floating or tied to ground. Connection to a voltage between 2 V and 6 V shuts down the internal oscillator and leaves the power switch running. |
| 3 (CS5172/4 only) | NFB | Negative feedback pin. This pin senses a negative output voltage and is referenced to -2.5 V . When the voltage at this pin goes above -0.65 V , chip switching frequency reduces to $20 \%$ of the nominal frequency. |
| 4 | SS | Synchronization and shutdown pin. This pin may be used to synchronize the part to nearly twice the base frequency. A TTL low will shut the part down and put it into low current mode. If synchronization is not used, this pin should be either tied high or left floating for normal operation. |

PACKAGE PIN DESCRIPTION

| Package Pin Number | Pin Symbol | Function |
| :---: | :---: | :---: |
| 8 LEAD SO NARROW (continued) |  |  |
| 5 | $\mathrm{V}_{\mathrm{CC}}$ | Input power supply pin. This pin supplies power to the part and should have a bypass capacitor connected to AGND. |
| 6 | AGND | Analog ground. This pin provides a clean ground for the controller circuitry and should not be in the path of large currents. The output voltage sensing resistors should be connected to this ground pin. This pin is connected to the IC substrate. |
| 7 | PGND | Power ground. This pin is the ground connection for the emitter of the power switching transistor. Connection to a good ground plane is essential. |
| 8 | $\mathrm{V}_{\text {SW }}$ | High current switch pin. This pin connects internally to the collector of the power switch. The open voltage across the power switch can be as high as 40 V . To minimize radiation, use a trace as short as practical. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. $\mathrm{I}_{\mathrm{CC}}$ (No Switching) vs. $\mathrm{T}_{\mathrm{A}}$


Figure 5. $\mathrm{V}_{\text {CE(SAT) }}$ vs. $\mathrm{I}_{\mathrm{SW}}$


Figure 7. Switching Frequency vs. $\mathrm{T}_{\mathrm{A}}$ (CS5171/2 only)


Figure 4. $\Delta \mathrm{I}_{\mathrm{CC}} / \Delta \mathrm{I} \mathrm{V}_{\mathrm{SW}}$ vs. $\mathrm{T}_{\mathrm{A}}$


Figure 6. Minimum Input Voltage vs. $\mathrm{T}_{\mathrm{A}}$


Figure 8. Switching Frequency vs. $\mathrm{T}_{\mathrm{A}}$ (CS5173/4 only)

## CS5171, CS5172, CS5173, CS5174

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 9. Switching Frequency vs. $\mathrm{V}_{\mathrm{FB}}$ (CS5171/3 only)


Figure 11. Reference Voltage vs. $\mathrm{T}_{\mathrm{A}}$ (CS5171/3 only)


Figure 13. $\mathrm{I}_{\mathrm{FB}}$ vs. $\mathrm{T}_{\mathrm{A}}$ (CS5171/3 only)


Figure 10. Switching Frequency vs. $\mathrm{V}_{\text {NFB }}$
(CS5172/4 only)


Figure 12. Reference Voltage vs. $\mathrm{T}_{\mathrm{A}}$ (CS5172/4 only)


Figure 14. $l_{\mathrm{NFB}}$ vs. $\mathrm{T}_{\mathrm{A}}$ (CS5172/4 only)


Figure 16. Current Limit vs. $\mathrm{T}_{\mathrm{A}}$


Figure 18. $\mathrm{V}_{\mathrm{C}}$ Threshold and High Clamp Voltage vs. $\mathrm{T}_{\mathrm{A}}$


Figure 20. Shutdown Delay vs. $\mathbf{T}_{\mathrm{A}}$


Figure 17. Maximum Duty Cycle vs. $\mathrm{T}_{\mathrm{A}}$


Figure 19. Shutdown Threshold vs. $\mathrm{T}_{\mathrm{A}}$


Figure 21. ISS vs. $\mathrm{V}_{\mathrm{SS}}$


Figure 22. Icc vs. $\mathrm{V}_{\mathrm{IN}}$ During Shutdown


Figure 24. Negative Error Amplifier Transconductance vs. $\mathrm{T}_{\mathrm{A}}$ (CS5172/4 only)


Figure 26. Error Amplifier IOUT vs. $\mathrm{V}_{\text {NFB }}$ (CS5172/4 only)


Figure 23. Error Amplifier Transconductance vs. $\mathrm{T}_{\mathrm{A}}$ (CS5171/3 only)


Figure 25. Error Amplifier IOUT vs. VFB (CS5171/3 only)


Figure 27. Switch Leakage vs. $\mathrm{T}_{\mathrm{A}}$

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## Current Mode Control



Figure 28. Current Mode Control Scheme
The CS517x family incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on-time of the power switch. The oscillator is used as a fixed-frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse-by-pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain-bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, subharmonic oscillation at duty cycles over $50 \%$. The CS517x family solves this problem by adopting a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

## Oscillator and Shutdown



Figure 29. Timing Diagram of Sync and Shutdown

The oscillator is trimmed to guarantee an $18 \%$ frequency accuracy. The output of the oscillator turns on the power switch at a frequency of $280 \mathrm{kHz}(\mathrm{CS} 5171 / 2)$ or 560 kHz (CS5173/4), as shown in Figure 28. The power switch is turned off by the output of the PWM Comparator.

A TTL-compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 29, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby resetting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.
A sustained logic low at the SS pin will shut down the IC and reduce the supply current.

An additional feature includes frequency shift to $20 \%$ of the nominal frequency when either the NFB or FB pins trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on-time is limited by the PWM comparator minimum pulse width. Extra switch off-time reduces the minimum duty cycle to protect external components and the IC itself.
As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

## Error Amplifier



Figure 30. Error Amplifier Equivalent Circuit
For CS5172/4, the NFB pin is internally referenced to -2.5 V with approximately a $250 \mathrm{k} \Omega$ input impedance. For CS5171/3, the FB pin is directly connected to the inverting input of the positive error amplifier, whose non-inverting input is fed by the 1.276 V reference. Both amplifiers are transconductance amplifiers with a high output impedance of approximately $1 \mathrm{M} \Omega$, as shown in Figure 30 . The $\mathrm{V}_{\mathrm{C}}$ pin is connected to the output of the error amplifiers and is internally clamped between 0.5 V and 1.7 V . A typical connection at the $\mathrm{V}_{\mathrm{C}}$ pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.
An external shunt can be connected between the $\mathrm{V}_{\mathrm{C}}$ pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

## Switch Driver and Power Switch

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors ( $63 \mathrm{~m} \Omega$ total) to the PGND pin. PGND is not connected to the IC substrate so that switching noise can be isolated from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5 A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40 V on the collector $\left(\mathrm{V}_{\mathrm{SW}} \mathrm{pin}\right)$. The saturation voltage of the switch is typically less than 1 V to minimize power dissipation.

## Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit (such as a fuse or relay) has to be implemented to protect the load, power supply and ICs.

In other topologies, the frequency shift built into the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.


Figure 31. Startup Waveforms of Circuit Shown in the Application Diagram. Load $=400 \mathrm{~mA}$.

The CS517x can be activated by either connecting the $\mathrm{V}_{\mathrm{CC}}$ pin to a voltage source or by enabling the SS pin. Startup waveforms shown in Figure 31 are measured in the boost converter demonstrated in the Application Diagram on the page 1383 of this document. Recorded after the input voltage is turned on, this waveform shows the various phases during the power up transition.

When the $\mathrm{V}_{\mathrm{CC}}$ voltage is below the minimum supply voltage, the $\mathrm{V}_{\mathrm{SW}}$ pin is in high impedance. Therefore, current conducts directly from the input power source to the
output through the inductor and diode. Once $\mathrm{V}_{\mathrm{CC}}$ reaches approximately 1.5 V , the internal power switch briefly turns on. This is a part of the CS517x's normal operation. The turn-on of the power switch accounts for the initial current swing.
When the $\mathrm{V}_{\mathrm{C}}$ pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the $\mathrm{V}_{\text {SW }}$ pin. Detecting a low output voltage at the FB pin, the built-in frequency shift feature reduces the switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is otherwise limited by the minimum on-time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V , the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull-on, by which the sink current of the error amplifier is increased once an overvoltage condition is detected. The overvoltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

## COMPONENT SELECTION

## Frequency Compensation

The goal of frequency compensation is to achieve desirable transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in Figure 32, provides a frequency response of two poles and one zero. This frequency response is further illustrated in the Bode plot shown in Figure 33.


Figure 32. A Typical Compensation Network
The high DC gain in Figure 33 is desirable for achieving DC accuracy over line and load variations. The DC gain of a transconductance error amplifier can be calculated as follows:

GaindC $=G_{M} \times R_{O}$
where:
$\mathrm{G}_{\mathrm{M}}=$ error amplifier transconductance;
$\mathrm{R}_{\mathrm{O}}=$ error amplifier output resistance $\approx 1 \mathrm{M} \Omega$.

The low frequency pole, $\mathrm{f}_{\mathrm{P} 1}$, is determined by the error amplifier output resistance and C 1 as:
$\mathrm{fP}_{\mathrm{P}}=\frac{1}{2 \pi \mathrm{C} 1 \mathrm{RO}_{\mathrm{O}}}$
The first zero generated by C 1 and R 1 is:
$\mathrm{f} Z 1=\frac{1}{2 \pi \mathrm{C} 1 \mathrm{R} 1}$
The phase lead provided by this zero ensures that the loop has at least a $45^{\circ}$ phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency:
$\mathrm{fP}=\frac{1}{2 \pi \mathrm{COR}_{\mathrm{LOAD}}}$
where:
$\mathrm{C}_{\mathrm{O}}=$ equivalent output capacitance of the error amplifier $\approx 120 \mathrm{pF}$;
$\mathrm{R}_{\mathrm{LOAD}}=$ load resistance.
The high frequency pole, $\mathrm{f}_{\mathrm{P} 2}$, can be placed at the output filter's ESR zero or at half the switching frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C2 and R1:
$\mathrm{fP} 2=\frac{1}{2 \pi \mathrm{C} 2 \mathrm{R} 1}$
One simple method to ensure adequate phase margin is to design the frequency response with a -20 dB per decade slope, until unity-gain crossover. The crossover frequency should be selected at the midpoint between $\mathrm{f}_{\mathrm{Z} 1}$ and $\mathrm{f}_{\mathrm{P} 2}$ where the phase margin is maximized.


Figure 33. Bode Plot of the Compensation Network Shown in Figure 32

## Negative Voltage Feedback

Since the negative error amplifier has finite input impedance as shown in Figure 34, its induced error has to be considered. If a voltage divider is used to scale down the negative output voltage for the NFB pin, the equation for calculating output voltage is:

$$
-\mathrm{V}_{\text {OUT }}=\left(\frac{-2.5(\mathrm{R} 1+\mathrm{R} 2)}{\mathrm{R} 2}\right)-10 \mu \mathrm{~A} \times \mathrm{R} 1
$$



Figure 34. Negative Error Amplifier and NFB Pin
It is shown that if R1 is less than 10 k , the deviation from the design target will be less than 0.1 V . If the tolerances of the negative voltage reference and NFB pin input current are considered, the possible offset of the output $V_{\text {OFFSET }}$ varies in the range of:

$$
\begin{aligned}
\left(\frac{-0.0 .5(\mathrm{R} 1+\mathrm{R} 2)}{\mathrm{R} 2}\right) & -(15 \mu \mathrm{~A} \times \mathrm{R} 1) \leq \mathrm{V}_{\text {OFFSET }} \\
& \leq\left(\frac{0.0 .5(\mathrm{R} 1+\mathrm{R} 2)}{\mathrm{R} 2}\right)-(5 \mu \mathrm{~A} \times \mathrm{R} 1)
\end{aligned}
$$

## $\mathrm{V}_{\text {SW }}$ Voltage Limit

In the boost topology, $\mathrm{V}_{\text {SW }}$ pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes

$$
V_{S W}(M A X)=V_{O U T}(M A X)+V_{F}
$$

where:
$\mathrm{V}_{\mathrm{F}}=$ output diode forward voltage.
In the flyback topology, peak $\mathrm{V}_{\mathrm{SW}}$ voltage is governed by:

$$
V_{S W}(M A X)=V_{C C}(M A X)+\left(V_{O U T}+V_{F}\right) \times N
$$

where:
$\mathrm{N}=$ transformer turns ratio, primary over secondary.
When the power switch turns off, there exists a voltage spike superimposed on top of the steady-state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the $\mathrm{V}_{\mathrm{SW}}$ and PGND pins. To prevent the voltage at the $\mathrm{V}_{\mathrm{SW}}$ pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the $\mathrm{V}_{\mathrm{SW}}$ pin and ground.

## Magnetic Component Selection

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain $\left(\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{CC}}\right)$,
assuming $100 \%$ energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$
\text { IRIPPLE }=\frac{\mathrm{V}_{\mathrm{CC}}\left(\mathrm{~V}_{\text {OUT }}-\mathrm{V}_{\mathrm{CC}}\right)}{(\mathrm{f})(\mathrm{L})\left(\mathrm{V}_{\mathrm{OUT}}\right)}
$$

where:
$\mathrm{f}=280 \mathrm{kHz}$ for CS5171/2 and 560 kHz for CS5173/4.
The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

## Input Capacitor Selection

In boost circuits, the inductor becomes part of the input filter, as shown in Figure 36. In continuous mode, the input current waveform is triangular and does not contain a large pulsed current, as shown in Figure 35. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from Figure 35, the product of the inductor current ripple and the input capacitor's effective series resistance (ESR) determine the $\mathrm{V}_{\mathrm{CC}}$ ripple. In most applications, input capacitors in the range of $10 \mu \mathrm{~F}$ to $100 \mu \mathrm{~F}$ with an ESR less than $0.3 \Omega$ work well up to a full 1.5 A switch current.


Figure 35. Boost Input Voltage and Current Ripple Waveforms


Figure 36. Boost Circuit Effective Input Filter
The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is seen by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator: energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than $20 \mu \mathrm{~F}$ with low ESR is required. To reduce the noise generated by the inductor, insert a $1.0 \mu \mathrm{~F}$ ceramic capacitor between $\mathrm{V}_{\mathrm{CC}}$ and ground as close as possible to the chip.

## Output Capacitor Selection



Figure 37. Typical Output Voltage Ripple
By examining the waveforms shown in Figure 37, we can see that the output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, $\mathrm{I}_{\mathrm{L}}$ flows into the output capacitor causing an instant $\Delta \mathrm{V}=\mathrm{I}_{\mathrm{IN}} \times$ ESR. At the same time, current $\mathrm{I}_{\mathrm{L}}-\mathrm{I}_{\text {OUT }}$ charges the capacitor and
increases the output voltage gradually. When the power switch is turned on, $\mathrm{I}_{\mathrm{L}}$ is shunted to ground and $\mathrm{I}_{\text {OUT }}$ discharges the output capacitor. When the $\mathrm{I}_{\mathrm{L}}$ ripple is small enough, $\mathrm{I}_{\mathrm{L}}$ can be treated as a constant and is equal to input current $\mathrm{I}_{\text {IN }}$. Summing up, the output voltage peak-peak ripple can be calculated by:

$$
\begin{aligned}
\mathrm{V}_{\text {OUT }}(\text { RIPPLE })= & \frac{(\mathrm{IIN}-\operatorname{lOUT})(1-\mathrm{D})}{(\mathrm{COUT})(\mathrm{f})} \\
& +\frac{\mathrm{IOUTD}}{(\mathrm{COUT})(\mathrm{f})}+\mathrm{I}_{\mathrm{IN}} \times \mathrm{ESR}
\end{aligned}
$$

The equation can be expressed more conveniently in terms of $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\text {OUT }}$ and $\mathrm{I}_{\text {OUT }}$ for design purposes as follows:

$$
\begin{aligned}
\mathrm{V}_{\text {OUT }}(\mathrm{RIPPLE})= & \frac{\mathrm{IOUT}\left(\mathrm{~V}_{\text {OUT }}-\mathrm{V}_{\mathrm{CC}}\right)}{(\mathrm{COUT})(\mathrm{f})} \times \frac{1}{(\mathrm{COUT})(\mathrm{f})} \\
& +\frac{(\mathrm{lOUT})\left(\mathrm{V}_{\text {OUT }}\right)(\mathrm{ESR})}{\mathrm{V}_{\mathrm{CC}}}
\end{aligned}
$$

The capacitor RMS ripple current is:

$$
\begin{aligned}
\text { IRIPPLE } & =\sqrt{\left(\mathrm{I}_{\mathrm{IN}}-\mathrm{IOUT}\right)^{2}(1-\mathrm{D})+(\mathrm{IOUT})^{2}(\mathrm{D})} \\
& =\operatorname{IOUT} \sqrt{\frac{V_{O U T}-V_{C C}}{V_{C C}}}
\end{aligned}
$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

## Reducing the Current Limit

In some applications, the designer may prefer a lower limit on the switch current than 1.5 A . An external shunt can be connected between the $\mathrm{V}_{\mathrm{C}}$ pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

The voltage on the $\mathrm{V}_{\mathrm{C}}$ pin can be evaluated with the equation
$V_{C}=I_{S W} R_{E A} A_{V}$
where:
$\mathrm{R}_{\mathrm{E}}=.063 \Omega$, the value of the internal emitter resistor;
$A_{V}=5 \mathrm{~V} / \mathrm{V}$, the gain of the current sense amplifier.
Since $R_{E}$ and $A_{V}$ cannot be changed by the end user, the only available method for limiting switch current below 1.5 A is to clamp the $\mathrm{V}_{\mathrm{C}}$ pin at a lower voltage. If the maximum switch or inductor current is substituted into the equation above, the desired clamp voltage will result.

A simple diode clamp, as shown in Figure 38, clamps the $\mathrm{V}_{\mathrm{C}}$ voltage to a diode drop above the voltage on resistor R 3 . Unfortunately, such a simple circuit is not generally acceptable if $\mathrm{V}_{\mathrm{IN}}$ is loosely regulated.


Figure 38. Current Limiting using a Diode Clamp
Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in Figure 39.


Figure 39. Current Limiting using a Current Sense Resistor
The switch current is limited to
ISWITCH(PEAK) $=\frac{\mathrm{V}_{\mathrm{BE}(\mathrm{Q} 1)}}{\operatorname{RSENSE}}$
where:
$\mathrm{V}_{\mathrm{BE}(\mathrm{Q} 1)}=$ the base-emitter voltage drop of Q 1 , typically 0.65 V .

The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor, $\mathrm{R}_{\text {SENSE }}$, results in a considerable power loss which
increases with the duty cycle. Resistor R2 and capacitor C3 form a low-pass filter to remove noise.

## Subharmonic Oscillation

Subharmonic oscillation (SHM) is a problem found in current-mode control systems, where instability results when duty cycle exceeds $50 \%$. SHM only occurs in switching regulators with a continuous inductor current. This instability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high-frequency audible noise.

SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal "slope compensation" to prevent any duty cycle instability from carrying through to the next switching cycle. In the CS517x family, slope compensation is added during the entire switch on-time, typically in the amount of $180 \mathrm{~mA} / \mu \mathrm{s}$.

In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is more slope compensation to avoid the unwanted oscillation. In that case, an external circuit, shown in Figure 40, can be added to increase the amount of slope compensation used. This circuit requires only a few components and is "tacked on" to the compensation network.


Figure 40. Technique for Increasing Slope Compensation
The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors R2 and R3 form a voltage divider off of the $\mathrm{V}_{\mathrm{SW}}$
pin. In normal operation, $\mathrm{V}_{\mathrm{SW}}$ looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating $\mathrm{V}_{\mathrm{SW}}$ in the boost and flyback topologies are given in the section "V $V_{S W}$ Voltage Limit." The voltage on $\mathrm{V}_{\text {SW }}$ charges capacitor C 3 when the switch is off, causing the voltage at the $\mathrm{V}_{\mathrm{C}}$ pin to shift upwards. When the switch turns on, C3 discharges through R3, producing a negative slope at the $\mathrm{V}_{\mathrm{C}}$ pin. This negative slope provides the slope compensation.
The amount of slope compensation added by this circuit is

$$
\frac{\Delta I}{\Delta T}=V_{S W}\left(\frac{R_{3}}{R_{2}+R_{3}}\right)\left(1-e^{\frac{-(1-D)}{R_{3} C_{3} f W}}\right)\left(\frac{f S W}{(1-D) R_{E A V}}\right)
$$

where:
$\Delta \mathrm{I} / \Delta \mathrm{T}=$ the amount of slope compensation added (A/s);
$\mathrm{V}_{\mathrm{SW}}=$ the voltage at the switch node when the transistor is turned off (V);
$\mathrm{f}_{\mathrm{SW}}=$ the switching frequency, typically 280 kHz (CS5171/3) or 560 kHz (CS5172/4) (Hz);
$\mathrm{D}=$ the duty cycle;
$\mathrm{R}_{\mathrm{E}}=0.063 \Omega$, the value of the internal emitter resistor;
$\mathrm{A}_{\mathrm{V}}=5 \mathrm{~V} / \mathrm{V}$, the gain of the current sense amplifier.
In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, then select values for R2 and R3 such that the amount of slope compensation added is $100 \mathrm{~mA} / \mu \mathrm{s}$. Then R2 may be increased or decreased as necessary. Of course, the series combination of R2 and R3 should be large enough to avoid drawing excessive current from $\mathrm{V}_{\mathrm{SW}}$. Additionally, to ensure that the control loop stability is improved, the time constant formed by the additional components should be chosen such that
$\mathrm{R}_{3} \mathrm{C}_{3}<\frac{1-\mathrm{D}}{\mathrm{fSW}}$
Finally, it is worth mentioning that the added slope compensation is a trade-off between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

## Soft Start

Through the addition of an external circuit, a soft-start function can be added to the CS5171/2/3/4 family of components. Soft-start circuitry prevents the $\mathrm{V}_{\mathrm{C}}$ pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope.

This circuit, shown in Figure 41, requires a minimum number of components and allows the soft-start circuitry to activate any time the SS pin is used to restart the converter.


Figure 41. Soft Start
Resistor R1 and capacitors C1 and C2 form the compensation network. At turn on, the voltage at the $\mathrm{V}_{\mathrm{C}}$ pin starts to come up, charging capacitor C3 through Schottky diode D 2, clamping the voltage at the $\mathrm{V}_{\mathrm{C}}$ pin such that switching begins when $\mathrm{V}_{\mathrm{C}}$ reaches the $\mathrm{V}_{\mathrm{C}}$ threshold, typically 1.05 V (refer to graphs for detail over temperature).
$V_{C}=V_{F}(D 2)+V_{C 3}$
Therefore, C 3 slows the startup of the circuit by limiting the voltage on the $\mathrm{V}_{\mathrm{C}}$ pin. The soft-start time increases with the size of C3.

Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to $\mathrm{V}_{\mathrm{IN}}$.

## Calculating Junction Temperature

To ensure safe operation of the CS5171/2/3/4, the designer must calculate the on-chip power dissipation and determine its expected junction temperature. Internal thermal protection circuitry will turn the part off once the junction temperature exceeds $180^{\circ} \mathrm{C} \pm 30^{\circ}$. However, repeated operation at such high temperatures will ensure a reduced operating life.

Calculation of the junction temperature is an imprecise but simple task. First, the power losses must be quantified. There are three major sources of power loss on the CS517x:

- biasing of internal control circuitry, PBIAS
- switch driver, P PRIVER
- switch saturation, $\mathrm{P}_{\text {SAT }}$

The internal control circuitry, including the oscillator and linear regulator, requires a small amount of power even when the switch is turned off. The specifications section of this datasheet reveals that the typical operating current, $\mathrm{I}_{\mathrm{Q}}$,
due to this circuitry is 5.5 mA . Additional guidance can be found in the graph of operating current vs. temperature. This graph shows that IQ is strongly dependent on input voltage, $\mathrm{V}_{\mathrm{IN}}$, and the ambient temperature, $\mathrm{T}_{\mathrm{A}}$. Then
PBIAS $=\mathrm{V}_{\text {IN }}{ }^{\prime} \mathrm{Q}$
Since the onboard switch is an NPN transistor, the base drive current must be factored in as well. This current is drawn from the $\mathrm{V}_{\text {IN }}$ pin, in addition to the control circuitry current. The base drive current is listed in the specifications as $\Delta \mathrm{I}_{\mathrm{CC}} / \Delta \mathrm{I}_{\mathrm{SW}}$, or switch transconductance. As before, the designer will find additional guidance in the graphs. With that information, the designer can calculate

$$
\text { PDRIVER }=\mathrm{V}_{\text {INIS }} \times \frac{\mathrm{I} \mathrm{CC}}{\Delta \mathrm{I} S W} \times \mathrm{D}
$$

where:
$\mathrm{I}_{\mathrm{SW}}=$ the current through the switch;
$\mathrm{D}=$ the duty cycle or percentage of switch on-time.
$\mathrm{I}_{\text {SW }}$ and D are dependent on the type of converter. In a boost converter,

$$
\begin{aligned}
\operatorname{ISW}(A V G) \cong \operatorname{LLOAD} & \times D \times \frac{1}{\text { Efficiency }} \\
D & \cong \frac{V_{O U T}-V_{I N}}{V_{O U T}}
\end{aligned}
$$

In a flyback converter,
$\operatorname{ISW}(A V G) \cong \frac{\text { VOUTILOAD }}{\text { VIN }} \times \frac{1}{\text { Efficiency }}$
$\mathrm{D} \cong \frac{\mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\text {OUT }}+\frac{N_{S}}{N_{P}} \mathrm{~V}_{\text {IN }}}$
The switch saturation voltage, $\mathrm{V}_{(\mathrm{CE}) \mathrm{SAT}}$, is the last major source of on-chip power loss. $\mathrm{V}_{\text {(CE)SAT }}$ is the collector-emitter voltage of the internal NPN transistor when it is driven into saturation by its base drive current. The value for $\mathrm{V}_{(\mathrm{CE}) \text { SAT }}$ can be obtained from the specifications or from the graphs, as "Switch Saturation Voltage." Thus,

$$
\mathrm{PSAT}_{S A} \cong \mathrm{~V}_{(C E) S A T I S W} \times \mathrm{D}
$$

Finally, the total on-chip power losses are

```
PD = PBIAS + PDRIVER + PSAT
```

Power dissipation in a semiconductor device results in the generation of heat in the junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturers' data sheets as $\Theta_{\mathrm{JA}}$, or junction-to-ambient thermal resistance. The on-chip junction temperature can be calculated if $\Theta_{\mathrm{JA}}$, the air temperature near the surface of the IC, and the on-chip power dissipation are known.
$T J=T_{A}+(P D \Theta J A)$
where:
$\mathrm{T}_{\mathrm{J}}=\mathrm{IC}$ or FET junction temperature $\left({ }^{\circ} \mathrm{C}\right)$;

## CS5171, CS5172, CS5173, CS5174

$\mathrm{T}_{\mathrm{A}}=$ ambient temperature $\left({ }^{\circ} \mathrm{C}\right)$;
$\mathrm{P}_{\mathrm{D}}=$ power dissipated by part in question (W);
$\Theta_{\mathrm{JA}}=$ junction-to-ambient thermal resistance $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$.
For ON Semiconductor components, the value for $\Theta_{\mathrm{JA}}$ can be found on page 1402 of the datasheet, under "Package Thermal Data." Note that this value is different for every package style and every manufacturer. For the CS517x, $\Theta_{\mathrm{JA}}=165^{\circ} \mathrm{C} / \mathrm{W}$.

Once the designer has calculated $\mathrm{T}_{\mathrm{J}}$, the question of whether the CS517x can be used in an application is settled. If $\mathrm{T}_{\mathrm{J}}$ exceeds $150^{\circ} \mathrm{C}$, the absolute maximum allowable junction temperature, the CS517x is not suitable for that application.

If $\mathrm{T}_{\mathrm{J}}$ approaches $150^{\circ} \mathrm{C}$, the designer should consider possible means of reducing the junction temperature. Perhaps another converter topology could be selected to reduce the switch current. Increasing the airflow across the surface of the chip might be considered to reduce $T_{A}$. $A$ copper "landing pad" can be connected to the ground or $\mathrm{V}_{\text {IN }}$ pins - designers are referred to ON Semiconductor applications note SR-006 for more information on properly sizing a copper area.

## Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents
combined with trace inductance generates voltage transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on-chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on-chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.


Figure 42. Additional Application Diagram, 5.0 V to -12 V Inverting Converter


Figure 43. Additional Application Diagram, 3.3 V Input, 5 V/ 400 mA Output Boost Converter


Figure 44. Additional Application Diagram, 2.7 to 13 V Input, $\pm 12 \mathrm{~V} / 200 \mathrm{~mA}$ Output Flyback Converter


Figure 45. Additional Application Diagram, $\mathbf{- 9 . 0}$ V to -28 V Input, $\mathbf{- 5 . 0} \mathrm{V} / 700 \mathrm{~mA}$ Output Inverted Buck Converter


Figure 46. Additional Application Diagram,2.7 V to 28 V Input, 5.0 V Output SEPIC Converter


Figure 47. Additional Application Diagram, 4.0 V Input, 100 V/ 10 mA Output Boost Converter with Output Voltage Multiplier


Figure 48. Additional Application Diagram, 5.0 V Input, $\pm 12 \mathrm{~V}$ Output Dual Boost Converter

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package | Shipping |
| :--- | :---: | :---: | :---: |
| CS5171ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5171EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |
| CS5172ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5172EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |
| CS5173ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5173EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |
| CS5174ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5174EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |
| CS5171GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5171GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS5172GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5172GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |
| CS5173GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5173GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |
| CS5174GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 95 Units/Rail |
| CS5174GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ | 2500 Tape \& Reel |

PACKAGE THERMAL DATA

| Parameter |  | 8 Lead SO Narrow | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 45 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 165 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## Variable Frequency Micropower DC-to-DC Converter

The MC33463 series are micropower step-up switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of $4.0 \mu \mathrm{~A}$ typical.

The MC33463H-XXKT1 series features a highly accurate voltage reference, an oscillator, a variable frequency modulation (VFM) controller, a driver transistor (Lx), a comparator and feedback resistive divider.

The MC33463H-XXLT1 is identical to the MC33463H-XXKT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

## MC33463 Series Features:

- Low Quiescent Bias Current of $4.0 \mu \mathrm{~A}$
- High Output Voltage Accuracy of $\pm 2.5 \%$
- Low Startup Voltage of 0.9 V at 1.0 mA
- Wide Output Voltage Range of 2.5 V to 7.5 V Available
- High Efficiency of $80 \%$ Typical
- Surface Mount Package


Figure 1. Typical Circuit Configurations for the MC33463H


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


## PIN CONNECTIONS

MC33463H-XXKT1

(Top View)

MC33463H-XXLT1


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1413 of this data sheet.


This device contains 100 active transistors.
Figure 2. Representative Block Diagrams

MAXIMUM RATINGS $\left(T_{C}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage (Transient) | $\mathrm{V}_{\mathrm{CC}}$ | 12 | V |
| Power Supply Voltage (Operating) | $\mathrm{V}_{\mathrm{CC}}$ | 8.0 | V |
| External Pin Voltage | $\mathrm{V}_{\text {EXT }}$ | -0.3 to $\mathrm{V}_{\mathrm{O}}$ | V |
| Lx Pin Voltage | $\mathrm{V}_{\text {Lx }}$ | 12 | V |
| EXT Pin Source/Sink Current | $\mathrm{I}_{\text {EXT }}$ | $\pm 50$ | mA |
| Lx Pin Sink Current | LLx | 250 | mA |
| Power Dissipation and Thermal Characteristics H Suffix, Plastic Package Case 1213 (SOT-89) Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $\begin{array}{r} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{JA}} \\ \hline \end{array}$ | $\begin{aligned} & 500 \\ & 200 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -30 to +80 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}\right.$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Maximum Oscillator Frequency | $\mathrm{f}_{\text {osc }}$ | 80 | 100 | 120 | kHz |
| Oscillator Minimum Supply Voltage ( $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ ) KT1 Suffix | $\mathrm{V}_{\mathrm{CC}}$ | 0.7 | - | - | V |
| Oscillator Startup Voltage ( $\mathrm{I}=1.0 \mathrm{~mA}$ ) <br> KT1 Suffix | $\mathrm{V}_{\mathrm{CC}}$ | - | 0.8 | 0.9 | V |
| Oscillator Startup Voltage ( $\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}$ ) LT1 Suffix | $\mathrm{V}_{\mathrm{CC}}$ | - | 0.7 | 0.8 | V |
| Maximum Oscillator Duty Cycle | $\mathrm{D}_{\text {max }}$ | 65 | 75 | 85 | \% |

Lx OUTPUT (KT1 SUFFIX)

| ON State Sink Current ( $\mathrm{V}_{\mathrm{Lx}}=0.4 \mathrm{~V}$ ) <br> 30KT1 Suffix <br> 33KT1 Suffix <br> 50KT1 Suffix | LLx | $\begin{aligned} & 60 \\ & 63 \\ & 80 \end{aligned}$ |  | - | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {Lx }}$ Voltage Limit (Note 1) | $V_{\text {LxLim }}$ | 0.65 | 0.8 | 1.0 | V |
| OFF State Leakage Current ( $\mathrm{V}_{\mathrm{Lx}}=6.0 \mathrm{~V}$ ) | ILKG | - | - | 0.5 | $\mu \mathrm{A}$ |

EXT OUTPUT (LT1 SUFFIX)

| ON State Source Current $\left(\mathrm{V}_{\mathrm{EXT}}=\mathrm{V}_{\mathrm{O}}-0.4 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {source }}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| 30LT1 Suffix |  | 1.5 | - | - |  |
| 33LT1 Suffix |  | 1.575 | - | - |  |
| 50LT1 Suffix |  | 2.0 | - | - |  |
| OFF State Sink Current $\left(\mathrm{V}_{\mathrm{EXT}}=0.4 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {sink }}$ |  |  |  | mA |
| 30LT1 Suffix |  | 1.5 | - | - |  |
| 33LT1 Suffix |  | 1.575 | - | - |  |
| 50LT1 Suffix |  | 2.0 | - | - |  |

TOTAL DEVICE

| Output Voltage <br> 30KT1 or 30LT1 Suffix 33KT1 or 33LT1 Suffix 50KT1 or 50LT1 Suffix | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 2.925 \\ & 3.218 \\ & 4.875 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.075 \\ & 3.383 \\ & 5.125 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Quiescent Bias Current ( $\mathrm{I}=0 \mathrm{~mA}$ ) <br> $30 \mathrm{KT1}$ Suffix ( $\mathrm{V}_{\text {in }}=1.8 \mathrm{~V}$ ) <br> 33KT1 Suffix <br> 50KT1 Suffix ( $\mathrm{V}_{\text {in }}=3.0 \mathrm{~V}$ ) <br> Quiescent Bias Current ( $\left.\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O}}+0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}\right)$ <br> 30KT1 Suffix <br> 33KT1 Suffix <br> 50KT1 Suffix | $\mathrm{I}_{\mathrm{Q}}$ |  | $\begin{aligned} & 4.0 \\ & 4.3 \\ & 6.0 \\ & 2.0 \\ & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 8.0 \\ & 8.6 \\ & 12 \\ & 5.0 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| ```Quiescent Bias Current ( \(\mathrm{I}=0 \mathrm{~mA}\) ) 30LT1 Suffix ( \(\mathrm{V}_{\text {in }}=1.8 \mathrm{~V}\) ) 33LT1 Suffix 50LT1 Suffix ( \(\mathrm{V}_{\text {in }}=3.0 \mathrm{~V}\) ) Quiescent Bias Current ( \(\left.\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O}}+0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}\right)\) 30LT1 Suffix 33LT1 Suffix 50LT1 Suffix``` | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{gathered} 30 \\ 34.5 \\ 60 \\ \\ 2.0 \\ 2.0 \\ 2.0 \\ \hline \end{gathered}$ | $\begin{aligned} & 50 \\ & 56 \\ & 90 \\ & \\ & 5.0 \\ & 5.0 \\ & 5.0 \\ & \hline \end{aligned}$ | $\mu \mathrm{A}$ |

1. When the $L x$ switch is turned on, $\mathrm{I}_{\mathrm{Lx}}$ carried through the $\mathrm{R}_{\mathrm{DS}(o n)}$ of the Lx switch results in $\mathrm{V}_{\mathrm{Lx}}$. When $\mathrm{V}_{\mathrm{Lx}}$ reaches $\mathrm{V}_{\mathrm{Lx}}$.im , the Lx switch is turned off by the Lx switch protection circuit.


Figure 3. Quiescent Current versus Temperature


Figure 5. Oscillator Frequency versus Temperature


Figure 7. Lx Switching Current versus Temperature


Figure 4. Quiescent Current versus Temperature


Figure 6. Oscillator Duty Ratio versus Temperature


Figure 8. $\mathrm{V}_{\mathrm{Lx}}$ Voltage Limit versus Temperature


Figure 9. Output Voltage versus Output Current

Figure 11. Efficiency versus Output Current


Figure 13. Startup/Hold Voltage versus Output Current


Figure 10. Output Voltage versus Output Current


Figure 12. Efficiency versus Output Current


Figure 14. Startup/Hold Voltage versus Output Current


Figure 15. Output Voltage versus Temperature

## DEFINITIONS

Quiescent Bias Current - Current which is used to operate the switching regulator chip and is not delivered to the load.
Leakage Current - Current drawn through a transistor junction, under a specified collector voltage, when the transistor is off.

## FUNCTIONAL DESCRIPTION

## Introduction

The MC33463 series are monolithic power switching regulators optimized for dc-to-dc converter applications where power drain must be minimized. The combination of features in this series allows the system designer to directly implement step-up, step-down or flyback converters with a small number of external components. Potential applications include low power consumer products and battery powered portable products. Typical application circuits are shown in Figure 17 and Figure 18.

## Operating Description

The MC33463 series converters each operate as a fixed on-time, variable off-time voltage mode ripple regulator. Operation is intended to be in the discontinuous mode, where the inductor current ramps up to a peak value which is greater than or equal to twice the value of the dc input current during the on-time of the transistor switch. During the off-time of the transistor switch, the inductor current ramps down to zero and remains at zero until another switching cycle begins.

Because the output voltage pin is also used as the supply voltage for powering internal circuitry, an external startup circuit is needed in step-down and flyback converter designs to provide initial power to the integrated circuit to begin switching. The startup circuit needed can be three


Figure 16. Startup/Hold Voltage versus Temperature
discrete components, as shown in Figure 19, or a micropower undervoltage sensor, as shown in Figure 20.

## Oscillator

The maximum oscillator frequency, is internally programmed to 100 kHz . The duty ratio of the oscillator is designed for a constant value of 0.75 nominal. Hence the nominal on-time of the power switch is:

$$
t_{\text {on }}=\frac{D}{f_{\mathrm{osc}}}=\frac{0.75}{(100 \mathrm{kHz})}=7.5 \mu \mathrm{~s}
$$

## Feedback Comparator

The output voltage is sensed and fed to a high speed comparator noninverting input through an internal resistive divider. The comparator inverting input is connected to an internally trimmed to 0.7 V reference.
With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated and terminated by the oscillator, off-time is controlled by the high speed voltage feedback comparator.

## Driver and Output Switch

To aid in system design flexibility and conversion efficiency, two output driver options are provided. The MC33463H-XXKT1 converters have an internal drive transistor which is capable of sinking currents greater than 60 mA into the Lx pin. An internal $\mathrm{V}_{\mathrm{Lx}}$ limiter circuit senses if the Lx pin voltage exceeds 1.0 V during $\mathrm{t}_{\mathrm{on}}$ and turns off the drive transistor. The MC33463H-XXLT1 provides output drive for an external transistor.

## Applications

The following converter applications show the simplicity and flexibility of the converter architecture. Three main converter topologies are demonstrated in Figures 17 through 21.

## MC33463



Figure 17. MC33463H-50KT1 Typical Step-Up Application


Figure 18. MC33463H-50LT1 Typical Step-Up Application


Figure 19. MC33463H-33KT1 Step-Down Application

| Test | Conditions | Results |
| :---: | :---: | :---: |
| Line Regulation | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}$ to $8.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | $18.5 \mathrm{mV}= \pm 0.3 \%$ |
| Load Regulation | $\mathrm{V}_{\mathrm{in}}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 100 mA | $5.7 \mathrm{mV}= \pm 0.1 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | 40 mVpp |
| Efficiency | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | $60.3 \%$ |

## MC33463



Figure 20. Micropower Step-Down Application


Figure 21. Flyback Application

| Calculation | Step-Down | Step-Up | Flyback |
| :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {on }}$ | $\frac{D}{f_{\text {osc }}}$ | $\frac{\mathrm{D}}{\mathrm{f}_{\text {osc }}}$ | $\frac{D}{f_{\text {osc }}}$ |
| L |  | $<\frac{(\mathrm{n})\left(\mathrm{V}_{\text {in }}\right)^{2}\left(\mathrm{t}_{\mathrm{on}}\right)}{\mathrm{P}_{\mathrm{O}}}$ | $<\frac{(n)\left(\mathrm{V}_{\mathrm{in}}\right)^{2}\left(\mathrm{t}_{\mathrm{on}}\right)}{\mathrm{P}_{\mathrm{O}}}$ |
| L(avg) | 10 | $\mathrm{l}_{\text {in }}$ | $\mathrm{l}_{\text {in }}$ |
| $\mathrm{I}_{\mathrm{L}(\mathrm{pk})}$ | $\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {sat }}-\mathrm{V}_{\mathrm{O}}\right)\left(\mathrm{t}_{\text {on }}\right)}{\mathrm{L}}$ | $\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {sat }}\right)\left(\mathrm{t}_{\text {on }}\right)}{\mathrm{L}}$ | $\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {sat }}\right)\left(\mathrm{t}_{\text {on }}\right)}{\mathrm{L}}$ |
| $\mathrm{V}_{\text {ripple(pp) }}$ | $\Delta \mathrm{I}_{\mathrm{L}}\left[\left(\frac{1}{16 f_{\text {OSC }} \mathrm{C}_{\mathrm{O}}}\right)^{2}+(E S R)^{2}\right]^{\frac{1}{2}}$ | $\approx \frac{\left(\mathrm{t}_{\mathrm{on}}\right)\left(\mathrm{I}_{\mathrm{O}}\right)}{\left(\mathrm{C}_{\mathrm{O}}\right)}$ | $\approx \frac{\left(\mathrm{t}_{\mathrm{On}}\right)\left(\mathrm{I}_{\mathrm{O}}\right)}{\left(\mathrm{C}_{\mathrm{O}}\right)}$ |

The following converter design characteristics must be chosen:
$V_{\text {in }}$ - Nominal Operating dc input voltage
$\mathrm{V}_{\mathrm{O}}$ - Desired dc output voltage
Io - Desired dc output current
$\mathrm{V}_{\text {ripple(pp) }}$ - Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor $\mathrm{C}_{\mathrm{O}}$ should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

1. $\mathrm{V}_{\text {sat }}$ - Saturation voltage of the switching transistor.
n -Estimated circuit efficiency.
Figure 22. Design Equations

## MC33463

ORDERING INFORMATION

| Device | Output Voltage | Type | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MC33463H-30KT1 | 3.0 | Int. Switch | $\mathrm{T}_{\mathrm{A}}=-30^{\circ}$ to $+80^{\circ} \mathrm{C}$ | SOT-89 | 1000 Tape \& Reel |
| MC33463H-33KT1 | 3.3 |  |  |  |  |
| MC33463H-50KT1 | 5.0 |  |  |  |  |
| MC33463H-30LT1 | 3.0 |  |  |  |  |
| MC33463H-33LT1 | 3.3 | Switch |  |  |  |
| MC33463H-50LT1 | 5.0 | Drive |  |  |  |

Other voltages from 2.5 V to 7.5 V , in 0.1 V increments are available. Consult factory for information.

## MC33466

## Fixed Frequency PWM Micropower DC-to-DC Converter

The MC33466 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of $15 \mu \mathrm{~A}$ typical.

The MC33466H-XXJT1 series features a highly accurate voltage reference, an oscillator, a pulse width modulation (PWM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33466H-XXLT1 is identical to the MC33466H-XXJT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

## MC33466 Series Features:

- Low Quiescent Bias Current of $15 \mu \mathrm{~A}$
- High Output Voltage Accuracy of $\pm 2.5 \%$
- Low Startup Voltage of 0.9 V at 1.0 mA
- Soft-Start $=500 \mu \mathrm{~s}$
- Surface Mount Package

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


PIN CONNECTIONS


MC33466H-XXLT1


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1426 of this data sheet.

## MC33466

## MC33466H-XXJT1



XX Denotes Output Voltage
This device contains 100 active transistors.

Figure 1. Representative Block Diagrams

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage (Transient) | $\mathrm{V}_{\mathrm{O}}$ | 12 | V |
| Power Supply Voltage (Operating) | $\mathrm{V}_{\mathrm{O}}$ | 8.0 | V |
| External Pin Voltage | $\mathrm{V}_{\mathrm{EXT}}$ | -0.3 to $\mathrm{V}_{\mathrm{O}}$ | V |
| Lx Pin Voltage | $\mathrm{V}_{\mathrm{Lx}}$ | 12 | V |
| EXT Pin Source/Sink Current | $\mathrm{I}_{\mathrm{EXT}}$ | $\pm 50$ | mA |
| Lx Pin Sink Current | $\mathrm{I}_{\mathrm{Lx}}$ | 250 | mA |
| Power Dissipation and Thermal Characteristics <br> H Suffix, Plastic Package Case 1213 (SOT-89) <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air |  |  |  |
| Operating Junction Temperature | $\mathrm{P}_{\mathrm{D}}$ | 500 | mW |
| Operating Ambient Temperature | $\mathrm{R}_{\text {日JA }}$ | $\mathrm{T}_{\mathrm{J}}$ | 200 |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -30 to +80 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}\right.$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Frequency JT1 Suffix LT1 Suffix | $\mathrm{f}_{\text {osc }}$ | $\begin{aligned} & 40 \\ & 80 \end{aligned}$ | $\begin{gathered} 50 \\ 100 \end{gathered}$ | $\begin{gathered} 60 \\ 120 \end{gathered}$ | kHz |
| Oscillator Minimum Startup Voltage ( $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ ) JT1 Suffix | $\mathrm{V}_{\text {start }}$ | - | 0.8 | 0.9 | V |
| Oscillator Minimum Supply Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}$ ) JT1 Suffix | $\mathrm{V}_{\mathrm{CC}}$ | 0.7 | - | - | V |
| Oscillator Startup Voltage ( $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ ) LT1 Suffix | $\mathrm{V}_{\text {start }}$ | - | 0.7 | 0.8 | V |

LX OUTPUT (JT1 SUFFIX)

| ON State Sink Current (V $\mathrm{V}_{\mathrm{Lx}}=0.4 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{Lx}}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| 30JT1 Suffix |  | 60 | - | - |  |
| 33JT1 Suffix |  | 63 | - | - |  |
| 50JT1 Suffix |  | 80 | - | - |  |
| $\mathrm{V}_{\text {Lx }}$ Voltage Limit (Note 1) | $\mathrm{V}_{\text {LxLim }}$ | 0.65 | 0.8 | 1.0 | V |
| OFF State Leakage Current $\left(\mathrm{V}_{\mathrm{Lx}}=6.0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {LKG }}$ | - | - | 0.5 | $\mu \mathrm{~A}$ |

EXT OUTPUT (LT1 SUFFIX)

| ON State Source Current $\left(\mathrm{V}_{\mathrm{EXT}}=\mathrm{V}_{\mathrm{O}}-0.4 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {source }}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| 30LT1 Suffix |  | 1.5 | - | - |  |
| 33LT1 Suffix |  | 1.575 | - | - |  |
| 50LT1 Suffix |  | 2.0 | - | - |  |
| OFF State Sink Current $\left(\mathrm{V}_{\text {EXT }}=0.4 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {sink }}$ |  |  |  | mA |
| 30LT1 Suffix |  | 1.5 | - | - |  |
| 33LT1 Suffix |  | 1.575 | - | - |  |
| 50LT1 Suffix |  | 2.0 | - | - |  |

TOTAL DEVICE

| Maximum Duty Ratio Each Cycle | D | 70 | 80 | 90 | \% |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage <br> 30JT1 or 30LT1 Suffix <br> 33JT1 or 33LT1 Suffix <br> 50JT1 or 50LT1 Suffix | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & 2.925 \\ & 3.218 \\ & 4.875 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 3.075 \\ & 3.383 \\ & 5.125 \end{aligned}$ | V |
| Soft-Start Time (Note 2) | $\mathrm{T}_{\text {ss }}$ | 0.5 | 2.0 | - | ms |
| Quiescent Bias Current ( $\mathrm{l}=0 \mathrm{~mA}$ ) <br> 30JT1 Suffix ( $\mathrm{V}_{\text {in }}=1.8 \mathrm{~V}$ ) <br> 33JT1 Suffix <br> 50JT1 Suffix ( $\mathrm{V}_{\text {in }}=3.0 \mathrm{~V}$ ) <br> Quiescent Bias Current $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O}}+0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}\right)$ <br> 30JT1 Suffix <br> 33JT1 Suffix <br> 50JT1 Suffix | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{aligned} & 15 \\ & 17 \\ & 30 \\ & \\ & 2.0 \\ & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 25 \\ & 27 \\ & 45 \\ & \\ & 5.0 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| ```Quiescent Bias Current ( \(\mathrm{I}=0 \mathrm{~mA}\) ) 30LT1 Suffix (Vin \(=1.8 \mathrm{~V}\) ) 33LT1 Suffix 50LT1 Suffix ( \(\mathrm{V}_{\text {in }}=3.0 \mathrm{~V}\) ) Quiescent Bias Current ( \(\left.\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{O}}+0.5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}\right)\) 30LT1 Suffix 33LT1 Suffix 50LT1 Suffix``` | $\mathrm{I}_{\mathrm{Q}}$ | - | $\begin{gathered} 30 \\ 34.5 \\ 60 \\ \\ 2.0 \\ 2.0 \\ 2.0 \end{gathered}$ | $\begin{aligned} & 50 \\ & 56 \\ & 90 \\ & \\ & 5.0 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\mu \mathrm{A}$ |

1. When the Lx switch is turned on, $\mathrm{I}_{\mathrm{Lx}}$ current carried through the $\mathrm{R}_{\mathrm{DS}(o n)}$ of the Lx switch results in $\mathrm{V}_{\mathrm{Lx}}$. When $\mathrm{V}_{\mathrm{Lx}}$ reaches $\mathrm{V}_{\mathrm{LxLim}}$, the Lx switch is turned off by the Lx switch protection circuit.
2. The soft-start circuit turn-on sequence is as follows:
a) $V_{\text {in }}$ is applied.
b) The internal IC $V_{\text {ref }}$ is held at zero for $200 \mu \mathrm{~s}$. During this time, the error amplifier output voltage ramps up to the positive voltage rail.
c) The internal reference steps up to 0.7 V after $200 \mu \mathrm{~s}$ delay has timed out.
d) The error amplifier output voltage integrates down to its steady state value. As the error amplifier output integrates down, the output Lx pin of EXT pin pulse width gradually widens to its steady operating value.

TYPICAL APPLICATIONS


Figure 2. Quiescent Current versus Temperature

Figure 4. Oscillator Frequency versus Temperature


Figure 6. Lx Switching Current versus Temperature


Figure 3. Quiescent Current versus Temperature


Figure 5. Maximum Duty Ratio versus Temperature


Figure 7. $\mathrm{V}_{\mathrm{Lx}}$ Voltage Limit versus Temperature

TYPICAL APPLICATIONS


Figure 8. Output Voltage versus Output Current


Figure 10. Output Voltage versus Output Current


Figure 12. Efficiency versus Output Current


Figure 9. Output Voltage versus Output Current


Figure 11. Output Voltage versus Output Current

$\mathrm{I}_{\mathrm{o}}$, OUTPUT CURRENT (mA)
Figure 13. Effciency versus Output Current

TYPICAL APPLICATIONS


Figure 14. Efficiency versus Output Current


Figure 16. Startup/Hold Voltage versus Output Current


Figure 18. Output Voltage versus Temperature

$\mathrm{I}_{\mathrm{O}}$, OUTPUT CURRENT (mA)
Figure 15. Efficiency versus Output Current


Figure 17. Startup/Hold Voltage versus Output Current


Figure 19. Startup/Hold Voltage versus Temperature

## MC33466

TYPICAL APPLICATIONS


Figure 20. Supply Current versus Input Voltage

## DEFINITIONS

Quiescent Bias Current - Current which is used to operate the switching regulator chip and is not delivered to the load.
Leakage Current - Current drawn through a transistor junction, under a specified collector voltage, when the transistor is off.

## FUNCTIONAL DESCRIPTION

## Introduction

The MC33466 series are monolithic power switching regulators optimized for dc-to-dc converter applications where power drain must be minimized. The combination of features in this series allows the system designer to directly implement step-up, step-down or flyback converters with a small number of external components. Potential applications include low power consumer products and battery powered portable products. Typical application circuits are shown in Figures 22 through 26.

## Operating Description

The MC33466 series converters operate as a fixed frequency voltage mode regulator. Operation is intended to be in the discontinuous mode, where the inductor current ramps up to a peak value which is greater than or equal to twice the value of the dc input current during the on-time of the transistor switch. During the off-time of the transistor switch, the inductor current ramps down to zero and remains at zero until another switching cycle begins.

Because the output voltage pin is also used as the supply voltage for powering internal circuitry, an external startup circuit is needed in step-down converter and flyback designs to provide initial power to the integrated circuit to begin switching. The startup circuit needed can be three discrete components, as shown in Figure 24, or a micropower undervoltage sensor, as shown in Figure 25.

## Oscillator

The oscillator frequency, is internally programmed to 50 kHz for the JT1 suffix and 100 kHz for the LT1 suffix. The timing capacitor $\left(\mathrm{C}_{\mathrm{T}}\right)$ discharge to charge ratio of the oscillator is designed for a maximum duty cycle of $80 \%$ at the Lx or EXT output. During the charge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the PWM control off, disabling the output transistor drive. The oscillator peak and valley thresholds are 0.5 V and ground, respectively.

## Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the inverting input, while the error amplifier output is applied to the noninverting input. Output switch conduction is initiated when the timing capacitor is charged to its peak voltage value. When the timing capacitor ramp discharges to a voltage below the error amplifier output, the comparator resets a latch terminating output transistor drive for the duration of the oscillator ramp period.

## Error Amplifier and Reference

An Error Amplifier is provided which has a nominal 80 dB of voltage gain at dc. Internal compensation components provide poles at $0.25 \mathrm{~Hz}, 30 \mathrm{kHz}$ and 33 kHz . Two zeros are provided at 1.0 kHz and at 2.5 kHz . The output voltage value is set by the internal voltage divider and a 0.7 V reference which is trimmed to an accuracy of $\pm 2.5 \%$. Because the loop compensation components are located within the IC, discontinuous mode operation is recommended for most applications.

## Driver and Output Switch

To aid in system design flexibility and conversion efficiency, two output driver options are provided. The MC33466H-XXJT1 converters have an internal drive transistor which is capable of sinking currents greater than 60 mA into the Lx pin. An internal $\mathrm{V}_{\mathrm{Lx}}$ limiter circuit senses if the Lx pin voltage exceeds 1.0 V during $\mathrm{t}_{\mathrm{on}}$ and turns off the drive transistor. The MC33466H-XXLT1 provides output drive for an external transistor.

## Applications

The following converter applications show the simplicity and flexibility of the converter architecture. Three main converter topologies are demonstrated in Figures 22 through 26.


Figure 22. MC33466H-50JT1 Typical Step-Up Application


Figure 23. MC33466H-50LT1 Typical Step-Up Application


Figure 24. MC33466H-33JT1 Step-Down Application

| Test | Condition | Results |
| :--- | :---: | :---: |
| Line Regulation | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}$ to $10 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=320 \mathrm{~mA}$ | $7.0 \mathrm{mV}= \pm 0.1 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.3 \mathrm{~mA}$ to 320 mA | $3.0 \mathrm{mV}= \pm 0.04 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=320 \mathrm{~mA}$ | 70 mVpp |
| Efficiency | $\mathrm{V}_{\text {in }}=7.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=320 \mathrm{~mA}$ | $63.8 \%$ |

## MC33466



NOTE: Using the MC33464N-30ATR reduces current drawn in the startup circuit to 1 mA during normal operation.
Figure 25. Micropower Step-Down Application

## MC33466



Figure 26. Flyback Application

| Calculation | Step-Down | Step-Up | Flyback |
| :---: | :---: | :---: | :---: |
| L | $<\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}\right)\left(\mathrm{t}_{\mathrm{on}}\right)}{{ }^{2 \mathrm{l}} \mathrm{O}}$ | $<\frac{\left(\mathrm{v}_{\text {in }}\right)\left(\mathrm{t}_{\mathrm{on}}\right)}{2 \mathrm{I}_{\text {in }}}$ | $<\frac{\left(\mathrm{v}_{\text {in }}\right)\left(\mathrm{t}_{\mathrm{on}}\right)}{\left.2\right\|_{\text {in }}}$ |
| $\mathrm{t}_{\text {on }}$ | $\frac{\mathrm{D}}{\mathrm{fs}}$ | $\frac{\mathrm{D}}{\mathrm{fs}}$ | $\frac{\mathrm{D}}{\mathrm{fs}}$ |
| D | $<\frac{\left(\mathrm{V}_{\mathrm{O}}\right)}{\left(\mathrm{V}_{\text {in }}\right)}$ | $<\frac{\left(\mathrm{V}_{\mathrm{O}}-\mathrm{V}_{\mathrm{in}}\right)}{\left(\mathrm{V}_{\mathrm{O}}\right)}$ | $<\frac{v_{O}}{\left[\left(\frac{N s}{N p}\right)\left(v_{\text {in }}\right)+v_{O}\right]}$ |
| L(avg) | 10 | $1{ }_{\text {in }}$ | $\mathrm{l}_{\text {in }}$ |
| $\mathrm{I}_{\mathrm{L}(\mathrm{pk})}$ | $\frac{\left(V_{\text {in }}-V_{0}\right)\left(t_{\text {on }}\right)}{L}$ | $\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {sat }}\left(\mathrm{t}_{\text {on }}\right)\right.}{L}$ | $\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {sat }}\left(\mathrm{t}_{\text {on }}\right)\right.}{\mathrm{L}}$ |
| $\mathrm{V}_{\text {ripple(pp) }}$ |  | $\mathrm{I}_{\mathrm{L}(\mathrm{pk})}\left[\left(\frac{1}{8 f \mathrm{~S}_{\mathrm{O}}}\right)^{2}+(\mathrm{ESR})^{2}\right]^{\frac{1}{2}}$ |  |

The following converter design characteristics must be chosen:
$\mathrm{V}_{\text {in }}$ - Nominal Operating dc input voltage
$\mathrm{V}_{\mathrm{O}}$ - Desired dc output voltage
$\mathrm{I}_{\mathrm{O}}$ - Desired dc output current
$\mathrm{V}_{\text {ripple(pp) }}$ - Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor $\mathrm{C}_{\mathrm{o}}$ should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.
$D$ - Operating duty cycle $=t_{\mathrm{on}}(\mathrm{fs})$. This parameter must be chosen to be $<0.5$ for step-up and flyback applications.
NOTES: 1. $\mathrm{V}_{\text {sat }}$ - Saturation voltage of the switching transistor.
2. $\mathrm{I}_{\mathrm{in}}$ - DC input switch.
3. fs - Switching frequency, nominally 50 kHz .
4. $\mathrm{R}_{\mathrm{O}}$ - Load resistance. $\mathrm{R}_{\mathrm{O}}=\mathrm{V}_{\mathrm{O}} / \mathrm{l}_{\mathrm{O}}$.
5. Ns, Np - In flyback applications Ns is the number of turns of the secondary transformer winding; Np is the number of the primary winding turns.

Figure 27. Design Equations

## Design Example - Step-down Application

Required: $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$, an output voltage of 3.3 V at 300 mA is desired with an output ripple of less than 300 mVpp .

$$
\mathrm{R}_{\mathrm{O}}=\frac{\mathrm{v}_{\mathrm{O}}}{\mathrm{I}_{\mathrm{O}}}=11 \Omega
$$

1. Because this is a discontinuous mode design, $D<\frac{V_{O}}{V_{i n}}=\frac{3.3}{8}=0.41$. Choose $D=0.33$.
2. $\mathrm{t}_{\mathrm{on}} \approx \frac{\mathrm{D}}{\mathrm{fs}}=\frac{0.33}{(50 \mathrm{kHz})}=6.6 \mu \mathrm{~s}$.
3. $\mathrm{L}<\frac{\left(\mathrm{V}_{\mathrm{in}}-\mathrm{V}_{\mathrm{O}}\right)\left(\mathrm{t}_{\mathrm{on}}\right)}{2 \mathrm{I}_{\mathrm{O}}}=\frac{(8-3.3)(6.6 \mu \mathrm{~s})}{[2(0.3)]}=51.7 \mu \mathrm{H}$.

Choose $\mathrm{L}=47 \mu \mathrm{H}$. Coilcraft part number DO3316P-473.
4. $\mathrm{I}_{\mathrm{L}(\mathrm{pk})}=\frac{\left(\mathrm{V}_{\mathrm{in}}-\mathrm{V}_{\mathrm{O}}\right)\left(\mathrm{t}_{\mathrm{on}}\right)}{\mathrm{L}}=\frac{(8-3.3)(6.6 \mu \mathrm{~s})}{(47 \mu \mathrm{H})}=660 \mathrm{~mA}$.
5. $\mathrm{ESR}<\frac{\mathrm{V}_{\text {ripple(pp) }}}{\mathrm{I}_{\mathrm{L}(\mathrm{pk})}}=\frac{(300 \mathrm{mV})}{(660 \mathrm{~mA})}=0.455 \Omega$.

Choose $\mathrm{C}_{\mathrm{O}}=$ two parallel AVX $330 \mu \mathrm{~F}$ tantalum chip capacitors. Part Number TAJE337M006.
Specified maximum ESR for each is $0.9 \Omega$.
The complete design schematic is shown in Figure 24.

## MC33466

ORDERING INFORMATION

| Device | Output Voltage | Type | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MC33466H-30JT1 | 3.0 | Int. Switch | $\mathrm{T}_{\mathrm{A}}=-30^{\circ}$ to $+80^{\circ} \mathrm{C}$ | SOT-89 | 1000 Tape \& Reel |
| MC33466H-33JT1 | 3.3 |  |  |  |  |
| MC33466H-50JT1 | 5.0 |  |  |  |  |
| MC33466H-30LT1 | 3.0 |  |  |  |  |
| MC33466H-33LT1 | 3.3 | Switch |  |  |  |
| MC33466H-50LT1 | 5.0 | Drive |  |  |  |

Other voltages from 2.5 V to 7.5 V , in 0.1 V increments are available. Consult factory for information.

## NCP1400A

## 100 mA , Fixed Frequency PWM Step-Up Micropower Switching Regulator

The NCP1400A series are micropower step-up DC to DC converters that are specifically designed for powering portable equipment from one or two cell battery packs. These devices are designed to start-up with a cell voltage of 0.8 V and operate down to less than 0.2 V . With only four external components, this series allows a simple means to implement highly efficient converters that are capable of up to 100 mA of output current.

Each device consists of an on-chip fixed frequency oscillator, pulse width modulation controller, phase compensated error amplifier that ensures converter stability with discontinuous mode operation, soft-start, voltage reference, driver, and power MOSFET switch with current limit protection. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1400A device series are available in the Thin SOT-23-5 package with six standard regulated output voltages. Additional voltages that range from 1.8 V to 4.9 V in 100 mV steps can be manufactured.

## Features

- Extremely Low Start-Up Voltage of 0.8 V
- Operation Down to Less than 0.2 V
- Only Four External Components for Simple Highly Efficient Converters
- Up to 100 mA Output Current Capability
- Fixed Frequency Pulse Width Modulation Operation
- Phase Compensated Error Amplifier for Stable Converter Operation
- Chip Enable Power Down Capability for Extended Battery Life


## Typical Applications

- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Handheld Instruments

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http://onsemi.com


THIN SOT-23-5
SN SUFFIX CASE 483

## PIN CONNECTIONS AND MARKING DIAGRAM



$$
\begin{aligned}
\text { xxx } & =\text { Marking } \\
\mathrm{Y} & =\text { Year } \\
\mathrm{W} & =\text { Work Week } \\
& \text { (Top View) }
\end{aligned}
$$

## ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 1428 of this data sheet.


Figure 1. Typical Step-Up Converter Application

ORDERING INFORMATION

| Device | Output Voltage | Switching <br> Frequency | Marking | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP1400ASN19T1 | 1.9 V | 180 KHz | DAI | Thin SOT-23-5 | 3000 Units on 7 Inch Reel |
| NCP1400ASN25T1 | 2.5 V |  | DAV |  |  |
| NCP1400ASN27T1 | 2.7 V |  | DAA |  |  |
| NCP1400ASN30T1 | 3.0 V |  | DAB |  |  |
| NCP1400ASN33T1 | 3.3 V |  | DAJ |  |  |
| NCP1400ASN50T1 | 5.0 V |  | DAD |  |  |

NOTE: The ordering information lists six standard output voltage device options. Additional devices with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage (Pin 2) | $\mathrm{V}_{\text {OUT }}$ | -0.3 to 6.0 | V |
| Input/Output Pins <br> LX (Pin 5) <br> LX Peak Sink Current | $\mathrm{V}_{\mathrm{LX}}$ | -0.3 to 6.0 |  |
| CE (Pin 1) <br> Input Voltage Range <br> Input Current Range | $\mathrm{ILX}_{\mathrm{LX}}$ | 400 | V |
| Thermal Resistance Junction to Air | $\mathrm{V}_{\mathrm{CE}}$ | -0.3 to 6.0 | mA |
| Operating Ambient Temperature Range (Note 2) | $\mathrm{I}_{\mathrm{CE}}$ | -150 to 150 | V |
| Operating Junction Temperature Range | $\mathrm{R}_{\text {日JA }}$ | 250 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |

## NOTES:

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\pm 2.0 \mathrm{kV}$ per JEDEC standard: JESD22-A114.
Machine Model (MM) $\pm 200$ V per JEDEC standard: JESD22-A115.
2. The maximum package power dissipation limit must not be exceeded.

$$
P D=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

3. Latch-up Current Maximum Rating: $\pm 150 \mathrm{~mA}$ per JEDEC standard: JESD78.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Frequency ( $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SET }} \times 0.96$, Note 5) | fosc | 144 | 180 | 216 | kHz |
| Frequency Temperature Coefficient ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\Delta f$ | - | 0.11 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| Maximum PWM Duty Cycle ( $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SET }} \times 0.96$ ) | $\mathrm{D}_{\text {MAX }}$ | 68 | 75 | 82 | \% |
| Minimum Start-up Voltage ( $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {start }}$ | - | 0.8 | 0.95 | V |
| Minimum Start-up Voltage Temperature Coefficient ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{V}_{\text {start }}$ | - | -1.6 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Minimum Operation Hold Voltage ( $\mathrm{l}=0 \mathrm{~mA}$ ) | $V_{\text {hold }}$ | 0.3 | - | - | V |
| Soft-Start Time (V $\mathrm{V}_{\text {OUT }}>0.8 \mathrm{~V}$ ) | $\mathrm{t}_{\text {Ss }}$ | 0.5 | 2.0 | - | ms |

## LX (PIN 5)

| ```LX Pin On-State Sink Current ( \(\mathrm{V}_{\mathrm{LX}}=0.4 \mathrm{~V}\) ) Device Suffix: 19T1 25T1 27T1 30T1 33T1 50T1``` | ILX | $\begin{gathered} 80 \\ 80 \\ 100 \\ 100 \\ 100 \\ 100 \end{gathered}$ | $\begin{gathered} 90 \\ 120 \\ 125 \\ 130 \\ 135 \\ 160 \end{gathered}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \\ & - \end{aligned}$ | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Voltage Limit ( $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {CE }}=\mathrm{V}_{\text {SET }} \times 0.96, \mathrm{~V}_{\text {Lx }}$ "L" Side $)$ | $\mathrm{V}_{\text {LXLIM }}$ | 0.65 | 0.8 | 1.0 | V |
| Off-State Leakage Current ( $\mathrm{V}_{\mathrm{LX}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | ILKG | - | 0.5 | 1.0 | $\mu \mathrm{A}$ |

CE (PIN 1)

| CE Input Voltage $\left(\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SET }} \times 0.96\right)$ High State, Device Enabled Low State, Device Disabled | $\mathrm{V}_{\text {CE(high) }}$ <br> $\mathrm{V}_{\mathrm{CE} \text { (low) }}$ | 0.9 |  | - 0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CE Input Current (Note 6) <br> High State, Device Enabled ( $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\mathrm{CE}}=5.0 \mathrm{~V}$ ) <br> Low State, Device Disabled (VOUT $=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=0 \mathrm{~V}$ ) | $I_{C E(\text { high })}$ ICE(low) | $\begin{aligned} & -0.5 \\ & -0.5 \end{aligned}$ | $\begin{gathered} 0 \\ 0.15 \end{gathered}$ | 0.5 0.5 | $\mu \mathrm{A}$ |

TOTAL DEVICE

| $\begin{aligned} & \text { Output Voltage }\left(\mathrm{V}_{\text {in }}>0.8 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=4.0 \mathrm{~mA}\right) \\ & \text { Device Suffix: } \\ & \text { 19T1 } \\ & \text { 25T1 } \\ & \text { 27T1 } \\ & \text { 30T1 } \\ & \text { 33T1 } \\ & \text { 50T1 } \end{aligned}$ | $\mathrm{V}_{\text {OUT }}$ | $\begin{aligned} & 1.853 \\ & 2.438 \\ & 2.633 \\ & 2.925 \\ & 3.218 \\ & 4.875 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 2.5 \\ & 2.7 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.948 \\ & 2.563 \\ & 2.768 \\ & 3.075 \\ & 3.383 \\ & 5.125 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ```Output Voltage Temperature Coefficient (T}\mp@subsup{\textrm{T}}{\textrm{A}}{=-4\mp@subsup{0}{}{\circ}\textrm{C}\mathrm{ to +85}\mp@subsup{}{}{\circ}\textrm{C}) Device Suffix: 19T1 25T1 27T1 30T1 33T1 50T1``` | $\Delta \mathrm{V}_{\text {OUT }}$ |  | $\begin{aligned} & 100 \\ & 100 \\ & 100 \\ & 100 \\ & 100 \\ & 150 \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | ppm/ ${ }^{\circ} \mathrm{C}$ |
| Operating Current $2\left(\mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\text {CE }}=\mathrm{V}_{\text {SET }}+0.5 \mathrm{~V}\right.$, Note 5) | $\mathrm{I}_{\mathrm{DD} 2}$ | - | 7.0 | 15 | $\mu \mathrm{A}$ |
| Off-State Current ( $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, Note 6) | IOFF | - | 0.6 | 1.5 | $\mu \mathrm{A}$ |
| ```Operating Current \(1\left(\mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\text {CE }}=\mathrm{V}_{\text {SET }} \times 0.96\right.\), fosc \(\left.=180 \mathrm{kHz}\right)\) Device Suffix: 19T1 25T1 27T1 30T1 33T1 50T1``` | $l_{\text {DD1 }}$ | - | $\begin{aligned} & 23 \\ & 32 \\ & 32 \\ & 37 \\ & 37 \\ & 70 \end{aligned}$ | $\begin{gathered} 50 \\ 60 \\ 60 \\ 60 \\ 60 \\ 100 \\ \hline \end{gathered}$ | $\mu \mathrm{A}$ |

5. $\mathrm{V}_{\text {SET }}$ means setting of output voltage.
6. CE pin is integrated with an internal $10 \mathrm{M} \Omega$ pull-up resistor.


Figure 2. NCP1400ASN19T1 Output Voltage vs. Output Current


Figure 4. NCP1400ASN50T1 Output Voltage vs. Output Current


Figure 6. NCP1400ASN30T1 Efficiency vs. Output Current


Figure 3. NCP1400ASN30T1 Output Voltage vs. Output Current


Figure 5. NCP1400ASN19T1 Efficiency vs. Output Current


Figure 7. NCP1400ASN50T1 Efficiency vs. Output Current


Figure 8. NCP1400ASNXXT1 Operating Current (lDD1) vs. Output Voltage


Figure 10. NCP1400ASN50T1 Current Consumption vs. Temperature


Figure 12. NCP1400ASN30T1 $\mathrm{V}_{\mathrm{Lx}}$ Voltage Limit vs. Temperature


Figure 9. NCP1400ASN30T1 Current Consumption vs. Temperature


Figure 11. NCP1400ASN19T1 $\mathrm{V}_{\mathrm{Lx}}$ Voltage Limit vs. Temperature


Figure 13. NCP1400ASN50T1 $\mathrm{V}_{\mathrm{LX}}$ Voltage Limit vs. Temperature


Figure 14. NCP1400ASN30T1 Output Voltage vs. Temperature


Figure 16. NCP1400ASN30T1 Oscillator Frequency vs. Temperature


Figure 18. NCP1400ASN30T1 Maximum Duty Cycle vs. Temperature


Figure 15. NCP1400ASN50T1 Output Voltage vs. Temperature


Figure 17. NCP1400ASN50T1 Oscillator Frequency vs. Temperature


TA, AMBIENT TEMPERATURE ( ${ }^{\circ} \mathrm{C}$ )
Figure 19. NCP1400ASN50T1 Maximum Duty Cycle vs. Temperature


Figure 20. NCP1400ASN30T1 Startup/Hold Voltage vs. Temperature


Figure 22. NCP1400ASN30T1 LX Pin On-State Current vs. Temperature


Figure 24. NCP1400ASNXXT1 LX Pin On-State Current vs. Output Voltage


Figure 21. NCP1400ASN50T1 Startup/Hold Voltage vs. Temperature


Figure 23. NCP1400ASN50T1 LX Pin On-State Current vs. Temperature


Figure 25. NCP1400ASNXXT1 LX Switch On-Resistance vs. Output Voltage


Figure 26. NCP1400ASN19T1 Operation Startup/Hold Voltage vs. Output Current


Figure 28. NCP1400ASN50T1 Operation Startup/Hold Voltage vs. Output Current


Figure 30. NCP1400ASN30T1 Ripple Voltage vs. Output Current


Figure 27. NCP1400ASN30T1 Operation Startup/Hold Voltage vs. Output Current


Figure 29. NCP1400ASN19T1 Ripple Voltage vs. Output Current


Figure 31. NCP1400ASN50T1 Ripple Voltage vs. Output Current

$\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA} ., \mathrm{L}=22 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$ 1. $\mathrm{V}_{\mathrm{LX}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\text {OUT }}, 20 \mathrm{mV} / \mathrm{div}$, AC coupled
3. $\mathrm{I}_{\mathrm{L}}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 32. Operating Waveforms (Medium Load)

$\mathrm{V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{~L}=22 \mu \mathrm{H}$

1. $\mathrm{V}_{\mathrm{OUT}}=1.9 \mathrm{~V}$ (AC coupled), $50 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~mA}$ to 30 mA

Figure 34. NCP1400ASN19T1
Load Transient Response

$\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~L}=22 \mu \mathrm{H}$

1. $\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$ (AC coupled), $50 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~mA}$ to 30 mA

Figure 36. NCP1400ASN30T1 Load Transient Response

$\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=25 \mathrm{~mA} ., \mathrm{L}=22 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$ 1. $\mathrm{V}_{\mathrm{LX}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\mathrm{OUT}}, 20 \mathrm{mV} / \mathrm{div}, \mathrm{AC}$ coupled
3. $\mathrm{I}_{\mathrm{L}}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 33. Operating Waveforms (Heavy Load)

$\mathrm{V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{~L}=22 \mu \mathrm{H}$

1. $\mathrm{V}_{\mathrm{OUT}}=1.9 \mathrm{~V}$ (AC coupled), $50 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}$ to 3.0 mA

Figure 35. NCP1400ASN19T1 Load Transient Response

$\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~L}=22 \mu \mathrm{H}$

1. $\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$ (AC coupled), $50 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}$ to 3.0 mA

Figure 37. NCP1400ASN30T1 Load Transient Response


Figure 38. NCP1400ASN50T1 Load Transient Response

$V_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~L}=22 \mu \mathrm{H}$

1. $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}$ (AC coupled), $50 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{l}_{\mathrm{O}}=30 \mathrm{~mA}$ to 3.0 mA

Figure 39. NCP1400ASN50T1 Load Transient Response


Figure 40. Representative Block Diagram

## PIN FUNCTION DESCRIPTION

| Pin \# | Symbol |  |
| :---: | :---: | :--- |
| 1 | CE | Chip Enable Pin <br> (1) The chip is enabled if a voltage equal to or greater than 0.9 V is applied. <br> (2) The chip is disabled if a voltage less than 0.3 V is applied. <br> (3) The chip is enabled if this pin is left floating. |
| 2 | OUT | Output voltage monitor pin and also the power supply pin for the device. |
| 3 | NC | No internal connection to this pin. |
| 4 | GND | Ground pin. |
| 5 | LX | External inductor connection pin to power switch drain. |

## DETAILED OPERATING DESCRIPTION

## Operation

The NCP1400A series are monolithic power switching regulators optimized for applications where power drain must be minimized. These devices operate as fixed frequency, voltage mode boost regulator and is designed to operate in the discontinuous conduction mode. Potential applications include low powered consumer products and battery powered portable products.

The NCP1400A series are low noise fixed frequency voltage-mode PWM DC-DC converters, and consist of soft-start circuit, feedback resistor, reference voltage, oscillator, loop compensation network, PWM control circuit, current limit circuit and power switch. Due to the on-chip feedback resistor and loop compensation network, the system designer can get the regulated output voltage from 1.8 V to 5.0 V with a small number of external components. The quiescent current is typically $32 \mu \mathrm{~A}$ $\left(\mathrm{V}_{\text {OUT }}=2.7 \mathrm{~V}\right)$, and can be further reduced to about $1.5 \mu \mathrm{~A}$ when the chip is disabled $\left(\mathrm{V}_{\mathrm{CE}}<0.3 \mathrm{~V}\right)$.

## Soft Start

There is a soft start circuit in NCP1400A. When power is applied to the device, the soft start circuit pumps up the output voltage to approximately 1.5 V at a fixed duty cycle, the level at which the converter can operate normally. What is more, the start-up capability with heavy loads is also improved.

## Oscillator

The oscillator frequency is internally set to 180 kHz at an accuracy of $\pm 20 \%$ and with low temperature coefficient of $0.11 \% /{ }^{\circ} \mathrm{C}$. Figures 16 and 17 illustrate oscillator frequency versus temperature.

## Regulated Converter Voltage (VOUT)

The Vout is set by an internal feedback resistor network. This is trimmed to a selected voltage from 1.8 V to 5.0 V range in 100 mV steps with an accuracy of $\pm 2.5 \%$.

## Compensation

The device is designed to operate in discontinuous conduction mode. An internal compensation circuit was designed to guarantee stability over the full input/output voltage and full output load range. Stability cannot be guaranteed in continuous conduction mode.

## Current Limit

The NCP1400A series utilizes cycle-by-cycle current limiting as a means of protecting the output switch MOSFET from overstress and preventing the small value inductor from saturation. Current limiting is implemented by monitoring the output MOSFET current build-up during conduction, and upon sensing an overcurrent conduction immediately turning off the switch for the duration of the oscillator cycle.

The voltage across the output MOSFET is monitored and compared against a reference by the VLX limiter. When the threshold is reached, a signal is sent to the PWM controller block to terminate the output switch conduction. The current limit threshold is typically set at 350 mA .

## Enable/Disable Operation

The NCP1400A series offer IC shutdown mode by chip enable pin (CE pin) to reduce current consumption. An internal pull-up resistor tied the CE pin to OUT pin by default, i.e., user can float the pin CE for permanent "On". When voltage at pin CE is equal or greater than 0.9 V , the chip will be enabled, which means the regulator is in normal operation. When voltage at pin CE is less than 0.3 V , the chip is disabled, which means IC is shutdown.
Important: DO NOT apply a voltage between 0.3 V to 0.9 V to pin CE as this voltage will place the IC into an undefined state and the IC may drain excessive current from the supply.

## APPLICATION CIRCUIT INFORMATION



Figure 41. Typical Step-Up Converter Application

## Step-up Converter Design Equations

General step-up DC-DC converter designed to operate in discontinuous conduction mode can be defined by:

| Calculation | Equation |
| :---: | :---: |
| D | $\frac{\mathrm{t}_{\text {on }}}{T}$ |
| $\mathrm{I}_{\mathrm{PK}}$ | $\frac{\mathrm{V}_{\text {in }} \mathrm{t}_{\text {on }}}{\mathrm{L}}$ |
| $\mathrm{I}_{\mathrm{O}}$ | $\frac{\left(\mathrm{V}_{\text {in }}\right)^{2}\left(\mathrm{t}_{\text {on }}\right)^{2 \mathrm{f}}}{2 \mathrm{~L}\left(\mathrm{~V}_{\text {out }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {in }}\right)}$ |

## NOTES:

D - Duty cycle
IPK - Peak inductor current
$\mathrm{I}_{\mathrm{O}}$ - Desired dc output current
$\mathrm{V}_{\text {in }}$ - Nominal operating dc input voltage
$V_{\text {out }}$ - Desired dc output voltage
$V_{F}$ - Diode forward voltage
Assume saturation voltage of the internal FET switch is negligible.

## External Component Selection

## Inductor

Inductance values between $18 \mu \mathrm{H}$ and $27 \mu \mathrm{H}$ are the best suitable values for NCP1400A. In general, smaller inductance values can provide larger peak inductor current and output current capability, and lower conversion efficiency, and vice versa. Select an inductor with smallest possible DCR, usually less than $1.0 \Omega$ to minimize loss. It is necessary to choose an inductor with saturation current greater than the peak current which the inductor will encounter in the application.

## Diode

The diode is the largest source of loss in DC-DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, $\mathrm{V}_{\mathrm{F}}$, and the reverse recovery time, trr. The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the $\mathrm{P}-\mathrm{N}$ junction. A schottky diode with the following characteristics is recommended:

Small forward voltage, $\mathrm{V}_{\mathrm{F}}<0.3 \mathrm{~V}$
Small reverse leakage current
Fast reverse recovery time/switching speed
Rated current larger than peak inductor current,

$$
\mathrm{I}_{\text {rated }}>\mathrm{I}_{\mathrm{PK}}
$$

Reverse voltage larger than output voltage,

$$
V_{\text {reverse }}>V_{\text {out }}
$$

## Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small ESR (Equivalent Series Resistance) Tantalum or ceramic capacitor with value of $10 \mu \mathrm{~F}$ should be suitable.

## Output Capacitor

The output capacitor is used for sustaining the output voltage when the internal MOSFET is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a $47 \mu \mathrm{~F}$ to $68 \mu \mathrm{~F}$ low ESR ( $0.15 \Omega$ to $0.30 \Omega$ ) Tantalum capacitor should be appropriate.

An evaluation board of NCP1400A has been made in the small size of $23 \mathrm{~mm} \times 20 \mathrm{~mm}$ and is shown in Figures 42 and 43. Please contact your ON Semiconductor representative
for availability. The evaluation board schematic diagram, the artwork and the silkscreen of the surface mount PCB are shown below:


Figure 42. NCP1400A PWM Step-up DC-DC Converter Evaluation Board Silkscreen


Figure 43. NCP1400A PWM Step-up DC-DC Converter Evaluation Board Artwork (Component Side)

Components Supplier

| Parts | Supplier | Part Number | Description | Phone |
| :--- | :--- | :--- | :--- | :---: |
| Inductor, L1 | Sumida Electric Co. Ltd. | CD54-220MC | Inductor $22 \mu \mathrm{H} / 1.11 \mathrm{~A}$ | $(852) 2880-6688$ |
| Schottky Diode, D1 | ON Semiconductor Corp. | MBR0520LT1 | Schottky Power Rectifier | $(852) 2689-0088$ |
| Output Capacitor, C2 | KEMET Electronics Corp. | T494D686K010AS | Low ESR Tantalum Capacitor <br> $68 \mu \mathrm{~F} / 10 \mathrm{~V}$ | $(852) 2305-1168$ |
| Input Capacitor, C1 | KEMET Electronics Corp. | T491C106K016AS | Low Profile Tantalum Capacitor <br> $10 \mu \mathrm{~F} / 16 \mathrm{~V}$ | (852) 2305-1168 |

## PCB Layout Hints

## Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise as shown in Figure 44, e.g.: C2 GND, C1 GND, and U1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

## Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve
efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g.: short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to Lx pin of U1
3. Trace from L1 to anode pin of D1
4. Trace from cathode pin of D1 to TP2

## Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.


Figure 44. NCP1400A Evaluation Board Schematic Diagram

## NCP1402

## 200 mA, PFM Step-Up Micropower Switching Regulator

The NCP1402 series are monolithic micropower step-up DC to DC converter that are specially designed for powering portable equipment from one or two cell battery packs.These devices are designed to start-up with a cell voltage of 0.8 V and operate down to less than 0.3 V . With only three external components, this series allow a simple means to implement highly efficient converters that are capable of up to 200 mA of output current at $\mathrm{V}_{\text {in }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.0 \mathrm{~V}$.

Each device consists of an on-chip PFM (Pulse Frequency Modulation) oscillator, PFM controller, PFM comparator, soft-start, voltage reference, feedback resistors, driver, and power MOSFET switch with current limit protection. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1402 device series are available in the Thin SOT-23-5 package with five standard regulated output voltages. Additional voltages that range from 1.8 V to 5.0 V in 100 mV steps can be manufactured.

## Features

- Extremely Low Start-Up Voltage of 0.8 V
- Operation Down to Less than 0.3 V
- High Efficiency $85 \%\left(\mathrm{~V}_{\text {in }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.0 \mathrm{~V}, 70 \mathrm{~mA}\right)$
- Low Operating Current of $30 \mu \mathrm{~A}\left(\mathrm{~V}_{\text {OUT }}=1.9 \mathrm{~V}\right)$
- Output Voltage Accuracy $\pm 2.5 \%$
- Low Converter Ripple with Typical 30 mV
- Only Three External Components Are Required
- Chip Enable Power Down Capability for Extended Battery Life
- Micro Miniature Thin SOT-23-5 Packages


## Typical Applications

- Cellular Telephones
- Pagers
- Personal Digital Assistants (PDA)
- Electronic Games
- Portable Audio (MP3)
- Camcorders
- Digital Cameras
- Handheld Instruments

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


SOT23-5
(TSOP-5, SC59-5) SN SUFFIX CASE 483

## PIN CONNECTIONS AND MARKING DIAGRAM



$$
\begin{aligned}
\mathrm{xxx} & =\text { Marking } \\
\mathrm{Y} & =\text { Year } \\
\mathrm{W} & =\text { Work Week } \\
& \text { (Top View) }
\end{aligned}
$$

## ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 1443 of this data sheet.


Figure 1. Typical Step-Up Converter Application


Figure 2. Representative Block Diagram

## PIN FUNCTION DESCRIPTIONS

| Pin \# | Symbol |  |
| :---: | :---: | :--- |
| 1 | CE | Chip Enable pin <br> (1) The chip is enabled if a voltage which is equal to or greater than 0.9 V is applied <br> (2) The chip is disabled if a voltage which is less than 0.3 V is applied <br> (3) The chip will be enabled if it is left floating |
| 2 | OUT | Output voltage monitor pin, also the power supply pin of the device |
| 3 | NC | No internal connection to this pin |
| 4 | GND | Ground pin |
| 5 | LX | External inductor connection pin to power switch drain |

ORDERING INFORMATION

| Device | Output Voltage | Device Marking | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCP1402SN19T1 | 1.9 V | DAU |  |  |
| NCP1402SN27T1 | 2.7 V | DAE | SOT23-5 | 3000 Units Per Reel |
| NCP1402SN30T1 | 3.0 V | DAF |  |  |
| NCP1402SN33T1 | 3.3 V | DAG |  |  |
| NCP1402SN50T1 | 5.0 V | DAH |  |  |

NOTE: The ordering information lists five standard output voltage device options. Additional device with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage (Pin 2) | $\mathrm{V}_{\text {OUT }}$ | 6.0 | V |
| Input/Output Pins <br> LX (Pin 5) <br> LX Peak Sink Current | $\mathrm{V}_{\mathrm{LX}}$ | -0.3 to 6.0 |  |
| CE (Pin 1) | $\mathrm{I}_{\mathrm{LX}}$ | 400 | V |
| Input Voltage Range <br> Input Current Range | $\mathrm{V}_{\mathrm{CE}}$ | mA |  |
| Thermal Resistance Junction to Air | $\mathrm{I}_{\mathrm{CE}}$ | -0.3 to 6.0 |  |
| Operating Ambient Temperature Range (Note 2) | $\mathrm{R}_{\text {өJA }}$ | V |  |
| Operating Junction Temperature Range to 150 | mA |  |  |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## NOTES:

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\pm 2.0$ kV per JEDEC standard: JESD22-A114.
Machine Model (MM) $\pm 200$ V per JEDEC standard: JESD22-A115.
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

3. Latch-up Current Maximum Rating: $\pm 150 \mathrm{~mA}$ per JEDEC standard: JESD78.
4. Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Switch On Time (current limit not asserted) | $\mathrm{t}_{\text {on }}$ | 3.6 | 5.5 | 7.6 | $\mu \mathrm{s}$ |
| Switch Minimum Off Time | $\mathrm{t}_{\text {off }}$ | 1.0 | 1.45 | 1.9 | $\mu \mathrm{s}$ |
| Maximum Duty Cycle | $\mathrm{D}_{\text {MAX }}$ | 70 | 78 | 85 | \% |
| Minimum Start-up Voltage ( $\mathrm{l}_{\mathrm{O}}=0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {start }}$ | - | 0.8 | 0.95 | V |
| Minimum Start-up Voltage Temperature Coefficient ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{V}_{\text {start }}$ | - | -1.6 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Minimum Operation Hold Voltage ( $\mathrm{l}_{0}=0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {hold }}$ | 0.3 | - | - | V |
| Soft-Start Time (V $\mathrm{V}_{\text {OUT }}>0.8 \mathrm{~V}$ ) | $\mathrm{t}_{\text {SS }}$ | 0.3 | 2.0 | - | ms |

LX (PIN 5)

| Internal Switching N-Channel FET Drain Voltage | $\mathrm{V}_{\mathrm{LX}}$ | - | - | 6.0 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| LX Pin On-State Sink Current (V $\mathrm{LX}=0.4 \mathrm{~V})$ | ILX |  |  |  | mA |
| Device Suffix: |  |  |  |  |  |
| 19T1 |  | 110 | 145 | - |  |
| 27T1 |  | 130 | 180 | - |  |
| 30T1 |  | 130 | 190 | - |  |
| 33T1 |  | 130 | 200 | - |  |
| 50T1 |  | 215 | - |  |  |
| Voltage Limit | $\mathrm{V}_{\mathrm{LXLIM}}$ | 0.45 | 0.65 | 0.9 | V |
| Off-State Leakage Current $\left(\mathrm{V}_{\mathrm{LX}}=6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $\left.85^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{LKG}}$ | - | 0.5 | 1.0 | $\mu \mathrm{~A}$ |

CE (PIN 1)

| CE Input Voltage (VOUT $=\mathrm{V}_{\text {SET }} \times 0.96$ ) High State, Device Enabled Low State, Device Disabled | $\mathrm{V}_{\mathrm{CE} \text { (high) }}$ <br> $\mathrm{V}_{\mathrm{CE}(\text { low })}$ | 0.9 |  | - ${ }^{-}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CE Input Current (Note 6) High State, Device Enabled ( $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\mathrm{CE}}=6.0 \mathrm{~V}$ ) Low State, Device Disabled (VOUT $=6.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=0 \mathrm{~V}$ ) | $I_{\text {CE(high) }}$ ICE(low) | $\begin{aligned} & -0.5 \\ & -0.5 \end{aligned}$ | $\begin{gathered} 0 \\ 0.15 \end{gathered}$ | 0.5 0.5 | $\mu \mathrm{A}$ |

TOTAL DEVICE

| Output Voltage  <br> Device Suffix: Vout |  |  |  |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| 19T1 |  | 1.853 | 1.9 | 1.948 |  |
| $27 T 1$ |  | 2.632 | 2.7 | 2.768 |  |
| 30T1 |  | 2.925 | 3.0 | 3.075 |  |
| 33 T 1 |  | 3.218 | 3.3 | 3.383 |  |
| 50T1 |  | 4.875 | 5.0 | 5.125 |  |
| Output Voltage Temperature Coefficient ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$ Device Suffix: | $\Delta \mathrm{V}_{\text {OUT }}$ | Device Suffix: |  |  | ppm $/{ }^{\circ} \mathrm{C}$ |
| 19T1 |  | - | 150 | - |  |
| $27 T 1$ |  | - | 150 | - |  |
| 30T1 |  | - | 150 | - |  |
| 33T1 |  | - | 150 | - |  |
| 50T1 |  | - | 150 | - |  |
| Operating Current $2\left(\mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\text {CE }}=\mathrm{V}_{\text {SET }}+0.5 \mathrm{~V}\right.$, Note 5) | $\mathrm{I}_{\text {DD2 }}$ | - | 13 | 15 | $\mu \mathrm{A}$ |
| Off-State Current ( $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, Note 6) | IOFF | - | 0.6 | 1.0 | $\mu \mathrm{A}$ |
| Operating Current $1\left(\mathrm{~V}_{\text {OUT }}=\mathrm{V}_{\text {CE }}=\mathrm{V}_{\text {SET }} \times 0.96\right)$ | $\mathrm{I}_{\mathrm{DD} 1}$ |  |  |  | $\mu \mathrm{A}$ |
| Device Suffix: |  |  |  |  |  |
| 19T1 |  | - | 30 | 50 |  |
| $27 T 1$ |  | - | 39 | 60 |  |
| 30 T 1 |  | - | 42 | 60 |  |
| 33 T 1 |  | _ | 45 | 60 |  |
| 50T1 |  | - | 70 | 100 |  |

5. $\mathrm{V}_{\text {SET }}$ means setting of output voltage.
6. CE pin is integrated with an internal $10 \mathrm{M} \Omega$ pull-up resistor.


Figure 3. NCP1402SN19T1 Output Voltage vs. Output Current


Figure 5. NCP1402SN50T1 Output Voltage vs. Output Current


Figure 7. NCP1402SN30T1 Efficiency vs. Output Current


Figure 4. NCP1402SN30T1 Output Voltage vs. Output Current


Figure 6. NCP1402SN19T1 Efficiency vs.
Output Current

Figure 8. NCP1402SN50T1 Efficiency vs. Output Current


Figure 9. NCP1402SN19T1 Output Voltage vs. Temperature


Figure 11. NCP1402SN50T1 Output Voltage vs. Temperature


Figure 13. NCP1402SN30T1 Operating Current 1 vs. Temperature


Figure 10. NCP1402SN30T1 Output Voltage vs. Temperature


Figure 12. NCP1402SN19T1 Operating Current 1 vs. Temperature


Figure 14. NCP1402SN50T1 Operating Current 1 vs. Temperature


Figure 15. NCP1402SN19T1 Switch On Time vs. Temperature


Figure 17. NCP1402SN50T1 Switch On Time vs. Temperature


Figure 19. NCP1402SN30T1 Minimum Switch Off Time vs. Temperature


Figure 16. NCP1402SN30T1 Switch On Time vs. Temperature


Figure 18. NCP1402SN19T1 Minimum Switch Off Time vs. Temperature


Figure 20. NCP1402SN50T1 Minimum Switch Off Time vs. Temperature


Figure 21. NCP1402SN19T1 Maximum Duty Cycle vs. Temperature


Figure 23. NCP1402SN50T1 Maximum Duty Cycle vs. Temperature


Figure 25. NCP1402SN30T1 LX Pin On-State Current vs. Temperature


Figure 22. NCP1402SN30T1 Maximum Duty Cycle vs. Temperature


Figure 24. NCP1402SN19T1 LX Pin On-State Current vs. Temperature


Figure 26. NCP1402SN50T1 LX Pin On-State Current vs. Temperature


Figure 27. NCP1402SN19T1 VLx Voltage Limit vs. Temperature


Figure 29. NCP1402SN50T1 VLx Voltage Limit vs. Temperature


Figure 31. NCP1402SN30T1 Switch-on Resistance vs. Temperature


Figure 28. NCP1402SN30T1 VLx Voltage Limit vs. Temperature


Figure 30. NCP1402SN19T1 Switch-on Resistance vs. Temperature


Figure 32. NCP1402SN50T1 Switch-on Resistance vs. Temperature


Figure 33. NCP1402SN19T1 Startup/Hold Voltage vs. Temperature


Figure 35. NCP1402SN50T1 Startup/Hold Voltage vs. Temperature


Figure 37. NCP1402SN30T1 Startup/Hold Voltage vs. Output Current


Figure 34. NCP1402SN30T1 Startup/Hold Voltage vs. Temperature


Figure 36. NCP1402SN19T1 Startup/Hold Voltage vs. Output Current


Figure 38. NCP1402SN50T1 Startup/Hold Voltage vs. Output Current

$\mathrm{V}_{\text {OUT }}=1.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\mathrm{LX}}, 1.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\mathrm{OUT}}, 20 \mathrm{mV} /$ div, AC coupled
3. $\mathrm{I}_{\mathrm{L}}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 39. NCP1402SN19T1 Operating Waveforms (Medium Load)

$\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\mathrm{LX}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\mathrm{OUT}}, 20 \mathrm{mV} / \mathrm{div}, \mathrm{AC}$ coupled
3. $I_{L}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 41. NCP1402SN30T1 Operating Waveforms (Medium Load)

$\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=30 \mathrm{~mA}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\mathrm{LX}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\text {OUT }}, 20 \mathrm{mV} /$ div, AC coupled
3. $\mathrm{I}_{\mathrm{L}}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 43. NCP1402SN50T1 Operating Waveforms (Medium Load)

$\mathrm{V}_{\text {OUT }}=1.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=70 \mathrm{~mA}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$ 1. $\mathrm{V}_{\mathrm{LX}}, 1.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\text {OUT }}, 20 \mathrm{mV} /$ div, AC coupled
3. $I_{L}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 40. NCP1402SN19T1 Operating Waveforms (Heavy Load)

$\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=70 \mathrm{~mA}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$ 1. $\mathrm{V}_{\mathrm{LX}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\text {OUT }}, 20 \mathrm{mV} /$ div, AC coupled
3. $\mathrm{L}_{\mathrm{L}}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 42. NCP1402SN30T1 Operating Waveforms (Heavy Load)

$\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=60 \mathrm{~mA}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\mathrm{LX}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{V}_{\text {OUT }}, 20 \mathrm{mV} / \mathrm{div}, \mathrm{AC}$ coupled
3. $\mathrm{I}_{\mathrm{L}}, 100 \mathrm{~mA} / \mathrm{div}$

Figure 44. NCP1402SN50T1 Operating Waveforms (Heavy Load)


Figure 45. NCP1402SN19T1 Load Transient Response

$\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$ (AC coupled), $100 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~mA}$ to 80 mA

Figure 47. NCP1402SN30T1 Load Transient Response

$\mathrm{V}_{\text {in }}=2.4 \mathrm{~V}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUt }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}$ (AC coupled), $100 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~mA}$ to 80 mA

Figure 49. NCP1402SN50T1 Load Transient Response

$\mathrm{V}_{\text {in }}=1.2 \mathrm{~V}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUt }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\text {OUT }}=1.9 \mathrm{~V}$ (AC coupled), $100 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=80 \mathrm{~mA}$ to 0.1 mA

Figure 46. NCP1402SN19T1 Load Transient Response

$V_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}$ (AC coupled), $100 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=80 \mathrm{~mA}$ to 0.1 mA

Figure 48. NCP1402SN30T1 Load Transient Response

$\mathrm{V}_{\text {in }}=2.4 \mathrm{~V}, \mathrm{~L}=47 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=68 \mu \mathrm{~F}$

1. $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}$ (AC coupled), $100 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}=80 \mathrm{~mA}$ to 0.1 mA

Figure 50. NCP1402SN50T1 Load Transient Response


Figure 51. NCP1402SN19T1 Ripple Voltage vs. Output Current


Figure 53. NCP1402SN50T1 Ripple Voltage vs. Output Current


Figure 55. NCP1402SNXXT1 Pin On-state Current vs. Output Voltage


Figure 52. NCP1402SN30T1 Ripple Voltage vs. Output Current


Figure 54. NCP1402SNXXT1 Operating Current 1 vs. Output Voltage


Figure 56. NCP1402SNXXT1 Switch-On Resistance vs. Output Voltage


Figure 57. NCP1402SNXXT1 No Load Input Current vs. Input Voltage

## DETAILED OPERATING DESCRIPTION

## Operation

The NCP1402 series are monolithic power switching regulators optimized for applications where power drain must be minimized. These devices operate as variable frequency, voltage mode boost regulators and designed to operate in continuous conduction mode. Potential applications include low powered consumer products and battery powered portable products.

The NCP1402 series are low noise variable frequency voltage-mode DC-DC converters, and consist of soft-start circuit, feedback resistor, reference voltage, oscillator, PFM comparator, PFM control circuit, current limit circuit and power switch. Due to the on-chip feedback resistor network, the system designer can get the regulated output voltage from 1.8 V to 5 V with a small number of external components. The operating current is typically $30 \mu \mathrm{~A}$ $\left(\mathrm{V}_{\text {OUT }}=1.9 \mathrm{~V}\right)$, and can be further reduced to about $0.6 \mu \mathrm{~A}$ when the chip is disabled $\left(\mathrm{V}_{\mathrm{CE}}<0.3 \mathrm{~V}\right)$.

The NCP1402 operation can be best understood by examining the block diagram in Figure 2. PFM comparator monitors the output voltage via the feedback resistor. When the feedback voltage is higher than the reference voltage, the power switch is turned off. As the feedback voltage is lower than reference voltage and the power switch has been off for at least a period of minimum off-time decided by PFM oscillator, the power switch is then cycled on for a period of on-time also decided by PFM oscillator, or until current limit signal is asserted. When the power switch is on, current ramps up in the inductor, storing energy in the magnetic field. When the power switch is off, the energy in the magnetic field is transferred to output filter capacitor and the load. The output filter capacitor stores the charge while the inductor current is high, then holds up the output voltage until next switching cycle.


Figure 58. NCP1402SNXXT1 Maximum Output Current vs. Input Voltage

## Soft Start

There is a soft start circuit in NCP1402. When power is applied to the device, the soft start circuit pumps up the output voltage to approximately 1.5 V at a fixed duty cycle, the level at which the converter can operate normally. What is more, the start-up capability with heavy loads is also improved.

## Regulated Converter Voltage ( $\mathrm{V}_{\text {OUT }}$ )

The $\mathrm{V}_{\text {OUT }}$ is set by an internal feedback resistor network. This is trimmed to a selected voltage from 1.8 to 5.0 V range in 100 mV steps with an accuracy of $\pm 2.5 \%$.

## Current Limit

The NCP1402 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch MOSFET from overstress and preventing the small value inductor from saturation. Current limiting is implemented by monitoring the output MOSFET current build-up during conduction, and upon sensing an overcurrent conduction immediately turning off the switch for the duration of the oscillator cycle.

The voltage across the output MOSFET is monitored and compared against a reference by the VLX limiter. When the threshold is reached, a signal is sent to the PFM controller block to terminate the power switch conduction. The current limit threshold is typically set at 350 mA .

## Enable / Disable Operation

The NCP1402 series offer IC shut-down mode by chip enable pin (CE pin) to reduce current consumption. An internal pull-up resistor tied the CE pin to OUT pin by default i.e. user can float the pin CE for permanent "On". When voltage at pin CE is equal or greater than 0.9 V , the chip will be enabled, which means the regulator is in normal operation. When voltage at pin CE is less than 0.3 V , the chip is disabled, which means IC is shutdown.

Important: DO NOT apply a voltage between 0.3 V and 0.9 V to pin CE as this is the CE pin's hyteresis voltage range. Clearly defined output states can only be obtained by applying voltage out of this range.

## APPLICATIONS CIRCUIT INFORMATION



Figure 59. Typical Application Circuit

## Step-up Converter Design Equations

NCP1402 step-up DC-DC converter designed to operate in continuous conduction mode can be defined by:

| Calculation | Equation |
| :---: | :---: |
| L | $\leq \mathrm{M}\left(\frac{\mathrm{V}_{\text {in }}{ }^{2}}{\mathrm{~V}_{\text {OUT }} \text { IOmax }}\right)$ |
| IPK | $\frac{\left(V_{\text {in }}-V_{S}\right)^{t_{0 n}}}{L}+I_{\text {min }}$ |
| 1 min | $\frac{\left(t_{\text {on }}+t_{\text {off }}\right)_{\mathrm{O}}}{t_{\text {off }}}-\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{S}}\right) \mathrm{t}_{\mathrm{on}}}{2 \mathrm{~L}}$ |
| $\mathrm{t}_{\text {off }}$ | $\frac{\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{S}} \text { ton }^{\left(\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{F}}-\mathrm{V}_{\text {in }}\right)}\right.}{\text { ( }}$ |
| $\Delta \mathrm{Q}$ | $\left(\mathrm{L}_{\mathrm{L}}-\mathrm{l}_{\mathrm{O}}\right) \mathrm{t}_{\text {off }}$ |
| $\mathrm{V}_{\text {ripple }}$ | $\approx \frac{\Delta \mathrm{Q}}{\mathrm{COUT}}+(\mathrm{IL}-\mathrm{IO}) \mathrm{ESR}$ |

*NOTES:
lpK - Peak inductor current
$I_{\text {min }}$ - Minimum inductor current
Io - Desired dc output current
Iomax - Desired maximum dc output current
$I_{L}$ - Average inductor current
$V_{\text {in }}$ - Nominal operating dc input voltage
$V_{\text {OUT }}$ - Desired dc output voltage
$V_{F}$ - Diode forward voltage
$V_{S}$ - Saturation voltage of the internal FET switch
$\Delta$ Q - Charge stores in the Cout during charging up
$\mathrm{V}_{\text {ripple }}$ - Output ripple voltage
ESR - Equivalent series resistance of the output capacitor
M - An empirical factor, when $\mathrm{V}_{\text {OUT }} \geq 3.0 \mathrm{~V}$,
$M=8 \times 10^{-6}$, otherwise $M=5.3 \times 10^{-6}$.

## EXTERNAL COMPONENT SELECTION

## Inductor

The NCP1402 is designed to work well with a $47 \mu \mathrm{H}$ inductor in most applications. $47 \mu \mathrm{H}$ is a sufficiently low value to allow the use of a small surface mount coil, but large
enough to maintain low ripple. Low inductance values supply higher output current, but also increase the ripple and reduce efficiency. Note that values below $27 \mu \mathrm{H}$ is not recommended due to NCP1402 switch limitations. Higher inductor values reduce ripple and improve efficiency, but also limit output current.
The inductor should have small DCR, usually less than 1 $\Omega$ to minimize loss. It is necessary to choose an inductor with saturation current greater than the peak current which the inductor will encounter in the application.

## Diode

The diode is the main source of loss in DC-DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, $\mathrm{V}_{\mathrm{F}}$, and the reverse recovery time, $\mathrm{t}_{\mathrm{rr}}$. The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the $\mathrm{P}-\mathrm{N}$ junction. A Schottky diode with the following characteristics is recommended:

Small forward voltage, $\mathrm{V}_{\mathrm{F}}<0.3 \mathrm{~V}$
Small reverse leakage current
Fast reverse recovery time/ switching speed
Rated current larger than peak inductor current,
$\mathrm{I}_{\text {rated }}>\mathrm{I}_{\mathrm{PK}}$
Reverse voltage larger than output voltage,
$\mathrm{V}_{\text {reverse }}>\mathrm{V}_{\text {OUT }}$

## Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small ESR (Equivalent Series Resistance) Tantalum or ceramic capacitor with value of $10 \mu \mathrm{~F}$ should be suitable.

## Output Capacitor

The output capacitor is used for sustaining the output voltage when the internal MOSFET is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a 47 uF to 68 uF low ESR ( $0.15 \Omega$ to $0.30 \Omega$ ) Tantalum capacitor should be appropriate. For applications where space is a critical factor, two parallel 22 uF low profile SMD ceramic capacitors can be used.

An evaluation board of NCP1402 has been made in the size of $23 \mathrm{~mm} \times 20 \mathrm{~mm}$ only, as shown in Figures 60 and 61. Please contact your ON Semiconductor representative for availability. The evaluation board schematic diagram, the artwork and the silkscreen of the surface-mount PCB are shown below:


Figure 60. NCP1402 PFM Step-Up DC-DC Converter Evaluation Board Silkscreen


Figure 61. NCP1402 PFM Step-Up DC-DC Converter Evaluation Board Artwork (Component Side)

## Components Supplier

| Parts | Supplier | Part Number | Description | Phone |
| :--- | :--- | :---: | :--- | :---: |
| Inductor, L1 | Sumida Electric Co. Ltd. | CD54-470L | Inductor 47 $\mu \mathrm{H} / 0.72 \mathrm{~A}$ | $(852)-2880-6688$ |
| Schottky Diode, D1 | ON Semiconductor Corp. | MBR0520LT1 | Schottky Power Rectifier | $(852)-2689-0088$ |
| Output Capacitor, C2 | KEMET Electronics Corp. | T494D686K010AS | Low ESR Tantalum Capacitor <br> $68 ~ \mu \mathrm{~F} / 10 \mathrm{~V}$ | $(852)-2305-1168$ |
| Input Capacitor, C1 | KEMET Electronics Corp. | T491C106K016AS | Low Profile Tantalum Capacitor <br> $10 \mu \mathrm{~F} / 16 \mathrm{~V}$ | (852)-2305-1168 |

## PCB Layout Hints

## Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise as shown in Figure 62, e.g. : C2 GND, C1 GND, and U1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

## Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve
efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g. : short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to Lx pin of U1
3. Trace from L1 to anode pin of D1
4. Trace from cathode pin of D1 to TP2

## Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.


Figure 62. NCP1402 Evaluation Board Schematic Diagram

## NCP1410

## 250 mA Sync-Rect PFM Step-Up DC-DC Converter with Low-Battery Detector

NCP1410 is a monolithic micropower high frequency Boost (step-up) voltage switching converter IC specially designed for battery operated hand-held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz ) allows low profile inductor and output capacitor being used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. With all these functions ON, the device quiescent supply current is only $9.0 \mu \mathrm{~A}$ typical. This device is available in space saving compact Micro8 package.

## Features

- High Efficiency up to $92 \%$
- Very Low Device Quiescent Supply Current of $9.0 \mu \mathrm{~A}$ Typical
- Allows use of Small Size Inductor and Capacitor
- Built-in Synchronous Rectifier (PFET) Eliminates One External Schottky Diode
- High Switching Frequency (up to 600 kHz ) Allows Use of Small Size Inductor and Capacitor
- High Accuracy Reference Output, $1.19 \mathrm{~V} \pm 0.6 \%$ @ $25^{\circ} \mathrm{C}$, can supply more than 2.5 mA when $\mathrm{V}_{\text {OUT }} \geq 3.3 \mathrm{~V}$
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.5 V Adjustable
- Output Current up to $250 \mathrm{~mA} @ \mathrm{~V}_{\text {in }}=2.5 \mathrm{~V}, \mathrm{~V}_{\text {out }}=3.3 \mathrm{~V}$
- Logic-Controlled Shutdown
- Open Drain Low-Battery Detector Output
- 1.0 A Cycle-by-Cycle Current Limit
- Low Profile and Minimum External Parts
- Compact Micro8 Package


## Typical Applications

- Personal Digital Assistant (PDA)
- Handheld Digital Audio Product
- Camcorders and Digital Still Camera
- Hand-held Instrument
- Conversion from One or Two NiMH or NiCd, or One Li-ion Cell to 3.3 V/5.0 V


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


Micro8 DM SUFFIX CASE 846A

A1 = Device Marking
A = Assembly Location
Y = Year
W = Work Week

## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP1410DMR2 | Micro8 | 4000 Tape \& Reel |



Figure 1. Typical Operating Circuit

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Device Power Supply (Pin 8) | $\mathrm{V}_{\text {OUT }}$ | -0.3 to 6.0 | V |
| Input/Output Pins Pin 1-5, Pin 7 | $\mathrm{V}_{10}$ | -0.3 to 6.0 | V |
| Thermal Characteristics <br> Micro8 Plastic Package Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance Junction to Air | $P_{D}$ $\mathrm{R}_{\theta \mathrm{JA}}$ | $\begin{aligned} & 520 \\ & 240 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\text {A }}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\pm 2.0 \mathrm{kV}$ per JEDEC standard: JESD22-A114.
Machine Model Method (MM) $\pm 200$ V per JEDEC standard: JESD22-A115.
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

3. Latch-up Current Maximum Rating: $\pm 150 \mathrm{~mA}$ per JEDEC standard: JESD78.
4. Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

ELECTRICAL CHARACTERISTICS (VOUT $=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for typical value, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ for min/max values unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Voltage | $\mathrm{V}_{\text {IN }}$ | 1.0 | - | 5.5 | V |
| Output Voltage Range (Adjusted by external feedback) | $\mathrm{V}_{\text {OUT }}$ | $\mathrm{V}_{\text {IN }}$ | - | 5.5 | V |
| Reference Voltage ( $\mathrm{C}_{\text {REF }}=150 \mathrm{nF}$, under no loading, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {REF_NL }}$ | 1.183 | 1.190 | 1.197 | V |
| Reference Voltage ( $\mathrm{C}_{\text {REF }}=150 \mathrm{nF}$, under no loading, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ ) | V ${ }_{\text {EEF_NL_A }}$ | 1.178 | - | 1.202 | V |
| Reference Voltage Temperature Coefficient | TC Vref | - | 0.03 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Reference Voltage Load Current }\left(\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V},\right. \\ & \left.\mathrm{V}_{\text {REF }}=\mathrm{V}_{\text {REF_NL }} \pm 1.5 \%, \mathrm{C}_{\text {REF }}=1.0 \mu \mathrm{~F}\right)(\text { Note } 5) \end{aligned}$ | $\mathrm{I}_{\text {REF }}$ | 2.5 | - | - | mA |
| $\begin{aligned} & \text { Reference Voltage Load Regulation }\left(\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}\right. \text {, } \\ & \left.\mathrm{I}_{\text {REF }}=0 \text { to } 100 \mu \mathrm{~A}, \mathrm{C}_{\text {REF }}=1.0 \mu \mathrm{~F}\right) \end{aligned}$ | $\mathrm{V}_{\text {REF_LOAD }}$ | - | 0.015 | 1.0 | mV |
| Reference Voltage Line Regulation ( $\mathrm{V}_{\text {OUT }}$ from 1.5 V to 5.5 V , $\left.C_{R E F}=1.0 \mu \mathrm{~F}\right)$ | $\mathrm{V}_{\text {REF_LINE }}$ | - | 0.03 | 1.0 | mV/V |
| FB, LBI Input Threshold ( ${ }_{\text {LOAD }}=0 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\text {LBI }}$ | 1.174 | 1.190 | 1.200 | V |
| N-FET ON Resistance | RDS(ON)-N |  | 0.6 |  | $\Omega$ |
| P-FET ON Resistance | $\mathrm{R}_{\mathrm{DS} \text { (ON)-P }}$ |  | 0.9 |  | $\Omega$ |
| LX Switch Current Limit (NFET) | ILIM | - | 1.0 | - | A |
| Operating Current into OUT ( $\mathrm{V}_{\mathrm{FB}}=1.4 \mathrm{~V}$, i.e. No switching, $\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{Q}}$ | - | 9.0 | 14 | $\mu \mathrm{A}$ |
| Shutdown Current into OUT (SHDN = GND) | ISD | - | 0.05 | 1.0 | $\mu \mathrm{A}$ |
| LX Switch MAX. ON-Time ( $\mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ ) | ton | 1.2 | 1.4 | 1.8 | $\mu \mathrm{S}$ |
| LX Switch MIN. OFF-Time ( $\mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ ) | toff | 0.25 | 0.31 | 0.37 | $\mu \mathrm{S}$ |
| FB Input Current | $\mathrm{I}_{\text {FB }}$ | - | 1.5 | 9.0 | nA |
| LBI Input Current | lıBI | - | 1.5 | 8.0 | nA |
| LBO Low Output Voltage ( $\mathrm{V}_{\text {LBI }}=0, \mathrm{I}_{\text {SINK }}=1.0 \mathrm{~mA}$ ) | VLBO_L | - | - | 0.05 | V |
| SHDN Input Current | ISHDN | - | 1.5 | 8.0 | nA |
| SHDN Input Threshold, Low | $\mathrm{V}_{\text {SHDN_L }}$ | - | - | 0.3 | V |
| SHDN Input Threshold, High | $\mathrm{V}_{\text {SHDN_H }}$ | 0.6 | - | - | V |

5. Loading capability increases with $\mathrm{V}_{\text {OUT }}$.

PIN FUNCTION DESCRIPTIONS

| Pin \# | Symbol | Pin Description |
| :---: | :---: | :--- |
| 1 | FB | Output Voltage Feedback Input. |
| 2 | LBI | Low-Battery Detector Input. |
| 3 | LBO | Open-Drain Low-Battery Detector Output. Output is LOW when $\mathrm{V}_{\text {LBI }}$ is $<1.178 \mathrm{~V}$. LBO is high <br> impedance during shutdown. |
| 4 | REF | 1.190 V Reference Voltage Output, bypass with 150 nF capacitor if this pin is not loaded, bypass with <br> $1.0 \mu \mathrm{~F}$ if this pin is loaded up to $2.5 \mathrm{~mA} @ \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$. |
| 5 | SHDN | Shutdown Input. HIGH ( $>0.6 \mathrm{~V}$ ) = operating; LOW $(<0.3 \mathrm{~V})=$ shutdown. |
| 6 | GND | Ground. |
| 7 | LX | N-Channel and P-Channel Power MOSFET Drain Connection. |
| 8 | OUT | Power Output. OUT provides bootstrap power to the IC. |



Figure 2. Simplified Functional Diagram

## TYPICAL OPERATING CHARACTERISTICS



Figure 3. Reference Voltage vs. Output Current


Figure 5. Reference Voltage vs. Temperature


Figure 7. $\mathrm{L}_{\mathrm{x}}$ Switch Maximum ON Time vs. Temperature


Figure 4. Reference Voltage vs. Input Voltage at OUT pin


Figure 6. Switch ON Resistance vs. Temperature


Figure 8. Minimum Startup Battery Voltage vs. Loading Current


Figure 9. Efficiency vs. Load Current


Figure 11. Efficiency vs. Load Current


Figure 13. Efficiency vs. Load Current


Figure 10. Efficiency vs. Load Current


Figure 12. Efficiency vs. Load Current


Figure 14. Efficiency vs. Load Current

## TYPICAL OPERATING CHARACTERISTICS



Figure 15. Output Voltage Change vs. Load Current


Figure 17. Output Ripple Voltage vs. Battery Input Voltage


Figure 19. No Load Operating Current vs. Input Voltage at OUT Pin


Figure 16. Output Voltage Change vs. Load Current


Figure 18. Output Ripple Voltage vs. Battery Input Voltage
 Lower Trace: Shutdown Pin Waveform, 1.0 V/Division

Figure 20. Startup Transient Response

## TYPICAL OPERATING CHARACTERISTICS



Upper Trace: Voltage at $\mathrm{L}_{\mathrm{X}}$ pin, 2.0 V/Division MiddleTrace Otuput Voltage Ripple, $50 \mathrm{mV} /$ Division Lower Trace: Inductor Current, $\mathrm{I}_{\mathrm{L}}, 100 \mathrm{~mA} /$ Division
Figure 21. Continuous Conduction Mode Switching Waveform

$\left(\mathrm{V}_{\text {IN }}=1.8 \mathrm{~V}\right.$, to $\left.3.0 \mathrm{~V}, \mathrm{~L}=22 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=33 \mu \mathrm{~F}\right)$
Upper Trace: Battery Voltage, $\mathrm{V}_{\mathrm{IN}}, 1.0 \mathrm{~V} /$ Division Lower Trace: Output Voltage Ripple, $100 \mathrm{mV} /$ Division

Figure 23. Line Transient Response for $\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}$


Figure 25. Load Transient Response for $\mathrm{V}_{\mathrm{IN}}=2.4 \mathrm{~V}$


Figure 22. Discontinuous Conduction Mode Switching Waveform

( $V_{\text {OUT }}=3.3 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=10 \mathrm{~mA}$ to $100 \mathrm{~mA} ; \mathrm{L}=22 \mu \mathrm{H}$, Cout $=33 \mu \mathrm{~F}$ )
Upper Trace: Output Voltage Ripple, $100 \mathrm{mV} /$ Division Lower Trace: Load Current, ILOAD, $50 \mathrm{~mA} /$ Division
Figure 24. Load Transient Response for $\mathrm{V}_{\mathrm{IN}}=1.8 \mathrm{~V}$


Upper Trace: Output Voltage Ripple, $100 \mathrm{mV} /$ Division Lower Trace: Load Current, ILOAD, $50 \mathrm{~mA} /$ Division
Figure 26. Load Transient Response for $\mathrm{V}_{\mathrm{IN}}=3.3 \mathrm{~V}$

## DETAILED OPERATION DESCRIPTIONS

NCP1410 is a monolithic micropower high frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz ) allows low profile inductor and output capacitor being used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated application. With all these functions ON, the quiescent supply current is only $9.0 \mu \mathrm{~A}$ typical. This device is available in a compact Micro8 package.

## PFM Regulation Scheme

From the simplified Functional Diagram (Figure 2), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to REF. A switching cycle is initiated by the falling edge of the comparator, at the moment, the main switch (M1) is turned ON. After the maximum ON-time (typical $1.4 \mu \mathrm{~S}$ ) elapses or the current limit is reached, M1 is turned OFF, and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typical $0.31 \mu \mathrm{~S}$ ), this is to ensure energy transfer from the inductor to the output capacitor. If the regulator is operating at continuous conduction mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating at discontinuous conduction mode (DCM), which means the coil current will decrease to zero before the next cycle, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting, when the voltage drop is below the offset, the ZLC comparator output goes HIGH, and M2 is turned OFF. Negative feedback of closed loop operation regulates voltage at pin $1(\mathrm{FB})$ equal to the internal voltage reference (1.190 V).

## Synchronous Rectification

Synchronous Rectifier is used to replace Schottky Diode for eliminating the conduction loss contributed by forward voltage of the latter. Synchronous Rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns.

As main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M 2 is being turned ON .

When the main regulator is operating in CCM, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completed OFF, the above mentioned situation will occur. So dead time is introduced to make sure M2 is completed OFF before M1 is being turned ON.
When the regulator is operating in DCM, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So the ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.
With the implementation of synchronous rectification, efficiency can be as high as $92 \%$. For single cell input voltage, use an external Schottky diode such as MBR0520 connected from pin 7 to pin 8 to ensure start-up.

## Cycle-by-Cycle Current Limit

From Figure 2, SENSEFET is applied to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, sense-voltage is developed. Threshold detector (ILIM) detects whether the sense-voltage is higher than preset level. If it happens, detector output signifies the CONTROL LOGIC to switch OFF M1, and M1 can only be switched ON as next cycle starts after the minimum OFF-time (typical $0.31 \mu \mathrm{~S}$ ). With properly sizing of SENSEFET and sense resistor, the peak coil current limit is set at 1.0 A typically.

## Voltage Reference

The voltage at REF is set typically at +1.190 V . It can output up to 2.5 mA with load regulation $\pm 1.5 \%$, at $\mathrm{V}_{\text {OUT }}$ equal to 3.3 V . If $\mathrm{V}_{\text {OUT }}$ is increased, the REF load capability can also be increased. A bypass capacitor of $0.15 \mu \mathrm{~F}$ is required for proper operation when REF is not loaded. If REF is loaded, $1.0 \mu \mathrm{~F}$ capacitor at REF is needed.

## Shutdown

The IC is shutdown when the voltage at pin 5 ( $\overline{\mathrm{SHDN}}$ ) is pulled lower than 0.3 V . During shutdown, M1 and M2 are both switched OFF, however, the body diode of M2 allows current flow from battery to the output, the IC internal circuit will consume less than $0.05 \mu \mathrm{~A}$ current typically. If the pin 5 voltage is pull higher than 0.6 V , for example, by a resistor connected to VIN, the IC is enabled, and the internal circuit will only consume $9.0 \mu \mathrm{~A}$ current typically from the OUT pin. Refer to Figure 2, the product of $\mathrm{R}_{\text {SHDN }}$ and $\mathrm{C}_{\text {SHDN }}$ must be larger than ( $500 \mathrm{k} \cdot 56 \mathrm{nF}$, i.e. 28 msec ). This is to provide reset pulse for startup as battery is plugged in.

## Low-Battery Detection

A comparator with 30 mV hysteresis is applied to perform the low-battery detection function. When pin 2 (LBI) is at a voltage, which can be defined by a resistor divider from the battery voltage, lower than the internal reference voltage, 1.190 V , the comparator output will cause a 50 Ohm low side switch to be turned ON. It will pull down the voltage at pin 3 (LBO) which has a hundreds kilo-Ohm of pull-high resistance. If the pin 2 voltage is higher than $1.190 \mathrm{~V}+30$ mV , the comparator output will cause the 50 Ohm low side switch to be turned OFF, pin 3 will become high impedance, and its voltage will be pulled high by the external resistor.

## APPLICATIONS INFORMATION

## Output Voltage Setting

The output voltage of the converter is determined by the external feedback network comprised of $\mathrm{R}_{\mathrm{FB} 1}$ and $\mathrm{R}_{\mathrm{FB} 2}$ and the relationship is given by:

$$
\mathrm{V}_{\mathrm{OUT}}=1.190 \mathrm{~V} \times\left(1+\frac{\mathrm{R}_{\mathrm{FB} 1}}{\mathrm{R}_{\mathrm{FB} 2}}\right)
$$

where $R_{F 2}$ and $R_{F 1}$ are the upper and lower feedback resistors respectively.

## Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network comprised of $\mathrm{R}_{\mathrm{LB} 1}$ and $\mathrm{R}_{\mathrm{LB} 2}$ and the relationship is given by:

$$
\mathrm{V}_{\mathrm{LB}}=1.190 \mathrm{~V} \times\left(1+\frac{R_{\mathrm{LB} 1}}{R_{\mathrm{LB} 2}}\right)
$$

where $\mathrm{R}_{\mathrm{LB} 1}$ and $\mathrm{R}_{\mathrm{LB} 2}$ are the upper and lower divider resistors respectively.

## Inductor Selection

The NCP1410 is tested to produce optimum performance with a $22 \mu \mathrm{H}$ inductor at $\mathrm{V}_{\text {IN }}=3 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ supplying output current up to 250 mA . For other input/output requirements, inductance in the range $10 \mu \mathrm{H}$ to $47 \mu \mathrm{H}$ can be used according to end application specifications. Selecting an inductor is a compromise between output current capability and tolerable output voltage ripple. Of course, the first thing we need to obey is to keep the peak inductor current below its saturation limit at maximum current and the $\mathrm{I}_{\text {LIM }}$ of the device. In NCP1410, $\mathrm{I}_{\text {LIM }}$ is set at 1 A . As a rule of thumb, low inductance values supply higher output current, but also increase the ripple at output and reducing efficiency, on the other hand, high inductance values can improve output ripple and efficiency, however it also limit the output current capability at the same time. One other parameter of the inductor is its DC resistance, this resistance can introduce unwanted power loss and hence reduce overall efficiency, the basic rule is selecting an inductor with lowest DC resistance within the board space limitation of the end application.

## Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals sees pulsating voltage/current waveforms. The currents flowing into and out of the capacitors multiplying with the Equivalent Series Resistance (ESR) of the capacitor producing ripple voltage at the terminals. During the syn-rect switch off cycle, the charges stored in the output capacitor is used to sustain the output load current. Load current at this period and the ESR combined and reflected as ripple at the output terminals. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guide line, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as a cost effective substitute.

## Optional Startup Schottky Diode for Low Battery Voltage

In general operation, no external Schottky diode is required, however, in case you are intended to operate the device close to 1 V level, a Schottky diode connected between the LX and OUT pins as shown in Figure 27 can help during startup of the converter. The effect of the additional Schottky was shown in Figure 8.


Figure 27. Schottky Device Between LX and OUT Pins

## PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints in the following paragraphs, can be used as guidelines in most situations.

## Grounding

Star-ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high current running paths must be thick enough for current flowing through and producing insignificant voltage drop along the path. Feedback signal path must be separated with the main current path and sensing directly at the anode of the output capacitor.

## Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and thick. High current flowing and switching paths must be kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

## Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. External feedback network must be placed very close to the feedback (FB, pin 1) pin and sensing the output voltage directly at the anode of the output capacitor.

## TYPICAL APPLICATION CIRCUIT



Figure 28. Typical Application Schematic for 2 Alkaline Cells Supply

## GENERAL DESIGN PROCEDURES

Switching mode converter design is considered as black magic to most engineers, some complicate empirical formulae are available for reference usage. Those formulae are derived form the assumption that the key components, i.e. power inductor and capacitors are available with no tolerance. Practically, its not true, the result is not a matter of how accurate the equations you are using to calculate the component values, the outcome is still somehow away from the optimum point. In below a simple method base on the most basic first order equations to estimate the inductor and capacitor values for NCP1410 operate in Continuous Conduction Mode is introduced. The component value set can be used as a starting point to fine tune the circuit operation. By all means, detail bench testing is needed to get the best performance out of the circuit.

## Design Parameters:

$\mathrm{V}_{\mathrm{IN}}=1.8 \mathrm{~V}$ to 3.0 V , Typical 2.4 V
$\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}$
$\mathrm{I}_{\text {OUT }}=200 \mathrm{~mA}(250 \mathrm{~mA}$ max $)$
$\mathrm{V}_{\mathrm{LB}}=2.0 \mathrm{~V}$
$\mathrm{V}_{\text {OUT-RIPPLE }}=40 \mathrm{mV}_{\text {P-P }}$ at $\mathrm{I}_{\text {OUT }}=250 \mathrm{~mA}$
Calculate the feedback network:
Select $\mathrm{R}_{\mathrm{FB} 2}=200 \mathrm{~K}$

$$
\begin{aligned}
& R_{F B 1}=\operatorname{RFB2}\left(\frac{V_{\text {OUT }}}{V_{\text {REF }}}-1\right) \\
& R_{\text {FB1 }}=200 \mathrm{~K}\left(\frac{3.3 \mathrm{~V}}{1.19 \mathrm{~V}}-1\right)=355 \mathrm{~K}
\end{aligned}
$$

Calculate the Low Battery Detect divider:
$\mathrm{V}_{\mathrm{LB}}=2.0 \mathrm{~V}$
Select $\mathrm{R}_{\mathrm{LB} 2}=330 \mathrm{~K}$

$$
\begin{aligned}
& R_{\mathrm{LB} 1}=\mathrm{R}_{\mathrm{LB} 2}\left(\frac{\mathrm{~V}_{\mathrm{LB}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right) \\
& \mathrm{R}_{\mathrm{LB} 1}=330 \mathrm{~K}\left(\frac{2.0 \mathrm{~V}}{1.19 \mathrm{~V}}-1\right)=225 \mathrm{~K}
\end{aligned}
$$

Determine the Steady State Duty Ratio, D for typical $\mathrm{V}_{\mathrm{IN}}$, operation will be optimized around this point:

$$
\begin{gathered}
\frac{V_{\text {OUT }}}{V_{I N}}=\frac{1}{1-D} \\
D=1-\frac{V_{I N}}{V_{\text {OUT }}}=1-\frac{2.4 \mathrm{~V}}{3.3 \mathrm{~V}}=0.273
\end{gathered}
$$

Determine the average inductor current, $\mathrm{I}_{\mathrm{LAVG}}$ at maximum IOUT:

$$
\text { lLAVG }=\frac{\text { IOUT }}{1-D}=\frac{250 \mathrm{~mA}}{1-0.273}=344 \mathrm{~mA}
$$

Determine the peak inductor ripple current, $\mathrm{I}_{\text {RIPPLE-P }}$ and calculate the inductor value:

Assume $\mathrm{I}_{\text {RIPPLE-P }}$ is $20 \%$ of $\mathrm{I}_{\text {LAVG }}$, the inductance of the power inductor can be calculated as in below:

$$
\begin{aligned}
& \text { IRIPPLE-P }=0.20 \times 344 \mathrm{~mA}=68.8 \mathrm{~mA} \\
& \qquad L=\frac{\mathrm{VIN}_{\mathrm{IN}} \times \mathrm{tON}}{2 \mathrm{I}_{\text {RIPPLE }}-\mathrm{P}}=\frac{2.4 \mathrm{~V} \times 0.4 \mu \mathrm{~S}}{2(68.8 \mathrm{~mA})}=24.4 \mu \mathrm{H}
\end{aligned}
$$

Standard value of $22 \mu \mathrm{H}$ is selected for initial trial.
Determine the output voltage ripple, VOUT-RIPPLE and calculate the output capacitor value:
VOUT-RIPPLE $=40 \mathrm{mV}_{\text {P-P }}$ at $\mathrm{I}_{\text {OUT }}=250 \mathrm{~mA}$

$$
\text { COUT }>\frac{\text { IOUT } \times \text { tON }}{\text { VOUT-RIPPLE }- \text { IOUT } \times \text { ESRCOUT }}
$$

where $\mathrm{t}_{\mathrm{ON}}=1.4 \mu \mathrm{~S}$ and $\mathrm{ESR}_{\mathrm{COUT}}=0.1 \Omega$,

$$
\text { COUT }>\frac{250 \mathrm{~mA} \times 0.4 \mu \mathrm{~S}}{40 \mathrm{mV}-250 \mathrm{~mA} \times 0.1 \Omega}=23.33 \mu \mathrm{~F}
$$

From above calculation, you need at least $23.33 \mu \mathrm{~F}$ in order to achieve the specified ripple level at conditions stated. Practically, a one level larger capacitor will be used to accommodate factors not take into account in the calculation, therefore a capacitor value of $33 \mu \mathrm{~F}$ is selected.

## NCP1411

## Sync－Rect PFM Step－Up DC－DC Converter with Low－Battery Detector and Ring－Killer

NCP1411 is a monolithic micropower high frequency Boost （step－up）voltage switching converter IC specially designed for battery operated hand－held electronic products up to 250 mA loading． It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode．High switching frequency （up to 600 kHz ）allows low profile inductor and output capacitor being used．Low－Battery Detector，Logic－Controlled Shutdown and Cycle－by－Cycle Current Limit provide value－added features for various battery－operated applications．The innovative Ring－Killer circuitry guarantees quiet operation in discontinuous conduction mode．With all these functions ON，the device quiescent supply current is only $9.0 \mu \mathrm{~A}$ typical．This device is available in the space saving compact Micro8 ${ }^{\text {TM }}$ package．

## Features

－High Efficiency，up to $92 \%$
－Very Low Device Quiescent Supply Current of $9.0 \mu \mathrm{~A}$ Typical
－Built－in Synchronous Rectifier（P－FET）Eliminates One External Schottky Diode
－High Switching Frequency（up to 600 kHz ）Allows use of Small Size Inductor
－High Accuracy Reference Output， $1.19 \mathrm{~V} \pm 0.6 \%$＠ $25^{\circ} \mathrm{C}$ ，can supply more than 2.5 mA when $\mathrm{V}_{\text {OUT }} \geq 3.3 \mathrm{~V}$
－Ring－Killer for Quiet Operation in Discontinuous Conduction Mode
－ 1.0 V Startup at No Load Guaranteed
－Output Voltage from 1.5 V to 5.5 V Adjustable
－Output Current up to $250 \mathrm{~mA} @ \mathrm{~V}_{\mathrm{IN}}=2.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$
－Logic－Controlled Shutdown
－Open Drain Low－Battery Detector Output
－1．0 A Cycle by Cycle Current Limit
－Low Profile and Minimum External Parts
－Compact Micro8 Package

## Typical Applications

－Personal Digital Assistant（PDA）
－Handheld Digital Audio Product
－Camcorder and Digital Still Camera
－Handheld Instrument
－Conversion from One or Two NiMH or NiCd，or One Li－ion Cell to 3．3 V／5．0 V

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MARKING
DIAGRAM

| 日且且且 |
| :---: |
| A2 |
| AYW |
| $\bigcirc$ |

A2＝Device Marking
A＝Assembly Location
Y＝Year
W＝Wafer Lot

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP1411DMR2 | Micro8 | 4000 Tape \＆Reel |



Figure 1. Typical Operating Circuit

PIN FUNCTION DESCRIPTION

| Pin \# | Symbol | Pin Description |
| :---: | :---: | :--- |
| 1 | FB | Output Voltage Feedback Input. |
| 2 | LBI/EN | Low-Battery Detector Input and IC Enable. |
| 3 | LBO | Open-Drain Low-Battery Detector Output. Output is LOW when $\mathrm{V}_{\text {LBI }}$ is $<1.178 \mathrm{~V}$. LBO is high impedance <br> during shutdown. |
| 4 | REF | 1.190 V Reference Voltage Output, bypassing with 150 nF capacitor if this pin is not loaded, bypassing with <br> $1.0 \mu \mathrm{~F}$ if this pin is loaded up to $2.5 \mathrm{~mA} \mathrm{@} \mathrm{V} \mathrm{OUT}^{2}=3.3 \mathrm{~V}$. |
| 5 | BAT | Battery input connection for internal Ring-Killer. |
| 6 | GND | Ground. |
| 7 | LX | N-Channel and P-Channel Power MOSFET Drain Connection. |
| 8 | OUT | Power Output. OUT also provides bootstrapped power to the device. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Device Power Supply (Pin 8) | $\mathrm{V}_{\text {OUT }}$ | -0.3 to 6.0 | V |
| Input/Output Pins <br> Pins 1-5, Pin 7 | $\mathrm{V}_{\text {IO }}$ | -0.3 to 6.0 | V |
| Thermal Characteristics |  |  |  |
| Micro8 Plastic Package <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $\mathrm{P}_{\mathrm{D}}$ |  |  |
| Operating Junction Temperature Range | $\mathrm{R}_{\text {日JA }}$ | 520 | mW |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | 240 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. This device contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\pm 2.0 \mathrm{kV}$ per JEDEC standard: JESD22-A114.
Machine Model (MM) $\pm 200$ V per JEDEC standard: JESD22-A115.
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

3. Latch-up Current Maximum Rating: $\pm 150 \mathrm{~mA}$ per JEDEC standard: JESD78.
4. Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ for typical value, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ for min/max values unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Input Voltage | $\mathrm{V}_{\text {IN }}$ | 1.0 | - | 5.5 | V |
| Output Voltage Range (Adjusted by external feedback) | $\mathrm{V}_{\text {OUT }}$ | $\mathrm{V}_{\mathrm{IN}}$ | - | 5.5 | V |
| Reference Voltage ( $\mathrm{C}_{\text {REF }}=150 \mathrm{nF}$, under no loading, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {REF_NL }}$ | 1.183 | 1.190 | 1.197 | V |
| Reference Voltage <br> ( $\mathrm{C}_{\text {REF }}=150 \mathrm{nF}$, under no loading, $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ ) | VREF_NL_A | 1.178 | - | 1.202 | V |
| Reference Voltage Temperature Coefficient | TC VREF | - | 0.03 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Reference Voltage Load Current $\left(\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {REF }}=\mathrm{V}_{\text {REF_NL }} \pm 1.5 \%, \mathrm{C}_{\text {REF }}=1.0 \mu \mathrm{~F}\right)(\text { Note } 5)$ | $\mathrm{I}_{\text {REF }}$ | 2.5 | - | - | mA |
| Reference Voltage Load Regulation $\left(\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=0 \text { to } 100 \mu \mathrm{~A}, \mathrm{C}_{\text {REF }}=1.0 \mu \mathrm{~F}\right)$ | $V_{\text {REF_LOAD }}$ | - | 0.015 | 1.0 | mV |
| Reference Voltage Line Regulation (VOUT from 1.5 V to $5.5 \mathrm{~V}, \mathrm{C}_{\text {REF }}=1.0 \mu \mathrm{~F}$ ) | V $\mathrm{REF}_{\text {_LINE }}$ | - | 0.03 | 1.0 | $\mathrm{mV} / \mathrm{V}$ |
| FB, LBI Input Threshold ( ${ }_{\text {LOAD }}=0 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\text {LBI }}$ | 1.174 | 1.190 | 1.200 | V |
| N-FET ON Resistance | $\mathrm{R}_{\mathrm{DS}(\mathrm{ON}) \text { - }}$ | - | 0.6 | - | $\Omega$ |
| P-FET ON Resistance | $\mathrm{R}_{\mathrm{DS}(\mathrm{ON}) \text { - }}$ | - | 0.9 | - | $\Omega$ |
| LX Switch Current Limit (N-FET) | lıim | - | 1.0 | - | A |
| Operating Current into OUT $\left(\mathrm{V}_{\mathrm{FB}}=1.4 \mathrm{~V}\right.$, i.e. no switching, $\left.\mathrm{V}_{\mathrm{OUT}}=3.3 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{Q}}$ | - | 9.0 | 14 | $\mu \mathrm{A}$ |
| Shutdown Current into OUT (LBI/EN = GND) | $\mathrm{I}_{\text {SD }}$ | - | 0.05 | 1.0 | $\mu \mathrm{A}$ |
| LX Switch MAX. ON-Time ( $\mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ ) | ton | 1.2 | 1.4 | 1.8 | $\mu \mathrm{S}$ |
| LX Switch MIN. OFF-Time ( $\mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ ) | toff | 0.25 | 0.31 | 0.37 | $\mu \mathrm{S}$ |
| FB Input Current | $\mathrm{I}_{\text {FB }}$ | - | 1.5 | 9.0 | nA |
| Shutdown Current into BAT (LBI/EN $=0 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {BAT }}=3.0 \mathrm{~V}$ ) | ILBT | - | 50 | - | nA |
| BAT to LX resistance ( $\mathrm{V}_{\mathrm{FB}}=1.4 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ ) | RLBT_LX | - | 100 | - | $\Omega$ |
| LBI/EN Input Current | ILBIEN | - | 1.5 | 8.0 | nA |
| LBO Low Output Voltage ( $\mathrm{V}_{\text {LBI }}=0 \mathrm{~V}$, $\left.\mathrm{I}_{\text {SINK }}=1.0 \mathrm{~mA}\right)$ | VLBO_L | - | - | 0.05 | V |
| ENABLE (Pin 2) Input threshold, Low | $\mathrm{V}_{\mathrm{EN}}$ | - | - | 0.3 | V |
| ENABLE (Pin 2) Input threshold, High | $\mathrm{V}_{\mathrm{EN}}$ | 0.6 | - | - | V |

5. Loading capability increases with $\mathrm{V}_{\text {OUT }}$.


Figure 2. Simplified Functional Diagram

## TYPICAL OPERATING CHARACTERISTICS



Figure 3. Reference Voltage versus Output Current


Figure 5. Reference Voltage versus Temperature


Figure 7. Lx Switch Max. ON Time versus Temperature


Figure 4. Reference Voltage versus Input Voltage at OUT Pin


Figure 6. Switch ON Resistance versus Temperature


Figure 8. Min. Startup Battery Voltage versus Loading Current


Figure 9. Efficiency versus Load Current


Figure 11. Efficiency versus Load Current


Figure 13. Efficiency versus Load Current


Figure 10. Efficiency versus Load Current


Figure 12. Efficiency versus Load Current


Figure 14. Efficiency versus Load Current


Figure 15. Output Voltage Change versus Load Current


Figure 17. Battery Input Voltage vesus Output Ripple Voltage


Figure 19. No Load Operating Current versus Input Voltage at OUT Pin


Figure 16. Output Voltage Change versus Load Current


Figure 18. Battery Input Voltage versus Output Ripple Voltage


Upper Trace: Output Voltage Waveform, 2.0 V/Division Lower Trace: Shutdown Pin Waveform, 1.0 V/Division

Figure 20. Startup Transient Response


Figure 21. Continuous Conduction Mode Switching Waveform


Upper Trace: Output Voltage Ripple, $100 \mathrm{mV} /$ Division Lower Trace: Battery Voltage, $\mathrm{V}_{\mathrm{IN}}, 1.0 \mathrm{~V} /$ Division

Figure 23. Line Transient Response for $\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}$

( $\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=10 \mathrm{~mA}$ to $100 \mathrm{~mA} ; \mathrm{L}=22 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=33 \mu \mathrm{~F}$ ) Upper Trace: Output Voltage Ripple, $100 \mathrm{mV} /$ Division Lower Trace: Load Current, ILOAD, $50 \mathrm{~mA} /$ Division

Figure 25. Load Transient Response for $\mathrm{V}_{\mathrm{IN}}=2.4 \mathrm{~V}$


Figure 22. Discontinuous Conduction Mode Switching Waveform

$\left(\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}\right.$, $\mathrm{I}_{\text {LOAD }}=10 \mathrm{~mA}$ to $100 \mathrm{~mA} ; \mathrm{L}=22 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=33 \mu \mathrm{~F}$ ) Upper Trace: Output Voltage Ripple, $100 \mathrm{mV} /$ Division Lower Trace: Load Current, I LOAD, 50 mA /Division

Figure 24. Load Transient Response for $\mathrm{V}_{\mathrm{IN}}=1.8 \mathrm{~V}$

$\left(\mathrm{V}_{\text {OUT }}=3.3 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=10 \mathrm{~mA}\right.$ to $100 \mathrm{~mA} ; \mathrm{L}=22 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=33 \mu \mathrm{~F}$ ) Upper Trace: Output Voltage Ripple, $100 \mathrm{mV} /$ Division Lower Trace: Load Current, ILOAD, $50 \mathrm{~mA} /$ Division

Figure 26. Load Transient Response
for $\mathrm{V}_{\mathrm{IN}}=3.3 \mathrm{~V}$

## DETAILED OPERATION DESCRIPTIONS

NCP1411 is a monolithic micropower high frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 250 mA loading. It integrates Synchronous Rectifier for improving efficiency as well as eliminating the external Schottky Diode. High switching frequency (up to 600 kHz ) allows low profile inductor and output capacitor being used. Low-Battery Detector, Logic-Controlled Shutdown and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated application. With all these functions ON, the quiescent supply current is only $9.0 \mu \mathrm{~A}$ typical. This device is available in a compact Micro8 package.

## PFM Regulation Scheme

From the simplified Functional Diagram (Figure 2), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to REF. A switching cycle is initiated by the falling edge of the comparator, at the moment, the main switch (M1) is turned ON. After the maximum ON-time (typical $1.4 \mu \mathrm{~S}$ ) elapses or the current limit is reached, M1 is turned OFF, and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typical $0.31 \mu \mathrm{~S}$ ), this is to ensure energy transfer from the inductor to the output capacitor. If the regulator is operating at continuous conduction mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating at discontinuous conduction mode (DCM), which means the coil current will decrease to zero before the next cycle, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting, when the voltage drop is below the offset, the ZLC comparator output goes HIGH, and M2 is turned OFF. Negative feedback of closed loop operation regulates voltage at pin $1(\mathrm{FB})$ equal to the internal voltage reference (1.190 V).

## Synchronous Rectification

Synchronous Rectifier is used to replace Schottky Diode for eliminating the conduction loss contributed by forward voltage of the latter. Synchronous Rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns.

As main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M 2 is being turned ON .

When the main regulator is operating in CCM, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completely turned OFF, the above mentioned
situation will occur. So dead time is introduced to make sure M2 is completely turned OFF before M1 is being turned ON.

When the regulator is operating in DCM, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So the ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.

With the implementation of synchronous rectification, efficiency can be as high as $92 \%$. For single cell input voltage, use an external schottky diode such as MBR0520 connected from pin 7 to pin 8 to ensure quick start-up.

## Ring-Killer

When the device entered Discontinuous Conduction Mode operation, a typical ringing at LX pin will start while the inductor current just ceased. This ringing is caused primarily by the capacitance and inductance at LX node and the result can produce unwanted EMI problem to the system. In order to eliminate this ringing, an internal damping switch (M3) is implemented to provide a low impedance path to dissipate the residue energy stored in the inductor once the operation entered the Discontinuous Conduction Mode. This feature can improve the EMI problem. The performance of the Ring-Killer switch is shown in Figure 22.

## Cycle-by-Cycle Current Limit

From Figure 2, SenseFET is applied to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, sense-voltage is developed. Threshold detector (ILIM) detects whether the sense-voltage is higher than preset level. If it happens, detector output signifies the CONTROL LOGIC to switch OFF M1, and M1 can only be switched ON as next cycle starts after the minimum OFF-time (typical $0.31 \mu \mathrm{~S}$ ). With properly sizing of SenseFET and sense resistor, the peak coil current limit is set at 1.0 A typically.

## Voltage Reference

The voltage at REF is set typically at +1.190 V . It can deliver up to 2.5 mA with load regulation $\pm 1.5 \%$, at $\mathrm{V}_{\text {OUT }}$ equal to 3.3 V . If $\mathrm{V}_{\text {OUT }}$ is increased, the REF load capability can also be increased. A bypass capacitor of $0.15 \mu \mathrm{~F}$ is required for proper operation when REF is not loaded. If REF is loaded, $1.0 \mu \mathrm{~F}$ capacitor at REF is needed.

## Shutdown

The IC will shutdown when the voltage at pin 2 (LBI/EN) is pulled lower than 0.3 V . During shutdown, M1 and M2 are both switched OFF, however, the body diode of M2 allows current flow from battery to the output, the IC internal circuit will consume less than $0.05 \mu \mathrm{~A}$ current typically. If the pin

1 voltage raised higher than 0.6 V , the IC will be enabled. The internal circuit will only consume $9.0 \mu \mathrm{~A}$ current typically from the OUT pin. In order to ensure proper startup, a timing capacitor $\mathrm{C}_{\mathrm{EN}}$ as shown in Figure 1 is required to provide the reset pulse during batteries are plugged in. The product of $\mathrm{R}_{\mathrm{LB} 1}$ and $\mathrm{C}_{\mathrm{EN}}$ must be larger than 28 msec .

## Low-Battery Detection

A comparator with 30 mV hysteresis is applied to perform the low-battery detection function. When pin 2 (LBI/EN) is at a voltage, which can be defined by a resistor divider from the battery voltage, lower than the internal reference voltage, 1.190 V , the comparator output will cause a 50 Ohm low side switch to be turned ON. It will pull down the voltage at pin 3 (LBO) which has a hundreds kilo-Ohm of pull-high resistance. If the pin 2 voltage is higher than $1.190 \mathrm{~V}+30 \mathrm{mV}$, the comparator output will cause the 50 Ohm low side switch to be turned OFF, pin 3 will become high impedance, and its voltage will be pulled high.

## APPLICATIONS INFORMATION

## Output Voltage Setting

The output voltage of the converter is determined by the external feedback network comprised of $\mathrm{R}_{\mathrm{FB} 1}$ and $\mathrm{R}_{\mathrm{FB} 2}$ and the relationship is given by:

$$
\mathrm{V}_{\mathrm{OUT}}=1.190 \mathrm{~V} \times\left(1+\frac{\mathrm{R}_{\mathrm{FB} 1}}{\mathrm{R}_{\mathrm{FB} 2}}\right)
$$

where $\mathrm{R}_{\mathrm{FB} 1}$ and $\mathrm{R}_{\mathrm{FB} 2}$ are the upper and lower feedback resistors respectively.

## Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network comprised of $\mathrm{R}_{\mathrm{LB} 1}$ and $\mathrm{R}_{\mathrm{LB} 2}$ and the relationship is given by:

$$
\mathrm{V} \mathrm{LB}=1.190 \mathrm{~V} \times\left(1+\frac{\mathrm{R}_{\mathrm{LB} 1}}{\mathrm{R}_{\mathrm{LB} 2}}\right)
$$

where $\mathrm{R}_{\mathrm{LB} 1}$ and $\mathrm{R}_{\mathrm{LB} 2}$ are the upper and lower divider resistors respectively.

## Inductor Selection

The NCP1411 is tested to produce optimum performance with a $22 \mu \mathrm{H}$ inductor at $\mathrm{V}_{\mathrm{IN}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.3 \mathrm{~V}$ supplying output current up to 250 mA . For other input/output requirements, inductance in the range $10 \mu \mathrm{H}$ to $47 \mu \mathrm{H}$ can be used according to end application specifications. Selecting an inductor is a compromise between output current capability and tolerable output voltage ripple. Of course, the first thing we need to obey is to keep the peak inductor current below its saturation limit at maximum current and the $\mathrm{I}_{\mathrm{LIM}}$ of the device. In NCP1411, $\mathrm{I}_{\text {LIM }}$ is set at 1.0 A . As a rule of thumb, low inductance values supply higher output current, but also increase the ripple at output and reducing efficiency, on the other hand, high inductance values can improve output ripple and efficiency,
however it also limit the output current capability at the same time. One other parameter of the inductor is its DC resistance, this resistance can introduce unwanted power loss and hence reduce overall efficiency, the basic rule is selecting an inductor with lowest DC resistance within the board space limitation of the end application.

## Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals sees impulsive voltage/current waveforms. The currents flowing into and out of the capacitors multiplying with the Equivalent Series Resistance (ESR) of the capacitor producing ripple voltage at the terminals. During the syn-rect switch off cycle, the charges stored in the output capacitor is used to sustain the output load current. Load current at this period and the ESR combined and reflected as ripple at the output terminal. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guide line, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as a cost effective substitute.

## Optional Startup Schottky Diode for Low Battery Voltage

In general operation, no external schottky diode is required, however, in case you are intended to operate the device close to 1.0 V level, a schottky diode connected between the LX and OUT pins as shown in Figure 27 can help during startup of the converter. The effect of the additional schottky was shown in Figure 8.


Figure 27. PCB Layout Recommendations

## PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise and unwanted feedback that can affect the performance of the converter. Hints suggested in below can be used as a guide line in most situations.

## Grounding

Star-ground connection should be used to connect the output power return ground, the input power return ground and the device power ground together at one point. All high
current running paths must be thick enough for current flowing through and producing insignificant voltage drop along the path. Feedback signal path must be separated with the main current path and sensing directly at the anode of the output capacitor.

## Components Placement

Power components, i.e. input capacitor, inductor and output capacitor, must be placed as close together as possible. All connecting traces must be short, direct and
thick. High current flowing and switching paths must be kept away from the feedback ( FB , pin 1) terminal to avoid unwanted injection of noise into the feedback path.

## Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. External feedback network must be placed very close to the feedback (FB, pin 1) pin and sensing the output voltage directly at the anode of the output capacitor.


Figure 28. Typical Application Schematic for 2 Alkaline Cells Supply

## GENERAL DESIGN PROCEDURES

Switching mode converter design is considered as black magic to most engineers, some complicate empirical formulae are available for reference usage. Those formulae are derived from the assumption that the key components, i.e. power inductor and capacitors are available with no tolerance. Practically, its not true, the result is not a matter of how accurate the equations you are using to calculate the component values, the outcome is still somehow away from the optimum point. In below a simple method base on the most basic first order equations to estimate the inductor and capacitor values for NCP1411 operate in Continuous Conduction Mode is introduced. The component value set can be used as a starting point to fine tune the circuit operation. By all means, detail bench testing is needed to get the best performance out of the circuit.

Design Parameters:

| $\mathrm{V}_{\text {IN }}$ | $=1.8 \mathrm{~V}$ to 3.0 V , Typical 2.4 V |
| :--- | :--- |
| $\mathrm{~V}_{\text {OUT }}$ | $=3.3 \mathrm{~V}$ |
| $\mathrm{I}_{\text {OUT }}$ | $=200 \mathrm{~mA}(250 \mathrm{~mA}$ max $)$ |
| $\mathrm{V}_{\text {LB }}$ | $=2.0 \mathrm{~V}$ |
| $\mathrm{~V}_{\text {OUT-RIPPLE }}$ | $=40 \mathrm{mV} \mathrm{P}_{\text {P-P }}$ at $\mathrm{I}_{\text {OUT }}=250 \mathrm{~mA}$ |

Calculate the feedback network:
Select $\mathrm{R}_{\mathrm{FB} 2}=200 \mathrm{~K}$

$$
\begin{gathered}
\mathrm{R}_{\text {FB1 }}=\mathrm{R}_{\mathrm{FB} 2}\left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{\mathrm{~V}_{\text {REF }}}-1\right) \\
\mathrm{R}_{\mathrm{FB} 1}=200 \mathrm{~K}\left(\frac{3.3 \mathrm{~V}}{1.19 \mathrm{~V}}-1\right)=355 \mathrm{~K}
\end{gathered}
$$

With the feedback resistor divider, additional small capacitor, $\mathrm{C}_{\mathrm{FB} 1}$ in parallel with $\mathrm{R}_{\mathrm{FB} 1}$ is required to ensure stability. The value can be in between 68 pF to 220 pF , the rule is to select the lowest capacitance to ensure stability. Also a small capacitor, $\mathrm{C}_{\mathrm{FB} 2}$ in parallel with $\mathrm{R}_{\mathrm{FB} 2}$ may also be needed to lower the feedback ripple hence improve output regulation. The use of $\mathrm{C}_{\mathrm{FB} 2}$ is a compromise between output ripple level and regulation, so careful selection of the value according to end application requirement is needed. In this example, values for $\mathrm{C}_{\mathrm{FB} 1}$ and $\mathrm{C}_{\mathrm{FB} 2}$ are 150 pF and 220 pF respectively.

Calculate the Low Battery Detect divider:
$\mathrm{V}_{\mathrm{LB}} \quad=2.0 \mathrm{~V}$
Select $R_{\text {LB2 }}=330 \mathrm{~K}$

$$
\begin{gathered}
\mathrm{R}_{\mathrm{LB} 1}=\mathrm{R}_{\mathrm{LB} 2}\left(\frac{\mathrm{~V}_{\mathrm{LB}}}{\mathrm{~V}_{\mathrm{REF}}}-1\right) \\
\mathrm{R}_{\mathrm{LB} 1}=330 \mathrm{~K}\left(\frac{2.0 \mathrm{~V}}{1.19 \mathrm{~V}}-1\right)=225 \mathrm{~K} \\
\mathrm{C}_{\mathrm{EN}}=\frac{28 \mathrm{msec}}{225 \mathrm{~K}}=120 \mathrm{nF}
\end{gathered}
$$

Determine the Steady State Duty Ratio, D for typical $\mathrm{V}_{\text {IN }}$, operation will be optimized around this point:

$$
\begin{gathered}
\frac{\mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\text {IN }}}=\frac{1}{1-\mathrm{D}} \\
\mathrm{D}=1-\frac{\mathrm{VIN}}{\mathrm{~V}_{\text {OUT }}}=1-\frac{2.4 \mathrm{~V}}{3.3 \mathrm{~V}}=0.273
\end{gathered}
$$

Determine the average inductor current, $\mathrm{I}_{\mathrm{LAVG}}$ at maximum IOUT:

$$
\text { l} \mathrm{LAVG}=\frac{\mathrm{IOUT}}{1-\mathrm{D}}=\frac{250 \mathrm{~mA}}{1-0.273}=344 \mathrm{~mA}
$$

Determine the peak inductor ripple current, $\mathrm{I}_{\text {RIPPLE-P }}$ and calculate the inductor value:

Assume $\mathrm{I}_{\text {RIPPLE-P }}$ is $20 \%$ of $\mathrm{I}_{\text {LAVG }}$, the inductance of the power inductor can be calculated as in below:
$\mathrm{I}_{\text {RIPPLE-P }}=0.20 \times 344 \mathrm{~mA}=68.8 \mathrm{~mA}$

$$
\mathrm{L}=\frac{\mathrm{V} \text { IN } \times \operatorname{tON}}{2 \mathrm{I} \mathrm{RIPPLE}-\mathrm{P}}=\frac{2.4 \mathrm{~V} \times 1.4 \mu \mathrm{~S}}{2(68.8 \mathrm{~mA})}=24.4 \mu \mathrm{H}
$$

Standard value of $22 \mu \mathrm{H}$ is selected for initial trial.
Determine the output voltage ripple, VOUT-RIPPLE and calculate the output capacitor value:
$\mathrm{V}_{\text {OUT-RIPPLE }}=40 \mathrm{mV}$ P-P at $\mathrm{I}_{\text {OUT }}=250 \mathrm{~mA}$

$$
\text { COUT } \geq \frac{\text { IOUT } \times \text { tON }}{\text { VOUT }- \text { RIPPLE }- \text { IOUT } \times \text { ESRCOUT }}
$$

where $\mathrm{t}_{\mathrm{ON}}=1.4 \mu \mathrm{~S}$ and $\mathrm{ESR}_{\text {COUT }}=0.1 \Omega$,

$$
\text { COUT } \geq \frac{250 \mathrm{~mA} \times 1.4 \mu \mathrm{~S}}{40 \mathrm{mV}-250 \mathrm{~mA} \times 0.1 \Omega}=23.33 \mu \mathrm{~F}
$$

From above calculation, we need at least $23.33 \mu \mathrm{~F}$ in order to achieve the specified ripple level at conditions stated. Practically, a one level larger capacitor will be used to accommodate factors not take into account in the calculation. So a capacitor value of $33 \mu \mathrm{~F}$ is selected.

## NCP1450A

## PWM Step-up DC-DC Controller

The NCP1450A series are PWM step-up DC-DC switching controller that are specially designed for powering portable equipment from one or two cells battery packs. The NCP1450A series have a driver pin, EXT pin, for connecting to an external transistor. Large output currents can be obtained by connecting a low ON-resistance external power transistor to the EXT pin. With only five external components, this series allows a simple means to implement highly efficient converter for large output current applications.

Each device consists of an on-chip PWM (Pulse Width Modulation) oscillator, PWM controller, phase-compensated error amplifier, soft-start, voltage reference, and driver for driving external power transistor. Additionally, a chip enable feature is provided to power down the converter for extended battery life.

The NCP1450A device series are available in the TSOP-5 package with five standard regulated output voltages. Additional voltages that range from 1.8 V to 5.0 V in 100 mV steps can be manufactured.

## Features

- High Efficiency $86 \%$ at $\mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}, \mathrm{~V}_{\mathrm{IN}}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=3.0 \mathrm{~V}$

$$
88 \% \text { at } \mathrm{I}_{\mathrm{O}}=400 \mathrm{~mA}, \mathrm{~V}_{\mathrm{IN}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=5.0 \mathrm{~V}
$$

- Low Start-up Voltage of 0.9 V typical at $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$
- Operation Down to 0.6 V
- Five Standard Voltages: 1.9 V, 2.7 V, 3.0 V, 3.3 V, 5.0 V with High Accuracy $\pm 2.5 \%$
- Low Conversion Ripple
- High Output Current up to 1000 mA (3.0 V version at $\mathrm{V}_{\text {IN }}=2.0 \mathrm{~V}, \mathrm{~L}=10 \mu \mathrm{H}, \mathrm{C}_{\mathrm{OUT}}=220 \mu \mathrm{~F}$ )
- Fixed Frequency Pulse Width Modulation (PWM) at 180 kHz
- Chip Enable Pin with On-chip Pull-up Resistor
- Low Profile and Micro Miniature TSOP-5 Package


## Typical Applications

- Personal Digital Assistant (PDA)
- Electronic Games
- Portable Audio (MP3)
- Digital Still Cameras
- Handheld Instruments

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TSOP-5
SN SUFFIX
CASE 483

PIN CONNECTIONS AND
MARKING DIAGRAM


ORDERING INFORMATION
See detailed ordering and shipping information in the ordering information section on page 1484 of this data sheet.


Figure 1. Typical Step-up Converter Application


Figure 2. Representative Block Diagram
PIN FUNCTION DESCRIPTION

| Pin \# | Symbol | Pin Description |
| :---: | :---: | :--- |
| 1 | CE | Chip Enable Pin <br> (1) The chip is enabled if a voltage equal to or greater than 0.9 V is applied. <br> (2) The chip is disabled if a voltage less than 0.3 V is applied. <br> (3) The chip is enabled if this pin is left floating. |
| 2 | OUT | Output voltage monitor pin and also the power supply pin for the device. |
| 3 | NC | No internal connection to this pin. |
| 4 | GND | Ground pin. |
| 5 | EXT | External transistor drive pin. |

ORDERING INFORMATION (Note 1)

| Device | Output Voltage | Switching Frequency | Marking | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP1450ASN19T1 | 1.9 V | 180 KHz | DAY | TSOP-5 | 3000 Units on 7 Inch Reel |
| NCP1450ASN27T1 | 2.7 V |  | DAZ |  |  |
| NCP1450ASN30T1 | 3.0 V |  | DBA |  |  |
| NCP1450ASN33T1 | 3.3 V |  | DBC |  |  |
| NCP1450ASN50T1 | 5.0 V |  | DBD |  |  |

1. The ordering information lists five standard output voltage device options. Additional devices with output voltage ranging from 1.8 V to 5.0 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage (Pin 2) | $\mathrm{V}_{\text {OUT }}$ | 6.0 | V |
| Input/Output Pins <br> EXT (Pin 5) <br> EXT Sink/Source Current | $\begin{aligned} & V_{\text {EXT }} \\ & \mathrm{I}_{\text {EXT }} \end{aligned}$ | $\begin{gathered} -0.3 \text { to } 6.0 \\ -150 \text { to } 150 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| CE (Pin 1) Input Voltage Range Input Current Range | $\begin{aligned} & \mathrm{V}_{\mathrm{CE}} \\ & \mathrm{I}_{\mathrm{CE}} \end{aligned}$ | $\begin{gathered} -0.3 \text { to } 6.0 \\ -150 \text { to } 150 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance Junction to Air | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{AJA}} \end{gathered}$ | $\begin{aligned} & 500 \\ & 250 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

2. This device series contains ESD protection and exceeds the following tests:

Human Body Model (HBM) $\pm 2.0 \mathrm{kV}$ per JEDEC standard: JESD22-A114. Machine Model (MM) $\pm 200$ V per JEDEC standard: JESD22-A115.
3. Latch-up Current Maximum Rating: $\pm 150 \mathrm{~mA}$ per JEDEC standard: JESD78.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Frequency ( $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SET }} \times 0.96$, Note 5 ) | fosc | 144 | 180 | 216 | kHz |
| Frequency Temperature Coefficient ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\Delta f$ | - | 0.11 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| Maximum PWM Duty Cycle ( $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {SET }} \times 0.96$ ) | $\mathrm{D}_{\text {MAX }}$ | 70 | 80 | 90 | \% |
| Minimum Start-up Voltage ( $\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {start }}$ | - | 0.8 | 0.9 | V |
| Minimum Start-up Voltage Temperature Coefficient ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{V}_{\text {start }}$ | - | -1.6 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Minimum Operation Hold Voltage ( $\mathrm{l}=0 \mathrm{~mA}$ ) | $V_{\text {hold }}$ | - | 0.6 | 0.7 | V |
| Soft-Start Time (V $\mathrm{V}_{\text {OUT }}>0.8 \mathrm{~V}$ ) | tss | 0.5 | 2.0 | - | ms |

## CE (PIN 1)

| CE Input Voltage $\left(V_{\text {OUT }}=V_{S E T} \times 0.96\right)$ <br> High State, Device Enabled <br> Low State, Device Disabled | $\mathrm{V}_{\mathrm{CE}(\text { high })}$ | 0.9 | - | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| CE Input Current (Note 6) | $\mathrm{V}_{\mathrm{CE}(\text { low })}$ | - | - | 0.3 |  |
| High State, Device Enabled $\left(\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\mathrm{CE}}=5.0 \mathrm{~V}\right)$ |  |  |  |  |  |
| Low State, Device Disabled $\left(\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{CE}(\text { (high })}$ | -0.5 | 0 |  | $\mu \mathrm{~A}$ |

EXT (PIN 5)

| EXT "H" Output Current $\left(\mathrm{V}_{\text {EXT }}=\mathrm{V}_{\text {OUT }}-0.4 \mathrm{~V}\right)$ Device Suffix: 19T1 27T1 30T1 33T1 50T1 | IEXTH |  | $\begin{aligned} & -25.0 \\ & -35.0 \\ & -37.7 \\ & -40.0 \\ & -53.7 \end{aligned}$ | $\begin{aligned} & -20.0 \\ & -30.0 \\ & -30.0 \\ & -30.0 \\ & -35.0 \end{aligned}$ | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \text { EXT "L" Output Current }\left(\mathrm{V}_{\mathrm{EXT}}=0.4 \mathrm{~V}\right) \\ & \text { Device Suffix: } \\ & \text { 19T1 } \\ & \text { 27T1 } \\ & \text { 30T1 } \\ & \text { 33T1 } \\ & \text { 50T1 } \end{aligned}$ | $\mathrm{l}_{\text {EXTL }}$ | $\begin{aligned} & 20.0 \\ & 30.0 \\ & 30.0 \\ & 30.0 \\ & 35.0 \end{aligned}$ | $\begin{aligned} & 38.3 \\ & 48.0 \\ & 50.8 \\ & 52.0 \\ & 58.2 \end{aligned}$ |  | mA |

TOTAL DEVICE

| Output Voltage Device Suffix: 19T1 $27 T 1$ 30T1 33T1 50T1 | $\mathrm{V}_{\text {OUT }}$ | $\begin{aligned} & 1.853 \\ & 2.633 \\ & 2.925 \\ & 3.218 \\ & 4.875 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 2.7 \\ & 3.0 \\ & 3.3 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 1.948 \\ & 2.768 \\ & 3.075 \\ & 3.383 \\ & 5.125 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage Temperature Coefficient ( $\mathrm{T}_{\mathrm{A}}=-40$ to $+85^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{V}_{\text {OUT }}$ | - | 150 | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| ```Operating Current ( \(\mathrm{V}_{\mathrm{OUT}}=\mathrm{V}_{\mathrm{CE}}=\mathrm{V}_{\mathrm{SET}} \times 0.96\), Note 5 ) Device Suffix: 19T1 27T1 30T1 33T1 50T1``` | IDD |  | $\begin{gathered} 55 \\ 93 \\ 98 \\ 103 \\ 136 \end{gathered}$ | $\begin{gathered} 90 \\ 140 \\ 150 \\ 160 \\ 220 \end{gathered}$ | $\mu \mathrm{A}$ |
| Stand-by Current ( $\left.\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {CE }}=\mathrm{V}_{\text {SET }}+0.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {StB }}$ | - | 15 | 20 | $\mu \mathrm{A}$ |
| Off-State Current (VOUT $=5.0 \mathrm{~V}, \mathrm{~V}_{\text {CE }}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40$ to $+85^{\circ} \mathrm{C}$, Note 6) | loff | - | 0.6 | 1.5 | $\mu \mathrm{A}$ |

5. $\mathrm{V}_{\text {SET }}$ means setting of output voltage.
6. CE pin is integrated with an internal $10 \mathrm{M} \Omega$ pull-up resistor.


Figure 3. NCP1450ASN19T1 Output Voltage vs. Output Current


Figure 5. NCP1450ASN50T1 Output Voltage vs. Output Current


Figure 7. NCP1450ASN30T1 Efficiency vs. Output Current


Figure 4. NCP1450ASN30T1 Output Voltage vs. Output Current


Figure 6. NCP1450ASN19T1 Efficiency vs. Output Current


Figure 8. NCP1450ASN50T1 Efficiency vs. Output Current


Figure 9. NCP1450ASN19T1 Output Voltage vs. Temperature


Figure 11. NCP1450ASN50T1 Output Voltage vs. Temperature


Figure 13. NCP1450ASN30T1 Operating Current vs. Temperature


Figure 10. NCP1450ASN30T1 Output Voltage
vs. Temperature


Figure 12. NCP1450ASN19T1 Operating Current vs. Temperature


Figure 14. NCP1450ASN50T1 Operating Current vs. Temperature


Figure 15. NCP1450ASN19T1 Standby Current vs. Temperature


Figure 17. NCP1450ASN50T1 Standby Current vs. Temperature


Figure 19. NCP1450ASN30T1 Off-State Current vs. Temperature


Figure 16. NCP1450ASN30T1 Standby Current vs. Temperature


Figure 18. NCP1450ASN19T1 Off-State Current vs. Temperature


Figure 20. NCP1450ASN50T1 Off-State Current vs. Temperature


Figure 21. NCP1450ASN19T1 Oscillator Frequency vs. Temperature


Figure 22. NCP1450ASN30T1 Oscillator Frequency vs. Temperature


Figure 23. NCP1450ASN50T1 Oscillator Frequency vs. Temperature


Figure 25. NCP1450ASN30T1 Maximum Duty Cycle vs. Temperature


Figure 24. NCP1450ASN19T1 Maximum Duty Cycle vs. Temperature


Figure 26. NCP1450ASN50T1 Maximum Duty Cycle vs. Temperature


Figure 27. NCP1450ASN19T1 EXT "H" Output Current vs. Temperature


Figure 29. NCP1450ASN50T1 EXT "H" Output Current vs. Temperature


Figure 31. NCP1450ASN30T1 EXT "L" Output Current vs. Temperature


Figure 28. NCP1450ASN30T1 EXT "H" Output Current vs. Temperature


Figure 30. NCP1450ASN19T1 EXT "L" Output Current vs. Temperature


Figure 32. NCP1450ASN50T1 EXT "L" Output Current vs. Temperature


Figure 33. NCP1450ASN19T1 EXT "H" ON-Resistance vs. Temperature


Figure 35. NCP1450ASN50T1 EXT "H" ON-Resistance vs. Temperature


Figure 37. NCP1450ASN30T1 EXT "L" ON-Resistance vs. Temperature


Figure 34. NCP1450ASN30T1 EXT "H" ON-Resistance vs. Temperature


Figure 36. NCP1450ASN19T1 EXT "L" ON-Resistance vs. Temperature


Figure 38. NCP1450ASN50T1 EXT "L" ON-Resistance vs. Temperature


Figure 39. NCP1450ASN19T1 Startup/Hold Voltage vs. Temperature


Figure 40. NCP1450ASN30T1 Startup/Hold Voltage vs. Temperature


Figure 41. NCP1450ASN50T1 Startup/Hold Voltage vs. Temperature


Figure 43. NCP1450ASN30T1 Ripple Voltage vs. Output Current


Figure 42. NCP1450ASN19T1 Ripple Voltage vs. Output Current


Figure 44. NCP1450ASN50T1 Ripple Voltage vs. Output Current


Figure 45. NCP1450ASN19T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)


Figure 46. NCP1450ASN19T1 Startup/Hold Voltage vs. Output Current (Using BJT)


Figure 47. NCP1450ASN30T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)


Figure 48. NCP1450ASN30T1 Startup/Hold Voltage vs. Output Current (Using BJT)


Figure 49. NCP1450ASN50T1 Startup/Hold Voltage vs. Output Current (Using MOSFET)


Figure 50. NCP1450ASN50T1 Startup/Hold Voltage vs. Output Current (Using BJT)


Figure 51. NCP1450ASN19T1 Operating Waveforms (Medium Load)

$\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=1.8 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=20 \mathrm{~mA}, \mathrm{~L}=10 \mu \mathrm{H}$,
Cout $=220 \mu \mathrm{~F}$

1. $\mathrm{V}_{\mathrm{L}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{L}}, 500 \mathrm{~mA} / \mathrm{div}$
3. $\mathrm{V}_{\text {OUt }}, 50 \mathrm{mV} / \mathrm{div}$, AC coupled

Figure 53. NCP1450ASN30T1 Operating Waveforms (Medium Load)


Figure 55. NCP1450ASN50T1 Operating Waveforms (Medium Load)


Figure 52. NCP1450ASN19T1 Operating Waveforms (Heavy Load)

$\mathrm{V}_{\text {OUT }}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {IN }}=1.8 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~L}=10 \mu \mathrm{H}$, $C_{\text {OUT }}=220 \mu \mathrm{~F}$

1. $\mathrm{V}_{\mathrm{L}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{L}, 500 \mathrm{~mA} / \mathrm{div}$
3. $\mathrm{V}_{\text {OUT }}, 50 \mathrm{mV} / \mathrm{div}$, AC coupled

Figure 54. NCP1450ASN30T1 Operating Waveforms (Heavy Load)

$\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=3.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}, \mathrm{~L}=10 \mu \mathrm{H}$,

$$
\mathrm{C}_{\text {OUT }}=220 \mu \mathrm{~F}
$$

1. $\mathrm{V}_{\mathrm{L}}, 2.0 \mathrm{~V} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{L}}, 500 \mathrm{~mA} / \mathrm{div}$
3. $\mathrm{V}_{\text {OUT }}, 50 \mathrm{mV} / \mathrm{div}$, AC coupled

Figure 56. NCP1450ASN50T1 Operating Waveforms (Heavy Load)


Figure 57. NCP1450ASN19T1 Load Transient Response

$\mathrm{V}_{\text {IN }}=2.0 \mathrm{~V}, \mathrm{~L}=4.7 \mu \mathrm{H}, \mathrm{C}_{\text {OUT }}=220 \mu \mathrm{~F}$

1. $\mathrm{V}_{\text {OUt }}, 3.0 \mathrm{~V}$ (AC coupled), $200 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}, 1.0 \mathrm{~mA}$ to 100 mA

Figure 59. NCP1450ASN30T1 Load Transient Response

$\mathrm{V}_{\text {IN }}=3.0 \mathrm{~V}, \mathrm{~L}=4.7 \mu \mathrm{H}, \mathrm{C}_{\mathrm{OUT}}=220 \mu \mathrm{~F}$

1. $\mathrm{V}_{\text {OUt }} 5.0 \mathrm{~V}$ (AC coupled), $200 \mathrm{mV} / \mathrm{div}$
2. $\mathrm{I}_{\mathrm{O}}, 1.0 \mathrm{~mA}$ to 100 mA

Figure 61. NCP1450ASN50T1 Load Transient Response


Figure 58. NCP1450ASN19T1 Load Transient Response


Figure 60. NCP1450ASN30T1 Load Transient Response


$$
\mathrm{V}_{\text {IN }}=3.0 \mathrm{~V}, \mathrm{~L}=4.7 \mu \mathrm{H}, \mathrm{C}_{\mathrm{OUT}}=220 \mu \mathrm{~F}
$$

1. $\mathrm{V}_{\text {OUT }}, 5.0 \mathrm{~V}$ (AC coupled), $200 \mathrm{mV} /$ div
2. $\mathrm{I}_{\mathrm{O}}, 100 \mathrm{~mA}$ to 1.0 mA

Figure 62. NCP1450ASN50T1 Load Transient Response


Figure 63. NCP1450ASN19T1 Output Voltage vs. Output Current (Ext. BJT)


Figure 65. NCP1450ASN50T1 Output Voltage
vs. Output Current (Ext. BJT)


Figure 67. NCP1450ASN30T1 Efficiency vs. Output Current (Ext. BJT)


Figure 64. NCP1450ASN30T1 Output Voltage vs. Output Current (Ext. BJT)


Figure 66. NCP1450ASN19T1 Efficiency vs. Output Current (Ext. BJT)

Figure 68. NCP1450ASN50T1 Efficiency vs. Output Current (Ext. BJT)


Figure 69. NCP1450ASNXXT1 No Load Input Current vs. Input Voltage (Using MOSFET)


Figure 70. NCP1450ASNXXT1 No Load Input Current vs. Input Voltage (Using BJT)

## DETAILED OPERATING DESCRIPTION

## Operation

The NCP1450A series are monolithic power switching controllers optimized for battery powered portable products where large output current is required.

The NCP1450A series are low noise fixed frequency voltage-mode PWM DC-DC controllers, and consist of start-up circuit, feedback resistor divider, reference voltage, oscillator, loop compensation network, PWM control circuit, and low ON resistance driver. Due to the on-chip feedback resistor and loop compensation network, the system designer can get the regulated output voltage from 1.8 V to 5.0 V with 0.1 V stepwise with a small number of external components. The quiescent current is typically $93 \mu \mathrm{~A}\left(\mathrm{~V}_{\text {OUT }}=2.7 \mathrm{~V}, \mathrm{f}_{\text {OSC }}=180 \mathrm{kHz}\right)$, and can be further reduced to about $1.5 \mu \mathrm{~A}$ when the chip is disabled ( $\mathrm{V}_{\mathrm{CE}}<$ 0.3 V ).

The NCP1450A operation can be best understood by referring to the block diagram in Figure 2. The error amplifier monitors the output voltage via the feedback resistor divider by comparing the feedback voltage with the reference voltage. When the feedback voltage is lower than the reference voltage, the error amplifier output will decrease. The error amplifier output is then compared with the oscillator ramp voltage at the PWM controller. When the ramp voltage is higher than the error amplifier output, the high-side driver is turned on and the low-side driver is turned off which will then switch on the external transistor; and vice versa. As the error amplifier output decreases, the high-side driver turn-on time increases and duty cycle increases. When the feedback voltage is higher than the reference voltage, the error amplifier output increases and the duty cycle decreases. When the external power switch is on, the current ramps up in the inductor, storing energy in the magnetic field. When the external power switch is off, the energy stored in the magnetic field is transferred to the output filter capacitor and the load. The output filter capacitor stores the charge while the inductor current is higher than the output current, then sustains the output voltage until the next switching cycle.

As the load current is decreased, the switch transistor turns on for a shorter duty cycle. Under the light load condition, the controller will skip cycles to maintain the output voltage regulation.

## Soft Start

There is a soft start circuit in NCP1450A. When power is applied to the device, the soft start circuit pumps up the output voltage to approximately 1.5 V at a fixed duty cycle, the level at which the controller can operate normally. In addition to that, the start-up capability with heavy loads is also improved.

## Oscillator

The oscillator frequency is internally set to 180 kHz at an accuracy of $\pm 20 \%$ and with low temperature coefficient of $0.11 \% /{ }^{\circ} \mathrm{C}$.

## Regulated Converter Voltage ( $\mathrm{V}_{\text {OUT }}$ )

The $\mathrm{V}_{\text {OUT }}$ is set by an integrated feedback resistor network. This is trimmed to a selected voltage from 1.8 V to 5.0 V range in 100 mV steps with an accuracy of $\pm 2.5 \%$.

## Compensation

The device is designed to operate in continuous conduction mode. An internal compensation circuit was designed to guarantee stability over the full input/output voltage and full output load range.

## Enable/Disable Operation

The NCP1400A series offer IC shut-down mode by chip enable pin (CE pin) to reduce current consumption. An internal pull-up resistor tied the CE pin to OUT pin by default, i.e., user can float the pin CE for permanent "ON". When voltage at pin CE is equal or greater than 0.9 V , the chip will be enabled, which means the controller is in normal operation. When voltage at pin CE is less than 0.3 V , the chip is disabled, which means IC is shutdown.
Important: DO NOT apply a voltage between 0.3 V to 0.9 V to pin CE as this is the CE pin's hysteresis voltage range. Clearly defined output states can only be obtained by applying voltage out of this range.

## APPLICATION CIRCUIT INFORMATION

## Step-up Converter Design Equations

The NCP1450A PWM step-up DC-DC controller is designed to operate in continuous conduction mode and can be defined by the following equations. External components values can be calculated from these equations, however, the optimized value should obtained through experimental results.

| Calculation | Equation |
| :---: | :---: |
| D | $\leq \frac{V_{O U T}+V_{D}-V_{I N}}{V_{O U T}+V_{D}-V_{S}}$ |
| l | $\frac{\mathrm{lO}}{1-\mathrm{D}}$ |
| L | $\frac{\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{S}} \mathrm{D}_{\mathrm{in}}\right.}{2 \mathrm{f}\left(\mathrm{I} \mathrm{~L}-I_{\min }\right)}$ |
| lPK | $\mathrm{LL}+\frac{\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{S}}\right) \mathrm{D}}{2 \mathrm{Lf}}$ |
| $\Delta \mathrm{Q}$ | $\frac{(\mathrm{IL}-\mathrm{IO})(1-\mathrm{D})}{f}$ |
| $V_{\text {PP }}$ | $\approx \frac{\Delta \mathrm{Q}}{\mathrm{COUT}}+(\mathrm{IL}-\mathrm{IO}) \mathrm{ESR}$ |

## NOTES:

D - On-time duty cycle
IL - Average inductor current
IPK - Peak inductor current
$I_{\text {min }}$ - Minimum inductor current
IO - Desired dc output current
$\mathrm{V}_{\mathrm{IN}}$ - Nominal operating dc input voltage
$V_{\text {OUT }}$ - Desired dc output voltage
$V_{D}$ - Diode forward voltage
$\mathrm{V}_{\mathrm{S}}$ - Saturation voltage of the external transistor switch
$\Delta Q \quad$ - Charge stores in the Cout during charging up
ESR - Equivalent series resistance of the output capacitor

## External Component Selection

## Inductor Selection

The NCP1450A is designed to work well with a 6.8 to 12 $\mu \mathrm{H}$ inductors in most applications $10 \mu \mathrm{H}$ is a sufficiently low value to allow the use of a small surface mount coil, but large enough to maintain low ripple. Lower inductance values supply higher output current, but also increase the ripple and reduce efficiency.

Higher inductor values reduce ripple and improve efficiency, but also limit output current.
The inductor should have small DCR , usually less than $1 \Omega$, to minimize loss. It is necessary to choose an inductor with a saturation current greater than the peak current which the inductor will encounter in the application.

## Diode

The diode is the largest source of loss in DC-DC converters. The most importance parameters which affect their efficiency are the forward voltage drop, $\mathrm{V}_{\mathrm{D}}$, and the reverse recovery time, trr. The forward voltage drop creates a loss just by having a voltage across the device while a current flowing through it. The reverse recovery time generates a loss when the diode is reverse biased, and the current appears to actually flow backwards through the diode due to the minority carriers being swept from the $\mathrm{P}-\mathrm{N}$ junction. A Schottky diode with the following characteristics is recommended:

Small forward voltage, $\mathrm{V}_{\mathrm{F}}<0.3 \mathrm{~V}$
Small reverse leakage current
Fast reverse recovery time/switching speed
Rated current larger than peak inductor current,

$$
\mathrm{I}_{\text {rated }}>\mathrm{I}_{\mathrm{PK}}
$$

Reverse voltage larger than output voltage,
$\mathrm{V}_{\text {reverse }}>\mathrm{V}_{\text {OUT }}$

## Input Capacitor

The input capacitor can stabilize the input voltage and minimize peak current ripple from the source. The value of the capacitor depends on the impedance of the input source used. Small ESR (Equivalent Series Resistance) Tantalum or ceramic capacitor with a value of $10 \mu \mathrm{~F}$ should be suitable.

## Output Capacitor

The output capacitor is used for sustaining the output voltage when the external MOSFET or bipolar transistor is switched on and smoothing the ripple voltage. Low ESR capacitor should be used to reduce output ripple voltage. In general, a $100 \mu \mathrm{~F}$ to $220 \mu \mathrm{~F}$ low $\operatorname{ESR}(0.10 \Omega$ to $0.30 \Omega$ ) Tantalum capacitor should be appropriate.

## External Switch Transistor

An enhancement N -channel MOSFET or a bipolar NPN transistor can be used as the external switch transistor.

For enhancement N-channel MOSFET, since enhancement MOSFET is a voltage driven device, it is a more efficient switch than a BJT transistor. However, the MOSFET requires a higher voltage to turn on as compared with BJT transistors. An enhancement N-channel MOSFET can be selected by the following guidelines:

1. Low ON -resistance, $\mathrm{R}_{\mathrm{DS}(o n)}$, typically $<0.1 \Omega$.
2. Low gate threshold voltage, $\mathrm{V}_{\mathrm{GS}(\mathrm{th})}$, must be < $\mathrm{V}_{\text {OUT }}$, typically $<1.5 \mathrm{~V}$, it is especially important for the low $\mathrm{V}_{\text {OUT }}$ device, like $\mathrm{V}_{\text {OUT }}=1.9 \mathrm{~V}$.
3. Rated continuous drain current, $\mathrm{I}_{\mathrm{D}}$, should be larger than the peak inductor current, i.e. $\mathrm{I}_{\mathrm{D}}>\mathrm{I}_{\mathrm{PK}}$.
4. Gate capacitance should be 1200 pF or less.

For bipolar NPN transistor, medium power transistor with continuous collector current typically 1 A to 5 A and $\mathrm{V}_{\mathrm{CE} \text { (sat) }}$ $<0.2 \mathrm{~V}$ should be employed. The driving capability is determined by the DC current gain, $\mathrm{H}_{\mathrm{FE}}$, of the transistor and the base resistor, Rb ; and the controller's EXT pin must be able to supply the necessary driving current.

Rb can be calculated by the following equation:

$$
\begin{gathered}
\mathrm{Rb}=\frac{\mathrm{V}_{\mathrm{OUT}}-0.7}{\mathrm{Ib}}-\frac{0.4}{|\mathrm{IEXTH}|} \\
\mathrm{lb}=\frac{\mathrm{IPK}}{\mathrm{H}_{\mathrm{FE}}}
\end{gathered}
$$

Since the pulse current flows through the transistor, the exact Rb value should be finely tuned by the experiment. Generally, a small Rb value can increase the output current capability, but the efficiency will decrease due to more energy is used to drive the transistor.

Moreover, a speed-up capacitor, Cb , should be connected in parallel with Rb to reduce switching loss and improve efficiency. Cb can be calculated by the equation below:

$$
\mathrm{Cb} \leq \frac{1}{2 \pi \times \mathrm{Rb} \times \mathrm{fOSC} \times 0.7}
$$

It is due to the variation in the characteristics of the transistor used. The calculated value should be used as the initial test value and the optimized value should be obtained by the experiment.

External Component Reference Data

| Device | $\mathbf{V}_{\text {OUT }}$ | Inductor <br> Model | Inductor <br> Value | External <br> Transistor | Diode | Output <br> Capacitor |
| :---: | :---: | :---: | :---: | :---: | :--- | :---: |
| NCP1450ASN19T1 | 1.9 V | CD54 | $12 \mu \mathrm{H}$ | MGSF3442VT | MBRM120LT3 | $220 \mu \mathrm{~F}$ |
| NCP1450ASN30T1 | 3.0 V | CD54 | $10 \mu \mathrm{H}$ | MGSF3442VT | MBRM120LT3 | $220 \mu \mathrm{~F}$ |
| NCP1450ASN50T1 | 5.0 V | CD54 | $10 \mu \mathrm{H}$ | MGSF3442VT | MBRM120LT3 | $220 \mu \mathrm{~F}$ |
| NCP1450ASN19T1 | 1.9 V | CD54 | $12 \mu \mathrm{H}$ | MMJT9410 | MBRM120LT3 | $220 \mu \mathrm{~F}$ |
| NCP1450ASN30T1 | 3.0 V | CD54 | $10 \mu \mathrm{H}$ | MMJT9410 | MBRM120LT3 | $220 \mu \mathrm{~F}$ |
| NCP1450ASN50T1 | 5.0 V | CD54 | $10 \mu \mathrm{H}$ | MMJT9410 | MBRM120LT3 | $220 \mu \mathrm{~F}$ |

An evaluation board of NCP1450A has been made in the small size of $89 \mathrm{~mm} \times 51 \mathrm{~mm}$. The artwork and the silk screen of the surface-mount evaluation board PCB are shown in Figures 71 and 72. Please contact your ON

Semiconductor representative for availability. The evaluation board schematic diagrams are shown in Figures 73 and 74.


Figure 71. NCP1450A PWM Step-up DC-DC Controller Evaluation Board Silkscreen


Figure 72. NCP1450A PWM Step-up DC-DC Controller Evaluation Board Artwork (Component Side)


Figure 73. NCP1450A Evaluation Board Schematic Diagram 1 (Step-up DC-DC Converter Using External MOSFET Switch)


Figure 74. NCP1450A Evaluation Board Schematic Diagram 2 (Step-up DC-DC Converter Using External Bipolar Transistor Switch)

## PCB Layout Hints

## Grounding

One point grounding should be used for the output power return ground, the input power return ground, and the device switch ground to reduce noise. In Figure 73, e.g.: C2 GND, C1 GND, and IC1 GND are connected at one point in the evaluation board. The input ground and output ground traces must be thick enough for current to flow through and for reducing ground bounce.

## Power Signal Traces

Low resistance conducting paths should be used for the power carrying traces to reduce power loss so as to improve
efficiency (short and thick traces for connecting the inductor L can also reduce stray inductance), e.g.: short and thick traces listed below are used in the evaluation board:

1. Trace from TP1 to L1
2. Trace from L1 to anode pin of D1
3. Trace from cathode pin of D1 to TP2

## Output Capacitor

The output capacitor should be placed close to the output terminals to obtain better smoothing effect on the output ripple.

Components Supplier

| Parts | Supplier | Part Number | Description | Phone |
| :---: | :---: | :---: | :---: | :---: |
| Inductor: L1, L2 | Sumida Electric Co. Ltd. | CD54-100MC | Inductor $10 \mu \mathrm{H} / 1.44 \mathrm{~A}$ | (852) 2880-6688 |
| Schottky Diode: D1, D2 | ON Semiconductor | MBRM120LT3 | Schottky Power Rectifier | (852) 2689-0088 |
| MOSFET: Q1 | ON Semiconductor | MGSF3442VT1 | Power MOSFET N-Channel | (852) 2689-0088 |
| BJT: Q2 | ON Semiconductor | MMJT9410 | Bipolar Power Transistor | (852) 2689-0088 |
| Output Capacitor: C1, C3 | KEMET Electronics Corp. | T495D227K006AS | Low ESR Tantalum Capacitor $220 \mu \mathrm{~F} / 6.0 \mathrm{~V}$ | (852) 2305-1168 |
| Input Capacitor: C2, C4 | KEMET Electronics Corp. | T491C106K016AS | Low Profile Tantalum Capacitor $10 \mu \mathrm{~F} / 16 \mathrm{~V}$ | (852) 2305-1168 |

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


TSOP-5
(Footprint Compatible with SOT23-5)

TSOP-5
T1 ORIENTATION
8 mm


## MC34063A, MC33063A

### 1.5 A, Step-Up/Down/ Inverting Switching Regulators

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision $2 \%$ Reference


This device contains 51 active transistors.
Figure 1. Representative Schematic Diagram


PIN CONNECTIONS

(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1514 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 1514 of this data sheet.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 40 | Vdc |
| Comparator Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | -0.3 to +40 | Vdc |
| Switch Collector Voltage | $\mathrm{V}_{\text {( } \text { (switch) }}$ | 40 | Vdc |
| Switch Emitter Voltage ( $\mathrm{V}_{\text {Pin } 1}=40 \mathrm{~V}$ ) | $\mathrm{V}_{\mathrm{E} \text { (switch) }}$ | 40 | Vdc |
| Switch Collector to Emitter Voltage | $\mathrm{V}_{\text {CE(switch) }}$ | 40 | Vdc |
| Driver Collector Voltage | $\mathrm{V}_{\mathrm{C} \text { (driver) }}$ | 40 | Vdc |
| Driver Collector Current (Note 1) | $\mathrm{I}_{\mathrm{C} \text { (driver) }}$ | 100 | mA |
| Switch Current | Isw | 1.5 | A |
| Power Dissipation and Thermal Characteristics <br> Plastic Package, P, P1 Suffix $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance <br> SOIC Package, D Suffix $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 1.25 \\ & 100 \\ & \\ & 625 \\ & 160 \end{aligned}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range $\begin{aligned} & \text { MC34063A } \\ & \text { MC33063AV } \\ & \text { MC33063A } \end{aligned}$ | $\mathrm{T}_{\mathrm{A}}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+125 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 3], unless otherwise specified.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Frequency ( $\mathrm{V}_{\text {Pin } 5}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{f}_{\text {osc }}$ | 24 | 33 | 42 | kHz |
| Charge Current ( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ to $\left.40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\text {chg }}$ | 24 | 35 | 42 | $\mu \mathrm{A}$ |
| Discharge Current ( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ to $\left.40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $l_{\text {dischg }}$ | 140 | 220 | 260 | $\mu \mathrm{A}$ |
| Discharge to Charge Current Ratio (Pin 7 to $\mathrm{V}_{\mathrm{CC}}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{I}_{\text {dischg }} / I_{\text {chg }}$ | 5.2 | 6.5 | 7.5 | - |
| Current Limit Sense Voltage ( $l_{\text {chg }}=I_{\text {dischg }}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{ipk}}$ (sense) | 250 | 300 | 350 | mV |

OUTPUT SWITCH (Note 4)

| Saturation Voltage, Darlington Connection ( $\mathrm{I}_{\mathrm{sw}}=1.0 \mathrm{~A}$, Pins 1, 8 connected) | $\mathrm{V}_{\mathrm{CE} \text { (sat) }}$ | - | 1.0 | 1.3 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Saturation Voltage (Note 5) $\left(I_{\text {SW }}=1.0 \mathrm{~A}, \mathrm{R}_{\text {Pin } 8}=82 \Omega \text { to } \mathrm{V}_{\mathrm{CC}}, \text { Forced } \beta \simeq 20\right)$ | $\mathrm{V}_{\mathrm{CE} \text { (sat) }}$ | - | 0.45 | 0.7 | V |
| DC Current Gain ( $\mathrm{I}_{\text {SW }}=1.0 \mathrm{~A}, \mathrm{~V}_{\mathrm{CE}}=5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{h}_{\text {FE }}$ | 50 | 75 | - | - |
| Collector Off-State Current ( $\mathrm{V}_{\text {CE }}=40 \mathrm{~V}$ ) | $\mathrm{I}_{\text {( } \text { (ff) }}$ | - | 0.01 | 100 | $\mu \mathrm{A}$ |

COMPARATOR

| Threshold Voltage | $\mathrm{V}_{\text {th }}$ |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 1.225 | 1.25 | 1.275 |  |
| $\mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ |  | 1.21 | - | 1.29 |  |
| Threshold Voltage Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}\right.$ to 40 V$)$ | Regline |  |  |  | mV |
| MC33063A, MC34063A |  | - | 1.4 | 5.0 |  |
| MC33363AV |  | - | 1.4 | 6.0 |  |
| Input Bias Current $\left(\mathrm{V}_{\text {in }}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | -20 | -400 | nA |

## TOTAL DEVICE

| Supply Current $\left(V_{C C}=5.0 \mathrm{~V}\right.$ to $40 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}$, Pin $7=\mathrm{V}_{\mathrm{CC}}$, <br> $\mathrm{V}_{\text {Pin } 5}>\mathrm{V}_{\text {th }}$, Pin $2=G n d$, remaining pins open $)$ | $\mathrm{I}_{\mathrm{CC}}$ | - | - | 4.0 | mA |
| :--- | :--- | :--- | :--- | :--- | :--- |

3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34063A, $-40^{\circ} \mathrm{C}$ for MC33063A, AV $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34063A, $+85^{\circ} \mathrm{C}$ for MC33063A,$+125^{\circ} \mathrm{C}$ for MC33063AV 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
4. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ( $\leq 300 \mathrm{~mA}$ ) and high driver currents ( $\geq 30 \mathrm{~mA}$ ), it may take up to $2.0 \mu \mathrm{~s}$ for it to come out of saturation. This condition will shorten the off time at frequencies $\geq 30 \mathrm{kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:
Forced $\beta$ of output switch : $\frac{\text { IC output }}{I_{C} \text { driver }-7.0 \mathrm{~mA}^{*}} \geq 10$

* The $100 \Omega$ resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.


Figure 2. Output Switch On-Off Time versus Oscillator Timing Capacitor


Figure 4. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current


Figure 6. Current Limit Sense Voltage versus Temperature


Figure 3. Timing Capacitor Waveform


Figure 5. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current


Figure 7. Standby Supply Current versus Supply Voltage

[^31]
## MC34063A, MC33063A



| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$ to $16 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=175 \mathrm{~mA}$ | $30 \mathrm{mV}= \pm 0.05 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=75 \mathrm{~mA}$ to 175 mA | $10 \mathrm{mV}= \pm 0.017 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=175 \mathrm{~mA}$ | 400 mVpp |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=175 \mathrm{~mA}$ | $87.7 \%$ |
| Output Ripple With Optional Filter | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=175 \mathrm{~mA}$ | 40 mVpp |

Figure 8. Step-Up Converter

## MC34063A, MC33063A



Figure 9. External Current Boost Connections for $\mathrm{I}_{\mathrm{C}}$ Peak Greater than 1.5 A

## 9a. External NPN Switch

9b. External NPN Saturated Switch
(See Note 7)
7. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ( $\leq 300 \mathrm{~mA}$ ) and high driver currents ( $\geq 30 \mathrm{~mA}$ ), it may take up to $2.0 \mu \mathrm{~s}$ to come out of saturation. This condition will shorten the off time at frequencies $\geq 30 \mathrm{kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.


| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=15 \mathrm{~V}$ to $25 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | $12 \mathrm{mV}= \pm 0.12 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}$ to 500 mA | $3.0 \mathrm{mV}= \pm 0.03 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | 120 mVpp |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 1.1 A |
| Efficiency | $\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | $83.7 \%$ |
| Output Ripple With Optional Filter | $\mathrm{V}_{\text {in }}=25 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=500 \mathrm{~mA}$ | 40 mVpp |

Figure 10. Step-Down Converter


Figure 11. External Current Boost Connections for $\mathrm{I}_{\mathrm{C}}$ Peak Greater than 1.5 A

11a. External NPN Switch
11b. External PNP Saturated Switch

## MC34063A, MC33063A



| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=4.5 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | $3.0 \mathrm{mV}= \pm 0.012 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$ to 100 mA | $0.022 \mathrm{~V}= \pm 0.09 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | 500 mVpp |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 910 mA |
| Efficiency | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | $62.2 \%$ |
| Output Ripple With Optional Filter | $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=100 \mathrm{~mA}$ | 70 mVpp |

Figure 12. Voltage Inverting Converter


Figure 13. External Current Boost Connections for $I_{C}$ Peak Greater than 1.5 A

## 13a. External NPN Switch

13b. External PNP Saturated Switch

MC34063A, MC33063A

(Top view, copper foil as seen through the board from the component side)


Figure 14. Printed Circuit Board and Component Layout
(Circuits of Figures 8, 10, 12)

INDUCTOR DATA

| Converter | Inductance $(\mu \mathrm{H})$ | Turns/Wire |
| :--- | :---: | :---: |
| Step-Up | 170 | 38 Turns of \#22 AWG |
| Step-Down | 220 | 48 Turns of \#22 AWG |
| Voltage-Inverting | 88 | 28 Turns of \#22 AWG |

All inductors are wound on Magnetics Inc. 55117 toroidal core.

## MC34063A, MC33063A

| Calculation | Step-Up | Step-Down | Voltage-Inverting |
| :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {on }} / \mathrm{toff}$ | $\frac{V_{\text {out }}+V_{F}-V_{\text {in(min })}}{V_{\text {in(min })}-V_{\text {sat }}}$ | $\frac{v_{\text {out }}+v_{F}}{V_{\text {in(min })}-v_{\text {sat }}-v_{\text {out }}}$ | $\frac{\left\|V_{\text {out }}\right\|+V_{F}}{V_{\text {in }}-V_{\text {sat }}}$ |
| $\left(\mathrm{ton}_{\text {on }}+\mathrm{t}_{\text {off }}\right)$ | $\frac{1}{f}$ | $\frac{1}{f}$ | $\frac{1}{f}$ |
| toff | $\frac{t_{\text {on }}+t_{\text {off }}}{\frac{t_{\text {on }}}{t_{\text {off }}}+1}$ | $\frac{t_{\text {on }}+t_{\text {off }}}{\frac{t_{\text {on }}}{t_{\text {off }}}+1}$ | $\frac{t_{\text {on }}+t_{\text {off }}}{\frac{t_{\text {on }}}{t_{\text {off }}}+1}$ |
| $\mathrm{t}_{\text {on }}$ | $\left(\mathrm{t}_{\text {on }}+\mathrm{t}_{\text {off }}\right)-\mathrm{t}_{\text {off }}$ | $\left(\mathrm{ton}_{\text {of }}+\mathrm{t}_{\text {off }}\right)-\mathrm{t}_{\text {off }}$ | $\left(\mathrm{t}_{\text {on }}+\mathrm{t}_{\text {off }}\right)-\mathrm{t}_{\text {off }}$ |
| $\mathrm{C}_{\text {T }}$ | $4.0 \times 10^{-5} \mathrm{t}_{\text {on }}$ | $4.0 \times 10^{-5} \mathrm{t}_{\text {on }}$ | $4.0 \times 10^{-5} \mathrm{t}_{\text {on }}$ |
| 1 pk (switch) | $2 \mathrm{l}_{\text {out(max) }}\left(\frac{\mathrm{t}_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right)$ | ${ }^{21}$ out(max) | $2 \mathrm{l}_{\text {out(max) }}\left(\frac{\mathrm{t}_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right)$ |
| $\mathrm{R}_{\text {sc }}$ | 0.3/lop(switch) | 0.3/l $/ \mathrm{pk}$ (switch) | 0.3/ $/ \mathrm{lk}$ (switch) |
| $\mathrm{L}_{\text {(min) }}$ | $\left(\frac{\left(\mathrm{V}_{\text {in(min) }}-\mathrm{V}_{\text {sat }}\right)}{\mathrm{I}_{\mathrm{pk}(\text { switch })}}\right) \mathrm{t}_{\text {on(max })}$ | $\left(\frac{\left(V_{\text {in(min) }}-V_{\text {sat }}-V_{\text {out }}\right)}{\mathrm{I}_{\mathrm{pk}(\text { switch })}}\right)^{\mathrm{t}_{\text {on(max }}}$ | $\left(\frac{\left(V_{\text {in(min) }}-V_{\text {sat }}\right)}{\mathrm{I}_{\mathrm{pk}(\text { switch })}}\right) \mathrm{t}_{\text {on(max })}$ |
| $\mathrm{C}_{0}$ | $9 \frac{\mathrm{I}_{\text {out }} \mathrm{t}_{\mathrm{on}}}{\mathrm{~V}_{\text {ripple(pp) }}}$ | $\frac{\mathrm{I}_{\mathrm{pk}(\text { switch })}\left(\mathrm{t}_{\text {on }}+\mathrm{t}_{\text {off }}\right)}{8 \mathrm{~V}_{\text {ripple }(\mathrm{pp})}}$ | $9 \frac{\mathrm{I}_{\text {out }}{ }^{\text {ton }}}{} \mathrm{V}_{\text {ripple(pp) }}$ |

$V_{\text {sat }}=$ Saturation voltage of the output switch.
$\mathrm{V}_{\mathrm{F}}=$ Forward voltage drop of the output rectifier.
The following power supply characteristics must be chosen:
$\mathrm{V}_{\text {in }}$ - Nominal input voltage.
$\mathrm{V}_{\text {out }}$ - Desired output voltage, $\left|\mathrm{V}_{\text {out }}\right|=1.25\left(1+\frac{\mathrm{R} 2}{\mathrm{R} 1}\right)$
$I_{\text {out }}$ - Desired output current.
$f_{\text {min }}$ - Minimum desired output switching frequency at the selected values of $V_{\text {in }}$ and $I_{O}$.
$\mathrm{V}_{\text {ripple(pp) }}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.
NOTE: For further information refer to Application Note AN920A/D and AN954/D.

Figure 15. Design Formula Table

MC34063A, MC33063A
ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33063AD | SO-8 | 98 Units / Rail |
| MC33063ADR2 | SO-8 | 2500 Units / Tape \& Reel |
| MC33063AP1 | DIP-8 | 50 Units / Rail |
| MC33063AVD | SO-8 | 98 Units / Rail |
| MC33063AVDR2 | SO-8 | 2500 Units / Tape \& Reel |
| MC33063AVP | DIP-8 | 50 Units / Rail |
| MC34063AD | SO-8 | 98 Units / Rail |
| MC34063ADR2 | SO-8 | 2500 Units / Tape \& Reel |
| MC34063AP1 | DIP-8 | 50 Units / Rail |

## MARKING DIAGRAMS

PDIP-8
P, P1 SUFFIX CASE 626


| X | $=3$ or 4 |
| :--- | :--- |
| A | $=$ Assembly Location |
| WL, L | $=$ Wafer Lot |
| YY, Y | $=$ Year |
| WW, W | $=$ Work Week |

## MC34163, MC33163

### 3.4 A, Step-Up/Down/ Inverting Switching Regulators

The MC34163 series are monolithic power switching regulators that contain the primary functions required for dc-to-dc converters. This series is specifically designed to be incorporated in step-up, step-down, and voltage-inverting applications with a minimum number of external components.

These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- Output Switch Current in Excess of 3.0 A
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision $2 \%$ Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-by-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package
- Moisture Sensitivity Level (MSL) Equals 1


Figure 1. Representative Block Diagram


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33163DW | SO-16W | 47 Units/Rail |
| MC33163DWR2 | SO-16W | 1000 Tape \& Reel |
| MC33163P | PDIP-16 | 25 Units/Rail |
| MC34163DW | SO-16W | 47 Units/Rail |
| MC34163DWR2 | SO-16W | 1000 Tape \& Reel |
| MC34163P | PDIP-16 | 25 Units/Rail |

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| Switch Collector Voltage Range | $\mathrm{V}_{\mathrm{C} \text { (switch) }}$ | -1.0 to +40 | V |
| Switch Emitter Voltage Range | $\mathrm{V}_{\mathrm{E}(\text { switch) }}$ | - 2.0 to $\mathrm{V}_{\mathrm{C} \text { (switch) }}$ | V |
| Switch Collector to Emitter Voltage | $\mathrm{V}_{\mathrm{CE} \text { (switch) }}$ | 40 | V |
| Switch Current (Note 2) | Isw | 3.4 | A |
| Driver Collector Voltage | $\mathrm{V}_{\mathrm{C} \text { (driver) }}$ | -1.0 to +40 | V |
| Driver Collector Current | $\mathrm{I}_{\mathrm{C} \text { (driver) }}$ | 150 | mA |
| Bootstrap Input Current Range (Note 2) | $\mathrm{I}_{\mathrm{BS}}$ | -100 to +100 | mA |
| Current Sense Input Voltage Range | $\mathrm{V}_{\text {lpk }}$ (Sense) | $\left(\mathrm{V}_{\mathrm{CC}}-7.0\right)$ to $\left(\mathrm{V}_{\mathrm{CC}}+1.0\right)$ | V |
| Feedback and Timing Capacitor Input Voltage Range | $V_{\text {in }}$ | -1.0 to +7.0 | V |
| Low Voltage Indicator Output Voltage Range | $\mathrm{V}_{\mathrm{C} \text { (LVI) }}$ | -1.0 to +40 | V |
| Low Voltage Indicator Output Sink Current | $\mathrm{I}_{\mathrm{C}(\mathrm{LVI})}$ | 10 | mA |
| Thermal Characteristics <br> P Suffix, Dual-In-Line Case 648C <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13) <br> DW Suffix, Surface Mount Case 751G <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case (Pins 4, 5, 12, 13) | $R_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJc }}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | $\begin{aligned} & 80 \\ & 15 \\ & \\ & 94 \\ & 18 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 4) <br> MC34163 <br> MC33163 | $\mathrm{T}_{\mathrm{A}}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$, Pin $16=\mathrm{V}_{\mathrm{CC}}, \mathrm{C}_{\mathrm{T}}=620 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies (Note 4), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| ```Frequency \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) Total Variation over \(\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}\) to 40 V , and Temperature``` | fosc | $\begin{aligned} & 46 \\ & 45 \end{aligned}$ | $50$ | $\begin{aligned} & 54 \\ & 55 \end{aligned}$ | kHz |
| Charge Current | $I_{\text {chg }}$ | - | 225 | - | $\mu \mathrm{A}$ |
| Discharge Current | $\mathrm{l}_{\text {dischg }}$ | - | 25 | - | $\mu \mathrm{A}$ |
| Charge to Discharge Current Ratio | $\mathrm{I}_{\text {chg }} / \mathrm{Id}$ dischg | 8.0 | 9.0 | 10 | - |
| Sawtooth Peak Voltage | $\mathrm{V}_{\text {Osc (P) }}$ | - | 1.25 | - | V |
| Sawtooth Valley Voltage | V Osc(V) | - | 0.55 | - | V |

FEEDBACK COMPARATOR 1

| Threshold Voltage | $\mathrm{V}_{\mathrm{th}(\mathrm{FB} 1)}$ |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 4.9 | 5.05 | 5.2 | V |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}\right.$ to $\left.40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ |  | - | 0.008 | 0.03 | $\% / \mathrm{V}$ |
| Total Variation over Line, and Temperature |  | 4.85 | - | 5.25 | V |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{FB} 1}=5.05 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}(\mathrm{FB} 1)}$ | - | 100 | 200 | $\mu \mathrm{~A}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 1500 V per MIL-STD-883, Method 3015.
Machine Model Method 150 V .
2. Maximum package power dissipation limits must be observed.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34163
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34163
$=-40^{\circ} \mathrm{C}$ for MC33163 $\quad=+85^{\circ} \mathrm{C}$ for MC33163

## MC34163, MC33163

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$, Pin $16=\mathrm{V}_{\mathrm{CC}}, \mathrm{C}_{\mathrm{T}}=620 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $T_{A}$ is the operating ambient temperature range that applies (Note 6), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| FEEDBACK COMPARATOR 2 |  |  |  |  |  |
| Threshold Voltage $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) Total Variation over Line, and Temperature | $\mathrm{V}_{\text {th(FB2 }}$ | $\begin{gathered} 1.225 \\ - \\ 1.213 \end{gathered}$ | $\begin{aligned} & 1.25 \\ & 0.008 \end{aligned}$ | $\begin{gathered} 1.275 \\ 0.03 \\ 1.287 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \% / \mathrm{V} \\ \mathrm{~V} \end{gathered}$ |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB} 2}=1.25 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{B} \text { (FB2) }}$ | -0.4 | 0 | 0.4 | $\mu \mathrm{A}$ |

CURRENT LIMIT COMPARATOR

| Threshold Voltage <br> $T_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Total Variation over $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}$ to 40 V , and Temperature | $\mathrm{V}_{\text {th(lpk Sense) }}$ | - | 250 | - | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{Ipk}}(\right.$ Sense $\left.)=15 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}(\text { sense })}$ | - | 1.0 | 20 | $\mu \mathrm{~A}$ |

DRIVER AND OUTPUT SWITCH (Note 5)
$\left.\begin{array}{|l|c|c|c|c|c|}\hline \text { Sink Saturation Voltage (ISW }=2.5 \mathrm{~A}, \text { Pins } 14,15 \text { grounded) } & \mathrm{V}_{\mathrm{CE} \text { (sat) }} & & & & \mathrm{V} \\ \text { Non-Darlington Connection }\left(R_{\text {Pin }}=110 \Omega \text { to } \mathrm{V}_{\mathrm{CC}}, \mathrm{I}_{\mathrm{SW}} / \mathrm{I}_{\mathrm{DRV}} \approx 20\right) & & - & 0.6 & 1.0 & \\ \text { Darlington Connection (Pins } 9,10,11 \text { connected) }\end{array}\right)$

LOW VOLTAGE INDICATOR

| Input Threshold ( $\mathrm{V}_{\mathrm{FB} 2}$ Increasing $)$ | $\mathrm{V}_{\mathrm{th}}$ | 1.07 | 1.125 | 1.18 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Hysteresis $\left(\mathrm{V}_{\mathrm{FB} 2}\right.$ Decreasing $)$ | $\mathrm{V}_{\mathrm{H}}$ | - | 15 | - | mV |
| Output Sink Saturation Voltage $\left(\mathrm{I}_{\text {sink }}=2.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OL}(\mathrm{LVI})}$ | - | 0.15 | 0.4 | V |
| Output Off-State Leakage Current $\left(\mathrm{V}_{\mathrm{OH}}=15 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{OH}}$ | - | 0.01 | 5.0 | $\mu \mathrm{~A}$ |

TOTAL DEVICE

| Standby Supply Current $\left(V_{C C}=2.5\right.$ <br> Pins $6,14,15=G$ to 40 V, , Pin $8=V_{C C}$, | $\mathrm{I}_{\mathrm{CC}}$ | - | 6.0 | 10 | mA |
| :--- | :--- | :--- | :--- | :--- | :--- |

5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34163 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34163
$=-40^{\circ} \mathrm{C}$ for MC33163 $=+85^{\circ} \mathrm{C}$ for MC33163


Figure 2. Output Switch On-Off Time versus Oscillator Timing Capacitor


Figure 3. Oscillator Frequency Change versus Temperature


Figure 4. Feedback Comparator 1 Input Bias Current versus Temperature


Figure 6. Bootstrap Input Current Source versus Temperature


Figure 8. Output Switch Source Saturation versus Emitter Current


Figure 5. Feedback Comparator 2 Threshold Voltage versus Temperature


Figure 7. Bootstrap Input Zener Clamp Voltage versus Temperature


Figure 9. Output Switch Sink Saturation versus Collector Current


Figure 10. Output Switch Negative Emitter Voltage versus Temperature


Figure 12. Current Limit Comparator Threshold Voltage versus Temperature


Figure 11. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current


Figure 13. Current Limit Comparator Input Bias Current versus Temperature


Figure 14. Standby Supply Current versus Supply Voltage


Figure 15. Standby Supply Current versus Temperature


Figure 16. Minimum Operating Supply Voltage versus Temperature


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 18. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC34163, MC33163



Figure 19. Representative Block Diagram


Figure 20. Typical Operating Waveforms

## INTRODUCTION

The MC34163 series are monolithic power switching regulators optimized for dc-to-dc converter applications. The combination of features in this series enables the system designer to directly implement step-up, step-down, and voltage-inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 19.

## OPERATING DESCRIPTION

The MC34163 operates as a fixed on-time, variable off-time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 20. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

## Oscillator

The oscillator frequency and on-time of the output switch are programmed by the value selected for timing capacitor $\mathrm{C}_{\mathrm{T}}$. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As $\mathrm{C}_{\mathrm{T}}$ charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp-up and can be enabled by the comparator output only at the start of ramp-down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V , respectively, with a charge current of $225 \mu \mathrm{~A}$ and a discharge current of $25 \mu \mathrm{~A}$, yielding a maximum on-time duty cycle of $90 \%$. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition
of an external deadtime resistor $\left(\mathrm{R}_{\mathrm{DT}}\right)$ placed across $\mathrm{C}_{\mathrm{T}}$. The resistor increases the discharge current which reduces the on-time of the output switch. A graph of the Output Switch On-Off Time versus Oscillator Timing Capacitance for various values of $\mathrm{R}_{\mathrm{DT}}$ is shown in Figure 2. Note that the maximum output duty cycle, $\mathrm{t}_{\mathrm{on}} / \mathrm{t}_{\text {on }}+\mathrm{t}_{\text {off }}$, remains constant for values of $\mathrm{C}_{\mathrm{T}}$ greater than 0.2 nF . The converter output can be inhibited by clamping $\mathrm{C}_{\mathrm{T}}$ to ground with an external NPN small-signal transistor.

## Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is $\pm 0.4 \mu \mathrm{~A}$, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V , the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V . The additional 50 mV compensates for a $1.0 \%$ voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.
The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor-based systems. The inverting input is internally biased at 1.125 V , which sets the noninverting input thresholds to $90 \%$ of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 11). An external resistor $\left(\mathrm{R}_{\mathrm{LVI}}\right)$ and capacitor $\left(\mathrm{C}_{\mathrm{DLY}}\right)$ can be used to program a reset delay time ( $\mathrm{t}_{\mathrm{DLY}}$ ) by the formula shown below, where $\mathrm{V}_{\mathrm{th}(\mathrm{MPU})}$ is the microprocessor reset input threshold. Refer to Figure 21.

$$
t_{D L Y}=R_{L V I} C_{D L Y} \ln \left(\frac{1}{1-\frac{V_{\text {th }(M P U)}}{V_{\text {out }}}}\right)
$$

## Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, $\mathrm{R}_{\mathrm{SC}}$, in series with $\mathrm{V}_{\mathrm{CC}}$ and output switch transistor $\mathrm{Q}_{2}$. The voltage drop across $\mathrm{R}_{\mathrm{SC}}$ is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to $\mathrm{V}_{\mathrm{CC}}$, the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle. The calculation for a value of $\mathrm{R}_{\mathrm{SC}}$ is:

$$
\text { RSC }=\frac{0.25 \mathrm{~V}}{\operatorname{lpk}(\text { Switch })}
$$

Figures 12 and 13 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of $1.0 \mu \mathrm{~A}$. The propagation delay from the comparator input to the Output Switch is typically 200 ns . The parasitic inductance associated with $\mathrm{R}_{\mathrm{SC}}$ and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at $170^{\circ} \mathrm{C}$, the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

## Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5 A and is designed to switch a maximum of 40 V collector to emitter, with up to 3.4 A peak collector current. The minimum value for $\mathrm{R}_{\mathrm{SC}}$ is:

$$
\operatorname{RSC}(\min )=\frac{0.25 \mathrm{~V}}{3.4 \mathrm{~A}}=0.0735 \Omega
$$

When configured for step-down or voltage-inverting applications, as in Figures 21 and 25, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing
additional device heating and reduced conversion efficiency.

Figure 10 shows that by clamping the emitter to 0.5 V , the collector current will be in the range $10 \mu \mathrm{~A}$ over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.
A bootstrap input is provided to reduce the output switch saturation voltage in step-down and voltage-inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above $\mathrm{V}_{\mathrm{CC}}$. An internal zener limits the bootstrap input voltage to $\mathrm{V}_{\mathrm{CC}}$ +7.0 V. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA . An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$
\mathrm{C}_{\mathrm{B}(\min )}=\mathrm{I} \frac{\Delta \mathrm{t}}{\Delta \mathrm{~V}}=4.0 \mathrm{~mA} \frac{\mathrm{t}_{\mathrm{on}}}{4.0 \mathrm{~V}}=0.001 \mathrm{t} \mathrm{ton}
$$

Parametric operation of the MC34163 is guaranteed over a supply voltage range of 2.5 V to 40 V . When operating below 3.0 V , the Bootstrap Input should be connected to $\mathrm{V}_{\mathrm{CC}}$. Figure 16 shows that functional operation down to 1.7 V at room temperature is possible.

## Package

The MC34163 is contained in a heatsinkable 16-lead plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 17 and 18 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction-to-air thermal resistance. These examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

## APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.


| Test | Condition | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$ to $24 \mathrm{~V}, \mathrm{I}=3.0 \mathrm{~A}$ | $6.0 \mathrm{mV}= \pm 0.06 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.6 \mathrm{~A}$ to 3.0 A | $2.0 \mathrm{mV}= \pm 0.02 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}$ | 36 mVpp |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 3.3 A |
| Efficiency, Without Bootstrap | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}$ | $76.7 \%$ |
| Efficiency, With Bootstrap | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=3.0 \mathrm{~A}$ | $81.2 \%$ |

Figure 21. Step-Down Converter


Figure 22A. External NPN Switch
Figure 22. External Current Boost Connections for $\mathrm{I}_{\mathrm{pk}}$ (Switch) Greater Than 3.4 A

## MC34163, MC33163



| Test | Condition | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=9.0 \mathrm{~V}$ to $16 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.6 \mathrm{~A}$ | $30 \mathrm{mV}= \pm 0.05 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~A}$ to 0.6 A | $50 \mathrm{mV}= \pm 0.09 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.6 \mathrm{~A}$ | 140 mVpp |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.6 \mathrm{~A}$ | $88.1 \%$ |

Figure 23. Step-Up Converter


Figure 24A. External NPN Switch


Figure 24B. External PNP Saturated Switch

Figure 24. External Current Boost Connections for $\mathrm{I}_{\mathrm{pk}}($ Switch) Greater Than 3.4 A

## MC34163, MC33163



| Test | Condition | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=9.0 \mathrm{~V}$ to $16 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | $5.0 \mathrm{mV}= \pm 0.02 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.6 \mathrm{~A}$ to 1.0 A | $2.0 \mathrm{mV}= \pm 0.01 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | 130 mVpp |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 3.2 A |
| Efficiency, Without Bootstrap | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | $73.1 \%$ |
| Efficiency, With Bootstrap | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | $77.5 \%$ |

Figure 25. Voltage-Inverting Converter


Figure 26. External Current Boost Connections for $\mathrm{I}_{\mathrm{pk}}$ (Switch) Greater Than 3.4 A


Figure 27. Printed Circuit Board and Component Layout (Circuits of Figures 21, 23, 25)

## MC34163, MC33163

| Calculation | Step-Down | Step-Up | Voltage-Inverting |
| :---: | :---: | :---: | :---: |
| $\left.\frac{t_{o n}}{(\text { Notesolf }} 2,3\right)$ | $\frac{V_{\text {out }}+V_{F}}{V_{\text {in }}-V_{\text {sat }}-V_{\text {out }}}$ | $\frac{V_{\text {out }}+V_{F}-V_{\text {in }}}{V_{\text {in }}-V_{\text {sat }}}$ | $\frac{\left\|V_{\text {out }}\right\|+V_{F}}{V_{\text {in }}-V_{\text {sat }}}$ |
| ton | $\frac{\frac{t_{\mathrm{on}}}{\mathrm{t}_{\mathrm{off}}}}{f\left(\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{t}_{\mathrm{off}}}+1\right)}$ | $\frac{\frac{t_{\mathrm{on}}}{\mathrm{t}_{\mathrm{off}}}}{f\left(\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{t}_{\mathrm{off}}}+1\right)}$ | $\frac{\frac{t_{\text {on }}}{t_{\text {off }}}}{f\left(\frac{t_{\text {on }}}{t_{\text {off }}}+1\right)}$ |
| $\mathrm{C}^{\top}$ | $\frac{32.143 \cdot 10^{-6}}{f}$ | $\frac{32.143 \cdot 10^{-6}}{f}$ | $\frac{32.143 \cdot 10^{-6}}{f}$ |
| IL(avg) | lout | $\mathrm{I}_{\text {out }}\left(\frac{\mathrm{t}_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right)$ | $\mathrm{I}_{\text {out }}\left(\frac{\mathrm{t}_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right)$ |
| Ipk (Switch) | $\mathrm{L}(\mathrm{avg})+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}$ | $\mathrm{L}($ avg $)+\frac{\Delta l_{L}}{2}$ | $\mathrm{L}($ avg $)+\frac{\Delta I_{L}}{2}$ |
| RSC | $\frac{0.25}{\text { lpk (Switch) }}$ | $\frac{0.25}{\text { Ipk (Switch) }}$ | $\frac{0.25}{\text { Ipk (Switch) }}$ |
| L | $\left(\frac{v_{\text {in }}-v_{\text {sat }}-v_{\text {out }}}{\Delta \mathrm{I}_{\mathrm{L}}}\right) \mathrm{t}_{\text {on }}$ | $\left(\frac{v_{\text {in }}-v_{\text {sat }}}{\Delta I_{L}}\right) t_{\text {on }}$ | $\left(\frac{v_{\text {in }}-v_{\text {sat }}}{\Delta \mathrm{I}_{\mathrm{L}}}\right) \mathrm{t}_{\text {on }}$ |
| $\mathrm{V}_{\text {ripple(pp) }}$ | $\Delta \mathrm{IL} \sqrt{\left(\frac{1}{8 \mathrm{CO}_{\mathrm{O}}}\right)^{2}+(\mathrm{ESR})^{2}}$ | $\approx \frac{t_{\text {on }} I_{\text {out }}}{C_{\mathrm{O}}}$ | $\approx \frac{t_{\text {on }} I_{\text {out }}}{C_{\mathrm{O}}}$ |
| Vout | $\mathrm{V}_{\text {ref }}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ | $\mathrm{V}_{\text {ref }}\left(\frac{R_{2}}{R_{1}}+1\right)$ | $\mathrm{V}_{\text {ref }}\left(\frac{R_{2}}{R_{1}}+1\right)$ |

The following Converter Characteristics must be chosen:
$V_{\text {in }}$ - Nominal operating input voltage.
$V_{\text {out }}$ - Desired output voltage.
$\mathrm{I}_{\text {out }}$ - Desired output current.
$\Delta_{\mathrm{L}}$ - Desired peak-to-peak inductor ripple current. For maximum output current it is suggested that $\Delta_{\mathrm{L}}$ be chosen to be less

> threshold set by $R_{S C}$. If the design goal is to use a minimum inductance value, let $\Delta_{\mathrm{L}}=2$ ( $\mathrm{L}(\mathrm{avg})$ ). This will proportionally reduce converter output current capability.
> $f$ - Maximum output switch frequency.
> $\mathrm{V}_{\text {ripple(pp) }}$ - Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor $\mathrm{C}_{\mathrm{O}}$ should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

NOTES: 1. $\mathrm{V}_{\text {sat }}$ - Saturation voltage of the output switch, refer to Figures 8 and 9.
2. $\mathrm{V}_{F}$ - Output rectifier forward voltage drop. Typical value for 1 N 5822 Schottky barrier rectifier is 0.5 V .
3. The calculated $\mathrm{t}_{\mathrm{on}} / \mathrm{t}_{\text {off }}$ must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8 , at the minimum operating input voltage.

Figure 28. Design Equations

## MC34166, MC33166

### 3.0 A, Step-Up/Down/ Inverting Switching Regulators

The MC34166, MC33166 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc-to-dc converters. This series was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to $36 \mu \mathrm{~A}$.

- Output Switch Current in Excess of 3.0 A
- Fixed Frequency Oscillator ( 72 kHz ) with On-Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision $2 \%$ Reference
- 0\% to $95 \%$ Output Duty Cycle
- Cycle-by-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to $36 \mu \mathrm{~A}$
- Economical 5-Lead TO-220 Package with Two Optional Leadforms
- Also Available in Surface Mount D ${ }^{2}$ PAK Package
- Moisture Sensitivity Level (MSL) Equals 1


Figure 1. Simplified Block Diagram
(Step Down Application)


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Heatsink surface connected to Pin 3


Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V VCC
5. Compensation/Standby


Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1545 of this data sheet.

MAXIMUM RATINGS (Note 2)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| Switch Output Voltage Range | $\mathrm{V}_{\mathrm{O}(\text { switch }}$ | -1.5 to $+\mathrm{V}_{\text {in }}$ | V |
| Voltage Feedback and Compensation Input Voltage Range | $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{Comp}}$ | -1.0 to +7.0 | V |
| Power Dissipation |  |  |  |
| Case 314A, 314B and 314D $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | W |
| Thermal Resistance, Junction-to-Ambient | $\theta_{\mathrm{JA}}$ | 65 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case | $\theta_{\mathrm{JC}}$ | 5.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Case 936A (D$\left.{ }^{2} \mathrm{PAK}\right)\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{P}_{\mathrm{D}}$ | Internally Limited | W |
| Thermal Resistance, Junction-to-Ambient | $\theta_{\mathrm{JA}}$ | 70 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case | $\theta_{\mathrm{JC}}$ | 5.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 3) | $\mathrm{T}_{\mathrm{A}}$ |  | ${ }^{\circ} \mathrm{C}$ |
| MC34166 |  | 0 to +70 |  |
| MC33166 |  | -40 to +85 |  |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V.
3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34166 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34166
$=-40^{\circ} \mathrm{C}$ for MC33166

## MC34166, MC33166

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$, for typical values $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Notes 4, 5], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
|  | fosc | $\begin{aligned} & \hline 65 \\ & 62 \end{aligned}$ | $72$ | $\begin{aligned} & 79 \\ & 81 \end{aligned}$ | kHz |
| ERROR AMPLIFIER |  |  |  |  |  |
| $\begin{array}{ll}\text { Voltage Feedback Input Threshold } & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}\end{array}$ | $\mathrm{V}_{\mathrm{FB} \text { (th) }}$ | $\begin{aligned} & 4.95 \\ & 4.85 \end{aligned}$ | $5.05$ | $\begin{gathered} \hline 5.15 \\ 5.2 \end{gathered}$ | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=7.5 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) | Regline | - | 0.03 | 0.078 | \%/V |
| Input Bias Current ( $\left.\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{FB} \text { (th) }}+0.15 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{B}}$ | - | 0.15 | 1.0 | $\mu \mathrm{A}$ |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to $20 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz}$ ) | PSRR | 60 | 80 | - | dB |
| $\begin{aligned} & \text { Output Voltage Swing } \\ & \text { High State }\left(I_{\text {Source }}=75 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}=4.5 \mathrm{~V}\right) \\ & \text { Low State }\left(I_{\text {Sink }}=0.4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=5.5 \mathrm{~V}\right) \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | 4.2 | $\begin{aligned} & 4.9 \\ & 1.6 \end{aligned}$ | $\overline{1.9}$ | V |

PWM COMPARATOR

| Duty Cycle |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum $\left(\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\max )}$ | 92 | 95 | 100 | $\%$ |
| Minimum $\left(\mathrm{V}_{\text {Comp }}=1.9 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\min )}$ | 0 | 0 | 0 |  |

## SWITCH OUTPUT

| Output Voltage Source Saturation ( $\left.\mathrm{V}_{\mathrm{CC}}=7.5 \mathrm{~V}, \mathrm{I}_{\text {Source }}=3.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{sat}}$ | - | $\left(\mathrm{V}_{\mathrm{CC}}\right.$ <br> $-1.5)$ | $\left(\mathrm{V}_{\mathrm{CC}}\right.$ <br> $-1.8)$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Off-State Leakage (V $\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}$, Pin 2 = Gnd) | $\mathrm{I}_{\mathrm{sw}(\mathrm{off})}$ | - | 0 | 100 | $\mu \mathrm{~A}$ |
| Current Limit Threshold | $\mathrm{I}_{\mathrm{pk}(\text { switch })}$ | 3.3 | 4.3 | 6.0 | A |
| Switching Times $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{I}_{\mathrm{pk}}=3.0 \mathrm{~A}, \mathrm{~L}=375 \mu \mathrm{H}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ |  |  |  |  | ns |
| Output Voltage Rise Time | $\mathrm{t}_{\mathrm{r}}$ | - | 100 | 200 |  |
| Output Voltage Fall Time | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | 100 |  |

UNDERVOLTAGE LOCKOUT

| Startup Threshold $\left(\mathrm{V}_{\mathrm{CC}}\right.$ Increasing, $\left.\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{th}(\mathrm{UVLO})}$ | 5.5 | 5.9 | 6.3 | V |
| :--- | :--- | :--- | :--- | :--- | :---: |
| Hysteresis $\left(\mathrm{V}_{\mathrm{CC}}\right.$ Decreasing, $\left.\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{H}(\mathrm{UVLO})}$ | 0.6 | 0.9 | 1.2 | V |

## TOTAL DEVICE

| Power Supply Current $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Standby $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{Comp}}<0.15 \mathrm{~V}\right)$ | - | 36 | 100 | $\mu \mathrm{~A}$ |  |
| Operating (VCC $=40 \mathrm{~V}$, Pin $1=$ Gnd for maximum duty cycle $)$ |  | - | 31 | 55 | mA |

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34166
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34166
$=-40^{\circ} \mathrm{C}$ for MC33166 $=+85^{\circ} \mathrm{C}$ for MC33166


Figure 2. Voltage Feedback Input Threshold versus Temperature


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency


Figure 6. Oscillator Frequency Change versus Temperature


Figure 3. Voltage Feedback Input Bias Current versus Temperature


Figure 5. Error Amp Output Saturation versus Sink Current


Figure 7. Switch Output Duty Cycle versus Compensation Voltage


Figure 8. Switch Output Source Saturation versus Source Current


Figure 9. Negative Switch Output Voltage versus Temperature


Figure 11. Standby Supply Current versus Supply Voltage


Figure 13. Operating Supply Current versus Supply Voltage


Figure 14. MC34166 Representative Block Diagram


Figure 15. Timing Diagram

## MC34166, MC33166

## INTRODUCTION

The MC34166, MC33166 series are monolithic power switching regulators that are optimized for dc-to-dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. They can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 14.

## Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor $\mathrm{C}_{\mathrm{T}}$ and a trimmed current source. The charge to discharge ratio is controlled to yield a $95 \%$ maximum duty cycle at the Switch Output. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

## Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when $\mathrm{C}_{\mathrm{T}}$ is discharged to the oscillator valley voltage. As $\mathrm{C}_{\mathrm{T}}$ charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 7 and 15 illustrate the switch output duty cycle versus the compensation voltage.

## Current Sense

The MC34166 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set
at 4.3 A. Figure 10 illustrates switch output current limit threshold versus temperature.

## Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB , and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 4). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of $\pm 2.0 \%$ at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a $1.0 \%$ voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V , resistor $\mathrm{R}_{1}$ must be added to form a divider network at the feedback input as shown in Figures 14 and 19. The equation for determining the output voltage with the divider network is:

$$
\mathrm{V}_{\text {out }}=5.05\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)
$$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor $\left(\mathrm{R}_{2}\right)$ from the regulated output to the inverting input, and a series resistor-capacitor $\left(\mathrm{R}_{\mathrm{F}}, \mathrm{C}_{\mathrm{F}}\right)$ between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 19) is the easiest to compensate for stability. The step-up (Figure 21) and voltage-inverting (Figure 23) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting $R_{F}$ and $\mathrm{C}_{\mathrm{F}}$ for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV , the internal circuitry will be placed into a low power standby mode, reducing the power supply current to $36 \mu \mathrm{~A}$ with a 12 V supply voltage. Figure 11 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a $100 \mu \mathrm{~A}$ current source pull-up that can be used to implement soft-start. Figure 18 shows the current source charging capacitor $\mathrm{C}_{\text {SS }}$ through a series diode. The diode disconnects $\mathrm{C}_{\mathrm{SS}}$ from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

## MC34166, MC33166

## Switch Output

The output transistor is designed to switch a maximum of 40 V , with a minimum peak collector current of 3.3 A . When configured for step-down or voltage-inverting applications, as in Figures 19 and 23, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 9 shows that by clamping the emitter to 0.5 V , the collector current will be in the range of $100 \mu \mathrm{~A}$ over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

## Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully
functional before the output stage is enabled. The internal 5.05 V reference is monitored by the comparator which enables the output stage when $\mathrm{V}_{\mathrm{CC}}$ exceeds 5.9 V . To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

## Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at $170^{\circ} \mathrm{C}$, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking. The MC34166 is contained in a 5-lead TO-220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

## DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire-wrap or plug-in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a
tight component layout is recommended. Capacitors $\mathrm{C}_{\text {IN }}$, $\mathrm{C}_{\mathrm{O}}$, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

## MC34166, MC33166



Figure 16. Low Power Standby Circuit


Figure 17. Over Voltage Shutdown Circuit


Figure 18. Soft-Start Circuit


L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step-Down Converter application is shown in Figure 19. The output switch transistor $Q_{1}$ interrupts the input voltage, generating a squarewave at the LC o filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between $V_{\text {in }}$ and $V_{\text {ref }}$ by controlling the percent conduction time of $Q_{1}$ to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V , resistor $\mathrm{R}_{1}$ must be added to form a divider network at the feedback input.

Figure 19. Step-Down Converter


Figure 20. Step-Down Converter Printed Circuit Board and Component Layout


L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. MC34166: 5903B, or 5930B MTP3055EL: 5925B
Figure 21 shows that the MC34166 can be configured as a step-up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the on-time of transistors $Q_{1}$ and $Q_{2}$. During the off-time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step-up converter circuit. The first advantage is that output short-circuit protection is provided by the MC34166, since $Q_{1}$ is directly in series with $V_{\text {in }}$ and the load. Second, the output voltage can be programmed to be less than $\mathrm{V}_{\text {in }}$. Notice that during the off-time, the inductor forward biases diodes $\mathrm{D}_{1}$ and $\mathrm{D}_{2}$, transferring its energy with respect to ground rather than with respect to $\mathrm{V}_{\text {in }}$. When operating with $\mathrm{V}_{\text {in }}$ greater than 20 V , a gate protection network is required for the MOSFET. The network consists of components $\mathrm{R}_{\mathrm{G}}, \mathrm{D}_{3}$, and $\mathrm{D}_{4}$.

Figure 21. Step-Up/Down Converter


Figure 22. Step-Up/Down Converter Printed Circuit Board and Component Layout


L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage-inverting converter with the MC34166. First, the Switch Output emitter is limited to -1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 23. This keeps the emitter of $Q_{1}$ positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across $\mathrm{R}_{1}$ is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage-Inverting Converter


Figure 24. Voltage-Inverting Converter Printed Circuit Board and Component Layout


| Tests |  | Conditions | Results |
| :---: | :---: | :---: | :---: |
| Line Regulation | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\mathrm{V}_{\text {in }}=15 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=2.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=300 \mathrm{~mA}, \mathrm{I}_{03}=100 \mathrm{~mA}$ | $\begin{aligned} & 4.0 \mathrm{mV}= \pm 0.04 \% \\ & 450 \mathrm{mV}= \pm 1.9 \% \\ & 350 \mathrm{mV}= \pm 1.5 \% \end{aligned}$ |
| Load Regulation | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\begin{aligned} & \mathrm{V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=500 \mathrm{~mA} \text { to } 2.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=300 \mathrm{~mA}, \mathrm{I}_{\mathrm{O3}}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=2.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=100 \mathrm{~mA} \text { to } 300 \mathrm{~mA}, \mathrm{I}_{\mathrm{O3}}=100 \mathrm{~mA} \\ & \mathrm{~V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=2.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=300 \mathrm{~mA}, \mathrm{I}_{\mathrm{O} 3}=30 \mathrm{~mA} \text { to } 100 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 2.0 \mathrm{mV}= \pm 0.02 \% \\ & 420 \mathrm{mV}= \pm 1.7 \% \\ & 310 \mathrm{mV}= \pm 1.3 \% \end{aligned}$ |
| Output Ripple | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\mathrm{V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=2.0 \mathrm{~A}, \mathrm{I}_{02}=300 \mathrm{~mA}, \mathrm{I}_{\mathrm{O} 3}=100 \mathrm{~mA}$ | 50 mV pp 25 mV pp 10 mV pp |
| Short Circuit Current | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\mathrm{V}_{\text {in }}=24 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | $\begin{aligned} & 4.3 \mathrm{~A} \\ & 1.83 \mathrm{~A} \\ & 1.47 \mathrm{~A} \end{aligned}$ |
| Efficiency | TOTAL | $\mathrm{V}_{\mathrm{in}}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=2.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=300 \mathrm{~mA}, \mathrm{I}_{\mathrm{O} 3}=100 \mathrm{~mA}$ | 83.3\% |

T1 = Primary: Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core. Secondary: $\mathrm{V}_{\mathrm{O} 2}-65$ turns of \#26 AWG

$$
\mathrm{V}_{\mathrm{O} 3}-96 \text { turns of \#28 AWG }
$$

Heatsink $=$ AAVID Engineering Inc. 5903B, or 5930B.
Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$
\# \operatorname{TURNS}_{(\mathrm{SEC})}=\frac{\mathrm{V}_{\mathrm{O}(\mathrm{SEC})}+\mathrm{V}_{\mathrm{F}(\mathrm{SEC})}}{\left(\frac{\mathrm{V}_{\mathrm{O}(\mathrm{PRI})}+\mathrm{V}_{\mathrm{F}(\mathrm{PRI})}}{\# \mathrm{TURNS}(\mathrm{PRI})}\right)}
$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than $33 \%$ of the total output power.

Figure 25. Triple Output Converter

$L=$ Coilcraft M1496-A or ELMACO CHK1050, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. 5903B or 5930B
Figure 26. Negative Input/Positive Output Regulator


Figure 27. Variable Motor Speed Control with EMF Feedback Sensing

## MC34166, MC33166



The MC34166 can be used cost effectively in off-line applications even though it is limited to a maximum input voltage of 40 V . Figure 28 shows a simple and efficient method for converting the AC line voltage down to 24 V . This preconverter has a total power rating of 125 W with a conversion efficiency of $90 \%$. Transformer $T_{1}$ provides output isolation from the AC line and isolation between each of the secondaries. The circuit self-oscillates at 50 kHz and is controlled by the saturation characteristics of $\mathrm{T}_{2}$. Multiple MC34166 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. Off-Line Preconverter


Figure 29. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC34166, MC33166

Table 1. Design Equations

| Calculation | Step-Down | Step-Up/Down | Voltage-Inverting |
| :---: | :---: | :---: | :---: |
| $\begin{gathered} \frac{t_{\text {on }}}{t_{\text {off }}} \\ (\text { Notes 1, 2) } \end{gathered}$ | $\frac{V_{\text {out }}+V_{F}}{V_{\text {in }}-V_{\text {sat }}-V_{\text {out }}}$ | $\frac{V_{\text {out }}+V_{F 1}+V_{F 2}}{V_{\text {in }}-V_{\text {satQ1 }}-V_{\text {satQ2 }}}$ | $\frac{\mid V_{\text {out }}+V_{F}}{V_{\text {in }}-V_{\text {sat }}}$ |
| $\mathrm{t}_{\text {on }}$ | $\frac{\frac{t_{\text {on }}}{t_{\text {toff }}}}{\operatorname{fosc}\left(\frac{t_{0 n}}{t_{\text {off }}}+1\right)}$ | $\frac{\frac{t_{\text {on }}}{t_{\text {off }}}}{\mathrm{fosc}^{\left(\frac{t_{0 n}}{t_{\text {off }}}+1\right)}}$ | $\frac{\frac{t_{0 n}}{t_{\text {off }}}}{\mathrm{fosc}^{\left(\frac{t_{\mathrm{on}}}{t_{\text {off }}}+1\right)}}$ |
| Duty Cycle (Note 3) | $\mathrm{t}_{\text {on }} \mathrm{f}_{\text {osc }}$ | $\mathrm{t}_{\text {on }} \mathrm{f}_{\text {osc }}$ | $\mathrm{t}_{\text {on }} \mathrm{f}_{\text {osc }}$ |
| L $\mathrm{Lavg}^{\text {a }}$ | Iout | $\mathrm{l}_{\text {out }}\left(\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{t}_{\text {off }}}+1\right)$ | $\mathrm{l}_{\text {out }}\left(\frac{\mathrm{t}_{\mathrm{on}}}{\mathrm{toff}}+1\right)$ |
| 1 lk (switch) | $\mathrm{LLavg}+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}$ | $\mathrm{LLavg}+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}$ | $\mathrm{LLavg}+\frac{\Delta L_{\mathrm{L}}}{2}$ |
| L | $\left(\frac{V_{\text {in }}-V_{\text {sat }}-V_{\text {out }}}{\Delta l_{\text {L }}}\right)_{\text {ton }}$ | $\left(\frac{V_{\text {in }}-V_{\text {satQ1 }}-\mathrm{V}_{\text {satQ2 }}}{\Delta \mathrm{l}_{\mathrm{L}}}\right)_{\text {ton }}$ | $\left(\frac{V_{\text {in }}-V_{\text {sat }}}{\Delta_{\mathrm{L}}}\right)_{\text {ton }}$ |
| $\mathrm{V}_{\text {ripple(pp) }}$ | $\Delta \mathrm{L} \mathrm{L} \sqrt{\left(\frac{1}{8 \mathrm{fosc} \mathrm{Co}_{0}}\right)^{2}+(\mathrm{ESR})^{2}}$ | $\left(\frac{t_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right) \sqrt{\left(\frac{1}{\mathrm{fosc}^{\text {oso }}}\right)^{2}+(\mathrm{ESR})^{2}}$ | $\left(\frac{t_{0 n}}{t_{\text {off }}}+1\right) \sqrt{\left(\frac{1}{f_{\text {osc }} C_{0}}\right)^{2}+(\mathrm{ESR})^{2}}$ |
| $V_{\text {out }}$ | $\mathrm{V}_{\text {ref }}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ | $\mathrm{V}_{\text {ref }}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ | $\mathrm{V}_{\text {ref }}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ |

1. $\mathrm{V}_{\text {sat }}-$ Switch Output source saturation voltage, refer to Figure 8.
2. $\mathrm{V}_{\mathrm{F}}$ - Output rectifier forward voltage drop. Typical value for 1 N5822 Schottky barrier rectifier is 0.5 V .
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $\mathrm{DC}_{(\max )}$ specification of 0.92 .

The following converter characteristics must be chosen:
$V_{\text {out }}$ - Desired output voltage.
$I_{\text {out }}$ - Desired output current.
$\Delta L_{\mathrm{L}}$ - Desired peak-to-peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5 , it is suggested that $\Delta I_{\mathrm{L}}$ be chosen to be less than $10 \%$ of the average inductor current $I_{\mathrm{L}}$ avg. This will help prevent $\mathrm{I}_{\mathrm{pk}(\text { switch })}$ from reaching the guaranteed minimum current limit threshold of 3.3 A. If the design goal is to use a minimum inductance value, let $\Delta L_{\mathrm{L}}=2\left(\mathrm{I}_{\mathrm{L}}\right.$ avg $)$. This will proportionally reduce the converter's output current capability.
$\mathrm{V}_{\text {ripple }(\mathrm{pp})}$ - Desired peak-to-peak output ripple voltage. For best performance, the ripple voltage should be kept to less than $2 \%$ of $\mathrm{V}_{\text {out }}$. Capacitor $\mathrm{C}_{\mathrm{O}}$ should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

## MC34166, MC33166

ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: |
| MC33166D2T | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | D²PAK (Surface Mount) | 50 Units/Rail |
| MC33166D2TR4 |  | $D^{2}$ PAK (Surface Mount) |  |
| MC33166T |  | TO-220 (Straight Lead) |  |
| MC33166TH |  | TO-220 (Horizontal Mount) |  |
| MC33166TV |  | TO-220 (Vertical Mount) |  |
| MC34166D2T | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | $\mathrm{D}^{2}$ PAK (Surface Mount) |  |
| MC34166D2TR4 |  | D²PAK (Surface Mount) |  |
| MC34166T |  | TO-220 (Straight Lead) |  |
| MC34166TH |  | TO-220 (Horizontal Mount) |  |
| MC34166TV |  | TO-220 (Vertical Mount) |  |

## MC34167, MC33167

### 5.0 A, Step-Up/Down/ Inverting Switching Regulators

The MC34167, MC33167 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc-to-dc converters. This series was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to $36 \mu \mathrm{~A}$.

- Output Switch Current in Excess of 5.0 A
- Fixed Frequency Oscillator ( 72 kHz ) with On-Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision $2 \%$ Reference
- 0\% to $95 \%$ Output Duty Cycle
- Cycle-by-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to $36 \mu \mathrm{~A}$
- Economical 5-Lead TO-220 Package with Two Optional Leadforms
- Also Available in Surface Mount D ${ }^{2}$ PAK Package
- Moisture Sensitivity Level (MSL) Equals 1


Figure 1. Simplified Block Diagram
(Step Down Application)


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


Heatsink surface connected to Pin 3


Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V CC
5. Compensation/Standby


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1562 of this data sheet.

MAXIMUM RATINGS (Note 2)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| Switch Output Voltage Range | $\mathrm{V}_{\text {O(switch) }}$ | -2.0 to $+\mathrm{V}_{\text {in }}$ | V |
| Voltage Feedback and Compensation Input Voltage Range | $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\text {Comp }}$ | -1.0 to +7.0 | V |
| Power Dissipation <br> Case 314A, 314B and 314D ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) <br> Thermal Resistance, Junction-to-Ambient <br> Thermal Resistance, Junction-to-Case <br> Case 936A ( $\mathrm{D}^{2} \mathrm{PAK}$ ) ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) <br> Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $P_{D}$ <br> $\theta_{\mathrm{JA}}$ <br> $\theta_{\mathrm{Jc}}$ <br> $P_{D}$ <br> $\theta_{\mathrm{JA}}$ <br> $\theta_{\mathrm{Jc}}$ | Internally Limited <br> 65 <br> 5.0 <br> Internally Limited <br> 70 <br> 5.0 | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | TJ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 3) MC34167 <br> MC33167 | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34167 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34167
$=-40^{\circ} \mathrm{C}$ for MC33167 $\quad=+85^{\circ} \mathrm{C}$ for MC33167

## MC34167, MC33167

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$, for typical values $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Notes 4, 5], unless otherwise noted.)

| Characteristic |  | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |  |
| Frequency ( $\mathrm{V}_{\mathrm{CC}}=7.5 \mathrm{~V}$ to 40 V ) | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | fosc | $\begin{aligned} & \hline 65 \\ & 62 \end{aligned}$ | $72$ | $\begin{aligned} & \hline 79 \\ & 81 \end{aligned}$ | kHz |

## ERROR AMPLIFIER

| $\begin{array}{ll}\text { Voltage Feedback Input Threshold } & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}\end{array}$ | $\mathrm{V}_{\mathrm{FB} \text { (th) }}$ | $\begin{aligned} & 4.95 \\ & 4.85 \end{aligned}$ | $5.05$ | $\begin{aligned} & \hline 5.15 \\ & 5.20 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=7.5 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{Reg}_{\text {line }}$ | - | 0.03 | 0.078 | \%/V |
| Input Bias Current ( $\left.\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{FB} \text { (th })}+0.15 \mathrm{~V}\right)$ | $\mathrm{I}_{1 \mathrm{~B}}$ | - | 0.15 | 1.0 | $\mu \mathrm{A}$ |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to $20 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz}$ ) | PSRR | 60 | 80 | - | dB |
| Output Voltage Swing High State ( ISource $=75 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{FB}}=4.5 \mathrm{~V}$ ) <br> Low State ( $\mathrm{I}_{\text {Sink }}=0.4 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=5.5 \mathrm{~V}$ ) | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $4.2$ | $\begin{aligned} & 4.9 \\ & 1.6 \end{aligned}$ | $1.9$ | V |

## PWM COMPARATOR

| Duty Cycle $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right)$ | Maximum $\left(\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}\right)$ <br>  <br>  Minimum $\left(\mathrm{V}_{\mathrm{Comp}}=1.9 \mathrm{~V}\right)$ | $\mathrm{DC}_{(\max )}$ | 92 | 95 | 100 | $\%$ |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{DC}_{(\min )}$ | 0 | 0 | 0 |  |  |  |

## SWITCH OUTPUT

| Output Voltage Source Saturation $\left(\mathrm{V}_{\mathrm{CC}}=7.5 \mathrm{~V}, \mathrm{I}_{\text {Source }}=5.0 \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{sat}}$ | - | $\left(\mathrm{V}_{\mathrm{CC}}-1.5\right)$ | $\left(\mathrm{V}_{\mathrm{CC}}-1.8\right)$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Off-State Leakage $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}\right.$, Pin $\left.2=\mathrm{Gnd}\right)$ | $\mathrm{I}_{\mathrm{sw}(\mathrm{off})}$ | - | 0 | 100 | $\mu \mathrm{~A}$ |
| Current Limit Threshold $\left(\mathrm{V}_{\mathrm{CC}}=7.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{pk}(\mathrm{switch})}$ | 5.5 | 6.5 | 8.0 | A |
| Switching Times $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{I}_{\mathrm{pk}}=5.0 \mathrm{~A}, \mathrm{~L}=225 \mu \mathrm{H}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ |  |  |  |  | ns |
| Output Voltage Rise Time | $\mathrm{t}_{\mathrm{r}}$ | - | 100 | 200 |  |
| Output Voltage Fall Time | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | 100 |  |

UNDERVOLTAGE LOCKOUT

| Startup Threshold $\left(\mathrm{V}_{\mathrm{CC}}\right.$ Increasing, $\left.\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {th(UVLO }}$ | 5.5 | 5.9 | 6.3 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Hysteresis $\left(\mathrm{V}_{\mathrm{CC}}\right.$ Decreasing, $\left.\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{H}(\mathrm{UVLO})}$ | 0.6 | 0.9 | 1.2 | V |

## TOTAL DEVICE

| Power Supply Current $\left(T_{A}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| Standby $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{Comp}}<0.15 \mathrm{~V}\right)$ |  | - | 36 | 100 |
| Operating $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \operatorname{Pin} 1=\mathrm{Gnd}\right.$ for maximum duty cycle $)$ |  | - | 40 | 60 |

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34167
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34167
$=-40^{\circ} \mathrm{C}$ for MC33167
$=+85^{\circ} \mathrm{C}$ for MC33167


Figure 2. Voltage Feedback Input Threshold versus Temperature


Figure 3. Voltage Feedback Input Bias Current versus Temperature


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency


Figure 5. Error Amp Output Saturation versus Sink Current


Figure 7. Switch Output Duty Cycle versus Compensation Voltage


Figure 8. Switch Output Source Saturation versus Source Current


Figure 9. Negative Switch Output Voltage versus Temperature


Figure 11. Standby Supply Current versus Supply Voltage


Figure 13. Operating Supply Current versus Supply Voltage

## MC34167, MC33167



Figure 14. MC34167 Representative Block Diagram


Figure 15. Timing Diagram

## INTRODUCTION

The MC34167, MC33167 series are monolithic power switching regulators that are optimized for dc-to-dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. They can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 14.

## Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor $\mathrm{C}_{\mathrm{T}}$ and a trimmed current source. The charge to discharge ratio is controlled to yield a $95 \%$ maximum duty cycle at the Switch Output. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

## Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when $\mathrm{C}_{\mathrm{T}}$ is discharged to the oscillator valley voltage. As $\mathrm{C}_{\mathrm{T}}$ charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 7 and 15 illustrate the switch output duty cycle versus the compensation voltage.

## Current Sense

The MC34167 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.
The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 6.5 A .

Figure 10 illustrates switch output current limit threshold versus temperature.

## Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB , and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 4). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of $\pm 2.0 \%$ at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a $1.0 \%$ voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V , resistor $\mathrm{R}_{1}$ must be added to form a divider network at the feedback input as shown in Figures 14 and 19. The equation for determining the output voltage with the divider network is:

$$
\mathrm{V}_{\text {out }}=5.05\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)
$$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor $\left(\mathrm{R}_{2}\right)$ from the regulated output to the inverting input, and a series resistor-capacitor $\left(\mathrm{R}_{\mathrm{F}}, \mathrm{C}_{\mathrm{F}}\right)$ between Pins 1 and 5 . The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 19) is the easiest to compensate for stability. The step-up (Figure 21) and voltage-inverting (Figure 23) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting $R_{F}$ and $\mathrm{C}_{\mathrm{F}}$ for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV , the internal circuitry will be placed into a low power standby mode, reducing the power supply current to $36 \mu \mathrm{~A}$ with a 12 V supply voltage. Figure 11 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a $100 \mu \mathrm{~A}$ current source pull-up that can be used to implement soft-start. Figure 18 shows the current source charging capacitor $\mathrm{C}_{\text {SS }}$ through a series diode. The diode disconnects $\mathrm{C}_{\mathrm{SS}}$ from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5 .

## MC34167, MC33167

## Switch Output

The output transistor is designed to switch a maximum of 40 V , with a minimum peak collector current of 5.5 A . When configured for step-down or voltage-inverting applications, as in Figures 19 and 23, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 9 shows that by clamping the emitter to 0.5 V , the collector current will be in the range of $100 \mu \mathrm{~A}$ over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

## Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully
functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when $\mathrm{V}_{\mathrm{CC}}$ exceeds 5.9 V . To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

## Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at $170^{\circ} \mathrm{C}$, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking. The MC34167 is contained in a 5-lead TO-220 type package. The tab of the package is common with the center pin ( Pin 3 ) and is normally connected to ground.

## DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire-wrap or plug-in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a
tight component layout is recommended. Capacitors $\mathrm{C}_{\mathrm{in}}$, $\mathrm{C}_{\mathrm{O}}$, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

## MC34167, MC33167



Figure 16. Low Power Standby Circuit


Figure 17. Over Voltage Shutdown Circuit


Figure 18. Soft-Start Circuit


L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step-Down Converter application is shown in Figure 19. The output switch transistor $Q_{1}$ interrupts the input voltage, generating a squarewave at the LCo filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between $V_{\text {in }}$ and $V_{\text {ref }}$ by controlling the percent conduction time of $Q_{1}$ to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V , resistor $\mathrm{R}_{1}$ must be added to form a divider network at the feedback input.

Figure 19. Step-Down Converter


Figure 20. Step-Down Converter Printed Circuit Board and Component Layout


| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=10 \mathrm{~V}$ to $24 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.9 \mathrm{~A}$ | $10 \mathrm{mV}= \pm 0.017 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~A}$ to 0.9 A | $30 \mathrm{mV}= \pm 0.053 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.9 \mathrm{~A}$ | $140 \mathrm{mV}_{\mathrm{pp}}$ |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 6.0 A |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.9 \mathrm{~A}$ | $80.1 \%$ |
|  | $\mathrm{~V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.9 \mathrm{~A}$ | $87.8 \%$ |

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. MC34167: 5903B, or 5930B MTP3055EL: 5925B
Figure 21 shows that the MC34167 can be configured as a step-up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the ON time of transistors $Q_{1}$ and $Q_{2}$. During the OFF time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step-up converter circuit. The first advantage is that output short circuit protection is provided by the MC34167, since $Q_{1}$ is directly in series with $V_{\text {in }}$ and the load. Second, the output voltage can be programmed to be less than $V_{\text {in }}$. Notice that during the OFF time, the inductor forward biases diodes $D_{1}$ and $D_{2}$, transferring its energy with respect to ground rather than with respect to $\mathrm{V}_{\text {in }}$. When operating with $\mathrm{V}_{\text {in }}$ greater than 20 V , a gate protection network is required for the MOSFET. The network consists of components $R_{G}, D_{3}$, and $D_{4}$.

Figure 21. Step-Up/Down Converter


Figure 22. Step-Up/Down Converter Printed Circuit Board and Component Layout

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=10 \mathrm{~V}$ to $24 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.7 \mathrm{~A}$ | $15 \mathrm{mV}= \pm 0.61 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.1 \mathrm{~A}$ to 1.7 A | $4.0 \mathrm{mV}= \pm 0.020 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.7 \mathrm{~A}$ | 78 mV ppp |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 5.7 A |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.7 \mathrm{~A}$ | $79.5 \%$ |
|  | $\mathrm{~V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.7 \mathrm{~A}$ | $86.2 \%$ |

L = Coilcraft M1496-A or General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage-inverting converter with the MC34167. First, the Switch Output emitter is limited to -1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 23. This keeps the emitter of $Q_{1}$ positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across $R_{1}$ is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage-Inverting Converter


Figure 24. Voltage-Inverting Converter Printed Circuit Board and Component Layout


Figure 25. Triple Output Converter

| Tests |  | Conditions | Results |
| :---: | :---: | :---: | :---: |
| Line Regulation | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\mathrm{V}_{\text {in }}=15 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=3.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=250 \mathrm{~mA}, \mathrm{I}_{03}=200 \mathrm{~mA}$ | $\begin{aligned} & 3.0 \mathrm{mV}= \pm 0.029 \% \\ & 572 \mathrm{mV}= \pm 2.4 \% \\ & 711 \mathrm{mV}= \pm 2.9 \% \end{aligned}$ |
| Load Regulation | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\begin{aligned} & \mathrm{V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=30 \mathrm{~mA} \text { to } 3.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=250 \mathrm{~mA}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA} \\ & \mathrm{~V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=3.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=100 \mathrm{~mA} \text { to } 250 \mathrm{~mA}, I_{\mathrm{O} 3}=200 \mathrm{~mA} \\ & \mathrm{~V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=3.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=250 \mathrm{~mA}, I_{\mathrm{O} 3}=75 \mathrm{~mA} \text { to } 200 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} 1.0 \mathrm{mV} & = \pm 0.009 \% \\ 409 \mathrm{mV} & = \pm 1.5 \% \\ 528 \mathrm{mV} & = \pm 2.0 \% \end{aligned}$ |
| Output Ripple | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\mathrm{V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=3.0 \mathrm{~A}, \mathrm{I}_{02}=250 \mathrm{~mA}, \mathrm{l}_{\mathrm{O} 3}=200 \mathrm{~mA}$ | 75 mV pp 20 mV pp 20 mV pp |
| Short Circuit Current | $\begin{array}{r} 5.0 \mathrm{~V} \\ 12 \mathrm{~V} \\ -12 \mathrm{~V} \end{array}$ | $\mathrm{V}_{\text {in }}=24 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | $\begin{aligned} & 6.5 \mathrm{~A} \\ & 2.7 \mathrm{~A} \\ & 2.2 \mathrm{~A} \end{aligned}$ |
| Efficiency | TOTAL | $\mathrm{V}_{\text {in }}=24 \mathrm{~V}, \mathrm{I}_{\mathrm{O} 1}=3.0 \mathrm{~A}, \mathrm{I}_{\mathrm{O} 2}=250 \mathrm{~mA}, \mathrm{I}_{\mathrm{O} 3}=200 \mathrm{~mA}$ | 84.2\% |

$\begin{aligned} \mathrm{T} 1= & \text { Primary: Coilcraft M1496-A or General Magnetics Technology GMT-0223, } 42 \text { turns of \#16 AWG on Magnetics Inc. 58350-A2 core. } \\ & \text { Secondary: } \mathrm{V}_{\mathrm{O} 2}-69 \text { turns of \#26 AWG }\end{aligned}$ $\mathrm{V}_{\mathrm{O} 3}-104$ turns of \#28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.
Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$
\# \operatorname{TURNS}_{(\mathrm{SEC})}=\frac{\mathrm{V}_{\mathrm{O}(\mathrm{SEC})}+\mathrm{V}_{\mathrm{F}(\mathrm{SEC})}}{\left(\frac{\mathrm{V}_{\mathrm{O}(\mathrm{PRI})}+\mathrm{V}_{\mathrm{F}(\mathrm{PRI})}}{\text { \#TURNS(PRI) }}\right)}
$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than $33 \%$ of the total output power.


| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=-10 \mathrm{~V}$ to $-20 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.3 \mathrm{~A}$ | $266 \mathrm{mV}= \pm 0.38 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=-12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.03 \mathrm{~A}$ to 0.3 A | $7.90 \mathrm{mV}= \pm 1.1 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=-12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.3 \mathrm{~A}$ | $100 \mathrm{mV}_{\mathrm{pp}}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=-12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.3 \mathrm{~A}$ | $78.4 \%$ |

$\mathrm{L}=$ General Magnetics Technology GMT-0223, 42 turns of \#16 AWG on Magnetics Inc. 58350-A2 core. Heatsink = AAVID Engineering Inc. 5903B or 5930B

Figure 26. Negative Input/Positive Output Regulator


Figure 27. Variable Motor Speed Control with EMF Feedback Sensing

## MC34167, MC33167



The MC34167 can be used cost effectively in off-line applications even though it is limited to a maximum input voltage of 40 V . Figure 28 shows a simple and efficient method for converting the AC line voltage down to 24 V . This preconverter has a total power rating of 125 W with a conversion efficiency of $90 \%$. Transformer $\mathrm{T}_{1}$ provides output isolation from the AC line and isolation between each of the secondaries. The circuit self-oscillates at 50 kHz and is controlled by the saturation characteristics of $\mathrm{T}_{2}$. Multiple MC34167 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. Off-Line Preconverter


Figure 29. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## MC34167, MC33167

Table 1. Design Equations

| Calculation | Step-Down | Step-Up/Down | Voltage-Inverting |
| :---: | :---: | :---: | :---: |
| $\frac{\frac{t_{0 n}}{t_{\text {off }}}}{(\text { Notes 1, 2) }}$ | $\frac{V_{\text {out }}+V_{F}}{V_{\text {in }}-V_{\text {sat }}-V_{\text {out }}}$ | $\frac{V_{\text {out }}+V_{F 1}+V_{F 2}}{V_{\text {in }}-V_{\text {satQ1 }}-V_{\text {satQ2 }}}$ | $\frac{\mid V_{\text {out }}+V_{F}}{V_{\text {in }}-V_{\text {sat }}}$ |
| $\mathrm{t}_{\text {on }}$ | $\frac{\frac{t_{\text {on }}}{t_{\text {off }}}}{\left.\mathrm{fosc}_{\left(\frac{t_{\mathrm{on}}}{t_{\text {off }}}+1\right)}\right)}$ | $\frac{\frac{\operatorname{ton}}{\text { toff }}}{\mathrm{fosc}^{\left(\frac{\mathrm{ton}}{\mathrm{t}_{\text {toff }}}+1\right)}}$ | $\frac{\frac{t_{0 n}}{t_{\text {off }}}}{\mathrm{fosc}_{\left(\frac{t_{0 n}}{t_{\text {off }}}+1\right)}}$ |
| Duty Cycle (Note 3) | $\mathrm{t}_{\text {on }} \mathrm{f}_{\text {osc }}$ | $\mathrm{t}_{\text {on }} \mathrm{f}_{\text {osc }}$ | $\mathrm{t}_{\text {on }} \mathrm{f}_{\text {osc }}$ |
| L $\mathrm{Lavg}^{\text {a }}$ | Iout | lout ( $\left(\frac{t_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right)$ | lout $\left(\frac{t_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right)$ |
| $\mathrm{I}_{\mathrm{pk} \text { (switch) }}$ | $\mathrm{LLavg}+\frac{\Delta \mathrm{LL}}{2}$ | $\mathrm{LLavg}+\frac{\Delta \mathrm{LL}}{2}$ | $\mathrm{LLavg}+\frac{\Delta \mathrm{LL}}{2}$ |
| L | $\left(\frac{V_{\text {in }}-V_{\text {sat }}-V_{\text {out }}}{\Delta l_{\text {L }}}\right)_{\text {ton }}$ | $\left(\frac{V_{\text {in }}-V_{\text {SatQ1 }}-V_{\text {satQ2 }}}{\Delta l_{\text {L }}}\right)_{\text {on }}$ | $\left(\frac{V_{\text {in }}-V_{\text {sat }}}{\Delta I_{\mathrm{L}}}\right)_{\text {ton }}$ |
| $\mathrm{V}_{\text {ripple(pp) }}$ | $\Delta \mathrm{I} \mathrm{~L} \sqrt{\left(\frac{1}{8 \mathrm{f}_{\mathrm{osc}} \mathrm{C}_{0}}\right)^{2}+(\mathrm{ESR})^{2}}$ | $\left(\frac{t_{\text {on }}}{t_{\text {off }}}+1\right) \sqrt{\left(\frac{1}{f_{\text {osc }} \mathrm{C}_{0}}\right)^{2}+(\mathrm{ESR})^{2}}$ | $\left(\frac{t_{\text {on }}}{\mathrm{t}_{\text {off }}}+1\right) \sqrt{\left(\frac{1}{\mathrm{fosc}^{\text {a }}}\right)^{2}+(\mathrm{ESR})^{2}}$ |
| $V_{\text {out }}$ | $\mathrm{V}_{\text {ref }}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)$ | $V_{\text {ref }}\left(\frac{R_{2}}{R_{1}}+1\right)$ | $V_{\text {ref }}\left(\frac{R_{2}}{R_{1}}+1\right)$ |

1. $\mathrm{V}_{\text {sat }}-$ Switch Output source saturation voltage, refer to Figure 8.
2. $\mathrm{V}_{\mathrm{F}}$ - Output rectifier forward voltage drop. Typical value for 1 N 5822 Schottky barrier rectifier is 0.35 V .
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $\mathrm{DC}_{(\max )}$ specification of 0.92 .

The following converter characteristics must be chosen:
$V_{\text {out }}$ - Desired output voltage.
$\mathrm{I}_{\text {out }}$ - Desired output current.
$\Delta L_{\mathrm{L}}$ - Desired peak-to-peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5 , it is suggested that $\Delta L_{\mathrm{L}}$ be chosen minimum current limit threshold of 5.5 A. If the design goal is to use a minimum inductance value, let $\Delta I_{\mathrm{L}}=2\left(\mathrm{l}_{\mathrm{L}}\right.$ avg $)$. This will proportionally reduce the converter's output current capability.
$\mathrm{V}_{\text {ripple(pp) }}$ - Desired peak-to-peak output ripple voltage. For best performance, the ripple voltage should be kept to less than $2 \%$ of $\mathrm{V}_{\text {out }}$. Capacitor $\mathrm{C}_{0}$ should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

## MC34167, MC33167

ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: |
| MC33167D2T | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | D²PAK (Surface Mount) | 50 Units/Rail |
| MC33167T |  | TO-220 (Straight Lead) |  |
| MC33167TH |  | TO-220 (Horizontal Mount) |  |
| MC33167TV |  | TO-220 (Vertical Mount) |  |
| MC34167D2T | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | $\mathrm{D}^{2}$ PAK (Surface Mount) |  |
| MC34167T |  | TO-220 (Straight Lead) |  |
| MC34167TH |  | TO-220 (Horizontal Mount) |  |
| MC34167TV |  | TO-220 (Vertical Mount) |  |

## CS51031

## Fast PFET Buck Controller

The CS51031 is a switching controller for use in DC-DC converters. It can be used in the buck topology with a minimum number of external components. The CS51031 consists of a $\mathrm{V}_{\mathrm{CC}}$ monitor for controlling the state of the device, 1.0 A power driver for controlling the gate of a discrete P -channel transistor, fixed frequency oscillator, short circuit protection timer, programmable soft start, precision reference, fast output voltage monitoring comparator, and output stage driver logic with latch.

The high frequency oscillator allows the use of small inductors and output capacitors, minimizing PC board area and systems cost. The programmable soft start reduces current surges at start up. The short circuit protection timer significantly reduces the duty cycle to approximately $1 / 30$ of its cycle during short circuit conditions.

The CS51031 is available in 8 Lead SO and 8 Lead PDIP plastic packages.

## Features

- 1.0 A Totem Pole Output Driver
- High Speed Oscillator (700 kHz max)
- No Stability Compensation Required
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- $2.0 \%$ Precision Reference
- Programmable Soft Start
- Wide Ambient Temperature Range:
- Industrial Grade: $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$
- Commercial Grade: $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$


Figure 1. Typical Application Diagram


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com

ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51031YD8 | SO-8 | 95 Units/Rail |
| CS51031YDR8 | SO-8 | 2500 Tape \& Reel |
| CS51031YN8 | DIP-8 | 50 Units/Rail |
| CS51031GD8 | SO-8 | 95 Units/Rail |
| CS51031GDR8 | SO-8 | 2500 Tape \& Reel |

*Additional ordering information can be found on page 1571 of this data sheet.

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage, $\mathrm{V}_{\text {CC }}$ |  | 20 | V |
| Driver Supply Voltage, $\mathrm{V}_{\mathrm{C}}$ |  | 20 | V |
| Driver Output Voltage, $\mathrm{V}_{\text {GATE }}$ |  | 20 | V |
| Cosc, CS, V $\mathrm{FBB}^{\text {(Logic Pins) }}$ |  | 6.0 | V |
| Peak Output Current |  | 1.0 | A |
| Steady State Output Current |  | 200 | mA |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Temperature Range, $\mathrm{T}_{\mathrm{A}}$ |  | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering: | Wave Solder: (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2) | 260 peak <br> 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |

1. 10 sec . maximum.
2. 60 sec. max above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (Specifications apply for $4.5 \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}, 3.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{C}} \leq 16 \mathrm{~V}$; Industrial Grade: $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$; $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$ : Commercial Grade: $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillator | $\mathrm{V}_{\mathrm{FB}}=1.2 \mathrm{~V}$ |  |  |  |  |
| Frequency | $\mathrm{C}_{\text {OSC }}=470 \mathrm{pF}$ | 160 | 200 | 240 | kHz |
| Charge Current | $1.4 \mathrm{~V}<\mathrm{V}_{\text {cosc }}<2.0 \mathrm{~V}$ | - | 110 | - | $\mu \mathrm{A}$ |
| Discharge Current | $2.7 \mathrm{~V}>\mathrm{V}_{\text {cosc }}>2.0 \mathrm{~V}$ | - | 660 | - | $\mu \mathrm{A}$ |
| Maximum Duty Cycle | 1-(toff/ton) | 80.0 | 83.3 | - | \% |

## Short Circuit Timer $\quad \mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V} ; \mathrm{CS}=\mathbf{0 . 1} \mu \mathrm{F} ; \mathrm{V}_{\text {COSC }}=2.0 \mathrm{~V}$

| Charge Current | $1.0 \mathrm{~V}<\mathrm{V}_{\text {CS }}<2.0 \mathrm{~V}$ | 175 | 264 | 325 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fast Discharge Current | $2.55 \mathrm{~V}>\mathrm{V}_{\text {CS }}>2.4 \mathrm{~V}$ | 40 | 66 | 80 | $\mu \mathrm{A}$ |
| Slow Discharge Current | $2.4 \mathrm{~V}>\mathrm{V}_{\text {CS }}>1.5 \mathrm{~V}$ | 4.0 | 6.0 | 10 | $\mu \mathrm{A}$ |
| Start Fault Inhibit Time | $0 \mathrm{~V}<\mathrm{V}_{\mathrm{CS}}<2.5 \mathrm{~V}$ | 0.70 | 0.85 | 1.40 | ms |
| Valid Fault Time | $2.6 \mathrm{~V}>\mathrm{V}_{\text {CS }}>2.4 \mathrm{~V}$ | 0.2 | 0.3 | 0.45 | ms |
| GATE Inhibit Time | $2.4 \mathrm{~V}>\mathrm{V}_{\text {CS }}>1.5 \mathrm{~V}$ | 9.0 | 15 | 23 | ms |
| Fault Duty Cycle | - | 2.5 | 3.1 | 4.6 | \% |

CS Comparator

| Fault Enable CS Voltage | - | - | 2.5 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Max. CS Voltage | $\mathrm{V}_{\mathrm{FB}}=1.5 \mathrm{~V}$ | - | 2.6 | - | V |
| Fault Detect Voltage | $\mathrm{V}_{\mathrm{CS}}$ when GATE goes high | - | 2.4 | - | V |
| Fault Inhibit Voltage | Minimum $\mathrm{V}_{\mathrm{CS}}$ | - | 1.5 | - | V |
| Hold Off Release Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 0.4 | 0.7 | 1.0 | V |
| Regulator Threshold Voltage Clamp | $\mathrm{V}_{\mathrm{CS}}=1.5 \mathrm{~V}$ | 0.725 | 0.866 | 1.035 | V |

ELECTRICAL CHARACTERISTICS (continued) (Specifications apply for $4.5 \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}, 3.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{C}} \leq 16 \mathrm{~V}$;
Industrial Grade: $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$; $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$ : Commercial Grade: $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {FB }}$ Comparators | $\mathrm{V}_{\text {cosc }}=\mathrm{V}_{\text {cs }}=2.0 \mathrm{~V}$ |  |  |  |  |
| Regulator Threshold Voltage | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C}(\text { Note } 3) \\ & \mathrm{T}_{J}=-40 \text { to } 125^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & 1.225 \\ & 1.210 \end{aligned}$ | $\begin{aligned} & 1.250 \\ & 1.250 \end{aligned}$ | $\begin{aligned} & 1.275 \\ & 1.290 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Fault Threshold Voltage | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C}(\text { Note } 3) \\ & \mathrm{T}_{J}=-40 \text { to } 125^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & 1.12 \\ & 1.10 \end{aligned}$ | $\begin{aligned} & 1.15 \\ & 1.15 \end{aligned}$ | $\begin{aligned} & 1.17 \\ & 1.19 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Threshold Line Regulation | $4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | - | 6.0 | 15 | mV |
| Input Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 1.0 | 4.0 | $\mu \mathrm{A}$ |
| Voltage Tracking | (Regulator Threshold - Fault Threshold Voltage) | 70 | 100 | 120 | mV |
| Input Hysteresis Voltage | - | - | 4.0 | 20 | mV |

Power Stage

| $l \mid$ |  |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| GATE DC Low Saturation Voltage | $\mathrm{V}_{\mathrm{COSC}}=1.0 \mathrm{~V} ; 200 \mathrm{~mA}$ Sink | - | 1.2 | 1.5 | V |
| GATE DC High Saturation Voltage | $\mathrm{V}_{\mathrm{COSC}}=2.7 \mathrm{~V} ; 200 \mathrm{~mA}$ Source; $\mathrm{V}_{\mathrm{C}}=\mathrm{V}_{\mathrm{GATE}}$ | - | 1.5 | 2.1 | V |
| Rise Time | $\mathrm{C}_{\mathrm{GATE}}=1.0 \mathrm{nF} ; 1.5 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}}<9.0 \mathrm{~V}$ | - | 25 | 60 | ns |
| Fall Time | $\mathrm{C}_{\mathrm{GATE}}=1.0 \mathrm{nF} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}}>1.5 \mathrm{~V}$ | - | 25 | 60 | ns |

$\mathrm{V}_{\mathrm{CC}}$ Monitor

| Turn On Threshold | - | 4.200 | 4.400 | 4.600 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Turn Off Threshold | - | 4.085 | 4.300 | 4.515 | V |
| Hysteresis | - | 65 | 130 | 200 | mV |

Current Drain

| $\mathrm{I}_{\mathrm{CC}}$ | $4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<16 \mathrm{~V}$, Gate switching | - | 4.5 | 6.0 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{C}}$ | $3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<16 \mathrm{~V}$, Gate non-switching | - | 2.7 | 4.0 | mA |
| Shutdown $\mathrm{I}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}=4.0$ | - | 500 | 900 | $\mu \mathrm{~A}$ |

3. Guaranteed by design, not $100 \%$ tested in production.

## PACKAGE LEAD DESCRIPTION

| PACKAGE PIN NUMBER |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| SO-8 | DIP-8 |  |  |
| 1 | 1 | $V_{\text {GATE }}$ | Driver pin to gate of external PFET. |
| 2 | 2 | PGND | Output power stage ground connection. |
| 3 | 3 | Cosc | Oscillator frequency programming capacitor. |
| 4 | 4 | GND | Logic ground. |
| 5 | 5 | $V_{\text {FB }}$ | Feedback voltage input. |
| 6 | 6 | $\mathrm{V}_{\mathrm{CC}}$ | Logic supply voltage. |
| 7 | 7 | CS | Soft start and fault timing capacitor. |
| 8 | 8 | $\mathrm{V}_{\mathrm{C}}$ | Driver supply voltage. |



Figure 2. Block Diagram

## CIRCUIT DESCRIPTION

## THEORY OF OPERATION

## Control Scheme

The CS51031 monitors and the output voltage to determine when to turn on the PFET. If $\mathrm{V}_{\mathrm{FB}}$ falls below the internal reference voltage of 1.25 V during the oscillator's charge cycle, the PFET is turned on and remains on for the
duration of the charge time. The PFET gets turned off and remains off during the oscillator's discharge time with the maximum duty cycle to $80 \%$. It requires 7.0 mV typical, and 20 mV maximum ripple on the $\mathrm{V}_{\mathrm{FB}}$ pin is required to operate. This method of control does not require any loop stability compensation.

## Startup

The CS51031 has an externally programmable soft start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As $\mathrm{V}_{\mathrm{CC}}$ rises, the $\mathrm{V}_{\mathrm{C}}$ voltage along with the internal resistor $\mathrm{R}_{\mathrm{G}}$ keeps the PFET off. As $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}$ continue to rise, the oscillator capacitor (COSC ) and the Soft Start/Fault Timing capacitor (CS) charges via internal current sources. COSC gets charged by the current source IC and CS gets charged by the $\mathrm{I}_{\mathrm{T}}$ source combination described by:

$$
I_{C S}=I_{T}-\left(\frac{I T}{55}+\frac{I T}{5}\right)
$$

The internal Holdoff Comparator ensures that the external PFET is off until $\mathrm{V}_{\mathrm{CS}}>0.7 \mathrm{~V}$, preventing the GATE flip-flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft start is obtained by clamping the $\mathrm{V}_{\mathrm{FB}}$ comparator's (A6) reference input to approximately $1 / 2$ of the voltage at the CS pin during startup, permitting the control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7 V , the low feedback to the $\mathrm{V}_{\mathrm{FB}}$ Comparator sets the GATE flip-flop during CoSC 's charge cycle. Once the GATE flip-flop is set, $\mathrm{V}_{\text {GATE }}$ goes low and turns on the PFET. When $\mathrm{V}_{\mathrm{CS}}$ exceeds 2.4 V , the CS charge sense comparator ( A 4 ) sets the $\mathrm{V}_{\mathrm{FB}}$ comparator reference to 1.25 V completing the startup cycle.

## Lossless Short Circuit Protection

The CS51031 has "lossless" short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage ) reaches 2.5 V during startup, the fault timing circuitry is enabled. During normal operation the CS voltage is 2.6 V . During a short circuit or a transient condition, the output voltage moves lower and the voltage at $\mathrm{V}_{\mathrm{FB}}$ drops. If $\mathrm{V}_{\mathrm{FB}}$ drops below 1.15 V , the output of the fault comparator goes high and the CS51031 goes into a fast discharge mode. The fault timing capacitor, CS , discharges to 2.4 V . If the $\mathrm{V}_{\mathrm{FB}}$ voltage is still below 1.15 V when the CS pin reaches 2.4 V , a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip flop. The $\mathrm{V}_{\text {GATE }}$ flip flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5 V . The CS51031 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5 V , the fast and slow discharge cycles repeat as shown in figure 3.
If the $\mathrm{V}_{\mathrm{FB}}$ voltage is above 1.15 V when CS reaches 2.4 V a fault condition is not detected, normal operation resumes and CS charges back to 2.6 V . This reduces the chance of erroneously detecting a load transient as a fault condition.


Figure 3. Voltage on Start Capacitor ( $\mathrm{V}_{\mathrm{GS}}$ ), the Gate ( $\mathrm{V}_{\mathrm{GATE}}$ ), and in the Feedback Loop ( $\mathrm{V}_{\mathrm{FB}}$ ), During Startup, Normal and Fault Conditions.

## Buck Regulator Operation

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current $\mathrm{I}_{\mathrm{L}}$ is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor $\mathrm{C}_{\mathrm{O}}$. When the voltage across $\mathrm{C}_{\mathrm{O}}$ drops below the threshold established by the feedback resistors R1
and R2 and the reference voltage $\mathrm{V}_{\text {REF }}$, the power transistor Q1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by $\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) / \mathrm{L}$. The duty cycle (or "on" time) for the CS51031 is limited to $80 \%$. If output voltage remains higher than nominal during the entire $\mathrm{C}_{\mathrm{OSC}}$ change time, the Q1 does not turn on, skipping the pulse.


Figure 4. Buck Regulator Block Diagram.

## APPLICATIONS INFORMATION

## CS51031 DESIGN EXAMPLE

## Specifications 12 V to 5.0 V, 3.0 A Buck Controller

- $\mathrm{V}_{\mathrm{IN}}=12 \mathrm{~V} \pm 20 \%$ (i.e. 14.4 V max., 12 V nom., 9.6 V min.)
- $\mathrm{V}_{\text {OUT }}=5.0 \mathrm{~V} \pm 2 \%$
- $\mathrm{I}_{\text {OUT }}=0.3 \mathrm{~A}$ to 3.0 A
- Output ripple voltage $<50 \mathrm{mV}$ max.
- Efficiency > 80\%
- $\mathrm{f}_{\mathrm{SW}}=200 \mathrm{kHz}$


## 1) Duty Cycle Estimates

Since the maximum duty cycle D, of the CS51031 is limited to $80 \% \mathrm{~min}$., it is necessary to estimate the duty cycle for the various input conditions over the complete operating range.

The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}}{\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{SAT}}}
$$

where:
$\mathrm{V}_{\mathrm{SAT}}=\mathrm{R}_{\mathrm{ds}(\text { on })} \times \mathrm{I}_{\text {OUT }}$ max. and $\mathrm{R}_{\mathrm{ds}(\text { on })}$ is the value at $\mathrm{T}_{\mathrm{J}}$ $100^{\circ} \mathrm{C}$.

If $\mathrm{V}_{\mathrm{F}}=0.60 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{SAT}}=0.60 \mathrm{~V}$ then the above equation becomes:

$$
\begin{aligned}
& D_{M A X}=\frac{5.6}{9.0}=0.62 \\
& D_{M I N}=\frac{5.6}{13.8}=0.40
\end{aligned}
$$

## 2) Switching Frequency and On and Off Time Calculations

Given that $\mathrm{f}_{\mathrm{SW}}=200 \mathrm{kHz}$ and $\mathrm{D}_{\mathrm{MAX}}=0.80$

$$
\begin{gathered}
\mathrm{T}=\frac{1.0}{\mathrm{fSW}}=5.0 \mu \mathrm{~s} \\
\mathrm{TON}(\max )=\mathrm{T} \times \mathrm{DMAX}_{\mathrm{M}}=5.0 \mu \mathrm{~s} \times 0.62 \cong 3.0 \mu \mathrm{~s} \\
\mathrm{TON}(\min )=\mathrm{T} \times \mathrm{DMIN}=5.0 \mu \mathrm{~s} \times 0.40 \cong 2.0 \mu \mathrm{~s} \\
\mathrm{TOFF}(\max )=\mathrm{TON}(\min )=5.0 \mu \mathrm{~s}-2.0 \mu \mathrm{~s}=3.0 \mu \mathrm{~s}
\end{gathered}
$$

## 3) Oscillator Capacitor Selection

The switching frequency is set by COSC, whose value is given by:

$$
\operatorname{COSC} \text { in } \mathrm{pF}=\frac{95 \times 10-6}{\operatorname{FSW}\left(1+\frac{\mathrm{FSW}}{3 \times 10^{6}}-\left(\frac{30 \times 10^{3}}{\mathrm{FSW}}\right)^{2}\right)}
$$

## 4) Inductor Selection

The inductor value is chosen for continuous mode operation down to 0.3 Amps .

The ripple current $\Delta \mathrm{I}=2 \times \mathrm{I}_{\text {OUT }} \mathrm{min}=2 \times 0.3 \mathrm{~A}=0.6 \mathrm{~A}$.
$\mathrm{L}_{\text {min }}=\frac{\left(\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{D}}\right) \times \operatorname{TOFF}(\max )}{\Delta \mathrm{I}}=\frac{5.6 \mathrm{~V} \times 3.0 \mu \mathrm{~s}}{0.6 \mathrm{~A}}=28 \mu \mathrm{H}$
This is the minimum value of inductor to keep the ripple current < 0.6 A during normal operation.

A smaller inductor will result in larger ripple current. Ripple current at a minimum off time is

$$
\Delta \mathrm{l}=\frac{\left(\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{F}}\right) \times \mathrm{TOFF}(\mathrm{~min})}{\mathrm{L}_{\mathrm{MIN}}}=\frac{5.6 \mathrm{~V} \times 2.0 \mu \mathrm{~s}}{28 \mu \mathrm{H}}=0.4 \mathrm{~A}
$$

The core must not saturate with the maximum expected current, here given by:

$$
\mathrm{ImAX}=\mathrm{IOUT}+\Delta \mathrm{I} / 2=3.0 \mathrm{~A}+0.4 \mathrm{~A} / 2=3.2 \mathrm{~A}
$$

## 5) Output Capacitor

The output capacitor and the inductor form a low pass filter. The output capacitor should have a low ESL and ESR. Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are less expensive. Solid tantalum chip capacitors are available from a number of suppliers and are the best choice for surface mount applications.

The output capacitor limits the output ripple voltage. The CS51031 needs a maximum of 20 mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50 mV peak to peak is given by:

$$
\mathrm{C}=\frac{\Delta \mathrm{I}}{8.0 \times \mathrm{fSW} \times \Delta \mathrm{V}}=\frac{0.6 \mathrm{~A}}{8.0 \times\left(200 \times 10^{3} \mathrm{~Hz}\right) \times\left(50 \times 10^{-3} \mathrm{~V}\right)}=7.5 \mu \mathrm{~F}
$$

The minimum ESR needed to limit the output voltage ripple to 50 mV peak to peak is:

$$
\mathrm{ESR}=\frac{\Delta \mathrm{V}}{\Delta \mathrm{l}}=\frac{50 \times 10-3}{0.6 \mathrm{~A}}=83 \mathrm{~m} \Omega
$$

The output capacitor should be chosen so that its ESR is less than $83 \mathrm{~m} \Omega$.

During the minimum off time, the ripple current is 0.4 A and the output voltage ripple will be:

$$
\Delta \mathrm{V}=\mathrm{ESR} \times \Delta \mathrm{I}=83 \mathrm{~m} \Omega \times 0.4=33 \mathrm{mV}
$$

## 6) $V_{F B}$ Divider

$$
\mathrm{V}_{\text {OUT }}=1.25 \mathrm{~V}\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 2}\right)=1.25 \mathrm{~V}\left(\frac{\mathrm{R} 1}{\mathrm{R} 2}+1.0\right)
$$

The input bias current to the comparator is $4.0 \mu \mathrm{~A}$. The resistor divider current should be considerably higher than this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this permits a divider current of 1 mA and simplifies the calculations.

$$
\frac{5.0 \mathrm{~V}}{1.0 \mathrm{~mA}}=\mathrm{R} 1+\mathrm{R} 2=5.0 \mathrm{~K} \Omega
$$

Let R2 $=1.0 \mathrm{~K}$
Rearranging the divider equation gives:
$R 1=\operatorname{R2}\left(\frac{\mathrm{V}_{\text {OUT }}}{1.25}-1.0\right)=1.0 \mathrm{k} \Omega\left(\frac{5.0 \mathrm{~V}}{1.25}-1.0\right)=3.0 \mathrm{k} \Omega$

## 7) Divider Bypass Capacitor $\mathrm{C}_{\mathrm{RR}}$

Since the feedback resistors divide the output voltage by a factor of 4.0 , i.e. $5.0 \mathrm{~V} / 1.25 \mathrm{~V}=4.0$, it follows that the output ripple is also divided by four. This would require that the output ripple be at least $60 \mathrm{mV}(4.0 \times 15 \mathrm{mV})$ to trip the feedback comparator. We use a capacitor $C_{R R}$ to act as an AC short.
The ripple voltage frequency is equal to the switching frequency so we choose $\mathrm{C}_{\mathrm{RR}}=1.0 \mathrm{nF}$.

## 8) Soft Start and Fault Timing Capacitor CS

CS performs several important functions. First it provides a delay time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides soft start by clamping the reference voltage during startup, allowing it to rise slowly, and, finally it controls the hiccup short circuit protection circuitry. This reduces the duty cycle to approximately 0.035 during short circuit conditions.

An important consideration in calculating CS is that it's voltage does not reach 2.5 V (the voltage at which the fault detect circuitry is enabled) before $\mathrm{V}_{\mathrm{FB}}$ reaches 1.15 V otherwise the power supply will never start.

If the $\mathrm{V}_{\mathrm{FB}}$ pin reaches 1.15 V , the fault timing comparator will discharge CS and the supply will not start. For the $\mathrm{V}_{\mathrm{FB}}$ voltage to reach 1.15 V the output voltage must be at least $4 \times 1.15=4.6 \mathrm{~V}$.

If we choose an arbitrary startup time of $900 \mu \mathrm{~s}$, the value of CS is:

$$
\begin{gathered}
\text { tstartup }_{=\frac{\mathrm{CS} \times 2.5 \mathrm{~V}}{\text { ICharge }}}^{\mathrm{CS}_{\min }=\frac{900 \mu \mathrm{~s} \times 264 \mu \mathrm{~A}}{2.5 \mathrm{~V}}=950 \mathrm{nF} \cong 0.1 \mu \mathrm{~F}}
\end{gathered}
$$

The fault time is the sum of the slow discharge time the fast discharge time and the recharge time. It is dominated by the slow discharge time.

The first parameter is the slow discharge time, it is the time for the CS capacitor to discharge from 2.4 V to 1.5 V and is given by:

$$
\text { tSlowDischarge }(\mathrm{t})=\frac{\mathrm{CS} \times(2.4 \mathrm{~V}-1.5 \mathrm{~V})}{\text { IDischarge }}
$$

where $\mathrm{I}_{\text {Discharge }}$ is $6.0 \mu \mathrm{~A}$ typical.

$$
\text { tSlowDischarge }(\mathrm{t})=\mathrm{CS} \times 1.5 \times 10^{5}
$$

The fast discharge time occurs when a fault is first detected. The CS capacitor is discharged from 2.5 V to 2.4 V .

$$
\text { tFastDischarge }(\mathrm{t})=\frac{\mathrm{CS} \times(2.5 \mathrm{~V}-2.4 \mathrm{~V})}{\mathrm{I} \text { FastDischarge }}
$$

where $\mathrm{I}_{\text {FastDischarge }}$ is $66 \mu \mathrm{~A}$ typical.

$$
\mathrm{t} \text { FastDischarge }(\mathrm{t})=\mathrm{CS} \times 1515
$$

The recharge time is the time for CS to charge from 1.5 V to 2.5 V .

$$
\text { tCharge }(\mathrm{t})=\frac{\mathrm{CS} \times(2.5 \mathrm{~V}-1.5 \mathrm{~V})}{\mathrm{I}^{\text {Charge }}}
$$

where $I_{\text {Charge }}$ is $264 \mu \mathrm{~A}$ typical.

$$
\text { tCharge }(\mathrm{t})=\mathrm{CS} \times 3787
$$

The fault time is given by:

$$
\begin{gathered}
\text { tFault }=\mathrm{CS} \times\left(3787+1515+1.5 \times 10^{5}\right) \\
\mathrm{t} \text { Fault }=\mathrm{CS} \times\left(1.55 \times 10^{5}\right)
\end{gathered}
$$

For this circuit

$$
\text { tFault }=0.1 \times 10^{-6} \times 1.55 \times 10^{5}=15.5 \mu \mathrm{~s}
$$

A larger value of CS will increase the fault time out time but will also increase the soft start time.

## 9) Input Capacitor

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on
the $V_{C C}$ and $V_{C}$ pins. This capacitor must also ensure that the $\mathrm{V}_{\mathrm{CC}}$ remains above the UVLO voltage in the event of an output short circuit. A low ESR capacitor of at least $100 \mu \mathrm{~F}$ is good. A ceramic surface mount capacitor should also be connected between $\mathrm{V}_{\mathrm{CC}}$ and ground to filter high frequency noise.

## 10) MOSFET Selection

The CS51031 drives a P-channel MOSFET. The $\mathrm{V}_{\text {GATE }}$ pin swings from GND to $\mathrm{V}_{\mathrm{C}}$. The type of PFET used depends on the operating conditions but for input voltages below 7.0 V a logic level FET should be used.

A PFET with a continuous drain current $\left(\mathrm{I}_{\mathrm{D}}\right)$ rating greater than the maximum output current is required.
The Gate-to-Source voltage $\mathrm{V}_{\mathrm{GS}}$ and the Drain-to Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$
P_{D}=I_{O U T}{ }^{2} \times R_{D S}(O N) \times D
$$

where

$$
\operatorname{RDS}(O N) \text { is the value at } T J=100^{\circ} \mathrm{C}
$$

The power dissipation of the PFET due to the switching losses is given by:

$$
\mathrm{PD}=0.5 \times \mathrm{V}_{\mathrm{IN}} \times \mathrm{IOUT} \times\left(\mathrm{t}_{\mathrm{r}}\right) \times \mathrm{fSW}
$$

where $t_{r}=$ Rise Time.

## 11) Diode Selection

The flyback or catch diode should be a Schottky diode because of it's fast switching ability and low forward voltage drop. The current rating must be at least equal to the maximum output current. The breakdown voltage should be at least 20 V for this 12 V application.

The diode power dissipation is given by:

$$
P_{D}=I_{O U T} \times V_{D} \times\left(1.0-D_{\text {min }}\right)
$$

## CS51031

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package | Shipping |
| :--- | :---: | :---: | :---: |
| CS51031YD8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51031YDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51031YN8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | DIP-8 | 50 Units/Rail |
| CS51031GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51031GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | DIP-8 | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 45 | 52 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 165 | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS51033

## Fast PFET Buck Controller

The CS51033 is a switching controller for use in DC-DC converters. It can be used in the buck topology with a minimum number of external components. The CS51033 consists of a 1.0 A power driver for controlling the gate of a discrete P -channel transistor, fixed frequency oscillator, short circuit protection timer, programmable Soft Start, precision reference, fast output voltage monitoring comparator, and output stage driver logic with latch.

The high frequency oscillator allows the use of small inductors and output capacitors, minimizing PC board area and systems cost. The programmable Soft Start reduces current surges at start up. The short circuit protection timer significantly reduces the PFET duty cycle to approximately $1 / 30$ of its normal cycle during short circuit conditions.

The CS51033 is available in 8 Lead SO and 8 Lead PDIP plastic packages.

## Features

- 1.0 A Totem Pole Output Driver
- High Speed Oscillator (700 kHz max)
- No Stability Compensation Required
- Lossless Short Circuit Protection
- $2.0 \%$ Precision Reference
- Programmable Soft Start
- Wide Ambient Temperature Range:
- Industrial Grade: $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$
- Commercial Grade: $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51033ED8 | SO-8 | 95 Units/Rail |
| CS51033EDR8 | SO-8 | 2500 Tape \& Reel |
| CS51033EN8 | DIP-8 | 50 Units/Rail |
| CS51033GD8 | SO-8 | 95 Units/Rail |
| CS51033GDR8 | SO-8 | 2500 Tape \& Reel |
| CS51033GN8 | DIP-8 | 50 Units/Rail |

*Additional ordering information can be found on page 1580 of this data sheet.


Figure 1. Typical Application Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ |  | 5.0 | V |
| Driver Supply Voltage, $\mathrm{V}_{\mathrm{C}}$ |  | 20 | V |
| Driver Output Voltage, $\mathrm{V}_{\text {GATE }}$ |  | 20 | V |
| Cosc, CS, $\mathrm{V}_{\text {FB }}$ (Logic Pins) |  | 5.0 | V |
| Peak Output Current |  | 1.0 | A |
| Steady State Output Current |  | 200 | mA |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering: | Wave Solder: (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2) | 260 peak <br> 230 peak | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |

1. 10 sec . maximum.
2. 60 sec . max above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (Specifications apply for $3.135 \leq \mathrm{V}_{\mathrm{CC}} \leq 3.465,3.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{C}} \leq 16 \mathrm{~V}$; Industrial Grade: $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$; $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$ : Commercial Grade: $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillator | $\mathrm{V}_{\mathrm{FB}}=1.2 \mathrm{~V}$ |  |  |  |  |
| Frequency | Cosc $=470 \mathrm{pF}$ | 160 | 200 | 240 | kHz |
| Charge Current | $1.4 \mathrm{~V}<\mathrm{V}_{\operatorname{cosc}}<2.0 \mathrm{~V}$ | - | 110 | - | $\mu \mathrm{A}$ |
| Discharge Current | $2.7 \mathrm{~V}>\mathrm{V}_{\text {cosc }}>2.0 \mathrm{~V}$ | - | 660 | - | $\mu \mathrm{A}$ |
| Maximum Duty Cycle | 1 - (toff/ton) | 80.0 | 83.3 | - | \% |

Short Circuit Timer
$\mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V} ; \mathrm{CS}=0.1 \mu \mathrm{~F} ; \mathrm{V}_{\mathrm{COSC}}=2.0 \mathrm{~V}$

| Charge Current | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CS}}<2.0 \mathrm{~V}$ | 175 | 264 | 325 | $\mu \mathrm{~A}$ |  |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Fast Discharge Current | $2.55 \mathrm{~V}>\mathrm{V}_{\mathrm{CS}}>2.4 \mathrm{~V}$ | 40 | 66 | 80 | $\mu \mathrm{~A}$ |  |  |  |  |  |
| Slow Discharge Current | $2.4 \mathrm{~V}>\mathrm{V}_{\mathrm{CS}}>1.5 \mathrm{~V}$ | 4.0 | 6.0 | 10 | $\mu \mathrm{~A}$ |  |  |  |  |  |
| Start Fault Inhibit Time | - |  |  |  |  |  | 0.70 | 0.85 | 1.40 | ms |
| Valid Fault Time | $2.6 \mathrm{~V}>\mathrm{V}_{\mathrm{CS}}>2.4 \mathrm{~V}$ | 0.2 | 0.3 | 0.45 | ms |  |  |  |  |  |
| GATE Inhibit Time | $2.4 \mathrm{~V}>\mathrm{V}_{\mathrm{CS}}>1.5 \mathrm{~V}$ | 9.0 | 15 | 23 | ms |  |  |  |  |  |
| Duty Cycle | - | 2.5 | 3.1 | 4.6 | $\%$ |  |  |  |  |  |

## CS Comparator

$\mathrm{V}_{\mathrm{FB}}=1.0 \mathrm{~V}$

| Fault Enable CS Voltage | - | - | 2.5 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Max. CS Voltage | $\mathrm{V}_{\mathrm{FB}}=1.5 \mathrm{~V}$ | - | 2.6 | - | V |
| Fault Detect Voltage | $\mathrm{V}_{\mathrm{CS}}$ when GATE goes high | - | 2.4 | - | V |
| Fault Inhibit Voltage | Minimum $\mathrm{V}_{\mathrm{CS}}$ | - | 1.5 | - | V |
| Hold Off Release Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 0.4 | 0.7 | 1.0 | V |
| Regulator Threshold Voltage Clamp | $\mathrm{V}_{\mathrm{CS}}=1.5 \mathrm{~V}$ | 0.725 | 0.866 | 1.035 | V |

$\mathrm{V}_{\mathrm{FB}}$ Comparators $\quad \mathrm{V}_{\mathrm{COSC}}=\mathrm{V}_{\mathrm{CS}}=2.0 \mathrm{~V}$

| Regulator Threshold Voltage | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}($ Note 3) | 1.225 | 1.250 | 1.275 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | $\mathrm{~T}_{J}=-40$ to $125^{\circ} \mathrm{C}$ | 1.210 | 1.250 | 1.290 | V |
| Fault Threshold Voltage | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}($ Note 3) | 1.12 | 1.15 | 1.17 | V |
|  | $\mathrm{~T}_{\mathrm{J}}=-40$ to $125^{\circ} \mathrm{C}$ | 1.10 | 1.15 | 1.19 | V |
| Threshold Line Regulation | $3.135 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 3.465$ | - | 6.0 | 15 | mV |
| Input Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 1.0 | 4.0 | $\mu \mathrm{~A}$ |
| Voltage Tracking | (Regulator Threshold - Fault Threshold Voltage) | 70 | 100 | 120 | mV |
| Input Hysteresis Voltage | - | - | 4.0 | 20 | mV |

Power Stage $\quad \mathrm{V}_{\mathrm{C}}=10 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=1.2 \mathrm{~V}$

| GATE DC Low Saturation Voltage | $\mathrm{V}_{\text {COSC }}=1.0 \mathrm{~V} ; 200 \mathrm{~mA}$ Sink | - | 1.2 | 1.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| GATE DC High Saturation Voltage | $\mathrm{V}_{\text {COSC }}=2.7 \mathrm{~V} ; 200 \mathrm{~mA}$ Source; $\mathrm{V}_{\mathrm{C}}=\mathrm{V}_{\text {GATE }}$ | - | 1.5 | 2.1 | V |
| Rise Time | $\mathrm{C}_{\text {GATE }}=1.0 \mathrm{nF} ; 1.5 \mathrm{~V}<\mathrm{V}_{\text {GATE }}<9.0 \mathrm{~V}$ | - | 25 | 60 | ns |
| Fall Time | $\mathrm{C}_{\text {GATE }}=1.0 \mathrm{nF} ; 9.0 \mathrm{~V}>\mathrm{V}_{\text {GATE }}>1.5 \mathrm{~V}$ | - | 25 | 60 | ns |

## Current Drain

| $I_{C C}$ | $3.135 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<3.465 \mathrm{~V}$, Gate switching | - | 3.5 | 6.0 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{C}}$ | $3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<16 \mathrm{~V}$, Gate non-switching | - | 2.7 | 4.0 | mA |

[^32]PACKAGE LEAD DESCRIPTION

| PACKAGE PIN NUMBER |  |  |  |
| :---: | :---: | :---: | :--- |
| SO-8 | DIP-8 | PIN SYMBOL |  |
| 1 | 1 |  | FUNCTION |
| 2 | 2 | PGND | Output power stage ground connection. |
| 3 | 3 | Cosc | Oscillator frequency programming capacitor. |
| 4 | 4 | GND | Logic ground. |
| 5 | 5 | $\mathrm{~V}_{\text {FB }}$ | Feedback voltage input. |
| 6 | 6 | $\mathrm{~V}_{\mathrm{CC}}$ | Logic supply voltage. |
| 7 | 7 | CS | Soft Start and fault timing capacitor. |
| 8 | 8 | $\mathrm{~V}_{\mathrm{C}}$ | Driver supply voltage. |



Figure 2. Block Diagram

## THEORY OF OPERATION

## Control Scheme

The CS51033 monitors the output voltage to determine when to turn on the PFET. If $\mathrm{V}_{\mathrm{FB}}$ falls below the internal reference voltage of 1.25 V during the oscillator's charge cycle, the PFET is turned on and remains on for the duration of the charge time. The PFET gets turned off and remains off during the oscillator's discharge cycle time with the maximum duty cycle to $80 \%$. It requires 7.0 mV typical, and 20 mV maximum ripple on the $\mathrm{V}_{\mathrm{FB}}$ pin to operate. This method of control does not require any loop stability compensation.

## Startup

The CS51033 has an externally programmable Soft Start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As $\mathrm{V}_{\mathrm{CC}}$ rises, the $\mathrm{V}_{\mathrm{C}}$ voltage along with the internal resistor $\mathrm{R}_{\mathrm{G}}$ keeps the PFET off. As $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}$ continue to rise, the oscillator capacitor (COSC) and the Soft Start/Fault Timing capacitor (CS) charges via internal current sources. COSC gets charged by the current source $I_{C}$ and $C S$ gets charged by the $I_{T}$ source combination described by:

$$
I_{C S}=I_{T}-\left(\frac{I T}{55}+\frac{I T}{5}\right)
$$

The internal Holdoff Comparator ensures that the external PFET is off until $\mathrm{V}_{\mathrm{CS}}>0.7 \mathrm{~V}$, preventing the GATE flip-flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft Start is obtained by clamping the $\mathrm{V}_{\mathrm{FB}}$ comparator's (A6) reference input to approximately $1 / 2$ of the voltage at the CS
pin during startup, permitting the control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7 V , the low feedback to the $\mathrm{V}_{\mathrm{FB}}$ Comparator sets the GATE flip-flop during CosC's charge cycle. Once the GATE flip-flop is set, $\mathrm{V}_{\text {GATE }}$ goes low and turns on the PFET. When $\mathrm{V}_{\mathrm{CS}}$ exceeds 2.4 V , the CS charge sense comparator ( A 4 ) sets the $\mathrm{V}_{\mathrm{FB}}$ comparator reference to 1.25 V completing the startup cycle.

## Lossless Short Circuit Protection

The CS51033 has "lossless" short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage ) reaches 2.5 V , the fault timing circuitry is enabled. During normal operation the CS voltage is 2.6 V . During a short circuit or a transient condition, the output voltage moves lower and the voltage at $\mathrm{V}_{\mathrm{FB}}$ drops. If $\mathrm{V}_{\mathrm{FB}}$ drops below 1.15 V , the output of the fault comparator goes high and the CS51033 goes into a fast discharge mode. The fault timing capacitor, CS, discharges to 2.4 V . If the $\mathrm{V}_{\mathrm{FB}}$ voltage is still below 1.15 V when the CS pin reaches 2.4 V , a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip flop. The $\mathrm{V}_{\text {GATE }}$ flip flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5 V . The CS51033 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5 V , the fast and slow discharge cycles repeat as shown in Figure 3.

If the $\mathrm{V}_{\mathrm{FB}}$ voltage is above 1.15 V when CS reaches 2.4 V a fault condition is not detected, normal operation resumes and CS charges back to 2.6 V . This reduces the chance of erroneously detecting a load transient as a fault condition.


Figure 3. Voltage on Start Capacitor ( $\mathrm{V}_{\mathrm{GS}}$ ), the Gate ( $\mathrm{V}_{\mathrm{GATE}}$ ), and in the Feedback Loop ( $\mathrm{V}_{\mathrm{FB}}$ ), During Startup, Normal and Fault Conditions.

## Buck Regulator Operation

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current $\mathrm{I}_{\mathrm{L}}$ is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor $\mathrm{C}_{\mathrm{O}}$. When the voltage across $\mathrm{C}_{\mathrm{O}}$ drops below the threshold established by the feedback resistors R1
and R2 and the reference voltage $\mathrm{V}_{\text {REF }}$, the power transistor Q1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by ( $\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}$ )/Load. The duty cycle (or "on" time) for the CS51033 is limited to $80 \%$. If output voltage remains higher than nominal during the entire CosC change time, the Q1 does not turn on, skipping the pulse.


Figure 4. Buck Regulator Block Diagram.

## Charge Pump Circuit

(Refer to the CS51033 Application Diagram on page 1573).

An external charge pump circuit is necessary when the $V_{C}$ input voltage is below 5.0 V to ensure that there is suffifient gate drive voltage for the external FET. When $\mathrm{V}_{\text {IN }}$ is applied, capacitors C 1 and C 2 will be charged to a diodes drop below $\mathrm{V}_{\text {IN }}$ via diodes D2 and D4, respectively. When the PFET
turns on, it's drain voltage will be approximately equal to $\mathrm{V}_{\mathrm{IN}}$. Since the voltage across C 1 can not change instantaneously, D2 is reverse biased and the anode voltage rises to approximately $2.0 \times 3.3 \mathrm{~V}-\mathrm{VD} 2$. C 1 transfers some of its stored charge C2 via D3. After several cycles there is sufficient gate drive voltage.

## APPLICATIONS INFORMATION

## DESIGNING A POWER SUPPLY WITH THE CS51033

## Specifications

- $\mathrm{V}_{\mathrm{IN}}=3.3 \mathrm{~V} \pm 10 \%$ (i.e. 3.63 V max., 2.97 V min.)
- $\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V} \pm 2.0 \%$
- $\mathrm{I}_{\text {OUT }}=0.3 \mathrm{~A}$ to 3.0 A
- Output ripple voltage $<33 \mathrm{mV}$.
- $\mathrm{F}_{\mathrm{SW}}=200 \mathrm{kHz}$


## 1) Duty Cycle Estimates

Since the maximum duty cycle D, of the CS51033 is limited to $80 \% \mathrm{~min}$., it is best to estimate the duty cycle for the various input conditions to see that the design will work over the complete operating range.

The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{D}}}{\mathrm{~V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{SAT}}}
$$

where:
$\mathrm{V}_{\mathrm{SAT}}=\mathrm{R}_{\mathrm{DS}(\mathrm{ON})} \times \mathrm{I}_{\mathrm{OUT}}$ Max.

In this case we can assume that $\mathrm{V}_{\mathrm{D}}=0.6 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{SAT}}=$ 0.6 V so the equation reduces to:

$$
\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}}{\mathrm{~V}_{\mathrm{IN}}}
$$

From this, the maximum duty cycle $\mathrm{D}_{\mathrm{MAX}}$ is $53 \%$, this occurs when $\mathrm{V}_{\mathrm{IN}}$ is at it's minimum while the minimum duty cycle $\mathrm{D}_{\mathrm{MIN}}$ is $0.35 \%$.

## 2) Switching Frequency and On and Off Time Calculations

$\mathrm{F}_{\mathrm{SW}}=200 \mathrm{kHz}$. The switching frequency is determined by CosC, whose value is determined by:

$$
\begin{gathered}
\operatorname{COSC}=\frac{95}{\mathrm{FSW}^{2} \times\left(1-\left(\frac{\mathrm{FSW}}{3 \times 10^{6}}\right)-\left(\frac{30 \times 10^{3}}{\mathrm{FSW}}\right)^{2}\right)} \cong 470 \mathrm{pF} \\
\mathrm{~T}=\frac{1.0}{\mathrm{FSW}}=5.0 \mu \mathrm{~s} \\
\operatorname{TON}(\mathrm{MAX})=5.0 \mu \mathrm{~s} \times 0.53=2.65 \mu \mathrm{~s}
\end{gathered}
$$

$$
\begin{gathered}
\mathrm{TON}(\mathrm{MIN})=5.0 \mu \mathrm{~s} \times 0.35=1.75 \mu \mathrm{~s} \\
\mathrm{TOFF}(\mathrm{MAX})=5.0 \mu \mathrm{~s}-0.7 \mu \mathrm{~s}=4.3 \mu \mathrm{~s}
\end{gathered}
$$

## 3) Inductor Selection

Pick the inductor value to maintain continuous mode operation down to 0.3 Amps.

The ripple current $\Delta \mathrm{I}=2 \times \mathrm{I}$ OUT $(\mathrm{MIN})=2 \times 0.3 \mathrm{~A}=0.6 \mathrm{~A}$.
$\mathrm{L}_{\mathrm{MIN}}=\frac{\mathrm{V}_{\text {OUT }}+\mathrm{V}_{\mathrm{D}} \times \operatorname{TOFF}(\mathrm{MAX})}{\Delta \mathrm{l}}=\frac{2.1 \mathrm{~V} \times 4.3 \mu \mathrm{~s}}{0.6 \mathrm{~A}} \cong 15 \mu \mathrm{H}$
The CS51033 will operate with almost any value of inductor. With larger inductors the ripple current is reduced and the regulator will remain in a continuous conduction mode for lower values of load current. A smaller inductor will result in larger ripple current. The core must not saturate with the maximum expected current, here given by:

$$
\mathrm{I} \mathrm{MAX}=\frac{\mathrm{IOUT}+\Delta \mathrm{I}}{2.0}=3.0 \mathrm{~A}+0.6 \mathrm{~A} / 2.0=3.3 \mathrm{~A}
$$

## 4) Output Capacitor

The output capacitor limits the output ripple voltage. The CS51033 needs a maximum of 15 mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50 mV peak to peak is given by:

$$
\begin{aligned}
\mathrm{CO} & =\frac{\Delta \mathrm{l}}{8.0 \times \mathrm{FSW} \times \Delta \mathrm{V}} \\
& =\frac{0.6 \mathrm{~A}}{8.0 \times\left(200 \times 10^{3} \mathrm{~Hz}\right) \times\left(33 \times 10^{-3 \mathrm{~V})} \cong 11.4 \mu \mathrm{~F}\right.}
\end{aligned}
$$

The minimum ESR needed to limit the output voltage ripple to 50 mV peak to peak is:

$$
\mathrm{ESR}=\frac{\Delta \mathrm{V}}{\Delta \mathrm{l}}=\frac{50 \times 10-3}{0.6 \mathrm{~A}}=55 \mathrm{~m} \Omega
$$

The output capacitor should be chosen so that its ESR is at least half of the calculated value and the capacitance is at least ten times the calculated value. It is often advisable to use several capacitors in parallel to reduce ESR.

Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are the cheapest but are not available in surface mount at present. Solid tantalum chip capacitors are available from a number of suppliers and offer the best choice for surface mount applications. The capacitor working voltage should be greater than the output voltage in all cases.

## 5) $\mathrm{V}_{\mathrm{FB}}$ Divider

$$
\mathrm{V}_{\mathrm{OUT}}=1.25 \mathrm{~V}\left(\frac{\mathrm{R} 1+\mathrm{R} 2}{\mathrm{R} 2}\right)=1.25 \mathrm{~V}\left(\frac{\mathrm{R} 1}{\mathrm{R} 2}+1.0\right)
$$

The input bias current to the comparator is $4.0 \mu \mathrm{~A}$. The resistor divider current should be considerably higher than
this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this gives a divider current of 1.0 mA and simplifies the calculations.

$$
\frac{1.5 \mathrm{~V}}{1.0 \mathrm{~mA}}=\mathrm{R} 1+\mathrm{R} 2=1.5 \mathrm{k} \Omega
$$

Let R2 $=1.0 \mathrm{k}$
Rearranging the divider equation gives:

$$
\mathrm{R} 1=\mathrm{R} 2\left(\frac{\mathrm{~V}_{\mathrm{OUT}}}{1.25}-1.0\right)=1.0 \mathrm{k} \Omega\left(\frac{1.5 \mathrm{~V}}{1.25}\right)=200 \Omega
$$

## 6) Divider Bypass Capacitor CRR $_{\text {R }}$

Since the feedback resistors divide the output voltage by a factor of 4.0 , i.e. $5.0 \mathrm{~V} / 1.25 \mathrm{~V}=4.0$, it follows that the output ripple is also divided by four. This would require that the output ripple be at least $60 \mathrm{mV}(4.0 \times 15 \mathrm{mV})$ to trip the feedback comparator. We use a capacitor $C_{R R}$ to act as an AC short so that the output ripple is not attenuated by the divider network. The ripple voltage frequency is equal to the switching frequency so we choose $C_{R R}$ so that:

$$
X_{C}=\frac{1.0}{2 \pi f C}
$$

is negligible at the switching frequency.
In this case $\mathrm{F}_{\mathrm{SW}}$ is 200 kHz if we allow $\mathrm{X}_{\mathrm{C}}=3.0 \Omega$ then:

$$
C=\frac{1.0}{2 \pi f 3} \cong 0.265 \mu \mathrm{~F}
$$

## 7) Soft Start and Fault Timing Capacitor CS

CS performs several important functions. First it provides a dead time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides Soft Start by clamping the reference voltage during startup to rise slowly and finally it controls the hiccup short circuit protection circuitry. This function reduces the PFET's duty cycle to $2.0 \%$ of the CS period.

The most important consideration in calculating CS is that it's voltage does not reach 2.5 V (the voltage at which the fault detect circuitry is enabled) before $\mathrm{V}_{\mathrm{FB}}$ reaches 1.15 V otherwise the power supply will never start.

If the $\mathrm{V}_{\mathrm{FB}}$ pin reaches 1.15 V , the fault timing comparator will discharge CS and the supply will not start. For the $\mathrm{V}_{\mathrm{FB}}$ voltage to reach 1.15 V the output voltage must be at least $4 \times 1.15=4.6 \mathrm{~V}$.
If we choose an arbitrary startup time of $200 \mu \mathrm{~s}$, we calculate the value of CS from:

$$
\begin{gathered}
\mathrm{T}=\frac{\mathrm{CS} \times 2.5 \mathrm{~V}}{\mathrm{I} \mathrm{CHARGE}} \\
\mathrm{CS}(\mathrm{MIN})=\frac{200 \mu \mathrm{~s} \times 264 \mu \mathrm{~A}}{2.5 \mathrm{~V}}=0.02 \mu \mathrm{~F}
\end{gathered}
$$

Use $0.1 \mu \mathrm{f}$.

The fault time out time is the sum of the slow discharge time the fast discharge time and the recharge time and is obviously dominated by the slow discharge time.

The first parameter is the slow discharge time, it is the time for the CS capacitor to discharge from 2.4 V to 1.5 V and is given by:

$$
\text { TSLOWDISCHARGE }=\frac{\mathrm{CS} \times(2.4 \mathrm{~V}-1.5 \mathrm{~V})}{\mathrm{I} \text { DISCHARGE }}
$$

where $I_{\text {DISCHARGE }}$ is $6.0 \mu \mathrm{~A}$ typical.

$$
\text { TSLOWDISCHARGE }=\mathrm{CS} \times 1.5 \mathrm{~V} \times 10^{5}
$$

The fast discharge time occurs when a fault is first detected. The CS capacitor is discharged from 2.5 V to 2.4 V .

$$
\text { TFASTDISCHARGE }=\frac{\mathrm{CS} \times(2.5 \mathrm{~V}-2.4 \mathrm{~V})}{\mathrm{I} \text { FASTDISCHARGE }}
$$

where $\mathrm{I}_{\text {FASTDISCHARGE }}$ is $66 \mu \mathrm{~A}$ typical.

$$
\text { TFASTDISCHARGE }=\text { CS } \times 1515
$$

The recharge time is the time for CS to charge from 1.5 V to 2.5 V .

$$
\text { TCHARGE }=\frac{\mathrm{CS} \times(2.5 \mathrm{~V}-1.5 \mathrm{~V})}{\mathrm{I} \mathrm{CHARGE}}
$$

where $I_{\text {CHARGE }}$ is $264 \mu \mathrm{~A}$ typical.

$$
\text { TCHARGE }=\mathrm{CS} \times 3787
$$

The fault time out time is given by:

$$
\begin{gathered}
\mathrm{T}_{\mathrm{FAULT}}=\mathrm{CS} \times\left(3787+1515+1.5 \times 10^{5}\right) \\
\mathrm{T}_{\mathrm{FAULT}}=\mathrm{CS} \times(1.55 \times 105)
\end{gathered}
$$

For this circuit

$$
\mathrm{T}_{\text {FAULT }}=0.1 \times 10^{-6} \times 1.55 \times 10^{5}=0.0155
$$

A larger value of CS will increase the fault time out time but will also increase the Soft Start time.

## 8) Input Capacitor

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on
the $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}$ pins. This capacitor must also ensure that the $\mathrm{V}_{\mathrm{CC}}$ remains above the UVLO voltage in the event of an output short circuit. $\mathrm{C}_{\text {IN }}$ should be a low ESR capacitor of at least $100 \mu \mathrm{~F}$. A ceramic surface mount capacitor should also be connected between $\mathrm{V}_{\mathrm{CC}}$ and ground to prevent spikes.

## 9) MOSFET Selection

The CS51033 drives a P-channel MOSFET. The $\mathrm{V}_{\text {GATE }}$ pin swings from GND to $\mathrm{V}_{\mathrm{C}}$. The type of PFET used depends on the operating conditions but for input voltages below 7.0 V a logic level FET should be used.

Choose a PFET with a continuous drain current ( $\mathrm{I}_{\mathrm{D}}$ ) rating greater than the maximum output current. $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ should be less than

$$
\operatorname{RDS}<=\frac{0.6 \mathrm{~V}}{\operatorname{lOUT}(\mathrm{MAX})} 167 \mathrm{~m} \Omega
$$

The Gate-to-Source voltage $\mathrm{V}_{\mathrm{GS}}$ and the Drain-to Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$
P_{D}=I_{O U T}{ }^{2} \times \operatorname{RDS}(O N) \times D
$$

The power dissipation due to the switching losses is given by:

$$
\mathrm{PD}_{\mathrm{D}}=0.5 \times \mathrm{V}_{\text {IN }} \times \mathrm{IOUT} \times\left(\mathrm{T}_{\mathrm{R}}{ }^{r}+\mathrm{T}_{\mathrm{F}}\right) \times \mathrm{FSW}
$$

where $T_{R}=$ Rise Time and $T_{F}=$ Fall Time.

## 10) Diode Selection

The flyback or catch diode should be a Schottky diode because of it's fast switching ability and low forward voltage drop. The current rating must be at least equal to the maximum output current. The breakdown voltage should be at least 20 V for this 12 V application.

The diode power dissipation is given by:

$$
\mathrm{PD}_{\mathrm{D}}=\mathrm{IOUT} \times \mathrm{V}_{\mathrm{D}} \times\left(1.0-\mathrm{D}_{\mathrm{MIN}}\right)
$$

## CS51033

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package | Shipping |
| :--- | :---: | :---: | :---: |
| CS51033ED8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51033EDR8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51033EN8 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | DIP-8 | 50 Units/Rail |
| CS51033GD8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 95 Units/Rail |
| CS51033GDR8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-8 | 2500 Tape \& Reel |
| CS51033GN8 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | DIP-8 | 50 Units/Rail |

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | DIP-8 | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 45 | 52 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 165 | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5211

## Low Voltage Synchronous Buck Controller

The CS5211 is a low voltage synchronous buck controller. It contains all required circuitry for a synchronous buck converter using external N-Channel MOSFETs. High current internal gate drivers are capable of driving high gate capacitance of low $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ NFETs for better efficiency. The $\mathrm{V}^{2 \mathrm{TM}}$ control architecture is used to achieve unmatched transient response, the best overall regulation and the simplest loop compensation. The CS5211 is in a 14-pin package to allow the designer added flexibility.

The CS5211 provides overcurrent protection, undervoltage lockout, Soft Start and built in adaptive nonoverlap. The CS5211 also provides adjustable fixed frequency range of 150 kHz to 750 kHz . This gives the designer more flexibility to make efficiency and component size compromises. The CS5211 will operate over a 4.5 V to 14 V range using either single of dual input voltage.

## Features

- Switching Regulator Controller
- N-Channel Synchronous Buck Design
- $\mathrm{V}^{2}$ Control Topology
- 200 ns Transient Response
- Programmable Fixed Frequency of $150 \mathrm{kHz}-750 \mathrm{kHz}$
- $1.0 \mathrm{~V} 1.5 \%$ Internal Reference
- Lossless Inductor Sensing Overcurrent Protection
- Hiccup Mode Short Circuit Protection
- Programmable Soft Start
- 40 ns GATE Rise and Fall Times (3.3 nF Load)
- 70 ns Adaptive FET Nonoverlap Time
- Differential Remote Sense Capability
- System Power Management
- 5.0 V or 12 V Operation
- Undervoltage Lockout
- On/Off Control Through Use of the COMP Pin


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1594 of this data sheet.


Figure 1. Application Diagram, 5.0 V to 2.5 V/8.0 A Converter with Differential Remote Sense

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\text {S }}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance: Junction-to-Case, R ®Jc Junction-to-Ambient, R ®JA |  | $\begin{gathered} 30 \\ 125 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| JEDEC Moisture Sensitivity |  | 1.0 | - |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | ISOURCE | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\text {CC }}$ | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | 50 mA DC |
| Power input for the low side driver | $\mathrm{V}_{\mathrm{C}}$ | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ |
| Power Supply input for the high <br> side driver | BST | 20 V | -0.3 V | $1.5 \mathrm{~A} \mathrm{Peak} 200 mA DC$, |  |
| Compensation Capacitor | COMP | 6.0 V | -0.3 V | $1.5 \mathrm{~A} \mathrm{Peak} 200 mA DC$, |  |
| Voltage Feedback Input | $\mathrm{V}_{\text {FB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Oscillator Resistor | $\mathrm{R}_{\text {OSC }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

## MAXIMUM RATINGS (continued)

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fast Feedback Input | $\mathrm{V}_{\text {FFB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| High-Side FET Driver | GATE(H) | 20 V | -0.3 V <br> -2.0 V for 50 ns | 1.5 A Peak <br> 200 mA DC | 1.5 A Peak <br> 200 mA DC |
| Low-Side FET Driver | GATE(L) | 16 V | -0.3 V <br> -2.0 V for 50 ns | 1.5 A Peak <br> 200 mA DC | 1.5 A Peak <br> 200 mA DC |
| Positive Current Sense | IS+ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Negative Current Sense | IS- | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Power Ground | PGND | 0.3 V | -0.3 V | 1.5 A Peak, 200 mA DC | $\mathrm{N} / \mathrm{A}$ |
| Logic Ground | LGND | 0 V | 0 V | 100 mA | $\mathrm{~N} / \mathrm{A}$ |
| Sense Ground | SGND | 0.3 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}<14 \mathrm{~V}\right.$;
$7.0 \mathrm{~V}<\mathrm{BST}<20 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}(\mathrm{H})=\mathrm{C}_{\mathrm{GATE}}(\mathrm{L})=3.3 \mathrm{nF} ; \mathrm{R}_{\mathrm{OSC}}=51 \mathrm{k} ; \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Error Amplifier |  |  |  |  |  |
| $V_{\text {FB }}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| COMP Source Current | $\mathrm{V}_{\mathrm{FB}}=0.8 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP SINK Current | $\mathrm{V}_{\mathrm{FB}}=1.2 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Open Loop Gain | - | - | 98 | - | dB |
| Unity Gain Bandwidth | $\mathrm{C}=0.1 \mu \mathrm{~F}$ | - | 50 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |
| Output Transconductance | - | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Reference Voltage | $\begin{aligned} & -0.1 \mathrm{~V}<\mathrm{SGND}<0.1 \mathrm{~V}, \\ & \mathrm{COMP}=\mathrm{V}_{\mathrm{FB}}, \text { Measure } \mathrm{V}_{\mathrm{FB}} \text { to } \mathrm{SGND} \end{aligned}$ | 0.977 | 0.992 | 1.007 | V |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=0.8 \mathrm{~V}$ | 2.5 | 3.0 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.2 \mathrm{~V}$ | - | 0.1 | 0.2 | V |

GATE(H) and GATE(L)

| High Voltage (AC) | GATE(L), <br> GATE(H) $0.5 \mathrm{nF}<\mathrm{C}_{\mathrm{GATE}(H)}=\mathrm{C}_{\mathrm{GATE}(\mathrm{~L})}<10 \mathrm{nF}$ | $\begin{gathered} \mathrm{V}_{\mathrm{C}}-0.5 \\ \mathrm{BST}-0.5 \end{gathered}$ | - | - | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | $\operatorname{GATE}(\mathrm{L})$ or $\operatorname{GATE}(\mathrm{H})$ $0.5 \mathrm{nF}<\mathrm{C}_{\mathrm{GATE}(\mathrm{H})} ; \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}<10 \mathrm{nF}$ | - | - | 0.5 | V |
| Rise Time | $\begin{gathered} \mathrm{V}_{\mathrm{C}}=\mathrm{BST}=10 \mathrm{~V}, \text { Measure: } \\ 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{L})<9.0 \mathrm{~V}, \\ 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{H})<9.0 \mathrm{~V} \end{gathered}$ | - | 40 | 80 | ns |
| Fall Time | $\begin{gathered} \mathrm{V}_{\mathrm{C}}=\mathrm{BST}=10 \mathrm{~V}, \text { Measure: } \\ 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{L})<9.0 \mathrm{~V}, \\ 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{H})<9.0 \mathrm{~V} \end{gathered}$ | - | 40 | 80 | ns |
| GATE(H) to GATE(L) Delay | $\operatorname{GATE}(\mathrm{H})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{~L})>2.0 \mathrm{~V}$ | 40 | 70 | 110 | ns |
| GATE(L) to GATE(H) Delay | GATE $(\mathrm{L})<2.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{H})>2.0 \mathrm{~V}$ | 40 | 70 | 110 | ns |
| GATE(H)/(L) Pull-Down | Resistance to PGND | 20 | 50 | 115 | K $\Omega$ |

2. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}<14 \mathrm{~V}\right.$; $7.0 \mathrm{~V}<\mathrm{BST}<20 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{R}_{\mathrm{OSC}}=51 \mathrm{k} ; \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Overcurrent Protection

| OVC Comparator Offset Voltage | $0 \mathrm{~V}<\mathrm{IS}+<\mathrm{V}_{\mathrm{CC}}, 0 \mathrm{~V}<\mathrm{IS}-<\mathrm{V}_{\mathrm{CC}}$ | 54 | 60 | 66 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| IS+ Bias Current | $0 \mathrm{~V}<\mathrm{IS}+<\mathrm{V}_{\mathrm{CC}}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| IS- Bias Current | $0 \mathrm{~V}<\mathrm{IS}-<\mathrm{V}_{\mathrm{CC}}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| COMP Discharge Threshold |  | 0.20 | 0.25 | 0.30 | V |
| COMP Discharge Current in OVC <br> Fault Mode | $\mathrm{COMP}=1.0 \mathrm{~V}$ | 2.0 | 5.0 | 8.0 | $\mu \mathrm{~A}$ |

PWM Comparator

| Transient Response | COMP $=0-1.5 \mathrm{~V}, \mathrm{~V}_{\text {FFB }}, 20 \mathrm{mV}$ overdrive | - | 100 | 200 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PWM Comparator Offset | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$; Increase COMP until GATE(H) starts switching | 0.425 | 0.475 | 0.525 | V |
| Artificial Ramp | Duty Cycle $=90 \%$ | 40 | 70 | 100 | mV |
| $V_{\text {FFB }}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| $V_{\text {FFB }}$ Input Range | Note 3. | - | - | 1.1 | V |
| Minimum Pulse Width | - | - | - | 200 | ns |

## Oscillator

| Switching Frequency | R OSC $=18 \mathrm{k}$ | 600 | 750 | 900 | kHz |
| :--- | :--- | :--- | :--- | :--- | :---: |
| Switching Frequency | $\mathrm{R}_{\text {OSC }}=51 \mathrm{k}$ | 240 | 300 | 360 | kHz |
| Switching Frequency | $\mathrm{R}_{\text {OSC }}=96 \mathrm{k}$ | 120 | 150 | 180 | kHz |
| R OSC Voltage |  | 1.21 | 1.25 | 1.29 | V |

## General Electrical Specifications

| $V_{C C}$ Supply Current | COMP $=0$ V (no switching) | - | 5.0 | 8.0 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| BST/V $\mathrm{V}_{\mathrm{C}}$ Supply Current | COMP $=0$ V (no switching) | - | 2.0 | 3.0 | mA |
| Start Threshold | GATE(H) Switching, COMP Charging | 3.90 | 4.05 | 4.20 | V |
| Stop Threshold | GATE(H) Not Switching, COMP Not Charging | 3.75 | 3.90 | 4.05 | V |
| Hysteresis | Start-Stop | 100 | 150 | 200 | mV |
| Sense Ground Current | Note 3. | - | 0.15 | 1.00 | mA |

3. Recommended maximum operating voltage between the three grounds is 200 mV .

## PACKAGE PIN DESCRIPTION

| PIN NO. | PIN SYMBOL | FUNCTION |
| :---: | :---: | :--- |
| 1 | GATE(H) | High Side Switch FET driver pin. Capable of delivering peak currents of 1.0 A. |
| 2 | BST | Power supply input for the high side driver. |
| 3 | LGND | Reference ground. All control circuits are referenced to this pin. IC substrate connection. |
| 4 | V $_{\text {FFB }}$ | Input for the PWM comparator. |
| 5 | VFB $^{\text {COMP }}$ | Error amplifier input. |
| 6 | SGND | Error Amp output. PWM Comparator reference input. A capacitor to LGND provides error amp <br> compensation. |
| 7 | Internal reference is connected to this ground. Connect directly at the load for ground remote <br> sensing. |  |
| 8 | VCC | A resistor from this pin to SGND sets switching frequency. |
| 10 | IS- | Input Power Supply Pin. It supplies power to control circuitry. A 0.1 $\mu$ F Decoupling cap is rec- <br> ommended. |
| 11 | Vegative input for overcurrent comparator. |  |
| 12 | GATE(L) | Positive input for overcurrent comparator. |
| 13 | PGND | High Current ground for the GATE(H) and GATE(L) pins. |
| 14 |  |  |



Figure 2. Block Diagram

## THEORY OF OPERATION

## $V^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variations in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. $\mathrm{V}^{\mathbf{2}}$ Control Block Diagram
The $V^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of the change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in the inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an effect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this "slow" feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulations are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variations, since both line and load affect the ramp signal.

## Constant Frequency Operation

The CS5211 uses a constant frequency, trailing edge modulation architecture for generating PWM signal. During normal operation, the oscillator generates a narrow pulse at the beginning of each switching cycle to turn on the main switch. The main switch will be turned off when the ramp signal intersects with the output of the error amplifier (COMP pin voltage). Therefore, the switch duty cycle can be modified to regulate the output voltage to the desired value as line and load conditions change.
The major advantage of constant frequency operation is that the component selections, especially the magnetic component design, become very easy. The oscillator frequency of CS5211 is programmable from 150 kHz to 750 kHz using an external resistor connected from the R OSC pin to ground.

## Start-Up

If there are no fault conditions and the fault latch is reset, the error amplifier will start charging the COMP pin capacitor after the CS5211 is powered up. The output of the error amplifier (COMP voltage) will ramp up linearly. The COMP capacitance and the source current of the error amplifier determine the slew rate of COMP voltage. The output of the error amplifier is connected internally to the inverting input of the PWM comparator and it is compared with the $\mathrm{V}_{\text {FFB }}$ pin voltage plus 0.5 V offset at the non-inverting input of the PWM comparator. Since $\mathrm{V}_{\mathrm{FFB}}$ voltage is zero before the start-up, the PWM comparator output will stay high until the COMP pin voltage hits 0.5 V . There is no switching action while the PWM comparator output is high.
After the COMP voltage exceeds the 0.5 V offset, the output of PWM comparator toggles and releases the PWM latch. The narrow pulse generated by the oscillator at the beginning of the next oscillator cycle will set the latch so that the main switch can be turned on and the regulator output voltage ramps up. When the output voltage achieves a level set by the COMP voltage, the main switch will be turned off. The $\mathrm{V}^{2}$ control loop will adjust the main switch duty cycle as required to ensure the regulator output voltage tracks the

COMP voltage. Since the COMP voltage increases gradually, the Soft-Start can be achieved. The start-up period ends when the output voltage reaches the level set by the external resistor divider.

## Output Enable

Since there can be no switching until the COMP pin exceeds the 0.5 V offset built into the PWM comparator, the COMP pin can also be used for an enable function. Hold the COMP pin below 0.4 V with an open collector circuit to disable the output. When the COMP pin is released to enable start-up, the user must ensure there is no leakage current from the enable circuit into COMP. During normal operation the COMP output is driven with only $5.0 \mu \mathrm{~A}$ to $30 \mu \mathrm{~A}$ internally.

## Hiccup Mode Overcurrent Protection

Under normal load conditions, the voltage across the IS+ and IS- pins is less than the 60 mV overcurrent threshold. If the threshold is exceeded, the overcurrent fault latch is set, the high side gate driver is forced low, and the COMP pin is discharged with $5.0 \mu \mathrm{~A}$. There is no switching until the COMP voltage drops below a 0.25 V threshold. Then, the fault latch is cleared and a soft-start is initiated. The low effective duty cycle during hiccup overcurrent greatly reduces component stress for an extended fault.

## Inductor Current Sensing

Besides using a current sense resistor to sense inductor current, CS5211 provides the users with the possibility of using loss-less inductor sensing technique. This sensing technique utilizes the Equivalent Series Resistance (ESR) of the inductor to sense the current. The output current is sensed through an RC network in parallel with the inductor as shown in Figure 4. The voltage across the small capacitor is then fed to the OC comparator.


Figure 4. Inductor Current Sensing

If the values of R and C are chosen such that:

$$
\frac{L}{R_{L}}=R C
$$

Then the voltage across the capacitor C will be:

$$
V_{C}=R_{L} I_{L}
$$

Therefore, if the time constant of the RC network is equal to that of the inductor, the voltage across the capacitor is proportional to the inductor current by a factor of the inductor ESR. In practice, the user should ensure that under all component tolerances, the RC time constant is larger than the $\mathrm{L} / \mathrm{R}$ time constant. This will keep the high frequency gain for $\mathrm{V}_{\mathrm{C}}(\mathrm{s}) / \mathrm{I}_{\mathrm{L}}(\mathrm{s})$ less than the low frequency gain, and avoid unnecessary OCP tripping during short duration overcurrent situations.

Compared with conventional resistor sensing, the inductor ESR current sensing technique is lossless, but is not as accurate due to variation in the ESR from inductor to inductor and over temperature. For typical inductor ESR, the $0.39 \% /{ }^{\circ} \mathrm{C}$ positive temperature coefficient will reduce the current limit at high temperature, and will help prevent thermal runaway, but will force an increased design target at room temperature. This technique can be more accurate than using a PCB trace, since PCB copper thickness can vary $10-20 \%$, compared to $1 \%$ variation in wire diameter thickness typical of inductors.

## Remote Voltage Sensing

The CS5211 has the capability to sense the voltage when the load is located far away from the regulator. The SGND pin is dedicated to the differential remote sensing. The negative remote sense line is connected to SGND pin directly, while the positive remote sense line is usually connected to the top of the feedback voltage divider. To prevent over-voltage condition caused by open remote sense lines, the divider should also be locally connected to the output of the regulator through a low value resistor. That resistor is used to compensate for the voltage drop across the output power cables.

## APPLICATIONS AND COMPONENT SELECTION

## Inductor Component Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady-state and transient performance of the converter. When selecting an inductor the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size, and cost (usually the primary concern).

In general, the output inductance value should be as low and physically small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc) resulting in increased dissipation and lower converter efficiency. Also, increased ripple currents will force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors - the converter cost will be adversely effected.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. The following equation may be used to calculate the minimum inductor value to produce a given maximum ripple current ( $\alpha \bullet \mathrm{I}_{\mathrm{O}, \mathrm{MAX}}$ ). The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the maximum ripple current.

$$
\text { LoMIN }=(\text { Vin }- \text { Vout }) \cdot \text { Vout } /(\alpha \cdot \text { IO,MAX } \cdot \text { Vin } \cdot \text { fSW })
$$

$\alpha$ is the ripple current as a percentage of the maximum output current ( $\alpha=0.15$ for $\pm 15 \%, \alpha=0.25$ for $\pm 25 \%$, etc) and $f_{s w}$ is the switching frequency. If the minimum inductor value is used, the inductor current will swing $\pm \alpha / 2 \%$ about Iout. Therefore, the inductor must be designed or selected such that it will not saturate with a peak current of $(1+\alpha / 2)$

- IO,MAX.

Power dissipation in the inductor can now be calculated from the RMS current level. The RMS of the AC component of the inductor is given by the following relationship:

$$
I_{A C}=\frac{I P P}{\sqrt{12}}
$$

where IPP $=\alpha \bullet \mathrm{I}_{\mathrm{O}, \mathrm{MAX}}$.
The total $\mathrm{I}_{\mathrm{RMS}}$ of the current will be calculated from:

$$
\mathrm{I}_{\mathrm{RMS}}=\sqrt{\mathrm{IOUT}}{ }^{2}+\mathrm{I}_{\mathrm{AC}}{ }^{2}
$$

The power dissipation for the inductor can be determined from:

$$
\mathrm{P}=\mathrm{I}_{\mathrm{RMS}}{ }^{2} \times \mathrm{R}_{\mathrm{L}}
$$

## Input Capacitor Selection and Considerations

The input capacitor is used to reduce the current surges caused by conduction of current of the top pass transistor charging the PWM inductor.

The input current is pulsing at the switching frequency going from 0 to peak current in the inductor. The duty factor will be a function of the ratio of the input to output voltage and of the efficiency.

$$
D F=\frac{V_{\mathrm{O}}}{\mathrm{~V}_{\mathrm{I}}} \times \frac{1}{E f f}
$$

The RMS value of the ripple into the input capacitors can now be calculated:

$$
\operatorname{IIN}(\mathrm{RMS})=\operatorname{IOUT} \sqrt{D F-D F^{2}}
$$

The input RMS is maximum at $50 \% \mathrm{DF}$, so selection of the possible duty factor closest to $50 \%$ will give the worst case dissipation in the capacitors. The power dissipation of the input capacitors can be calculated by multiplying the square of the RMS current by the ESR of the capacitor.

## Output Capacitor

The output capacitor filters output inductor ripple current and provides low impedance for load current changes. The effect of the capacitance for handling the power supply induced ripple will be discussed here. Effects of load transient behavior can be considered separately.
The principle consideration for the output capacitor is the ripple current induced by the switches through the inductor. This ripple current was calculated as $\mathrm{I}_{\mathrm{AC}}$ in the above discussion of the inductor. This ripple component will induce heating in the capacitor by a factor of the RMS current squared multiplied by the ESR of the output capacitor section. It will also create output ripple voltage.

The ripple voltage will be a vector summation of the ripple current times the ESR of the capacitor, plus the ripple current integrating in the capacitor, and the rate of change in current times the total series inductance of the capacitor and connections.
The inductor ripple current acting against the ESR of the output capacitor is the major contributor to the output ripple voltage. This fact can be used as a criterion to select the output capacitor.

$$
V_{P P}=I P P \times C_{E S R}
$$

The power dissipation in the output capacitor can be calculated from:

$$
P=I_{A C}{ }^{2} \times C_{E S R}
$$

where:
$\mathrm{I}_{\mathrm{AC}}=\mathrm{AC}$ RMS of the inductor
$\mathrm{C}_{\text {ESR }}=$ Effective series resistance of the output capacitor network.

## MOSFET \& Heatsink Selection

Power dissipation, package size, and thermal solution drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non-overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$
\begin{aligned}
& \text { Pd,CONTROL }=\left(\text { IRMS,CNTL }{ }^{2} \cdot \operatorname{RDS}(o n)\right) \\
& +\left(\mathrm{L}_{\mathrm{L}, \mathrm{MAX}} \cdot \mathrm{Q}_{\text {switch }} / \mathrm{Ig} \cdot \mathrm{~V}_{\mathrm{IN}} \cdot \mathrm{fs}^{2}\right) \\
& +\left(Q_{\text {oss }} / 2 \cdot V_{\text {IN }} \cdot f S W\right)+\left(V_{\text {IN }} \cdot Q_{R R} \cdot f S W\right)
\end{aligned}
$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the losses associated with the control and synchronous MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the synchronous MOSFET. The first two terms are usually adequate to predict the majority of the losses.

Where $\mathrm{I}_{\mathrm{RMS}, \mathrm{CNTL}}$ is the RMS value of the trapezoidal current in the control MOSFET:

$$
\begin{aligned}
I_{R M S, C N T L}=\sqrt{D} & \cdot\left[\left(I_{\text {Lo }}, M A X^{2}+I_{\text {Lo }}, M A X \cdot I_{\text {Lo }}, \mathrm{MIN}\right.\right. \\
& \left.+I_{\left.\mathrm{Lo}, \mathrm{MIN}^{2}\right) / 3}\right]^{1 / 2}
\end{aligned}
$$

$\mathrm{I}_{\text {Lo,MAX }}$ is the maximum output inductor current:

$$
\mathrm{I}_{\mathrm{Lo}, \mathrm{MAX}}=\mathrm{I} \mathrm{O}, \mathrm{MAX} / 2+\Delta \mathrm{I}_{\mathrm{Lo}} / 2
$$

$\mathrm{I}_{\text {Lo,MIN }}$ is the minimum output inductor current:

$$
\mathrm{I} \mathrm{Lo}, \mathrm{MIN}=\mathrm{I}, \mathrm{MAX} / 2-\Delta \mathrm{I} \mathrm{Lo} / 2
$$

$\mathrm{I}_{\mathrm{O}, \text { MAX }}$ is the maximum converter output current.
D is the duty cycle of the converter:
D = VOUT/VIN
$\Delta \mathrm{I}_{\mathrm{Lo}}$ is the peak-to-peak ripple current in the output inductor of value Lo:

$$
\Delta \mathrm{I}_{\mathrm{Lo}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \cdot \mathrm{D} /(\mathrm{Lo} \cdot \mathrm{fSW})
$$

$\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ is the ON resistance of the MOSFET at the applied gate drive voltage.

Qswitch is the post gate threshold portion of the gate-to-source charge plus the gate-to-drain charge. This
may be specified in the data sheet or approximated from the gate-charge curve as shown in the Figure 5.

$$
Q_{\text {switch }}=Q_{g s 2}+Q_{g d}
$$



Figure 5. MOSFET Switching Characteristics
$\mathrm{I}_{\mathrm{g}}$ is the output current from the gate driver IC.
$\mathrm{V}_{\text {IN }}$ is the input voltage to the converter.
$\mathrm{f}_{\text {sw }}$ is the switching frequency of the converter.
$\mathrm{Q}_{\mathrm{G}}$ is the MOSFET total gate charge to obtain $\mathrm{R}_{\mathrm{DS}(\text { on })}$. Commonly specified in the data sheet.
$\mathrm{V}_{\mathrm{g}}$ is the gate drive voltage.
$\mathrm{Q}_{\mathrm{RR}}$ is the reverse recovery charge of the lower MOSFET.
$\mathrm{Q}_{\text {oss }}$ is the MOSFET output charge specified in the data sheet.
For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$
\begin{aligned}
& \text { PD,SYNCH }=\left(I_{R M S}, S Y N C H^{2} \cdot \operatorname{RDS}(o n)\right) \\
& \quad+\left(\text { Vf }_{\text {diode }} \cdot \mathrm{IO}_{\mathrm{O}}, \mathrm{MAX} / 2 \cdot \mathrm{t} \text { _nonoverlap } \cdot \mathrm{fSW}\right)
\end{aligned}
$$

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non-overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$
\begin{aligned}
& \text { IRMS,SYNCH }=\sqrt{1-\mathrm{D}} \\
& \quad \cdot\left[\left(\text { ILo }_{\text {Lo }}\right.\right. \text { MAX }
\end{aligned}
$$

where:
$\mathrm{Vf}_{\text {diode }}$ is the forward voltage of the MOSFET's intrinsic diode at the converter output current.
t _nonoverlap is the non-overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.
When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature

$$
\theta \mathrm{T}<\left(\mathrm{T}_{\mathrm{J}}-\mathrm{T}_{\mathrm{A}}\right) / \mathrm{P}_{\mathrm{D}}
$$

where;
$\theta_{\mathrm{T}}$ is the total thermal impedance $\left(\theta_{\mathrm{JC}}+\theta_{\mathrm{SA}}\right)$.
$\theta_{\mathrm{JC}}$ is the junction-to-case thermal impedance of the MOSFET.
$\theta_{\mathrm{SA}}$ is the sink-to-ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal "pad" is used).
$\mathrm{T}_{\mathrm{J}}$ is the specified maximum allowed junction temperature.
$\mathrm{T}_{\mathrm{A}}$ is the worst case ambient operating temperature.
For TO-220 and TO-263 packages, standard FR-4 copper clad circuit boards will have approximate thermal resistances $\left(\theta_{\mathrm{SA}}\right)$ as shown below:

| Pad Size <br> (in $^{2} / \mathrm{mm}^{2}$ ) | Single-Sided <br> $\mathbf{1}$ oz. Copper |
| :---: | :---: |
| $0.5 / 323$ | $60-65^{\circ} \mathrm{C} / \mathrm{W}$ |
| $0.75 / 484$ | $55-60^{\circ} \mathrm{C} / \mathrm{W}$ |
| $1.0 / 645$ | $50-55^{\circ} \mathrm{C} / \mathrm{W}$ |
| $1.5 / 968$ | $45-50^{\circ} \mathrm{C} / \mathrm{W}$ |
| $2.0 / 1290$ | $38-42^{\circ} \mathrm{C} / \mathrm{W}$ |
| $2.5 / 1612$ | $33-37^{\circ} \mathrm{C} / \mathrm{W}$ |

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e. worst case MOSFET $\mathrm{R}_{\mathrm{DS}(o n)}$ ). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, its advisable to have as much heatsink area as possible - all too often new designs are found to be too hot and require re-design to add heatsinking.

## Compensation Capacitor Selection

The nominal output current capability of the error amp is $30 \mu \mathrm{~A}$. This current charging the capacitor on the COMP pin is used as soft start for the converter. The COMP pin is going to ramp up to a voltage level that is within 70 mV of what $\mathrm{V}_{\mathrm{FFB}}$ is going to be when in regulation. This is the voltage that will determine the soft start. Therefore, the COMP capacitor can be established by the following relationship:

$$
\mathrm{C}=30 \mu \mathrm{~A} \times \frac{\text { soft start }}{\mathrm{V}_{\mathrm{FFB}}(\mathrm{REG})}
$$

where:
soft start = output ramp-up time
$\mathrm{V}_{\mathrm{FFB}(\mathrm{REG})}=\mathrm{V}_{\mathrm{FFB}}$ voltage when in regulation
$30 \mu \mathrm{~A}=$ COMP output current, typ.

The COMP output current range is given in the data sheet and will affect the ramp-up time. The value of the capacitor on the COMP pin will have an effect on the loop response and the transient response of the converter. Transient response can be enhanced by the addition of a parallel combination of a resistor and capacitor between the COMP pin and the comp capacitor.

## $\mathrm{R}_{\text {osc }}$ Selection

The switching frequency is programmed by selecting the resistor connected between the R $_{\text {OSC }}$ pin and SGND (pin 7). The grounded side of this resistor should be directly connected to the SGND pin, without any other currents flowing between the bottom of the resistor and the pin. Also, avoid running any noisy signals under the resistor, since injected noise could cause frequency jitter. The graph in Figure 6 shows the required resistance to program the frequency. Below 500 kHz , the following formula is accurate:

$$
R=13500 / \mathrm{f} S W+6 \mathrm{k} \Omega
$$

where $\mathrm{f}_{\mathrm{SW}}$ is the switching frequency in kHz .


Figure 6. Frequency vs. Rosc

## Differential Remote Sense Operation

The ability to implement fully differential remote sense is provided by the CS5211. The positive remote sense is implemented by bringing the output remote sense connection to the positive load connection. A low value resistor is connected from Vout to the feedback point at the regulator to provide feedback in the instance when the remote sense point is not connected.
The negative remote sense connection is provided by connecting the SGND of the CS5211 to the negative of the load return. Again, a low value resistor should be connected between SGND and LGND at the regulator to provide feedback in the instance when the remote sense point is not connected. The maximum voltage differential between the three grounds for this part is 200 mV .

## Feedback Divider Selection

The feedback voltage measured at $\mathrm{V}_{\mathrm{FB}}$ during normal regulation will be 1.0 V . This voltage is compared to an internal 1.0 V reference and is used to regulate the output voltage. The bias current into the error amplifier is $1.0 \mu \mathrm{~A}$ max, so select the resistor values so that this current does not add an excessive offset voltage.

## $V_{\text {FFB }}$ Feedback Selection

To take full advantage of the $\mathrm{V}^{2}$ control scheme, a small amount of output ripple must be fed back to the $V_{\text {FFB }}$ pin, typically 50 mV . For most application, this requirement is simple to achieve and the $V_{\mathrm{FFB}}$ can be connected directly to the $\mathrm{V}_{\mathrm{FB}}$ pin. There are some application that have to meet stringent load transient requirements. One of the key factor in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. This situation could result in increase noise sensitivity and a potential for loop instability. In applications where the output ripple is not sufficient, the performance of the CS5211 can be improved by adding a fixed amount external ramp compensation to the $\mathrm{V}_{\mathrm{FFB}}$ pin. Refer to Figure 7, the amount of ramp at the $\mathrm{V}_{\mathrm{FFB}}$ pin depends on the switch node Voltage, Feedback Voltage, R1 and C2.

$$
\text { Vramp }=\left(V s w-V_{F B}\right) \times \operatorname{ton} /(R 1 \times C 2)
$$

where:
Vramp = amount of ramp needed;
Vsw = switch note voltage;
$\mathrm{V}_{\mathrm{FB}}=$ voltage feedback, 1 V ;
ton $=$ switch on-time.
To minimize the lost in efficiency R1 resistance should be large, typically 100 k or larger. With R1 chosen, C2 can be determined by the following;

$$
\mathrm{C} 2=\left(\mathrm{Vsw}-\mathrm{V}_{\mathrm{FB}}\right) \times \text { ton } /(\mathrm{R} 1 \times \mathrm{Vramp})
$$

C 1 is used as a bypass capacitor and its value should be equal to or greater than C 2 .


Figure 7. Small RC Filter Providing the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

## Maximum Frequency Operation

The minimum pulse width may limit the maximum operating frequency. The duty factor, given by the output/input voltage ratio, multiplied by the period determines the pulse width during normal operation. This pulse width must be greater than 200 ns , or duty cycle jitter could become excessive. For low pulse widths below 300 ns , external slope compensation should be added to the $\mathrm{V}_{\mathrm{FFB}}$ pin to increase the PWM ramp signal and improve stability. 50 mV of added ramp at the $\mathrm{V}_{\mathrm{FFB}}$ pin is typically enough.

## Current Sense Component Selection

The current limit threshold is set by sensing a 60 mV voltage differential between the IS+ and IS- pins. Referring to Figure 8, the time constant of the R2,C1 filter should be set larger than the L/R1 time constant under worst case tolerances, to prevent overshoot in the sensed voltage and tripping the current limit too low. Resistor R3 of value equal to R2 is added for bias current cancellation. R2 and R3 should not be made too large, to reduce errors from bias current offsets. For typical L/R time constants, a $0.1 \mu \mathrm{~F}$ capacitor for C 1 will allow R 2 to be between 1.0 k and $10 \mathrm{k} \Omega$.
The current limit without R4 and R5, which are optional, is given by $60 \mathrm{mV} / \mathrm{R} 1$, where R 1 is the internal resistance of the inductor, obtained from the manufacturer. The addition of R5 can be used to decrease the current limit to a value given by:

$$
\mathrm{I} \text { LIM }=\left(60 \mathrm{mV}-\left(\mathrm{V}_{\text {OUT }} \times \mathrm{R} 3 /(\mathrm{R} 3+\mathrm{R} 5)\right) / R 1\right.
$$

where $\mathrm{V}_{\text {OUT }}$ is the output voltage.
Similiarly, omitting R5 and adding R4 will increase the current limit to a value given by:

$$
\mathrm{I} \mathrm{LIM}=60 \mathrm{mV} / \mathrm{R} 1 \times(1+\mathrm{R} 2 / \mathrm{R} 4)
$$

Essentially, R4 or R5 are used to increase or decrease the inductor voltage drop which corresponds to 60 mV at the IS+ and IS- pins.


Figure 8. Current Limit

## Boost Component Selection for Upper FET Gate Drive

The boost (BST) pin provides for application of a higher voltage to drive the upper FET. This voltage may be provided by a fixed higher voltage or it may be generated with a boost capacitor and charging diode, as shown in Figure 10. The voltage in the boost configuration would be
the summation of the voltage from the charging diode and the output voltage swing. Care must be taken to keep the peak voltage with respect to ground less than 20 V peak. The capacitor should be large enough to drive the capacitance of the top FET.


Figure 9. Additional Application Diagram, 12 V to 5.0 V/8.0 A Converter with Differential Remote Sense


Figure 10. Additional Application Diagram, 12 V to 5.0 V Bias to 3.3 V/8.0 A Converter with Differential Remote Sense

## CS5211

ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping |
| :--- | :---: | :---: | :---: |
| CS5211ED14 | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| CS5211EDR14 |  | SO-14 | 2500 Tape \& Reel |
| CS5211GD14 | $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| CS5211GDR14 |  | SO-14 | 2500 Tape \& Reel |

## NCP1570

## Low Voltage Synchronous Buck Controller

The NCP1570 is a low voltage buck controller. It provides the control for a DC-DC power solution producing an output voltage as low as 0.985 V over a wide current range. The NCP1570-based solution is powered from 12 V with the output derived from a 5 V supply. It contains all required circuitry for a synchronous NFET buck regulator using the $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation. The NCP1570 operates at a fixed internal 200 kHz frequency and is packaged in an SO-8.

The NCP1570 provides undervoltage lockout protection, Soft Start, Power Good with delay, and built-in adaptive non-overlap.

## Features

- $0.985 \mathrm{~V} \pm 1.0 \%$ Reference
- $\mathrm{V}^{2}$ Control Topology
- 200 ns Transient Response
- Programmable Soft Start
- Power Good
- Programmable Power Good Delay
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- 50 ns Adaptive FET Non-Overlap Time
- Fixed 200 kHz Oscillator Frequency
- Undervoltage Lockout
- On/Off Control Through Use of the COMP Pin
- Overvoltage Protection through Synchronous MOSFETs
- Synchronous N-Channel Buck Design
- Dual Supply, 12 V Control, 5 V Power Source


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| NCP1570D | SO-8 | 95 Units/Rail |
| NCP1570DR2 | SO-8 | 2500 Tape \& Reel |

12 V PWRGD VLOGIC

5.0 V

1.2 V

Figure 1. Applications Circuit

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| ESD Susceptibility (Machine Model) |  | 200 | V |
| Lead Temperature Soldering: | Reflow: (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Moisture Sensitivity Level |  | 2 | - |
| ```Package Thermal Resistance, SO-8 Junction-to-Case, R 日Jc Junction-to-Ambient, R ®JA``` |  | $\begin{gathered} 48 \\ 165 \end{gathered}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\mathrm{CC}}$ | 15 V | -0.5 V | N/A | 1.5 A Peak 450 mA DC |
| Compensation Capacitor | COMP | 6.0 V | -0.5 V | 10 mA | 10 mA |
| Voltage Feedback Input | $V_{\text {FB }}$ | 6.0 V | -0.5 V | 1.0 mA | 1.0 mA |
| Power Good Output | PWRGD | 15 V | -0.5 V | 1.0 mA | 20 mA |
| Power Good Delay | PGDELAY | 6.0 V | -0.5 V | 1.0 mA | 10 mA |
| High-Side FET Driver | GATE(H) | 15 V | $\begin{gathered} -0.5 \mathrm{~V} \\ -2.0 \mathrm{~V} \text { for } 50 \mathrm{~ns} \end{gathered}$ | 1.5 A Peak 200 mA DC | 1.5 A Peak 200 mA DC |
| Low-Side FET Driver | GATE(L) | 15 V | $\begin{gathered} -0.5 \mathrm{~V} \\ -2.0 \mathrm{~V} \text { for } 50 \mathrm{~ns} \end{gathered}$ | 1.5 A Peak 200 mA DC | 1.5 A Peak 200 mA DC |
| Ground | GND | 0.5 V | -0.5 V | 1.5 A Peak 450 mA DC | N/A |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, 11.4 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<12.6 \mathrm{~V}, \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}\right.$,
$\mathrm{C}_{\text {PGDELAY }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Error Amplifier

| $V_{\text {FB }}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | $\mathrm{COMP}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=0.8 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\mathrm{COMP}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.2 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Reference Voltage | COMP $=\mathrm{V}_{\mathrm{FB}}$ | 0.975 | 0.985 | 0.995 | V |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=0.8$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.2$ | - | 0.1 | 0.2 | V |
| COMP Fault Discharge Current at UVLO | $\mathrm{COMP}=1.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=6.9 \mathrm{~V}$ | 0.5 | 1.7 | - | mA |
| COMP Fault Discharge Threshold to Reset UVLO | $\begin{aligned} & \mathrm{COMP}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}-6.9 \mathrm{~V}-12 \mathrm{~V} \text {. } \\ & \text { Ramp COMP to } 0.1 \mathrm{~V} \text {. Monitor } \mathrm{I} \text { (COMP) } \end{aligned}$ | 0.1 | 0.25 | 0.3 | V |
| Open Loop Gain | - | - | 98 | - | dB |
| Unity Gain Bandwidth | - | - | 20 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |
| Output Transconductance | - | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |

GATE(H) and GATE(L)

| Rise Time | $1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{L}) \& \operatorname{GATE}(\mathrm{H})<\mathrm{V}_{\mathrm{CC}}-2.0$ | - | 40 | 80 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fall Time | $\mathrm{V}_{\mathrm{CC}}-2.0<\operatorname{GATE}(\mathrm{L}) \&$ GATE(H) < 1.0 V | - | 40 | 80 | ns |
| GATE(H) to GATE(L) Delay | $\operatorname{GATE}(\mathrm{H})<2.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{L})>2.0 \mathrm{~V}$ | 25 | 50 | 75 | ns |
| GATE(L) to GATE(H) Delay | GATE $(\mathrm{L})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{H})>2.0 \mathrm{~V}$ | 25 | 50 | 75 | ns |
| Minimum Pulse Width | $\operatorname{GATE}(\mathrm{X})=4.0 \mathrm{~V}$ | - | 250 | - | ns |
| High Voltage (AC) | $\begin{aligned} & \text { Measure } \operatorname{GATE}(\mathrm{L}) \text { or } \operatorname{GATE}(\mathrm{H}) \\ & 0.5 \mathrm{nF}<\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{~L})}<10 \mathrm{nF} \\ & \text { Note } 2 \end{aligned}$ | $V_{C C}-0.5$ | $\mathrm{V}_{\mathrm{CC}}$ | - | V |
| Low Voltage (AC) | Measure GATE(L) or GATE(H) $0.5 \mathrm{nF}<\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}<10 \mathrm{nF}$ Note 2 | - | 0 | 0.5 | V |
| GATE(H)/(L) Pull-Down | Resistance to GND. Note 2 | 20 | 50 | 115 | k $\Omega$ |

## Power Good

| Lower Threshold, $\mathrm{V}_{\mathrm{O}}$ Rising | - | 0.856 | 0.887 | 0.917 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Lower Threshold, $\mathrm{V}_{\mathrm{O}}$ Falling | - | 0.666 | 0.690 | 0.713 | V |
| PWRGD Low Voltage | $\mathrm{I}_{\mathrm{SINK}}=1.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=0$ | - | 0.15 | 0.4 | V |
| Delay Charge Current | $\mathrm{PGDELAY}=2.0 \mathrm{~V}$ | 7.0 | 12 | 18 | $\mu \mathrm{A}$ |
| Delay Clamp Voltage | - | 3.45 | 4.0 | 4.3 | V |
| Delay Charge Threshold | Ramp PGDELAY, Monitor PWRGD | 3.1 | 3.3 | 3.5 | V |
| Delay Discharge Current at UVLO | PGDELAY $=0.5 \mathrm{~V}, \mathrm{~V}_{C C}=6.9 \mathrm{~V}$ | 0.5 | 2.0 | - | mA |
| Delay Discharge Threshold to Reset UVLO | PGDELAY $=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 6.9 to 12 V , Ramp PGDELAY to 0.1 V , Monitor I (PGDELAY) | 0.1 | 0.25 | 0.3 | V |
| "Good" Signal Delay | With $0.01 \mu \mathrm{~F}$. Note 2 | 1.0 | 3.0 | 5.0 | ms |

2. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, 11.4 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<12.6 \mathrm{~V}, \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}\right.$, $\mathrm{C}_{\text {PGDELAY }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

PWM Comparator

| PWM Comparator Offset | V <br> FB <br> Starts Switching | 0.475 | 0.525 | 0.575 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Ramp Max Duty Cycle | - | - | 80 | - | $\%$ |
| Artificial Ramp | Duty Cycle $=50 \%$ | 18 | 25 | 35 | mV |
| Transient Response | COMP $=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}} 20 \mathrm{mV}$ Overdrive. <br> Note 3 | - | 200 | 300 | ns |
| $\mathrm{~V}_{\mathrm{FB}}$ Input Range | Note 3 | 0 | - | 1.4 | V |

Oscillator

| Switching Frequency | - | 150 | 200 | 250 | kHz |
| :--- | :--- | :--- | :--- | :--- | :--- |

General Electrical Specifications

| $V_{\text {CC }}$ Supply Current | COMP = O V (No Switching) | - | 10 | 15 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Start Threshold | GATE(H) Switching, COMP Charging | 8.0 | 8.5 | 9.0 | V |
| Stop Threshold | GATE(H) Not Switching, COMP Discharging | 7.0 | 7.5 | 8.0 | V |
| Hysteresis | Start - Stop | 0.75 | 1.0 | 1.25 | V |

3. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-8 | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{CC}}$ | Power supply input. |
| 2 | PWRGD | Open collector output goes low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. User must externally limit current into this pin to less than 20 mA . |
| 3 | PGDELAY | External capacitor programs PWRGD low-to-high transition delay. |
| 4 | COMP | Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft Start. Pulling pin $<0.45$ locks gate outputs to a zero percent duty cycle state. |
| 5 | GATE(H) | High-side switch FET driver pin. Capable of delivering peak currents of 1.5 A . |
| 6 | GATE(L) | Low-side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A . |
| 7 | $V_{F B}$ | Error amplifier and PWM comparator input. |
| 8 | GND | Power supply return. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Supply Current vs. Temperature


Figure 5. Reference Voltage vs. Temperature


Figure 4. Oscillator Frequency vs. Temperature


Figure 6. Artificial Ramp Amplitude vs. Temperature (50\% Duty Cycle)


Figure 8. Undervoltage Lockout Thresholds vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 9. $\mathrm{V}_{\mathrm{FB}}$ Bias Current vs. Temperature


Figure 11. COMP Voltages vs. Temperature


Figure 13. GATE Output Rise and Fall Times vs. Temperature


Figure 10. Error Amp Output Currents vs. Temperature


Figure 12. COMP Fault Mode Discharge Current vs. Temperature


Figure 14. GATE Non-Overlap Times vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 15. Power Good Thresholds vs. Temperature


Figure 17. PGOOD Delay Charge Current vs. Temperature


Figure 19. Power Good Discharge Threshold Voltage vs. Temperature


Figure 16. PGOOD Output Low Voltage vs. Temperature


Figure 18. PGDELAY Discharge Current vs. Temperature


Figure 20. PGDELAY Voltages vs. Temperature

## APPLICATION INFORMATION

## THEORY OF OPERATION

The NCP1570 is a simple, synchronous, fixed-frequency, low-voltage buck controller using the $\mathrm{V}^{2}$ control method. It provides a programmable-delay Power Good function to indicate when the output voltage is out of regulation.

## $V^{2}$ Control Method

The $\mathrm{V}^{2}$ control method uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The $\mathrm{V}^{2}$ method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.


Figure 21. $\mathbf{V}^{2}$ Control with Slope Compensation

The $\mathrm{V}^{2}$ control method is illustrated in Figure 21. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction
time to the output load step is not related to the crossover frequency of the error signal loop.
The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at duty cycles above $50 \%$.

## Start Up

The NCP1570 features a programmable Soft Start function, which is implemented through the error amplifier and the external compensation capacitor. This feature prevents stress to the power components and limits output voltage overshoot during start-up. As power is applied to the regulator, the NCP1570 undervoltage lockout circuit (UVL) monitors the IC's supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ). The UVL circuit prevents the MOSFET gates from switching until $\mathrm{V}_{\mathrm{CC}}$ exceeds the 8.5 V threshold. A hysteresis function of 1.0 V improves noise immunity. The compensation capacitor connected to the COMP pin is charged by a $30 \mu \mathrm{~A}$ current source. When the capacitor voltage exceeds the 0.5 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated turning on the upper MOSFET. The current then ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.5 V

PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.


Figure 22. Idealized Waveforms

## Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the $\mathrm{V}^{2}$ control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

## Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading.

## Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

## Overvoltage Protection

Overvoltage protection is provided as a result of the normal operation of the $\mathrm{V}^{2}$ control method and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns , turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

## Power Good

The PWRGD pin is asserted when the output voltage is within regulation limits. Sensing for the PWRGD pin is achieved through the $\mathrm{V}_{\mathrm{FB}}$ pin. When the output voltage is rising, PWRGD goes high at $90 \%$ of the designed output voltage. When the output voltage is falling, PWRGD goes
low at $70 \%$ of the designed output voltage. PWRGD is an open-collector output and should be externally pulled to logic high through a resistor to limit current to no more than 20 mA . Figure 23 shows the hysteretic nature of the PWRGD pin's operation.


Figure 23. PWRGD Assertion

## Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.
In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.
The voltage change during the load current transient is:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I}_{\mathrm{OUT}} \times\left(\frac{\mathrm{ESL}}{\Delta \mathrm{t}}+\mathrm{ESR}+\frac{\mathrm{t} T \mathrm{R}}{\mathrm{COUT}}\right)
$$

where:
$\Delta \mathrm{I}_{\text {OUT }} / \Delta \mathrm{t}=$ load current slew rate;
$\Delta \mathrm{I}_{\text {OUT }}=$ load transient;
$\Delta t=$ load transient duration time;
$\mathrm{ESL}=$ Maximum allowable ESL including capacitors, circuit traces, and vias;
$\mathrm{ESR}=$ Maximum allowable ESR including capacitors and circuit traces;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time.
The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$
\text { ESRMAX }=\frac{\Delta V_{\text {ESR }}}{\Delta \mathrm{I}_{\text {OUT }}}
$$

where:
$\Delta \mathrm{V}_{\mathrm{ESR}}=$ change in output voltage due to ESR (assigned by the designer)
Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where:
$E S R_{C A P}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).
$E S R_{M A X}=$ maximum allowable ESR.
The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$
\Delta \mathrm{V}_{\mathrm{ESR}}=\Delta \mathrm{I} \text { OUT } \times \mathrm{ESR}_{\mathrm{MAX}}
$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$
\text { ESLMAX }=\frac{\Delta V_{E S L} \times \Delta t}{\Delta l}
$$

## Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$
\operatorname{LIN}=\frac{\Delta V}{(\mathrm{dl} / \mathrm{dt}) \mathrm{MAX}}
$$

where:
$\mathrm{L}_{\mathrm{IN}}=$ input inductor value;
$\Delta \mathrm{V}=$ voltage seen by the input inductor during a full load swing;
$(\mathrm{dI} / \mathrm{dt})_{\mathrm{MAX}}=$ maximum allowable input current slew rate.
The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0 , a roll-off rate of $-40 \mathrm{~dB} / \mathrm{dec}$, and a corner frequency:

$$
\mathrm{f}_{\mathrm{C}}=\frac{1}{2 \pi \times \sqrt{\mathrm{LC}}}
$$

where:
$\mathrm{L}=$ input inductor;
$\mathrm{C}=$ input capacitor( s ).

## Selection of the Output Inductor

There are many factors to consider when choosing the output inductor. Maximum load current, core and winding losses, ripple current, short circuit current, saturation characteristics, component height and cost are all variables that the designer should consider. However, the most important consideration may be the effect inductor value has on transient response.
The amount of overshoot or undershoot exhibited during a current transient is defined as the product of the current step and the output filter capacitor ESR. Choosing the inductor value appropriately can minimize the amount of energy that must be transferred from the inductor to the capacitor or vice-versa. In the subsequent paragraphs, we will determine the minimum value of inductance required for our system and consider the trade-off of ripple current vs. transient response.
In order to choose the minimum value of inductance, input voltage, output voltage and output current must be known. Most computer applications use reasonably well regulated bulk power supplies so that, while the equations below specify $\mathrm{V}_{\mathrm{IN}(\mathrm{MAX})}$ or $\mathrm{V}_{\text {IN(MIN) }}$, it is possible to use the nominal value of $\mathrm{V}_{\text {IN }}$ in these calculations with little error.
Current in the inductor while operating in the continuous current mode is defined as the load current plus ripple current.

$$
\mathrm{IL}=\mathrm{ILOAD}+\mathrm{IRIPPLE}
$$

The ripple current waveform is triangular, and the current is a function of voltage across the inductor, switch FET on-time and the inductor value. FET on-time can be defined as the product of duty cycle and switch frequency, and duty cycle can be defined as a ratio of $V_{\text {OUT }}$ to $V_{\text {IN }}$. Thus,

$$
\text { IRIPPLE }=\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(\mathrm{foSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}\right)}
$$

Peak inductor current is defined as the load current plus half of the peak current. Peak current must be less than the maximum rated FET switch current, and must also be less than the inductor saturation current. Thus, the maximum output current can be defined as:
$\operatorname{IOUT}(\mathrm{MAX})=\operatorname{ISWITCH}(\mathrm{MAX})-\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MAX})-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(2)(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}(\mathrm{MAX})\right)}$
Since the maximum output current must be less than the maximum switch current, the minimum inductance required can be determined.

$$
L_{(\text {MIN })}=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(\mathrm{fOSC})\left(\operatorname{ISWITCH}(\mathrm{MAX})\left(\mathrm{V}_{\text {IN }(\text { MIN })}\right)\right.}
$$

This equation identifies the value of inductor that will provide the full rated switch current as inductor ripple current, and will usually result in inefficient system operation. The system will sink current away from the load during some portion of the duty cycle unless load current is greater than half of the rated switch current. Some value larger than the minimum inductance must be used to ensure the converter does not sink current. Choosing larger values of inductor will reduce the ripple current, and inductor value can be designed to accommodate a particular value of ripple current by replacing $\mathrm{I}_{\text {SWITCH(MAX) }}$ with a desired value of IRIPPLE:

$$
\left.\mathrm{L}_{(\text {RIPPLE }}\right)=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\mathrm{OUT}}\right) \mathrm{V}_{\mathrm{OUT}}}{(\mathrm{fOSC})(\mathrm{IRIPPLE})\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})\right)}
$$

However, reducing the ripple current will cause transient response times to increase. The response times for both increasing and decreasing current steps are shown below.

$$
\begin{aligned}
& \text { TRESPONSE(INCREASING) }=\frac{(\mathrm{L})(\Delta \text { IOUT })}{\left(\mathrm{V}_{\text {IN }}-\text { VOUT }\right)} \\
& \text { TRESPONSE(DECREASING })^{(\mathrm{L})\left(\Delta \text { IOUT }^{\prime}\right)} \frac{\left(\mathrm{V}_{\text {OUT }}\right)}{}
\end{aligned}
$$

Inductor value selection also depends on how much output ripple voltage the system can tolerate. Output ripple voltage is defined as the product of the output ripple current and the output filter capacitor ESR.

Thus, output ripple voltage can be calculated as:
$\mathrm{V}_{\text {RIPPLE }}=\left(\mathrm{ESR}_{\mathrm{C}}\right)(\operatorname{IRIPPLE})=\frac{\left(\mathrm{ESR}_{\mathrm{C}}\right)\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}\right)}$
Finally, we should consider power dissipation in the output inductors. Power dissipation is proportional to the square of inductor current:

$$
\mathrm{P}_{\mathrm{D}}=\left(\mathrm{I}_{\mathrm{L}}^{2}\right)\left(\mathrm{ESR}_{\mathrm{L}}\right)
$$

The temperature rise of the inductor relative to the air surrounding it is defined as the product of power dissipation and thermal resistance to ambient:

$$
\Delta \mathrm{T}(\text { inductor })=(\mathrm{Ra})\left(\mathrm{P}_{\mathrm{D}}\right)
$$

Ra for an inductor designed to conduct 20 A to 30 A is approximately $45^{\circ} \mathrm{C} / \mathrm{W}$. The inductor temperature is given as:

$$
\mathrm{T} \text { (inductor) }=\Delta \mathrm{T} \text { (inductor) }+ \text { Tambient }
$$

## $V_{\text {cc }}$ Bypass Filtering

A small RC filter should be added between module $\mathrm{V}_{\mathrm{CC}}$ and the $\mathrm{V}_{\mathrm{CC}}$ input to the IC. A $10 \Omega$ resistor and a $0.1 \mu \mathrm{~F}$ capacitor should be sufficient to ensure the controller IC does not operate erratically due to injected noise.

## Input Filter Capacitors

The input filter capacitors provide a charge reservoir that minimizes supply voltage variations due to changes in current flowing through the switch FETs. These capacitors must be chosen primarily for ripple current rating.


Figure 24.
Consider the schematic shown in Figure 24. The average current flowing in the input inductor $\mathrm{L}_{\mathrm{IN}}$ for any given output current is:

$$
\operatorname{IIN}(\mathrm{AVE})=\operatorname{IOUT} \times \frac{\mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\text {IN }}}
$$

Input capacitor current is positive into the capacitor when the switch FETs are off, and negative out of the capacitor when the switch FETs are on. When the switches are off, $\mathrm{I}_{\text {IN(AVE) }}$ flows into the capacitor. When the switches are on, capacitor current is equal to the per-phase output current minus $\mathrm{I}_{\mathrm{IN}(\mathrm{AVE})}$. If we ignore the small current variation due to the output ripple current, we can approximate the input capacitor current waveform as a square wave. We can then calculate the RMS input capacitor ripple current:
$\operatorname{IRMS}($ CIN $)=\sqrt{\begin{array}{l}I_{\text {IN(AVE) }}^{2}+\frac{V_{\text {OUT }}}{V_{\text {IN }}} \\ \times\left[(\operatorname{IOUT} \text { per phase }-\operatorname{IIN(AVE)})^{2}-I_{\text {IN(AVE }}^{2}\right]\end{array}}$
The input capacitance must be designed to conduct the worst case input ripple current. This will require several capacitors in parallel. In addition to the worst case current, attention must be paid to the capacitor manufacturer's derating for operation over temperature.

As an example, let us define the input capacitance for a 5 V to 3.3 V conversion at 10 A at an ambient temperature of $60^{\circ} \mathrm{C}$. A droop voltage of 90 mV to 1.61 V and efficiency of $80 \%$ is assumed. Average input current in the input filter inductor is:

$$
\operatorname{IIN}(A V E)=(10 \mathrm{~A})(3.3 \mathrm{~V} / 5 \mathrm{~V})=6.6 \mathrm{~A}
$$

Input capacitor RMS ripple current is then

$$
\begin{aligned}
\operatorname{IIN}(\mathrm{RMS}) & =\sqrt{\begin{array}{l}
6.6^{2}+\frac{3.3 \mathrm{~V}}{5 \mathrm{~V}} \\
\times\left[(10 \mathrm{~A}-6.6 \mathrm{~A})^{2}-6.6 \mathrm{~A}^{2}\right]
\end{array}} \\
& =4.74 \mathrm{~A}
\end{aligned}
$$

If we consider a Rubycon MBZ series capacitor, the ripple current rating for a $6.3 \mathrm{~V}, 1800 \mathrm{nF}$ capacitor is 2000 mA at 100 kHz and $105^{\circ} \mathrm{C}$. We determine the number of input capacitors by dividing the ripple current by the per-capacitor current rating:

$$
\text { Number of capacitors }=4.74 \mathrm{~A} / 2.0 \mathrm{~A}=2.3
$$

A total of at least 3 capacitors in parallel must be used to meet the input capacitor ripple current requirements.

## Output Switch FETs

Output switch FETs must be chosen carefully, since their properties vary widely from manufacturer to manufacturer. The NCP1570 system is designed assuming that n -channel FETs will be used. The FET characteristics of most concern are the gate charge/gate-source threshold voltage, gate capacitance, on-resistance, current rating and the thermal capability of the package.

The onboard FET driver has a limited drive capability. If the switch FET has a high gate charge, the amount of time the FET stays in its ohmic region during the turn-on and turn-off transitions is larger than that of a low gate charge FET, with the result that the high gate charge FET will consume more power. Similarly, a low on-resistance FET will dissipate less power than will a higher on-resistance FET at a given current. Thus, low gate charge and low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ will result in higher efficiency and will reduce generated heat.

It can be advantageous to use multiple switch FETs to reduce power consumption. By placing a number of FETs in parallel, the effective $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ is reduced, thus reducing the ohmic power loss. However, placing FETs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel FET reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so. However, at some point the law of diminishing returns will take hold, and a marginal increase in efficiency may not be worth the board area required to add the extra FET. Additionally, as more FETs are used, the limited drive capability of the FET driver will have to charge a larger gate capacitance, resulting in increased gate voltage rise and fall times. This will affect the amount of time the FET operates in its ohmic region and will increase power dissipation.

The following equations can be used to calculate power dissipation in the switch FETs.

For ohmic power losses due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ :

$$
\begin{gathered}
\mathrm{PON}(\mathrm{TOP})=\frac{\left(\mathrm{RDS}(\mathrm{ON})(\mathrm{TOP})(\mathrm{I} \mathrm{RMS}(\mathrm{TOP}))^{2}\right.}{(\text { number of topside FETs })} \\
\mathrm{PON}(\mathrm{BOTTOM})=\frac{\left(\mathrm{RDS}(\mathrm{ON})(\mathrm{BOTTOM})(\mathrm{I} M \mathrm{RM}(\mathrm{BOTTOM}))^{2}\right.}{(\text { number of bottom }- \text { side FETs })}
\end{gathered}
$$

where:
$\mathrm{n}=$ number of phases.
Note that $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ increases with temperature. It is good practice to use the value of $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ at the FET's maximum junction temperature in the calculations shown above.

$$
\begin{aligned}
& I_{R M S}(T O P)=\sqrt{I_{P K}^{2}-\left(I_{P K}\right)\left(I_{\text {RIPPLE }}\right)+\frac{D}{3} I_{\text {RIPPLE }}^{2}} \\
& \operatorname{IRMS}(\text { BOTTOM })=I_{\text {PK }}^{2}-(\text { IPKIRIPPLE })+\frac{(1-D)}{3} I_{\text {RIPPLE }}^{2} \\
& \text { IRIPPLE }=\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right)\left(\mathrm{V}_{\mathrm{OUT}}\right)}{(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\mathrm{IN}}\right)}
\end{aligned}
$$

$$
\text { IPEAK }=\text { ILOAD }+\frac{\text { IRIPPLE }}{2}=\frac{\text { IOUT }}{3}+\frac{\text { IRIPPLE }}{2}
$$

where:
D = Duty cycle.
For switching power losses:

$$
\mathrm{PD}=\mathrm{nCV}{ }^{2}(\mathrm{fOSC})
$$

where:
$\mathrm{n}=$ number of switch FETs (either top or bottom),
$\mathrm{C}=\mathrm{FET}$ gate capacitance,
$\mathrm{V}=$ maximum gate drive voltage (usually $\mathrm{V}_{\mathrm{CC}}$ ),
$\mathrm{f}_{\mathrm{OSC}}=$ switching frequency.

## Layout Considerations

1. The fast response time of $\mathrm{V}^{2}$ technology increases the IC's sensitivity to noise on the $\mathrm{V}_{\mathrm{FB}}$ line. Fortunately, a simple RC filter, formed by the feedback network and a small capacitor $(100 \mathrm{pF}$ works well, shown below as C6) placed between $\mathrm{V}_{\mathrm{FB}}$ and GND, filters out most noise and provides a system practically immune to jitter. This capacitor should be located as close as possible to the IC.
2. The COMP capacitor (shown below as C13) should be connected via its own path to the IC ground. The COMP capacitor is sensitive to the intermittent ground drops caused by switching currents. A separate ground path will reduce the potential for jitter.
3. The $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor $(0.1 \mu \mathrm{~F}$ or greater, shown below as C 4 ) should be located as close as possible to the IC. This capacitor's connection to GND must be as short as possible. The $10 \Omega$ resistor (shown below as R3) should be placed close to the $\mathrm{V}_{\mathrm{CC}}$ pin.
4. The IC should not be placed in the path of switching currents. If a ground plane is used, care should be taken by the designer to ensure that the IC is not located over a ground or other current return path.


Figure 25.

## NCP1571

## Low Voltage Synchronous Buck Controller

The NCP1571 is a low voltage buck controller. It provides the control for a DC-DC power solution producing an output voltage as low as 0.980 V over a wide current range. The NCP1571-based solution is powered from 12 V with the output derived from a $2-7 \mathrm{~V}$ supply. It contains all required circuitry for a synchronous NFET buck regulator using the $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation. NCP1571 operates at a fixed internal 200 kHz frequency and is packaged in an SO-8.

This device provides undervoltage lockout protection, Soft Start, Power Good with delay, and built-in adaptive non-overlap. During undervoltage lockout, the NCP1571 controller allows the power supply output to drift down, allowing the load time to shut off. This operation distinguishes the NCP1571 from other parts in its family.

## Features

- $0.980 \mathrm{~V} \pm 1.0 \%$ Reference Voltage
- $\mathrm{V}^{2}$ Control Topology
- 200 ns Transient Response
- Programmable Soft Start
- Power Good
- Programmable Power Good Delay
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- Adaptive FET Non-Overlap Time
- Fixed 200 kHz Oscillator Frequency
- Undervoltage Lockout Holds Both Gate Outputs Low
- On/Off Control Through Use of the COMP Pin
- Overvoltage Protection through Synchronous MOSFETs
- Synchronous N-Channel Buck Design
- Dual Supply, 12 V Control, 2-7 V Power Source

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAM


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| NCP1571D | SO-8 | 95 Units/Rail |
| NCP1571DR2 | SO-8 | 2500 Tape \& Reel |



Figure 1．Applications Circuit
MAXIMUM RATINGS＊

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | －65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility（Human Body Model） |  | 2.0 | kV |
| Lead Temperature Soldering： | Reflow：（Note 1） | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Moisture Sensitivity Level |  | 1 | － |
| ```Package Thermal Resistance, SO-8 Junction-to-Case, R⿴囗⿱一𫝀口C Junction-to-Ambient, R``` |  | $\begin{gathered} 48 \\ 165 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |

1． 60 second maximum above $183^{\circ} \mathrm{C}$ ．
＊The maximum package power dissipation must be observed．

## MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{C C}$ | 15 V | －0．5 V | N／A | 1．5 A Peak 450 mA DC |
| Compensation Capacitor | COMP | 6.0 V | －0．5 V | 10 mA | 10 mA |
| Voltage Feedback Input | $V_{F B}$ | 6.0 V | －0．5 V | 1.0 mA | 1.0 mA |
| Power Good Output | PWRGD | 15 V | －0．5 V | 1.0 mA | 20 mA |
| Power Good Delay | PGDELAY | 6.0 V | －0．5 V | 1.0 mA | 10 mA |
| High－Side FET Driver | GATE（H） | 15 V | $\begin{gathered} -0.5 \mathrm{~V} \\ -2.0 \mathrm{~V} \text { for } 50 \mathrm{~ns} \end{gathered}$ | 1．5 A Peak 200 mA DC | 1．5 A Peak 200 mA DC |
| Low－Side FET Driver | GATE（L） | 15 V | $\begin{gathered} -0.5 \mathrm{~V} \\ -2.0 \mathrm{~V} \text { for } 50 \mathrm{~ns} \end{gathered}$ | 1．5 A Peak 200 mA DC | 1．5 A Peak 200 mA DC |
| Ground | GND | 0.5 V | －0．5 V | 1．5 A Peak 450 mA DC | N／A |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, 11.4 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<12.6 \mathrm{~V}, \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}\right.$,
$\mathrm{C}_{\text {PGDELAY }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Error Amplifier |  |  |  |  |  |
| $V_{\text {FB }}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| COMP Source Current | $\mathrm{COMP}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=0.8 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\mathrm{COMP}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.2 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Reference Voltage | $\begin{aligned} & \mathrm{COMP}=\mathrm{V}_{\mathrm{FB}} \\ & \mathrm{~T}_{\mathrm{J}}<25^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & 0.970 \\ & 0.965 \end{aligned}$ | $\begin{aligned} & 0.980 \\ & 0.980 \end{aligned}$ | $\begin{aligned} & 0.990 \\ & 0.995 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=0.8$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.2$ | - | 0.1 | 0.2 | V |
| COMP Fault Discharge Current at UVLO | $\mathrm{COMP}=1.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=6.9 \mathrm{~V}$ | 0.5 | 1.7 | - | mA |
| COMP Fault Discharge Threshold to Reset UVLO | $\begin{aligned} & \mathrm{COMP}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}-6.9 \mathrm{~V}-12 \mathrm{~V} \text {. } \\ & \text { Ramp COMP to } 0.1 \mathrm{~V} \text {. Monitor } \mathrm{I} \text { (COMP) } \end{aligned}$ | 0.1 | 0.25 | 0.3 | V |
| Open Loop Gain | - | - | 98 | - | dB |
| Unity Gain Bandwidth | - | - | 20 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |
| Output Transconductance | - | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |

GATE(H) and GATE(L)

| Rise Time | $1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{L}) \& \operatorname{GATE}(\mathrm{H})<\mathrm{V}_{\mathrm{CC}}-2.0$ | - | 40 | 80 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Fall Time | $\mathrm{V}_{\mathrm{CC}}-2.0<\operatorname{GATE}(\mathrm{L}) \&$ GATE $(\mathrm{H})<1.0 \mathrm{~V}$ | - | 40 | 80 | ns |
| GATE(H) to GATE(L) Delay | GATE $(\mathrm{H})<2.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{L})>2.0 \mathrm{~V}$ | 40 | 60 | 100 | ns |
| GATE(L) to GATE(H) Delay | GATE $(\mathrm{L})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{H})>2.0 \mathrm{~V}$ | 40 | 60 | 100 | ns |
| Minimum Pulse Width | $\operatorname{GATE}(\mathrm{X})=4.0 \mathrm{~V}$ | - | 250 | - | ns |
| High Voltage (AC) | Measure GATE(L) or GATE(H) $0.5 \mathrm{nF}<\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}<10 \mathrm{nF}$ Note 2. | $V_{C C}-0.5$ | $\mathrm{V}_{\mathrm{CC}}$ | - | V |
| Low Voltage (AC) | $\begin{aligned} & \text { Measure } \operatorname{GATE}(\mathrm{L}) \text { or } \operatorname{GATE}(\mathrm{H}) \\ & 0.5 \mathrm{nF}<\mathrm{C}_{\operatorname{GATE}(H)}=\mathrm{C}_{\operatorname{GATE}(\mathrm{L})}<10 \mathrm{nF} \\ & \text { Note } 2 \text {. } \end{aligned}$ | - | 0 | 0.5 | V |
| GATE(H)/(L) Pull-Down | Resistance to GND. Note 2. | 20 | 50 | 115 | k $\Omega$ |

Power Good

| Lower Threshold, $\mathrm{V}_{\mathrm{O}}$ Rising |  | 0.852 | 0.882 | 0.912 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | $\mathrm{~T}_{J}<25^{\circ} \mathrm{C}$ | 0.847 | 0.882 | 0.917 | V |
| Lower Threshold, $\mathrm{V}_{\mathrm{O}}$ Falling |  | 0.663 | 0.685 | 0.709 | V |
|  | $\mathrm{~T}_{J}<25^{\circ} \mathrm{C}$ | 0.658 | 0.685 | 0.714 | V |
| PWRGD Low Voltage | $\mathrm{I}_{\mathrm{SINK}}=1.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=0$ | - | 0.15 | 0.4 | V |
| Delay Charge Current | PGDELAY $=2.0 \mathrm{~V}$ | 7.0 | 12 | 18 | $\mu \mathrm{~A}$ |
| Delay Clamp Voltage |  | - | 3.45 | 4.0 | 4.3 |
| Delay Charge Threshold | Ramp PGDELAY, Monitor PWRGD | 3.1 | 3.3 | 3.5 | V |
| Delay Discharge Current at UVLO | PGDELAY $=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=6.9 \mathrm{~V}$ | 0.5 | 2.0 | - | mA |

2. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, 11.4 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<12.6 \mathrm{~V}, \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}\right.$, $\mathrm{C}_{\text {PGDELAY }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | | Power Good |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: |
| Delay Discharge Threshold to Reset <br> UVLO | PGDELAY $=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 6.9 to 12 V, <br> Ramp PGDELAY to 0.1 V, Monitor I <br> (PGDELAY) | 0.1 | 0.25 | 0.3 |
| "Good" Signal Delay | With $0.01 \mu$ F. Note 3. | 1.0 | 3.0 | 5.0 |

PWM Comparator

| PWM Comparator Offset | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$, Increase COMP Until GATE(H) <br> Starts Switching | 0.475 | 0.525 | 0.575 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Ramp Max Duty Cycle | - | - | 80 | - | $\%$ |
| Artificial Ramp | Duty Cycle $=50 \%$ | 18 | 25 | 35 | mV |
| Transient Response | COMP $=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}} 20 \mathrm{mV}$ Overdrive. <br> Note 3 | - | 200 | 300 | ns |
| $\mathrm{~V}_{\mathrm{FB}}$ Input Range | Note 3 | 0 | - | 1.4 | V |

## Oscillator

| Switching Frequency | - | 150 | 200 | 250 | kHz |
| :--- | :--- | :--- | :--- | :--- | :--- |

## General Electrical Specifications

| $V_{\text {CC }}$ Supply Current | COMP $=0$ V (No Switching) | - | 10 | 15 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Start Threshold | GATE(H) Switching, COMP Charging | 8.0 | 8.5 | 9.0 | V |
| Stop Threshold | GATE(H) Not Switching, COMP Discharging | 7.0 | 7.5 | 8.0 | V |
| Hysteresis | Start - Stop | 0.75 | 1.0 | 1.25 | V |

3. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-8 | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\text {CC }}$ | Power supply input. |
| 2 | PWRGD | Open collector output goes low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. User must externally limit current into this pin to less than 20 mA . |
| 3 | PGDELAY | External capacitor programs PWRGD low-to-high transition delay. |
| 4 | COMP | Error amp output. PWM comparator reference input. A capacitor to LGND provides error amp compensation and Soft Start. Pulling pin $<0.475 \mathrm{~V}$ locks gate outputs to a zero percent duty cycle state. |
| 5 | GATE(H) | High-side switch FET driver pin. Capable of delivering peak currents of 1.5 A . |
| 6 | GATE(L) | Low-side synchronous FET driver pin. Capable of delivering peak currents of 1.5 A . |
| 7 | $V_{\text {FB }}$ | Error amplifier and PWM comparator input. |
| 8 | GND | Power supply return. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Supply Current vs. Temperature


Figure 5. Reference Voltage vs. Temperature


Figure 4. Oscillator Frequency vs. Temperature


Figure 6. Artificial Ramp Amplitude vs. Temperature (50\% Duty Cycle)


Figure 8. Undervoltage Lockout Thresholds vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 9. $\mathrm{V}_{\mathrm{FB}}$ Bias Current vs. Temperature


Figure 11. COMP Voltages vs. Temperature


Figure 13. GATE Output Rise and Fall Times vs. Temperature


Figure 10. Error Amp Output Currents vs. Temperature


Figure 12. COMP Fault Mode Discharge Current vs. Temperature


Figure 14. GATE Non-Overlap Times vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 15. PWRGD Thresholds vs. Temperature


Figure 17. PGDELAY Charge Current vs. Temperature


Figure 19. PGDELAY Discharge Threshold Voltage vs. Temperature


Figure 16. PWRGD Output Low Voltage vs. Temperature


Figure 18. PGDELAY Discharge Current vs. Temperature


Figure 20. PGDELAY Voltages vs. Temperature

## APPLICATION INFORMATION

## THEORY OF OPERATION

The NCP1571 is a simple, synchronous, fixed-frequency, low-voltage buck controller using the $\mathrm{V}^{2}$ control method. It provides a programmable-delay Power Good function to indicate when the output voltage is out of regulation.

## $V^{2}$ Control Method

The $\mathrm{V}^{2}$ control method uses a ramp signal generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The $\mathrm{V}^{2}$ method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.


Figure 21. ${ }^{2}$ Control with Slope Compensation

The $\mathrm{V}^{2}$ control method is illustrated in Figure 21. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction
time to the output load step is not related to the crossover frequency of the error signal loop.
The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.
The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity, particularly at duty cycles above $50 \%$.

## Start Up

The NCP1571 features a programmable Soft Start function, which is implemented through the error amplifier and the external compensation capacitor. This feature prevents stress to the power components and limits output voltage overshoot during start-up. As power is applied to the regulator, the NCP1571 undervoltage lockout circuit (UVL) monitors the IC's supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ). The UVL circuit holds both gate outputs low until $\mathrm{V}_{\mathrm{CC}}$ exceeds the 8.5 V threshold. A hysteresis function of 1.0 V improves noise immunity. The compensation capacitor connected to the COMP pin is charged by a $30 \mu \mathrm{~A}$ current source. When the capacitor voltage exceeds the 0.5 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE(H) is activated, turning on the upper MOSFET. The current ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.5 V PWM comparator offset
threshold and the artificial ramp, the PWM comparator terminates the initial pulse.


Figure 22. Idealized Waveforms

## Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the $\mathrm{V}^{2}$ control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

## Input Supplies

The NCP1571 can be used in applications where a 12 V supply is available along with a lower voltage supply. Often the lower voltage supply is 5 V , but it can be any voltage less than the 12 V supply minus the required gate drive voltage of the top MOSFET. The greater the difference between the two voltages, the better the efficiency due to increasing $\mathrm{V}_{\mathrm{GS}}$ available to turn on the upper MOSFET. In order to maintain power supply stability, the lower supply voltage should be at least 1.5 times the desired voltage.

A lower supply voltage between $2-7 \mathrm{~V}$ is recommended.

## Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading.

## Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

## Overvoltage Protection

Overvoltage protection is provided as a result of the normal operation of the $\mathrm{V}^{2}$ control method and requires no additional external components. The control loop responds
to an overvoltage condition within 200 ns , turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage, preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

## Power Good

The PWRGD pin is asserted when the output voltage is within regulation limits. Sensing for the PWRGD pin is achieved through the $\mathrm{V}_{\mathrm{FB}}$ pin. When the output voltage is rising, PWRGD goes high at $90 \%$ of the designed output voltage. When the output voltage is falling, PWRGD goes low at $70 \%$ of the designed output voltage. PWRGD is an open-collector output and should be externally pulled to logic high through a resistor to limit current to no more than 20 mA . Figure 23 shows the hysteretic nature of the PWRGD pin's operation.


Figure 23. PWRGD Assertion

## Shutdown

When the input voltage connected to $\mathrm{V}_{\mathrm{CC}}$ falls through the lower threshold of the UVLO comparator, a fault latch is set. The fault latch provides a signal that forces both GATE(H) and GATE(L) into their logic low state, producing a high-impedance output at the converter switch node. At the same time, the latch also turns on two transistors which pull down on the COMP and PGDELAY pins, quickly discharging their external capacitors, and allowing PWRGD to fall.

## CONVERTER DESIGN

## Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.
In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the
output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I} \mathrm{OUT} \times\left(\frac{\mathrm{ESL}}{\Delta \mathrm{t}}+\mathrm{ESR}+\frac{\mathrm{t} \mathrm{TR}}{\mathrm{COUT}}\right)
$$

where:
$\Delta \mathrm{I}_{\text {OUT }} / \Delta \mathrm{t}=$ load current slew rate;
$\Delta \mathrm{I}_{\text {OUT }}=$ load transient;
$\Delta t=$ load transient duration time;
ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;
ESR $=$ Maximum allowable ESR including capacitors and circuit traces;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time.
The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESR}}}{\Delta \mathrm{I}_{\mathrm{OUT}}}
$$

where:
$\Delta \mathrm{V}_{\mathrm{ESR}}=$ change in output voltage due to ESR (assigned by the designer)
Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where:
$E S R_{C A P}=$ maximum $E S R$ per capacitor (specified in manufacturer's data sheet).
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR.
The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$
\Delta \mathrm{V}_{\mathrm{ESR}}=\Delta \mathrm{I}_{\mathrm{OUT}} \times \mathrm{ESR}_{\mathrm{MAX}}
$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$
\mathrm{ESL}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESL}} \times \Delta \mathrm{t}}{\Delta \mathrm{l}}
$$

## Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up.

The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$
\mathrm{L}_{\mathrm{IN}}=\frac{\Delta \mathrm{V}}{(\mathrm{dl} / \mathrm{dt}) \mathrm{MAX}}
$$

where:
$\mathrm{L}_{\mathrm{IN}}=$ input inductor value;
$\Delta \mathrm{V}=$ voltage seen by the input inductor during a full load swing;
$(\mathrm{dI} / \mathrm{dt})_{\mathrm{MAX}}=$ maximum allowable input current slew rate.
The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0 , a roll-off rate of $-40 \mathrm{~dB} / \mathrm{dec}$, and a corner frequency:

$$
\mathrm{f}_{\mathrm{C}}=\frac{1}{2 \pi \times \sqrt{\mathrm{LC}}}
$$

where:
$\mathrm{L}=$ input inductor;
$\mathrm{C}=$ input capacitor(s).

## Selection of the Output Inductor

There are many factors to consider when choosing the output inductor. Maximum load current, core and winding losses, ripple current, short circuit current, saturation characteristics, component height and cost are all variables that the designer should consider. However, the most important consideration may be the effect inductor value has on transient response.

The amount of overshoot or undershoot exhibited during a current transient is defined as the product of the current step and the output filter capacitor ESR. Choosing the inductor value appropriately can minimize the amount of energy that must be transferred from the inductor to the capacitor or vice-versa. In the subsequent paragraphs, we will determine the minimum value of inductance required for our system and consider the trade-off of ripple current vs. transient response.

In order to choose the minimum value of inductance, input voltage, output voltage and output current must be known. Most computer applications use reasonably well regulated bulk power supplies so that, while the equations below specify $\mathrm{V}_{\text {IN(MAX) }}$ or $\mathrm{V}_{\mathrm{IN}(\mathrm{MIN})}$, it is possible to use the nominal value of $\mathrm{V}_{\text {IN }}$ in these calculations with little error.

Current in the inductor while operating in the continuous current mode is defined as the load current plus ripple current.

$$
\mathrm{IL}=\mathrm{I} \mathrm{LOAD}+\mathrm{I} \text { RIPPLE }
$$

The ripple current waveform is triangular, and the current is a function of voltage across the inductor, switch FET on-time and the inductor value. FET on-time can be defined as the product of duty cycle and switch frequency, and duty cycle can be defined as a ratio of $\mathrm{V}_{\text {OUT }}$ to $\mathrm{V}_{\text {IN }}$. Thus,

$$
\text { IRIPPLE }=\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}\right)}
$$

Peak inductor current is defined as the load current plus half of the peak current. Peak current must be less than the maximum rated FET switch current, and must also be less than the inductor saturation current. Thus, the maximum output current can be defined as:
$\operatorname{IOUT}(\mathrm{MAX})=\operatorname{ISWITCH}(\mathrm{MAX})-\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MAX})-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(2)(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}(\mathrm{MAX})\right)}$
Since the maximum output current must be less than the maximum switch current, the minimum inductance required can be determined.

$$
L_{(M I N)}=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\mathrm{OUT}}\right) \mathrm{V}_{\mathrm{OUT}}}{(\mathrm{fOSC})(\operatorname{ISWITCH}(\mathrm{MAX}))\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})\right)}
$$

This equation identifies the value of inductor that will provide the full rated switch current as inductor ripple current, and will usually result in inefficient system operation. The system will sink current away from the load during some portion of the duty cycle unless load current is greater than half of the rated switch current. Some value larger than the minimum inductance must be used to ensure the converter does not sink current. Choosing larger values of inductor will reduce the ripple current, and inductor value can be designed to accommodate a particular value of ripple current by replacing $\mathrm{I}_{\text {SWITCH(MAX) }}$ with a desired value of I $_{\text {RIPPLE }}:$

$$
L_{(\text {RIPPLE })}=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(\mathrm{fOSC})(\operatorname{IRIPPLE})\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})\right)}
$$

However, reducing the ripple current will cause transient response times to increase. The response times for both increasing and decreasing current steps are shown below.

$$
\begin{aligned}
& \text { TRESPONSE(INCREASING) }=\frac{(\mathrm{L})(\Delta \text { IOUT })}{\left(\mathrm{V}_{\text {IN }}-\text { VOUT }^{\prime}\right)} \\
& \text { TRESPONSE(DECREASING })=\frac{(\mathrm{L})(\text { (IIOUT })}{\left(\text { VOUT }^{\prime}\right)}
\end{aligned}
$$

Inductor value selection also depends on how much output ripple voltage the system can tolerate. Output ripple voltage is defined as the product of the output ripple current and the output filter capacitor ESR.

Thus, output ripple voltage can be calculated as:
$\mathrm{V}_{\text {RIPPLE }}=($ ESRC $)(\operatorname{IRIPPLE})=\frac{\left(E_{R} C\right)\left(V_{\text {IN }}-V_{\text {OUT }}\right) V_{\text {OUT }}}{(\mathrm{fOSC})(L)\left(\mathrm{V}_{\text {IN }}\right)}$

Finally, we should consider power dissipation in the output inductors. Power dissipation is proportional to the square of inductor current:

$$
P_{D}=\left(I_{L}^{2}\right)\left(E S R_{L}\right)
$$

The temperature rise of the inductor relative to the air surrounding it is defined as the product of power dissipation and thermal resistance to ambient:

$$
\Delta \mathrm{T}(\text { inductor })=(\mathrm{Ra})\left(\mathrm{P}_{\mathrm{D}}\right)
$$

Ra for an inductor designed to conduct 20 A to 30 A is approximately $45^{\circ} \mathrm{C} / \mathrm{W}$. The inductor temperature is given as:

$$
\mathrm{T} \text { (inductor) }=\Delta \mathrm{T} \text { (inductor) }+ \text { Tambient }
$$

## $\mathrm{V}_{\mathrm{Cc}}$ Bypass Filtering

A small RC filter should be added between module $\mathrm{V}_{\mathrm{CC}}$ and the $\mathrm{V}_{\mathrm{CC}}$ input to the IC. A $10 \Omega$ resistor and a $0.47 \mu \mathrm{~F}$ capacitor should be sufficient to ensure the controller IC does not operate erratically due to injected noise, and will also supply reserve charge for the onboard gate drivers.

## Input Filter Capacitors

The input filter capacitors provide a charge reservoir that minimizes supply voltage variations due to changes in current flowing through the switch FETs. These capacitors must be chosen primarily for ripple current rating.


Figure 24.
Consider the schematic shown in Figure 24. The average current flowing in the input inductor $\mathrm{L}_{\mathrm{IN}}$ for any given output current is:

$$
\operatorname{IIN}(A V E)=\operatorname{IOUT} \times \frac{V_{\text {OUT }}}{V_{\text {IN }}}
$$

Input capacitor current is positive into the capacitor when the switch FETs are off, and negative out of the capacitor when the switch FETs are on. When the switches are off, $\mathrm{I}_{\text {IN(AVE) }}$ flows into the capacitor. When the switches are on, capacitor current is equal to the per-phase output current minus $\mathrm{I}_{\mathrm{IN}(\mathrm{AVE}) \text {. }}$ If we ignore the small current variation due to the output ripple current, we can approximate the input capacitor current waveform as a square wave. We can then calculate the RMS input capacitor ripple current:
$I_{\text {RMS }(C I N)}=\sqrt{\begin{array}{l}I_{\text {INAVE }}^{2}+\frac{V_{\text {OUT }}}{V_{\text {II }}} \\ \left.\times[\text { IOUT per phase }-\operatorname{IIN(AVE)})^{2}-I_{\operatorname{INAVE})}^{2}\right]\end{array}}$
The input capacitance must be designed to conduct the worst case input ripple current. This will require several capacitors in parallel. In addition to the worst case current, attention must be paid to the capacitor manufacturer's derating for operation over temperature.

As an example, let us define the input capacitance for a 5 V to 3.3 V conversion at 10 A at an ambient temperature of $60^{\circ} \mathrm{C}$. Efficiency of $80 \%$ is assumed. Average input current in the input filter inductor is:

$$
\operatorname{IIN}(\mathrm{AVE})=(10 \mathrm{~A})(3.3 \mathrm{~V} / 5 \mathrm{~V})=6.6 \mathrm{~A}
$$

Input capacitor RMS ripple current is then

$$
\begin{aligned}
\operatorname{IIN}(\mathrm{RMS}) & =\sqrt{\begin{array}{l}
6.6^{2}+\frac{3.3 \mathrm{~V}}{5 \mathrm{~V}} \\
\times\left[(10 \mathrm{~A}-6.6 \mathrm{~A})^{2}-6.6 \mathrm{~A}^{2}\right]
\end{array}} \\
& =4.74 \mathrm{~A}
\end{aligned}
$$

If we consider a Rubycon MBZ series capacitor, the ripple current rating for a $6.3 \mathrm{~V}, 1800 \mathrm{nF}$ capacitor is 2000 mA at 100 kHz and $105^{\circ} \mathrm{C}$. We determine the number of input capacitors by dividing the ripple current by the per-capacitor current rating:

Number of capacitors $=4.74 \mathrm{~A} / 2.0 \mathrm{~A}=2.3$
A total of at least 3 capacitors in parallel must be used to meet the input capacitor ripple current requirements.

## Output Switch FETs

Output switch FETs must be chosen carefully, since their properties vary widely from manufacturer to manufacturer. The NCP1571 system is designed assuming that n -channel FETs will be used. The FET characteristics of most concern are the gate charge/gate-source threshold voltage, gate capacitance, on-resistance, current rating and the thermal capability of the package.

The onboard FET driver has a limited drive capability. If the switch FET has a high gate charge, the amount of time the FET stays in its ohmic region during the turn-on and turn-off transitions is larger than that of a low gate charge FET, with the result that the high gate charge FET will consume more power. Similarly, a low on-resistance FET will dissipate less power than will a higher on-resistance FET at a given current. Thus, low gate charge and low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ will result in higher efficiency and will reduce generated heat.

It can be advantageous to use multiple switch FETs to reduce power consumption. By placing a number of FETs in parallel, the effective $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ is reduced, thus reducing the ohmic power loss. However, placing FETs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel FET reduces the ohmic power loss more than the switching losses increase,
there is some advantage to doing so. However, at some point the law of diminishing returns will take hold, and a marginal increase in efficiency may not be worth the board area required to add the extra FET. Additionally, as more FETs are used, the limited drive capability of the FET driver will have to charge a larger gate capacitance, resulting in increased gate voltage rise and fall times. This will affect the amount of time the FET operates in its ohmic region and will increase power dissipation.
The following equations can be used to calculate power dissipation in the switch FETs.
For ohmic power losses due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ :

$$
\begin{gathered}
\mathrm{PON}(\mathrm{TOP})=\frac{\left(\mathrm{RDS}(\mathrm{ON})(\mathrm{TOP})(\mathrm{IRMS}(\mathrm{TOP}))^{2}\right.}{(\text { number of topside FETs })} \\
\mathrm{PON}(\mathrm{BOTTOM})=\frac{\left(\mathrm{RDS}(\mathrm{ON})(\text { BOTTOM })(\text { (RMS }(\mathrm{BOTTOM}))^{2}\right.}{(\text { number of bottom-side FETs })}
\end{gathered}
$$

where:
$\mathrm{n}=$ number of phases.
Note that $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ increases with temperature. It is good practice to use the value of $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ at the FET's maximum junction temperature in the calculations shown above.

$$
\begin{aligned}
& I_{R M S}(T O P)=\sqrt{I_{\text {PK }}^{2}-(I P K)\left(I_{\text {RIPPLE }}\right)+\frac{D}{3} I_{\text {RIPPLE }}^{2}} \\
& \operatorname{IRMS}(\text { BOTTOM })=I_{\text {PK }}^{2}-(\text { IPKIRIPPLE })+\frac{(1-\mathrm{D})}{3} I_{\text {RIPPLE }}^{2} \\
& { }_{\text {IRIPPLE }}=\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right)\left(\mathrm{V}_{\text {OUT }}\right)}{(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}\right)} \\
& I_{\text {IPEAK }}=\text { ILOAD }^{\text {I }} \frac{\text { IRIPPLE }}{2}=\frac{\text { IOUT }}{3}+\frac{\text { IRIPPLE }}{2}
\end{aligned}
$$

where:
D = Duty cycle.
For switching power losses:

$$
\mathrm{P}_{\mathrm{D}}=\mathrm{nCV}{ }^{2}(\mathrm{fOSC})
$$

where:
$\mathrm{n}=$ number of switch FETs (either top or bottom),
$\mathrm{C}=\mathrm{FET}$ gate capacitance,
$\mathrm{V}=$ maximum gate drive voltage (usually $\mathrm{V}_{\mathrm{CC}}$ ),
$f_{\text {OSC }}=$ switching frequency .

## Layout Considerations

1. The fast response time of $\mathrm{V}^{2}$ technology increases the IC's sensitivity to noise on the $\mathrm{V}_{\mathrm{FB}}$ line. Fortunately, a simple RC filter, formed by the feedback network and a small capacitor ( 100 pF works well, shown below as C6) placed between $\mathrm{V}_{\mathrm{FB}}$ and GND, filters out most noise and provides a system practically immune to jitter. This capacitor should be located as close as possible to the IC.
2. The COMP capacitor (shown below as C13) should be connected via its own path to the IC ground. The COMP capacitor is sensitive to the
intermittent ground drops caused by switching currents. A separate ground path will reduce the potential for jitter.
3. The $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor $(0.1 \mu \mathrm{~F}$ or greater, shown below as C 4 ) should be located as close as possible to the IC. This capacitor's connection to GND must be as short as possible. The $10 \Omega$ resistor (shown below as R3) should be placed close to the $\mathrm{V}_{\mathrm{CC}}$ pin.
4. The IC should not be placed in the path of switching currents. If a ground plane is used, care should be taken by the designer to ensure that the IC is not located over a ground or other current return path.


Figure 25.

## NCP5162

## General Purpose Synchronous Buck Controller

The NCP5162 is a synchronous dual N -Channel buck controller designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. It operates using a proprietary control method which allows a 100 ns response time to load transients. The NCP5162 is designed to operate over a 9-16 V range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V as the main supply for conversion.

The NCP5162 is specifically designed for high performance core logic. It includes the following features: $0.8 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The NCP5162 is available in a 16 pin surface mount package.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 2.0 A Gate Drivers
- 1.02 V Reference Voltage with $0.8 \%$ Tolerance
- 5.0 V \& 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Overvoltage Protection

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com
MARKING
DIAGRAM

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| NCP5162D | SO-16 | 48 Units/Rail |
| NCP5162DR2 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, 5.0 V to 2.5 V/20 A Core Logic Converter with 12 V Bias

## MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{\mathrm{J}}$ | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| Thermal Resistance, Junction-to-Case, $\mathrm{R}_{\text {©JC }}$ |  | 28 |
| Thermal Resistance, Junction-to-Ambient, $\mathrm{R}_{\text {©JA }}$ |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Lead Temperature Soldering: | Reflow: (Note 1$)$ | 230 peak |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $V_{C C 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 3.0 \mathrm{~A}$ peak |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 3.0 \mathrm{~A}$ peak |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{FB}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\text {OFF }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |

MAXIMUM RATINGS (continued)

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| Disable | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {GATE }(\mathrm{H})}$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 3.0 \mathrm{~A}$ peak |
| $\mathrm{V}_{\text {GATE }(\mathrm{L})}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/3.0} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/3.0} \mathrm{~A} \mathrm{peak}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}\right.$;
$\mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=6.6 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Error Amplifier

| Reference Voltage | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ | 1.012 | 1.02 | 1.028 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {FB }}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.3 | 1.0 | $\mu \mathrm{A}$ |
| Open Loop Gain | $\begin{aligned} & 1.25 \mathrm{~V}<\mathrm{V}_{\mathrm{COMP}}, 4.0 \mathrm{~V} ; \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F} \text {; } \\ & \text { Note } 2 \end{aligned}$ | - | 80 | - | dB |
| Unity Gain Bandwidth | $\mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F} ;$ Note 2 | - | 50 | - | kHz |
| COMP SINK Current | $\mathrm{V}_{\mathrm{COMP}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V} ; \mathrm{V}_{\text {SS }}>2.0 \mathrm{~V}$ | 30 | 60 | 120 | $\mu \mathrm{A}$ |
| COMP SOURCE Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP CLAMP Current | $\mathrm{V}_{\text {COMP }}=0 \mathrm{~V} ; \mathrm{V}_{\text {FB }}=2.7 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 4.0 | 4.3 | 5.0 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}$ | - | 1.00 | 1.15 | V |
| PSRR | $\begin{aligned} & 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} @ 1.0 \mathrm{kHz} \text {; } \\ & \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F} \text {; Note } 2 \end{aligned}$ | - | 70 | - | dB |
| Transconductance | - | - | 33 | - | mmho |

## $\mathrm{V}_{\text {CC1 }}$ Monitor

| Start Threshold | Output switching | 8.60 | 8.95 | 9.30 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 8.45 | 8.80 | 9.15 | V |
| Hysteresis | Start-Stop | - | 150 | - | mV |

## Soft Start (SS)

| Charge Time | - | 1.6 | 3.3 | 5.0 | ms |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | (Charge Time /Pulse Period) $\times 100$ | 1.0 | 3.3 | 6.0 | \% |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}\right.$; $\mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=6.6 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |
| :--- |
|  Test Conditions Min Typ Max Unit <br> Disable Input      <br> Threshold Voltage - 1.00 1.25 2.40 V <br> Pull Down Resistance - 25 50 110 $\mathrm{k} \Omega$ <br> Pull Down Voltage - 0.00 0.00 0.15 V |

$\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$

| Out Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})} \\ & <9.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})} \\ & >1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to $1.0 \mathrm{~V}_{;} \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=6.6 \mathrm{nF} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ rising to 1.0 V | 45 | 70 | 95 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to $1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=6.6 \mathrm{nF} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ rising to 1.0 V | 45 | 70 | 95 | ns |
| $\left.\mathrm{V}_{\text {GATE( }} \mathrm{H}\right), \mathrm{V}_{\text {GATE(L) }}$ Resistance | Resistor to LGND. Note 3 | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE(H), }} \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})} @ 10 \mathrm{~mA}$; LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} @ 10 \mathrm{~mA}$ | - | 600 | 800 | mV |

## Supply Current

| $\mathrm{I}_{\mathrm{CC} 1}$ No Switching | - | - | 14 | 17.5 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{CC} 2}$ No Switching | - | - | 11 | 13 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 1}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 14 | 17 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 2}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 11 | 13.5 | mA |

Coff

| Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | $\mathrm{C}_{\mathrm{OFF}}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |


| Time Out Timer |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ;$ <br> Record $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ Pulse High Duration | 10 | 30 | 65 |

3. Guaranteed by design, not $100 \%$ tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| SO-16 |  |  |
| 1 | Disable | This pin is internally pulled down to ground through a resistor, providing a logic 0 if left open. When pulled to $\mathrm{V}_{\mathrm{CC}}$, The output gate drivers are pulled low, powering off the external output stage. At the same time the Soft Start capacitor is slowly discharged by an internal $2.0 \mu \mathrm{~A}$ current source, setting the time out before the IC is restarted. |
| $2,3,4,6$ | NC | No connection. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE }}(\mathrm{H})$ | High FET driver pin capable of 3.0 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}}(\mathrm{L})$ from being in high state simultaneously. |
| 11 | PGND | High current ground for the IC. The MOSFET drivers are referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 3.0 A peak switching current. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC and low side gate driver. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $\mathrm{V}_{\mathrm{FB}}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## V $^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. ${ }^{2}$ Control Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the NCP5162 uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on
time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.
Switch on time is limited by an internal $30 \mu$ s timer, minimizing stress to the power components.

## Programmable Output

The NCP5162 has a 1.0 V reference voltage at the non-inverting input of the error amplifier, and the output voltage is programmed by connecting resistor divider feedback to the $V_{F B}$ and $V_{F F B}$ pins.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 8.95 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.
When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the COFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input (VCC1 and VCC2) (5.0 V/div.)
Trace 4-5.0 V Input ( $1.0 \mathrm{~V} /$ div.)
Figure 4. NCP5162 Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. NCP5162 Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1- Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Figure 6. NCP5162 Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Figure 7. NCP5162 Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUt }}=2.8 \mathrm{~V}$, I OUT $=0.5 \mathrm{~A}$ (Light Load)


Trace 1- Regulator Output Voltage ( $10 \mathrm{mV} /$ div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Figure 8. NCP5162 Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=13 \mathrm{~A}$ (Heavy Load)

## Transient Response

The NCP5162 $\mathrm{V}^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Trace 2- Regulator Output Voltage (output set for $1.55 \mathrm{~V}, 20 \mathrm{mV} / \mathrm{div}$.)
Figure 9. NCP5162 Output Voltage Response to a 12 A Load Pulse


Figure 10. NCP5162 Output Voltage Response to a 0 to 12 A Load Increase


Trace 2- Regulator Output Voltage (output set for $1.55 \mathrm{~V}, 20 \mathrm{mV} / \mathrm{div}$.)
Figure 11. NCP5162 Output Voltage Response to a 12 to 0 A Load Decrease

## PROTECTION AND MONITORING FEATURES

## $V_{\text {CC1 }}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 8.95 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 8.80 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\mathrm{FFB}}$ low comparator sets the FAULT latch. This causes the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=3.3 \%)$, while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3- Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. NCP5162 Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. NCP5162 Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.

> Trace 1- Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
> Trace 2- Inductor Switching Node $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 4-5.0 V from PC Power Supply (5.0 V/div.)

Figure 14. NCP5162 OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Trace 4-5.0 V from PC Power Supply (5.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Figure 15. NCP5162 OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 16). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power Good }}$.


Figure 16. Implementing Power Good with the NCP5162


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $10 \mathrm{~V} /$ div. )
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1- Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$. )
Trace 2- Power Good Signal (2.0 V/div.)
Figure 17. NCP5162 During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V

## Slope Compensation

The $\mathrm{V}^{2}$ control method uses a ramp signal, generated by the ESR of the output capacitors, that is proportional to the ripple current through the inductor. To maintain regulation, the $\mathrm{V}^{2}$ control loop monitors this ramp signal, through the PWM comparator, and terminates the switch on-time.
The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope presented to the PWM comparator, due to the very low ESR, can lead to pulse width jitter and variation caused by both random or synchronous noise.

Adding slope compensation to the control loop, avoids erratic operation of the PWM circuit, particularly at lower duty cycles and higher frequencies, where there is not enough ramp signal, and provides a more stable switchpoint.

The scheme that prevents that switching noise prematurely triggers the PWM circuit consists of adding a positive voltage slope to the output of the Error Amplifier (COMP pin) during an off-time cycle.

The circuit that implements this function is shown in Figure 18.


Figure 18. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of each On-Time Cycle
The ramp waveform is generated through a small RC filter that provides the proper voltage ramp at the beginning of each on-time cycle. The resistors R1 and R2 in the circuit of Figure 18 form a voltage divider from the GATE(L) output, superimposing a small artificial ramp on the output of the error amplifier. It is important that the series combination $\mathrm{R} 1 / \mathrm{R} 2$ is high enough in resistance not to load down and negatively affect the slew rate on the GATE(L) pin.

## Selecting External Components

The NCP5162 can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias
supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;
$\mathrm{V}_{\mathrm{GATE}}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{L})=12 \mathrm{~V}$
The gate drive waveforms are shown in Figure 19.


Figure 19. NCP5162 Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is RDS $_{\mathrm{ON}}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\mathrm{ILOAD}^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:
Power $=$ LLOAD $^{2} \times$ RDSON $\times(1-$ duty cycle $)$
Duty Cycle =

$$
\frac{\text { VOUT }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\text { VIN }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET }) \\
-(\text { ILOAD } \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (Coff)

The Coff timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\text {OFF }}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=\mathrm{V}_{\mathrm{BD}} \times$ ILOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the NCP5162 demonstration board as shown in Figure 8;
Power $=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}$
This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$
\text { Thermal Impedance }=\frac{T_{J U N C T I O N(M A X)}-\text { TAMBIENT }^{\text {Power }}}{}
$$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 20. Filter Components


Figure 21. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. Connect the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
7. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.
Route gate drive signals $\mathrm{V}_{\operatorname{GATE}(\mathrm{H})}$ (pin 10) and $\mathrm{V}_{\text {GATE(L) }}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.


Figure 22. Layout Guidelines

## CS5421

## Dual Out-of-Phase Synchronous Buck Controller with Remote Sense

The CS5421 is a dual N -channel synchronous buck regulator controller. It contains all the circuitry required for two independent buck regulators and utilizes the $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation, while using the least number of external components. The CS5421 features out-of-phase synchronization between the channels, reducing the input filter requirement. The CS5421 also provides undervoltage lockout, Soft Start, built in adaptive FET non-overlap and remote sense capability. The part is available in a 16 Lead SO Narrow package allowing the designer to minimize solution size.

## Features

- $\mathrm{V}^{2}$ Control Topology
- 150 ns Transient Response
- Programmable Soft Start
- 25 ns Gate Rise and Fall Times (with 1.0 nF load)
- 40 ns Adaptive FET Nonoverlap Time
- 100\% Duty Cycle for Enhanced Transient Response
- Internal Slope Compensation
- $1.0 \mathrm{~V} 0.8 \%$ and $2.0 \%$ Error Amplifier References
- 150 kHz to 750 kHz Programmable Frequency Operation
- Switching Frequency Set by Single Resistor
- Out-Of-Phase Synchronization Between the Channels Reduces the Input Filter Requirement
- Undervoltage Lockout
- On/Off Control Through Use of the COMP Pins

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SO-16
D SUFFIX
CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5421GD16 | SO-16 | 48 Units/Rail |
| CS5421GDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, 5.0 V/12 V to 3.3 V/11 A and 1.5 V/9.0 A Converter for Processor I/O and Core Supplies

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\text {S }}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Package Thermal Resistance: Junction-to-Case, R өJc Junction-to-Ambient, $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{gathered} 28 \\ 115 \end{gathered}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{w} \end{aligned}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Symbol | Pin Name | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | $\mathrm{I}_{\text {SOURCE }}$ | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | IC Power Input | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | 1.5 A peak <br> 200 mA DC |
| COMP1, COMP2 | Compensation Capacitor for <br> Channel 1 or 2 | 4.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $\mathrm{~V}_{\text {FB1 }}, \mathrm{V}_{\text {FB2 }}$ | Voltage Feedback Input for <br> Channel 1 or 2 | 5.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $\mathrm{~V}_{\text {FB1 }}, \mathrm{V}_{\text {FB2 }}$ | Fast Voltage Feedback <br> Input for Channel 1 or 2 | 5.0 V | -0.3 V | 1.0 mA | 1.0 mA |

## ABSOLUTE MAXIMUM RATINGS (continued)

| Pin Symbol | Pin Name | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Rosc | Oscillator Resistor | 4.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| GATE(H)1, GATE(H)2 | High-Side FET Driver for Channel 1 or 2 | 16 V | -0.3 V | 1.5 A peak 200 mA DC | 1.5 A peak 200 mA DC |
| GATE(L)1, GATE(L)2 | Low-Side FET Driver for Channel 1 or 2 | 16 V | -0.3 V | 1.5 A peak 200 mA DC | 1.5 A peak 200 mA DC |
| PGND1 | Power Ground for Channel 1 | 0 V | 0 V | 1.5 A peak 200 mA DC | N/A |
| PGND2 | Power Ground for Channel 2 | 0 V | 0 V | $\begin{aligned} & 1.5 \mathrm{~A} \text { peak } \\ & 200 \mathrm{~mA} \mathrm{DC} \end{aligned}$ | N/A |
| SGND | Ground for Internal Reference | 150 mV | 0 V | 1.0 mA | N/A |
| LGND | Logic Ground | 0 V | 0 V | 50 mA | N/A |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}\right.$; $\mathrm{R}_{\mathrm{OSC}}=30.9 \mathrm{k}, \mathrm{C}_{\text {COMP } 1,2}=0.1 \mu \mathrm{~F}$,
$10.8 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<13.2 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H}) 1,2}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L}) 1,2}=1.0 \mathrm{nF}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- |

Error Amplifier

| $\mathrm{V}_{\mathrm{FB} 1(2)}$ Bias Current | $\mathrm{V}_{\mathrm{FB} 1(2)}=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{COMP} 1,2$ Source Current | $\mathrm{COMP} 1,2=1.2 \mathrm{~V}$ to $2.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB} 1(2)}=0.8 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| COMP1,2 Sink Current | $\mathrm{COMP} 1,2=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB} 1(2)}=1.2 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| Reference Voltage 1 | $\mathrm{COMP} 1=\mathrm{V}_{\mathrm{FB} 1 ; 25^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}}$ | 0.992 | 1.000 | 1.008 | V |
| Reference Voltage 2 | $\mathrm{COMP} 2=\mathrm{V}_{\mathrm{FB} 2}$ | 0.980 | 1.000 | 1.020 | V |
| COMP1,2 Max Voltage | $\mathrm{V}_{\mathrm{FB} 1(2)}=0.8 \mathrm{~V}$ | 3.0 | 3.3 | - | V |
| COMP1,2 Min Voltage | $\mathrm{V}_{\mathrm{FB} 1(2)}=1.2 \mathrm{~V}$ | - | 0.25 | 0.35 | V |
| Open Loop Gain |  | - | - | 40 | - |
| Unity Gain Band Width | - | - | 70 | - | dB |
| PSRR @ 1.0 kHz | - | - | 32 | - | mmho |
| Transconductance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Output Impedance | - |  | - | dB |  |

GATE(H) and GATE(L)

| High Voltage (AC) | $\begin{aligned} & \text { Measure: } \mathrm{V}_{\mathrm{CC}}-\mathrm{GATE}(\mathrm{~L}) 1,2 ; \\ & \mathrm{V}_{\mathrm{CC}}-\operatorname{GATE}(\mathrm{H}) 1,2 ; \text { Note } 2 \end{aligned}$ | - | 0 | 0.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Measure:GATE(L)1,2 or GATE(H)1,2; Note 2 | - | 0 | 0.5 | V |
| Rise Time | $\begin{aligned} 1.5 \mathrm{~V} & <\operatorname{GATE}(\mathrm{L}) 1,2<\mathrm{V}_{\mathrm{CC}}-1.5 \mathrm{~V} \\ 1.5 \mathrm{~V} & <\operatorname{GATE}(\mathrm{H}) 1,2<\mathrm{V}_{\mathrm{CC}}-1.5 \mathrm{~V} \end{aligned}$ | - | 25 | 60 | ns |
| Fall Time | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}-1.5>\operatorname{GATE}(\mathrm{L}) 1,2>1.5 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}-1.5>\operatorname{GATE}(\mathrm{H}) 1,2>1.5 \mathrm{~V} \end{gathered}$ | - | 20 | 60 | ns |
| GATE(H) to GATE(L) Delay | GATE(H) $1,2<1.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{L}) 1,2>1.0 \mathrm{~V}$ | 40 | 70 | 100 | ns |
| GATE(L) to GATE(H) Delay | GATE(L) $1,2<1.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{H}) 1,2>1.0 \mathrm{~V}$ | 40 | 70 | 100 | ns |
| GATE(H)1(2) and GATE(L)1(2) pull-down | Resistance to PGND Note 2 | 50 | 125 | 280 | k $\Omega$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}\right.$; $\mathrm{R}_{\mathrm{OSC}}=30.9 \mathrm{k}, \mathrm{C}_{\mathrm{COMP} 1,2}=0.1 \mu \mathrm{~F}$, $10.8 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<13.2 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H}) 1,2}=\mathrm{C}_{\mathrm{GATE}}(\mathrm{L}) 1,2=1.0 \mathrm{nF}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PWM Comparator |  |  |  |  |  |
| Transient Response | COMP1,2 $=1.0 \mathrm{~V}, \mathrm{~V}_{\text {FB1 }}(2)=\mathrm{V}_{\text {FFB1 }}(2)=0$ to 1.2 V | - | 150 | 300 | ns |
| PWM Comparator Offset | $\mathrm{V}_{\mathrm{FFB} 1(2)}=0 \mathrm{~V}$; Increase COMP1,2 until GATE(H)1,2 starts switching | 0.30 | 0.45 | 0.60 | V |
| Artificial Ramp | Duty cycle $=50 \%$, Note 3 | 40 | 70 | 100 | mV |
| $\mathrm{V}_{\text {FFB1 (2) }}$ Bias Current | $\mathrm{V}_{\text {FFB1 }}(2)=0 \mathrm{~V}$ | - | 0.4 | 1.5 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {FFB1 (2) }}$ Input Range | - | 0.0 | - | 1.1 | V |
| Minimum Pulse Width | - | - | - | 300 | ns |

## Oscillator

| Switching Frequency | $\mathrm{R}_{\text {OSC }}=61.9 \mathrm{k}$; Measure GATE(H)2, Note 3 | 112 | 150 | 188 | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Switching Frequency | $\mathrm{R}_{\text {OSC }}=30.9 \mathrm{k}$; Measure GATE(H)2 | 224 | 300 | 376 | kHz |
| Switching Frequency | Rosc $=11.8 \mathrm{k}$; Measure GATE(H)2, Note 3 | 600 | 750 | 900 | kHz |
| Rosc Voltage | $\mathrm{R}_{\text {OSC }}=30.9 \mathrm{k}$, Note 3 | 0.970 | 1.000 | 1.030 | V |
| Phase Difference | - | - | 180 | - | 。 |

## Supply Currents

| $V_{\text {CC }}$ Current | COMP1,2 = 0 V (No Switching) | - | 16 | 22 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| SGND Current | - | 75 | 150 | 225 | $\mu \mathrm{~A}$ |

Undervoltage Lockout

| Start Threshold | GATE(H) Switching; COMP1,2 charging | 7.8 | 8.6 | 9.6 | V |
| :--- | :--- | :--- | :--- | :--- | :---: |
| Stop Threshold | GATE(H) not switching; COMP1,2 discharging | 7.0 | 7.8 | 8.6 | V |
| Hysteresis | Start-Stop | 0.5 | 0.8 | 1.5 | V |

3. Guaranteed by design, not $100 \%$ tested in production.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 16 Lead SO Narrow | PIN SYMBOL | FUNCTION |
| 1 | GATE(H)1 | High Side Switch FET driver pin for the channel 1 FET. |
| 2 | GATE(L) 1 | Low Side Synchronous FET driver pin for the channel 1 FET. |
| 3 | PGND1 | High Current ground for the GATE(H)1 and GATE(L)1 pins. |
| 4 | LGND | Logic ground. All control circuits are referenced to this pin. IC substrate connection. |
| 5 | SGND | Ground sense for the internal reference. |
| 6 | $\mathrm{V}_{\text {FFB1 }}$ | Input for the channel 1 PWM comparator. |
| 7 | $\mathrm{V}_{\mathrm{FB} 1}$ | Error amplifier inverting input for channel 1. |
| 8 | COMP1 | Channel 1 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation. The same capacitor provides Soft Start timing for channel 1. This pin also disables the channel 1 output when pulled below 0.3 V . |
| 9 | COMP2 | Channel 2 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation and Soft Start timing for channel 2. Channel 2 output is disabled when this pin is pulled below 0.3 V . |

## PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 16 Lead SO Narrow | PIN SYMBOL | FUNCTION |
| 10 | $\mathrm{V}_{\text {FB2 }}$ | Error amplifier inverting input for channel 2. |
| 11 | $\mathrm{V}_{\text {FFB2 }}$ | Input for the channel 2 PWM comparator. |
| 12 | Rosc | A resistor from this pin to ground sets switching frequency. |
| 13 | $V_{\text {cc }}$ | Input Power supply pin. |
| 14 | PGND2 | High Current ground for the GATE(H)2 and GATE(L)2 pins. |
| 15 | GATE(L)2 | Low Side Synchronous FET driver pin for the channel 2 FET. |
| 16 | GATE(H)2 | High Side Switch FET driver pin for the channel 2 FET. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

The CS5421 is a dual power supply controller that utilizes the $\mathrm{V}^{2}$ control method. Two synchronous $\mathrm{V}^{2}$ buck regulators can be built using a single controller. The fixed-frequency architecture, driven from a common oscillator, ensures a $180^{\circ}$ phase differential between channels.

## $V^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The $\mathrm{V}^{2}$ method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.


Figure 3. ${ }^{2}$ Control with Slope Compensation
The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction
time to the output load step is not related to the crossover frequency of the error signal loop.
The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation is drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulations. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.
The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity particularly at higher duty cycle (above 50\%).

## Startup

The CS5421 features a programmable Soft Start function, which is implemented through the Error Amplifier and the external Compensation Capacitor. This feature prevents stress to the power components and overshoot of the output voltage during start-up. As power is applied to the regulator, the CS5421 Undervoltage Lockout circuit (UVL) monitors the IC's supply voltage $\left(\mathrm{V}_{\mathrm{CC}}\right)$. The UVL circuit prevents the MOSFET gates from switching until $\mathrm{V}_{\mathrm{CC}}$ exceeds the 8.6 V threshold. A hysteresis function of 800 mV improves noise immunity. The Compensation Capacitor connected to the COMP pin is charged by a $30 \mu \mathrm{~A}$ current source. When the capacitor voltage exceeds the 0.4 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE $(\mathrm{H})$ is activated turning on the upper MOSFET. The current then ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the COMP pin voltage minus the 0.4 V PWM comparator offset
threshold and the artificial ramp, the PWM comparator terminates the initial pulse.


Figure 4. Idealized Waveforms

## Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the $\mathrm{V}^{2}$ control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

## Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading, according to the following graphs.


Figure 5. Average Rise and Fall Times

## Transient Response

The 200 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor
current. For better transient response, several high frequency and bulk output capacitors are usually used.

## Out-of-Phase Synchronization

In out-of-phase synchronization, the turn-on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel which is $180^{\circ}$ out of phase with the clock signal of the first channel.
The advantages of out-of-phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. The effect of this overlap reduction is to reduce the input filter requirement, allowing the use of smaller components. In addition, since peak current occurs during a shorter time period, emitted EMI is also reduced, thereby reducing shielding requirements.

## Overvoltage Protection

Overvoltage Protection (OVP) is provided as a result of the normal operation of the $\mathrm{V}^{2}$ control method and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns , turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

## Remote Sense

When the load is far away from the regulator, the long feedback traces can cause additional voltage drop and induce noise which affects the accuracy of voltage regulation. A separate signal ground is provided to improve the noise immunity of remote voltage sensing. The 1.0 V reference voltage of the error amplifiers is directly referenced to this ground and no large currents flow through this ground during normal operation. The noise immunity and regulation accuracy can be improved significantly.

## Output Enable

On/Off control of the regulator outputs can be implemented by pulling the COMP pins low. The COMP pins must be driven below the 0.4 V PWM comparator offset voltage in order to disable the switching of the GATE drivers.

## DESIGN GUIDELINES

## Definition of the design specifications

The output voltage tolerance can be affected by any or all of the following reasons:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide an output voltage that will meet the specified tolerance at the load.

The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

## Selecting Feedback Divider Resistors



Figure 6. Selecting Feedback Divider Resistors
The feedback pins $\left(\mathrm{V}_{\mathrm{FB} 1(2)}\right)$ are connected to externalresistor dividers to set the output voltages. The error amplifier is referenced to 1.0 V and the output voltage is determined by selecting resistor divider values. Resistor R1 is selected based on a design trade-off between efficiency and output voltage accuracy. The output voltage error can be estimated due to the bias current of the error amplifier neglecting resistor tolerance:

$$
\text { Error\% }=\frac{1 \times 10^{-6} \times \mathrm{R} 1}{1.0} \times 100 \%
$$

R2 can be sized after R1 has been determined:

$$
\mathrm{R} 2=\mathrm{R} 1\left(\frac{\mathrm{~V} \text { OUT }}{1.0}-1.0\right)
$$

## Calculating Duty Cycle

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$
\text { Duty Cycle }=\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\left(\mathrm{V}_{\mathrm{HFET}}+\mathrm{V}_{\mathrm{L}}\right)}{\mathrm{V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{LFE}}-\mathrm{V}_{\mathrm{HFET}}-\mathrm{V}_{\mathrm{L}}}
$$

where:
$\mathrm{V}_{\text {OUT }}=$ buck regulator output voltage;
$\mathrm{V}_{\text {HFET }}=$ high side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$;
$\mathrm{V}_{\mathrm{L}}=$ output inductor voltage drop due to inductor wire DC resistance;
$\mathrm{V}_{\mathrm{IN}}=$ buck regulator input voltage;
$\mathrm{V}_{\mathrm{LFET}}=$ low side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$.


Figure 7. Switching Frequency

## Selecting the Switching Frequency

Selecting the switching frequency is a trade-off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

The value of the oscillator resistor is designed to be linearly related to the switching period. If the designer prefers not to use Figure 7 to select the necessary resistor, the following equation quite accurately predicts the proper resistance for room temperature conditions.

$$
\text { ROSC }=\frac{21700-\mathrm{fSW}}{2.31 \mathrm{fSW}}
$$

where:
$\mathrm{R}_{\mathrm{OSC}}=$ oscillator resistor in $\mathrm{k} \Omega$;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency in kHz .

## Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due
to its high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The minimum value of inductance which prevents inductor saturation or exceeding the rated FET current can be calculated as follows:

$$
\mathrm{L}_{\mathrm{MIN}}=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\mathrm{OUT}}\right) \mathrm{V}_{\mathrm{OUT}}}{\mathrm{fSW} \times \mathrm{V}_{\text {IN }}(\mathrm{MIN}) \times \operatorname{ISW}(\mathrm{MAX})}
$$

where:
$\mathrm{L}_{\mathrm{MIN}}=$ minimum inductance value;
$\mathrm{V}_{\mathrm{IN}(\mathrm{MIN})}=$ minimum design input voltage;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency;
$\mathrm{I}_{\mathrm{SW}(\mathrm{MAX})}$ - maximum design switch current.
The inductor ripple current can then be determined:

$$
\Delta_{\mathrm{L}}=\frac{\mathrm{VOUT} \times(1.0-\mathrm{D})}{\mathrm{L} \times \mathrm{fSW}}
$$

where:
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{L}=$ inductor value;
$\mathrm{D}=$ duty cycle.
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency
The designer can now verify if the number of output capacitors will provide an acceptable output voltage ripple ( $1.0 \%$ of output voltage is common). The formula below is used:

$$
\Delta \mathrm{I}_{\mathrm{L}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\mathrm{ESR}_{\mathrm{MAX}}}
$$

Rearranging we have:

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{I}_{\mathrm{L}}}
$$

where:
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR;
$\Delta \mathrm{V}_{\text {OUT }}=1.0 \% \times \mathrm{V}_{\text {OUT }}=$ maximum allowable output voltage ripple ( budgeted by the designer );
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage.
The number of output capacitors is determined by:

$$
\text { Number of capacitors }=\frac{\mathrm{ESR} \mathrm{CAP}}{\mathrm{ESR}} \mathrm{MAX}
$$

where:
$E S R_{\text {CAP }}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).
The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$
\mathrm{I}(\mathrm{PEAK})=\mathrm{IOUT}+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2.0}
$$

where:
$\mathrm{I}_{\mathrm{L}(\mathrm{PEAK})}=$ inductor peak current;
IOUT $=$ load current;
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current.

$$
\mathrm{IL}(\mathrm{VALLEY})=\mathrm{IOUT}-\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2.0}
$$

where:
$\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current.

## Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I} \mathrm{OUT} \times\left(\frac{\mathrm{ESL}}{\Delta \mathrm{t}}+\mathrm{ESR}+\frac{\mathrm{tTR}}{\mathrm{COUT}}\right)
$$

where:
$\Delta \mathrm{I}_{\text {OUT }} / \Delta \mathrm{t}=$ load current slew rate;
$\Delta \mathrm{I}_{\text {OUT }}=$ load transient;
$\Delta \mathrm{t}=$ load transient duration time;
$\mathrm{ESL}=$ Maximum allowable ESL including capacitors, circuit traces, and vias;
ESR $=$ Maximum allowable ESR including capacitors and circuit traces;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time.
The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$
\mathrm{ESR}_{\text {MAX }}=\frac{\Delta \mathrm{V}_{\mathrm{ESR}}}{\Delta \mathrm{I} \text { OUT }}
$$

where:
$\Delta \mathrm{V}_{\mathrm{ESR}}=$ change in output voltage due to ESR (assigned by the designer)
Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where:
$\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).
$\mathrm{ESR}=$ maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$
\Delta \mathrm{V}_{\mathrm{ESR}}=\Delta \mathrm{I} \text { OUT } \times \text { ESRMAX }
$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$
\mathrm{ESL}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESL}} \times \Delta \mathrm{t}}{\Delta \mathrm{I}}
$$

## Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$
\operatorname{LIN}=\frac{\Delta V}{(\mathrm{dl} / \mathrm{dt}) \mathrm{MAX}}
$$

where:
$\mathrm{L}_{\mathrm{IN}}=$ input inductor value;
$\Delta \mathrm{V}=$ voltage seen by the input inductor during a full load swing;
$(\mathrm{dI} / \mathrm{dt})_{\mathrm{MAX}}=$ maximum allowable input current slew rate.
The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2 , a roll-off rate of $-40 \mathrm{~dB} / \mathrm{dec}$, and a corner frequency:

$$
\mathrm{ff}_{\mathrm{C}}=\frac{1.0}{2 \pi \times \sqrt{\mathrm{LC}}}
$$

where:
$\mathrm{L}=$ input inductor;
$\mathrm{C}=$ input capacitor(s).

## SELECTION OF THE POWER FET

## FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) Its very high input impedance; and 2) Its very fast switching times. The electrical characteristics of a MOSFET are considered to be those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven.

The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of $\mathrm{V}_{\mathrm{GS}}$, and the faster the turn-on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn-on switching losses, 4) turn-off switching losses, and 5) gate-transitions losses. The latter three losses are proportional to frequency.

The most important aspect of FET performance is the Static Drain-To-Source On-Resistance ( $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ ), which effects regulator efficiency and FET thermal management requirements. The On-Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On-Resistance also increases. Its positive temperature coefficient is between $+0.6 \% /{ }^{\circ} \mathrm{C}$ and $+0.85 \% /{ }^{\circ} \mathrm{C}$. The higher the On-Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used.
Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail-to-rail due to overshoot caused by the capacitive load they present to the controller IC.

## Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed $150^{\circ} \mathrm{C}$.

The maximum RMS current through the switch can be determined by the following formula:

$$
\operatorname{IRMS}(\mathrm{H})=\sqrt{\frac{\left[\begin{array}{l}
\mathrm{IL}(\mathrm{PEAK})^{2}+(\mathrm{IL}(\mathrm{PEAK}) \times \mathrm{I}(\mathrm{VALLEY})) \\
+\mathrm{I}(\mathrm{VALLEY})^{2} \times \mathrm{D}
\end{array}\right]}{3.0}}
$$

where:
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{I}_{\mathrm{L}(\text { PEAK })}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current;
D = duty cycle.
Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$
\operatorname{PRMS}(\mathrm{H})=\operatorname{IRMS}(\mathrm{H})^{2} \times \operatorname{RDS}(\mathrm{ON})
$$

where:
$\mathrm{P}_{\text {RMS }}(\mathrm{H})=$ switching MOSFET conduction losses;
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=\mathrm{FET}$ drain-to-source on-resistance

The upper MOSFET switching losses are caused during MOSFET switch-on and switch-off and can be determined by using the following formula:

$$
\begin{aligned}
\mathrm{PSWH} & =\operatorname{PSWH}(\mathrm{ON})+\mathrm{PSWH}(\mathrm{OFF}) \\
& =\frac{\mathrm{V}_{\text {IN }} \times \operatorname{IOUT} \times(\mathrm{tRISE}+\mathrm{tFALL})}{6.0 \mathrm{~T}}
\end{aligned}
$$

where:
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses;
$\mathrm{V}_{\mathrm{IN}}=$ input voltage;
$\mathrm{I}_{\text {OUT }}=$ load current;
$t_{\text {RISE }}=$ MOSFET rise time (from FET manufacturer's
switching characteristics performance curve);
$\mathrm{t}_{\text {FALL }}=$ MOSFET fall time (from FET manufacturer's
switching characteristics performance curve);
$\mathrm{T}=1 / \mathrm{f}_{\mathrm{SW}}=$ period.
The total power dissipation in the switching MOSFET can then be calculated as:

$$
\text { PHFET(TOTAL) }=\text { PRMS }(\mathrm{H})+\mathrm{PSWH}(\mathrm{ON})+\mathrm{PSWH}(\mathrm{OFF})
$$

where:
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) MOSFET losses;
$\mathrm{P}_{\text {RMS }}(\mathrm{H})=$ upper MOSFET switch conduction Losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses;
Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$
\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\mathrm{A}}+\left[\mathrm{PHFET}(\mathrm{TOTAL}) \times \mathrm{R}_{\Theta} \mathrm{JA}\right]
$$

where:
$\mathrm{T}_{\mathrm{J}}=\mathrm{FET}$ junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) FET losses;
$\mathrm{R}_{\Theta \mathrm{JA}}=$ upper FET junction-to-ambient thermal resistance.

## Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$
\begin{aligned}
\operatorname{PRMS}(\mathrm{L}) & =\mathrm{I}_{\mathrm{RMS}^{2}} \times \mathrm{R}_{\mathrm{DS}(\mathrm{ON})} \\
& =[\mathrm{IOUT} \times \sqrt{(1.0-\mathrm{D})}]^{2} \times \mathrm{RDS}(\mathrm{ON})
\end{aligned}
$$

where:
$\mathrm{P}_{\text {RMS(L) }}=$ lower MOSFET conduction losses;
$\mathrm{I}_{\text {OUT }}=$ load current;
D = Duty Cycle;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=$ lower FET drain-to-source on-resistance.
The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non-overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$
\text { PSWL }=V_{S D} \times \operatorname{ILOAD} \times \text { non-overlap time } \times f \text { SW }
$$

where:
$\mathrm{P}_{\text {SWL }}=$ lower FET switching losses;
$\mathrm{V}_{\mathrm{SD}}=$ lower FET source-to-drain voltage;
$\mathrm{I}_{\text {LOAD }}=$ load current;
Non-overlap time $=\operatorname{GATE}(\mathrm{L})$-to-GATE(H) or GATE(H)-to-GATE(L) delay (from CS5421 data sheet Electrical Characteristics section);
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency.
The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$
\text { PLFET(TOTAL) }=\text { PRMS(L) }+ \text { PSWL }
$$

where:
$P_{\text {LFET(TOTAL) }}=$ Synchronous (lower) FET total losses;
$\mathrm{P}_{\mathrm{RMS}(\mathrm{L})}=$ Switch Conduction Losses;
$\mathrm{P}_{\text {SWL }}=$ Switching losses.
Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$
\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\mathrm{A}}+\left[\mathrm{PLFET}(\mathrm{TOTAL}) \times \mathrm{R}_{\Theta J A}\right]
$$

where:
$\mathrm{T}_{\mathrm{J}}=$ MOSFET junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\left.\mathrm{P}_{\text {LFET }(\text { TOTAL }}\right)=$ total synchronous (lower) FET losses;
$\mathrm{R}_{\Theta \mathrm{JA}}=$ lower FET junction-to-ambient thermal resistance.

## Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, $\mathrm{V}_{\mathrm{CC}}$, and the CS5421 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:

$$
\begin{aligned}
\operatorname{PCONTROL}(\mathrm{IC}) & =\operatorname{ICC1} \mathrm{V}_{\mathrm{CC} 1}+\operatorname{PGATE}(\mathrm{H}) 1 \\
& +\operatorname{PGATE}(\mathrm{L}) 1+\operatorname{PGATE}(\mathrm{H}) 2+\operatorname{PGATE}(\mathrm{L}) 2
\end{aligned}
$$

where:
$\mathrm{P}_{\text {CONTROL(IC) }}=$ control IC power dissipation;
$\mathrm{I}_{\mathrm{CC} 1}=\mathrm{IC}$ quiescent supply current;
$\mathrm{V}_{\mathrm{CC} 1}=\mathrm{IC}$ supply voltage;
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{P}_{\text {GATE(L) }}=$ lower MOSFET gate driver (IC) losses.
The upper (switching) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{H})=\operatorname{QGATE}(\mathrm{H}) \times \mathrm{fSW} \times \mathrm{V}_{\mathrm{CC}}
$$

where:
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{H})}=$ total upper MOSFET gate charge at $\mathrm{V}_{\mathrm{CC}}$;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency;
The lower (synchronous) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{L})=\operatorname{QGATE}_{\mathrm{G}}(\mathrm{~L}) \times \mathrm{fSW} \times \mathrm{V}_{\mathrm{GATE}}(\mathrm{~L})
$$

where:
$\mathrm{P}_{\mathrm{GATE}(\mathrm{L})}=$ lower MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{L})}=$ total lower MOSFET gate charge at $\mathrm{V}_{\mathrm{CC}}$;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency;
The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

## Adding External Slope Compensation

Today's voltage regulators are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that very little voltage ramp exists at the control IC feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ), resulting in increased regulator sensitivity to noise and the potential for loop instability. In applications where the internal slope compensation is insufficient, the performance of the CS5421-based regulator can be improved through the addition of a fixed amount of external slope compensation at the output of the PWM Error Amplifier (the COMP pin) during the regulator off-time. Referring to Figure 7, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1 and R2.
$\mathrm{V}_{\text {SLOPECOMP }}=\mathrm{V}_{\text {GATE }}(\mathrm{L}) \times\left(\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}\right) \times\left(1.0-\mathrm{e}^{\frac{-\mathrm{t}}{\tau}}\right)$
where:
$\mathrm{V}_{\text {SLOPECOMP }}=$ amount of slope added;
$\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}=$ lower MOSFET gate voltage;
R1, R2 = voltage divider resistors;
$\mathrm{t}=\mathrm{t}_{\mathrm{ON}}$ or $\mathrm{t}_{\text {OFF }}$ (switch off-time);
$\tau=\mathrm{RC}$ constant determined by C 1 and the parallel combination of R1, R 2 neglecting the low driver output impedance.
The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off-time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin.


Figure 8. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFET

As the plastic packaging of a semiconductor will deteriorate at high temperatures, it is necessary to limit the junction temperature of the control IC and power MOSFETs to maintain high reliability. Most semiconductor devices have a maximum junction temperature of $150^{\circ} \mathrm{C}$, and manufacturers recommend operating their products at lower temperatures if at all possible.
Power dissipation in a semiconductor devices results in the generation of heat in the pin junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturer's data sheets as $\Theta_{\mathrm{JA}}$, or junction-to-air thermal resistance. The on-chip junction temperature can be calculated if $\Theta_{\mathrm{JA}}$, the air temperature at the surface of the IC, and the on-chip power dissipation are known.

$$
T_{J}=T_{A}+(P D \Theta J A)
$$

where:
TJ = IC or FET junction temperature (in degrees C);
TA = ambient temperature (in degrees C);
$\mathrm{PD}=$ power dissipated by part in question (in watts);
$\Theta_{\mathrm{JA}}=$ junction-to-ambient thermal resistance (in degrees C per watt).
The value for $\Theta_{\mathrm{JA}}$ can be found in the Absolute Maximum Ratings table on page 1637 of this datasheet. Note that this value is different for every package style and every manufacturer.
The junction temperature should be calculated for all semiconductor devices as a part of the design phase in order to ensure that the devices are operated below the manufacturer's maximum junction temperature specification. If any component's temperature exceeds the manufacturer's maximum temperature, some form of heatsink will be required.

Heatsinking improves the thermal performance of any component. Adding a heatsink will reduce the magnitude of $\Theta_{\mathrm{JA}}$ by providing a larger surface area for the transfer of heat from the component to the surrounding air. Typical heatsinking techniques include the use of commercial heatsinks for devices in TO-220 packages, or printed circuit board techniques such as thermal bias and large copper foil areas for surface mount packages.
When choosing a heatsink, it is important to realize that $\Theta_{\mathrm{JA}}$ is comprised of several components:

$$
\Theta_{\mathrm{JA}}=\Theta_{\mathrm{JC}}+\Theta_{\mathrm{CS}}+\Theta_{\mathrm{SA}}
$$

where:
$\Theta_{\mathrm{JC}}=$ the junction-to-case thermal resistance (in degrees C per watt);
$\Theta_{\mathrm{CS}}=$ the case-to-sink thermal resistance (in degrees C per watt);
$\Theta_{\mathrm{SA}}=$ the sink-to-ambient thermal resistance (in degrees C per watt).
The value for $\Theta_{\mathrm{JC}}$ is included in the component manufacturer's data sheets. Its value is dependent on the mold compound and lead frames used in assembly of the semiconductor device in question.
$\Theta_{\mathrm{CS}}$ is the thermal impedance from the surface of the case to the heatsink. This component of the thermal resistance is dependent on the roughness of the heatsink and component as well as on the pressure applied between the two. $\Theta_{\mathrm{CS}}$ can be reduced by using thermal pads or by applying a thin layer of thermal grease between the case and the heatsink. Such materials reduce the air gap normally found between the heatsink and the case and provide a better path for thermal energy. Values of $\Theta_{\mathrm{CS}}$ are found in catalogs published by manufacturers of heatsinks and thermal compounds.

Finally, $\Theta_{\mathrm{SA}}$ is the thermal impedance from the heatsink to the ambient environment. $\Theta_{\mathrm{SA}}$ is the important parameter when selecting a heatsink. Low values of $\Theta_{\mathrm{SA}}$ allow increased power dissipation without exceeding the maximum junction temperature of the component. Values of $\Theta_{\text {SA }}$ are found in catalogs published by heatsink manufacturers.

The basic equation for selecting a heatsink is:

$$
P=\frac{T J-T_{A}}{\Theta J C+\Theta C S+\Theta S A}
$$

where:
$\mathrm{P}_{\mathrm{D}}=$ power dissipated by part in question (in watts);
$\mathrm{T}_{\mathrm{J}}=\mathrm{IC}$ or FET junction temperature (in degrees C );
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature (in degrees C );
$\Theta_{\mathrm{JC}}=$ the junction-to-case thermal resistance (in degrees C per watt);
$\Theta_{\mathrm{CS}}=$ the case-to-sink thermal resistance (in degrees C per watt);
$\Theta_{\mathrm{SA}}=$ the sink-to-ambient thermal resistance (in degrees C per watt).
The choice of heatsink is dependent on the value of $\Theta_{\text {SA }}$ required to keep the calculated junction temperature at the given level of power dissipation below the component manufacturer's maximum junction temperature.

## EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The
input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

## LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS5421.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double-sided PCB's a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCB's are usually sufficient for a good layout, four-layer PCB's are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layers for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the COMP capacitor as close as possible to the COMP pin.
12. Connect the filter components of the following pins: $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}$, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
13. Place the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitors as close as possible to the IC.

## CS5422

## Dual Out-of-Phase <br> Synchronous <br> Buck Controller with Current Limit

The CS5422 is a dual N -channel synchronous buck regulator controller. It contains all the circuitry required for two independent buck regulators and utilizes the $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation, while using the least number of external components. The CS5422 features out-of-phase synchronization between the channels, reducing the input filter requirement. The CS5422 also provides undervoltage lockout, Soft Start, built in adaptive FET non-overlap and hiccup mode overcurrent protection. The part is available in a 16 Lead SO Narrow or 24 Lead Fused SO Wide package allowing the designer to minimize solution size.

## Features

- $\mathrm{V}^{2}$ Control Topology
- Hiccup Mode Overcurrent Protection
- 150 ns Transient Response
- Programmable Soft Start
- 100\% Duty Cycle for Enhanced Transient Response
- 150 kHz to 600 kHz Programmable Frequency Operation
- Switching Frequency Set by Single Resistor
- Out-Of-Phase Synchronization Between the Channels Reduces the Input Filter Requirement
- Undervoltage Lockout
- Internally Fused Leads available in 24 Lead SO Wide Package

ON Semiconductor ${ }^{\text {T }}$
ttp://onsemi.com


PIN CONNECTIONS AND MARKING DIAGRAMS


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5422GD16 | SO-16 | 48 Units/Rail |
| CS5422GDR16 | SO-16 | 2500 Tape \& Reel |
| CS5422GDWF24 | SO-24L | 31 Units/Rail |
| CS5422GDWFR24 | SO-24L | 1000 Tape \& Reel |



Figure 1. Application Diagram, 12 V to 1.5 V/10 A and 1.8 V/10 A Converter

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{\mathrm{J}}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Package Thermal Resistance, SO-16: <br> Junction-to-Case, R ®Jc <br> Junction-to-Ambient, R ®JA |  | $\begin{gathered} 28 \\ 115 \end{gathered}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance, SO-24L: Junction-to-Case, R ®Jc Junction-to-Ambient, R ®JA |  | $\begin{aligned} & 9.0 \\ & 55 \end{aligned}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Symbol | Pin Name | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | Isink |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | IC Power Input | 16 V | -0.3 V | N/A | 1.5 A peak 200 mA DC |
| COMP1, COMP2 | Compensation Capacitor for Channel 1 or 2 | 4.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $\mathrm{V}_{\mathrm{FB} 1}, \mathrm{~V}_{\mathrm{FB} 2}$ | Voltage Feedback Input for Channel 1 or 2 | 5.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| BST | Power Input for GATE(H)1, 2 | 20 V | -0.3 V | N/A | 1.5 A peak 200 mA DC |
| Rosc | Oscillator Resistor | 4.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| GATE(H)1, GATE(H)2 | High-Side FET Driver for Channel 1 or 2 | 20 V | -0.3 V | 1.5 A peak 200 mA DC | 1.5 A peak 200 mA DC |
| GATE(L)1, GATE(L)2 | Low-Side FET Driver for Channel 1 or 2 | 16 V | -0.3 V | 1.5 A peak 200 mA DC | 1.5 A peak 200 mA DC |
| GND | Ground | 0 V | 0 V | 1.5 A peak 200 mA DC | N/A |
| IS+1, IS+2 | Positive Current Sense for Channel 1 or 2 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| IS-1, IS-2 | Negative Current Sense for Channel 1 or 2 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}\right.$; $\mathrm{R}_{\mathrm{OSC}}=30.9 \mathrm{k}, \mathrm{C}_{\mathrm{COMP} 1,2}=0.1 \mu \mathrm{~F}$, $10.8 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<13.2 \mathrm{~V} ; 10.8 \mathrm{~V}<\mathrm{BST}<20 \mathrm{~V}, \mathrm{C}_{\mathrm{GATE}(\mathrm{H}) 1,2}=\mathrm{C}_{\mathrm{GATE}}(\mathrm{L}) 1,2=1.0 \mathrm{nF}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Error Amplifier |  |  |  |  |  |
| $\mathrm{V}_{\text {FB1 }}$ (2) Bias Current | $\mathrm{V}_{\mathrm{FB} 1(2)}=0 \mathrm{~V}$ | - | 0.5 | 1.6 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {FB1 } 12)}$ Input Range | - | 0 | - | 1.1 | V |
| COMP1,2 Source Current | COMP1,2 = 1.2 V to 2.5 $\mathrm{V} ; \mathrm{V}_{\mathrm{FB} 1(2)}=0.8 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP1,2 Sink Current | $\mathrm{COMP1}, 2=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB} 1(2)}=1.2 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Reference Voltage 1(2) | COMP1 $=\mathrm{V}_{\mathrm{FB} 1} ;$ COMP2 $=\mathrm{V}_{\mathrm{FB} 2}$ | 0.980 | 1.000 | 1.020 | V |
| COMP1,2 Max Voltage | $\mathrm{V}_{\mathrm{FB} 1(2)}=0.8 \mathrm{~V}$ | 3.0 | 3.3 | - | V |
| COMP1,2 Min Voltage | $\mathrm{V}_{\mathrm{FB} 1(2)}=1.2 \mathrm{~V}$ | - | 0.25 | 0.35 | V |
| Open Loop Gain | - | - | 95 | - | dB |
| Unity Gain Band Width | - | - | 40 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |
| Transconductance | - | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |

GATE(H) and GATE(L)

| High Voltage (AC) | Measure: $V_{C C}-G A T E(L) 1,2 ;$ BST - GATE(H) 1,$2 ;$ Note 2 | - | 0 | 0.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Measure:GATE(L)1,2 or GATE(H)1,2; Note 2 | - | 0 | 0.5 | V |
| Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{L}) 1,2<\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V} \\ & 1.0 \mathrm{~V}<\operatorname{GATE}(\mathrm{H}) 1,2<\mathrm{BST}-1.0 \mathrm{~V}, \\ & \mathrm{BST} \leq 14 \mathrm{~V} \end{aligned}$ | - | 20 | 50 | ns |
| Fall Time | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}-1.0>\operatorname{GATE}(\mathrm{L}) 1,2>1.0 \mathrm{~V} \\ & \mathrm{BST}-1.0>\operatorname{GATE}(\mathrm{H}) 1,2>1.0 \mathrm{~V}, \\ & \mathrm{BST} \leq 14 \mathrm{~V} \end{aligned}$ | - | 15 | 50 | ns |
| GATE(H) to GATE(L) Delay | $\begin{aligned} & \text { GATE(H) } 1,2<2.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{~L}) 1,2>2.0 \mathrm{~V} \\ & \mathrm{BST} \leq 14 \mathrm{~V} \end{aligned}$ | 20 | 40 | 70 | ns |
| GATE(L) to GATE(H) Delay | ```GATE(L)1,2 < 2.0 V, GATE(H)1,2 > 2.0 V; BST \leq 14 V``` | 20 | 40 | 70 | ns |
| GATE(H)1(2) and GATE(L)1(2) pull-down. | Resistance to GND Note 2 | 50 | 125 | 280 | $\mathrm{k} \Omega$ |

PWM Comparator

| Transient Response | COMP1,2 $=1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB1} 12)}=0$ to 1.2 V | - | 150 | 300 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| PWM Comparator Offset | $\mathrm{V}_{\text {FFB1 }}(2)$ <br> GATE(H) 1,2 , $\operatorname{Increase~COMP1,2~until~}$ | 0.30 | 0.45 | 0.60 | V |
| Artificial Ramp | Duty cycle $=50 \%$, Note 2 | 40 | 70 | 100 | mV |
| Minimum Pulse Width | Note 2 | - | - | 300 | ns |

Oscillator

| Switching Frequency | R OSC $=61.9 \mathrm{k}$; Measure GATE(H)1; Note 2 | 112 | 150 | 188 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | R OSC $=30.9 \mathrm{k}$; Measure GATE(H)1 | 224 | 300 | 376 | kHz |
| Switching Frequency | R OSC $=15.1 \mathrm{k}$; Measure GATE(H)1; Note 2 | 450 | 600 | 750 | kHz |
| ROSc Voltage | ROSC $=30.9 \mathrm{k}$, Note 2 | 0.970 | 1.000 | 1.030 | V |
| Phase Difference | - | - | 180 | - | $\circ$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}\right.$; $\mathrm{R}_{\mathrm{OSC}}=30.9 \mathrm{k}, \mathrm{C}_{\text {COMP } 1,2}=0.1 \mu \mathrm{~F}$, $10.8 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<13.2 \mathrm{~V} ; 10.8 \mathrm{~V}<\mathrm{BST}<20 \mathrm{~V}, \mathrm{C}_{\mathrm{GATE}(\mathrm{H}) 1,2}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L}) 1,2}=1.0 \mathrm{nF}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Currents |  |  |  |  |  |
| $\mathrm{V}_{\text {CC }}$ Current | COMP1,2 = 0 V (No Switching) | - | 13 | 17 | mA |
| BST Current | COMP1,2 = 0 V (No Switching) | - | 3.5 | 6.0 | mA |

## Undervoltage Lockout

| Start Threshold | GATE(H) Switching; COMP1,2 charging | 7.8 | 8.6 | 9.4 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Stop Threshold | GATE(H) not switching; COMP1,2 discharging | 7.0 | 7.8 | 8.6 | V |
| Hysteresis | Start-Stop | 0.5 | 0.8 | 1.5 | V |

## Hiccup Mode Overcurrent Protection

| OVC Comparator Offset Voltage | $0 \mathrm{~V}<\mathrm{IS}+1(2)<5.5 \mathrm{~V}, 0 \mathrm{~V}<\mathrm{IS}-1(2)<5.5 \mathrm{~V}$ | 55 | 70 | 85 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Threshold | - | 0.20 | 0.25 | 0.30 | V |
| IS+1(2) Bias Current | $0 \mathrm{~V}<\mathrm{IS}+1(2)<5.5 \mathrm{~V}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| IS-1(2) Bias Current | $0 \mathrm{~V}<\mathrm{IS}-1(2)<5.5 \mathrm{~V}$ | -1.0 | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| OVC Common Mode Range | - | 0 | - | 5.5 | V |
| OVC Latch COMP1 Discharge Current | $\mathrm{COMP1}=1.0 \mathrm{~V}$ | 2.0 | 5.0 | 8.0 | $\mu \mathrm{~A}$ |
| OVC Latch COMP2 Discharge Current | $\mathrm{COMP2}=1.0 \mathrm{~V}$ | 0.3 | 1.2 | 3.5 | mA |
| COMP1 Charge/Discharge <br> Ratio in OVC | - | 5.0 | 6.0 | 7.0 | - |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| SO-16 | SO-24L |  |  |
| 1 | 1 | GATE(H) 1 | High Side Switch FET driver pin for channel 1. |
| 2 | 2 | GATE(L)1 | Low Side Synchronous FET driver pin for channel 1. |
| 3 | - | GND | Ground pin for all circuitry contained in the IC. This pin is internally bonded to the substrate of the IC. |
| - | 3 | PGND | Ground pin for the FET drivers. |
| 4 | 4 | BST | Power input for GATE(H)1 and GATE(H)2 pins. |
| - | 5-8, 17-20 | LGND | Ground pin for the internal control circuitry. The pin is internally bonded to the substrate of the IC. |
| 5 | 9 | IS+1 | Positive input for channel 1 overcurrent comparator. |
| 6 | 10 | IS-1 | Negative input for channel 1 overcurrent comparator. |
| 7 | 11 | $\mathrm{V}_{\text {FB1 }}$ | Error amplifier inverting input for channel 1. |
| 8 | 12 | COMP1 | Channel 1 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation. The same capacitor provides Soft Start timing for channel 1. This pin also disables the channel 1 output when pulled below 0.3 V . |
| 9 | 13 | COMP2 | Channel 2 Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation and Soft Start timing for channel 2. Channel 2 output is disabled when this pin is pulled below 0.3 V . |
| 10 | 14 | $\mathrm{V}_{\text {FB2 }}$ | Error amplifier inverting input for channel 2. |
| 11 | 15 | IS-2 | Negative input for channel 2 overcurrent comparator. |
| 12 | 16 | IS+2 | Positive input for channel 2 overcurrent comparator. |
| 13 | 21 | Rosc | Oscillator frequency pin. A resistor from this pin to ground sets the oscillator frequency. |
| 14 | 22 | $\mathrm{V}_{\mathrm{CC}}$ | Input Power supply pin. |
| 15 | 23 | GATE(L)2 | Low Side Synchronous FET driver pin for channel 2. |
| 16 | 24 | GATE(H)2 | High Side Switch FET driver pin for channel 2. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

The CS5422 is a dual power supply controller that utilizes the $\mathrm{V}^{2}$ control method. Two synchronous $\mathrm{V}^{2}$ buck regulators can be built using a single controller. The fixed-frequency architecture, driven from a common oscillator, ensures a $180^{\circ}$ phase differential between channels.

## $\mathrm{V}^{2}$ Control Method

The $V^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. The $\mathrm{V}^{2}$ method differs from traditional techniques such as voltage mode control, which generates an artificial ramp, and current mode control, which generates a ramp using the inductor current.


Figure 3. ${ }^{\mathbf{2}}$ Control with Slope Compensation
The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage generates both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output, regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, allowing the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A variation in line voltage changes the current ramp in the inductor, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since any variation in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme offers the same advantages in line transient response.

A variation in load current will affect the output voltage, modifying the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. The comparator response time and the transition speed of the main switch determine the load transient response. Unlike traditional control methods, the reaction
time to the output load step is not related to the crossover frequency of the error signal loop.

The error signal loop can have a low crossover frequency, since the transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation is drastically improved because there are two independent control loops. A voltage mode controller relies on the change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulations. A current mode controller maintains a fixed error signal during line transients, since the slope of the ramp signal changes in this case. However, regulation of load transients still requires a change in the error signal. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.
The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope in the output ripple can lead to pulse width jitter and variation caused by both random and synchronous noise. A ramp waveform generated in the oscillator is added to the ramp signal from the output voltage to provide the proper voltage ramp at the beginning of each switching cycle. This slope compensation increases the noise immunity particularly at higher duty cycle (above 50\%).

## Start Up

The CS5422 features a programmable Soft Start function, which is implemented through the Error Amplifier and the external Compensation Capacitor. This feature prevents stress to the power components and overshoot of the output voltage during start-up. As power is applied to the regulator, the CS5422 Undervoltage Lockout circuit (UVL) monitors the IC's supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ). The UVL circuit prevents the MOSFET gates from switching until $\mathrm{V}_{\mathrm{CC}}$ exceeds the 8.6 V threshold. A hysteresis function of 800 mV improves noise immunity. The Compensation Capacitor connected to the COMP pin is charged by a $30 \mu \mathrm{~A}$ current source. When the capacitor voltage exceeds the 0.45 V offset of the PWM comparator, the PWM control loop will allow switching to occur. The upper gate driver GATE $(\mathrm{H})$ is activated turning on the upper MOSFET. The current then ramps up through the main inductor and linearly powers the output capacitors and load. When the regulator output voltage exceeds the

COMP pin voltage minus the 0.45 V PWM comparator offset threshold and the artificial ramp, the PWM comparator terminates the initial pulse.


Figure 4. Idealized Waveforms

## Normal Operation

During normal operation, the duty cycle of the gate drivers remains approximately constant as the $\mathrm{V}^{2}$ control loop maintains the regulated output voltage under steady state conditions. Variations in supply line or output load conditions will result in changes in duty cycle to maintain regulation.

## Gate Charge Effect on Switching Times

When using the onboard gate drivers, the gate charge has an important effect on the switching times of the FETs. A finite amount of time is required to charge the effective capacitor seen at the gate of the FET. Therefore, the rise and fall times rise linearly with increased capacitive loading, according to the following graphs.


Figure 5. Average Rise and Fall Times

## Transient Response

The 150 ns reaction time of the control loop provides fast transient response to any variations in input voltage and output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required
level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitors during the time required to slew the inductor current. For better transient response, several high frequency and bulk output capacitors are usually used.

## Out-of-Phase Synchronization

In out-of-phase synchronization, the turn-on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel which is $180^{\circ}$ out of phase with the clock signal of the first channel.

The advantages of out-of-phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. The effect of this overlap reduction is to reduce the input filter requirement, allowing the use of smaller components. In addition, since peak current occurs during a shorter time period, emitted EMI is also reduced, thereby reducing shielding requirements.

## Overvoltage Protection

Overvoltage Protection (OVP) is provided as a result of the normal operation of the $\mathrm{V}^{2}$ control method and requires no additional external components. The control loop responds to an overvoltage condition within 150 ns , turning off the upper MOSFET and disconnecting the regulator from its input voltage. This results in a crowbar action to clamp the output voltage preventing damage to the load. The regulator remains in this state until the overvoltage condition ceases.

## Hiccup Overcurrent Protection

A lossless hiccup mode short circuit protection feature is provided on the chip. The only external component required is the COMP1 capacitor. Any overcurrent condition results in the immediate shutdown of both output phases.

A comparator between the IS+ and IS- on each output phase detects a short circuit when the voltage difference between the two pins exceeds 70 mV and sets the fault latch. The fault latch immediately turns off the error amplifier and discharges both COMP capacitors. The capacitor connected to COMP1 is discharged through a $5.0 \mu \mathrm{~A}$ current sink in order to provide timing for the reset cycle. When COMP1 has fallen below 0.25 V , a comparator resets the fault latch and error amplifier 1 begins to charge COMP1 with a $30 \mu \mathrm{~A}$ source current. When COMP1 exceeds the feedback voltage plus the PWM Comparator offset voltage, the normal switching cycle will resume.

If the short circuit condition persists through the restart cycle, the overcurrent reset cycle will repeat itself until the short circuit is removed, resulting in small hiccup output pulses while the COMP capacitor charges, as shown in Figure 6.


Figure 6. Hiccup Overcurrent Protection

## Output Enable

On/Off control of the regulator outputs can be implemented by pulling the COMP pins low. The COMP pins must be driven below the 0.45 V PWM comparator offset voltage in order to disable the switching of the GATE drivers.

## DESIGN GUIDELINES

## Definition of the design specifications

The output voltage tolerance can be affected by any or all of the following reasons:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide an output voltage that will meet the specified tolerance at the load.

The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

## Selecting Feedback Divider Resistors



Figure 7. Selecting Feedback Divider Resistors
The feedback pins ( $\mathrm{V}_{\mathrm{FB} 1(2)}$ ) are connected to external resistor dividers to set the output voltages. The error amplifier is referenced to 1.0 V and the output voltage is determined by selecting resistor divider values. Resistor R1 is selected based on a design trade-off between efficiency and output voltage accuracy. The output voltage error can be estimated due to the bias current of the error amplifier neglecting resistor tolerance:

$$
\text { Error } \%=\frac{1 \times 10^{-6} \times \mathrm{R} 1}{1} \times 100 \%
$$

R2 can be sized after R1 has been determined:

$$
\mathrm{R} 2=\mathrm{R} 1\left(\frac{\mathrm{VOUT}}{1}-1\right)
$$

## Calculating Duty Cycle

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$
\text { Duty Cycle }=\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\left(\mathrm{V}_{\mathrm{HFET}}+\mathrm{V}_{\mathrm{L}}\right)}{\mathrm{V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{LFET}}-\mathrm{V}_{\mathrm{HFET}}-\mathrm{V}_{\mathrm{L}}}
$$

where:
$\mathrm{V}_{\text {OUT }}=$ buck regulator output voltage;
$\mathrm{V}_{\mathrm{HFET}}=$ high side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$;
$\mathrm{V}_{\mathrm{L}}=$ output inductor voltage drop due to inductor wire DC resistance;
$\mathrm{V}_{\mathrm{IN}}=$ buck regulator input voltage;
$\mathrm{V}_{\mathrm{LFET}}=$ low side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$.

## Selecting the Switching Frequency

Selecting the switching frequency is a trade-off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower
frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

The value of the oscillator resistor is designed to be linearly related to the switching period. If the designer prefers not to use Figure 8 to select the necessary resistor, the following equation quite accurately predicts the proper resistance for room temperature conditions.

$$
\text { ROSC }=\frac{21700-f(S W}{2.31 \mathrm{fSW}}
$$

where:
$\mathrm{R}_{\mathrm{OSC}}=$ oscillator resistor in $\mathrm{k} \Omega$;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency in kHz .


Figure 8. Switching Frequency

## Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss.

There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due to its high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The minimum value of inductance which prevents inductor saturation or exceeding the rated FET current can be calculated as follows:

$$
\mathrm{L}_{\mathrm{MIN}}=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\mathrm{OUT}}\right) \mathrm{V}_{\mathrm{OUT}}}{\mathrm{fSW} \times \mathrm{V}_{\text {IN }}(\mathrm{MIN}) \times \operatorname{ISW}(\mathrm{MAX})}
$$

where:
$\mathrm{L}_{\mathrm{MIN}}=$ minimum inductance value;
$\mathrm{V}_{\mathrm{IN}(\mathrm{MIN})}=$ minimum design input voltage;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency;
$\mathrm{I}_{\text {SW (MAX) }}$ - maximum design switch current.
The inductor ripple current can then be determined:

$$
\Delta \mathrm{I}_{\mathrm{L}}=\frac{\mathrm{V}_{\mathrm{OUT}} \times(1-\mathrm{D})}{\mathrm{L} \times \mathrm{f} \mathrm{SW}}
$$

where:
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{L}=$ inductor value;
$\mathrm{D}=$ duty cycle.
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency
The designer can now verify if the number of output capacitors will provide an acceptable output voltage ripple ( $1.0 \%$ of output voltage is common). The formula below is used:

$$
\Delta \mathrm{I}_{\mathrm{L}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\mathrm{ESR} \mathrm{MAX}^{2}}
$$

Rearranging we have:

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{I}_{\mathrm{L}}}
$$

where:
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR ;
$\Delta \mathrm{V}_{\text {OUT }}=1.0 \% \times \mathrm{V}_{\text {OUT }}=$ maximum allowable output voltage ripple ( budgeted by the designer );
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage.
The number of output capacitors is determined by:

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where:
$E S R_{\text {CAP }}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).
The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$
\mathrm{I}(\mathrm{PEAK})=\mathrm{I} O U T+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}
$$

where:
$\mathrm{I}_{\mathrm{L}(\mathrm{PEAK})}=$ inductor peak current;
$\mathrm{I}_{\text {OUT }}=$ load current;
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current.

$$
\mathrm{IL}(\mathrm{VALLEY})=\mathrm{IOUT}-\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2}
$$

where:
$\mathrm{I}_{\mathrm{L}(\mathrm{VALLEY})}=$ inductor valley current.

## Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I} \mathrm{OUT} \times\left(\frac{\mathrm{ESL}}{\Delta \mathrm{t}}+\mathrm{ESR}+\frac{\mathrm{t} \mathrm{TR}}{\mathrm{COUT}}\right)
$$

where:
$\Delta \mathrm{I}_{\text {OUT }} / \Delta \mathrm{t}=$ load current slew rate;
$\Delta \mathrm{I}_{\text {OUT }}=$ load transient;
$\Delta \mathrm{t}=$ load transient duration time;
$\mathrm{ESL}=$ Maximum allowable ESL including capacitors, circuit traces, and vias;
$\mathrm{ESR}=$ Maximum allowable ESR including capacitors and circuit traces;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time.
The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula:

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESR}}}{\Delta \mathrm{I}_{\mathrm{OUT}}}
$$

where:
$\Delta \mathrm{V}_{\mathrm{ESR}}=$ change in output voltage due to ESR (assigned by the designer)
Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula:

$$
\text { Number of capacitors }=\frac{\mathrm{ESR}_{\mathrm{CAP}}}{\mathrm{ESR} \text { MAX }}
$$

where:
$\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR.
The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$
\Delta \mathrm{V}_{\mathrm{ESR}}=\Delta \mathrm{I} \text { OUT } \times \text { ESRMAX }
$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$
\mathrm{ESL}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESL}} \times \Delta \mathrm{t}}{\Delta \mathrm{I}}
$$

## Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.
The minimum inductance value for the input inductor is therefore:

$$
\mathrm{L}_{\mathrm{IN}}=\frac{\Delta \mathrm{V}}{(\mathrm{dl} / \mathrm{dt}) \mathrm{MAX}}
$$

where:
$\mathrm{L}_{\mathrm{IN}}=$ input inductor value;
$\Delta \mathrm{V}=$ voltage seen by the input inductor during a full load swing;
$(\mathrm{dI} / \mathrm{dt})_{\mathrm{MAX}}=$ maximum allowable input current slew rate.
The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0 , a roll-off rate of $-40 \mathrm{~dB} / \mathrm{dec}$, and a corner frequency:

$$
\mathrm{f}_{\mathrm{C}}=\frac{1}{2 \pi \times \sqrt{\mathrm{LC}}}
$$

where:
$\mathrm{L}=$ input inductor;
$\mathrm{C}=$ input capacitor(s).

## SELECTION OF THE POWER FET

## FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) Its very high input impedance; and 2) Its very fast switching times. The electrical characteristics of a MOSFET are considered to be those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of $\mathrm{V}_{\mathrm{GS}}$, and the faster the turn-on time. Power dissipation in the
switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn-on switching losses, 4) turn-off switching losses, and 5) gate-transitions losses. The latter three losses are proportional to frequency.

The most important aspect of FET performance is the Static Drain-To-Source On-Resistance ( $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ ), which affects regulator efficiency and FET thermal management requirements. The On-Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On-Resistance also increases. Its positive temperature coefficient is between $+0.6 \% /{ }^{\circ} \mathrm{C}$ and $+0.85 \% /{ }^{\circ} \mathrm{C}$. The higher the On-Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used.
Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail-to-rail due to overshoot caused by the capacitive load they present to the controller IC.

## Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed $150^{\circ} \mathrm{C}$.

The maximum RMS current through the switch can be determined by the following formula:

$$
\operatorname{IRMS}(\mathrm{H})=\sqrt{\frac{\left[\begin{array}{l}
\mathrm{IL}(\mathrm{PEAK})^{2}+(\mathrm{IL}(\mathrm{PEAK}) \times \mathrm{I}(\mathrm{VALLEY})) \\
+\mathrm{IL}(\mathrm{VALLEY})^{2} \times \mathrm{D}
\end{array}\right]}{3}}
$$

where:
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{I}_{\mathrm{L}(\mathrm{PEAK})}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\mathrm{VALLEY})}=$ inductor valley current;
D = duty cycle.
Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$
\operatorname{PRMS}(\mathrm{H})=\operatorname{IRMS}(\mathrm{H})^{2} \times \operatorname{RDS}(\mathrm{ON})
$$

where:
$\mathrm{P}_{\mathrm{RMS}(\mathrm{H})}=$ switching MOSFET conduction losses;
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=$ FET drain-to-source on-resistance
The upper MOSFET switching losses are caused during
MOSFET switch-on and switch-off and can be determined by using the following formula:

$$
\begin{aligned}
\mathrm{PSWH} & =\mathrm{PSWH}(\mathrm{ON})+\mathrm{PSWH}(\mathrm{OFF}) \\
& =\frac{\mathrm{VIN}^{2} \times \mathrm{IOUT} \times(\mathrm{tRISE}+\mathrm{tFALL})}{6 \mathrm{~T}}
\end{aligned}
$$

where:
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}}(\mathrm{OFF})=$ upper MOSFET switch-off losses;
$\mathrm{V}_{\text {IN }}=$ input voltage;
$\mathrm{I}_{\text {OUT }}=$ load current;
$t_{\text {RISE }}=$ MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{t}_{\mathrm{FALL}}=$ MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{T}=1 / \mathrm{f}_{\mathrm{SW}}=$ period.
The total power dissipation in the switching MOSFET can then be calculated as:
PHFET(TOTAL) $=\operatorname{PRMS}(\mathrm{H})+\operatorname{PSWH}(\mathrm{ON})+\mathrm{PSWH}(\mathrm{OFF})$
where:
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) MOSFET losses;
$\mathrm{P}_{\text {RMS }(\mathrm{H})}=$ upper MOSFET switch conduction Losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}}^{(\text {OFF })}$ = upper MOSFET switch-off losses;
Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$
T_{J}=T_{A}+\left[\operatorname{PHFET}(T O T A L) \times R_{\Theta J A}\right]
$$

where:
$\mathrm{T}_{\mathrm{J}}=\mathrm{FET}$ junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) FET losses;
$\mathrm{R}_{\Theta \mathrm{JA}}=$ upper FET junction-to-ambient thermal resistance.

## Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$
\begin{aligned}
\operatorname{PRMS}(\mathrm{L}) & =\mathrm{I}_{\mathrm{RMS}}{ }^{2} \times \mathrm{RDS}(\mathrm{ON}) \\
& =[\mathrm{IOUT} \times \sqrt{(1-\mathrm{D})}]^{2} \times \mathrm{R} \mathrm{DS}(\mathrm{ON})
\end{aligned}
$$

where:
$\mathrm{P}_{\mathrm{RMS}(\mathrm{L})}=$ lower MOSFET conduction losses;
IOUT = load current;
D = Duty Cycle;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=$ lower FET drain-to-source on-resistance.
The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non-overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$
\text { PSWL }=\mathrm{V}_{\mathrm{SD}} \times \mathrm{I}_{\mathrm{LOAD}} \times \text { non-overlap time } \times \mathrm{fSW}
$$

where:
$\mathrm{P}_{\text {SWL }}=$ lower FET switching losses;
$\mathrm{V}_{\mathrm{SD}}=$ lower FET source-to-drain voltage;
$\mathrm{I}_{\text {LOAD }}=$ load current;
Non-overlap time $=\operatorname{GATE}(\mathrm{L})$-to-GATE(H) or GATE(H)-to-GATE(L) delay (from CS5422 data sheet Electrical Characteristics section);
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency.
The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$
\text { PLFET(TOTAL) }=\operatorname{PRMS}(\mathrm{L})+\operatorname{PSWL}
$$

where:
$P_{\text {LFET (TOTAL) }}=$ Synchronous (lower) FET total losses;
$P_{\text {RMS(L) }}=$ Switch Conduction Losses;
$P_{\text {SWL }}=$ Switching losses.
Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$
\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\mathrm{A}}+\left[\text { PLFET }(\mathrm{TOTAL}) \times \mathrm{R}_{\Theta \mathrm{JA}}\right]
$$

where:
$\mathrm{T}_{\mathrm{J}}=$ MOSFET junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$P_{\text {LFET(TOTAL) }}=$ total synchronous (lower) FET losses;
$\mathrm{R}_{\Theta \mathrm{JA}}=$ lower FET junction-to-ambient thermal resistance.

## Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, $\mathrm{V}_{\mathrm{CC}}$, and the CS5422 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:

$$
\begin{aligned}
\operatorname{PCONTROL}(\mathrm{IC}) & =\operatorname{ICC1} \mathrm{V}_{\mathrm{CC} 1}+\operatorname{IBST} \mathrm{V}_{\mathrm{BST}}+\operatorname{PGATE}(\mathrm{H}) 1 \\
& +\operatorname{PGATE}(\mathrm{L}) 1+\operatorname{PGATE}(\mathrm{H}) 2+\operatorname{PGATE}(\mathrm{L}) 2
\end{aligned}
$$

where:
$\mathrm{P}_{\text {CONTROL(IC) }}=$ control IC power dissipation;
$\mathrm{I}_{\mathrm{CC} 1}=\mathrm{IC}$ quiescent supply current;
$\mathrm{V}_{\mathrm{CC} 1}=\mathrm{IC}$ supply voltage;
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{P}_{\text {GATE }(\mathrm{L})}=$ lower MOSFET gate driver (IC) losses.
The upper (switching) MOSFET gate driver (IC) losses are:

$$
\left.\operatorname{PGATE}(\mathrm{H})=\text { QGATE }^{\mathrm{P}} \mathrm{H}\right) \times \mathrm{fSW} \times \mathrm{V}_{\mathrm{BST}}
$$

where:
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{H})}=$ total upper MOSFET gate charge at $\mathrm{V}_{\mathrm{CC}}$;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency;
The lower (synchronous) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{L})=\mathrm{Q}_{\mathrm{GATE}}(\mathrm{~L}) \times \mathrm{fSW} \times \mathrm{V}_{\mathrm{CC}}
$$

where:
$\mathrm{P}_{\text {GATE(L) }}=$ lower MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{L})}=$ total lower MOSFET gate charge at $\mathrm{V}_{\mathrm{CC}}$;
$\mathrm{f}_{\mathrm{SW}}=$ switching frequency;

The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

## Current Sensing

The current supplied to the load can be sensed easily using the IS+ and IS- pins for the output. These pins sense a voltage, proportional to the output current, and compare it to a fixed internal voltage threshold. When the differential voltage exceeds 70 mV , the internal overcurrrent protection system goes into hiccup mode. Two methods for sensing the current are available.
Sense Resistor. A sense resistor can be added in series with the inductor. When the voltage drop across the sense resistor exceeds the internal voltage threshold of 70 mV , a fault condition is set.
The sense resistor is selected according to:

$$
\text { RSENSE }=\frac{0.070 \mathrm{~V}}{\text { ILIMIT }}
$$

In a high current supply, the sense resistor will be a very low value, typically less than $10 \mathrm{~m} \Omega$. Such a resistor can be either a discrete component or a PCB trace. The resistance value of a discrete component can be more precise than a PCB trace, but the cost is also greater.

Setting the current limit using an external sense resistor is very precise because all the values can be designed to specific tolerances. However, the disadvantage of using a sense resistor is its additional constant power loss and heat generation.
Inductor ESR. Another means of sensing current is to use the intrinsic resistance of the inductor. A model of an inductor reveals that the windings of an inductor have an effective series resistance (ESR).

The voltage drop across the inductor ESR can be measured with a simple parallel circuit: an RC integrator. If the value of $\mathrm{R}_{\mathrm{S} 1}$ and C are chosen such that:

$$
\frac{L}{E S R}=R_{S 1} C
$$

then the voltage measured across the capacitor C will be:

$$
\mathrm{V}_{\mathrm{C}}=\mathrm{ESR} \times \mathrm{ILIM}
$$

Selecting Components. Select the capacitor C first. A value of $0.1 \mu \mathrm{~F}$ is recommended. The value of $\mathrm{R}_{\mathrm{S} 1}$ can be selected according to:

$$
\mathrm{RS}_{1}=\frac{1}{\mathrm{ESR} \times \mathrm{C}}
$$

Typical values for inductor ESR range in the low m; consult manufacturer's datasheet for specific details.

Selection of components at these values will result in a current limit of:


Figure 9. Inductor ESR Current Sensing
Given an ESR value of $3.5 \mathrm{~m} \Omega$, the current limit becomes 20 A . If an increased current limit is required, a resistor divider can be added.

The advantages of setting the current limit by using the winding resistance of the inductor are that efficiency is maximized and heat generation is minimized. The tolerance of the inductor ESR must be factored into the design of the current limit. Finally, one or two more components are required for this approach than with resistor sensing.

## Adding External Slope Compensation

Today's voltage regulators are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that very little voltage ramp exists at the control IC feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ), resulting in increased regulator sensitivity to noise and the potential for loop instability. In applications where the internal slope compensation is insufficient, the performance of the CS5422-based regulator can be improved through the addition of a fixed amount of external slope compensation at the output of the PWM Error Amplifier (the COMP pin) during the regulator off-time. Referring to Figure 8, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1 and R2.
$\mathrm{V}_{\text {SLOPECOMP }}=\mathrm{V}_{\text {GATE }}(\mathrm{L}) \times\left(\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}\right) \times\left(1-\mathrm{e}^{\frac{-\mathrm{t}}{\tau}}\right)$
where:
$\mathrm{V}_{\text {SLOPECOMP }}=$ amount of slope added;
$\mathrm{V}_{\text {GATE(L) }}=$ lower MOSFET gate voltage;
R1, R2 = voltage divider resistors;
$\mathrm{t}=\mathrm{t}_{\mathrm{ON}}$ or $\mathrm{t}_{\mathrm{OFF}}$ (switch off-time);
$\tau=\mathrm{RC}$ constant determined by C 1 and the parallel combination of R1, R2 neglecting the low driver output impedance.


Figure 10. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On-Time Cycle
The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off-time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin. Also, C1 should be very small (less than a few nF ) to avoid heating the part.

## EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

## LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS5422.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double-sided PCB's a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCB's are usually sufficient for a good layout, four-layer PCB's are the
optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layers for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the COMP capacitor as close as possible to the COMP pin.
12. Connect the filter components of the following pins: $\mathrm{R}_{\mathrm{OSC}}, \mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}$, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
13. Place the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitors as close as possible to the IC.
14. Place the $\mathrm{R}_{\text {OSC }}$ resistor as close as possible to the $\mathrm{R}_{\mathrm{OSC}} \mathrm{pin}$.
15. Include provisions for $100-100 \mathrm{pF}$ capacitor across each resistor of the feedback network to improve noise immunity and add COMP.
16. Assign the output with lower duty cycle to channel 2, which has better noise immunity.

## MC34060A, MC33060A

## Fixed Frequency, PWM, Voltage Mode Single Ended Controllers

The MC34060A is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single-ended SWITCHMODE ${ }^{T M}$ power supply control.

The MC34060A is specified over the commercial operating temperature range of $0^{\circ}$ to $+70^{\circ} \mathrm{C}$, and the MC33060A is specified over an automotive temperature range of $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$.

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference, 1.5\% Accuracy
- Adjustable Dead-Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout

PIN CONNECTIONS

(Top View)


ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com
MARKING
DIAGRAMS


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1678 of this data sheet.

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 42 | V |
| Collector Output Voltage | $\mathrm{V}_{\mathrm{C}}$ | 42 | V |
| Collector Output Current (Note 1) | $\mathrm{I}_{\mathrm{C}}$ | 500 | mA |
| Amplifier Input Voltage Range | $\mathrm{V}_{\text {in }}$ | -0.3 to +42 | V |
| Power Dissipation @ $\mathrm{T}_{\mathrm{A}} \leq 45^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | 1000 | mW |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range <br> For MC34060A <br> For MC33060A | $\mathrm{T}_{\mathrm{A}}$ | 0 to +70 <br> -40 to +85 | ${ }^{\circ} \mathrm{C}$ |

## THERMAL CHARACTERISTICS

| Characteristics | Symbol | P Suffix <br> Package | D Suffix <br> Package | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {өJA }}$ | 80 | 120 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Derating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | 45 | 45 | ${ }^{\circ} \mathrm{C}$ |

RECOMMENDED OPERATING CONDITIONS

| Condition/Value | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 7.0 | 15 | 40 | V |
| Collector Output Voltage | $\mathrm{V}_{\mathrm{C}}$ | - | 30 | 40 | V |
| Collector Output Current | $\mathrm{I}_{\mathrm{C}}$ | - | - | 200 | mA |
| Amplifier Input Voltage | $\mathrm{V}_{\text {in }}$ | -0.3 | - | $\mathrm{V}_{\mathrm{CC}}-2$ | V |
| Current Into Feedback Terminal | $\mathrm{I}_{\mathrm{fb}}$ | - | - | 0.3 | mA |
| Reference Output Current | $\mathrm{I}_{\text {ref }}$ | - | - | 10 | mA |
| Timing Resistor | $\mathrm{R}_{\mathrm{T}}$ | 1.8 | 47 | 500 | $\mathrm{k} \Omega$ |
| Timing Capacitor | $\mathrm{C}_{\mathrm{T}}$ | 0.00047 | 0.001 | 10 | $\mu \mathrm{~F}$ |
| Oscillator Frequency | $\mathrm{f}_{\text {osc }}$ | 1.0 | 25 | 200 | kHz |
| PWM Input Voltage (Pins 3 and 4) | - | -0.3 | - | 5.3 | V |

1. Maximum thermal limits must be observed.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{C C}=15 \mathrm{~V}, \mathrm{C}_{T}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right.$, unless otherwise noted. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| $\begin{gathered} \text { Reference Voltage }\left(\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}} 25^{\circ} \mathrm{C}\right) \\ \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}-\mathrm{MC} 34060 \mathrm{~A} \\ -\mathrm{MC} 33060 \mathrm{~A} \end{gathered}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{gathered} 4.925 \\ 4.9 \\ 4.85 \end{gathered}$ | 5.0 | $\begin{gathered} 5.075 \\ 5.1 \\ 5.1 \end{gathered}$ | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~mA}$ ) | Regline | - | 2.0 | 25 | mV |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 2.0 | 15 | mV |
| Short Circuit Output Current ( $\mathrm{V}_{\text {ref }}=0 \mathrm{~V}$ ) | Isc | 15 | 35 | 75 | mA |

OUTPUT SECTION

| Collector Off-State Current ( $\mathrm{V}_{\text {CC }}=40 \mathrm{~V}, \mathrm{~V}_{\text {CE }}=40 \mathrm{~V}$ ) | $\mathrm{I}_{\text {(off) }}$ | - | 2.0 | 100 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Emitter Off-State Current ( $\left.\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{E}}=0 \mathrm{~V}\right)$ | $\mathrm{IE}_{\text {(off) }}$ | - | - | -100 | $\mu \mathrm{A}$ |
| ```Collector-Emitter Saturation Voltage (Note 2) Common-Emitter \(\left(\mathrm{V}_{\mathrm{E}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=200 \mathrm{~mA}\right)\) Emitter-Follower \(\left(\mathrm{V}_{\mathrm{C}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{E}}=-200 \mathrm{~mA}\right)\)``` | $\begin{aligned} & \mathrm{V}_{\text {sat }(\mathrm{C})} \\ & \mathrm{V}_{\text {sat(E) }} \end{aligned}$ | - | $1.1$ $1.5$ | $1.5$ $2.5$ | V |
| Output Voltage Rise Time ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13) | $\mathrm{t}_{\mathrm{r}}$ | - | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | ns |
| Output Voltage Fall Time ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13) | $\mathrm{tr}_{r}$ | - | 40 40 | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | ns |

ERROR AMPLIFIER SECTION

| Input Offset Voltage ( $\mathrm{V}_{\text {O[Pin 3] }}=2.5 \mathrm{~V}$ ) | $\mathrm{V}_{10}$ | - | 2.0 | 10 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Current ( $\mathrm{V}_{\mathrm{C} \text { Pin 3] }}=2.5 \mathrm{~V}$ ) | 10 | - | 5.0 | 250 | nA |
| Input Bias Current ( $\mathrm{V}_{\text {O[Pin 3] }}=2.5 \mathrm{~V}$ ) | IB | - | -0.1 | -2.0 | $\mu \mathrm{A}$ |
| Input Common Mode Voltage Range $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {ICR }}$ | $\begin{gathered} 0 \text { to } \\ \mathrm{V}_{\mathrm{CC}}-2.0 \end{gathered}$ | - | - | V |
| Inverting Input Voltage Range | $\mathrm{V}_{\text {IR(INV) }}$ | $\begin{gathered} -0.3 \text { to } \\ v_{C C}-2.0 \end{gathered}$ | - | - | V |
| Open-Loop Voltage Gain $\left(\Delta \mathrm{V}_{\mathrm{O}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0.5 \mathrm{~V} \text { to } 3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right)$ | Avol | 70 | 95 | - | dB |
| Unity-Gain Crossover Frequency $\left(\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}\right.$ to $\left.3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right)$ | $\mathrm{f}_{\mathrm{c}}$ | - | 600 | - | kHz |
| Phase Margin at Unity-Gain $\left(\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V} \text { to } 3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right)$ | $\phi_{m}$ | - | 65 | - | deg. |
| Common Mode Rejection Ratio $\left.\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0 \mathrm{~V} \text { to } 38 \mathrm{~V}\right)\right)$ | CMRR | 65 | 90 | - | dB |
| Power Supply Rejection Ratio $\left(\Delta \mathrm{V}_{\mathrm{CC}}=33 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=2.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right)$ | PSRR | - | 100 | - | dB |
| Output Sink Current ( $\mathrm{V}_{\text {O[Pin 3] }}=0.7 \mathrm{~V}$ ) | $\mathrm{I}^{-}$ | 0.3 | 0.7 | - | mA |
| Output Source Current ( $\mathrm{V}_{\text {O[Pin 3] }}=3.5 \mathrm{~V}$ ) | $\mathrm{l}^{+}$ | -2.0 | -4.0 | - | mA |

2. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.
$\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}$ for MC33060A
$\mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$ for MC33060A
$=0^{\circ} \mathrm{C}$ for MC34060A
$=+70^{\circ} \mathrm{C}$ for MC34060 A

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right.$, unless otherwise noted.
For typical values $T_{A}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | | PWM COMPARATOR SECTION (Test circuit Figure 11) | $\mathrm{V}_{\text {TH }}$ | - | 3.5 | 4.5 |
| :--- | :---: | :---: | :---: | :---: |
| Input Threshold Voltage <br> (Zero Duty Cycle) | $\mathrm{I}_{1}$ | 0.3 | 0.7 | - |
| Input Sink Current <br> $\left(\mathrm{V}_{[\text {Pin 3] }}=0.7 \mathrm{~V}\right)$ | mA |  |  |  |

DEAD-TIME CONTROL SECTION (Test circuit Figure 11)

| Input Bias Current (Pin 4) <br> $\left(V_{\text {in }}=0 \mathrm{~V}\right.$ to 5.25 V$)$ | $\mathrm{I}_{\mathrm{B}(\mathrm{DT})}$ | - | -1.0 | -10 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum Output Duty Cycle <br> $\left(\mathrm{V}_{\text {in }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right)$ <br> $\left(\mathrm{V}_{\text {in }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=47 \mathrm{k} \Omega\right)$ | $\mathrm{DC}_{\max }$ |  |  |  |  |
| Input Threshold Voltage (Pin 4) <br> (Zero Duty Cycle) <br> (Maximum Duty Cycle) |  | - | 90 | 100 | $\%$ |

OSCILLATOR SECTION

| $\begin{aligned} & \text { Frequency } \\ & \left(\mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}-\mathrm{MC} 34060 \mathrm{~A} \\ & \left(\mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{MC} 3060 \mathrm{~A}, \mathrm{R}_{\mathrm{T}}=47 \mathrm{k} \Omega\right) \end{aligned}$ | $\mathrm{f}_{\text {osc }}$ | $\begin{aligned} & 9.7 \\ & 9.5 \\ & 9.0 \\ & - \end{aligned}$ | $\begin{gathered} 10.5 \\ - \\ - \\ 25 \end{gathered}$ | $\begin{gathered} 11.3 \\ 11.5 \\ 11.5 \\ - \end{gathered}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Standard Deviation of Frequency* $\left(\mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=47 \mathrm{k} \Omega\right)$ | $\sigma f_{\text {osc }}$ | - | 1.5 | - | \% |
| Frequency Change with Voltage $\left(\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V} \text { to } 40 \mathrm{~V}\right)$ | $\Delta \mathrm{f}_{\text {osc }}(\Delta \mathrm{V})$ | - | 0.5 | 2.0 | \% |
| Frequency Change with Temperature $\begin{aligned} & \left(\Delta \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}\right) \\ & \left(\mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right) \end{aligned}$ | $\Delta \mathrm{f}_{\text {osc }}(\Delta \mathrm{T})$ | - | 4.0 | - | \% |

UNDERVOLTAGE LOCKOUT SECTION

| Turn-On Threshold ( $\mathrm{V}_{\text {CC }}$ increasing, $\mathrm{I}_{\text {ref }}=1.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {th }}$ | 4.0 | 4.7 | 5.5 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Hysteresis | $\mathrm{V}_{\mathrm{H}}$ | 50 | 150 | 300 | mV |

TOTAL DEVICE

| Standby Supply Current <br> (Pin 6 at $\mathrm{V}_{\text {ref }}$ all other inputs and outputs open) $\begin{aligned} & \left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}\right) \end{aligned}$ | ICC | - | $\begin{aligned} & 5.5 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Average Supply Current $\left(\mathrm{V}_{[\text {Pin 4] }}=2.0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=47 \mathrm{k} \Omega\right)$. See Figure 11 . | Is | - | 7.0 | - | mA |




Figure 1. Block Diagram

## Description

The MC34060A is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal-linear sawtooth oscillator is frequency-programmable by two external components, $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. The approximate oscillator frequency is determined by:

$$
f_{\mathrm{osc}} \cong \frac{1.2}{R_{T} \cdot C_{T}}
$$

For more information refer to Figure 3.


Figure 2. Timing Diagram

## MC34060A, MC33060A

## APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feed-back input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first $4 \%$ of the sawtooth-cycle time. This would result in a maximum duty cycle of $96 \%$. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 V to 3.3 V .

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback
pin varies from 0.5 V to 3.5 V . Both error amplifiers have a common mode input range from -0.3 V to $\left(\mathrm{V}_{\mathrm{CC}}-2.0 \mathrm{~V}\right)$, and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.
The MC34060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of $\pm 5 \%$ with a typical thermal drift of less than 50 mV over an operating temperature range of $0^{\circ}$ to $+70^{\circ} \mathrm{C}$.


Figure 3. Oscillator Frequency versus Timing Resistance


Figure 5. Percent Deadtime versus Oscillator Frequency


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current


Figure 4. Open Loop Voltage Gain and Phase versus Frequency


Figure 6. Percent Duty Cycle versus
Dead-Time Control Voltage


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current


Figure 9. Standby Supply Current versus Supply Voltage


Figure 11. Error Amplifier Characteristics


Figure 13. Common-Emitter Configuration and Waveform


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current


Figure 12. Deadtime and Feedback Control


Figure 14. Emitter-Follower Configuration and Waveform


Figure 15. Error Amplifier Sensing Techniques


Figure 16. Deadtime Control Circuit


Figure 17. Soft-Start Circuit


Figure 18. Slaving Two or More Control Circuits


| Test | Conditions | Results |
| :--- | :--- | :---: |
| Line Regulation | $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | $25 \mathrm{mV} \quad 0.5 \%$ |
| Load Regulation | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 1.0 A | $3.0 \mathrm{mV} \quad 0.06 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | 75 mV p-p P.A.R.D. |
| Short Circuit Current | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 1.6 A |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | $73 \%$ |

Figure 19. Step-Down Converter with Soft-Start and Output Current Limiting

MC34060A, MC33060A


| Test | Conditions | Results |
| :--- | :--- | :---: |
| Line Regulation | $\mathrm{V}_{\mathrm{in}}=8.0 \mathrm{~V}$ to $26 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.5 \mathrm{~A}$ | $40 \mathrm{mV} \quad 0.14 \%$ |
| Load Regulation | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 0.5 A | $5.0 \mathrm{mV} \quad 0.18 \%$ |
| Output Ripple | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.5 \mathrm{~A}$ | 24 mV p-p P.A.R.D. |
| Efficiency | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.5 \mathrm{~A}$ | $75 \%$ |

*Optional circuit to minimize output ripple

Figure 20. Step-Up Converter


| Test | Conditions | Results |
| :--- | :--- | :---: |
| Line Regulation | $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$ | $52 \mathrm{mV} \quad 0.35 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0$ to 250 mA | $47 \mathrm{mV} \quad 0.32 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$ | 10 mV p-p P.A.R.D. |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 330 mA |
| Efficiency | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$ | $86 \%$ |

*Optional circuit to minimize output ripple

Figure 21. Step-Up/Down Voltage Inverting Converter with Soft-Start and Current Limiting


Figure 22. 33 W Off-Line Flyback Converter with Soft-Start and Primary Power Limiting

## MC34060A, MC33060A

ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: |
| MC34060AD | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| MC34060ADR2 |  | SO-14 | 2500 Tape \& Reel |
| MC34060AP |  | PDIP-14 | 25 Units/Rail |
| MC33060AD | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| MC33060ADR2 |  | SO-14 | 2500 Tape \& Reel |
| MC33060AP |  | PDIP-14 | 25 Units/Rail |

## MC34023, MC33023

## High Speed Single-Ended PWM Controller

The MC34023 series are high speed, fixed frequency, single-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost-effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Output
- High Current Totem Pole Output
- Wide Bandwidth Error Amplifier
- Fully-Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle-By-Cycle Current Limiting
- Soft-Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up Current (500 $\mu \mathrm{A}$ Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- $90 \%$ Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3823


This device contains 176 active transistors.
Figure 1. Simplified Application

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 30 | V |
| Output Driver Supply Voltage | $\mathrm{V}_{\mathrm{C}}$ | 20 | V |
| ```Output Current, Source or Sink (Note 1) DC Pulsed ( \(0.5 \mu \mathrm{~s}\) )``` | 10 | $\begin{aligned} & 0.5 \\ & 2.0 \end{aligned}$ | A |
| Current Sense, Soft-Start, Ramp, and Error Amp Inputs | $\mathrm{V}_{\text {in }}$ | -0.3 to +7.0 | V |
| Error Amp Output and Soft-Start Sink Current | lo | 10 | mA |
| Clock and $\mathrm{R}_{\mathrm{T}}$ Output Current | Ico | 5.0 | mA |
| Power Dissipation and Thermal Characteristics SO-16L Package (Case 751G) <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> DIP Package (Case 648) <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ | $\begin{aligned} & 862 \\ & 145 \\ & \\ & 1.25 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | TJ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 2) <br> MC34023 <br> MC33023 | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+105 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=3.65 \mathrm{k} \Omega, \mathrm{C}_{T}=1.0 \mathrm{nF}\right.$, for typical values $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| Reference Output Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {ref }}$ | 5.05 | 5.1 | 5.15 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 30 V ) | Regline | - | 2.0 | 15 | mV |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 2.0 | 15 | mV |
| Temperature Stability | $\mathrm{T}_{\text {S }}$ | - | 0.2 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {ref }}$ | 4.95 | - | 5.25 | V |
| Output Noise Voltage ( $\mathrm{f}=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $V_{n}$ | - | 50 | - | $\mu \mathrm{V}$ |
| Long Term Stability ( $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ for 1000 Hours) | S | - | 5.0 | - | mV |
| Output Short Circuit Current | ISC | -30 | -65 | -100 | mA |

## OSCILLATOR SECTION

| Frequency $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ <br> Line ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 30 V ) and Temperature ( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ ) | $\mathrm{f}_{\text {osc }}$ | $\begin{aligned} & 380 \\ & 370 \end{aligned}$ | $\begin{aligned} & 400 \\ & 400 \\ & \hline \end{aligned}$ | $\begin{aligned} & 420 \\ & 430 \end{aligned}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 30 V ) | $\Delta \mathrm{f}_{\text {osc }} / \Delta \mathrm{V}$ | - | 0.2 | 1.0 | \% |
| Frequency Change with Temperature ( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ ) | $\Delta \mathrm{f}_{\text {osc }} / \Delta \mathrm{T}$ | - | 2.0 | - | \% |
| Sawtooth Peak Voltage | $\mathrm{V}_{\text {OSC(P) }}$ | 2.6 | 2.8 | 3.0 | V |
| Sawtooth Valley Voltage | Vosc(V) | 0.7 | 1.0 | 1.25 | V |
| Clock Output Voltage High State Low State | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | 3.9 | 4.5 2.3 | $\stackrel{-}{2.9}$ | V |

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34023
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34023
$=-40^{\circ} \mathrm{C}$ for MC33023
$=+105^{\circ} \mathrm{C}$ for MC33023

## MC34023, MC33023

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=3.65 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER SECTION |  |  |  |  |  |
| Input Offset Voltage | $\mathrm{V}_{10}$ | - | - | 15 | mV |
| Input Bias Current | IIB | - | 0.6 | 3.0 | $\mu \mathrm{A}$ |
| Input Offset Current | $\mathrm{I}_{10}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Open-Loop Voltage Gain ( $\mathrm{V}_{\mathrm{O}}=1.0 \mathrm{~V}$ to 4.0 V ) | AvoL | 60 | 95 | - | dB |
| Gain Bandwidth Product ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | GBW | 4.0 | 8.3 | - | MHz |
| Common Mode Rejection Ratio ( $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ to 5.5 V ) | CMRR | 75 | 95 | - | dB |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 30 V ) | PSRR | 85 | 110 | - | dB |
| Output Current, Source ( $\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{~V}$ ) <br> Sink $\left(V_{O}=1.0 \mathrm{~V}\right)$ | I Source $I_{\text {sink }}$ | $\begin{aligned} & 0.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.6 \end{aligned}$ | - | mA |
| Output Voltage Swing, High State $\left(\mathrm{I}_{\mathrm{O}}=-0.5 \mathrm{~mA}\right)$ <br> Low State ( $\mathrm{I}_{\mathrm{O}}=1 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{OH}}$ $\mathrm{V}_{\mathrm{OL}}$ | $\begin{gathered} 4.5 \\ 0 \end{gathered}$ | $\begin{gathered} 4.75 \\ 0.4 \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 1.0 \end{aligned}$ | V |
| Slew Rate | SR | 6.0 | 12 | - | V/us |

## PWM COMPARATOR SECTION

| Ramp Input Bias Current | $\mathrm{I}_{\mathrm{IB}}$ | - | -0.5 | -5.0 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Duty Cycle, Maximum | $\mathrm{DC}_{(\max )}$ | 80 | 90 | - | $\%$ |
| Minimum | $\mathrm{DC}_{(\min )}$ | - | - | 0 |  |
| Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) =0 V) | $\mathrm{V}_{\text {th }}$ | 1.1 | 1.25 | 1.4 | V |
| Propagation Delay (Ramp Input to Output, $\left.\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | tpLH(in/out) | - | 60 | 100 | ns |

## SOFT-START SECTION

| Charge Current $\left(\mathrm{V}_{\text {Soft-Start }}=0.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {chg }}$ | 3.0 | 9.0 | 20 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Discharge Current $\left(\mathrm{V}_{\text {Soft-Start }}=1.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {dischg }}$ | 1.0 | 4.0 | - | mA |

CURRENT SENSE SECTION

| Input Bias Current (Pin 9(12) $=0$ V to 4.0 V) | $\mathrm{I}_{\mathrm{IB}}$ | - | - | 15 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Current Limit Comparator Input Offset Voltage (Pin 11(14) $=1.1 \mathrm{~V})$ | $\mathrm{V}_{\mathrm{IO}}$ | - | - | 45 | mV |
| Current Limit Reference Input Common Mode Range (Pin 11(14)) | $\mathrm{V}_{\mathrm{CMR}}$ | 1.0 | - | 1.25 | V |
| Shutdown Comparator Threshold | $\mathrm{V}_{\text {th }}$ | 1.25 | 1.40 | 1.55 | V |
| Propagation Delay (Current Limit/Shutdown to Output, $\left.\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\text {PLH(in/out) }}$ | - | 50 | 80 | ns |

## OUTPUT SECTION

| Output Voltage |  |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Low State$\left(I_{\text {Sink }}=20 \mathrm{~mA}\right)$ <br> $\left(\mathrm{I}_{\text {Sink }}=200 \mathrm{~mA}\right)$ <br> High State <br> $\left(\mathrm{I}_{\text {Source }}=20 \mathrm{~mA}\right)$ <br> $\left(\mathrm{V}_{\text {Source }}=200 \mathrm{~mA}\right)$ |  | - | 0.25 | 0.4 |  |
| Output Voltage with UVLO Activated $\left(\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{I}_{\text {Sink }}=0.5 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ | 13 | 1.2 | 2.2 |  |
| Output Leakage Current $\left(\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}\right)$ |  | 12 | 13 | - |  |
| Output Voltage Rise Time $\left(\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{OL}(\mathrm{UVLO})}$ | - | 0.25 | 1.0 | V |
| Output Voltage Fall Time $\left(\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{L}}$ | - | 100 | 500 | $\mu \mathrm{~A}$ |

## UNDERVOLTAGE LOCKOUT SECTION

| Start-Up Threshold (VCC Increasing) | $\mathrm{V}_{\text {th }(o n)}$ | 8.8 | 9.2 | 9.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| UVLO Hysteresis Voltage ( $\mathrm{V}_{\text {CC }}$ Decreasing After Turn-On) | $\mathrm{V}_{\mathrm{H}}$ | 0.4 | 0.8 | 1.2 | V |

## TOTAL DEVICE

| Power Supply Current | ICC |  |  |  | mA |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Start-Up $(V C C=8.0 \mathrm{~V})$ |  | - | 0.5 | 1.2 |  |
| Operating |  | - | 20 | 30 |  |

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34023 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34023
$=-40^{\circ} \mathrm{C}$ for MC33023
$=+105^{\circ} \mathrm{C}$ for MC33023


Figure 2. Timing Resistor versus Oscillator Frequency


Figure 3. Oscillator Frequency versus Temperature


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

$0.1 \mu \mathrm{~s} / \mathrm{DIV}$

Figure 6. Error Amp Small Signal Transient Response


Figure 5. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

$0.1 \mu \mathrm{~s} /$ DIV
Figure 7. Error Amp Large Signal Transient Response


Figure 8. Reference Voltage Change versus Source Current

$\mathrm{V}_{\text {ref }}$ LINE REGULATION 10 V to 24 V
( $2.0 \mathrm{~ms} /$ DIV)
Figure 10. Reference Line Regulation


Figure 12. Current Limit Comparator Input Offset Voltage versus Temperature


Figure 9. Reference Short Circuit Current versus Temperature

$\mathrm{V}_{\text {ref }}$ LOAD REGULATION 1.0 mA to 10 mA
$(2.0 \mathrm{~ms} / \mathrm{DVV})$
Figure 11. Reference Load Regulation


Figure 13. Shutdown Comparator Threshold Voltage versus Temperature


Figure 14. Soft-Start Charge Current versus Temperature


OUTPUT RISE \& FALL TIME 1.0 nF LOAD $50 \mathrm{~ns} /$ DIV

Figure 16. Drive Output Rise and Fall Time


Figure 15. Output Saturation Voltage versus Load Current


OUTPUT RISE \& FALL TIME 10 nF LOAD $50 \mathrm{~ns} /$ DIV

Figure 17. Drive Output Rise and Fall Time


Figure 18. Supply Voltage versus Supply Current

## MC34023, MC33023



Figure 19. Representative Block Diagram


Figure 20. Current Limit Operating Waveforms

## OPERATING DESCRIPTION

The MC33023 and MC34023 series are high speed, fixed frequency, single-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 19.

## Oscillator

The oscillator frequency is programmed by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. The $\mathrm{R}_{\mathrm{T}}$ pin is set to a temperature compensated 3.0 V . By selecting the value of $\mathrm{R}_{\mathrm{T}}$, the charge current is set through a current mirror for the timing capacitor $\mathrm{C}_{\mathrm{T}}$. This charge current runs continuously through $\mathrm{C}_{\mathrm{T}}$. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of $90 \% . \mathrm{C}_{\mathrm{T}}$ is charged to 2.8 V and discharged to 1.0 V . During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that resets the PWM Latch and, inhibits the outputs. The threshold voltage on the oscillator comparator is trimmed to guarantee an oscillator accuracy of $5.0 \%$ at $25^{\circ} \mathrm{C}$.

Additional dead time can be added by externally increasing the charge current to $\mathrm{C}_{\mathrm{T}}$ as shown in Figure 24. This changes the charge to discharge ratio of $\mathrm{C}_{\mathrm{T}}$ which is set internally to $\mathrm{I}_{\text {charge }} / 10 \mathrm{I}_{\text {charge. }}$. The new charge to discharge ratio will be:

$$
\% \text { Deadtime }=\frac{\text { I additional }+I_{\text {charge }}}{10\left(I_{\text {charge }}\right)}
$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of $\mathrm{C}_{\mathrm{T}}$. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge $\mathrm{C}_{\mathrm{T}}$. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 28, 29 and 30 provide suggested synchronization.

## Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a gain bandwidth product of 8.3 MHz with 75 degrees of phase margin (Figure 4). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a common mode voltage $\left(\mathrm{V}_{\mathrm{CM}}\right)$ input range of 1.5 V to 5.5 V. The Error Amplifier Output is provided for external loop compensation.

## Soft-Start Latch

Soft-Start is accomplished in conjunction with an external capacitor. The Soft-Start capacitor is charged by an internal $9.0 \mu \mathrm{~A}$ current source. This capacitor clamps the
output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle. The time it takes for a capacitor to reach full charge is given by:

$$
t \approx\left(4.5 \cdot 10^{5}\right) C_{\text {Soft-Start }}
$$

A Soft-Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft-Start circuit to latch so that the Soft-Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\text {ref }}$. The second condition is when current sense input exceeds 1.4 V . Since this latch is "set dominant", it cannot be reset until either of these signals is removed and, the voltage at $\mathrm{C}_{\text {Soft-Start }}$ is less than 0.5 V .

## PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the error amplifier output voltage minus 1.25 V , the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

## Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. The reference voltage for the current limit comparator is not set internally. A pin is provided so the user can set the voltage. When the voltage at the current limit input pin exceeds the externally set voltage, the PWM latch is set, disabling the output. In this way cycle-by-cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$
\mathrm{R}_{\text {Sense }}=\frac{\mathrm{I}_{\text {Limit Reference Voltage }}}{\mathrm{I}_{\mathrm{pk}} \text { (switch) }}
$$

If the voltage at this pin exceeds 1.4 V , the second comparator is activated. This comparator sets a latch which, in turn, causes the soft start capacitor to be discharged. In this way a "hiccup" mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a "hiccup" mode is given by:

$$
I_{\text {shutdown }}=\frac{1.4 \mathrm{~V}}{\mathrm{R}_{\text {Sense }}}
$$

## Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses $\mathrm{V}_{\mathrm{CC}}$ and the second $\mathrm{V}_{\text {ref }}$. During power-up, $\mathrm{V}_{\mathrm{CC}}$ must exceed 9.2 V and $\mathrm{V}_{\text {ref }}$ must exceed 4.2 V before the outputs can be enabled and the Soft-Start latch released. If $\mathrm{V}_{\mathrm{CC}}$ falls below 8.4 V or $\mathrm{V}_{\text {ref }}$ falls below 3.6 V , the outputs are disabled and the Soft-Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off-line bootstrap start-up circuit. Typical start-up current is $500 \mu \mathrm{~A}$.

## Output

The MC34023 has a high current totem pole output specifically designed for direct drive of power MOSFETs. It is capable of up to $\pm 2.0$ A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for $\mathrm{V}_{\mathrm{C}}$ and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate $\mathrm{V}_{\mathrm{C}}$ supply input also allows the designer added flexibility in tailoring the drive voltage independent of $\mathrm{V}_{\mathrm{CC}}$.

## Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of $\pm 1.0 \%$ at $25^{\circ} \mathrm{C}$. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

## Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Shown in Figure 36 is a printed circuit layout of the application circuit. Note how the power and ground traces are run. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing for snubbing.

## Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the
current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp $\left(\mathrm{S}_{\mathrm{e}}\right)$ is added to the on-time ramp $\left(\mathrm{S}_{\mathrm{n}}\right)$ of the current-sense waveform, stability can be achieved.

One must be careful not to add too much ramp compensation. If too much is added the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figure 26 is an example of one way in which external ramp compensation can be implemented.


Figure 21. Ramp Compensation
A simple equation can be used to calculate the amount of external ramp slope necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 35 are also shown.

$$
S_{e}=\frac{V_{O}}{L}\left(\frac{N_{S}}{N_{P}}\right)\left(R_{S}\right) A_{i}
$$

$$
\begin{aligned}
& \text { where: } \begin{aligned}
& \mathrm{V}_{\mathrm{O}}= \mathrm{DC} \text { output voltage } \\
& \mathrm{N}_{\mathrm{P},} \mathrm{~N}_{\mathrm{S}}= \text { number of power transformer primary } \\
& \text { or secondary turns } \\
& \mathrm{A}_{\mathrm{i}}= \text { gain of the current sense network } \\
&\text { (see Figures } 24 \text { and } 25) \\
& \mathrm{L}= \text { output inductor } \\
& \mathrm{R}_{\mathrm{S}}= \text { current sense resistance } \\
& \\
& \text { For the application circuit: } \mathrm{S}_{\mathrm{e}}=\frac{5}{1.8 \mu}\left(\frac{2}{8}\right)(0.3)(0.55) \\
&=0.115 \mathrm{~V} / \mathrm{ms}
\end{aligned}
\end{aligned}
$$

## MC34023, MC33023

PIN FUNCTION DESCRIPTION

| Pin |  | Description |
| :---: | :---: | :---: |
| DIP/SOIC | Function |  |
| 1 | Error Amp Inverting Input | This pin is usually used for feedback from the output of the power supply. |
| 2 | Error Amp Noninverting Input | This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to $\mathrm{V}_{\text {ref }}$, however an external reference can also be used. |
| 3 | Error Amp Output | This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter. |
| 4 | Clock | This is a bidirectional pin used for synchronization. |
| 5 | $\mathrm{R}_{\mathrm{T}}$ | The value of $\mathrm{R}_{\mathrm{T}}$ sets the charge current through timing Capacitor, $\mathrm{C}_{\mathrm{T}}$. |
| 6 | $\mathrm{C}_{\mathrm{T}}$ | In conjunction with $\mathrm{R}_{\mathrm{T}}$, the timing Capacitor sets the switching frequency. |
| 7 | Ramp Input | For voltage mode operation this pin is connected to $\mathrm{C}_{\mathrm{T}}$. For current mode operation this pin is connected through a filter to the current sensing element. |
| 8 | Soft-Start | A capacitor at this pin sets the Soft-Start time. |
| 9 | Current Limit/ Shutdown | This pin has two functions. First, it provides cycle-by-cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft-Start cycle. |
| 10 | Ground | This pin is the ground for the control circuitry. |
| 11 | Current Limit Reference Input | This pin voltage sets the threshold for cycle-by-cycle current limiting. |
| 12 | Power Ground | This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry. |
| 13 | $\mathrm{V}_{\mathrm{C}}$ | This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry. |
| 14 | Output | This is a high current totem pole output. |
| 15 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the control IC. |
| 16 | $\mathrm{V}_{\text {ref }}$ | This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier. |



In voltage mode operation, the control range on the output of the Error Amplifier from 0\% to $90 \%$ duty cycle is from 2.25 V to 4.05 V .

Figure 22. Voltage Mode Operation


In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn-on of a power MOSFET.

Figure 23. Current Mode Operation


The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$
A_{i}=\frac{R_{\text {Sense }}}{\text { turns ratio }}
$$

Figure 24. Resistive Current Sensing


The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

$$
A_{i}=\frac{R_{w}}{\text { turns ratio }}
$$

Figure 25. Primary Side Current Sensing


This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor $\mathrm{C}_{1}$ provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors $R_{1}$ and $R_{2}$.

Figure 26A. Slope Compensation (Noise Sensitive)


When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor $R_{M}$ and capacitor $C_{M}$ provide the added slope necessary. By choosing $R_{M}$ and $C_{M}$ with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose $C_{M}$, then $R_{M}$ can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current $l_{M}$ can be calculated by $I_{M}=C_{M} S_{e}$. Then $R_{M}$ can be calculated by $R_{M}=V_{C C} / l_{M}$.

Figure 26B. Slope Compensation (Noise Immune)


Additional dead time can be added by the addition of a dead time resistor from $V_{\text {ref }}$ to $\mathrm{C}_{\mathrm{T}}$. See text on Oscillator section for more information.


The sync pulse fed into the clock pin must be at least 3.9 V . $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\boldsymbol{T}}$ need to be set $10 \%$ slower than the sync frequency. This circuit is also used in Voltage Mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set $10 \%$ slower.

Figure 27. Dead Time Addition

Figure 28. External Clock Synchronization


Figure 29. Current Mode Master/Slave Operation Over Short Distances


Figure 30. Synchronization Over Long Distances


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft-Start current is not affected by $\mathrm{R}_{1}$.

$$
\text { The new equation for Soft-Start is } \quad t \approx \frac{\mathrm{~V}_{\text {clamp }}+0.6}{9.0 \mu \mathrm{~A}}\left(\mathrm{C}_{\mathrm{SS}}\right)
$$

In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 31. Buffered Maximum Clamp Level


A series gate resistor may be needed to dampen high frequency parasitic oscillation caused by the MOSFET's input capacitance and any series wiring inductance in the gate-source circuit. The series resistor will also decrease the MOSFET switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 33. MOSFET Parasitic Oscillations


The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of the capacitor in series with the base.

Figure 32. Bipolar Transistor Drive


The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 34. Isolated MOSFET Drive

$\mathrm{T}_{1}$ - Primary: 8 turns \#48 AWG (1300 strands litz wire) Secondary: 2 turns $0.003^{\prime \prime}$ (2 layers) copper foil Bootstrap: 1 turn added to secondary \#36 AWG Core: Philips 3F3, part \#4312 0204124 Bobbin: Philips part \#4322 0213525 Coilcraft P3269-A
$\mathrm{L}_{1}-2$ turns \#48 AWG (1300 strands litz wire)
Core: Philips 3F3, part \#EP10-3F3
Bobbin: Philips part \#EP10PCB1-8
$\mathrm{L}=1.8 \mu \mathrm{H}$
Coilcraft P3270-A
Heatsinks - Power FET: AAVID Heatsink \#533902B02552 with clip Output Rectifiers: AAVID Heatsink \#533402B02552 with clip
Insulators - All power devices are insulated with Berquist Sil-Pad 150
(1) $-10(1.0 \mu \mathrm{~F})$ ceramic capacitors in parallel
(2) $-5(1.5 \Omega)$ resistors in parallel


Figure 36. PC Board With Components

(Top View)


Figure 37. PC Board Without Components

## CS51220

## Feed Forward Voltage Mode PWM Controller with Programmable Synchronization

CS51220 is a single output PWM Controller with switching frequency up to 500 kHz . The feed forward voltage mode control provides excellent line regulation for wide input range. This PWM controller has a synchronization output allowing programmable phase delay. For overcurrent protection, the "soft hiccup" technique effectively limits the output current with maximum flexibility. In addition, this device includes such features as: soft start, pulse-by-pulse current limit, programmable foldback current limit, volt-second clamping, maximum duty cycle, overvoltage and undervoltage protection, and synchronization input. The CS51220 is available in 16 SO narrow surface mount package.

## Features

- Constant Frequency Feed Forward Voltage Mode Control
- Programmable Pulse by Pulse Overcurrent Limit
- Programmable Foldback Overcurrent Limit with Delay
- Soft Hiccup Overcurrent Protection with Programmable Foldback
- Frequency Synchronization Output with Programmable Phase Delay
- Synchronization Input to Higher or Lower Frequency
- Direct Connection to External Opto Isolators
- Logic Gate Output Signal
- Accurate Volt-Second Clamping
- Programmable Soft Start
- Logic Input to Disable IC
- Line Overvoltage and Undervoltage Monitoring
- 3.3 V 3\% Reference Voltage Output

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


SO-16 D SUFFIX CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAM


A =Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51220ED16 | SO-16 | 48 Units/Rail |
| CS51220EDR16 | SO-16 | 2500 Tape \& Reel |



CS51220

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Thermal Resistance, Junction-to-Case, R ${ }_{\text {©JC }}$ |  | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Ambient, R ${ }_{\Theta J A}$ |  | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

*The maximum package power dissipation must be observed.
mAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gate Logic Output | $\mathrm{V}_{\mathrm{O}}$ | 20 V | -0.3 V | 100 mA | 100 mA |
| Current Sense Input | $I_{\text {SENSE }}$ | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Timing Capacitor | $\mathrm{C}_{\mathrm{T}}$ | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Feed Forward | FF | 6.0 V | -0.3 V | 10 mA | 100 mA |
| Error Amp Output | COMP | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Feedback Voltage | $\mathrm{V}_{\text {FB }}$ | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Sync Input | SYNCI | 20 V | -0.3 V | 10 mA | 10 mA |
| Power Down Input | DISABLE | 20 V | -0.3 V | 10 mA | 10 mA |
| Undervoltage | UV | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Overvoltage | OV | 6.0 V | -0.3 V | 10 mA |  |
| Current Set | $I_{\text {SET }}$ | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Soft Start | SS | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Power Supply | $\mathrm{V}_{\mathrm{CC}}$ | 20 V | -0.3 V | 100 mA | 50 mA |
| Sync Output | SYNCO | 20 V | -0.3 V | 100 mA |  |
| Reference Voltage | $\mathrm{V}_{\text {REF }}$ | 6.0 V | -0.3 V | Internally Limited | 10 mA |
| Sync Delay | $\mathrm{V}_{\text {SD }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Ground | GND | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ | 50 mA | $\mathrm{~N} / \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<16 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Supply Voltage/Current

| Start Threshold | - | 4.0 | 4.4 | 4.7 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Stop Threshold | - | 3.3 | 3.8 | 4.1 | V |
| Hysteresis | Start - Stop | 400 | 600 | 1000 | mV |
| ICC @ Startup | $\mathrm{V}_{\mathrm{CC}}<$ UVL Start Threshold | - | - | 500 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{CC}}$ Operating, Low $\mathrm{V}_{\mathrm{CC}}$ | $4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<10 \mathrm{~V}$ | - | - | 7.5 | mA |
| $I_{\text {cc }}$ Operating, High $\mathrm{V}_{\text {CC }}$ | 10 V < VCC < 16 V | - | - | 9.0 | mA |

## Reference Voltage

| Total Accuracy | $0 \mathrm{~mA}<\mathrm{I}_{\mathrm{REF}}<2.0 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Line Regulation | $\mathrm{I}_{\text {REF }}=2.0 \mathrm{~mA}$ | - | 6.0 | 20 | mV |
| Load Regulation | $0 \mathrm{~mA}<\mathrm{I}_{\text {REF }}<2.0 \mathrm{~mA}, \mathrm{~V}$ CC $=8.0 \mathrm{~V}$ | - | 6.0 | 15 | mV |
| Operating Life Shift | $\mathrm{T}=1000 \mathrm{Hrs},$. Note 2 | - | 4.0 | 20 | mV |
| Fault Voltage | - | 2.8 | 2.95 | 3.1 | V |
| $\mathrm{~V}_{\text {REF }}$ OK Voltage | - | 2.9 | 3.05 | 3.2 | V |
| $\mathrm{~V}_{\text {REF }}$ OK Hysteresis | - | 50 | 100 | 150 | mV |
| Current Limit |  | 2.0 | 25 | 65 | mA |

## Oscillator

| Frequency Accuracy |  | 223 | 266 | 309 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Temperature Stability | Note 2 | - | 8.0 | - | $\%$ |
| Max Frequency | Note 2 |  | 500 | - | - |
| Duty Cycle | Note 2 | 80 | 85 | 90 | $\%$ |
| Peak Voltage | Note 2 | 1.9 | 2.0 | 2.1 | V |
| Valley Voltage | $\mathrm{V}_{\text {CT }}=1.5 \mathrm{~V}$ | 0.85 | 0.90 | 0.98 | V |
| Discharge Current | $\mathrm{V}_{\text {CT }}=1.5 \mathrm{~V}$ | 0.70 | 0.85 | 1.05 | mA |
| Charge Current |  | 127 | 150 | 183 | $\mu \mathrm{~A}$ |

## Synchronization

| SYNCI Input Threshold | $\mathrm{f}_{\text {SYNC }}=500 \mathrm{kHz}$ | 1.0 | 2.0 | 3.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| SYNCI Input Resistance | $\mathrm{V}_{\text {SYNC }}=0.5$ | 50 | 150 | 250 | $\mathrm{k} \Omega$ |
| Minimum Sync Frequency | Reduction of nominal frequency. | 25 | - | - | $\%$ |
| Minimum Input Sync Pulse Width |  | - | - | - | 200 |
| SYNCO Output High | $\mathrm{R}_{\text {SYNCO }}=5.0 \mathrm{k}, \mathrm{V}_{\mathrm{CC}}=8.0 \mathrm{~V}$ | 5.0 | 6.5 | 7.5 | n |
| SYNCO Output Low | Sink $1.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{SD}}=2.5 \mathrm{~V}$ | - | 0.2 | 0.4 | V |
| SYNCO Delay Time | $\mathrm{V}_{\mathrm{CT}}=1.5 \mathrm{~V}$, Toggle $\mathrm{V}_{\mathrm{SD}}$ | 100 | 200 | 300 | ns |

2. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<16 \mathrm{~V} ; \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output (continued) |  |  |  |  |  |
| High Saturation Voltage | $\mathrm{V}_{\text {CC }}-\mathrm{V}_{\mathrm{O}}, \mathrm{V}_{\text {CC }}=10 \mathrm{~V}, \mathrm{I}_{\text {SOURCE }}=100 \mu \mathrm{~A}$ | - | 1.4 | 2.0 | V |
| Low Saturation Voltage | $\mathrm{V}_{\mathrm{O}}-\mathrm{GND}, \mathrm{I}_{\text {SINK }}=100 \mu \mathrm{~A}$ | - | 0.7 | 1.0 | V |
| Pull Down Resistance | $\mathrm{I}_{\text {SINK }}=100 \mu \mathrm{~A}$ | 25 | 50 | 75 | k $\Omega$ |
| Rise Time | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}, 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{O}}<6.0 \mathrm{~V} ; 50 \mathrm{pF}$ load | - | 35 | 80 | ns |
| Fall Time | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}, 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{O}}<6.0 \mathrm{~V} ; 50 \mathrm{pF}$ load | - | 25 | 50 | ns |

Feed Forward

| Discharge Voltage | $\mathrm{I}_{\mathrm{FF}}=2.0 \mathrm{~mA}$ | 0.25 | 0.35 | 0.45 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | $\mathrm{FF}=1.0 \mathrm{~V}$ | 2.0 | 10 | 30 | mA |
| FF to $\mathrm{V}_{\mathrm{O}}$ Delay | Connect $\mathrm{V}_{\mathrm{O}}$ to FF, Measure min. pulse width. | 50 | 75 | 150 | ns |
| FF Clamp Voltage | - | 1.15 | 1.3 | 1.45 | V |
| COMP Switch Off Voltage |  | 0.8 | 1.4 | 1.7 | V |
|  | $\mathrm{~V}_{\mathrm{FF}}=0.2 \mathrm{~V}$, Ramp down $\mathrm{V}_{\mathrm{COMP}}$ | 1.4 | 1.6 | 1.7 | V |

Overcurrent Protection

| Overcurrent Comparator DC Offset | - | 180 | 200 | 215 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {SENSE }}$ Attenuation | $\Delta \mathrm{V}_{\text {ISET }} / \Delta \mathrm{V}_{\text {ISENSE }}$ | 0.9 | 0.94 | 0.98 | $\mathrm{~V} / \mathrm{V}$ |
| $\mathrm{I}_{\text {SENSE }}$ Input Resistance | $\Delta \mathrm{V}_{\text {ISENSE }}=0 \mathrm{~V}$ | 40 | 82 | 150 | $\mathrm{k} \Omega$ |
| $\mathrm{I}_{\text {SENSE }}$ to GATE Delay | $\mathrm{V}_{\text {ISET }}=0.5 \mathrm{~V}$ | 50 | 100 | 175 | ns |
| I $\operatorname{ISET}$ Foldback Sink Current | $\mathrm{I}_{\text {SET }}=0.5 \mathrm{~V}, \mathrm{SS}=1.5 \mathrm{~V}$ and ISENSE $=0.5 \mathrm{~V}$ | 12 | 15 | 18 | $\mu \mathrm{~A}$ |

## External Voltage Monitors

| Overvoltage Threshold | OV pin increasing | 1.9 | 2.0 | 2.1 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| OV Hysteresis Current | OV = 2.15 V | 10 | 12.5 | 15 | $\mu \mathrm{~A}$ |
| Undervoltage Threshold | UV pin decreasing | 0.95 | 1.00 | 1.05 | V |
| UV Hysteresis |  | 25 | 75 | 125 | mV |

## Soft Start

| Charge Current | $\mathrm{SS}=1.5 \mathrm{~V}$ | 35 | 50 | 65 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | $\mathrm{SS}=1.5 \mathrm{~V}, \mathrm{UV}=1.5 \mathrm{~V}$ | 4.0 | 5.0 | 7.0 | $\mu \mathrm{~A}$ |
| OC Delay Discharge Current | $\mathrm{SS}=2.85 \mathrm{~V}, \mathrm{I}$ SET $=0.5$, I $\mathrm{SENSE}=0.5 \mathrm{~V}$ | 35 | 50 | 65 | $\mu \mathrm{~A}$ |
| SS Clamp Voltage | - | 2.7 | 2.9 | 3.1 | V |
| Discharge Voltage | - | 0.25 | 0.3 | 0.35 | V |
| Soft Start Fault Voltage | $\mathrm{OV}=2.5 \mathrm{~V}$ or UV = 0.85 V | - | 0.1 | 0.2 | V |
| Hiccup Delay Discharge Voltage | - | 0.08 | 0.1 | 0.12 | V |

Disable

| DISABLE Input Threshold | - | 1.0 | 2.0 | 3.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| DISABLE Input Resistance | $\mathrm{V}_{\text {DISABLE }}=0.5 \mathrm{~V}$ | 50 | 150 | 250 | $\mathrm{k} \Omega$ |
| DISABLE Operation Current, Low $\mathrm{V}_{\mathrm{CC}}$ | $4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<10 \mathrm{~V}$ | - | - | 800 | $\mu \mathrm{~A}$ |
| DISABLE Operation Current, High $\mathrm{V}_{\mathrm{CC}}$ | $10 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<16 \mathrm{~V}$ | - | - | 1600 | $\mu \mathrm{~A}$ |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 16 Lead SO Narrow | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{O}}$ | Logic output connecting to external gate driver. |
| 2 | GND | Ground. |
| 3 | $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage. |
| 4 | $\mathrm{V}_{\text {REF }}$ | 3.3 V reference voltage output. |
| 5 | $I_{\text {SET }}$ | Voltage at this pin sets pulse-by-pulse overcurrent threshold. When the ISENSE exceeds ISET for a sustained period of time, a sink current is generated at this pin. Along with external resistors, this current provides a foldback overcurrent threshold. The sink current is disabled periodically for restart. |
| 6 | IsENSE | Current sense input for overcurrent protection. |
| 7 | OV | Overvoltage protection monitor. |
| 8 | UV | Undervoltage protection monitor. |
| 9 | $\mathrm{C}_{\text {T }}$ | Timing capacitor $\mathrm{C}_{T}$ determines oscillator frequency. |
| 10 | SYNCI | By applying sync pulses to this pin, the IC can be synchronized to frequencies ranging from $25 \%$ slower to several times faster than the internal oscillator frequency. |
| 11 | DISABLE | Disable mode input pin. A voltage greater than 3.0 V turns off the whole IC. |
| 12 | FF | Feed forward input for PWM ramp. This pin allows external connection to make the ramp adjustable to the input line. |
| 13 | COMP | This pin carries feedback error signal from an external amplifier. Internally, it connects to the PWM controller. |
| 14 | SS | A capacitor is connected to this pin for Soft Start and soft hiccup timing. |
| 15 | $V_{S D}$ | The voltage at this pin programs the delay of the SYNCO output in reference to the internal oscillator. |
| 16 | SYNCO | Sync output. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## Feed Forward Voltage Mode Control

Conventional voltage mode control uses a fixed ramp signal for pulse width modulation, typically utilizing the oscillator output as the ramp signal. Since the only feedback signal comes from the output, this results in inferior line regulation and audio susceptibility. A significant improvement in line regulation and line transient response can be achieved using Feed Forward Voltage Mode Control, implemented using the CS51220 controller.

The enhancement comes from generating the ramp signal using a pull-up resistor from the FF pin to the line voltage and a capacitor to ground. The slope of the ramp then depends on the line voltage. At the start of each switch cycle, the capacitor connected to the FF pin is charged through the resistor connected to the input voltage. Meanwhile, the $\mathrm{V}_{\mathrm{O}}$ pin goes high to turn on a power mosfet through an external gate driver. When the rising FF pin exceeds the COMP input pin, as driven through the regulation feedback loop, $\mathrm{V}_{\mathrm{O}}$ goes low and turns off the external switch. Simultaneously, the FF capacitor is quickly discharged and set for the next switching cycle.

Overall, both input and output voltages control the dynamics of the duty cycle. As illustrated in Figure 3, with a fixed input voltage the output voltage is regulated solely by the error amplifier. For example, an elevated output voltage pulls down the COMP pin through an external error amplifier. This in turn causes duty cycle to decrease. On the another hand, if the input voltage varies, the slope of the FF pin ramp reacts correspondingly and immediately. As an example shown in Figure 4, when the input voltage goes up, the slope of the ramp signal increases, which reduces duty cycle and counteracts the change. For line variations, feed forward control requires less response from the error amplifier, which improves the transient speed and DC regulation.


Figure 3. Pulse Width Modulated by the Output Voltage with a Constant Input Voltage


Figure 4. Pulse Width Modulated by the Input Voltage with a Constant Output Voltage

The feed forward feature can also be employed for volt-second clamp, which limits the maximum product of input voltage and switch on time. This clamp is used in circuits, such as forward and flyback converters, to prevent the transformer from saturating. Calculations used in the design of the volt-second clamp are presented in the Design Guidelines section on page 1706 .

## $\mathrm{V}_{\mathrm{Cc}}$ Power Up and Fault Conditions

During power up, an undervoltage lockout comparator monitors $\mathrm{V}_{\mathrm{CC}}$ and disables $\mathrm{V}_{\mathrm{REF}}$, (which in turn disables the entire IC), until the $\mathrm{V}_{\mathrm{CC}}$ voltage reaches its start threshold. Hysteresis prevents "chattering" caused by the source impedance of the $\mathrm{V}_{\mathrm{CC}}$ supply. $\mathrm{V}_{\text {REF }}$ can also be disabled using the Disable input pin, which is active high. An internal pull-down resistor ensures the IC will start up if the Disable pin is allowed to float. In $\mathrm{V}_{\mathrm{CC}}$ or Disable lockout mode, the output stage is held low by the output pull-down resistance.

After $\mathrm{V}_{\text {REF }}$ turns on, there are three conditions that can cause fault mode:
10. The $3.3 \mathrm{~V} \mathrm{~V}_{\mathrm{REF}}$ is below regulation,
11. The OV pin rises above overvoltage threshold, or
12. The UV pin falls below undervoltage threshold.

Fault detection will cause the $\mathrm{V}_{\mathrm{O}}$ output to go low and the SS pin to discharge. The UV and OV inputs are typically used to monitor the input line voltage. The undervoltage comparator has a built-in hysteresis voltage, while the hysteresis for the OV comparator is programmable through a current sourced from the pin when above the threshold, and the equivalent external resistance. The fault condition can only be reset after the SS pin has been completely discharged and all faults have been removed.

After a fault is removed or upon initial startup, the SS pin charges at a rate determined by an internal charge current and an external capacitor. The rising voltage on the SS pin will override the regulation feedback voltage on the COMP pin and clamp the duty cycle, helping to reduce any in-rush current during startup. The duration of the Soft Start is typically set with a capacitor from $0.01 \mu \mathrm{~F}$ to $0.1 \mu \mathrm{~F}$.

## Overcurrent Protection

The CS51220 uses the "soft hiccup" technique to provide an adjustable and predictable overcurrent limit. By choosing external component values the designer can select pulse-by-pulse current limit, soft hiccup current limit or hard hiccup limit.

Normal pulse-by-pulse current limit can be obtained by selecting the $\mathrm{I}_{\text {SET }}$ resistor values for a low Thevenin
resistance to the $\mathrm{I}_{\text {SET }}$ pin. However with normal pulse-by-pulse current limit, the secondary currents during short circuits may be several times the maximum output current.

Soft hiccup limit can be obtained by setting the $\mathrm{I}_{\text {SET }}$ resistor values for a higher thevenin resistance. During overcurrent conditions, the $\mathrm{I}_{\text {SET }}$ level will fold back, after a short delay, to reduce the pulse by pulse threshold. If desired, the short circuit current can be chosen to be equal to or even less than the maximum output current. During soft hiccup the circuit will periodically disable the foldback and attempt to restart.

Hard hiccup limit can be obtained by setting the $\mathrm{I}_{\text {SET }}$ resistor values so that the ISET pin is held below 200 mV during foldback. During overcurrent conditions, the $I_{\text {SET }}$ level will fold back, after a short delay, preventing any gate pulses. When the SS capacitor is completely discharged, the circuit will attempt restart. This configuration provides the lowest power dissipation during short outputs.

The circuit functions can be best described by discussing the block diagram and illustrations of expected waveforms. Actual waveforms, values and circuit configurations from a design will be used. The design is from the 5.0 V supply of a dual synchronized converter.

The current is monitored with a voltage at the $I_{\text {SENSE }}$ pin. The ISENSE signal is slightly attenuated DC shifted by 200 mV , and is compared with the threshold voltage programmed by the voltage at the $I_{\text {SET }}$ pin. If the current signal reaches the threshold voltage, the overcurrent comparator resets the $\mathrm{V}_{\mathrm{O}}$ latch and terminates the $\mathrm{V}_{\mathrm{O}}$ pulse. The overcurrent comparator has a maximum common mode input voltage of 1.8 V . However, an $\mathrm{I}_{\text {SET }}$ voltage below 1.0 V is desirable for reducing the comparator's propagation delay. During initial turnon of the power supply, normal pulse-by-pulse overcurrent control is used to protect the power supply switches. This is accomplished by comparing the voltage at the ISENSE input to the voltage at the $\mathrm{I}_{\text {SET }} \mathrm{pin}$ and using this to limit the duty factor of $\mathrm{V}_{\mathrm{O}}$, the gate drive signal. This current limit control is maintained until the SS voltage reaches 2.9 V .

The block diagram of the soft hiccup circuit is shown in Figure 5. When overcurrent occurs and the SS is above 2.9 V , the OC pulses set the OC latch. The output of the OC latch turns on the OC delay discharge current to ramp down the SS voltage. This SS discharge ramp down is at a rate of $50 \mu \mathrm{~A}$ while the SS voltage is above 2.8 V . The level between 2.9 V and 2.8 V is called the hiccup delay discharge voltage. The time to cross this voltage creates a short delay. This delay is useful so that a quick transient overcurrent condition can be controlled and still allow the supply to return immediately to normal operation. After reaching the hiccup delay discharge voltage, the SS current is reduced to $5.0 \mu \mathrm{~A}$ and the $\mathrm{I}_{\mathrm{SET}}$ foldback current is turned on at $15 \mu \mathrm{~A}$. It is the $\mathrm{I}_{\mathrm{SET}}$ foldback current that adjusts the $\mathrm{I}_{\text {SET }}$ level to establish a new lower I ${ }_{\text {SENSE }}$ current limit level. See Figure 6 for details.


Figure 5. The Block Diagram of the Soft Hiccup Operation

A circuit monitors the OC pulses. If the OC pulses cease for $50 \mu \mathrm{~s}$, the $\mathrm{NOt}-$ OverCurrent (NOOC) signal is generated. This NOOC signal resets the OC Latch and allows the SS capacitor to charge back up allowing the output to reestablish regulation.

For an equivalent circuit shown in Figure 6, the $\mathrm{I}_{\text {SET }}$ current reduces the overcurrent threshold and sets the new threshold at

$$
\mathrm{V}_{\mathrm{I}}(\mathrm{SET})=(3.3-\mathrm{ISET} \times \mathrm{R} 1) \times \frac{\mathrm{R} 2}{(\mathrm{R} 1+\mathrm{R} 2)}
$$



Figure 6. The Voltage Divider Used at the ISET Pin Allows the ISET Foldback Current to Reduce the Overcurrent Threshold

The NOOC or SS low ( $\mathrm{V}_{\mathrm{SS}}<0.3 \mathrm{~V}$ ) signal can reset OC latch at any time. This event turns off I IET foldback and allows the recharging of the SS capacitor. Therefore, the IC allows the power supply to restart periodically or after the overcurrent condition is cleared. The OC latch can not be set until the SS capacitor is fully charged.

To implement "hard hiccup" which disables the $\mathrm{V}_{\mathrm{O}}$ completely when the SS voltage is ramping down, select a resistor value greater than $3.3 \mathrm{~V} / \mathrm{I}_{\text {SET }}$ for R1 in Figure 6, and saturate the internal $\mathrm{I}_{\mathrm{SET}}$ current source. Since the saturation voltage is less than the DC shift applied to the I IENSE signal, the OC comparator output is always high and in turn keeps the $\mathrm{V}_{\mathrm{O}}$ low. Figure 7 demonstrates the interactions among the voltage of SS, I ISET and internal signal OC. Figure 8 further describes the specifications associated with the soft hiccup. The ratio among the charge time, delay time and discharge time is given at the bottom of Figure 8.


Figure 7. Illustrative Waveforms of the Soft Hiccup Operation


Figure 8. The SS Pin Voltage Under Ramp Up and Overcurrent Condition and Associated Specifications.

The effect of the soft hiccup can be observed in Figure 9, which shows the output voltage as load increases. The output is maintained at the regulation value of 5.0 V until it goes into current limit. At the point of overcurrent inception (A), the current limit level changes to a lower level (B). The switchback to a lower current limit level can be seen as the bottom curve in Figure 9.


Figure 9. Overcurrent In a 5.0 V Output Converter Using Soft Hiccup
A typical overload scenario is shown in Figure 10. The top trace is the voltage on the Soft Start (SS) pin. The initial high discharge rate can be seen transitioning to a 40 ms discharge period. During this period the $\mathrm{I}_{\text {SET }}$ establishes a lower current limit level. The bottom trace shows the output current. The initial current spike is the output capacitors discharging. The next level around 4.0 A is the short circuit current level set by the $\mathrm{I}_{\text {SET }}$ current. The output then turns off allowing the current to reduce to a level that does not cause overcurrent pulses. This releases the SS pin to ramp back up. During ramp up, the output is still shorted as noted by the 8.0 A current level. When SS reaches the 2.9 V level, the short is again recognized and $\mathrm{I}_{\mathrm{SET}}$ is turned back on shifting the short circuit current level.


Figure 10. Over-Load Current and Soft Start Waveforms

The middle trace is a digitizing 'scope trace of the current sense line. The scope interprets the voltages as an average voltage. This voltage is actually a narrow duty cycle peak voltage representing the peak current level in the switching transistor. The actual peak voltages can be seen in the Figure 11. The peaks are 0.85 V at full load, reducing to 0.6 V peak at the reduced short circuit level. The 1.1 V peak is the full short circuit current while SS ramps back up. The 0.32 V level is the normal load resistance, while $\mathrm{I}_{\text {SET }}$ is still on. The 1.0 V surge is created by ramp up into a normal 5.0 A load and followed by the 0.85 V at normal load.


Figure 11. Over-Load Current and Isense Voltage

## Oscillator and Synchronization

The switching frequency is programmable through a capacitor connected to the $\mathrm{C}_{\mathrm{T}}$ pin. When the $\mathrm{C}_{\mathrm{T}}$ pin voltage reaches peak voltage ( 2.0 V ), the internal discharge current discharges the $\mathrm{C}_{\mathrm{T}}$ capacitor and $\mathrm{V}_{\mathrm{O}}$ stays low. When the $\mathrm{C}_{\mathrm{T}}$ voltage declines to valley voltage ( 0.9 V ), the current source toggles to charge current and ramps up the $\mathrm{C}_{\mathrm{T}}$ pin. This starts a new switching cycle. The duty cycle of the oscillator determines the maximum PWM duty cycle.

The switching frequency of the IC can be synchronized to an external frequency presented to the SYNCI pin. When pulses with amplitude over SYNCI input threshold are detected, the $\mathrm{C}_{\mathrm{T}}$ pin immediately ramps down the external capacitor and the $\mathrm{V}_{\mathrm{O}}$ pin is forced low. A new switching cycle begins when the $\mathrm{C}_{\mathrm{T}}$ pin reaches valley voltage. During synchronization, the oscillator charge current is reduced by $80 \mu \mathrm{~A}$, while discharge current is increased by $80 \mu \mathrm{~A}$. This effectively slows down the internal oscillator to avoid any race condition with the sync frequency. As a result, the sync frequency can be either higher or lower than the internal oscillator frequency. CS51220 is able to synchronize up to 500 kHz and down to $25 \%$ below $\mathrm{C}_{\mathrm{T}}$ frequency. The maximum duty cycle clamp is raised to $92 \%$ in synchronization mode. The original oscillator frequency is restored upon the removal of sync pulses.


Figure 12. Synchronization Input Timing
Figure 12 shows the sync input from one CS51220 into another. The delay between receiving the sync input and the start of the next switching cycle is 423 ns . This delay must be taken into account when establishing the total delay between two regulators.

The SYNCO pin provides outgoing synchronization pulses whose delay can be programmed by setting the voltage on the $\mathrm{V}_{\mathrm{SD}}$ pin. The feature allows two converters to run at interleaved phases. This implementation significantly reduces the input ripple, and thus the number of input capacitors. The phase delay is achieved by turning on SYNCO output only after the $\mathrm{C}_{\mathrm{T}}$ pin voltage reaches the $\mathrm{V}_{\mathrm{SD}}$ voltage. Therefore, the phase delay varies linearly with the $\mathrm{V}_{\mathrm{SD}}$ voltage. The SYNCO output is reset during the falling edge of the $\mathrm{C}_{\mathrm{T}} \mathrm{pin}$. For minimum phase delay ( $\sim 240 \mathrm{~ns}$ ), tie the $\mathrm{V}_{\mathrm{SD}}$ pin to the ground. To entirely disable the SYNCO output, connect the $\mathrm{V}_{\mathrm{SD}}$ pin to $\mathrm{V}_{\text {REF }}$.

The waveform in Figure 13 shows the $\mathrm{C}_{\mathrm{T}}$ ramp crossing the $\mathrm{V}_{\mathrm{SD}}$ voltage set at 1.41 V .


Figure 13. Synchronization Output Timing
The delay from the point of crossing to the output of the sync signal is 240 ns . The time for the sync out voltage is measured at the +2.0 V level, which is the level that triggers the next CS51220.

The desired effect on the input ripple is illustrated in Figure 14. This is the input current for two power converters operating from a 36 V line.


Figure 14. Input Current Ripple with Different Overlap Conditions

The top waveform in Figure 14 is the input current with the two supplies operating out of phase. The next down shows the same supplies but with both conduction times occurring simultaneously. The greatly increased ripple current can be observed. The last two waveforms are the two converters shown individually when operating out of phase.

## DESIGN GUIDELINES

## Program Volt-Second Clamp

Feed forward voltage mode control provides the volt-second clamp which clamps the product of the line voltage and switch on time. For the circuit shown in Figure 15, the charging current of the $\mathrm{C}_{\mathrm{FF}}$ can be considered as a constant current equal to $\mathrm{V}_{\mathrm{IN}} / \mathrm{R}_{\mathrm{FF}}$, provided $\mathrm{V}_{\mathrm{IN}}$ is much greater than the FF pin voltage. Then the volt-second clamp provided by CS51220 is given by

$$
\mathrm{V}_{\text {IN }} \mathrm{TON}(\mathrm{MAX})=1.0 \mathrm{RFF}_{\mathrm{FFF}}
$$



Figure 15. An RC Network Provides Both Volt-Second Clamp and Feed Forward Control

Select the time constant of the FF pin RC network to provide desirable volt-second clamp.

## Program Oscillator Frequency

CS51220 requires an external capacitor to program the oscillator frequency. The internally trimmed charge/discharge current determines the maximum duty cycle. The capacitor for a required switching frequency $f_{S}$ can be calculated by:

$$
C T=\frac{13400}{f S}-95
$$

where:
$\mathrm{C}_{\mathrm{T}}=$ Timing capacitance is in pF
$\mathrm{f}_{\mathrm{S}}=$ Switching frequency is in kHz
Figure 16 shows the relationship of $\mathrm{C}_{\mathrm{T}}$ and $\mathrm{f}_{\mathrm{S}}$.


Figure 16. Operating Frequency

## Synchronized Dual Converters with Soft Hiccup and Feed Forward

The circuits shown in Figures 17 and 18 illustrate typical applications for a dual output supply using independent but synchronized converters. These circuits demonstrate the use of the soft hiccup, feed forward, volt-second control and synchronization features of the CS51220.
In Figure 17, the feed forward circuit has a volt-second constant of $82 \mathrm{~V} / \mu \mathrm{s}$. This would limit the duty factor to 0.51 at 48 V input. With a turns ratio of $4: 1$ on the power transformer and 48 V input, a duty factor of 0.46 is required for 5.0 V output. This converter serves as the master synchronization generator. The voltage on the $\mathrm{V}_{\text {SD }}$ pin establishes the delay as it is compared to the ramp generated on the $\mathrm{C}_{\mathrm{T}}$ pin.

Adjustable synchronization allows the conduction time for the two converters to be adjusted so that they are not on at the same time. This greatly reduces the ripple current from the 48 V source.
In Figure 18, the feed forward circuit has a volt-second constant of $63 \mathrm{~V} / \mu \mathrm{s}$. This would limit the duty factor to 0.39 at 48 V input. With a turns ratio of $4: 1$ on the power transformer and 48 V input, a duty factor of 0.33 is required for 3.3 V output.


CS51220


CS51220

## Advance Information

Full Featured Voltage Mode PWM Controller

The NCP1560 PWM controller contains all of the features and flexibility needed to implement voltage-mode control for modern high performance power converters. This device cost effectively reduces system part count with the inclusion of a high-voltage start-up regulator that operates over a wide input range of 33 V to 150 V. The NCP1560 provides two control outputs, OUT1 which controls the main PWM switch and OUT2 with adjustable over-lap delay, which can control a synchronous rectifier. Other distinctive features include: two mode over-current protection, line under/over voltage lockout, fast line feed-forward, soft-start and a maximum duty cycle clamp.

## Features

- Internal High Voltage Start-up Regulator
- Dual Control Outputs with Adjustable Over-Lap Delay
- Single Resistor Oscillator Frequency Setting
- Fast Line Feed-Forward
- Line Under/Over Voltage Lockout
- Dual Mode Over-Current Protection
- Programmable Maximum Duty Cycle Control
- Maximum Duty Cycle Proportional to Line Voltage
- Programmable Soft-Start
- Precision Reference


## Typical Applications

- Telecommunication Power Converters
- Industrial Power Converters
- High Voltage Power Modules
- +42 V Automotive Systems
- Control Driven Synchronous Rectifier Power Converters

ON Semiconductor ${ }^{\text {w }}$ http://onsemi.com


```
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
```


## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP1560DR2 | SO-16 | 2500 Units/Reel |



Figure 1. Simplified Block Diagram


Figure 2. NCP1560 Block Diagram

## PIN DESCRIPTION

| Pin | Name | Description | Application Information |
| :---: | :---: | :---: | :---: |
| 1 | Vin | Source Input Voltage | Input range: 33 V to 150 V . |
| 2 | UV_OV | Input Undervoltage and Overvoltage shutdown. | An external divider from the power converter source input must be scaled $>1.49$ volts and $<3.60$ volts over the operational range. |
| 3 | TP_Ramp | Test point provided for the Feed Forward Ramp signal. | Internally this signal is compared to Vea. |
| 4 | FF_SET | An external resistor between Vin and this pin adjusts the amplitude of the FF_Ramp in proportion to Vin and R. | By varying the PWM ramp amplitude in proportion to the line voltage changes in loop bandwidth resulting from line voltage changes are eliminated. |
| 5 | CS | Current Sense input | If CS exceeds 0.5 volt the outputs will go into a Cycle by Cycle current limit. If CS exceeds 0.6 volts the outputs will be disabled for a period determined by the Current Sense Fault Timer. A softstart will follow at the conclusion of the fault timer. |
| 6 | C_SKIP_SET | An external capacitor sets the shutdown period after 0.6 V CS event. | An external capacitor sets the shutdown period. Range: $68 \mathrm{pF}=12 \mu \mathrm{~s}, 6800 \mathrm{pF}=1.2 \mathrm{~ms}$ |
| 7 | RT | A single external resistor between this pin and GND sets the fixed oscillator frequency. | Resistance Range $68 \mathrm{~K}=500 \mathrm{KHz}$ $390 \mathrm{~K}=100 \mathrm{KHz}$ |
| 8 | MAX_DUTY_SET | An external resistor between this pin and GND sets the maximum allowable Duty cycle. | Resistance Range 0 Ohms $=60 \%$ Open $=80 \%$ given the FF_Ramp of 2.0 V peak (low line). |
| 9 | SS | Softstart control | An external capacitor and the internal $6.0 \mu \mathrm{~A}$ current source, set the softstart ramp. The capacitor voltage sets a maximum duty cycle clamp from 0 to 2.0 volts ( 0 to $100 \%$ Duty). |
| 10 | Vea | Input from an external error amplifier. | There is no error amplifier included within this controller. The error amplifier is typically secondary side referenced while the controller is primary side referenced. |
| 11 | 5.0 V_REF | Precision 5.0 volt reference output. | Maximum output current: 10 mA . |
| 12 | Td_Set | An external resistor between Vref and this pin sets the leading edge and trailing edge time delay between OUT1 and OUT2. | Time delay (Td) <br> Rd open $=250 \mathrm{nS}$ (Max Delay) <br> Rd $(60 \mathrm{~K})=25 \mathrm{nS}$ (Min Delay) |
| 13 | OUT2 | Output of the PWM controller with leading edge and a trailing edge time delay of (Td). | OUT2 can be used to drive a synchronous rectifier. |
| 14 | GND | Return |  |
| 15 | OUT1 | Output of the PWM controller. | OUT1 main PWM output. |
| 16 | AUX | Auxiliary bias power. Upon turn-on an internal current source supplies bias power. An external slave winding then continues supplying bias power. | An internal current source supplies 12 mA until Vaux reaches 11 volts. An external capacitor is required to holdup Vaux above 7.0 volts while the converter starts. Typically an external slave winding then provides power to the control circuits. |

MAXIMUM RATINGS (Notes 1 \& 2)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Vin to GND | $\mathrm{V}_{\text {in }}$ | 150 | V |
| Vaux to GND | $\mathrm{V}_{\text {aux }}$ | 16 | V |
| All Other Inputs to GND | - | - | V |
| 5.0 V Reference Output Current | $\mathrm{I}_{\text {REF }}$ | 10 | mA |
| OUT1, OUT2 Output Current | $\mathrm{I}_{\text {OUT1 }}, \mathrm{I}_{\mathrm{OUT} 2}$ | 20 | mA |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | -40 to +140 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| Power Dissipation at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | 0.88 | $\mathrm{~W}^{\mathrm{C}}$ |
| Thermal Resistance, Junction to Case | $\mathrm{R}_{\text {日JA }}$ | 130 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
2. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per MIL-STD-883, Method 3015. Machine Model Method 200 V .

ELECTRICAL CHARACTERISTICS $\left(T_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high, }}, \mathrm{V}_{\text {in }}=48 \mathrm{~V}, \mathrm{~V}_{\text {aux }}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=100 \mathrm{~K}, \mathrm{C}_{\mathrm{ft}}=6800 \mathrm{pF}, \mathrm{R}_{\mathrm{d}}=60 \mathrm{~K}$, $\mathrm{R}_{\mathrm{FF}}=464 \mathrm{~K}$ )

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Reference |  |  |  |  |  |  |
| REF Output Voltage | $\mathrm{V}_{\text {REF }}$ | $\mathrm{I}_{\text {ref }}=0 \mathrm{~mA}$ | 4.9 | 5.0 | 5.1 | V |
| REF Voltage Regulation |  | $\mathrm{I}_{\text {ref }}=0$ to 10 mA | - | 50 | - | mV |

## Vaux Supply

| Vaux Current Source |  | Vaux $<11 \mathrm{~V}^{*}$ | 11 | 12 | - | mA |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Vaux Current Source Disable |  |  | - | 11 | - | V |
| Vaux Undervoltage Lockout Voltage |  |  | - | 7.0 | - | V |
| Startup Regulator Leakage |  | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\text {in }}=150 \mathrm{~V}$ | - | - | 50 | $\mu \mathrm{~A}$ |
| Supply Current (laux) | Vea $=0 \mathrm{~V}$ | - | - | 5.0 | mA |  |
| Shutdown Current (laux) | Vuv/ov $=0 \mathrm{~V}$ | - | - | 2.5 | mA |  |

## Input UV/OV Shutdown

| Undervoltage Shutdown (increasing) |  |  | 1.43 | 1.49 | 1.55 | V |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Undervoltage Shutdown Hysteresis |  |  | - | 0.16 | - | V |
| Overvoltage Shutdown (increasing) |  |  | 3.46 | 3.60 | 3.74 | V |
| Overvoltage Shutdown Hysteresis |  |  | - | 0.16 | - | V |

## Current Limit

| ILIM Delay to Output $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ |  |  | - | - | 150 | nS |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Cycle-by-Cycle Threshold Voltage |  |  | 0.47 | 0.5 | 0.53 | V |
| Cycle Skip Threshold Voltage |  |  | 0.57 | 0.6 | 0.63 | V |

## Cycle Skip Program

| Time Delay |  |  | - | 1.2 | - | mS |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

*Non-continuous rating. Vaux current source will supply 12 mA over the input voltage range of 33 V to 150 V . However package thermal restrictions apply.

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}, \mathrm{V}_{\text {in }}=48 \mathrm{~V}, \mathrm{~V}_{\text {aux }}=12 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=100 \mathrm{~K}, \mathrm{C}_{\mathrm{ft}}=6800$ $\mathrm{pF}, \mathrm{R}_{\mathrm{d}}=60 \mathrm{~K}, \mathrm{R}_{\mathrm{FF}}=464 \mathrm{~K}$ )

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |


|  |  |  |  |  |  |  |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Charge Current |  |  | 5.0 | 6.0 | 7.0 | $\mu \mathrm{~A}$ |
| Discharge Current |  |  | - | 10 | - | mA |

## Oscillator

| Frequency |  |  | 285 | 300 | 315 |
| :--- | :--- | :--- | :--- | :--- | :--- |

PWM Comparator

| Input Bias Current |  |  | - | 1.0 | - | nA |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Delay to Output $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ |  |  | - | - | 200 | nS |

## Feedforward

| FF Ramp Amplitude |  |  | - | 2.7 | - |
| :--- | :--- | :--- | :--- | :--- | :--- |

Max Duty Program

| Max Duty $60 \%$ |  | $R p=0$ Ohms, $V_{\text {in }}=36 \mathrm{~V}$ | 57 | 60 | 63 | $\%$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Max Duty $80 \%$ |  | $R p=o p e n, V_{\text {in }}=36 \mathrm{~V}$ | 76 | 80 | 84 | $\%$ |

Output Section

| Output High Saturation |  | $\mathrm{I}_{\text {out }}=10 \mathrm{~mA}$ | - | 11.4 | - | V |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Output Low Saturation |  | $\mathrm{I}_{\text {out }}=-10 \mathrm{~mA}$ | - | 0.25 | - | V |
| Rise Time | $\mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$ | - | 20 | - | nS |  |
| Fall Time |  | $\mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$ | - | 12 | - | nS |

Time Delay Set

| Time Delay Max | $\mathrm{Td}(\max )$ | $\mathrm{Rd}=$ open, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 225 | 250 | 275 | nS |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Time Delay Min | $\mathrm{Td}(\min )$ | $\mathrm{Rd}=60 \mathrm{~K}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 20 | 25 | 30 | nS |

## Thermal Shutdown

| Thermal Shutdown Temperature | Tsd |  | - | 150 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |

## DETAILED OPERATING DESCRIPTION

The NCP1560 PWM controller contains all of the features and flexibility needed for implementation of voltage-mode control for modern high performance power converters. This device cost effectively reduces system part count with the inclusion of a high-voltage start-up regulator. The NCP1560 provides two control outputs, OUT1 which controls the main PWM switch and OUT2 with adjustable over-lap delay, which can control a synchronous rectifier switch. Other distinctive features include: two mode over-current protection, line under/over voltage lockout, fast line feed-forward, soft-start and a maximum duty cycle clamp. The Functional Block Diagram is shown in Figure 1.

The NCP1560 is designed for Voltage-Mode Control converters. The features included in the NCP1560 enable all of the advantages of Current-Mode Control, fast line feed-forward, and cycle by cycle current limit. It eliminates the disadvantages of low power jitter, slope compensation and noise susceptibility. Finally the dual outputs of the NCP1560 allow for optimum control of a synchronous rectifier switch.

## High Voltage Start-up Regulator

The NCP1560 contains an internal high voltage current source. This current source is set to 12 mA . When the line voltage is in range, the current source is enabled and sources current into an external capacitor connected to the Vaux pin. When the voltage on the Vaux pin reaches 11 V the controller outputs are enabled and the internal current source is disabled. The Vaux voltage will then transition to the converter self bias voltage. The start-up regulator will remain off until the Vaux voltage falls below 7.0 V. At that time the outputs will be disabled until the Vaux pin again reaches 11 V . The external Vaux capacitor must be sized such that the self-bias will maintain a Vaux voltage greater than 7.0 V during initial start-up. During a fault mode when the converter self bias is inactive, external current draw on the Vaux line should be limited as to not exceed the maximum power dissipation of the controller.

## Input Under/Over Voltage Shutdown

The NCP1560 contains a line under/over voltage shut down circuit. An external voltage divider sets the operational range of the converter. The divider must be set for a voltage at the under/over voltage pin to be greater than 1.49 V and less than 3.60 V . If the Under voltage threshold is not met, all functions of the controller are disabled except the bias (Vaux) regulator and the controller will be in a low power state, $<500 \mu \mathrm{~A}$. If the Over voltage threshold is exceeded, OUT1 and OUT2 will be disabled and the softstart capacitor will be discharged.

The under/over voltage pin can also be used to implement a remote enable/disable function. By shorting the over/under pin to ground, the converter can be disabled. The internal bias regulator will continue to operate varying between 7.0 and 11 volts. All other functions will be disabled.

## Reference

The NCP1560 provides a precision reference output of 5 volts. This output should be locally bypassed with a $0.1 \mu \mathrm{~F}$ ceramic capacitor. The maximum current available from this output is 10 mA .

## Current Limit

The NCP1560 contains two levels of over current protection. If the voltage on the CS pin exceeds 0.5 volt the present cycle is terminated and the outputs are disabled. If the voltage on the CS pin exceeds 0.6 volts, the controller will disable the outputs, enable the Cycle Skip Timer and discharge the softstart capacitor. The outputs will remain disabled until the Cycle Skip Timer completes, then a softstart will commence. The duration of the Current Sense Fault Timer is set by an external capacitor. The range of capacitor (time set) is $68 \mathrm{pF}(12 \mu \mathrm{~s})$ to $6800 \mathrm{pF}(1.2 \mathrm{mS})$. A complete softstart will commence after the current sense fault timer completes.

## Oscillator and Ramp Feed-Forward

The NCP1560 oscillator is set by a single external resistor connected between the RT pin and return. Internally there are two ramp voltages generated by the oscillator. The OSC_Ramp is a fixed amplitude ramp of 0 to 1.5 volts. This ramp is used for the softstart comparator and as a basis for the Feed Forward ramp (FF_Ramp). The amplitude of the FF ramp varies in proportion to the voltage on the FF_SET pin. The FF_Ramp is used for the PWM comparator and the Max Duty Cycle comparator. The amplitude of the FF_Ramp is normally set to vary from 1.5 to 3.0 volts for a corresponding $2: 1$ change in line voltage. An external resistor between the FF_SET pin and the line sets the proportion to which the ramp amplitude changes with line voltage.

## Maximum Duty Cycle

A dedicated internal comparator limits the maximum output duty cycle. The Feedforward ramp is compared to a fixed voltage configured by the Max Duty Cycle pin. Since the amplitude of the Feedforward ramp increases with increasing line voltage the maximum duty cycle will then decrease with increasing line voltage, which is a desirable feature. If the Max Duty Cycle pin is left open the voltage present at the Max Duty Cycle comparator will be 1.6 volts, which will correspond to a maximum duty cycle of $80 \%$ when the FF_Ramp amplitude is at 2.0 volts. If the Max Duty Cycle pin is shorted to return the voltage present at the Max Duty Cycle comparator will be 1.2 volts, which will correspond to a maximum duty cycle of $60 \%$ when the FF_Ramp amplitude is 2.0 volts. If the Max Duty Cycle pin is connected to Vref, the maximum duty cycle feature will be disabled and the maximum duty cycle will approach $100 \%$. If the FF_Ramp amplitude increases to 4.0 volts as a result of the line increasing the maximum duty cycle will
then decrease to $40 \%$ or $30 \%$, respectively, depending upon the Maximum Duty Set pin configuration.

## PWM Comparator

The PWM comparator compares the Feedforward ramp to the voltage presented at the Vea pin. There is a 0.65 V (diode) offset between the Vea pin and the PWM comparator. The output of an external error amplifier generally drives the Vea pin. The comparator polarity is such that 0.65 volts or less on the Vea pin will cause a Zero duty cycle.

## Softstart

The softstart feature allows the converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. Upon power on, a $6.0 \mu \mathrm{~A}$ current is sourced out of the softstart pin into an external capacitor. The capacitor voltage will begin to ramp up. The voltage on the softstart pin is compared to a 2.0 V Oscillator Ramp signal and will act to reduce the maximum duty cycle until the capacitor voltage ramps up. In the event of a fault, line under/over voltage or current cycle skip, the softstart pin will discharge the external capacitor and disable the output drivers. When the fault condition is no longer present a softstart will be exercised again.

## OUT1, OUT2 and Time Delay

The NCP1560 provides two in-phase outputs, OUT1 and OUT2. However, OUT2 always precedes OUT1 at any low to high transition and OUT1 always precedes OUT2 at any high to low transition. The leading and trailing time delays are equal and set by the Time Delay pin. An open circuit on the Time Delay pin will cause the maximum delay of 500 nS . A 60 K resistor between the Time Delay pin and $5.0 \mathrm{~V} \_$REF will cause the minimum delay of 50 nS . Generally, OUT1 controls the main switching element. OUT2 once inverted can drive the free-wheeling synchronous rectifier switching element.

## Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 150 degrees Celsius, the controller is forced into a low power reset state, disabling the output drivers and the bias regulator. This feature is provided to prevent catastrophic failures from accidental device overheating.

## TL494

## SWITCHMODETM Pulse Width Modulation Control Circuit

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push-Pull or Single-Ended Operation
- Undervoltage Lockout

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

| Rating | Symbol | TL494C TL494I | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 42 | V |
| Collector Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{C} 1}, \\ & \mathrm{~V}_{\mathrm{C} 2} \end{aligned}$ | 42 | V |
| Collector Output Current (Each transistor) (Note 1) | $\mathrm{I}_{\mathrm{C} 1}, \mathrm{I}_{\mathrm{C} 2}$ | 500 | mA |
| Amplifier Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | -0.3 to +42 | V |
| Power Dissipation @ $\mathrm{T}_{\mathrm{A}} \leq 45^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | 1000 | mW |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {өJA }}$ | 80 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range TL494C TL494I | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Derating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | 45 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum thermal limits must be observed.



## ON Semiconductor

http://onsemi.com


PDIP-16 N SUFFIX CASE 648

$x \quad=\mathrm{C}$ or I
A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=\mathrm{Year}$
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| TL494CD | SO-16 | 48 Units/Rail |
| TL494CDR2 | SO-16 | 2500 Tape \& Reel |
| TL494CN | PDIP-16 | 500 Units/Rail |
| TL494IN | PDIP-16 | 500 Units/Rail |

## RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 7.0 | 15 | 40 | V |
| Collector Output Voltage | $\mathrm{V}_{\mathrm{C} 1}, \mathrm{~V}_{\mathrm{C} 2}$ | - | 30 | 40 | V |
| Collector Output Current (Each transistor) | $\mathrm{I}_{\mathrm{C} 1}, \mathrm{I}_{\mathrm{C} 2}$ | - | - | 200 | mA |
| Amplified Input Voltage | $\mathrm{V}_{\mathrm{in}}$ | -0.3 | - | $\mathrm{V}_{\mathrm{CC}}-2.0$ | V |
| Current Into Feedback Terminal | $\mathrm{I}_{\mathrm{fb}}$ | - | - | 0.3 | mA |
| Reference Output Current | $\mathrm{I}_{\mathrm{ref}}$ | - | - | 10 | mA |
| Timing Resistor | $\mathrm{R}_{\mathrm{T}}$ | 1.8 | 30 | 500 | $\mathrm{k} \Omega$ |
| Timing Capacitor | $\mathrm{C}_{\mathrm{T}}$ | 0.0047 | 0.001 | 10 | $\mu \mathrm{~F}$ |
| Oscillator Frequency | $\mathrm{f}_{\mathrm{osc}}$ | 1.0 | 40 | 200 | kHz |

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega$, unless otherwise noted.)
For typical values $T_{A}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| Reference Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {ref }}$ | 4.75 | 5.0 | 5.25 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ to 40 V ) | Regline | - | 2.0 | 25 | mV |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 3.0 | 15 | mV |
| Short Circuit Output Current ( $\mathrm{V}_{\text {ref }}=0 \mathrm{~V}$ ) | Isc | 15 | 35 | 75 | mA |

## OUTPUT SECTION

| Collector Off-State Current $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=40 \mathrm{~V}\right)$ | ${ }^{\text {C(off) }}$ | - | 2.0 | 100 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Emitter Off-State Current $\left.\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{E}}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {( }}$ (ff) | - | - | -100 | $\mu \mathrm{A}$ |
| Collector-Emitter Saturation Voltage (Note 2) <br> Common-Emitter ( $\mathrm{V}_{\mathrm{E}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=200 \mathrm{~mA}$ ) <br> Emitter-Follower $\left(\mathrm{V}_{\mathrm{C}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{E}}=-200 \mathrm{~mA}\right)$ | $\begin{aligned} & V_{\text {sat }(C)} \\ & V_{\text {sat }}(\mathrm{E}) \end{aligned}$ | - | $\begin{aligned} & 1.1 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 1.3 \\ & 2.5 \end{aligned}$ | V |
| Output Control Pin Current Low State ( $\mathrm{V}_{\mathrm{OC}} \leq 0.4 \mathrm{~V}$ ) High State $\left(\mathrm{V}_{\mathrm{OC}}=\mathrm{V}_{\text {ref }}\right)$ | $\begin{aligned} & \mathrm{l} \mathrm{OCL} \\ & \mathrm{loCH} \end{aligned}$ | - | $\begin{aligned} & 10 \\ & 0.2 \end{aligned}$ | $3.5$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| Output Voltage Rise Time Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13) | $\mathrm{t}_{\mathrm{r}}$ | - | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | ns |
| Output Voltage Fall Time Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13) | $t_{f}$ | - | 25 40 | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | ns |

2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right.$, unless otherwise noted.)
For typical values $T_{A}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER SECTION |  |  |  |  |  |
| Input Offset Voltage ( $\mathrm{V}_{\mathrm{O}}($ Pin 3) $=2.5 \mathrm{~V})$ | $\mathrm{V}_{10}$ | - | 2.0 | 10 | mV |
| Input Offset Current ( $\mathrm{V}_{\mathrm{O}}($ Pin 3) $=2.5 \mathrm{~V})$ | $1{ }_{10}$ | - | 5.0 | 250 | nA |
| Input Bias Current ( $\left.\mathrm{V}_{\mathrm{O}}(\operatorname{Pin} 3)=2.5 \mathrm{~V}\right)$ | $\mathrm{IIB}^{\text {I }}$ | - | -0.1 | -1.0 | $\mu \mathrm{A}$ |
| Input Common Mode Voltage Range ( $\left.\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {ICR }}$ | -0.3 to $\mathrm{V}_{\mathrm{CC}}-2.0$ |  |  | V |
| Open Loop Voltage Gain ( $\Delta \mathrm{V}_{\mathrm{O}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0.5 \mathrm{~V}$ to $\left.3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right)$ | AVOL | 70 | 95 | - | dB |
| Unity-Gain Crossover Frequency ( $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ to $3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$ ) | ${ }^{\mathrm{f}} \mathrm{C}$ - | - | 350 | - | kHz |
| Phase Margin at Unity-Gain ( $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ to $3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$ ) | $\phi_{\mathrm{m}}$ | - | 65 | - | deg. |
| Common Mode Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}$ ) | CMRR | 65 | 90 | - | dB |
| Power Supply Rejection Ratio ( $\left.\Delta \mathrm{V}_{\mathrm{CC}}=33 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=2.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right)$ | PSRR | - | 100 | - | dB |
| Output Sink Current ( $\left.\mathrm{V}_{\mathrm{O}}(\operatorname{Pin} 3)=0.7 \mathrm{~V}\right)$ | l | 0.3 | 0.7 | - | mA |
| Output Source Current ( $\mathrm{V}_{\mathrm{O}}($ Pin 3) $=3.5 \mathrm{~V}$ ) | $\mathrm{IO}^{+}$ | 2.0 | -4.0 | - | mA |

PWM COMPARATOR SECTION (Test Circuit Figure 11)

| Input Threshold Voltage (Zero Duty Cycle) | $\mathrm{V}_{\mathrm{TH}}$ | - | 2.5 | 4.5 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Sink Current $\left(\mathrm{V}_{(\text {Pin } 3)}=0.7 \mathrm{~V}\right)$ | $\mathrm{I}_{-}$ | 0.3 | 0.7 | - | mA |

DEADTIME CONTROL SECTION (Test Circuit Figure 11)

| Input Bias Current (Pin 4) (Vin 4 $=0 \mathrm{~V}$ to 5.25 V ) | $\mathrm{I}_{\mathrm{IB}(\mathrm{DT})}$ | - | -2.0 | -10 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum Duty Cycle, Each Output, Push-Pull Mode | $\mathrm{DC}_{\max }$ |  |  |  | $\%$ |
| $\left(\mathrm{~V}_{\text {Pin 4 }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right)$ | 45 | 48 | 50 |  |  |
| $\left(\mathrm{~V}_{\text {Pin 4 }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=30 \mathrm{k} \Omega\right)$ |  | - | 45 | 50 |  |
| Input Threshold Voltage (Pin 4) <br> (Zero Duty Cycle) <br> (Maximum Duty Cycle) | $\mathrm{V}_{\text {th }}$ |  |  |  | V |

OSCILLATOR SECTION

| Frequency ( $\mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=30 \mathrm{k} \Omega$ ) | $\mathrm{f}_{\text {osc }}$ | - | 40 | - | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Standard Deviation of Frequency* ( $\mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=30 \mathrm{k} \Omega$ ) | $\sigma \mathrm{f}_{\text {osc }}$ | - | 3.0 | - | \% |
| Frequency Change with Voltage ( $\mathrm{V} \mathrm{CC}=7.0 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{f}_{\text {osc }}(\Delta \mathrm{V})$ | - | 0.1 | - | \% |
| Frequency Change with Temperature $\left(\Delta \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\left.\mathrm{T}_{\text {high }}\right)$ $\left(\mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right)$ | $\Delta \mathrm{f}_{\text {osc }}(\Delta \mathrm{T})$ | - | - | 12 | \% |
| UNDERVOLTAGE LOCKOUT SECTION |  |  |  |  |  |
| Turn-On Threshold ( $\mathrm{V}_{\mathrm{CC}}$ increasing, $\mathrm{I}_{\text {ref }}=1.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {th }}$ | 5.5 | 6.43 | 7.0 | V |

TOTAL DEVICE

| Standby Supply Current (Pin 6 at $\mathrm{V}_{\text {ref }}$, All other inputs and outputs open) $\begin{aligned} & \left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}\right) \end{aligned}$ | $I_{\text {cc }}$ | - | $\begin{aligned} & 5.5 \\ & 7.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Average Supply Current } \\ & \left(\mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega, \mathrm{~V}_{(\text {Pin 4) }}=2.0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right)(\text { See Figure 12) } \end{aligned}$ |  | - | 7.0 | - | mA |

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma \sqrt{\begin{array}{l}N\left(X_{n}-X\right)^{2} \\ n=1\end{array}}$


This device contains 46 active transistors.
Figure 1. Representative Block Diagram


Figure 2. Timing Diagram

## APPLICATIONS INFORMATION

## Description

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency- programmable by two external components, $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. The approximate oscillator frequency is determined by:

$$
\mathrm{f}_{\mathrm{osc}} \approx \frac{1.1}{\mathrm{R}_{\mathrm{T}} \cdot \mathrm{C}_{\mathrm{T}}}
$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor $\mathrm{C}_{\mathrm{T}}$ to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first $4 \%$ of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of $96 \%$ with the output control grounded, and $48 \%$ with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime-control input to a fixed voltage, ranging between 0 V to 3.3 V .

Functional Table

| Input/Output <br> Controls | Output Function | $\frac{\mathbf{f}_{\text {out }}}{\mathbf{f}_{\text {osc }}}=$ |
| :---: | :--- | :---: |
| Grounded | Single-ended PWM @ Q1 and Q2 | 1.0 |
| @ $\mathrm{V}_{\text {ref }}$ | Push-pull Operation | 0.5 |

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V . Both error amplifiers have a
common mode input range from -0.3 V to $\left(\mathrm{V}_{\mathrm{CC}}-2 \mathrm{~V}\right)$, and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.
When capacitor $\mathrm{C}_{\mathrm{T}}$ is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than $50 \%$ is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $\pm 5.0 \%$ with a typical thermal drift of less than 50 mV over an operating temperature range of $0^{\circ}$ to $70^{\circ} \mathrm{C}$.


Figure 3. Oscillator Frequency versus Timing Resistance


Figure 4. Open Loop Voltage Gain and Phase versus Frequency


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current


Figure 5. Percent Deadtime versus Oscillator Frequency


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current


Figure 9. Standby Supply Current versus Supply Voltage


Figure 10. Error-Amplifier Characteristics


Figure 12. Common-Emitter Configuration Test Circuit and Waveform


Figure 11. Deadtime and Feedback Control Circuit


Figure 13. Emitter-Follower Configuration Test Circuit and Waveform


Figure 14. Error-Amplifier Sensing Techniques


Max. \% on Time, each output $\approx 45-\left(\frac{80}{1+\frac{\mathrm{R} 1}{\mathrm{R} 2}}\right)$
Figure 15. Deadtime Control Circuit


Figure 16. Soft-Start Circuit

Figure 17. Output Connections for Single-Ended and Push-Pull Configurations


Figure 18. Slaving Two or More Control Circuits


Figure 19. Operation with $\mathrm{V}_{\text {in }}>40 \mathrm{~V}$ Using External Zener


Figure 20. Pulse Width Modulated Push-Pull Converter

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=10 \mathrm{~V}$ to 40 V | $14 \mathrm{mV} 0.28 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 1.0 A | $3.0 \mathrm{mV} 0.06 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | 65 mV pp P.A.R.D. |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 1.6 A |
| Efficiency | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | $71 \%$ |

L1-3.5 mH @ 0.3 A
T1 - Primary: 20T C.T. \#28 AWG Secondary: 120T C.T. \#36 AWG Core: Ferroxcube 1408P-L00-3CB


Figure 21. Pulse Width Modulated Step-Down Converter

| Test | Conditions | Results |
| :--- | :--- | :---: |
| Line Regulation | $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$ to 40 V | $3.0 \mathrm{mV} \quad 0.01 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.2 \mathrm{~mA}$ to 200 mA | $5.0 \mathrm{mV} \quad 0.02 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ | $40 \mathrm{mV} \mathrm{pp} \quad$ P.A.R.D. |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 250 mA |
| Efficiency | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ | $72 \%$ |

## TL594

## Precision Switchmode Pulse Width Modulation Control Circuit

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control.

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference, 1.5\% Accuracy
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push-Pull or Single-Ended Operation
- Undervoltage Lockout

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 42 | V |
| Collector Output Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{C} 1}, \\ & \mathrm{~V}_{\mathrm{C} 2} \end{aligned}$ | 42 | V |
| Collector Output Current <br> (Each Transistor) (Note 1) | $\mathrm{I}_{\mathrm{C} 1}, \mathrm{I}_{\mathrm{C} 2}$ | 500 | mA |
| Amplifier Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | -0.3 to +42 | V |
| Power Dissipation @ $\mathrm{T}_{\mathrm{A}} \leq 45^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | 1000 | mW |
| Thermal Resistance Junction-to-Ambient (PDIP) Junction-to-Air (TSSOP) Junction-to-Ambient (SOIC) | $\mathrm{R}_{\text {өJA }}$ | $\begin{gathered} 80 \\ 140 \\ 135 \end{gathered}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range TL594CD, CN, CDTB | $\mathrm{T}_{\text {A }}$ | -25 to 85 | ${ }^{\circ} \mathrm{C}$ |
| Derating Ambient Temperature | $\mathrm{T}_{\text {A }}$ | 45 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum thermal limits must be observed.

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## RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 7.0 | 15 | 40 | V |
| Collector Output Voltage | $\mathrm{V}_{\mathrm{C} 1}, \mathrm{~V}_{\mathrm{C} 2}$ | - | 30 | 40 | V |
| Collector Output Current (Each transistor) | $\mathrm{I}_{\mathrm{C} 1}, \mathrm{I}_{\mathrm{C} 2}$ | - | - | 200 | mA |
| Amplified Input Voltage | $\mathrm{V}_{\mathrm{in}}$ | 0.3 | - | $\mathrm{V}_{\mathrm{CC}}-2.0$ | V |
| Current Into Feedback Terminal | $\mathrm{I}_{\mathrm{fb}}$ | - | - | 0.3 | mA |
| Reference Output Current | $\mathrm{I}_{\mathrm{ref}}$ | - | - | 10 | mA |
| Timing Resistor | $\mathrm{R}_{\mathrm{T}}$ | 1.8 | 30 | 500 | $\mathrm{k} \Omega$ |
| Timing Capacitor | $\mathrm{C}_{\mathrm{T}}$ | 0.0047 | 0.001 | 10 | $\mu \mathrm{~F}$ |
| Oscillator Frequency | $\mathrm{f}_{\mathrm{osc}}$ | 1.0 | 40 | 200 | kHz |
| PWM Input Voltage (Pins 3, 4, 13) | - | 0.3 | - | 5.3 | V |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{C}_{T}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right.$, unless otherwise noted.)
For typical values $T_{A}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | 

## OUTPUT SECTION

| Collector Off-State Current ( $\left.\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=40 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {( } \text { (ff) }}$ | - | 2.0 | 100 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Emitter Off-State Current ( $\left.\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=40 \mathrm{~V}, \mathrm{~V}_{\mathrm{E}}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {(off) }}$ | - | - | -100 | $\mu \mathrm{A}$ |
| Collector-Emitter Saturation Voltage (Note 2) <br> Common-Emitter ( $\mathrm{V}_{\mathrm{E}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=200 \mathrm{~mA}$ ) <br> Emitter-Follower $\left(\mathrm{V}_{\mathrm{C}}=15 \mathrm{~V}, \mathrm{I}_{\mathrm{E}}=-200 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{SAT}(\mathrm{C})}$ <br> $\mathrm{V}_{\mathrm{SAT}(\mathrm{E})}$ | - | $\begin{aligned} & 1.1 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 1.3 \\ & 2.5 \end{aligned}$ | V |
| Output Control Pin Current Low State ( $\mathrm{V}_{\mathrm{OC}} \leq 0.4 \mathrm{~V}$ ) High State $\left(\mathrm{V}_{\mathrm{OC}}=\mathrm{V}_{\text {ret }}\right)$ | locl loch | - | $\begin{aligned} & 0.1 \\ & 2.0 \end{aligned}$ | $\overline{20}$ | $\mu \mathrm{A}$ |
| Output Voltage Rise Time <br> Common-Emitter (See Figure 13) <br> Emitter-Follower (See Figure 14) | $\mathrm{tr}_{r}$ | - | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | $200$ | ns |
| Output Voltage Fall Time <br> Common-Emitter (See Figure 13) <br> Emitter-Follower (See Figure 14) | $\mathrm{t}_{\mathrm{f}}$ | - | $\begin{aligned} & 40 \\ & 40 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | ns |

## ERROR AMPLIFIER SECTION

| Input Offset Voltage ( $\mathrm{V}_{\mathrm{O} \text { (Pin 3) }}=2.5 \mathrm{~V}$ ) | $\mathrm{V}_{10}$ | - | 2.0 | 10 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Current ( $\mathrm{V}_{\mathrm{O}}($ Pin 3) $=2.5 \mathrm{~V}$ ) | 10 | - | 5.0 | 250 | nA |
| Input Bias Current ( $\mathrm{V}_{\text {O (Pin 3) }}=2.5 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{B}}$ | - | -0.1 | -1.0 | $\mu \mathrm{A}$ |
| Input Common Mode Voltage Range ( $\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $V_{\text {ICR }}$ | 0 to $\mathrm{V}_{\mathrm{Cc}}-2.0$ |  |  | V |
| Inverting Input Voltage Range | $\mathrm{V}_{\text {IR(INV) }}$ | -0.3 to $\mathrm{V}_{\text {CC }}-2.0$ |  |  | V |
| Open Loop Voltage Gain ( $\Delta \mathrm{V}_{\mathrm{O}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0.5 \mathrm{~V}$ to $3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$ ) | Avol | 70 | 95 | - | dB |
| Unity-Gain Crossover Frequency ( $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ to $\left.3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right)$ | $\mathrm{f}_{\mathrm{C}}$ | - | 700 | - | kHz |
| Phase Margin at Unity-Gain ( $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ to $3.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$ ) | ¢m | - | 65 | - | deg. |
| Common Mode Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}$ ) | CMRR | 65 | 90 | - | dB |
| Power Supply Rejection Ratio ( $\Delta \mathrm{V}_{\mathrm{CC}}=33 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=2.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$ ) | PSRR | - | 100 | - | dB |
| Output Sink Current ( $\mathrm{V}_{\mathrm{O}}($ Pin 3) $=0.7 \mathrm{~V}$ ) | $\mathrm{I}^{-}$ | 0.3 | 0.7 | - | mA |
| Output Source Current ( $\mathrm{V}_{\mathrm{O}}$ (Pin 3) $=3.5 \mathrm{~V}$ ) | $\mathrm{l}^{+}$ | -2.0 | -4.0 | - | mA |

2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega$, unless otherwise noted.)
For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.

| Characteristics |
| :--- |
|  Symbol Min Typ Max Unit <br>       <br> PWM COMPARATOR SECTION (Test Circuit Figure 11) $\mathrm{V}_{\text {TH }}$ - 3.6 4.5 V <br> Input Threshold Voltage (Zero Duty Cycle) $\mathrm{I}_{-}$ 0.3 0.7 - mA <br> Input Sink Current (VPin $=0.7 \mathrm{~V}$ )      |

DEADTIME CONTROL SECTION (Test Circuit Figure 11)

| Input Bias Current (Pin 4) ( $\mathrm{V}_{\text {Pin 4 }}=0 \mathrm{~V}$ to 5.25 V) | $\mathrm{I}_{\mathrm{IB}(\mathrm{DT})}$ | - | -2.0 | -10 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum Duty Cycle, Each Output, Push-Pull Mode <br> $\left(\mathrm{V}_{\text {Pin 4 }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right)$ <br> $\left(\mathrm{V}_{\text {Pin }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=30 \mathrm{k} \Omega\right)$ | $\mathrm{DC} \max$ | 45 | 48 | 50 | $\%$ |
| Input Threshold Voltage (Pin 4) <br> (Zero Duty Cycle) <br> (Maximum Duty Cycle) | $\mathrm{V}_{\mathrm{TH}}$ | - | 45 | - |  |

OSCILLATOR SECTION

| $\begin{aligned} & \text { Frequency } \\ & \begin{array}{l} \left(\mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=30 \mathrm{k} \Omega\right) \\ \left(\mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{T}=12 \mathrm{k} \Omega, \mathrm{~T}_{A}=25^{\circ} \mathrm{C}\right) \\ \left(\mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{T}=12 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}\right) \end{array} \end{aligned}$ | $\mathrm{f}_{\text {osc }}$ | $\begin{aligned} & -\overline{2} \\ & 9.2 \\ & 9.0 \end{aligned}$ | $\begin{aligned} & 40 \\ & 10 \end{aligned}$ | $\begin{gathered} - \\ 10.8 \\ 12 \end{gathered}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Standard Deviation of Frequency* ( $\mathrm{C}_{\mathrm{T}}=0.001 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=30 \mathrm{k} \Omega$ ) | $\sigma f_{\text {osc }}$ | - | 1.5 | - | \% |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ to $40 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{f}_{\text {osc }}(\Delta \mathrm{V})$ | - | 0.2 | 1.0 | \% |
| Frequency Change with Temperature $\left(\Delta \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right)$ | $\Delta \mathrm{f}_{\text {osc }}(\Delta \mathrm{T})$ | - | 4.0 | - | \% |

UNDERVOLTAGE LOCKOUT SECTION

| Turn-On Threshold (VCC Increasing, $\left.\mathrm{I}_{\text {ref }}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {th }}$ |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 4.0 | 5.2 | 6.0 |  |
| $\mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ |  | 3.5 | - | 6.5 |  |
| Hysteresis | $\mathrm{V}_{\mathrm{H}}$ |  |  |  | mV |
| TL594C,I |  | 100 | 150 | 300 |  |
| TL594M |  | 50 | 150 | 300 |  |

TOTAL DEVICE

| Standby Supply Current (Pin 6 at $\mathrm{V}_{\text {ref }}$, All other inputs and outputs <br> open $)$ <br> $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right)$ <br> $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}\right)$ | ICC | - | 8.0 | 15 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Average Supply Current $\left(\mathrm{V}_{\text {Pin }} 4=2.0 \mathrm{~V}, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega\right.$, <br> $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$, See Figure 11) |  | - | 8.0 | 18 |  |

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma \sqrt{\begin{array}{l}N\left(X_{n}-\bar{X}\right)^{2} \\ n=1 \\ N-1\end{array}}$


This device contains 46 active transistors.
Figure 1. Representative Block Diagram


Figure 2. Timing Diagram

## APPLICATIONS INFORMATION

## Description

The TL594 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency- programmable by two external components, $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. The approximate oscillator frequency is determined by:

$$
\mathrm{f}_{\mathrm{osc}} \approx \frac{1.1}{\mathrm{R}_{\mathrm{T}} \cdot \mathrm{C}_{T}}
$$

For more information refer to Figure 3.
Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor $\mathrm{C}_{\mathrm{T}}$ to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first $4 \%$ of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of $96 \%$ with the output control grounded, and $48 \%$ with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime-control input to a fixed voltage, ranging between 0 V to 3.3 V .
The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the deadtime control input, down to zero, as the voltage at the feedback


Figure 3. Oscillator Frequency versus Timing Resistance
pin varies from 0.5 V to 3.5 V . Both error amplifiers have a common-mode input range from -0.3 V to $\left(\mathrm{V}_{\mathrm{CC}}-2 \mathrm{~V}\right)$, and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

Functional Table

| Input/Output <br> Controls | Output Function | $\frac{\mathbf{f}_{\text {out }}}{\mathbf{f}_{\text {osc }}}=$ |
| :---: | :--- | :---: |
| Grounded | Single-ended PWM @ Q1 and Q2 | 1.0 |
| $@ \mathrm{~V}_{\text {ref }}$ | Push-pull Operation | 0.5 |

When capacitor $\mathrm{C}_{\mathrm{T}}$ is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than $50 \%$ is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.
The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $\pm 1.5 \%$ with a typical thermal drift of less than 50 mV over an operating temperature range of $0^{\circ}$ to $70^{\circ} \mathrm{C}$.


Figure 4. Open Loop Voltage Gain and Phase versus Frequency


Figure 5. Percent Deadtime versus Oscillator Frequency


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current


Figure 9. Standby Supply Current versus Supply Voltage


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current


Figure 11. Error-Amplifier Characteristics


Figure 13. Common-Emitter Configuration Test Circuit and Waveform


Figure 12. Deadtime and Feedback Control Circuit


Figure 14. Emitter-Follower Configuration Test Circuit and Waveform


Figure 15. Error-Amplifier Sensing Techniques


Figure 16. Deadtime Control Circuit


Figure 17. Soft-Start Circuit


Figure 18. Output Connections for Single-Ended and Push-Pull Configurations


Figure 19. Slaving Two or More Control Circuits


Figure 20. Operation with $\mathrm{V}_{\text {in }}>40 \mathrm{~V}$ Using External Zener


| Test | Conditions | Results | L1-3.5 mH @ 0.3 A <br> T1 - Primary: 20T C.T. \#28 AWG Secondary: 120T C.T. \#36 AWG Core: Ferroxcube 1408P-L00-3CB |
| :---: | :---: | :---: | :---: |
| Line Regulation | $\mathrm{V}_{\text {in }}=10 \mathrm{~V}$ to 40 V | $14 \mathrm{mV} \mathrm{0.28} \mathrm{\%}$ |  |
| Load Regulation | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 1.0 A | 3.0 mV 0.06\% |  |
| Output Ripple | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | 65 mVpp P.A.R.D. |  |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | 1.6 A |  |
| Efficiency | $\mathrm{V}_{\text {in }}=28 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~A}$ | 71\% |  |

Figure 21. Pulse Width Modulated Push-Pull Converter


| Test | Conditions | Results |
| :--- | :--- | :---: |
| Line Regulation | $\mathrm{V}_{\text {in }}=8.0 \mathrm{~V}$ to 40 V | 3.0 mV |
| Load Regulation | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.2 \mathrm{~mA}$ to 200 mA | 5.0 mV |
| Output Ripple | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ | 40 mVpp |
| Short Circuit Current | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=0.1 \Omega$ | P.A.R.D. |
| Efficiency | $\mathrm{V}_{\text {in }}=12.6 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=200 \mathrm{~mA}$ | 250 mA |

Figure 22. Pulse Width Modulated Step-Down Converter

## SG3525A

## Pulse Width <br> Modulator Control Circuit

The SG3525A pulse width modulator control circuit offers improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 V reference is trimmed to $\pm 1 \%$ and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of deadtime can be programmed by a single resistor connected between the $\mathrm{C}_{\mathrm{T}}$ and Discharge pins. This device also features built-in soft-start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when $\mathrm{V}_{\mathrm{CC}}$ is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA . The output stage of the SG3525A features NOR logic resulting in a low output for an off-state.

- 8.0 V to 35 V Operation
- $5.1 \mathrm{~V} \pm 1.0 \%$ Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: $\pm 400 \mathrm{~mA}$ Peak


Figure 1. Representative Block Diagram


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PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| SG3525AN | PDIP-16 | 25 Units/Rail |

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | +40 | Vdc |
| Collector Supply Voltage | $\mathrm{V}_{\mathrm{C}}$ | +40 | Vdc |
| Logic Inputs |  | -0.3 to +5.5 | V |
| Analog Inputs |  | -0.3 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Output Current, Source or Sink | $\mathrm{I}_{\mathrm{O}}$ | $\pm 500$ | mA |
| Reference Output Current | $\mathrm{I}_{\text {ref }}$ | 50 | mA |
| Oscillator Charging Current |  | 5.0 | mA |
| Power Dissipation (Plastic \& Ceramic Package) <br> $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (Note 2) <br> $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ (Note 3) | $\mathrm{P}_{\mathrm{D}}$ | mW |  |
| Thermal Resistance Junction-to-Air |  | $\mathrm{R}_{\text {өJA }}$ | 1000 |
| Thermal Resistance Junction-to-Case | $\mathrm{R}_{\text {өJC }}$ | 2000 |  |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Lead Temperature (Soldering, 10 seconds) | $\mathrm{T}_{\text {Solder }}$ | ${ }^{\circ} \mathrm{C}$ |  |

## RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 8.0 | 35 | Vdc |
| Collector Supply Voltage | $\mathrm{V}_{\mathrm{C}}$ | 4.5 | 35 | Vdc |
| Output Sink/Source Current <br> (Steady State) <br> (Peak) | $\mathrm{I}_{\mathrm{O}}$ |  |  | mA |
| Reference Load Current |  | 0 | $\pm 100$ |  |
| Oscillator Frequency Range | 0 | $\pm 400$ |  |  |
| Oscillator Timing Resistor | $\mathrm{I}_{\mathrm{ref}}$ | 0 | 20 | mA |
| Oscillator Timing Capacitor | $\mathrm{f}_{\mathrm{osc}}$ | 0.1 | 400 | kHz |
| Deadtime Resistor Range | $\mathrm{R}_{\mathrm{T}}$ | 2.0 | 150 | $\mathrm{k} \Omega$ |
| Operating Ambient Temperature Range | $\mathrm{C}_{\mathrm{T}}$ | 0.001 | 0.2 | $\mu \mathrm{~F}$ |

1. Values beyond which damage may occur.
2. Derate at $10 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for ambient temperatures above $+50^{\circ} \mathrm{C}$.
3. Derate at $16 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for case temperatures above $+25^{\circ} \mathrm{C}$.

## APPLICATION INFORMATION

## Shutdown Options (See Block Diagram, front page)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of $100 \mu \mathrm{~A}$ to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM
latch is immediately set providing the fastest turn-off signal to the outputs; and a $150 \mu \mathrm{~A}$ current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+20 \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 4], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| Reference Output Voltage ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | Vef | 5.00 | 5.10 | 5.20 | Vdc |
| Line Regulation ( $+8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq+35 \mathrm{~V}$ ) | $\mathrm{Reg}_{l i n e}$ | - | 10 | 20 | mV |
| Load Regulation ( $0 \mathrm{~mA} \leq \mathrm{I}_{\mathrm{L}} \leq 20 \mathrm{~mA}$ ) | Reg ${ }_{\text {load }}$ | - | 20 | 50 | mV |
| Temperature Stability | $\Delta \mathrm{V}_{\text {ref }} / \Delta T$ | - | 20 | - | mV |
| Total Output Variation Includes Line and Load Regulation over Temperature | $\Delta \mathrm{V}_{\text {ref }}$ | 4.95 | - | 5.25 | Vdc |
| Short Circuit Current $\left(\mathrm{V}_{\text {ref }}=0 \mathrm{~V}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C}\right)$ | $I_{\text {SC }}$ | - | 80 | 100 | mA |
| Output Noise Voltage ( $\left.10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 40 | 200 | $\mu \mathrm{V}_{\text {rms }}$ |
| Long Term Stability ( $\mathrm{T}_{\mathrm{J}}=+125^{\circ} \mathrm{C}$ ) (Note 5) | S | - | 20 | 50 | $\mathrm{mV} / \mathrm{khr}$ |

OSCILLATOR SECTION (Note 6, unless otherwise noted.)

| Initial Accuracy ( $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) |  | - | $\pm 2.0$ | $\pm 6.0$ | \% |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Stability with Voltage $\left(+8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq+35 \mathrm{~V}\right)$ | $\frac{\Delta \mathrm{f}_{\mathrm{osc}}}{\mathrm{D}_{\mathrm{VCC}}}$ | - | $\pm 1.0$ | $\pm 2.0$ | \% |
| Frequency Stability with Temperature | $\frac{\Delta f_{\text {osc }}}{D \quad T}$ | - | $\pm 0.3$ | - | \% |
| Minimum Frequency ( $\mathrm{R}_{\mathrm{T}}=150 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=0.2 \mu \mathrm{~F}$ ) | $\mathrm{f}_{\text {min }}$ | - | 50 | - | Hz |
| Maximum Frequency ( $\mathrm{R}_{\mathrm{T}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}$ ) | $\mathrm{f}_{\text {max }}$ | 400 | - | - | kHz |
| Current Mirror ( $\mathrm{l}_{\mathrm{RT}}=2.0 \mathrm{~mA}$ ) |  | 1.7 | 2.0 | 2.2 | mA |
| Clock Amplitude |  | 3.0 | 3.5 | - | V |
| Clock Width ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) |  | 0.3 | 0.5 | 1.0 | $\mu \mathrm{s}$ |
| Sync Threshold |  | 1.2 | 2.0 | 2.8 | V |
| Sync Input Current (Sync Voltage $=+3.5 \mathrm{~V}$ ) |  | - | 1.0 | 2.5 | mA |

ERROR AMPLIFIER SECTION $\left(\mathrm{V}_{\mathrm{CM}}=+5.1 \mathrm{~V}\right.$ )

| Input Offset Voltage | $\mathrm{V}_{\mathrm{IO}}$ | - | 2.0 | 10 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | $\mathrm{I}_{\mathrm{IB}}$ | - | 1.0 | 10 | $\mu \mathrm{~A}$ |
| Input Offset Current | $\mathrm{I}_{\mathrm{IO}}$ | - | - | 1.0 | $\mu \mathrm{~A}$ |
| DC Open Loop Gain $\left(\mathrm{R}_{\mathrm{L}} \geq 10 \mathrm{M} \Omega\right)$ | $\mathrm{A}_{\mathrm{VOL}}$ | 60 | 75 | - | dB |
| Low Level Output Voltage | $\mathrm{V}_{\mathrm{OL}}$ | - | 0.2 | 0.5 | V |
| High Level Output Voltage | $\mathrm{V}_{\mathrm{OH}}$ | 3.8 | 5.6 | - | V |
| Common Mode Rejection Ratio $\left(+1.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CM}} \leq+5.2 \mathrm{~V}\right)$ | CMRR | 60 | 75 | - | dB |
| Power Supply Rejection Ratio $\left(+8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq+35 \mathrm{~V}\right)$ | PSRR | 50 | 60 | - | dB |

PWM COMPARATOR SECTION

| Minimum Duty Cycle | $\mathrm{DC}_{\min }$ | - | - | 0 | $\%$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Maximum Duty Cycle | $\mathrm{DC}_{\max }$ | 45 | 49 | - | $\%$ |
| Input Threshold, Zero Duty Cycle (Note 6) | $\mathrm{V}_{\text {th }}$ | 0.6 | 0.9 | - | V |
| Input Threshold, Maximum Duty Cycle (Note 6) | $\mathrm{V}_{\text {th }}$ | - | 3.3 | 3.6 | V |
| Input Bias Current | $\mathrm{I}_{\mathrm{IB}}$ | - | 0.05 | 1.0 | $\mu \mathrm{~A}$ |

4. $\mathrm{T}_{\text {low }}=0^{\circ} \quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at $\mathrm{f}_{\text {osc }}=40 \mathrm{kHz}\left(\mathrm{R}_{\mathrm{T}}=3.6 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{D}}=0 \Omega\right)$.

ELECTRICAL CHARACTERISTICS (Continued)

| Characteristics | Symbol | Min | Typ | Max | Unit |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SOFT-START SECTION |  |  |  |  |  |  |  |
| Soft-Start Current $\left(V_{\text {shutdown }}=0 \mathrm{~V}\right)$ |  | 25 | 50 | 80 | $\mu \mathrm{~A}$ |  |  |
| Soft-Start Voltage $\left(\mathrm{V}_{\text {shutdown }}=2.0 \mathrm{~V}\right)$ |  | - | 0.4 | 0.6 | V |  |  |
| Shutdown Input Current $\left(\mathrm{V}_{\text {shutdown }}=2.5 \mathrm{~V}\right)$ |  | - | 0.4 | 1.0 | mA |  |  |

OUTPUT DRIVERS (Each Output, $\mathrm{V}_{\mathrm{CC}}=+20 \mathrm{~V}$ )

| $\begin{gathered} \text { Output Low Level } \\ \left(I_{\text {sink }}=20 \mathrm{~mA}\right) \\ \left(l_{\text {sink }}=100 \mathrm{~mA}\right) \end{gathered}$ | $\mathrm{V}_{\mathrm{OL}}$ |  | $\begin{aligned} & 0.2 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 2.0 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output High Level $\begin{aligned} & \left(I_{\text {source }}=20 \mathrm{~mA}\right) \\ & \left(\mathrm{I}_{\text {source }}=100 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 18 \\ & 17 \end{aligned}$ | $\begin{aligned} & 19 \\ & 18 \end{aligned}$ | - | V |
| Under Voltage Lockout (V8 and V9 = High) | $\mathrm{V}_{\mathrm{UL}}$ | 6.0 | 7.0 | 8.0 | V |
| Collector Leakage, $\mathrm{V}_{\mathrm{C}}=+35 \mathrm{~V}$ (Note 7) | $\mathrm{I}_{\text {(leak }}$ | - | - | 200 | $\mu \mathrm{A}$ |
| Rise Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{t}_{\mathrm{r}}$ | - | 100 | 600 | ns |
| Fall Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $t_{f}$ | - | 50 | 300 | ns |
| Shutdown Delay ( $\left.\mathrm{V}_{\mathrm{DS}}=+3.0 \mathrm{~V}, \mathrm{C}_{\mathrm{S}}=0, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\mathrm{ds}}$ | - | 0.2 | 0.5 | $\mu \mathrm{s}$ |
| Supply Current ( $\left.\mathrm{V}_{\mathrm{CC}}=+35 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{Cc}}$ | - | 14 | 20 | mA |

7. Applies to SG3525A only, due to polarity of output pulses.


Figure 2. Lab Test Fixture


Figure 3. Oscillator Charge Time versus $\mathbf{R}_{\mathbf{T}}$


Figure 5. Error Amplifier Open Loop Frequency Response


Figure 4. Oscillator Discharge Time versus $\mathbf{R}_{\mathbf{D}}$


Figure 6. Output Saturation Characteristics


Figure 7. Oscillator Schematic


Figure 8. Error Amplifier Schematic


Figure 9. Output Circuit
(1/2 Circuit Shown)


For single-ended supplies, the driver outputs are grounded. The $\mathrm{V}_{\mathrm{C}}$ terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 10. Single-Ended Supply


The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Figure 12. Driving Power FETS


In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C 1 and C 2 .

Figure 11. Push-Pull Configuration


Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

Figure 13. Driving Transformers in a Half-Bridge Configuration

## CS3524A

## Voltage Mode <br> PWM Control Circuit with 200 mA Output Drivers

The CS3524A PWM control circuit retains the same versatile architecture of the industry standard CS3524 (SG3524) while adding substantial improvements.

The CS3524 is pin-compatible with "non-A" versions, and in most applications can be directly interchanged. The CS3524A, however, eliminates many of the design restrictions which had previously required additional external circuitry.

The CS3524A includes a precision 5.0 V reference trimmed to $\pm 1 \%$ accuracy (eliminating the need for potentiometer adjustments), an error amplifier with an output voltage swing extending to 5.0 V , and a current sense amplifier useful in either the ground or power supply output lines. The uncommitted $60 \mathrm{~V}, 200 \mathrm{~mA}$ NPN output pair greatly enhances the output drive capability.

The CS3524A features an undervoltage lockout circuit which disables all internal circuitry (except the reference) until the input voltage has risen to 8.0 V . This holds standby current low until turn-on, and greatly simplifies the design of low power, off-line supplies. The turn-on circuit has approximately 600 mV of hysteresis for jitter free activation.

Other improvements include a PWM latch that insures freedom from multiple pulsing within a period, even in noisy environments; logic to eliminate double pulsing on a single output, a 200 ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit is usable to 500 kHz and is easier to synchronize with an external clock pulse.

## Features

- Precision Reference Internally Trimmed to $\pm 1 \%$
- Current Limit
- Undervoltage Lockout
- Start-Up Supply Current < 4.0 mA
- Output to 200 mA
- 60 V Output Capability
- Wide Common-Mode Input Range for Error and Current Limit Amplifiers
- PWM Latch Insures Single Pulse per Period
- Double Pulse Suppression
- 200 ns Shutdown
- Guaranteed Frequency
- Thermal Shutdown



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PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS3524AGN16 | DIP-16 | 25 Units/Rail |
| CS3524AGDW16 | SO-16L | 46 Units/Rail |
| CS3524AGDWR16 | SO-16L | 1000 Tape \& Reel |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ) | 40 | V |
| Collector Supply Voltage $\left(\mathrm{V}_{\mathrm{CC}}\right)$ | 60 | V |
| Output Current (Each Output) | 200 | mA |
| Reference Output Current | 50 | mA |
| Oscillator Charging Current | 5.0 | mA |
| Power Dissipation at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 1000 | mW |
| Power Dissipation at $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ <br> Derate for Case Temperature above $+25^{\circ} \mathrm{C}$ | 2000 |  |
| Storage Temperature Range | 16 | mW |
| Lead Temperature Soldering | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Turn-On Characteristics |  |  |  |  |  |
| Input Voltage | Operating Range after Turn-On | 8.0 | - | 40 | V |
| Turn-On Threshold | - | 5.5 | 7.5 | 8.5 | V |
| Turn-On Current | $\mathrm{V}_{\text {IN }}$ Turn-On-100 mV | - | 2.5 | 4.0 | mA |
| Operating Current | $\mathrm{V}_{\mathrm{IN}}=8.0$ to 40 V | - | 5.0 | 10 | mA |
| Turn-On Hysteresis (Note 3) | - | - | 0.6 | - | V |

Reference Section

| Output Voltage | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 4.9 | 5.0 | 5.2 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Line Regulation | $\mathrm{V}_{\mathrm{IN}}=10$ to 40 V | - | 10 | 30 | mV |
| Load Regulation | $\mathrm{I}_{\mathrm{L}}=0$ to 20 mA | - | 20 | 50 | mA |
| Temperature Stability (Note 3) | Over Operating Range | - | 20 | 50 | mV |
| Short Circuit Current | $\mathrm{V}_{\mathrm{REF}}=0, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 80 | 100 | mA |
| Output Noise Voltage (Note 3) | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 40 | - | $\mu \mathrm{V}_{\mathrm{RMS}}$ |
| Long Term Stability (Note 3) | $\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}, 1000 \mathrm{Hrs}$. | - | 20 | 50 | mV |

Oscillator Section $\quad R_{T}=2700 \Omega, \mathbf{C}_{T}=0.01 \mu \mathrm{~F}$; unless otherwise specified

| Initial Accuracy | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 39 | 43 | 47 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Temperature Stability (Note 3) | Over Operating Temperature Range | - | 1.0 | 2.0 | $\%$ |
| Minimum Frequency | $\mathrm{R}_{\mathrm{T}}=150 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=0.1 \mu \mathrm{~F}$ | - | - | 120 | Hz |
| Maximum Frequency | $\mathrm{R}_{\mathrm{T}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=470 \mathrm{pF}$ | 500 | - | - | kHz |
| Output Amplitude (Note 3) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 3.5 | - | V |
| Output Pulse Width (Note 3) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 0.5 | - | $\mu \mathrm{s}$ |
| Ramp Peak |  | 3.3 | 3.5 | 3.7 | V |
| Ramp Valley | - | 0.7 | 0.9 | 1.0 | V |

## Error Amplifier Section $\quad \mathrm{V}_{\mathbf{C M}}=\mathbf{2 . 5} \mathrm{V}$; unless otherwise specified

| Input Offset Voltage | - | - | 2.0 | 10 | mV |
| :--- | :--- | :--- | :--- | :---: | :---: |
| Input Bias Current | - | - | 1.0 | 10 | $\mu \mathrm{~A}$ |
| Input Offset Current | - | - | 0.5 | 1.0 | $\mu \mathrm{~A}$ |
| Common Mode Rejection Ratio | $\mathrm{V}_{\mathrm{CM}}=1.5$ to 5.5 V | 60 | 75 | - | dB |
| Power Supply Rejection Ratio | $\mathrm{V}_{\text {IN }}=10$ to 40 V | 50 | 60 | - | dB |
| Output Swing | Minimum Total Range | 0.5 | - | 5.0 | V |
| Open Loop Voltage Gain | $\Delta \mathrm{V}_{\text {OUT }}=1.0$ to $4.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geq 10 \mathrm{M} \Omega$ | 60 | 80 | - | dB |
| Gain-Bandwidth (Note 3) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{A}_{\mathrm{V}}=0 \mathrm{~dB}$ | - | 3.0 | - | MHz |

Current Limit Amplifier

| Input Offset Voltage | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, EA Set for Max. Output | 180 | 200 | 220 | mV |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage | Over Operating Temperature Range | 170 | - | 230 | mV |  |
| Input Bias Current |  |  |  |  |  |  |
| Common Mode Rejection Ratio | $V_{\text {SENSE }}=0$ to 15 V | - | -1.0 | -10 | $\mu \mathrm{~A}$ |  |
| Power Supply Rejection Ratio | $\mathrm{V}_{\text {IN }}=10$ to 40 V | 50 | 60 | - | dB |  |

3. These parameters are guaranteed by design but not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Limit Amplifier (continued) | $\mathrm{V}_{\text {SENSE }}=\mathrm{V}_{\mathrm{O}}$; unless otherwise specified |  |  |  |  |
| Output Swing | Minimum Total Range | 0.5 | - | 5.0 | V |
| Open Loop Voltage Gain | $\Delta \mathrm{V}_{\text {OUT }}=1.0$ to $4.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}} \geq 10 \mathrm{M} \Omega$ | 70 | 80 | - | dB |
| Delay Time (Note 4) | $\Delta \mathrm{V}_{\text {IN }}=300 \mathrm{mV}$ | - | 300 | - | ns |

Output Section (Each Output)

| Collector Emitter Voltage | $\mathrm{I}_{\mathrm{C}}=100 \mu \mathrm{~A}$ | 60 | 80 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Collector Leakage Current | $\mathrm{V}_{\mathrm{CE}}=50 \mathrm{~V}$ | - | 0.1 | 20 | $\mu \mathrm{~A}$ |
| Saturation | $\mathrm{I}_{\mathrm{C}}=20 \mathrm{~mA}$ | - | 0.2 | 0.4 | V |
|  | $\mathrm{I}_{\mathrm{C}}=200 \mathrm{~mA}$ | - | 1.0 | 2.2 | V |
| Emitter Output Voltage | $\mathrm{I}_{\mathrm{E}}=50 \mathrm{~mA}$ | 17 | 18 | - | V |
| Rise Time (Note 4) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}=2.0 \mathrm{k} \Omega$ | - | 200 | - | ns |
| Fall Time (Note 4) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}=2.0 \mathrm{k} \Omega$ | - | 100 | - | ns |
| Comparator Delay (Note 4) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\text {COMP }}$ to $\mathrm{V}_{\text {OUT }}$ | - | 300 | - | ns |
| Shutdown Delay (Note 4) | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\text {SHUT }}$ to $\mathrm{V}_{\mathrm{OUT}}$ | - | 200 | - | ns |
| Shutdown Threshold | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{C}}=2.0 \mathrm{k} \Omega$ | 0.5 | 0.7 | 1.0 | V |
| Thermal Shutdown (Note 4) | $-\quad-$ | 165 | - | ${ }^{\circ} \mathrm{C}$ |  |

4. These parameters are guaranteed by design but not $100 \%$ tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Error Amplifier Voltage Gain vs. Frequency Over RF


Figure 3. Duty Cycle vs. Input Voltage


Figure 4. Quiescent Supply Current vs. Supply Voltage Over Temperature


Figure 6. Oscillator Frequency vs. Timing Components Resistor Over Timing Capacitance


Figure 8. Current Limit Amplifier Delay


Figure 5. Shutdown Delay from PWM Comparator


Figure 7. Output Dead Time vs. Timing Capacitor Value


Figure 9. Turn-Off Delay from Shutdown


Figure 10. Output Saturation Voltage vs. Output Current Over Temperature


Figure 11. Open Loop Test Circuit

Note: The CS3524A should be able to be tested in any 3524 test circuit with two possible exceptions:

1. The higher gain-bandwidth of the current limit amplifier in the CS3524A may cause oscillations in an uncompensated 3524 test circuit.
2. The effect of the shutdown cannot be seen at the compensation terminal, but must be observed at the outputs.

PACKAGE THERMAL DATA

| Parameter |  | DIP-16 | SO-16L | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 42 | 23 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 80 | 105 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS51221

## Enhanced Voltage Mode PWM Controller

The CS51221 fixed frequency feed forward voltage mode PWM controller contains all of the features necessary for basic voltage mode operation. This PWM controller has been optimized for high frequency primary side control operation. In addition, this device includes such features as: Soft Start, accurate duty cycle limit control, less than $50 \mu \mathrm{~A}$ startup current, over and under voltage protection, and bidirectional synchronization. The CS51221 is available in a 16 lead SO narrow surface mount package.

## Features

- 1.0 MHz Frequency Capability
- Fixed Frequency Voltage Mode Operation, with Feed Forward
- Thermal Shutdown
- Undervoltage Lock-Out
- Accurate Programmable Max Duty Cycle Limit
- 1.0 A Sink/Source Gate Drive
- Programmable Pulse-By-Pulse Overcurrent Protection
- Leading Edge Current Sense Blanking
- 75 ns Shutdown Propagation Delay
- Programmable Soft Start
- Undervoltage Protection
- Overvoltage Protection with Programmable Hysteresis
- Bidirectional Synchronization
- 25 ns GATE Rise and Fall Time (1.0 nF Load)
- 3.3 V 3\% Reference Voltage Output

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


SO-16
D SUFFIX
CASE 751B

PIN CONNECTIONS AND MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51221ED16 | SO-16 | 48 Units/Rail |
| CS51221EDR16 | SO-16 | 2500 Tape \& Reel |



## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Operating Junction Temperature, $T_{J}$ | Reflow: (SMD styles only) (Note 1$)$ | 230 peak |
| Lead Temperature Soldering: |  | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $T_{S}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD (Humally |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gate Drive Output | GATE | 15 V | -0.3 V | 1.0 A Peak, 200 mA DC | 1.0 A Peak, 200 mA DC |
| Current Sense Input | $I_{\text {SENSE }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Timing Resistor/Capacitor | $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ | 6.0 V | -0.3 V | 1.0 mA | 10 mA |
| Feed Forward | FF | 6.0 V | -0.3 V | 1.0 mA | 25 mA |
| Error Amp Output | COMP | 6.0 V | -0.3 V | 10 mA | 20 mA |
| Feedback Voltage | $V_{F B}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Sync Input | SYNC | 6.0 V | -0.3 V | 10 mA | 10 mA |
| Undervoltage | UV | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Overvoltage | OV | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Set | $\mathrm{I}_{\text {SET }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Soft Start | SS | 6.0 V | -0.3 V | 1.0 mA | 10 mA |
| Logic Section Supply | $\mathrm{V}_{\mathrm{CC}}$ | 15 V | -0.3 V | 10 mA | 50 mA |
| Power Section Supply | $\mathrm{V}_{\mathrm{C}}$ | 15 V | -0.3 V | 10 mA | 1.0 A Peak, 200 mA DC |
| Reference Voltage | $V_{\text {REF }}$ | 6.0 V | -0.3 V | Internally Limited | 10 mA |
| Power Ground | PGND | N/A | N/A | 1.0 A Peak, 200 mA DC | N/A |
| Logic Ground | LGND | N/A | N/A | N/A | N/A |

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<15 \mathrm{~V} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<15 \mathrm{~V}\right.$; $\mathrm{R}_{\mathrm{T}}=12 \mathrm{k} ; \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Start/Stop Voltages |  |  |  |  |  |
| Start Threshold | - | 4.4 | 4.6 | 4.7 | V |
| Stop Threshold | - | 3.2 | 3.8 | 4.1 | V |
| Hysteresis | Start-Stop | 400 | 850 | 1400 | mV |
| ICC @ Startup | $\mathrm{V}_{\text {CC }}<$ UVL Start Threshold | - | 38 | 75 | $\mu \mathrm{A}$ |
| Supply Current |  |  |  |  |  |
| ICC Operating | - | - | 9.5 | 14 | mA |
| $I_{C}$ Operating | 1.0 nF Load on GATE | - | 12 | 18 | mA |
| $\mathrm{I}_{\mathrm{C}}$ Operating | No Switching | - | 2.0 | 4.0 | mA |

Reference Voltage

| Total Accuracy | $0 \mathrm{~mA}<\mathrm{I}_{\text {REF }}<2.0 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| :--- | :--- | :--- | :--- | :--- | :---: |

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<15 \mathrm{~V} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<15 \mathrm{~V}\right.$; $R_{T}=12 \mathrm{k} ; \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Reference Voltage (continued) |  |  |  |  |  |  |
| Line Regulation |  | - | - | 6.0 | 20 | mV |
| Load Regulation | $0 \mathrm{~mA}<\mathrm{I}_{\mathrm{REF}}<2.0 \mathrm{~mA}$ | - | 6.0 | 15 | mV |  |
| Noise Voltage | $10 \mathrm{~Hz}<\mathrm{F}<10 \mathrm{kHz}$. Note 2 | - | 50 | - | $\mu \mathrm{l}$ |  |
| Op Life Shift | $\mathrm{T}=1000 \mathrm{Hrs}$. Note 2 | - | 4.0 | 20 | mV |  |
| Fault Voltage | - | 2.8 | 2.95 | 3.1 | V |  |
| $\mathrm{~V}_{\text {REF(OK) }}$ Voltage | - | 2.9 | 3.05 | 3.2 | V |  |
| $\mathrm{~V}_{\text {REF(OK) }}$ Hysteresis | - | 30 | 100 | 150 | mV |  |
| Current Limit | - | 2.0 | 40 | 100 | mA |  |

## Error Amp

| Reference Voltage | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ | 1.234 | 1.263 | 1.285 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FB}}$ Input Current | $\mathrm{V}_{\mathrm{FB}}=1.2 \mathrm{~V}$ | - | 1.3 | 2.0 | $\mathrm{\mu A}$ |
| Open Loop Gain | Note 2 | 60 | - | - | dB |
| Unity Gain Bandwidth | Note 2 | 1.5 | - | - | MHz |
| COMP Sink Current | $\mathrm{COMP}=1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.45 \mathrm{~V}$ | 3.0 | 12 | 32 | mA |
| COMP Source Current | $\mathrm{COMP}=1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.15 \mathrm{~V}$ | 1.0 | 1.6 | 2.0 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=1.15 \mathrm{~V}$ | 2.8 | 3.1 | 3.4 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=1.45 \mathrm{~V}$ | 75 | 125 | 300 | mV |
| PSRR | $\mathrm{Freq}=120 \mathrm{~Hz}$. Note 2 | 60 | 85 | - | dB |
| SS Clamp, $\mathrm{V}_{\mathrm{COMP}}$ | $\mathrm{SS}=1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{SET}}=2.0 \mathrm{~V}$ | 1.3 | 1.4 | 1.5 | V |
| COMP Max Clamp | Note 2 | 1.7 | 1.8 | 1.9 | V |

## Oscillator

| Frequency Accuracy | - | 260 | 273 | 320 | kHz |  |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Voltage Stability | - | - | 1.0 | 2.0 | $\%$ |  |
| Temperature Stability | $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$. Note 2 | - | 8.0 | - | $\%$ |  |
| Max Frequency | Note 2 |  | 1.0 | - | - | MHz |
| Duty Cycle |  | - | 80 | 85 | 90 | $\%$ |
| Peak Voltage | Note 2 |  | 1.94 | 2.0 | 2.06 | V |
| Valley Clamp Voltage | Note 2 |  | 0.9 | 0.95 | 1.0 | V |
| Valley Voltage |  | 0.85 | 1.0 | 1.15 | V |  |
| Discharge Current |  | 0.85 | 1.0 | 1.15 | mA |  |

## Synchronization

| Input Threshold | - | 0.9 | 1.4 | 1.8 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Pulse Width | - | 200 | 320 | 450 | ns |
| Output High Voltage | $100 \mu \mathrm{~A}$ Load | 2.1 | 2.5 | 2.8 | V |
| Input Resistance | - | 35 | 70 | 140 | k $\Omega$ |
| SYNC to Drive Delay | Time from SYNC to GATE Shutdown | 100 | 140 | 180 | ns |
| Output Drive Current | $\mathrm{R}_{\text {SYNC }}=1.0 \Omega$ | 1.0 | 1.5 | 2.25 | mA |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<15 \mathrm{~V} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<15 \mathrm{~V}\right.$; $R_{T}=12 \mathrm{k} ; \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATE Driver |  |  |  |  |  |
| High Saturation Voltage | $\mathrm{V}_{\mathrm{C}}-\mathrm{GATE}, \mathrm{V}_{\mathrm{C}}=10 \mathrm{~V}$, $\mathrm{I}_{\text {SOURCE }}=200 \mathrm{~mA}$ | - | 1.5 | 2.0 | V |
| Low Saturation Voltage | GATE - PGND, ISINK $=200 \mathrm{~mA}$ | - | 1.2 | 1.5 | V |
| High Voltage Clamp | - | 11 | 13.5 | 16 | V |
| Output Current | 1.0 nF Load. Note 3 | - | 1.0 | 1.25 | A |
| Output UVL Leakage | GATE $=0 \mathrm{~V}$ | - | 1.0 | 50 | $\mu \mathrm{A}$ |
| Rise Time | 1.0 nF Load, $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}, 1.0 \mathrm{~V}<$ GATE $<9.0 \mathrm{~V}$ | - | 60 | 100 | ns |
| Fall Time | 1.0 nF Load, $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}, 9.0 \mathrm{~V}<\mathrm{GATE}<1.0 \mathrm{~V}$ | - | 25 | 50 | ns |
| Max Gate Voltage During UVL/Sleep | $\mathrm{I}_{\text {GATE }}=500 \mu \mathrm{~A}$ | 0.4 | 0.7 | 1.0 | V |

Feed Forward (FF)

| Discharge Voltage | $\mathrm{I}_{\mathrm{FF}}=2.0 \mathrm{~mA}$ | - | 0.3 | 0.7 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | FF $=1.0 \mathrm{~V}$ | 2.0 | 16 | 30 | mA |
| FF to GATE Delay |  | 50 | 75 | 125 | ns |

## Overcurrent Protection

| Overcurrent Threshold | $\mathrm{I}_{\text {SET }}=0.5 \mathrm{~V}$, Ramp ISENSE | 0.475 | 0.5 | 0.525 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| ISENSE to GATE Delay | - | 50 | 90 | 125 | ns |

External Voltage Monitors

| Overvoltage Threshold | OV Increasing | 1.9 | 2.0 | 2.1 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Overvoltage Hysteresis Current | OV = 2.15 V | 10 | 12.5 | 15 | $\mu \mathrm{~A}$ |
| Undervoltage Threshold | UV Increasing | 0.95 | 1.0 | 1.05 | V |
| Undervoltage Hysteresis |  | 25 | 75 | 125 | mV |

Soft Start (SS)

| Charge Current | SS $=2.0 \mathrm{~V}$ | 40 | 50 | 70 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | $\mathrm{SS}=2.0 \mathrm{~V}$ | 4.0 | 5.0 | 7.0 | $\mu \mathrm{~A}$ |
| Charge Voltage |  | - | 2.8 | 3.0 | 3.4 |
| Discharge Voltage |  | 0.25 | 0.3 | 0.35 | V |
| Soft Start Clamp Offset | $\mathrm{FF}=1.25 \mathrm{~V}$ | 1.15 | 1.25 | 1.35 | V |
| Soft Start Fault Voltage | $\mathrm{OV}=2.15 \mathrm{~V}$ or LV $=0.85 \mathrm{~V}$ | - | 0.1 | 0.2 | V |

## Blanking

| Blanking Time | - | 50 | 150 | 250 | ns |
| :--- | :--- | :--- | :--- | :--- | :--- |
| SS Blanking Disable Threshold | $\mathrm{V}_{\mathrm{FB}}<1.0$ | 2.8 | 3.0 | 3.3 | V |
| COMP Blanking Disable Threshold | $\mathrm{V}_{\mathrm{FB}}<1.0, \mathrm{SS}>3.0 \mathrm{~V}$ | 2.8 | 3.0 | 3.3 | V |

## Thermal Shutdown

| Thermal Shutdown | Note 3 | 125 | 150 | 180 | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Thermal Hysteresis | Note 3 | 5.0 | 10 | 15 | ${ }^{\circ} \mathrm{C}$ |

3. Guaranteed by design, not $100 \%$ tested in production.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-16 | PIN SYMBOL | FUNCTION |
| 1 | GATE | External power switch driver with 1.0 A peak capability. Rail to rail output occurs when the capacitive load is between 470 pF and 10 nF . |
| 2 | $I_{\text {SENSE }}$ | Current sense comparator input. |
| 3 | SYNC | Bidirectional synchronization. Locks to highest frequency. |
| 4 | FF | PWM ramp. |
| 5 | UV | Undervoltage protection monitor. |
| 6 | OV | Overvoltage protection monitor. |
| 7 | $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ | Timing resistor $\mathrm{R}_{\mathrm{T}}$ and capacitor $\mathrm{C}_{\mathrm{T}}$ determine oscillator frequency and maximum duty cycle, $\mathrm{D}_{\mathrm{MAX}}$. |
| 8 | $\mathrm{I}_{\text {SET }}$ | Voltage at this pin sets pulse-by-pulse overcurrent threshold. |
| 9 | $V_{F B}$ | Feedback voltage input. Connected to the error amplifier inverting input. |
| 10 | COMP | Error amplifier output. |
| 11 | SS | Charging external capacitor restricts error amplifier output voltage during the power up or fault conditions. |
| 12 | LGND | Logic ground. |
| 13 | $\mathrm{V}_{\text {REF }}$ | 3.3 V reference voltage output. Decoupling capacitor can be selected from $0.01 \mu \mathrm{~F}$ to $10 \mu \mathrm{~F}$. |
| 14 | $\mathrm{V}_{\mathrm{CC}}$ | Logic supply voltage. |
| 15 | PGND | Output power stage ground. |
| 16 | $\mathrm{V}_{\mathrm{C}}$ | Output power stage supply voltage. |



Figure 2. Block Diagram

## APPLICATION INFORMATION

## THEORY OF OPERATION

## Feed Forward Voltage Mode Control

In conventional voltage mode control, the ramp signal has fixed rising and falling slope. The feedback signal is derived solely from the output voltage. Consequently, voltage mode control has inferior line regulation and audio susceptibility.

Feed forward voltage mode control derives the ramp signal from the input line, as shown in Figure 3. Therefore, the ramp of the slope varies with the input voltage. At the start of each switch cycle, the capacitor connected to the FF pin is charged through a resistor connected to the input voltage. Meanwhile, the Gate output is turned on to drive an external power switching device. When the FF pin voltage reaches the error amplifier output $\mathrm{V}_{\text {COMP }}$, the PWM comparator turns off the Gate, which in turn opens the external switch. Simultaneously, the FF capacitor is quickly discharged to 0.3 V .

Overall, the dynamics of the duty cycle are controlled by both input and output voltages. As illustrated in Figure 4, with a fixed input voltage the output voltage is regulated solely by the error amplifier. For example, an elevated output voltage reduces $\mathrm{V}_{\text {COMP }}$ which in turn causes duty cycle to decrease. However, if the input voltage varies, the slope of the ramp signal will react immediately which provides a much improved line transient response. As an example shown in Figure 5, when the input voltage goes up, the rising edge of the ramp signal increases which reduces duty cycle to counteract the change.


Figure 3. Feed Forward Voltage Mode Control
The feed forward feature can also be employed to provide a volt-second clamp, which limits the maximum product of input voltage and turn on time. This clamp is used in circuits, such as Forward and Flyback converter, to prevent the transformer from saturating. Calculations used in the design
of the volt-second clamp are presented in the Design Guidelines section.


Figure 4. Pulse Width Modulated by Output Current with Constant Input Voltage


Figure 5. Pulse Width Modulated by Input Voltage with Constant Output Current

## Powering the IC \& UVL

The Under Voltage Lockout (UVL) comparator has two voltage references; the start and stop thresholds. During power-up, the UVL comparator disables $\mathrm{V}_{\text {REF }}$ (which in-turn disables the entire IC) until the controller reaches its $\mathrm{V}_{\mathrm{CC}}$ start threshold. During power-down, the UVL comparator allows the controller to operate until the $\mathrm{V}_{\mathrm{CC}}$ stop threshold is reached. The CS51221 requires only $50 \mu \mathrm{~A}$ during startup. The output stage is held at a low impedance state in lock out mode.
During power up and fault conditions, the soft-start clamps the Comp pin voltage and limits the duty cycle. The power up transition tends to generate temporary duty cycles
much greater than the steady state value due to the low output voltage. Consequently, excessive current stresses often take place in the system. Soft Start technique alleviates this problem by gradually releasing the clamp on the duty cycle to eliminate the in-rush current. The duration of the Soft Start can be programmed through a capacitance connected to the SS pin. The constant charging current to the SS pin is $50 \mu \mathrm{~A}$ (typ).

The $\mathrm{V}_{\text {REF }}$ (ok) comparator monitors the $3.3 \mathrm{~V} \mathrm{~V}_{\text {REF }}$ output and latches a fault condition if $\mathrm{V}_{\text {REF }}$ falls below 3.1 V . The fault condition may also be triggered when the OV pin voltage rises above 2.0 V or the UV pin voltage falls below 1.0 V . The under-voltage comparator has a built-in hysteresis of 75 mV (typ). The hysteresis for the OV comparator is programmable through a resistor connected to the OV pin. When an OV condition is detected, the over-voltage hysteresis current of $12.5 \mu \mathrm{~A}$ (typ) is sourced from the pin.

In Figure 6, the fault condition is triggered by pulling the UV pin to the ground. Immediately, the SS capacitor is discharged with $5.0 \mu \mathrm{~A}$ of current (typ) and the GATE output is disabled until the SS voltage reaches the discharge voltage of 0.3 V (typ). The IC starts the Soft Start transition again if the fault condition has recovered as shown in Figure 6. However, if the fault condition persists, the SS voltage will stay at 0.1 V until the removal of the fault condition.


Figure 6. The Fault Condition Is Triggered when the UV Pin Voltage Falls Below 1.0 V. The Soft Start Capacitor Is Discharged and the GATE Output Is Disabled. CH2: Envelop of GATE Output, CH3: SS Pin with $0.01 \mu$ F Capacitor, CH4: UV Pin

## Current Sense and Over Current Protection

The current can be monitored by the $\mathrm{I}_{\text {SENSE }}$ pin to achieve pulse by pulse current limit. Various techniques, such as a using current sense resistor or current transformer, can be adopted to derive current signals. The voltage of the ISET pin
sets the threshold for maximum current. As shown in Figure 7, when the I current limit comparator will reset the GATE latch flip-flop to terminate the GATE pulse.


Figure 7. The GATE Output Is Terminated When the I ISENSE Pin Voltage Reaches the Threshold Set By the $I_{\text {SET }}$ Pin. CH2: I ISENSE Pin, CH4: I CH3: GATE Pin

The current sense signal is prone to leading edge spikes caused by the switching transition. A RC low-pass filter is usually applied to the current signals to avoid premature triggering. However, the low pass filter will inevitably change the shape of the current pulse and also add cost. The CS51221 uses leading edge blanking circuitry that blocks out the first 150 ns (typ) of each current pulse. This removes the leading edge spikes without altering the current waveform. The blanking is disabled during Soft Start and when the $\mathrm{V}_{\text {COMP }}$ is saturated high so that the minimum on-time of the controller does not have the additional blanking period. The max SS detect comparator keeps the blanking function disabled until SS charges fully. The output of the max Duty Cycle detector goes high when the error amplifier output gets saturated high, indicating that the output voltage has fallen well below its regulation point and the power supply may be under load stress.

## Oscillator and Synchronization

The switching frequency is programmable through a RC network connected to the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ Pin. As shown in Figure 8, when the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ pin reaches 2.0 V , the capacitor is discharged by a 1.0 mA current source and the Gate signal is disabled. When the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ pin decreases to 1.0 V , the Gate output is turned on and the discharge current is removed to let the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ pin ramp up. This begins a new switching cycle. The $\mathrm{C}_{\mathrm{T}}$ charging time over the switch period sets the maximum duty cycle clamp which is programmable through the $\mathrm{R}_{\mathrm{T}}$ value as shown in the Design Guidelines. At the beginning
of each switching cycle, the SYNC pin generates a 2.5 V , 320 nS (typ) pulse. This pulse can be utilized to synchronize other power supplies.


Figure 8. The SYNC Pin Generates a Sync Pulse at the Beginning of Each Switching Cycle. CH2: GATE Pin, CH3: $\mathbf{R}_{\mathbf{T}} \mathrm{C}_{\mathrm{T}}, \mathrm{CH} 4$ : SYNC Pin

An external pulse signal can feed to the bidirectional SYNC pin to synchronize the switch frequency. For reliable operation, the sync frequency should be approximately $20 \%$ higher than free running IC frequency. As show in Figure 9, when the SYNC pin is triggered by an incoming signal, the IC immediately discharges $\mathrm{C}_{\mathrm{T}}$. The GATE signal is turned on once the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ pin reaches the valley voltage. Because of the steep falling edge, this valley voltage falls below the regular 1.0 V threshold. However, the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ pin voltage is then quickly raised by a clamp. When the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ pin reaches the 0.95 V (typ) Valley Clamp Voltage, the clamp is disconnected after a brief delay and $\mathrm{C}_{\mathrm{T}}$ is charged through $\mathrm{R}_{\mathrm{T}}$.


Figure 9. Operation with External Sync. CH2: SYNC Pin, CH3: GATE Pin, $\mathbf{C H} 4$ : $\mathbf{R}_{\mathbf{T}} \mathbf{C}_{\mathbf{T}}$ Pin

## DESIGN GUIDELINES

## Switch Frequency and Maximum Duty Cycle Calculations

Oscillator timing capacitor, $\mathrm{C}_{\mathrm{T}}$, is charged by $\mathrm{V}_{\mathrm{REF}}$ through $\mathrm{R}_{\mathrm{T}}$ and discharged by an internal current source. During the discharge time, the internal clock signal sets the Gate output to the low state, thus providing a user selectable maximum duty cycle clamp. Charge and discharge times are determined by following general formulas;

$$
\begin{gathered}
t_{C}=R_{T} C_{T} \ln \left(\frac{\left(V_{R E F}-V_{V A L L E Y}\right)}{\left(V_{R E F}-V_{P E A K}\right)}\right) \\
t_{d}=R_{T} C T \ln \left(\frac{\left(V_{R E F}-V_{\text {PEAK }}-I_{d} R T\right)}{\left(V_{R E F}-V_{V A L L E Y}-I_{d} R_{T}\right)}\right)
\end{gathered}
$$

where:
$\mathrm{t}_{\mathrm{C}}=$ charging time;
$\mathrm{t}_{\mathrm{d}}=$ discharging time;
$\mathrm{V}_{\text {VALLEY }}=$ valley voltage of the oscillator;
$\mathrm{V}_{\text {PEAK }}=$ peak voltage of the oscillator.
Substituting in typical values for the parameters in the above formulas, $\mathrm{V}_{\text {REF }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {VALLEY }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {PEAK }}=$ $2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{d}}=1.0 \mathrm{~mA}$ :

$$
\begin{gathered}
\mathrm{t}_{\mathrm{C}}=0.57 \mathrm{R}_{\mathrm{T}} \mathrm{C} T \\
\mathrm{t}_{\mathrm{d}}=\mathrm{R}_{\mathrm{T}} \mathrm{C} T \ln \left(\frac{1.3-0.001 \mathrm{R}_{\mathrm{T}}}{2.3-0.001 \mathrm{RT}}\right) \\
\mathrm{D}_{\text {max }}=\frac{0.57}{0.57+\ln \left(\frac{1.3-0.001 \mathrm{RT} T}{2.3-0.001 \mathrm{R}_{\mathrm{T}}}\right)}
\end{gathered}
$$

It is noticed from the equation that for the oscillator to function properly, $\mathrm{R}_{\mathrm{T}}$ has to be greater than 2.3 k .


Figure 10. Typical Performance Characteristics, Oscillator Frequency vs. $\mathrm{C}_{\mathbf{T}}$

## Select RC for Feed Forward Ramp

If the line voltage is much greater than the FF pin Peak Voltage, the charge current can be treated as a constant and is equal to $\mathrm{V}_{\mathrm{IN}} / \mathrm{R}$. Therefore, the volt-second value is determined by:

$$
\mathrm{V}_{\mathrm{IN}} \times \mathrm{T}_{\mathrm{ON}}=\left(\mathrm{V}_{\mathrm{COMP}}-\mathrm{V}_{\mathrm{FF}(\mathrm{~d})}\right) \times \mathrm{R} \times \mathrm{C}
$$

where:
$\mathrm{V}_{\text {COMP }}=$ COMP pin voltage;
$\mathrm{V}_{\mathrm{FF}(\mathrm{d})}=\mathrm{FF}$ pin discharge voltage.
As shown in the equation, the volt-second clamp is set by the $\mathrm{V}_{\mathrm{COMP}}$ clamp voltage which is equal to 1.8 V . In Forward or Flyback circuits, the volt-second clamp value is designed to prevent transformers from saturation.

In a buck or forward converter, volt-second is equal to

$$
\mathrm{V}_{\mathrm{IN}} \times \mathrm{T}_{\mathrm{ON}}=\left(\frac{\mathrm{V}_{\mathrm{OUT}} \times \mathrm{TS}_{\mathrm{S}}}{\mathrm{n}}\right)
$$

$\mathrm{n}=$ transformer turns ratio, which is a constant determined by the regulated output voltage, switching period and transformer turns ration (use 1.0 for buck converter). It is interesting to notice from the aforementioned two equations that during steady state, $\mathrm{V}_{\text {COMP }}$ doesn't change for input voltage variations. This intuitively explains why FF voltage mode control has superior line regulation and line transient response. Knowing the nominal value of $\mathrm{V}_{\mathrm{IN}}$ and $\mathrm{T}_{\mathrm{ON}}$, one can also select the value of RC to place $\mathrm{V}_{\mathrm{COMP}}$ at the center of its dynamic range.

## Select Feedback Voltage Divider

As shown in Figure 12, the voltage divider output feeds to the FB pin, which connects to the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to a 1.27 V (typ) reference voltage. The FB pin has an input current which has to be considered for accurate DC outputs. The following equation can be used to calculate the R1 and R2 value

$$
\left(\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}\right) \mathrm{V}_{\mathrm{OUT}}=1.27-\nabla
$$



Figure 11. Typical Performance Characteristics, Oscillator Duty Cycle vs. $\mathbf{R}_{\mathbf{T}}$
where $\nabla$ is the correction factor due to the existence of the FB pin input current Ier.

$$
\nabla=(\mathrm{Ri}+\mathrm{R} 1 / / \mathrm{R} 2) \mathrm{ler}
$$

$\mathrm{Ri}=\mathrm{DC}$ resistance between the FB pin and the voltage divider output.

Ier $=\mathrm{V}_{\mathrm{FB}}$ input current, $1.3 \mu \mathrm{~A}$ typical.


Figure 12. The Design of Feedback Voltage Divider Has to Consider the Error Amplifier Input Current

## Design Voltage Dividers for OV and UV Detection

In Figure 13, the voltage divider uses three resistors in series to set OV and UV threshold seen from the input voltage. The values of the resistors can be calculated from the following three equations, where the third equation is derived from OV hysteresis requirement.

$$
\begin{gather*}
\mathrm{V}_{\mathrm{IN}(\mathrm{LOW})} \times\left(\frac{\mathrm{R} 2+\mathrm{R} 3}{\mathrm{R} 2+\mathrm{R} 3+\mathrm{R} 1}\right)=1.0 \mathrm{~V}  \tag{A}\\
\mathrm{~V}_{\mathrm{IN}(\mathrm{HIGH})} \times\left(\frac{\mathrm{R} 3}{\mathrm{R} 2+\mathrm{R} 3+\mathrm{R} 1}\right)=2.0 \mathrm{~V}  \tag{B}\\
12.5 \mu \mathrm{~A} \times(\mathrm{R} 1+\mathrm{R} 2)=\mathrm{V}_{\mathrm{HYST}} \tag{C}
\end{gather*}
$$

where:

## CS51221

$\mathrm{V}_{\mathrm{IN}(\mathrm{LOW})}, \mathrm{V}_{\mathrm{IN}(\mathrm{HIGH})}=$ input voltage OV and UV threshold;
$\mathrm{V}_{\text {HYST }}=\mathrm{OV}$ hysteresis seen at $\mathrm{V}_{\text {IN }}$
It is self-evident from equation $A$ and $B$ that to use this design, $\mathrm{V}_{\text {IN(HIGH) }}$ has to be two times greater than $\mathrm{V}_{\text {IN(LOW). }}$. Otherwise, two voltage dividers have to be used to program OV and UV separately.


Figure 13. OV/UV Monitor Divider

PACKAGE THERMAL DATA

| Parameter |  | SO-16 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS51227

## Enhanced Voltage Mode PWM Controller

The CS51227 is a fixed frequency, single output PWM controller using feed forward voltage mode control. Feed forward control provides superior line regulation and line transient response. This PWM controller has been optimized for high frequency primary side control operation. It has undervoltage lockout with 4.7 V start up voltage and $75 \mu \mathrm{~A}$ start up current. One external capacitor can program the switching frequency up to 1.0 MHz . The protection features include pulse-by-pulse current limit with leading edge blanking and thermal shutdown. The CS51227 is available in 8 lead SO narrow surface mount package.

## Features

- 1.0 MHz Frequency Capability
- 4.7 V Start-Up Voltage
- Fixed Frequency Voltage Mode Operation with Feed Forward
- Undervoltage Lockout
- $75 \mu \mathrm{~A}$ Start-Up Current
- Thermal Shutdown
- 1.0 A Sink/Source Gate Drive
- Pulse-By-Pulse Current Limit with Leading Edge Blanking
- 50 ns GATE Rise and Fall Time (1.0 nF Load)
- Maximum Duty Cycle Over 85\%
- Programmable Volt-Second Clamp


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS51227ED8 | SO-8 | 95 Units/Rail |
| CS51227EDR8 | SO-8 | 2500 Tape \& Reel |



Figure 1. Applications Diagram, 5.0 V to 12 V/2.0 A Boost Converter

## MAXIMUM RATINGS*

| Rating | Value | Unit |  |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering: |  | 2.0 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gate Drive Output | GATE | 20 V | -0.3 V | 1.0 A Peak, 200 mA DC | 1.0 A Peak, 200 mA DC |
| Current Sense Input | $I_{\text {SENSE }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Timing Capacitor | CT | 6.0 V | -0.3 V | 1.0 mA | 10 mA |
| Feed Forward | FF | 6.0 V | -0.3 V | 1.0 mA | 25 mA |
| Error Amp Output | COMP | 6.0 V | -0.3 V | 10 mA | 20 mA |
| Feedback Voltage | $\mathrm{V}_{\text {FB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Power Supply | $\mathrm{V}_{\text {CC }}$ | 20 V | -0.3 V | 10 mA | 1.0 A Peak, 200 mA DC |
| Ground | GND | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ | 1.0 A Peak, 200 mA DC | $\mathrm{N} / \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS: $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<18 \mathrm{~V}\right.$
$\mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Start/Stop Voltages |  |  |  |  |  |
| Start Threshold | - | 4.4 | 4.5 | 4.7 | V |
| Stop Threshold | - | 3.2 | 3.8 | 4.2 | V |
| Hysteresis | Start - Stop | 300 | 700 | 1400 | mV |
| ICC @ Startup | $V_{\text {CC }}$ < UVL Start Threshold | - | 38 | 75 | $\mu \mathrm{~A}$ |

Supply Current

| $I_{\text {CC }}$ Operating | No Load | - | 10 | 16 | mA |
| :--- | :--- | :--- | :--- | :--- | :--- |

## Overcurrent Protection

| Overcurrent Threshold | Ramp ISENSE | 0.27 | 0.30 | 0.33 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $I_{\text {SENSE }}$ to GATE Delay | $\mathrm{V}_{\mathrm{FB}}=0.5 \mathrm{~V}$ (no blanking) | - | 60 | 125 | ns |

## Error Amp

| Reference Voltage | $\mathrm{V}_{\mathrm{FB}}$ connected to COMP | 1.234 | 1.263 | 1.285 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FB}}$ Input Current | $\mathrm{V}_{\mathrm{FB}}=1.25 \mathrm{~V}$ | - | 1.3 | 2.0 | $\mu \mathrm{~A}$ |
| Open Loop Gain | Note 2 | 60 | 90 | - | dB |
| Unity Gain Bandwidth | Note 2 | 1.5 | 2.5 | - | MHz |
| COMP Sink Current | $\mathrm{COMP}=1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.45 \mathrm{~V}$ | 3.0 | 12 | 32 | mA |
| COMP Source Current | $\mathrm{COMP}=1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.15 \mathrm{~V}$ | 1.0 | 1.7 | 2.4 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=1.15 \mathrm{~V}$ | 2.8 | 3.1 | 3.4 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=1.45 \mathrm{~V}$ | 75 | 150 | 300 | mV |
| PSRR | $\mathrm{Freq}=120 \mathrm{~Hz}$, Note 2 | 60 | 85 | - | dB |

## Oscillator

| Frequency Accuracy | - | 200 | 235 | 270 | kHz |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Max Duty Cycle |  | - | 85 | 90 | 95 | $\%$ |
| Peak Voltage | Note 2 |  | 1.99 | 2.05 | 2.11 | V |
| Valley Clamp Voltage | Note 2 |  | 0.90 | 0.95 | 1.00 | V |
| Valley Voltage |  | - | 0.90 | 0.95 | 1.00 | V |
| Discharge Current |  |  | 0.85 | 1.00 | 1.15 | mA |
| Charge Current |  | 95 | 115 | 135 | $\mu \mathrm{~A}$ |  |

## Gate Driver

| High Saturation Voltage | $\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{GATE}}, \mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}, \mathrm{I}_{\text {SOURCE }}=150 \mathrm{~mA}$ | - | 1.5 | 2.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Low Saturation Voltage | $\mathrm{V}_{\mathrm{GATE}}, \mathrm{I}_{\text {SINK }}=150 \mathrm{~mA}$ | - | 1.2 | 1.5 | V |
| High Voltage Clamp | - | 11 | 13.5 | 16 | V |
| Output UVL Leakage | $\mathrm{V}_{\mathrm{GATE}}=0 \mathrm{~V}$ | - | 1.0 | 50 | $\mu \mathrm{~A}$ |
| Rise Time | 1.0 nF Load, $\mathrm{V}_{\mathrm{CC}}=18 \mathrm{~V}, 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{O}}<9.0 \mathrm{~V}$ | - | 32 | 50 | ns |
| Fall Time | 1.0 nF Load, $\mathrm{V}_{\mathrm{CC}}=18 \mathrm{~V}, 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{O}}<1.0 \mathrm{~V}$ | - | 25 | 50 | ns |
| Max GATE Voltage @ UVL | $\mathrm{I}_{\text {LOAD }}=100 \mu \mathrm{~A}$ | 0.4 | 0.7 | 1.5 | V |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS: (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}, 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<18 \mathrm{~V}\right.$ $\mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Feed Forward (FF) |  |  |  |  |  |
| Discharge Voltage | $\mathrm{I}_{\mathrm{FF}}=2.0 \mathrm{~mA}$ | - | 0.3 | 0.7 | V |
| Discharge Current | $\mathrm{FF}=1.0 \mathrm{~V}$ | 2.0 | 16 | 30 | mA |
| FF to GATE Delay | - | 50 | 75 | 125 | ns |
| FF Max VOItage | $\mathrm{V}_{\mathrm{FB}}=1.15 \mathrm{~V}$ | 1.7 | 1.8 | 1.9 | V |

Blanking

| Blanking Time |  | - | 50 | 150 | 250 |
| :--- | :--- | :---: | :---: | :---: | :---: |
| ns |  |  |  |  |  |
| COMP Blanking Disable Threshold | $\mathrm{V}_{\mathrm{FB}}<1.0 \mathrm{~V}$ | 2.8 | 3.0 | 3.3 | V |

Thermal Shutdown

| Thermal Shutdown | Note 3 | 125 | 150 | 180 | ${ }^{\circ} \mathrm{C}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Thermal Hysteresis | Note 3 | 5.0 | 10 | 15 | ${ }^{\circ} \mathrm{C}$ |

3. Guaranteed by design, not $100 \%$ tested in production.

## PACKAGE PIN DESCRIPTION

| PACKAGE LEAD \# |  |  |
| :---: | :---: | :--- |
| SO-8 | LEAD SYMBOL |  |
| 1 | GATE | External power switch driver with 1.0 A peak capability. Rail-to-rail output <br> occurs when the capacitive load is between 470 pF and 10 nF. |
| 2 | I SENSE | Current sense comparator input. |
| 3 | FF | PWM ramp. |
| 4 | CT | Timing capacitor $\mathrm{C}_{\mathrm{T}}$ determines oscillator frequency. |
| 5 | $\mathrm{~V}_{\mathrm{FB}}$ | Feedback voltage input. Connected to the error amplifier inverting input. |
| 6 | COMP | Error amplifier output. |
| 7 | GND | Ground. |
| 8 | $\mathrm{~V}_{\mathrm{CC}}$ | Supply voltage. |



Figure 2. Block Diagram

## THEORY OF APPLICATION

## THEORY OF OPERATION

## Feed Forward Voltage Mode Control

In conventional voltage mode control, the ramp signal is fixed and often generated by the oscillator. The output voltage is the only feedback path for regulation against load and line variations. Feed forward voltage mode uses the ramp signal driven by the input line, as shown in Figure 3. Therefore, the ramp signal responds immediately to line change. At the start of each switch cycle, the FF pin capacitor is charged up through a resistor connected to the input line. Meanwhile, the Gate output is turned on to drive an external power switching device. When the FF pin voltage reaches the error amplifier output $\mathrm{V}_{\mathrm{COMP}}$, the PWM comparator turns off the Gate and the FF pin capacitor is quickly discharged by an internal current source.


Figure 3. Feed Forward Voltage Mode Control


Figure 4. Pulse Width Modulated By Output Current With Constant Input Voltage

Overall, the dynamics of the duty cycle are controlled by both input and output voltages. As shown in Figure 4, an elevated output voltage reduces $\mathrm{V}_{\text {COMP }}$ through the error amplifier. This in turn decreases the duty cycle and corrects the deviation of the output voltage. For line variation, the ramp signal responds immediately, which provides much improved line transient response. The delay associated with the power stage and feedback path has been totally avoided. As an example, shown in Figure 5, when the input line goes up, the slope of the ramp signal increases, reducing duty cycle to counteract the change.


Figure 5. Pulse Width Modulated By Input Voltage With Constant Output Voltage

The feed forward feature can also be employed to implement volt-second clamping, which limits the maximum product of input voltage and turn on time. This clamp is used in circuits, such as Forward and Flyback converters, to prevent the transformer from saturating. The calculation for volt-second clamping is presented in the Design Guidelines section.

## Powering the IC \& UVL

The internal logic monitors the supply voltage to ensure the controller has enough operating headroom. The $\mathrm{V}_{\text {REF }}$ block provides power to the controller's logic. The $\mathrm{V}_{\text {REF(OK) }}$ comparator monitors the internal $3.3 \mathrm{~V} \mathrm{~V}_{\text {REF }}$ line and flags a fault if $\mathrm{V}_{\text {REF }}$ falls below 3.1 V .
The Undervoltage Lockout (UVL) comparator has two voltage references; the start and stop thresholds. During power-up, the UVL comparator disables $\mathrm{V}_{\text {REF }}$ (which in-turn disables the entire IC) until the controller reaches its $\mathrm{V}_{\mathrm{CC}}$ start threshold. During power-down, the UVL comparator allows the controller to operate until the $\mathrm{V}_{\mathrm{CC}}$ stop threshold is reached. The CS51227 requires only $50 \mu \mathrm{~A}$ during startup. During low $\mathrm{V}_{\mathrm{CC}}$ and abnormal operation conditions, the output stage is held at a low level, low impedance state.

## Current Sense and Over Current Protection

The I pulse current limit. When the ISENSE pin voltage exceeds the internal threshold ( 0.3 V typical), the current limit comparator immediately turns off the Gate signal. The Gate will then stay off for the remainder of the cycle. Various techniques, such as using current sensing resistor or current transformer, are widely adopted to generate the current signal.
The current sense signal is prone to leading edge spikes caused by switching transitions. A RC low-pass filter can effectively reduce the spikes and avoid premature triggering. However, the low pass filter will inevitably change the shape of the current pulse and also add cost. The CS51227 has built-in leading edge blanking circuitry that blocks out the first 150 ns (typ) of each current pulse. This feature removes the leading edge spikes without altering the current waveform. Blanking is disabled when the COMP pin voltage exceeds 3.0 V (typ). This feature reduces the minimum duty cycle during an output short or overload condition.

## DESIGN GUIDELINES

## Programming Oscillator Frequency

The switching frequency is set by the capacitor connected to the $\mathrm{C}_{\mathrm{T}}$ pin. The $\mathrm{C}_{\mathrm{T}}$ pin voltage oscillates between 1.0 V and 2.0 V . The ratio of the charge and discharge currents sets the maximum duty cycle to be $90 \%$. Use the following equation to select $\mathrm{C}_{\mathrm{T}}$,

$$
\mathrm{C}_{\top}=\frac{9.027 \times 107}{\mathrm{f}_{\mathrm{S}}}
$$

where:
$\mathrm{fs}=$ Switching frequency
$\mathrm{C}_{\mathrm{T}}=$ Capacitance in pF

When $\mathrm{C}_{\mathrm{T}}$ is less than 100 pF , parasitic capacitance associated with the $\mathrm{C}_{\mathrm{T}}$ pin starts to impact frequency accuracy. Figure 6 shows typical oscillator frequency vs. $\mathrm{C}_{\mathrm{T}}$ value.


Figure 6. Typical Performance Characteristics: Oscillator Frequency vs. $\mathrm{C}_{\boldsymbol{T}}$

## Component Selection for Feed Forward Ramp

FF discharge voltage and FF maximum voltage limit the maximum voltage rise on the FF pin to 1.5 V typical. This provides the volt-second clamp feature when the FF pin is driven by the input line. If the line voltage is much greater than the FF pin voltage, the charge current is approximately equal to $\mathrm{V}_{\mathrm{IN}} / \mathrm{R}$ where R is the resistor connecting the FF pin and input line. The voltage second clamp then has the form of:

$$
\mathrm{V}_{\mathrm{IN}} \times \mathrm{T}_{\mathrm{ON}}=1.5 \times \mathrm{R} \times \mathrm{C}_{\mathrm{FF}}
$$

One can select $\mathrm{RC}_{\mathrm{FF}}$ to prevent magnetic devices from saturating.

In a buck or forward converter, the error amplifier output $\mathrm{V}_{\text {COMP }}$ is equal to:

$$
\mathrm{V}_{\mathrm{COMP}}=\frac{\mathrm{V}_{\mathrm{OUT}} \times \mathrm{TS}}{\mathrm{~N} \times \mathrm{R} \times \mathrm{C}_{\mathrm{FF}}}+0.3 \mathrm{~V}
$$

where:
$\mathrm{N}=$ Transformer turns ratio (use 1 for buck converter)
$\mathrm{T}_{\mathrm{S}}=$ Switching period
This equation shows that the error amplifier output is independent of the input voltage. Therefore, the system does not rely on the error amplifier to respond to line variations. This excludes the delay associated with the error amplifier. The line regulation is also greatly improved because both
error amplifier and ramp signal can contribute to DC regulation.

## Select Feedback Voltage Divider

As shown in Figure 7, the voltage divider output feeds the FB pin which connects to the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to a 1.263 V reference voltage. The FB pin has an input current which has to be taken into account for accurate output voltage programming. The following equation can be used to calculate the R1 and R2 value:

$$
\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2} \times \mathrm{V}_{\mathrm{OUT}}=1.263-\nabla
$$

where $\nabla$ is the correction factor

$$
\nabla=(R i+R 1 / / R 2) \times \operatorname{ler}
$$

$\mathrm{Ri}=\mathrm{DC}$ resistance between the FB pin and the voltage divider output, as shown in Figure 7.
Ier $=\mathrm{FB}$ pin input current, $1.3 \mu \mathrm{~A}$ typical.


Figure 7. The Feedback Voltage Divider Design Has to Consider the Error Amplifier Input Current

## Thermal Management

The CS51227 will enter thermal shutdown when the junction (die surface) temperature exceeds $150^{\circ} \mathrm{C}$, typical. $10^{\circ} \mathrm{C}$ typical thermal hysteresis will prevent part cycling, or a "chattering" startup near the shutdown temperature. Junction temperature is a function of the ambient temperature, thermal resistance of the die and package, and the power dissipated by the package and leads.

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 45 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 165 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC34025, MC33025

## High Speed Double-Ended PWM Controller

The MC34025 series are high speed, fixed frequency, double-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Outputs
- Dual High Current Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully-Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle-By-Cycle Current Limiting
- Soft-Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up Current (500 $\mu \mathrm{A}$ Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- $90 \%$ Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3825


Figure 1. Simplified Application


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


## PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33025DW | SO-16L | 47 Units/Rail |
| MC33025DWR2 | SO-16L | 1000 Tape \& Reel |
| MC33025P | PDIP-16 | 25 Units/Rail |
| MC34025DW | SO-16L | 47 Units/Rail |
| MC34025DWR2 | SO-16L | 1000 Tape \& Reel |
| MC34025P | PDIP-16 | 25 Units/Rail |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 30 | V |
| Output Driver Supply Voltage | $\mathrm{V}_{\mathrm{C}}$ | 25 | V |
| Output Current, Source or Sink (Note 1) DC Pulsed ( $0.5 \mu \mathrm{~s}$ ) | 10 | $\begin{aligned} & 0.5 \\ & 2.0 \end{aligned}$ | A |
| Current Sense, Soft-Start, Ramp, and Error Amp Inputs | $\mathrm{V}_{\text {in }}$ | -0.3 to +7.0 | V |
| Error Amp Output and Soft-Start Sink Current | 10 | 10 | mA |
| Clock and $\mathrm{R}_{\mathrm{T}}$ Output Current | $\mathrm{I}_{\mathrm{CO}}$ | 5.0 | mA |
| Power Dissipation and Thermal Characteristics SO-16 Package (Case 751G) Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air DIP Package (Case 648) Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ $\mathrm{R}_{\text {日JA }}$ $\mathrm{P}_{\mathrm{D}}$ $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 862 \\ & 145 \\ & \\ & 1.25 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 2) MC34025 MC33025 | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+105 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=3.65 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| Reference Output Voltage ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {ref }}$ | 5.05 | 5.1 | 5.15 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 30 V ) | Regline | - | 2.0 | 15 | mV |
| Load Regulation ( $\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 2.0 | 15 | mV |
| Temperature Stability | Ts | - | 0.2 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {ref }}$ | 4.95 | - | 5.25 | V |
| Output Noise Voltage ( $\mathrm{f}=10 \mathrm{~Hz}$ to $10 \mathrm{kHz}, \mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 50 | - | $\mu \mathrm{V}$ |
| Long Term Stability ( $\mathrm{T}_{\mathrm{A}}=+125^{\circ} \mathrm{C}$ for 1000 Hours) | S | - | 5.0 | - | mV |
| Output Short Circuit Current | Isc | -30 | -65 | -100 | mA |

OSCILLATOR SECTION

| Frequency <br> $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ <br> Line $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 30 V$)$ and Temperature $\left(\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\left.\mathrm{T}_{\text {high }}\right)$ | $\mathrm{f}_{\mathrm{osc}}$ | 380 | 400 | 420 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 30 V$)$ | $\Delta 70$ | 400 | 430 |  |  |
| Frequency Change with Temperature $\left(\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\left.\mathrm{T}_{\text {high }}\right)$ | $\Delta \mathrm{f}_{\text {osc }} / \Delta \mathrm{V}$ | - | 0.2 | 1.0 | $\%$ |
| Sawtooth Peak Voltage | $\Delta \mathrm{f}_{\text {osc }} / \Delta \mathrm{T}$ | - | 2.0 | - | $\%$ |
| Sawtooth Valley Voltage | $\mathrm{V}_{\mathrm{P}}$ | 2.6 | 2.8 | 3.0 | V |
| Clock Output Voltage <br> High State <br> Low State | $\mathrm{V}_{\mathrm{V}}$ | 0.7 | 1.0 | 1.25 | V |

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34025
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34025
$=-40^{\circ} \mathrm{C}$ for MC33025
$=+105^{\circ} \mathrm{C}$ for MC33025

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=3.65 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER SECTION |  |  |  |  |  |
| Input Offset Voltage | $\mathrm{V}_{10}$ | - | - | 15 | mV |
| Input Bias Current | IB | - | 0.6 | 3.0 | $\mu \mathrm{A}$ |
| Input Offset Current | $\mathrm{I}_{10}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Open-Loop Voltage Gain ( $\mathrm{V}_{\mathrm{O}}=1.0 \mathrm{~V}$ to 4.0 V ) | Avol | 60 | 95 | - | dB |
| Gain Bandwidth Product ( $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | GBW | 4.0 | 8.3 | - | MHz |
| Common Mode Rejection Ratio ( $\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}$ to 5.5 V ) | CMRR | 75 | 95 | - | dB |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 30 V ) | PSRR | 85 | 110 | - | dB |
| Output Current, Source ( $\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{~V}$ ) Sink ( $\mathrm{V}_{\mathrm{O}}=1.0 \mathrm{~V}$ ) | ISource $I_{\text {Sink }}$ | $\begin{aligned} & 0.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.6 \end{aligned}$ | - | mA |
| Output Voltage Swing, High State ( $\mathrm{I}_{\mathrm{O}}=-0.5 \mathrm{~mA}$ ) <br> Low State $\left(\mathrm{l}_{\mathrm{O}}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ VoL | $\begin{gathered} 4.5 \\ 0 \end{gathered}$ | $\begin{gathered} 4.75 \\ 0.4 \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 1.0 \end{aligned}$ | V |
| Slew Rate | SR | 6.0 | 12 | - | $\mathrm{V} / \mu \mathrm{s}$ |

## PWM COMPARATOR SECTION

| Ramp Input Bias Current | $I_{\text {IB }}$ | - | -0.5 | -5.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Duty Cycle, Maximum Minimum | $\begin{aligned} & \mathrm{DC}_{(\text {max })} \\ & \mathrm{DC}_{(\text {min })} \end{aligned}$ | $80$ | $90$ | $\overline{0}$ | \% |
| Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V) | $\mathrm{V}_{\text {th }}$ | 1.1 | 1.25 | 1.4 | V |
| Propagation Delay (Ramp Input to Output, $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{tpLH}_{\text {(in/out) }}$ | - | 60 | 100 | ns |

## SIFT-START SECTION

| Charge Current $\left(\mathrm{V}_{\text {Soft-Start }}=0.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {chg }}$ | 3.0 | 9.0 | 20 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Discharge Current $\left(\mathrm{V}_{\text {Soft-Start }}=1.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {dischg }}$ | 1.0 | 4.0 | - | mA |

## CURRENT SENSE SECTION

| Input Bias Current (Pin 9(12) $=0 \mathrm{~V}$ to 4.0 V ) | $\mathrm{I}_{\mathrm{IB}}$ | - | - | 15 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Current Limit Comparator Threshold | $\mathrm{V}_{\text {th }}$ | 0.9 | 1.0 | 1.10 | V |
| Shutdown Comparator Threshold | $\mathrm{V}_{\text {th }}$ | 1.25 | 1.40 | 1.55 |  |
| Propagation Delay (Current Limit/Shutdown to Output, $\mathrm{T}_{\left.J=+25^{\circ} \mathrm{C}\right)}$ | $\mathrm{tPLH}^{\text {(in/out) }}$ | - | 50 | 80 | ns |

## OUTPUT SECTION

| $\begin{array}{cl} \text { Output Voltage } \\ \text { Low State } & \left(I_{\text {Sink }}=20 \mathrm{~mA}\right) \\ & \left(I_{\text {Sink }}=200 \mathrm{~mA}\right) \\ \text { High State } & \left(l_{\text {Source }}=20 \mathrm{~mA}\right) \\ & \left(l_{\text {Source }}=200 \mathrm{~mA}\right) \end{array}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{OL}} \\ & \mathrm{~V}_{\mathrm{OH}} \end{aligned}$ | $\begin{aligned} & - \\ & 13 \\ & 12 \end{aligned}$ | $\begin{gathered} 0.25 \\ 1.2 \\ 13.5 \\ 13 \end{gathered}$ | $\begin{gathered} 0.4 \\ 2.2 \\ - \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage with UVLO Activated ( $\left.\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{I}_{\text {Sink }}=0.5 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {OL(UVLO) }}$ | - | 0.25 | 1.0 | V |
| Output Leakage Current ( $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}$ ) | IL | - | 100 | 500 | $\mu \mathrm{A}$ |
| Output Voltage Rise Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $t_{r}$ | - | 30 | 60 | ns |
| Output Voltage Fall Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$ ) | $\mathrm{t}_{\mathrm{f}}$ | - | 30 | 60 | ns |

## UNDERVOLTAGE LOCKOUT SECTION

| Start-Up Threshold (VCC Increasing) | $\mathrm{V}_{\text {th(on) }}$ | 8.8 | 9.2 | 9.6 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UVLO Hysteresis Voltage (VCC Decreasing After Turn-On) | $\mathrm{V}_{\mathrm{H}}$ | 0.4 | 0.8 | 1.2 | V |
| TOTAL DEVICE |  |  |  |  |  |
| Power Supply Current <br> Start-Up (VCC $=8.0 \mathrm{~V})$ <br> Operating | $I_{\text {cc }}$ | - | $\begin{aligned} & 0.5 \\ & 25 \end{aligned}$ | $\begin{aligned} & 1.2 \\ & 35 \end{aligned}$ | mA |

3. Maximum package power dissipation limits must be observed.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34025 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34025
$=-40^{\circ} \mathrm{C}$ for MC33025
$=+105^{\circ} \mathrm{C}$ for MC33025


Figure 2. Timing Resistor versus Oscillator Frequency


Figure 3. Oscillator Frequency versus Temperature


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

$0.1 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 6. Error Amp Small Signal Transient Response


Figure 5. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

$0.1 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 7. Error Amp Large Signal Transient Response


Figure 8. Reference Voltage Change versus Source Current

$\mathrm{V}_{\text {ref }}$ LINE REGULATION $10 \mathrm{~V}-24 \mathrm{~V}$ $2.0 \mathrm{~ms} / \mathrm{DIV}$

Figure 10. Reference Line Regulation


Figure 12. Current Limit Comparator Threshold Change versus Temperature


Figure 9. Reference Short Circuit Current versus Temperature


Figure 11. Reference Load Regulation


Figure 13. Shutdown Comparator Threshold Voltage versus Temperature


Figure 14. Soft-Start Charge Current versus Temperature


OUTPUT RISE \& FALL TIME 1.0 nF LOAD
$50 \mathrm{~ns} / \mathrm{DIV}$
Figure 16. Drive Output Rise and Fall Time


Figure 15. Output Saturation Voltage versus Load Current


OUTPUT RISE \& FALL TIME 10.0 nF LOAD
$50 \mathrm{~ns} / \mathrm{DIV}$
Figure 17. Drive Output Rise and Fall Time


Figure 18. Supply Voltage versus Supply Current


Figure 19. Representative Block Diagram


Figure 20. Current Limit Operating Waveforms

The MC33025 and MC34025 series are high speed, fixed frequency, double-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 19.

## Oscillator

The oscillator frequency is programmed by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. The $\mathrm{R}_{\mathrm{T}}$ pin is set to a temperature compensated 3.0 V . By selecting the value of $\mathrm{R}_{\mathrm{T}}$, the charge current is set through a current mirror for the timing capacitor $\mathrm{C}_{\mathrm{T}}$. This charge current runs continuously through $\mathrm{C}_{\mathrm{T}}$. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of $90 \%$. $\mathrm{C}_{\mathrm{T}}$ is charged to 2.8 V and discharged to 1.0 V . During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that resets the PWM Latch, inhibits the outputs, and toggles the steering flip-flop. The threshold voltages on the oscillator comparator is trimmed to guarantee an oscillator accuracy of $5.0 \%$ at $25^{\circ} \mathrm{C}$.

Additional dead time can be added by externally increasing the charge current to $\mathrm{C}_{\mathrm{T}}$ as shown in Figure 24. This changes the charge to discharge ratio of $\mathrm{C}_{\mathrm{T}}$ which is set internally to $\mathrm{I}_{\text {charge }} / 10 \mathrm{I}_{\text {charge }}$. The new charge to discharge ratio will be:

$$
\% \text { Deadtime }=\frac{I_{\text {additional }}+I_{\text {charge }}}{10\left(I_{\text {charge }}\right)}
$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of $\mathrm{C}_{\mathrm{T}}$. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge $\mathrm{C}_{\mathrm{T}}$. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 30 and 31 provide suggested synchronization.

## Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a gain bandwidth product of 8.3 MHz with 75 degrees of phase margin (Figure 4). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a Common Mode Voltage ( $\mathrm{V}_{\mathrm{CM}}$ ) input range of 1.5 V to 5.5 V . The Error Amplifier Output is provided for external loop compensation.

## Soft-Start Latch

Soft-Start is accomplished in conjunction with an external capacitor. The soft start capacitor is charged by an internal $9.0 \mu \mathrm{~A}$ current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle.
The time it takes for a capacitor to reach full charge is given by:

$$
t \approx\left(4.5 \cdot 10^{5}\right) C_{\text {Soft-Start }}
$$

A Soft-Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft-Start circuit to latch so that the Soft-Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\text {ref }}$. The second condition is when current sense input exceeds 1.4 V . Since this latch is "set dominant", it cannot be reset until either of these signals is removed, and the voltage at $\mathrm{C}_{\text {Soft-Start }}$ is less than 0.5 V .

## PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the Error Amplifier Output voltage minus 1.25 V , the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.
A toggle flip flop connected to the output of the PWM latch controls which output is active. The flip flop is pulsed by an OR gate that gets its inputs from the oscillator clock and the output of the PWM latch. A pulse from either one will cause the flip flop to enable the other output.

## Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. When the voltage at this pin exceeds 1.0 V , one of the comparators is activated. The output of this comparator sets the PWM latch, which disables the output. In this way cycle-by-cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$
\mathrm{R}_{\text {Sense }}=\frac{1.0 \mathrm{~V}}{\mathrm{I}_{\mathrm{pk}}(\text { switch })}
$$

If the voltage at this pin exceeds 1.4 V , the second comparator is activated. This comparator sets a latch which, in turn, causes the Soft-Start capacitor to be discharged. In this way a "hiccup" mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a "hiccup" mode is given by:

$$
I_{\text {shutdown }}=\frac{1.4 \mathrm{~V}}{\mathrm{R}_{\text {Sense }}}
$$

## Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses $\mathrm{V}_{\mathrm{CC}}$ and the second $\mathrm{V}_{\text {ref }}$. During power-up, $\mathrm{V}_{\mathrm{CC}}$ must exceed 9.2 V and $\mathrm{V}_{\text {ref }}$ must exceed 4.2 V before the outputs can be enabled and the Soft-Start latch released. If $\mathrm{V}_{\mathrm{CC}}$ falls below 8.4 V or $\mathrm{V}_{\text {ref }}$ falls below 3.6 V , the outputs are disabled and the Soft-Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off-line bootstrap start-up circuit. Typical start-up current is $500 \mu \mathrm{~A}$.

## Output

The MC34025 has two high current totem pole outputs specifically designed for direct drive of power MOSFETs. They are capable of up to $\pm 2.0$ A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for $\mathrm{V}_{\mathrm{C}}$ and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate $\mathrm{V}_{\mathrm{C}}$ supply input also allows the designer added flexibility in tailoring the drive voltage independent of $\mathrm{V}_{\mathrm{CC}}$.

## Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of $\pm 1.0 \%$ at $25^{\circ} \mathrm{C}$. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

## Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. All bypass capacitors
and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing or snubbing.

## Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp $\left(\mathrm{S}_{\mathrm{e}}\right)$ is added to the on-time $\operatorname{ramp}\left(\mathrm{S}_{\mathrm{n}}\right)$ of the current-sense waveform, stability can be achieved (see Figure 21).

One must be careful not to add too much ramp compensation. If too much is added, the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figures 29A and 29B show examples of two different ways in which external ramp compensation can be implemented.


Figure 21. Ramp Compensation
A simple equation can be used to calculate the amount of external ramp necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 37 are also shown.

$$
\mathrm{Se}=\frac{\mathrm{V}_{\mathrm{O}}}{\mathrm{~L}}\left(\frac{\mathrm{~N}_{\mathrm{S}}}{\mathrm{~N}_{\mathrm{P}}}\right)\left(\mathrm{R}_{\mathrm{S}}\right) A_{\mathrm{i}}
$$

$$
\text { where: } \left.\begin{array}{rl}
\mathrm{V}_{\mathrm{O}} & =\text { DC output voltage } \\
\mathrm{N}_{\mathrm{P},} \mathrm{~N}_{\mathrm{S}}= & \text { number of power transformer primary } \\
& \text { or secondary turns }
\end{array}\right\} \begin{aligned}
\mathrm{A}_{\mathrm{i}} & =\text { gain of the current sense network } \\
& \text { (see Figures } 26,27 \text { and } 28 \text { ) } \\
\mathrm{L}= & \text { output inductor } \\
\mathrm{R}_{\mathrm{S}}= & \text { current sense resistance } \\
\text { For the application circuit: } \mathrm{S}_{\mathrm{e}} & =\frac{5}{1.8 \mu}\left(\frac{4}{16}\right)(0.3)(0.55) \\
& =0.115 \mathrm{~V} / \mu \mathrm{s}
\end{aligned}
$$

## MC34025, MC33025

PIN FUNCTION DESCRIPTION

| Pin No. | Function | Description |
| :---: | :---: | :---: |
| DIP/SOIC |  |  |
| 1 | Error Amp Inverting Input | This pin is usually used for feedback from the output of the power supply. |
| 2 | Error Amp Noninverting Input | This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to $\mathrm{V}_{\text {ref }}$, however an external reference can also be used. |
| 3 | Error Amp Output | This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter. |
| 4 | Clock | This is a bidirectional pin used for synchronization. |
| 5 | $\mathrm{R}_{\mathrm{T}}$ | The value of $\mathrm{R}_{\mathrm{T}}$ sets the charge current through timing Capacitor, $\mathrm{C}_{\mathrm{T}}$. |
| 6 | $\mathrm{C}_{\mathrm{T}}$ | In conjunction with $\mathrm{R}_{\mathrm{T}}$, the timing Capacitor sets the switching frequency. Because this part is a push-pull output, each output runs at one-half the frequency set at this pin. |
| 7 | Ramp Input | For voltage mode operation this pin is connected to $\mathrm{C}_{\mathrm{T}}$. For current mode operation this pin is connected through a filter to the current sensing element. |
| 8 | Soft-Start | A capacitor at this pin sets the Soft-Start time. |
| 9 | Current Limit/Shutdown | This pin has two functions. First, it provides cycle-by-cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft-Start cycle. |
| 10 | Ground | This pin is the ground for the control circuitry. |
| 11 | Output A | This is a high current totem pole output. |
| 12 | Power Ground | This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry. |
| 13 | $\mathrm{V}_{\mathrm{C}}$ | This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry. |
| 14 | Output B | This is a high current totem pole output. |
| 15 | $\mathrm{V}_{\text {CC }}$ | This pin is the positive supply of the control IC. |
| 16 | $\mathrm{V}_{\text {ref }}$ | This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier. |



In voltage mode operation, the control range on the output of the Error Amplifier from 0\% to $90 \%$ duty cycle is from 2.25 V to 4.05 V .

Figure 22. Voltage Mode Operation


In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn-on of a power MOSFET.

Figure 23. Current Mode Operation


Additional dead time can be added by the addition of a dead time resistor from $\mathrm{V}_{\text {ref }}$ to $\mathrm{C}_{\mathrm{T}}$. See text on oscillator section for more information.

Figure 24. Dead Time Addition


The sync pulse fed into the clock pin must be at least 3.9 V . $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\top}$ need to be set $10 \%$ slower than the sync frequency. This circuit is also used in voltage mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set $10 \%$ slower.

Figure 25. External Clock Synchronization


The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$
A_{i}=\frac{R_{\text {Sense }}}{\text { turns ratio }}
$$

Figure 26. Resistive Current Sensing


Figure 27. Primary Side Current Sensing
The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

$$
A_{i}=\frac{\mathrm{R}_{\mathrm{w}}}{\text { turns ratio }}
$$

## MC34025, MC33025



This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor $\mathrm{C}_{1}$ provides $A C$ coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors $R_{1}$ and $R_{2}$.

Figure 29A. Slope Compensation (Noise Sensitive)


When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor $R_{M}$ and capacitor $\mathrm{C}_{\mathrm{M}}$ provide the added slope necessary. By choosing $\mathrm{R}_{\mathrm{M}}$ and $\mathrm{C}_{\mathrm{M}}$ with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose $C_{M}$, then $R_{M}$ can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current $I_{M}$ can be calculated by $I_{M}=C_{M} S_{e}$. Then $R_{M}$ can be calculated by $\mathrm{R}_{\mathrm{M}}=\mathrm{V}_{\mathrm{CC}} / \mathrm{I}_{\mathrm{M}}$.

Figure 29B. Slope Compensation (Noise Immune)


Figure 30. Current Mode Master/Slave Operation Over Short Distances

## MC34025, MC33025



Figure 31. Synchronization Over Long Distances


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft-Start current is not affected by $\mathrm{R}_{1}$.

$$
\text { The new equation for Soft-Start is } \quad t \approx \frac{V_{\text {clamp }}+0.6}{9.0 \mu \mathrm{~A}}\left(\mathrm{C}_{\mathrm{SS}}\right)
$$

In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 32. Buffered Maximum Clamp Level


Figure 34. Isolated MOSFET Drive


The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of the capacitor in series with the base.

Figure 33. Bipolar Transistor Drive


Figure 35. Direct Transformer Drive

The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.


A series gate resistor may be needed to damp high frequency parasitic oscillation caused by a MOSFET's input capacitance and any series wiring inductance in the gate-source circuit. The series resistor will also decrease the MOSFET's switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 36. MOSFET Parasitic Oscillations



Figure 38. PC Board With Components

(Top View)


Figure 39. PC Board Without Components

## UC3842A, UC3843A, UC2842A, UC2843A

## High Performance Current Mode Controllers

The UC3842A, UC3843A series of high performance fixed frequency current mode controllers are specifically designed for off-line and dc-to-dc converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in an 8-pin dual-in-line plastic package as well as the 14 -pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX842A has UYLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX843A is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Direct Interface with ON Semiconductor SENSEFET Products

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


SO-14 D SUFFIX CASE 751A


SO-8 D1 SUFFIX CASE 751

## PIN CONNECTIONS



See detailed ordering and shipping information in the package dimensions section on page 1800 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 1801 of this data sheet.


Pin numbers in parenthesis are for the $D$ suffix $S O-14$ package.
Figure 1. Simplified Block Diagram

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec) | $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}$ | 30 | V |
| Total Power Supply and Zener Current | ( $\mathrm{Icc}_{\text {+ }}+\mathrm{Iz}$ ) | 30 | mA |
| Output Current, Source or Sink (Note 1) | 10 | 1.0 | A |
| Output Energy (Capacitive Load per Cycle) | W | 5.0 | $\mu \mathrm{J}$ |
| Current Sense and Voltage Feedback Inputs | $V_{\text {in }}$ | -0.3 to +5.5 | V |
| Error Amp Output Sink Current | 10 | 10 | mA |
| Power Dissipation and Thermal Characteristics <br> D Suffix, Plastic Package Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air <br> N Suffix, Plastic Package Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{P}_{\mathrm{D}}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 862 \\ & 145 \\ & \\ & 1.25 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ \mathrm{~W} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | + 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature UC3842A, UC3843A UC2842A, UC2843A | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -25 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum Package power dissipation limits must be observed.

## UC3842A, UC3843A, UC2842A, UC2843A

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$, [Note 2], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ [Note 3], unless otherwise noted.)

| Characteristics | Symbol | UC284XA |  |  | UC384XA |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |

REFERENCE SECTION

| Reference Output Voltage ( $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {ref }}$ | 4.95 | 5.0 | 5.05 | 4.9 | 5.0 | 5.1 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 25 V ) | Regline | - | 2.0 | 20 | - | 2.0 | 20 | mV |
| Load Regulation ( $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 20 mA ) | Regload | - | 3.0 | 25 | - | 3.0 | 25 | mV |
| Temperature Stability | $\mathrm{T}_{\mathrm{S}}$ | - | 0.2 | - | - | 0.2 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Total Output Variation over Line, Load, Temperature | $\mathrm{V}_{\text {ref }}$ | 4.9 | - | 5.1 | 4.82 | - | 5.18 | V |
| Output Noise Voltage ( $\mathrm{f}=10 \mathrm{~Hz}$ to 10 kHz, <br> $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\mathrm{n}}$ | - | 50 | - | - | 50 | - | $\mu \mathrm{V}$ |
| Long Term Stability ( $\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}$ for 1000 Hours) | S | - | 5.0 | - | - | 5.0 | - | mV |
| Output Short Circuit Current | ISC | -30 | -85 | -180 | -30 | -85 | -180 | mA |

OSCILLATOR SECTION

| $\begin{aligned} & \text { Frequency } \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{f}_{\text {osc }}$ | $\begin{aligned} & 47 \\ & 46 \end{aligned}$ | 52 | $\begin{aligned} & 57 \\ & 60 \end{aligned}$ | $\begin{aligned} & 47 \\ & 46 \end{aligned}$ | 52 | $\begin{aligned} & 57 \\ & 60 \end{aligned}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 25 V ) | $\Delta \mathrm{f}_{\text {osc }} / \Delta \mathrm{V}$ | - | 0.2 | 1.0 | - | 0.2 | 1.0 | \% |
| Frequency Change with Temperature $T_{A}=T_{\text {low }} \text { to } T_{\text {high }}$ | $\Delta \mathrm{f}_{\text {osc } / \Delta^{\prime}}$ | - | 5.0 | - | - | 5.0 | - | \% |
| Oscillator Voltage Swing (Peak-to-Peak) | $V_{\text {osc }}$ | - | 1.6 | - | - | 1.6 | - | V |
| $\begin{aligned} & \text { Discharge Current (V} \begin{array}{l} \text { osc } \\ \mathrm{T}_{J}=2.05^{\circ} \mathrm{C} \end{array} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{I}_{\text {dischg }}$ | $\begin{aligned} & 7.5 \\ & 7.2 \end{aligned}$ |  | $\begin{aligned} & 9.3 \\ & 9.5 \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 7.2 \end{aligned}$ | 8.4 | 9.3 9.5 | mA |

ERROR AMPLIFIER SECTION

| Voltage Feedback Input ( $\mathrm{V}_{\mathrm{O}}=2.5 \mathrm{~V}$ ) | $\mathrm{V}_{\mathrm{FB}}$ | 2.45 | 2.5 | 2.55 | 2.42 | 2.5 | 2.58 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{B}}$ | - | -0.1 | -1.0 | - | -0.1 | -2.0 | $\mu \mathrm{A}$ |
| Open Loop Voltage Gain ( $\mathrm{V}_{\mathrm{O}}=2.0 \mathrm{~V}$ to 4.0 V ) | Avol | 65 | 90 | - | 65 | 90 | - | dB |
| Unity Gain Bandwidth ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | BW | 0.7 | 1.0 | - | 0.7 | 1.0 | - | MHz |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 25 V ) | PSRR | 60 | 70 | - | 60 | 70 | - | dB |
| Output Current <br> Sink ( $\mathrm{V}_{\mathrm{O}}=1.1 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) <br> Source ( $\mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) | Isink Isource | $\begin{gathered} 2.0 \\ -0.5 \end{gathered}$ | $\begin{gathered} 12 \\ -1.0 \end{gathered}$ |  | $\begin{gathered} 2.0 \\ -0.5 \end{gathered}$ | $\begin{gathered} 12 \\ -1.0 \end{gathered}$ | - | mA |
| $\begin{aligned} & \text { Output Voltage Swing } \\ & \text { High State }\left(R_{L}=15 \mathrm{k} \text { to ground, } \mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}\right) \\ & \text { Low State }\left(\mathrm{R}_{\mathrm{L}}=15 \mathrm{k} \text { to } \mathrm{V}_{\text {ref }}, \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ <br> $\mathrm{V}_{\mathrm{OL}}$ |  | $\begin{aligned} & 6.2 \\ & 0.8 \end{aligned}$ | $\overline{1.1}$ | 5.0 | $\begin{aligned} & 6.2 \\ & 0.8 \\ & \hline \end{aligned}$ | $\overline{-} \cdot 1$ | V |

2. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for UC3842A, UC3843A
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for UC3842A, UC3843A
$-25^{\circ} \mathrm{C}$ for UC2842A, UC2843A $+85^{\circ} \mathrm{C}$ for UC2842A, UC2843A

## UC3842A, UC3843A, UC2842A, UC2843A

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$, [Note 4], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ [Note 5], unless otherwise noted.)

| Characteristics | UC284XA | UC384XA |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  | Min | Typ | Max | Min | Typ | Max | Unit |

CURRENT SENSE SECTION

| Current Sense Input Voltage Gain (Notes 6 \& 7) | $\mathrm{A}_{\mathrm{V}}$ | 2.85 | 3.0 | 3.15 | 2.85 | 3.0 | 3.15 | $\mathrm{~V} / \mathrm{V}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum Current Sense Input Threshold (Note 6) | $\mathrm{V}_{\text {th }}$ | 0.9 | 1.0 | 1.1 | 0.9 | 1.0 | 1.1 | V |
| Power Supply Rejection Ratio <br> $\mathrm{V}_{\mathrm{CC}}=12$ to 25 V (Note 6) | PSRR | - | 70 | - | - | 70 | - | dB |
| Input Bias Current | $\mathrm{I}_{\mathrm{IB}}$ | - | -2.0 | -10 | - | -2.0 | -10 | $\mu \mathrm{~A}$ |
| Propagation Delay (Current Sense Input to Output) | $\mathrm{t}_{\text {PLH(in/out) }}$ | - | 150 | 300 | - | 150 | 300 | ns |

OUTPUT SECTION

| Output Voltage | $\mathrm{V}_{\text {OL }}$ | - | 0.1 | 0.4 | - | 0.1 | 0.4 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Low State ( ${ }_{\text {sink }}=20 \mathrm{~mA}$ ) |  |  |  |  |  |  |  |  |
| ( $\mathrm{I}_{\text {Sink }}=200 \mathrm{~mA}$ ) |  | - | 1.6 | 2.2 | - | 1.6 | 2.2 |  |
| High State ( $\mathrm{I}_{\text {Sink }}=20 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{OH}}$ | 13 | 13.5 | - | 13 | 13.5 | - |  |
| $\left(I_{\text {Sink }}=200 \mathrm{~mA}\right)$ |  | 12 | 13.4 | - | 12 | 13.4 | - |  |
| Output Voltage with UVLO Activated $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{I}_{\mathrm{Sink}}=1.0 \mathrm{~mA}$ | $\mathrm{V}_{\text {OL(UVLO) }}$ | - | 0.1 | 1.1 | - | 0.1 | 1.1 | V |
| Output Voltage Rise Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | 150 | - | 50 | 150 | ns |
| Output Voltage Fall Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | 150 | - | 50 | 150 | ns |

UNDERVOLTAGE LOCKOUT SECTION

| Startup Threshold | $\mathrm{V}_{\text {th }}$ |  |  |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UCX842A |  | 15 | 16 | 17 | 14.5 | 16 | 17.5 | V |
| UCX843A |  | 7.8 | 8.4 | 9.0 | 7.8 | 8.4 | 9.0 |  |
| Minimum Operating Voltage After Turn-On | $\mathrm{V}_{\text {CC(min) }}$ |  |  |  |  |  |  | V |
| UCX842A |  | 9.0 | 10 | 11 | 8.5 | 10 | 11.5 |  |
| UCX843A |  | 7.0 | 7.6 | 8.2 | 7.0 | 7.6 | 8.2 |  |

PWM SECTION

| Duty Cycle <br> Maximum <br> Minimum | DC <br> max <br>  <br> $\mathrm{DC}_{\min }$ | 94 | 96 | - | 94 | 96 | - | $\%$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

TOTAL DEVICE

| Power Supply Current (Note 4) <br> Startup: <br> (VCC $=6.5 \mathrm{~V}$ for UCX843A, <br> 14 V for UCX842A) Operating | I CC |  |  |  |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply Zener Voltage (ICC $=25 \mathrm{~mA})$ |  | - | 0.5 | 1.0 | - | 0.5 | 1.0 |  |

4. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for UC3842A, UC3843A $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for UC3842A, UC3843A $-25^{\circ} \mathrm{C}$ for UC2842A, UC2843A $+85^{\circ} \mathrm{C}$ for UC2842A, UC2843A
6. This parameter is measured at the latch trip point with $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$.
7. Comparator gain is defined as: $\mathrm{A}_{\mathrm{V}} \frac{\Delta \mathrm{V} \text { Output Compensation }}{\Delta \mathrm{V} \text { Current Sense Input }}$


Figure 2. Timing Resistor versus Oscillator Frequency


Figure 4. Oscillator Discharge Current versus Temperature


Figure 3. Output Deadtime versus Oscillator Frequency


Figure 5. Maximum Output Duty Cycle versus Timing Resistor


Figure 6. Error Amp Small Signal Transient Response


Figure 7. Error Amp Large Signal Transient Response


Figure 8. Error Amp Open Loop Gain and Phase versus Frequency


Figure 10. Reference Voltage Change versus Source Current


Figure 12. Reference Load Regulation


Figure 11. Reference Short Circuit Current versus Temperature


Figure 13. Reference Line Regulation


Figure 14. Output Saturation Voltage versus Load Current


Figure 16. Output Cross Conduction


Figure 15. Output Waveform


Figure 17. Supply Current versus
Supply Voltage

## UC3842A, UC3843A, UC2842A, UC2843A



Pin numbers in parenthesis are for the D suffix SO -14 package.
Figure 18. Representative Block Diagram

Capacitor $\mathrm{C}_{\mathrm{T}}$




Output/


Large $\mathrm{R}_{T} /$ Small $\mathrm{C}_{\mathrm{T}}$


Figure 19. Timing Diagram

The UC3842A, UC3843A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 18.

## Oscillator

The oscillator frequency is programmed by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged from the 5.0 V reference through resistor $\mathrm{R}_{\mathrm{T}}$ to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates and internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 2 shows $\mathrm{R}_{\mathrm{T}}$ versus Oscillator Frequency and Figure 3, Output Deadtime versus Frequency, both for given values of $C_{T}$. Note that many values of $R_{T}$ and $C_{T}$ will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within $\pm 10 \%$ at $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 4 and 5.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 21. For reliable locking, the free-running oscillator frequency should be set about $10 \%$ less than the clock frequency. A method for multi unit synchronization is shown in Figure 22. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

## Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB , and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 8). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is $-2.0 \mu \mathrm{~A}$ which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provide for external loop compensation (Figure 31). The output voltage is offset by two diode drops ( $\approx 1.4 \mathrm{~V}$ ) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state ( $\mathrm{V}_{\mathrm{OL}}$ ). This occurs when the power supply is operating and the load
is removed, or at the beginning of a soft-start interval (Figures 24, 25). The Error Amp minimum feedback resistance is limited by the amplifier's source current $(0.5 \mathrm{~mA})$ and the required output voltage $\left(\mathrm{V}_{\mathrm{OH}}\right)$ to reach the comparator's 1.0 V clamp level:

$$
\mathrm{R}_{\mathrm{f}(\min )} \approx \frac{3.0(1.0 \mathrm{~V})+1.4 \mathrm{~V}}{0.5 \mathrm{~mA}}=8800 \Omega
$$

## Current Sense Comparator and PWM Latch

The UC3842A, UC3843A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ in series with the source of output switch Q 1 . This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$
\mathrm{I}_{\mathrm{pk}}=\frac{\mathrm{V}_{(\operatorname{Pin} 1)}-1.4 \mathrm{~V}}{3 \mathrm{R}_{\mathrm{S}}}
$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V . Therefore the maximum peak switch current is:

$$
\mathrm{I}_{\mathrm{pk}(\max )}=\frac{1.0 \mathrm{~V}}{\mathrm{R}_{\mathrm{S}}}
$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of $\mathrm{R}_{\mathrm{S}}$ to a reasonable level. A simple method to adjust this voltage is shown in Figure 23. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $\mathrm{I}_{\mathrm{pk}(\max )}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 27.

PIN FUNCTION DESCRIPTION

| Pin |  | Function | Description |
| :---: | :---: | :---: | :---: |
| 8-Pin | 14-Pin |  |  |
| 1 | 1 | Compensation | This pin is Error Amplifier output and is made available for loop compensation. |
| 2 | 3 | Voltage Feedback | This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider. |
| 3 | 5 | Current Sense | A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction. |
| 4 | 7 | $\mathrm{R}_{T} / \mathrm{C}_{\mathrm{T}}$ | The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor $\mathrm{R}_{\mathrm{T}}$ to $\mathrm{V}_{\text {ref }}$ and capacitor $\mathrm{C}_{\mathrm{T}}$ to ground. Operation to 500 kHz is possible. |
| 5 | - | Gnd | This pin is the combined control circuitry and power ground (8-pin package only). |
| 6 | 10 | Output | This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. |
| 7 | 12 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the control IC. |
| 8 | 14 | $\mathrm{V}_{\text {ref }}$ | This is the reference output. It provides charging current for capacitor $\mathrm{C}_{\boldsymbol{T}}$ through resistor $\mathrm{R}_{\mathrm{T}}$. |
| - | 8 | Power Ground | This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry. |
| - | 11 | $\mathrm{V}_{\mathrm{C}}$ | The Output high state $\left(\mathrm{V}_{\mathrm{OH}}\right)$ is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry. |
| - | 9 | Gnd | This pin is the control circuitry ground return (14-pin package only) and is connected back to the power source ground. |
| - | 2,4,6,13 | NC | No connection (14-pin package only). These pins are not internally connected. |

## Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal $\left(\mathrm{V}_{\mathrm{CC}}\right)$ and the reference output $\left(\mathrm{V}_{\text {ref }}\right)$ are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The $\mathrm{V}_{\mathrm{CC}}$ comparator upper and lower thresholds are $16 \mathrm{~V} / 10 \mathrm{~V}$ for the UCX842A, and $8.4 \mathrm{~V} / 7.6 \mathrm{~V}$ for the UCX843A. The $\mathrm{V}_{\text {ref }}$ comparator upper and lower thresholds are $3.6 \mathrm{~V} / 3.4 \mathrm{~V}$. The large hysteresis and low startup current of the UCX842A makes it ideally suited in off-line converter applications where efficient bootstrap startup techniques are required (Figure 34). The UCX843A is intended for lower voltage dc to dc converter applications. A 36 V zener is connected as a shunt regulator form $\mathrm{V}_{\mathrm{CC}}$ to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX842A is 11 V and 8.2 V for the UCX843A.

## Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to $\pm 1.0 \mathrm{~A}$ peak drive current
and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.
The SO-14 surface mount package provides separate pins for $\mathrm{V}_{\mathrm{C}}$ (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $\mathrm{I}_{\mathrm{pk}(\max )}$ clamp level. The separate $\mathrm{V}_{\mathrm{C}}$ supply input allows the designer added flexibility in tailoring the drive voltage independent of $\mathrm{V}_{\mathrm{CC}}$. A zener clamp is typically connected to this input when driving power MOSFETs in systems where $\mathrm{V}_{\mathrm{CC}}$ is greater than 20 V . Figure 26 shows proper power and control ground connections in a current sensing power MOSFET application.

## Reference

The 5.0 V bandgap reference is trimmed to $\pm 1.0 \%$ tolerance at $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ on the UC284XA, and $\pm 2.0 \%$ on the UC384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

## DESIGN CONSIDERATIONS

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High Frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors $(0.1 \mu \mathrm{~F})$ connected directly to $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}$, and $\mathrm{V}_{\text {ref }}$ may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than $50 \%$ with continuous inductor current. This instability is independent of the regulators closed-loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 20A shows the phenomenon graphically. At $\mathrm{t}_{0}$, switch conduction begins, causing the inductor current to rise at a slope of $m_{1}$. This slope is a function of the input voltage divided by the inductance. At $t_{1}$, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of $\mathrm{m}_{2}$ until the next oscillator cycle. The unstable condition can be shown if a pertubation is added to the control voltage, resulting in a small $\Delta \mathrm{I}$ (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on $\left(\mathrm{t}_{2}\right)$ is increased by $\Delta \mathrm{I}+\Delta \mathrm{I} \mathrm{m} 2 / \mathrm{m} 1$. The minimum current at the next cycle
( $\mathrm{t}_{3}$ ) decreases to $\left(\Delta \mathrm{I}+{ }_{\Delta} \mathrm{I} \mathrm{m}_{2} / \mathrm{m}_{1}\right)\left(\mathrm{m}_{2} / \mathrm{m}_{1}\right)$. This pertubation is multiplied by $\mathrm{m}_{2} \cdot \mathrm{~m}_{1}$ on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If $\mathrm{m}_{2} / \mathrm{m}_{1}$ is greater than 1 , the converter will be unstable. Figure 20B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the $\Delta \mathrm{I}$ pertubation will decrease to zero on succeeding cycles. This compensation ramp ( $\mathrm{m}_{3}$ ) must have a slope equal to or slightly greater than $m_{2} / 2$ for stability. With $\mathrm{m}_{2} / 2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 33).


Figure 20. Continuous Current Waveforms


The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300 mV below ground.

Figure 21. External Clock Synchronization


Figure 22. External Duty Cycle Clamp and Multi Unit Synchronization


Figure 23. Adjustable Reduction of Clamp Level


Figure 24. Soft-Start Circuit


Figure 25. Adjustable Buffered Reduction of Clamp Level with Soft-Start


The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. Current Waveform Spike Suppression


Series gate resistor $\mathrm{R}_{\mathrm{g}}$ will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 28. MOSFET Parasitic Oscillations


The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor $\mathrm{C}_{1}$.

Figure 29. Bipolar Transistor Drive


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $\mathrm{T}_{\mathrm{A}(\text { min) }}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k .

Figure 31. Latched Shutdown


Figure 30. Isolated MOSFET Drive


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.


Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 32. Error Amplifier Compensation

## UC3842A, UC3843A, UC2842A, UC2843A



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.
Figure 33. Slope Compensation


| Test |  | Conditions | Results |
| :---: | :---: | :---: | :---: |
| Line Regulation: | $\begin{aligned} & 5.0 \mathrm{~V} \\ & \pm 12 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {in }}=95 \mathrm{Vac}$ to 130 Vac | $\begin{aligned} & \Delta=50 \mathrm{mV} \text { or } \pm 0.5 \% \\ & \Delta=24 \mathrm{mV} \text { or } \pm 0.1 \% \end{aligned}$ |
| Load Regulation: | $\begin{aligned} & 5.0 \mathrm{~V} \\ & \pm 12 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & V_{\text {in }}=115 \mathrm{Vac}, I_{\text {out }}=1.0 \mathrm{~A} \text { to } 4.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=115 \mathrm{Vac}, I_{\text {out }}=100 \mathrm{~mA} \text { to } 300 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & \Delta=300 \mathrm{mV} \text { or } \pm 3.0 \% \\ & \Delta=60 \mathrm{mV} \text { or } \pm 0.25 \% \end{aligned}$ |
| Output Ripple: | $\begin{aligned} & 5.0 \mathrm{~V} \\ & \pm 12 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}$ | $\begin{aligned} & 40 \mathrm{mV}_{\mathrm{pp}} \\ & 80 \mathrm{mV}_{\mathrm{pp}} \end{aligned}$ |
| Efficiency |  | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}$ | 70\% |

All outputs are at nominal load currents, unless otherwise noted.

ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: |
| UC3842AN | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | PDIP-8 | 50 Units/Rail |
| UC3842AD |  | SO-14 | 55 Units/Rail |
| UC3842ADR2 |  | SO-14 | 2500 Tape \& Reel |
| UC3843AN |  | PDIP-8 | 50 Units/Rail |
| UC3843AD |  | SO-14 | 55 Units/Rail |
| UC3843ADR2 |  | SO-14 | 2500 Tape \& Reel |
| UC3843AD1 |  | SO-8 | 98 Units/Rail |
| UC3843AD1R2 |  | SO-8 | 2500 Tape \& Reel |
| UC2842AN | $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ | PDIP-8 | 50 Units/Rail |
| UC2842AD |  | SO-14 | 55 Units/Rail |
| UC2842ADR2 |  | SO-14 | 2500 Tape \& Reel |
| UC2843AN |  | PDIP-8 | 50 Units/Rail |
| UC2843AD |  | SO-14 | 55 Units/Rail |
| UC2843ADR2 |  | SO-14 | 2500 Tape \& Reel |
| UC2843AD1 |  | SO-8 | 98 Units/Rail |
| UC2843AD1R2 |  | SO-8 | 2500 Tape \& Reel |

# UC3842A，UC3843A，UC2842A，UC2843A 

MARKING DIAGRAMS


| $\begin{gathered} \text { SO-14 } \\ \text { D SUFFIX } \\ \text { CASE } 751 A \end{gathered}$ |
| :---: |
| $\begin{aligned} & 14 \\ & \text { 月月 } \\ & \text { 月 } \end{aligned}$ |
| $\begin{aligned} & \text { UCx84xAD } \\ 0 & \text { AWLYWW } \end{aligned}$ |
|  1 |


x = 2 or 3
x = 2 or 3
A = Assembly Location
A = Assembly Location
WL, L = Wafer Lot
WL, L = Wafer Lot
YY, Y = Year
YY, Y = Year
WW, W = Work Week
WW, W = Work Week

## UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV

## High Performance Current Mode Controllers

The UC3842B, UC3843B series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in an 8-pin dual-in-line and surface mount (SO-8) plastic package as well as the 14 -pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX843B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current


Figure 1. Simplified Block Diagram


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PDIP-8 N SUFFIX CASE 626

SO-8 D1 SUFFIX CASE 751

SO-14 D SUFFIX CASE 751A


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 1817 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 1818 of this data sheet.

## UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec) | $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}$ | 30 | V |
| Total Power Supply and Zener Current | $\left(I_{C c}+I_{z}\right)$ | 30 | mA |
| Output Current, Source or Sink (Note 1) | 10 | 1.0 | A |
| Output Energy (Capacitive Load per Cycle) | W | 5.0 | $\mu \mathrm{J}$ |
| Current Sense and Voltage Feedback Inputs | $\mathrm{V}_{\text {in }}$ | -0.3 to +5.5 | V |
| Error Amp Output Sink Current | 10 | 10 | mA |
| Power Dissipation and Thermal Characteristics <br> D Suffix, Plastic Package, SO-14 Case 751A Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air <br> D1 Suffix, Plastic Package, SO-8 Case 751 Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air <br> N Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $\mathrm{P}_{\mathrm{D}}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $P_{D}$ <br> $R_{\text {日JA }}$ | $\begin{aligned} & 862 \\ & 145 \\ & 702 \\ & 178 \\ & \\ & 1.25 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature <br> UC3842B, UC3843B <br> UC2842B, UC2843B <br> UC3842BV, UC3843BV, NCV3843BV | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -25 \text { to }+85 \\ -40 \text { to }+105 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$ [Note 2], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

| Characteristics |  | UC284XB |  |  | UC384XB, XBV |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  | Symbol | Min | Typ | Max | Min | Typ | Max | Unit |

REFERENCE SECTION

| Reference Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {ref }}$ | 4.95 | 5.0 | 5.05 | 4.9 | 5.0 | 5.1 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$ to 25 V$)$ | Reg $_{\text {line }}$ | - | 2.0 | 20 | - | 2.0 | 20 | mV |
| Load Regulation $\left(\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}\right.$ to 20 mA$)$ | Regload | - | 3.0 | 25 | - | 3.0 | 25 | mV |
| Temperature Stability | $\mathrm{T}_{\mathrm{S}}$ | - | 0.2 | - | - | 0.2 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {ref }}$ | 4.9 | - | 5.1 | 4.82 | - | 5.18 | V |
| Output Noise Voltage $\left(\mathrm{f}=10 \mathrm{~Hz}\right.$ to $\left.10 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 50 | - | - | 50 | - | $\mu \mathrm{V}$ |
| Long Term Stability $\left(\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}\right.$ for 1000 Hours $)$ | S | - | 5.0 | - | - | 5.0 | - | mV |
| Output Short Circuit Current | $\mathrm{I}_{\mathrm{SC}}$ | -30 | -85 | -180 | -30 | -85 | -180 | mA |

OSCILLATOR SECTION

| $\begin{aligned} & \text { Frequency } \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } T_{\text {high }} \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C}\left(\mathrm{R}_{\mathrm{T}}=6.2 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}\right) \end{aligned}$ | fosc | $\begin{gathered} 49 \\ 48 \\ 225 \\ \hline \end{gathered}$ | $\begin{gathered} 52 \\ - \\ 250 \\ \hline \end{gathered}$ | $\begin{gathered} 55 \\ 56 \\ 275 \\ \hline \end{gathered}$ | $\begin{gathered} 49 \\ 48 \\ 225 \\ \hline \end{gathered}$ | $\begin{gathered} 52 \\ - \\ 250 \\ \hline \end{gathered}$ | $\begin{gathered} 55 \\ 56 \\ 275 \\ \hline \end{gathered}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 25 V ) | $\Delta \mathrm{f}_{\text {OSc }} / \Delta \mathrm{V}$ | - | 0.2 | 1.0 | - | 0.2 | 1.0 | \% |
| Frequency Change with Temperature, $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ | $\Delta \mathrm{f}_{\mathrm{OSc}} / \Delta \mathrm{T}$ | - | 1.0 | - | - | 0.5 | - | \% |
| Oscillator Voltage Swing (Peak-to-Peak) | V OSC | - | 1.6 | - | - | 1.6 | - | V |
| $\begin{gathered} \text { Discharge Current (VOSC }=2.0 \mathrm{~V}) \\ \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\mathrm{UC284XB,} \mathrm{UC384XB)} \\ \text { (UC384XBV) } \end{gathered}$ | ${ }^{\text {dischg }}$ | $\begin{aligned} & 7.8 \\ & 7.5 \end{aligned}$ | 8.3 | 8.8 8.8 | 7.8 7.6 7.2 | 8.3 | $\begin{aligned} & 8.8 \\ & 8.8 \\ & 8.8 \end{aligned}$ | mA |

1. Maximum Package power dissipation limits must be observed.
2. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for UC3842B, UC3843B; $-25^{\circ} \mathrm{C}$ for UC2842B, UC2843B; $-40^{\circ} \mathrm{C}$ for UC3842BV, UC3843BV
Thigh $=+70^{\circ} \mathrm{C}$ for UC3842B, UC3843B; $+85^{\circ} \mathrm{C}$ for UC2842B, UC2843B; $+105^{\circ} \mathrm{C}$ for UC3842BV, UC3843BV
NCV3843BV: $T_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.

## UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$ [Note 4], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 5], unless otherwise noted.)

| Characteristics | Symbol | UC284XB |  |  | UC384XB, XBV |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |

ERROR AMPLIFIER SECTION

| Voltage Feedback Input ( $\mathrm{V}_{\mathrm{O}}=2.5 \mathrm{~V}$ ) | $V_{\text {FB }}$ | 2.45 | 2.5 | 2.55 | 2.42 | 2.5 | 2.58 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB}}=5.0 \mathrm{~V}$ ) | $I_{\text {IB }}$ | - | -0.1 | -1.0 | - | -0.1 | -2.0 | $\mu \mathrm{A}$ |
| Open Loop Voltage Gain ( $\mathrm{V}_{\mathrm{O}}=2.0 \mathrm{~V}$ to 4.0 V ) | Avol | 65 | 90 | - | 65 | 90 | - | dB |
| Unity Gain Bandwidth ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | BW | 0.7 | 1.0 | - | 0.7 | 1.0 | - | MHz |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 25 V ) | PSRR | 60 | 70 | - | 60 | 70 | - | dB |
| Output Current <br> Sink ( $\mathrm{V}_{\mathrm{O}}=1.1 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) <br> Source ( $\mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) | ISink ISource | $\begin{gathered} 2.0 \\ -0.5 \end{gathered}$ | $\begin{gathered} 12 \\ -1.0 \end{gathered}$ | - | $\begin{gathered} 2.0 \\ -0.5 \end{gathered}$ | $\begin{gathered} 12 \\ -1.0 \end{gathered}$ | - | mA |
| Output Voltage Swing <br> High State ( $\mathrm{R}_{\mathrm{L}}=15 \mathrm{k}$ to ground, $\mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) <br> Low State ( $R_{L}=15 \mathrm{k}$ to $\mathrm{V}_{\text {ref }}, \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) <br> (UC284XB, UC384XB) <br> (UC384XBV) | $\mathrm{V}_{\mathrm{OH}}$ <br> $\mathrm{V}_{\mathrm{OL}}$ | 5.0 | $\begin{gathered} 6.2 \\ 0.8 \\ - \end{gathered}$ | - 1.1 | 5.0 | $\begin{aligned} & 6.2 \\ & 0.8 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & 1.1 \\ & 1.2 \end{aligned}$ | V |

## CURRENT SENSE SECTION

| Current Sense Input Voltage Gain (Notes 6 \& 7) <br> (UC284XB, UC384XB) <br> (UC384XBV) | $A_{V}$ | 2.85 - | 3.0 - | 3.15 - |  | $\begin{aligned} & 3.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 3.15 \\ & 3.25 \end{aligned}$ | V/V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum Current Sense Input Threshold (Note 6) (UC284XB, UC384XB) <br> (UC384XBV) | $\mathrm{V}_{\text {th }}$ | 0.9 | $1.0$ | 1.1 | $\begin{gathered} 0.9 \\ 0.85 \end{gathered}$ | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 1.1 \\ & 1.1 \end{aligned}$ | V |
| Power Supply Rejection Ratio (VCC 12 V to 25 V , Note 6) | PSRR | - | 70 | - | - | 70 | - | dB |
| Input Bias Current | $I_{\text {IB }}$ | - | -2.0 | -10 | - | -2.0 | -10 | $\mu \mathrm{A}$ |
| Propagation Delay (Current Sense Input to Output) | tplH(In/Out) | - | 150 | 300 | - | 150 | 300 | ns |

OUTPUT SECTION

| Output Voltage | $\mathrm{V}_{\text {OL }}$ | - | 0.1 | 0.4 | - | 0.1 | 0.4 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Low State ( $\mathrm{I}_{\text {Sink }}=20 \mathrm{~mA}$ ) |  |  |  |  |  |  |  |  |
| $\left(I_{\text {Sink }}=200 \mathrm{~mA}\right) \quad$ (UC284XB, UC384XB) |  | - | 1.6 | 2.2 | - | 1.6 | 2.2 |  |
| (UC384XBV) |  | - | - | - | - | 1.6 | 2.3 |  |
| High State ( ${ }_{\text {S }}$ ource $=20 \mathrm{~mA}$ ) (UC284XB, UC384XB) | $\mathrm{V}_{\mathrm{OH}}$ | 13 | 13.5 | - | 13 | 13.5 | - |  |
| (UC384XBV) |  | - | - | - | 12.9 | 13.5 | - |  |
| ( Source $^{\text {a }}$ = 200 mA ) |  | 12 | 13.4 | - | 12 | 13.4 | - |  |
| Output Voltage with UVLO Activated ( $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$, $\left.\mathrm{I}_{\text {Sink }}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {OL(UVLO) }}$ | - | 0.1 | 1.1 | - | 0.1 | 1.1 | V |
| Output Voltage Rise Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{t}_{\mathrm{r}}$ | - | 50 | 150 | - | 50 | 150 | ns |
| Output Voltage Fall Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | 150 | - | 50 | 150 | ns |

UNDERVOLTAGE LOCKOUT SECTION

| Startup Threshold (VCC) | $\mathrm{V}_{\mathrm{th}}$ |  |  |  |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UCX842B, BV |  | 15 | 16 | 17 | 14.5 | 16 | 17.5 |  |
| UCX843B, BV |  | 7.8 | 8.4 | 9.0 | 7.8 | 8.4 | 9.0 |  |
| Minimum Operating Voltage After Turn-On (VCC) | $\mathrm{V}_{\mathrm{CC}(\text { min })}$ |  |  |  |  |  |  | V |
| UCX842B, BV |  | 9.0 | 10 | 11 | 8.5 | 10 | 11.5 |  |
| UCX843B, BV | 7.0 | 7.6 | 8.2 | 7.0 | 7.6 | 8.2 |  |  |

4. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$T_{\text {low }}=0^{\circ} \mathrm{C}$ for UC3842B, UC3843B; $-25^{\circ} \mathrm{C}$ for UC2842B, UC2843B; $-40^{\circ} \mathrm{C}$ for UC3842BV, UC3843BV
$T_{\text {high }}=+70^{\circ} \mathrm{C}$ for UC3842B, UC3843B; $+85^{\circ} \mathrm{C}$ for UC2842B, UC2843B; $+105^{\circ} \mathrm{C}$ for UC3842BV, UC3843BV
NCV3843BV: $T_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
6. This parameter is measured at the latch trip point with $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$.
7. Comparator gain is defined as: $A_{V} \frac{\Delta V}{}$ Output Compensation
$\Delta V$ Current Sense Input

## UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$ [Note 8], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 9], unless otherwise noted.)

| Characteristics | Symbol | UC284XB |  |  | UC384XB, BV |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| PWM SECTION |  |  |  |  |  |  |  |  |
| Duty Cycle <br> Maximum (UC284XB, UC384XB) <br> (UC384XBV) <br> Minimum | $\begin{aligned} & \mathrm{DC}_{(\text {max })} \\ & \mathrm{DC}_{(\text {min })} \end{aligned}$ | 94 - | 96 - | $\overline{0}$ | 94 93 | 96 96 | 0 | \% |

TOTAL DEVICE

| Power Supply Current <br> Startup ( $\mathrm{V}_{\mathrm{CC}}=6.5 \mathrm{~V}$ for UCX843B, <br> ( $\mathrm{V}_{\mathrm{CC}} 14 \mathrm{~V}$ for UCX842B, BV) <br> Operating (Note 8) | $\mathrm{I}_{C C}+\mathrm{I}_{\mathrm{C}}$ | - | 0.3 12 | $\begin{aligned} & 0.5 \\ & 17 \\ & \hline \end{aligned}$ | - - | 0.3 12 | 0.5 17 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply Zener Voltage ( $\mathrm{I}_{\mathrm{CC}}=25 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{Z}}$ | 30 | 36 | - | 30 | 36 | - | V |

8. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
9. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$T_{\text {low }}=0^{\circ} \mathrm{C}$ for UC3842B, UC3843B; $-25^{\circ} \mathrm{C}$ for UC2842B, UC2843B; $-40^{\circ} \mathrm{C}$ for UC3842BV, UC3843BV
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for UC3842B, UC3843B; $+85^{\circ} \mathrm{C}$ for UC2842B, UC2843B; $+105^{\circ} \mathrm{C}$ for UC3842BV, UC3843BV
NCV3843BV: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.


Figure 2. Timing Resistor versus Oscillator Frequency


Figure 4. Oscillator Discharge Current versus Temperature


Figure 3. Output Deadtime versus Oscillator Frequency


Figure 5. Maximum Output Duty Cycle versus Timing Resistor

UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV


Figure 6. Error Amp Small Signal Transient Response


Figure 8. Error Amp Open Loop Gain and Phase versus Frequency


Figure 10. Reference Voltage Change versus Source Current


Figure 7. Error Amp Large Signal Transient Response


Figure 9. Current Sense Input Threshold versus Error Amp Output Voltage


Figure 11. Reference Short Circuit Current versus Temperature

## UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV



Figure 12. Reference Load Regulation


Figure 14. Output Saturation Voltage versus Load Current


Figure 16. Output Cross Conduction


Figure 13. Reference Line Regulation


Figure 15. Output Waveform


Figure 17. Supply Current versus Supply Voltage

# UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV 

PIN FUNCTION DESCRIPTION

| Pin |  | Function |  |
| :---: | :---: | :---: | :--- |
| 8-Pin | $\mathbf{1 4 - P i n}$ |  |  |

## OPERATING DESCRIPTION

The UC3842B, UC3843B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components. A representative block diagram is shown in Figure 18.

## Oscillator

The oscillator frequency is programmed by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged from the 5.0 V reference through resistor $\mathrm{R}_{\mathrm{T}}$ to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 2 shows $\mathrm{R}_{\mathrm{T}}$ versus Oscillator Frequency and Figure 3, Output Deadtime versus Frequency, both for given values of $\mathrm{C}_{\mathrm{T}}$. Note that many values of $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$ will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within $\pm 6 \%$ at 50 kHz . Also because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within $\pm 10 \%$ at 250 kHz . These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 4 and 5.

In many noise-sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 21. For reliable locking, the free-running oscillator frequency should be set about $10 \%$ less than the clock frequency. A method for multi-unit synchronization is shown in Figure 22. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

## Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB , and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 8). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is $-2.0 \mu \mathrm{~A}$ which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 32). The output voltage is offset by two diode drops ( $\approx 1.4 \mathrm{~V}$ ) and divided by three before it connects to the non-inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state $\left(\mathrm{V}_{\mathrm{OL}}\right)$.

This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 24, 25). The Error Amp minimum feedback resistance is limited by the amplifier's source current $(0.5 \mathrm{~mA})$ and the required output voltage $\left(\mathrm{V}_{\mathrm{OH}}\right)$ to reach the comparator's 1.0 V clamp level:

$$
\mathrm{R}_{\mathrm{f}(\min )} \approx \frac{3.0(1.0 \mathrm{~V})+1.4 \mathrm{~V}}{0.5 \mathrm{~mA}}=8800 \Omega
$$

## Current Sense Comparator and PWM Latch

The UC3842B, UC3843B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$
\mathrm{I}_{\mathrm{pk}}=\frac{\mathrm{V}_{(\mathrm{Pin} 1)}-1.4 \mathrm{~V}}{3 \mathrm{R}_{\mathrm{S}}}
$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V . Therefore the maximum peak switch current is:

$$
\mathrm{I}_{\mathrm{pk}(\max )}=\frac{1.0 \mathrm{~V}}{\mathrm{R}_{\mathrm{S}}}
$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of $\mathrm{R}_{\mathrm{S}}$ to a reasonable level. A simple method to adjust this voltage is shown in Figure 23. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $\mathrm{I}_{\mathrm{pk}(\max )}$ clamp voltage.
A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 27).


Figure 18. Representative Block Diagram


Figure 19. Timing Diagram

## Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal $\left(\mathrm{V}_{\mathrm{CC}}\right)$ and the reference output $\left(\mathrm{V}_{\text {ref }}\right)$ are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The $\mathrm{V}_{\mathrm{CC}}$ comparator upper and lower thresholds are $16 \mathrm{~V} / 10 \mathrm{~V}$ for the UCX842B, and $8.4 \mathrm{~V} / 7.6 \mathrm{~V}$ for the UCX843B. The $\mathrm{V}_{\text {ref }}$ comparator upper and lower thresholds are $3.6 \mathrm{~V} / 3.4 \mathrm{~V}$. The large hysteresis and low startup current of the UCX842B makes it ideally suited in off-line converter applications where efficient bootstrap startup techniques are required (Figure 34). The UCX843B is intended for lower voltage dc-to-dc converter applications. A 36 V zener is connected as a shunt regulator from $\mathrm{V}_{\mathrm{CC}}$ to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage $\left(\mathrm{V}_{\mathrm{CC}}\right)$ for the UCX842B is 11 V and 8.2 V for the UCX843B.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to $\pm 1.0$ A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for $\mathrm{V}_{\mathrm{C}}$ (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $\mathrm{I}_{\mathrm{pk}(\max )}$ clamp level. The separate $\mathrm{V}_{\mathrm{C}}$ supply input allows the designer added flexibility in tailoring the drive voltage independent of $\mathrm{V}_{\mathrm{CC}}$. A zener clamp is typically connected to this input when driving power MOSFETs in systems where $\mathrm{V}_{\mathrm{CC}}$ is greater than 20 V . Figure 26 shows proper power and control ground connections in a current-sensing power MOSFET application.

## Reference

The 5.0 V bandgap reference is trimmed to $\pm 1.0 \%$ tolerance at $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ on the UC284XB, and $\pm 2.0 \%$ on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has shortcircuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

## Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors $(0.1 \mu \mathrm{~F})$ connected directly to $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}$, and $\mathrm{V}_{\text {ref }}$ may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise-generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than $50 \%$ with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 20A shows the phenomenon graphically. At $t_{0}$, switch conduction begins, causing the inductor current to rise at a slope of $\mathrm{m}_{1}$. This slope is a function of the input voltage divided by the inductance. At $t_{1}$, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of $\mathrm{m}_{2}$, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small $\Delta \mathrm{I}$ (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on $\left(\mathrm{t}_{2}\right)$ is increased by $\Delta \mathrm{I}+\Delta \mathrm{I} \mathrm{m}_{2} / \mathrm{m}_{1}$. The minimum current at the next cycle $\left(\mathrm{t}_{3}\right)$ decreases to $\left(\Delta \mathrm{I}+\Delta \mathrm{I} \mathrm{m}_{2} / \mathrm{m}_{1}\right)\left(\mathrm{m}_{2} / \mathrm{m}_{1}\right)$. This perturbation is multiplied by $\mathrm{m}_{2} / \mathrm{m}_{1}$ on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If $\mathrm{m}_{2} / \mathrm{m}_{1}$ is greater than 1 , the converter will be unstable. Figure 20B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the $\Delta \mathrm{I}$ perturbation will decrease to zero on succeeding cycles. This compensating ramp ( $\mathrm{m}_{3}$ ) must have a slope equal to or slightly greater than $\mathrm{m}_{2} / 2$ for stability. With $\mathrm{m}_{2} / 2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 33).



Figure 23. Adjustable Reduction of Clamp Level


Figure 24. Soft-Start Circuit


Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over-current conditions, a reduction of the $\mathrm{I}_{\mathrm{pk}(\max )}$ clamp level must be implemented. Refer to Figures 23 and 25.

Figure 26. Current Sensing Power MOSFET


The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. Current Waveform Spike Suppression


Series gate resistor $\mathrm{R}_{\mathrm{g}}$ will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 28. MOSFET Parasitic Oscillations


Figure 30. Isolated MOSFET Drive


The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor $\mathrm{C}_{1}$.

Figure 29. Bipolar Transistor Drive


The MCR101 SCR must be selected for a holding of $<0.5 \mathrm{~mA} @ \mathrm{~T}_{\mathrm{A}(\min )}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k .

Figure 31. Latched Shutdown


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor curren


Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 32. Error Amplifier Compensation


Figure 33. Slope Compensation


| Test |  | Conditions |
| :--- | :--- | :---: |

All outputs are at nominal load currents, unless otherwise noted

UC3842B, UC3843B, UC2842B, UC2843B, NCV3843BV

ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: |
| UC384XBD | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| UC384XBDR2 |  | SO-14 | 2500 Tape \& Reel |
| UC384XBD1 |  | SO-8 | 98 Units/Rail |
| UC384XBD1R2 |  | SO-8 | 2500 Tape \& Reel |
| UC384XBN |  | PDIP-8 | 50 Units/Rail |
| UC3842BN1 |  | PDIP-8 | 50 Units/Rail |
| UC284XBD | $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| UC2843BDR2 |  | SO-14 | 2500 Tape \& Reel |
| UC284XBD1 |  | SO-8 | 98 Units/Rail |
| UC284XBD1R2 |  | SO-8 | 2500 Tape \& Reel |
| UC284XBN |  | PDIP-8 | 50 Units/Rail |
| UC3843BVD | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| UC384XBVDR2 |  | SO-14 | 2500 Tape \& Reel |
| UC384XBVD1 |  | SO-8 | 98 Units/Rail |
| UC384XBVD1R2 |  | SO-8 | 2500 Tape \& Reel |
| UC3843BVN |  | PDIP-8 | 50 Units/Rail |
| NCV3843BVDR2 |  | SO-14 | 2500 Tape \& Reel |

X indicates either a 2 or 3 to define specific device part numbers.

MARKING DIAGRAMS


SO-8 D1 SUFFIX CASE 751


SO-14 D SUFFIX CASE 751A




$$
\begin{aligned}
& \mathrm{X} \quad=2 \text { or } 3 \\
& \mathrm{~A} \\
& \mathrm{WL}, \mathrm{~L}=\text { Assembly Location } \\
& \mathrm{YY}, \mathrm{Y}=\text { Yearer Lot } \\
& \mathrm{WW}, \mathrm{~W}=\text { Work Week } \\
& \text { *This marking diagram also applies to NCV3843BV. }
\end{aligned}
$$

## UC3844B, UC3845B, UC2844B, UC2845B

## High Performance Current Mode Controllers

The UC3844B, UC3845B series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, a latch for single pulse metering, and a flip-flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from $50 \%$ to $70 \%$.

These devices are available in an 8 -pin dual-in-line and surface mount (SO-8) plastic package as well as the $14-$ pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX844B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX845B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50\% to 70\%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current


Pin numbers in parenthesis are for the D suffix $\mathrm{SO}-14$ package.


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SO-8 D1 SUFFIX CASE 751

SO-14 D SUFFIX CASE 751A


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1834 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 1835 of this data sheet.

## UC3844B, UC3845B, UC2844B, UC2845B

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Total Power Supply and Zener Current | $\left(\mathrm{I}_{\mathrm{CC}}+\mathrm{I}_{\mathrm{z}}\right.$ ) | 30 | mA |
| Output Current, Source or Sink (Note 1) | 10 | 1.0 | A |
| Output Energy (Capacitive Load per Cycle) | W | 5.0 | $\mu \mathrm{J}$ |
| Current Sense and Voltage Feedback Inputs | $\mathrm{V}_{\text {in }}$ | -0.3 to +5.5 | V |
| Error Amp Output Sink Current | 10 | 10 | mA |
| Power Dissipation and Thermal Characteristics <br> D Suffix, Plastic Package, SO-14 Case 751A <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> D1 Suffix, Plastic Package, SO-8 Case 751 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> N Suffix, Plastic Package, Case 626 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 862 \\ & 145 \\ & \\ & 702 \\ & 178 \\ & \\ & 1.25 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature UC3844B, UC3845B <br> UC2844B, UC2845B | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -25 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$ [Note 2], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

| Characteristic | Symbol | UC284XB |  |  | UC384XB, XBV |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |

REFERENCE SECTION

| Reference Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {ref }}$ | 4.95 | 5.0 | 5.05 | 4.9 | 5.0 | 5.1 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$ to 25 V$)$ | Regline | - | 2.0 | 20 | - | 2.0 | 20 | mV |
| Load Regulation ( $\mathrm{I}_{\mathrm{O}}=1.0 \mathrm{~mA}$ to 20 mA$)$ | Reg $_{\text {load }}$ | - | 3.0 | 25 | - | 3.0 | 25 | mV |
| Temperature Stability | $\mathrm{T}_{\mathrm{S}}$ | - | 0.2 | - | - | 0.2 | - | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Total Output Variation over Line, Load, and Temperature | $\mathrm{V}_{\text {ref }}$ | 4.9 | - | 5.1 | 4.82 | - | 5.18 | V |
| Output Noise Voltage $\left(\mathrm{f}=10 \mathrm{~Hz}\right.$ to $\left.10 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{n}}$ | - | 50 | - | - | 50 | - | $\mu \mathrm{V}$ |
| Long Term Stability $\left(\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}\right.$ for 1000 Hours $)$ | S | - | 5.0 | - | - | 5.0 | - | mV |
| Output Short Circuit Current | I SC | -30 | -85 | -180 | -30 | -85 | -180 | mA |

OSCILLATOR SECTION

| $\begin{aligned} & \text { Frequency } \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C}\left(\mathrm{R}_{\mathrm{T}}=6.2 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=1.0 \mathrm{nF}\right) \end{aligned}$ | fosc | $\begin{gathered} 49 \\ 48 \\ 225 \end{gathered}$ | $\begin{gathered} 52 \\ - \\ 250 \end{gathered}$ | $\begin{gathered} 55 \\ 56 \\ 275 \end{gathered}$ | $\begin{gathered} 49 \\ 48 \\ 225 \end{gathered}$ | $\begin{gathered} 52 \\ - \\ 250 \end{gathered}$ | $\begin{gathered} 55 \\ 56 \\ 275 \end{gathered}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 25 V ) | $\Delta \mathrm{f}_{\mathrm{OSc}} / \Delta \mathrm{V}$ | - | 0.2 | 1.0 | - | 0.2 | 1.0 | \% |
| Frequency Change with Temperature ( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ ) | $\Delta \mathrm{f}_{\text {OSc }} / \Delta \mathrm{T}$ | - | 1.0 | - | - | 0.5 | - | \% |
| Oscillator Voltage Swing (Peak-to-Peak) | V OSC | - | 1.6 | - | - | 1.6 | - | V |
| $\begin{aligned} & \text { Discharge Current }(\mathrm{V} \text { OSC }=2.0 \mathrm{~V}) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\mathrm{UC} 284 \mathrm{XB}, \mathrm{UC} 384 \mathrm{XB}) \\ & \\ & \text { (UC384XBV) } \end{aligned}$ | ${ }_{\text {dischg }}$ | $\begin{aligned} & 7.8 \\ & 7.5 \end{aligned}$ | 8.3 | 8.8 8.8 | 7.8 7.6 7.2 | 8.3 | $\begin{aligned} & 8.8 \\ & 8.8 \\ & 8.8 \end{aligned}$ | mA |

1. Maximum package power dissipation limits must be observed.
2. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

$$
\begin{aligned}
\mathrm{T}_{\text {low }} & =0^{\circ} \mathrm{C} \text { for UC3844B, UC3845B } \\
& =-25^{\circ} \mathrm{C} \text { for UC2844B, UC2845B } \\
& =-40^{\circ} \mathrm{C} \text { for UC3844BV, UC3845BV }
\end{aligned}
$$

$T_{\text {high }}=+70^{\circ} \mathrm{C}$ for UC3844B, UC3845B
$=+85^{\circ} \mathrm{C}$ for UC2844B, UC2845B
$=+105^{\circ} \mathrm{C}$ for UC3844BV, UC3845BV

## UC3844B, UC3845B, UC2844B, UC2845B

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right.$ [Note 4], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 5], unless otherwise noted.)

| Characteristic | Symbol | UC284XB |  |  | UC384XB, XBV |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |

ERROR AMPLIFIER SECTION

| Voltage Feedback Input ( $\mathrm{V}_{\mathrm{O}}=2.5 \mathrm{~V}$ ) | $\mathrm{V}_{\mathrm{FB}}$ | 2.45 | 2.5 | 2.55 | 2.42 | 2.5 | 2.58 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB}}=5.0 \mathrm{~V}$ ) | IB | - | -0.1 | -1.0 | - | -0.1 | -2.0 | $\mu \mathrm{A}$ |
| Open Loop Voltage Gain ( $\mathrm{V}_{\mathrm{O}}=2.0 \mathrm{~V}$ to 4.0 V ) | $A_{\text {VOL }}$ | 65 | 90 | - | 65 | 90 | - | dB |
| Unity Gain Bandwidth ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | BW | 0.7 | 1.0 | - | 0.7 | 1.0 | - | MHz |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ to 25 V ) | PSRR | 60 | 70 | - | 60 | 70 | - | dB |
| $\begin{aligned} & \text { Output Current } \\ & \text { Sink }\left(\mathrm{V}_{\mathrm{O}}=1.1 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right) \\ & \text { Source }\left(\mathrm{V}_{\mathrm{O}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}\right) \end{aligned}$ | $I_{\text {Sink }}$ ISource | $\begin{gathered} 2.0 \\ -0.5 \end{gathered}$ | $\begin{gathered} 12 \\ -1.0 \end{gathered}$ |  | $\begin{gathered} 2.0 \\ -0.5 \end{gathered}$ | $\begin{gathered} 12 \\ -1.0 \end{gathered}$ |  | mA |
| Output Voltage Swing <br> High State ( $\mathrm{R}_{\mathrm{L}}=15 \mathrm{k}$ to ground, $\mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) <br> Low State ( $R_{L}=15 \mathrm{k}$ to $\mathrm{V}_{\text {ref }}, \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) <br> (UC284XB, UC384XB) <br> (UC384XBV) | $\mathrm{V}_{\mathrm{OH}}$ <br> $\mathrm{V}_{\mathrm{OL}}$ | 5.0 | 6.2 0.8 | - 1.1 | 5.0 | $\begin{aligned} & 6.2 \\ & 0.8 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & 1.1 \\ & 1.2 \end{aligned}$ | V |

## CURRENT SENSE SECTION

| Current Sense Input Voltage Gain (Notes 6 \& 7) <br> (UC284XB, UC384XB) <br> (UC384XBV) | $\mathrm{A}_{\mathrm{V}}$ | 2.85 | 3.0 | 3.15 | 2.85 | 3.0 | 3.15 | $\mathrm{~V} / \mathrm{V}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum Current Sense Input Threshold (Note 6) <br> (UC284XB, UC384XB) <br> (UC384XBV) | $\mathrm{V}_{\text {th }}$ | - | - | - | 2.85 | 3.0 | 3.25 |  |
| Power Supply Rejection Ratio <br> (VCC $=12$ V to 25 V) (Note 6) |  | 0.9 | 1.0 | 1.1 | 0.9 | 1.0 | 1.1 | V |
| Input Bias Current | PSRR | - | 70 | - | - | 70 | - | dB |
| Propagation Delay (Current Sense Input to Output) |  |  |  |  |  |  |  |  |

## OUTPUT SECTION

| Output Voltage | $\mathrm{V}_{\text {OL }}$ |  |  |  |  |  |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Low State ( $\left.I_{\text {Sink }}=20 \mathrm{~mA}\right)$ |  | - | 0.1 | 0.4 | - | 0.1 | 0.4 |  |
| ( $\mathrm{I}_{\text {Sink }}=200 \mathrm{~mA}, \mathrm{UC} 284 \mathrm{XB}, \mathrm{UC384XB}$ ) |  | - | 1.6 | 2.2 | - | 1.6 | 2.2 |  |
| ( link $^{\text {a }}$ = $200 \mathrm{~mA}, \mathrm{UC} 384 \mathrm{XBV}$ ) |  | - | - | - | - | 1.6 | 2.3 |  |
| High State ( ${ }_{\text {Source }}=20 \mathrm{~mA}$, UC284XB, UC384XB) | $\mathrm{V}_{\mathrm{OH}}$ | 13 | 13.5 | - | 13 | 13.5 | - |  |
| ( ISource $=20 \mathrm{~mA}, \mathrm{UC} 384 \mathrm{XBV}$ ) |  | - | - | - | 12.9 | - | - |  |
| ( S $_{\text {source }}=200 \mathrm{~mA}$ ) |  | 12 | 13.4 | - | 12 | 13.4 | - |  |
| Output Voltage with UVLO Activated ( $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$, $\mathrm{I}_{\text {Sink }}=1.0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {OL(UVLO) }}$ | - | 0.1 | 1.1 | - | 0.1 | 1.1 | V |
| Output Voltage Rise Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $t_{r}$ | - | 50 | 150 | - | 50 | 150 | ns |
| Output Voltage Fall Time ( $\left.\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\mathrm{f}}$ | - | 50 | 150 | - | 50 | 150 | ns |

UNDERVOLTAGE LOCKOUT SECTION

| Startup Threshold | $V_{\text {th }}$ |  |  |  |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UCX844B, BV |  | 15 | 16 | 17 | 14.5 | 16 | 17.5 |  |
| UCX845B, BV |  | 7.8 | 8.4 | 9.0 | 7.8 | 8.4 | 9.0 |  |
| Minimum Operating Voltage After Turn-On | $V_{\text {CC(min })}$ |  |  |  |  |  |  | V |
| UCX844B, BV |  | 9.0 | 10 | 11 | 8.5 | 10 | 11.5 |  |
| UCX845B, BV |  | 7.0 | 7.6 | 8.2 | 7.0 | 7.6 | 8.2 |  |

4. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

$$
\begin{aligned}
\mathrm{T}_{\text {low }} & =0^{\circ} \mathrm{C} \text { for UC3844B, UC3845B } & \mathrm{T}_{\text {high }} & =+70^{\circ} \mathrm{C} \text { for UC3844B, UC3845B } \\
& =-25^{\circ} \mathrm{C} \text { for UC2844B, UC2845B } & & =+85^{\circ} \mathrm{C} \text { for UC2844B, UC2845B } \\
& =-40^{\circ} \mathrm{C} \text { for UC3844BV, UC3845BV } & & =+105^{\circ} \mathrm{C} \text { for UC3844BV, UC3845BV }
\end{aligned}
$$

6. This parameter is measured at the latch trip point with $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$.
7. Comparator gain is defined as: $A_{V}=\Delta V$ Output/Compensation
$\Delta \mathrm{V}$ Current Sense Input

## UC3844B, UC3845B, UC2844B, UC2845B

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$ [Note 8], $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $T_{A}$ is the operating ambient temperature range that applies [Note 9], unless otherwise noted.)

| Characteristic | Symbol | UC284XB |  |  | UC384XB, XBV |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |

PWM SECTION

| ```Duty Cycle Maximum (UC284XB, UC384XB) (UC384XBV) Minimum``` | $\begin{aligned} & \mathrm{DC}_{(\text {max })} \\ & \\ & \mathrm{DC}_{(\text {min })} \end{aligned}$ | 47 | 48 | 50 - 0 | 47 46 | 48 48 | 50 50 0 | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

TOTAL DEVICE

| Power Supply Current <br> Startup ( $\mathrm{V}_{\mathrm{CC}}=6.5 \mathrm{~V}$ for UCX845B, 14 V for UCX844B, BV) Operating (Note 8) | $\mathrm{I}_{\mathrm{CC}}$ | - - | $\begin{aligned} & 0.3 \\ & 12 \end{aligned}$ | $\begin{gathered} 0.5 \\ 17 \end{gathered}$ | - | 0.3 12 | $\begin{gathered} 0.5 \\ 17 \end{gathered}$ | mA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply Zener Voltage ( $\mathrm{I}_{\mathrm{CC}}=25 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{Z}}$ | 30 | 36 | - | 30 | 36 | - | V |

8. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 15 V .
9. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for UC3844B, UC3845B $\quad T_{\text {high }}=+70^{\circ} \mathrm{C}$ for UC3844B, UC3845B
$=-25^{\circ} \mathrm{C}$ for UC2844B, UC2845B
$=+85^{\circ} \mathrm{C}$ for UC2844B, UC2845B
$=-40^{\circ} \mathrm{C}$ for UC3844BV, UC3845BV
$=+105^{\circ} \mathrm{C}$ for UC3844BV, UC3845BV


Figure 2. Timing Resistor versus Oscillator Frequency


Figure 4. Error Amp Small Signal Transient Response


Figure 3. Output Deadtime versus Oscillator Frequency


Figure 5. Error Amp Large Signal Transient Response

UC3844B, UC3845B, UC2844B, UC2845B


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency


Figure 8. Reference Voltage Change versus Source Current


Figure 10. Reference Load Regulation


Figure 7. Current Sense Input Threshold versus Error Amp Output Voltage


Figure 9. Reference Short Circuit Current versus Temperature


Figure 11. Reference Line Regulation


Figure 12. Output Saturation Voltage versus Load Current


Figure 14. Output Cross Conduction


Figure 13. Output Waveform


Figure 15. Supply Current versus Supply Voltage

## UC3844B, UC3845B, UC2844B, UC2845B

PIN FUNCTION DESCRIPTION

| Pin |  | Function | Description |
| :---: | :---: | :---: | :---: |
| 8-Pin | 14-Pin |  |  |
| 1 | 1 | Compensation | This pin is the Error Amplifier output and is made available for loop compensation. |
| 2 | 3 | Voltage Feedback | This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider. |
| 3 | 5 | Current Sense | A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction. |
| 4 | 7 | $\mathrm{R}_{T} / \mathrm{C}_{T}$ | The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor $\mathrm{R}_{\mathrm{T}}$ to $\mathrm{V}_{\text {ref }}$ and capacitor $\mathrm{C}_{\mathrm{T}}$ to ground. Oscillator operation to 1.0 kHz is possible. |
| 5 |  | Gnd | This pin is the combined control circuitry and power ground. |
| 6 | 10 | Output | This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency. |
| 7 | 12 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the control IC. |
| 8 | 14 | $\mathrm{V}_{\text {ref }}$ | This is the reference output. It provides charging current for capacitor $\mathrm{C}_{\boldsymbol{T}}$ through resistor $\mathrm{R}_{\mathrm{T}}$. |
|  | 8 | Power Ground | This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry. |
|  | 11 | $\mathrm{V}_{\mathrm{c}}$ | The Output high state $\left(\mathrm{V}_{\mathrm{OH}}\right)$ is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry |
|  | 9 | Gnd | This pin is the control circuitry ground return and is connected back to the power source ground. |
|  | 2,4,6,13 | NC | No connection. These pins are not internally connected. |

The UC3844B, UC3845B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost-effective solution with minimal external components. A representative block diagram is shown in Figure 16.

## Oscillator

The oscillator frequency is programmed by the values selected for the timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged from the 5.0 V reference through resistor $\mathrm{R}_{\mathrm{T}}$ to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of $\mathrm{C}_{\mathrm{T}}$, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip-flop has been incorporated in the UCX844/5B which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the $\mathrm{C}_{\mathrm{T}}$ discharge period yields output deadtimes programmable from $50 \%$ to $70 \%$. Figure 2 shows $\mathrm{R}_{\mathrm{T}}$ versus Oscillator Frequency and Figure 3, Output Deadtime versus Frequency, both for given values of $\mathrm{C}_{\mathrm{T}}$. Note that many values of $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$ will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within $\pm 6 \%$ at 50 kHz . Also, because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within $\pm 10 \%$ at 250 kHz .

In many noise-sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 18. For reliable locking, the free-running oscillator frequency should be set about $10 \%$ less than the clock frequency. A method for multi-unit synchronization is shown in Figure 19. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than $70 \%$.

## Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB , and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 6). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is $-2.0 \mu \mathrm{~A}$ which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 29). The output voltage is offset by two diode drops ( $\approx 1.4 \mathrm{~V}$ ) and divided by three before it connects to the inverting input of the Current Sense

Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state ( $\mathrm{V}_{\mathrm{OL}}$ ). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 21, 22). The Error Amp minimum feedback resistance is limited by the amplifier's source current $(0.5 \mathrm{~mA})$ and the required output voltage $\left(\mathrm{V}_{\mathrm{OH}}\right)$ to reach the comparator's 1.0 V clamp level:

$$
\mathrm{R}_{\mathrm{f}(\min )} \approx \frac{3.0(1.0 \mathrm{~V})+1.4 \mathrm{~V}}{0.5 \mathrm{~mA}}=8800 \Omega
$$

## Current Sense Comparator and PWM Latch

The UC3844B, UC3845B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$
I_{\mathrm{pk}}=\frac{\mathrm{V}_{(\operatorname{Pin} 1)}-1.4 \mathrm{~V}}{3 \mathrm{R}_{\mathrm{S}}}
$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V . Therefore the maximum peak switch current is:

$$
\mathrm{I}_{\mathrm{pk}(\max )}=\frac{1.0 \mathrm{~V}}{\mathrm{R}_{\mathrm{S}}}
$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of $\mathrm{R}_{\mathrm{S}}$ to a reasonable level. A simple method to adjust this voltage is shown in Figure 20. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $\mathrm{I}_{\mathrm{pk}(\max )}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 24).

## UC3844B, UC3845B, UC2844B, UC2845B



Figure 16. Representative Block Diagram

Capacitor $\mathrm{C}_{\mathrm{T}}$


Output


Large $\mathrm{R}_{\mathrm{T}} /$ Small $\mathrm{C}_{\mathrm{T}}$


Small $R_{T} /$ Large $\mathrm{C}_{\mathrm{T}}$

Figure 17. Timing Diagram

## Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal $\left(\mathrm{V}_{\mathrm{CC}}\right)$ and the reference output $\left(\mathrm{V}_{\text {ref }}\right)$ are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The $\mathrm{V}_{\mathrm{CC}}$ comparator upper and lower thresholds are $16 \mathrm{~V} / 10 \mathrm{~V}$ for the UCX844B, and $8.4 \mathrm{~V} / 7.6 \mathrm{~V}$ for the UCX845B. The $\mathrm{V}_{\text {ref }}$ comparator upper and lower thresholds are $3.6 \mathrm{~V} / 3.4 \mathrm{~V}$. The large hysteresis and low startup current of the UCX844B makes it ideally suited in off-line converter applications where efficient bootstrap startup techniques are required (Figure 30). The UCX845B is intended for lower voltage dc-to-dc converter applications. A 36 V zener is connected as a shunt regulator from $\mathrm{V}_{\mathrm{CC}}$ to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX844B is 11 V and 8.2 V for the UCX845B.

## Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to $\pm 1.0$ A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for $\mathrm{V}_{\mathrm{C}}$ (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $\mathrm{I}_{\mathrm{pk}(\max )}$ clamp level. The separate $\mathrm{V}_{\mathrm{C}}$ supply input allows the
designer added flexibility in tailoring the drive voltage independent of $\mathrm{V}_{\mathrm{CC}}$. A zener clamp is typically connected to this input when driving power MOSFETs in systems where $\mathrm{V}_{\mathrm{CC}}$ is greater than 20 V . Figure 23 shows proper power and control ground connections in a current-sensing power MOSFET application.

## Reference

The 5.0 V bandgap reference is trimmed to $\pm 1.0 \%$ tolerance at $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ on the UC284XB, and $\pm 2.0 \%$ on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short-circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

## Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors $(0.1 \mu \mathrm{~F})$ connected directly to $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}$, and $\mathrm{V}_{\text {ref }}$ may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise-generating components.


The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of $\mathrm{C}_{\boldsymbol{T}}$ to go more than 300 mV below ground.

Figure 18. External Clock Synchronization


Figure 19. External Duty Cycle Clamp and Multi-Unit Synchronization


Figure 20. Adjustable Reduction of Clamp Level

Figure 22. Adjustable Buffered Reduction of Clamp Level with Soft-Start



Figure 21. Soft-Start Circuit


Figure 23. Current Sensing Power MOSFET


Figure 24. Current Waveform Spike Suppression


Series gate resistor $R_{g}$ will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 25. MOSFET Parasitic Oscillations


The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor $\mathrm{C}_{1}$.

Figure 26. Bipolar Transistor Drive


Figure 27. Isolated MOSFET Drive


The MCR101 SCR must be selected for a holding of $<0.5 \mathrm{~mA} @ \mathrm{~T}_{\mathrm{A}(\text { min) })}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k .

Figure 28. Latched Shutdown


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.


Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 29. Error Amplifier Compensation

## UC3844B, UC3845B, UC2844B, UC2845B



Figure 30.7 W Off-Line Flyback Regulator

| Test | Conditions | Results |
| :---: | :---: | :---: |
| Line Regulation: $\begin{aligned} & 5.0 \mathrm{~V} \\ & \pm 12 \mathrm{~V}\end{aligned}$ | $\mathrm{V}_{\text {in }}=95 \mathrm{Vac}$ to 130 Vac | $\begin{aligned} & \Delta=50 \mathrm{mV} \text { or } \pm 0.5 \% \\ & \Delta=24 \mathrm{mV} \text { or } \pm 0.1 \% \end{aligned}$ |
| Load Regulation: $\begin{aligned} 5.0 \mathrm{~V} \\ \pm 12 \mathrm{~V}\end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\text {out }}=1.0 \mathrm{~A} \text { to } 4.0 \mathrm{~A} \\ & \mathrm{~V}_{\text {in }}=115 \mathrm{Vac}, \mathrm{I}_{\text {out }}=100 \mathrm{~mA} \text { to } 300 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & \Delta=300 \mathrm{mV} \text { or } \pm 3.0 \% \\ & \Delta=60 \mathrm{mV} \text { or } \pm 0.25 \% \end{aligned}$ |
| $\begin{array}{ll} \text { Output Ripple: } & 5.0 \mathrm{~V} \\ & \pm 12 \mathrm{~V} \end{array}$ | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}$ | $\begin{aligned} & 40 \mathrm{mV}_{\mathrm{pp}} \\ & 80 \mathrm{mV}_{\mathrm{pp}} \end{aligned}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=115 \mathrm{Vac}$ | 70\% |

All outputs are at nominal load currents unless otherwise noted.

## UC3844B, UC3845B, UC2844B, UC2845B



The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A . An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Step-Up Charge Pump Converter


The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A .
An additional series resistor may be required when using tantalum or other low ESR capacitors.
Figure 32. Voltage-Inverting Charge Pump Converter

UC3844B, UC3845B, UC2844B, UC2845B

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: |
| UC384XBD | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| UC384XBDR2 |  | SO-14 | 2500 Tape \& Reel |
| UC384XBD1 |  | SO-8 | 98 Units/Rail |
| UC384XBD1R2 |  | SO-8 | 2500 Tape \& Reel |
| UC384XBN |  | PDIP-8 | 50 Units/Rail |
| UC2845BD | $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| UC284XBDR2 |  | SO-14 | 2500 Tape \& Reel |
| UC2845BD1 |  | SO-8 | 98 Units/Rail |
| UC284XBD1R2 |  | SO-8 | 2500 Tape \& Reel |
| UC2844BN |  | PDIP-8 | 50 Units/Rail |
| UC384XBVD | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | SO-14 | 55 Units/Rail |
| UC3844BVDR2 |  | SO-14 | 2500 Tape \& Reel |
| UC384XBVD1 |  | SO-8 | 98 Units/Rail |
| UC384XBVD1R2 |  | SO-8 | 2500 Tape \& Reel |
| UC384XBVN |  | PDIP-8 | 50 Units/Rail |

X indicates either a 4 or 5 to define specific device part numbers.

## UC3844B, UC3845B, UC2844B, UC2845B

MARKING DIAGRAMS


SO-8 D1 SUFFIX CASE 751


## SO-14 D SUFFIX CASE 751A



| $\begin{aligned} & 14 \\ & \text { H—月 } \end{aligned}$ |
| :---: |
| UC384xBVD |
| - AWLYWW |
|  |


|  |
| :---: |
| UC284xBD |
| - AWLYWW |
|  |

$$
\begin{array}{ll}
\mathrm{X} & =4 \text { or } 5 \\
\mathrm{~F} & =\text { Wafer Fab } \\
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, } & \text { W }
\end{array}
$$

## CS2841B

## Automotive Current Mode PWM Control Circuit

The CS2841B provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS2841B (a variation of the CS2843A) is designed specifically for use in automotive operation. The low start threshold voltage of 8.0 V (typ), and the ability to survive 40 V automotive load dump transients are important for automotive subsystem designs. The CS2841 series has a history of quality and reliability in automotive applications.

The CS2841B incorporates a precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. Duty-cycles greater than $50 \%$ are also possible. On board logic ensures that $\mathrm{V}_{\mathrm{REF}}$ is stabilized before the output stage is enabled. Ion implant resistors provide tighter control of undervoltage lockout.

## Features

- Optimized for Off-Line Control
- Internally Trimmed Temperature Compensated Oscillator
- Maximum Duty-Cycle Clamp
- $\mathrm{V}_{\text {REF }}$ Stabilized Before Output Stage Enabled
- Low Start-Up Current
- Pulse-By-Pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1.0 \% Trimmed Bandgap Reference
- High Current Totem Pole Output

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## PIN CONNECTIONS AND MARKING DIAGRAM



A $=$ Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS2841BEN8 | DIP-8 | 50 Units/Rail |
| CS2841BED14 | SO-14 | 55 Units/Rail |
| CS2841BEDR14 | SO-14 | 2500 Tape \& Reel |



Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Supply Voltage (Low Impedance Source) | 40 | V |
| Output Current | $\pm 1.0$ | A |
| Output Energy (Capacitive Load) | 5.0 | $\mu \mathrm{~J}$ |
| Analog Inputs (VB, Sense) | -0.3 to 5.5 | V |
| Error Amp Output Sink Current |  | 10 |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{T}}=680 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=0.022 \mu \mathrm{~F}\right.$ for Triangular Mode, $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$ (Note 3), $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$ for Sawtooth Mode (see Figure 7); unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Reference Section |  |  |  |  |  |
| Output Voltage | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$, $\mathrm{l}_{\text {OUT }}=1.0 \mathrm{~mA}$ | 4.9 | 5.0 | 5.1 | V |
| Line Regulation | $8.4 \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | - | 6.0 | 20 | mV |
| Load Regulation | $1.0 \leq \mathrm{l}_{\text {OUT }} \leq 20 \mathrm{~mA}$ | - | 6.0 | 25 | mV |
| Temperature Stability | Note 4 | - | 0.2 | 0.4 | $\mathrm{mV} /{ }^{\circ} \mathrm{C}$ |
| Total Output Variation | Line, Load, Temp. Note 4 | 4.82 | - | 5.18 | V |
| Output Noise Voltage | $10 \mathrm{~Hz} \leq \mathrm{f} \leq 10 \mathrm{kHz}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$. Note 4 | - | 50 | - | $\mu \mathrm{V}$ |
| Long Term Stability | $\mathrm{T}_{\mathrm{A}}=125^{\circ} \mathrm{C}, 1000 \mathrm{Hrs}$. Note 4 | - | 5.0 | 25 | mV |
| Output Short Circuit | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | -30 | -100 | -180 | mA |

Oscillator Section

| Initial Accuracy | Sawtooth Mode: $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$. See Figure 7. <br> Sawtooth Mode: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ <br> Triangular Mode: $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$. See Figure 7 . | $\begin{aligned} & 47 \\ & 44 \\ & 44 \end{aligned}$ | $\begin{aligned} & 52 \\ & 52 \\ & 52 \end{aligned}$ | $\begin{aligned} & 57 \\ & 60 \\ & 60 \end{aligned}$ | $\begin{aligned} & \mathrm{kHz} \\ & \mathrm{kHz} \\ & \mathrm{kHz} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Voltage Stability | $8.4 \leq \mathrm{V}_{\text {CC }} \leq 16 \mathrm{~V}$ | - | 0.2 | 1.0 | \% |
| Temperature Stability | Sawtooth Mode: $\mathrm{T}_{\text {MIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {MAX }}$. Note 4 Triangular Mode: $\mathrm{T}_{\text {MIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {MAX }}$. Note 4 |  | $\begin{aligned} & 5.0 \\ & 8.0 \end{aligned}$ |  | $\begin{aligned} & \% \\ & \% \end{aligned}$ |
| Amplitude | $\mathrm{V}_{\text {OsC }}$ (Peak to Peak) | - | 1.7 | - | V |
| Discharge Current | $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{MIN}} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{MAX}} \end{aligned}$ | $\begin{aligned} & 7.4 \\ & 7.2 \end{aligned}$ | 8.3 | $\begin{aligned} & 9.2 \\ & 9.4 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

Error Amp Section

| Input Voltage | $\mathrm{V}_{\mathrm{COMP}}=2.5 \mathrm{~V}$ | 2.42 | 2.5 | 2.58 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | -0.3 | -2.0 | $\mu \mathrm{~A}$ |
| AVOL | $2.0 \leq \mathrm{V}_{\mathrm{OUT}} \leq 4.0 \mathrm{~V}$ | 65 | 90 | - | dB |
| Unity Gain Bandwidth | Note 4 | 0.7 | 1.0 | - | MHz |
| PSRR | $8.4 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | 60 | 70 | - | dB |
| Output Sink Current | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{COMP}}=1.1 \mathrm{~V}$ | 2.0 | 6.0 | - | mA |
| Output Source Current | $\mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{COMP}}=5.0 \mathrm{~V}$ | -0.5 | -0.8 | - | mA |
| $\mathrm{V}_{\text {Out }}$ High | $\mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=15 \mathrm{k} \Omega$ to Ground | 5.0 | 6.0 | - | V |
| $\mathrm{V}_{\text {OUT }}$ Low | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=15 \mathrm{k} \Omega$ to $\mathrm{V}_{\text {REF }}$ | - | 0.7 | 1.1 | V |

Current Sense Section

| Gain | Notes 5 and 6 | 2.85 | 3.0 | 3.15 | $\mathrm{~V} / \mathrm{V}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Maximum Input Signal | $\mathrm{V}_{\mathrm{COMP}}=5.0 \mathrm{~V}$. Note 5 | 0.9 | 1.0 | 1.1 | V |
| PSRR | $12 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 25 \mathrm{~V}$. Note 5 | - | 70 | - | dB |
| Input Bias Current | $\mathrm{V}_{\text {Sense }}=0 \mathrm{~V}$ | - | -2.0 | -10 | $\mu \mathrm{~A}$ |
| Delay to Output | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$. Note 4 | - | 150 | 300 | ns |

3. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start threshold before setting at 15 V .
4. These parameters, although guaranteed, are not $100 \%$ tested in production.
5. Parameter measured at trip point of latch with $\mathrm{V}_{\mathrm{FB}}=0$.
6. Gain defined as:

$$
\mathrm{A}=\frac{\Delta \mathrm{V}_{\text {COMP }}}{\Delta \mathrm{V}_{\text {Sense }}} ; 0 \leq \mathrm{V}_{\text {Sense }} \leq 0.8 \mathrm{~V}
$$

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{T}}=680 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=0.022 \mu \mathrm{~F}\right.$ for Triangular Mode, $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$ (Note 3), $\mathrm{R}_{\mathrm{T}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$ for Sawtooth Mode (see Figure 7); unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Section |  |  |  |  |  |
| Output Low Level | $\begin{aligned} & \mathrm{I}_{\mathrm{SINK}}=20 \mathrm{~mA} \\ & \mathrm{I}_{\mathrm{SINK}}=200 \mathrm{~mA} \end{aligned}$ | - | $\begin{aligned} & 0.1 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 0.4 \\ & 2.2 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Output High Level | $\begin{aligned} & I_{\text {SOURCE }}=20 \mathrm{~mA} \\ & I_{\text {SOURCE }}=200 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 13 \\ & 12 \end{aligned}$ | $\begin{aligned} & 13.5 \\ & 13.5 \end{aligned}$ | - | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Rise Time | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$. Note 7 | - | 50 | 150 | ns |
| Fall Time | $\mathrm{T}_{J}=25^{\circ} \mathrm{C}, \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$. Note 7 | - | 50 | 150 | ns |
| Output Leakage | Undervoltage Active, $\mathrm{V}_{\text {OUT }}=0$ | - | -0.01 | -10 | $\mu \mathrm{A}$ |

Total Standby Current

| Start-Up Current | - | - | 0.5 | 1.0 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Operating Supply Current $\mathrm{I}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\text {Sense }}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=3.3 \mathrm{nF}$ | - | 11 | 17 | mA |

Undervoltage Lockout Section

| Start Threshold | - | 7.6 | 8.0 | 8.4 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Min. Operating Voltage | After Turn On | 7.0 | 7.4 | 7.8 | V |

7. These parameters, although guaranteed, are not $100 \%$ tested in production.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| DIP-8 | SO-14 |  |  |
| 1 | 1 | COMP | Error amp output, used to compensate error amplifier. |
| 2 | 3 | $V_{\text {FB }}$ | Error amp inverting input. |
| 3 | 5 | Sense | Noninverting input to Current Sense Comparator. |
| 4 | 7 | OSC | Oscillator timing network with Capacitor to Ground, resistor to $\mathrm{V}_{\text {REF }}$. |
| 5 | 8 | GND | Ground. |
|  | 9 | Pwr GND | Output driver Ground. |
| 6 | 10 | $\mathrm{V}_{\text {OUT }}$ | Output drive pin. |
|  | 11 | $\mathrm{V}_{\mathrm{CC}}$ Pwr | Output driver positive supply. |
| 7 | 12 | $\mathrm{V}_{\mathrm{CC}}$ | Positive power supply. |
| 8 | 14 | $\mathrm{V}_{\text {REF }}$ | Output of 5.0 V internal reference. |
|  | 2, 4, 6, 13 | NC | No connection. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Oscillator Frequency vs. $\mathbf{C}_{\mathbf{T}}$


Figure 3. Oscillator Duty Cycle vs. $\mathbf{R}_{\mathbf{T}}$


Figure 4. Test Circuit

## CIRCUIT DESCRIPTION

## Undervoltage Lockout

During Undervoltage Lockout (Figure 5), the output driver is biased to a high impedance state. The output should be shunted to ground with a resistor to prevent output leakage current from activating the power switch.


Figure 5. Typical Undervoltage Characteristics

## PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 6). An increase in $\mathrm{V}_{\mathrm{CC}}$ causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.


Figure 6. Timing Diagram for Key CS2841B Parameters

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.


Timing Parameters


## Sawtooth Mode



## Triangular Mode



Figure 7. Oscillator Timing Network and Parameters

## Setting the Oscillator

Oscillator timing capacitor, $\mathrm{C}_{\mathrm{T}}$, is charged by $\mathrm{V}_{\mathrm{REF}}$ through $\mathrm{R}_{\mathrm{T}}$ and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the Low state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:

$$
\begin{gathered}
t_{\mathrm{C}}=R_{T} C T \ln \left(\frac{V_{\text {REF }}-V_{\text {lower }}}{V_{\text {REF }}-V_{\text {upper }}}\right) \\
t_{d}=R_{T} C T \ln \left(\frac{V_{\text {REF }}-I_{d} R T-V_{\text {lower }}}{V_{\text {REF }}-I_{d} R T-V_{\text {upper }}}\right)
\end{gathered}
$$

Substituting in typical values for the parameters in the above formulas:
$\mathrm{V}_{\text {REF }}=5.0 \mathrm{~V}$
$\mathrm{V}_{\text {upper }}=2.7 \mathrm{~V}$
$V_{\text {lower }}=1.0 \mathrm{~V}$
$\mathrm{I}_{\mathrm{d}}=8.3 \mathrm{~mA}$
$\mathrm{t}_{\mathrm{C}} \approx 0.5534 \mathrm{R}_{\mathrm{T}} \mathrm{C} T$

The frequency and maximum duty cycle can be determined from the Typical Performance Characteristic graphs.

## Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to GND pin in a single point ground.

The transistor and $5.0 \mathrm{k} \Omega$ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

$$
t_{d}=R_{T} C_{T} \ln \left(\frac{2.3-0.0083 R_{T}}{4.0-0.0083 R_{T}}\right)
$$



Figure 8. Flyback Application


Figure 9. Boost Application

PACKAGE THERMAL DATA

| Parameter |  | DIP-8 | SO-14 | Unit |
| :--- | ---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 52 | 30 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 100 | 125 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5124, CS5126

## High Performance, Integrated Current Mode PWM Controllers

The CS5124/6 is a fixed frequency current mode controller designed specifically for DC-DC converters found in the telecommunications industry. The CS5124/6 integrates many commonly required current mode power supply features and allows the power supply designer to realize substantial cost and board space savings. The product matrix is as follows:

CS5124: 400 kHz w/VBIAS Pin, 195 mV first current sense threshold.
CS5126: 200 kHz w/SYNC Pin, 335 mV first current sense threshold.
The CS5124/6 integrates the following features: Internal Oscillator, Slope Compensation, Sleep On/Off, Undervoltage Lock Out, Thermal Shutdown, Soft Start Timer, Low Voltage Current Sense for Resistive Sensing, Second Current Threshold for Pulse by Pulse Over Current Protection, a Direct Optocoupler Interface and Leading Edge Current Blanking.

The CS5124/6 has supply range of 7.7 V to 20 V and is available in 8 pin SO narrow package.

## Features

- Line UVLO Monitoring
- Low Current Sense Voltage for Resistive Current Sensing
- External Synchronization to Higher or Lower Frequency Oscillator (CS5126 Only)
- Bias for Start Up Circuitry (CS5124 Only)
- Thermal Shutdown
- Sleep On/Off Pin
- Soft Start Timer
- Leading Edge Blanking
- Direct Optocoupler Interface
- 90 ns Propagation Delay
- 35 ns Driver Rise and Fall Times
- Sleep Mode

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http://onsemi.com


SO-8
D SUFFIX
CASE 751

## PIN CONNECTIONS AND MARKING DIAGRAM



$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5124XD8 | SO-8 | 95 Units/Rail |
| CS5124XDR8 | SO-8 | 2500 Tape \& Reel |
| CS5126XD8 | SO-8 | 95 Units/Rail |
| CS5126XDR8 | SO-8 | 2500 Tape \& Reel |



Figure 1. Application Diagram

MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | -40 to 135 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering: |  | 2.0 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| PIN NAME | PIN SYMBOL | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ Power Input | $\mathrm{V}_{\mathrm{CC}}$ | 20 V | -0.3 V | 1.0 mA | 1.5 A Peak 200 mA DC |
| Clock Synchronization Input | SYNC (CS5126) | 20 V | -0.3 V | 1.0 mA | 1.0 mA |
| $V_{\text {CC }}$ Clamp Output | $\mathrm{V}_{\text {BIAS }}$ (CS5124) | 20 V | -0.3 V | 1.0 mA | 1.0 mA |
| UVLO Shutdown Input | UVLO | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Soft Start Capacitor Input | SS | 6.0 V | -0.3 V | 1.0 mA | 2.0 mA |
| Voltage Feedback Input | $V_{F B}$ | 6.0 V | -0.3 V | 3.0 mA | 20 mA |
| Current Sense Input | $I_{\text {SENSE }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Ground | GROUND | 0 V | 0 V | 1.5 A peak 200 mA DC | 1.0 mA |
| Gate Drive Output | GATE | 20 V | -0.3 V | 1.5 A peak 200 mA DC | 1.5 A peak 200 mA DC |

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}, 7.60 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 20 \mathrm{~V}\right.$, UVLO $=3.0 \mathrm{~V}$, $I_{\text {SENSE }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{V}(\mathrm{CC})}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{GATE}}=1.0 \mathrm{nF}(\mathrm{ESR}=10 \Omega) ; \mathrm{C}_{\mathrm{SS}}=470 \mathrm{pF} ; \mathrm{C}_{\mathrm{V}(\mathrm{FB})}=100 \mathrm{pF}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| General |  |  |  |  |  |
| $\mathrm{I}_{\text {CC }}$ Operating - $\mathrm{V}_{\text {GATE }}$ not switching | - | - | 10 | 13 | mA |
| $\mathrm{I}_{\text {CC }}$ at $\mathrm{V}_{\text {CC }}$ Low | $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$ | - | 500 | 750 | $\mu \mathrm{A}$ |
| Icc Sleep | $\mathrm{V}_{\mathrm{UVL}}=1.0 \mathrm{~V}$ | - | 210 | 275 | $\mu \mathrm{A}$ |

Low $\mathrm{V}_{\mathrm{CC}}$ Lockout

| $V_{\text {CC }}$ Turn-on Threshold Voltage | - | 7.2 | 7.7 | 8.3 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\text {CC }}$ Turn-off Threshold Voltage | - | 6.8 | 7.3 | 7.8 | V |
| $\mathrm{~V}_{\text {CC }}$ Hysteresis | - | 350 | 425 | 500 | mV |

UVLO

| Sleep Threshold Voltage | UVLO decreasing | 1.5 | 1.8 | 2.3 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Sleep Threshold Voltage | UVLO increasing | - | 1.88 | 2.45 | V |
| Sleep Hysteresis |  | - | 35 | 85 | 150 |
| UVLO Turn-off Threshold Voltage | Note 2 | 2.3 | 2.45 | 2.6 | V |
| UVLO Turn-on Threshold Voltage | Note 2 | 2.50 | 2.63 | 2.76 | V |
| UVLO Hysteresis | Turn-on - Turn-off $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 100^{\circ} \mathrm{C}\right)$ Note 2 | 170 | 185 | 200 | mV |
| UVLO Hysteresis | Turn-on - Turn-off $\left(100^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}\right)$ Note 2 | 50 | 185 | 400 | mV |
| UVLO Input Bias Current | - | -1.0 | - | 1.0 | $\mu \mathrm{~A}$ |
| UVLO Clamp | With UVLO sinking 1.0 mA | 5.0 | 7.5 | 12 | V |


| lamp and BIAS Pin $\quad$ CS5124 Only. Connect an NFET as follows: $\mathrm{BIAS}=\mathrm{G}, \mathrm{V}_{\mathrm{CC}}=\mathrm{S}, \mathrm{V}_{\mathrm{IN}}=\mathrm{D}$. |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ Clamp Voltage | $\begin{aligned} & 36 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 60 \mathrm{~V}, 200 \mathrm{nF} \leq \mathrm{C}_{\mathrm{SS}} \leq 500 \mathrm{nF}, \\ & \mathrm{R}=500 \mathrm{k} \end{aligned}$ | 7.275 | 7.9 | 8.625 | V |
| BIAS Minimum Voltage | Measure Voltage on BIAS with: $10 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 20 \mathrm{~V} \& 50 \mu \mathrm{~A} \leq \mathrm{I}_{\mathrm{BIAS}} \leq 1.0 \mathrm{~mA}$ | 1.6 | 2.8 | 4.0 | V |
| BIAS Clamp | With BIAS pin sinking 1.0 mA | 12 | 15 | 20 | V |
| 200 kHz Oscillator | CS5126 Only |  |  |  |  |
| Operating Frequency | - | 175 | 200 | 225 | kHz |
| Max Duty Cycle Clamp | - | 78 | 82.5 | 85 | \% |
| Slope Compensation (Normal operation) | - | 12 | 18 | 23 | $\mathrm{mV} / \mu \mathrm{s}$ |
| Slope Compensation (Synchronized operation) | Note 2 | 7.0 | 12 | 16 | $\mathrm{mV} / \mathrm{ss}$ |
| SYNC Input Threshold Voltage | - | 1.0 | 2.0 | 3.0 | V |
| SYNC Input Impedance | Measured with SYNC $=1.0 \mathrm{~V}$ \& 10 V | 50 | 120 | 230 | $\mathrm{k} \Omega$ |
| 400 kHz Oscillator | CS5124 Only |  |  |  |  |
| Operating Frequency | - | 360 | 400 | 440 | kHz |
| Max Duty Cycle Clamp | - | 80.0 | 82.5 | 85.0 | \% |
| Slope Compensation | - | 15 | 21 | 26 | $\mathrm{mV} / \mu \mathrm{s}$ |

[^33]
## CS5124, CS5126

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}, 7.60 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 20 \mathrm{~V}, \mathrm{UVLO}=3.0 \mathrm{~V}\right.$, $I_{\text {SENSE }}=0 \mathrm{~V}, \mathrm{C}_{\mathrm{V}(\mathrm{CC})}=0.33 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{GATE}}=1.0 \mathrm{nF}(\mathrm{ESR}=10 \Omega) ; \mathrm{C}_{\mathrm{SS}}=470 \mathrm{pF} ; \mathrm{C}_{\mathrm{V}(\mathrm{FB})}=100 \mathrm{pF}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Soft Start |  |  |  |  |  |
| Soft Start Charge Current | - | 7.0 | 10 | 13 | $\mu \mathrm{A}$ |
| Soft Start Discharge Current | - | 0.5 | 10.0 | - | mA |
| $\mathrm{V}_{\mathrm{SS}}$ Voltage when $\mathrm{V}_{\text {FB }}$ Begins to Rise | $\mathrm{V}_{\mathrm{FB}}=300 \mathrm{mV}$ | 1.40 | 1.62 | 1.80 | V |
| Peak Soft Start Charge Voltage | - | 4.7 | 4.9 | - | V |
| Valley Soft Start Discharge Voltage | - | 200 | 275 | 400 | mV |
| Current Sense CS5124 Only |  |  |  |  |  |
| First Current Sense Threshold | At max duty cycle | 170 | 195 | 215 | mV |
| Second Current Sense Threshold | - | 250 | 275 | 315 | mV |
| ISENSE to GATE Prop. Delay | 0 to 700 mV pulse into ISENSE (after blanking time) | 60 | 90 | 130 | ns |
| Leading Edge Blanking Time | 0 to 400 mV pulse into I ISENSE | 90 | 130 | 180 | ns |
| Internal Offset | Note 3 | - | 60 | - | mV |
| Current Sense CS5126 Only |  |  |  |  |  |
| First Current Sense Threshold | At max duty cycle | 300 | 335 | 360 | mV |
| Second Current Sense Threshold | - | 485 | 525 | 575 | mV |
| ISENSE to GATE Prop. Delay | 0 to 800 mV pulse into ISENSE (after blanking time) | 60 | 90 | 130 | ns |
| Leading Edge Blanking Time | 0 to 550 mV pulse into I ISENSE | 110 | 175 | 210 | ns |
| Internal Offset | Note 3 | - | 125 | - | mV |

Voltage Feedback

| $\mathrm{V}_{\mathrm{FB}}$ Pull-up Res. |  | 2.9 | 4.3 | 8.1 | $\mathrm{k} \Omega$ |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{FB}}$ Clamp Voltage | CS5124 Only | 2.63 | 2.90 | 3.15 | V |
| $\mathrm{~V}_{\mathrm{FB}}$ Clamp Voltage | CS5126 Only | 2.40 | 2.65 | 290 | V |
| $\mathrm{~V}_{\mathrm{FB}}$ Fault Voltage Threshold |  | 460 | 490 | 520 | mV |

## Output Gate Drive

| Maximum Sleep Pull-down Voltage | $\mathrm{V}_{\text {CC }}=6.0 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATE High (AC) | Series resistance < $1.0 \Omega$, Note 3 | $\mathrm{V}_{C C}-1.0$ | $\mathrm{V}_{C C}-0.5$ | - | V |
| GATE Low (AC) | Series resistance < $1.0 \Omega$, Note 3 | - | 0.0 | 0.5 | V |
| GATE High Clamp Voltage | $\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}$ | 11.0 | 13.5 | 16.0 | V |
| Rise Time | Measure GATE rise time, $1.0 \mathrm{~V}<\mathrm{GATE}<9.0 \mathrm{~V}$ $V_{C C}=12 \mathrm{~V}$ | - | 45 | 65 | ns |
| Fall TIme | Measure GATE fall time, $9.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V}$ $V_{C C}=12 \mathrm{~V}$ | - | 25 | 55 | ns |

Thermal Shutdown

| Thermal Shutdown Temperature | Note 3 GATE low | 135 | 150 | 165 | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Thermal Enable Temperature | Note 3 GATE switching | 100 | 125 | 150 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Hysteresis | Note 3 | 15 | 25 | 35 | ${ }^{\circ} \mathrm{C}$ |

3. Not tested in production. Specification is guaranteed by design.

## CS5124, CS5126

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |  |
| :---: | :---: | :---: | :--- | :--- |
| $\mathbf{8}$ Lead SO Narrow |  |  |  |
| CS5124 | CS5126 |  | PIN SYMBOL |



Figure 2. Block Diagram

## THEORY OF OPERATION

## Powering the IC

$\mathrm{V}_{\mathrm{CC}}$ can be powered directly from a regulated supply and requires $500 \mu \mathrm{~A}$ of start-up current. The CS5124/6 includes a line bias pin (BIAS) that can be used to control a series pass transistor for operation over a wide input voltage. The BIAS pin will control the gate voltage of an N -channel MOSFET placed between $\mathrm{V}_{\mathrm{IN}}$ and $\mathrm{V}_{\mathrm{CC}}$ to regulate $\mathrm{V}_{\mathrm{CC}}$ at 8.0 V .

## $\mathrm{V}_{\mathrm{Cc}}$ and UVLO Pins

The UVLO pin has three different modes; low power shutdown, Line UVLO, and normal operation. To illustrate how the UVLO pin works; assume that $\mathrm{V}_{\mathrm{IN}}$, as shown in the application schematic, is ramped up starting at 0 V with the UVLO pin open. The SS and ISENSE pins also start at 0 V . While the UVLO is below 1.8 V , the IC will remain in a low current sleep mode and the BIAS pin of the CS5124 is internally clamped to a maximum of 15 V . When the voltage
on the UVLO pin rises to between 1.8 V and 2.6 V the reference for the $\mathrm{V}_{\mathrm{CC}}$ UVLO is enabled and $\mathrm{V}_{\mathrm{CC}}$ is regulated to 8.0 V by the BIAS pin (CS5124 only), but the IC remains in a UVLO state and the output driver does not switch. When the UVLO pin exceeds 2.6 V and the $\mathrm{V}_{\mathrm{CC}}$ pin exceeds 7.7 V , the GATE pin is released from a low state and can begin switching based on the comparison of the I IENSE and $V_{\text {FB }}$ pins. The Soft Start capacitor begins charging from 0 V at $10 \mu \mathrm{~A}$. As the capacitor charges, a buffered version of the capacitor voltage appears on the $\mathrm{V}_{\mathrm{FB}}$ pin and the $\mathrm{V}_{\mathrm{FB}}$ voltage begins to rise. As $\mathrm{V}_{\mathrm{FB}}$ rises the duty cycle increases until the supply comes into regulation.

## Soft Start

Soft Start is accomplished by clamping the $\mathrm{V}_{\mathrm{FB}}$ pin 1.32 V below the SS pin during normal start up and during restart after a fault condition. When the CS5124/6 starts, the Soft

Start capacitor is charged from a $10 \mu \mathrm{~A}$ source from 0 V to 4.9 V. The $\mathrm{V}_{\mathrm{FB}}$ pin follows the Soft Start pin offset by -1.32 V until the supply comes into regulation or until the Soft Start error amp is clamped at $2.9 \mathrm{~V}(2.65 \mathrm{~V}$ for the CS5126). During fault conditions the Soft Start capacitor is discharged at 10 mA .

## Fault Conditions

The CS5124/6 recognizes the following faults: UVLO off, Thermal Shutdown, $\mathrm{V}_{\operatorname{REF}(\mathrm{OK})}$, and Second Current Threshold. Once a fault is recognized, fault latch F2 is set and the IC immediately shuts down the output driver and discharges the Soft Start capacitor. Soft Start will begin only after all faults have been removed and the Soft Start capacitor has been discharged to less than 0.275 V. Each fault will be explained in the following sections.

## Under Voltage Lockout (UVLO)

The UVLO pin is tied to typically the midpoint of a resistive divider between $\mathrm{V}_{\text {IN }}$ and GROUND. During a start up sequence, this pin must be above 2.6 V in order for the IC to begin normal operation. If the IC is running and this pin is pulled below $1.8 \mathrm{~V}, \mathrm{~F} 2$ shuts down the output driver and discharges the Soft Start capacitor in order to insure proper start-up. If the UVLO pin is pulled high again before the Soft Start capacitor discharges, the IC will complete the Soft Start discharge and, if no other faults are present, will immediately restart the power supply. If the UVLO pin stays low, then it will enter either the low current sleep mode or the UVLO state depending on the level of the UVLO pin.

## Thermal Shutdown

If the IC junction temperature exceeds approximately $150^{\circ} \mathrm{C}$ the thermal shutdown circuit sets F2, which shuts down the output driver and discharges the Soft Start capacitor. If no other faults are present the IC will initiate Soft Start when the IC junction temperature has been reduced by $25^{\circ} \mathrm{C}$.

## $\mathbf{V}_{\text {REF(OK) }}$

$\mathrm{V}_{\mathrm{REF}(\mathrm{OK})}$ is an internal monitor that insures the internal regulator is running before any switching occurs. This function does not trip the fault comparator like the other fault functions. To insure that Soft Start will occur at low line conditions the UVLO divider should be set up so that the $\mathrm{V}_{\mathrm{CC}}$ UVLO comparator turns on before the LINE UVLO comparator.

## Second Threshold Comparator

Since the maximum dynamic range of the I IENSE signal in normal operation is 195 mV ( 335 mV for the CS5126), any voltage exceeding this threshold on the I IENSE pin is considered a fault and the PWM cycle is terminated. The 2nd $\mathrm{I}_{\text {COMP }}$ compares the $\mathrm{I}_{\text {SENSE }}$ signal with a 275 mV ( 525 mV for the CS5126) threshold. If the ISENSE voltage exceeds the second threshold, F2 is set, the driver turns off, and the Soft Start capacitor discharges. After the Soft Start capacitor has discharged to less than 0.275 V Soft Start will begin. If the fault condition has been removed the supply will operate normally. If the fault remains the supply will operate in hiccup mode until the fault condition is removed.

## $\mathrm{V}_{\mathrm{FB}}$ Comparator

The $\mathrm{V}_{\mathrm{FB}}$ comparator detects when the output voltage is too high. When the regulated output voltage is too high, the feedback loop will drive $\mathrm{V}_{\mathrm{FB}}$ low. If $\mathrm{V}_{\mathrm{FB}}$ is less than 0.49 V the output of the $\mathrm{V}_{\mathrm{FB}}$ comparator will go high and shut the output driver off.

## Oscillator

The internally trimmed, 400 kHz (CS5124) or 200 kHz (CS5126) provides the slope compensation ramp as well as the pulse for enabling the output driver.

## PWM Comparator and Slope Compensation

The CS5124/6 provides a fixed internal slope compensation ramp that is subtracted from the feedback signal. The PWM comparator compares peak primary current to a portion of the difference of the feedback voltage and slope compensation ramp. The $170 \mathrm{mV} / \mu \mathrm{s}(85 \mathrm{mV} / \mu \mathrm{s}$ for the CS5126) slope compensation ramp is subtracted from the voltage feedback signal internally. The difference signal is then divided by ten (five for the CS5126) before the PWM comparator to provide high noise rejection with a low voltage across the current sense network. (The effective ramp is $21 \mathrm{mV} / \mu \mathrm{s}$ for the CS5124, and $18 \mathrm{mV} / \mu \mathrm{s}$ for the CS5126). A 60 mV ( 125 mV for the CS5126) nominal offset on the positive input to the PWM comparator allows for operation with the $\mathrm{I}_{\text {SENSE }}$ pin at, or even slightly below GND.

A $4.3 \mathrm{k} \Omega$ pull-up resistor internally connected to a 5.0 V nominal reference provides the bias current to for an optocoupler connection to the $\mathrm{V}_{\mathrm{FB}}$ pin.

## APPLICATION INFORMATION

## UVLO and Thermal Shutdown Interaction

The UVLO pin and thermal shutdown circuit share the same internal comparator. During high temperature operation $\left(\mathrm{T}_{\mathrm{J}}>100^{\circ} \mathrm{C}\right)$ the UVLO pin will interact with the thermal shutdown circuit. This interaction increases the turn-on threshold (and hysteresis) of the UVLO circuit. If the UVLO pin shuts down the IC during high temperature operation, higher hysteresis (see hysteresis specification) might be required to enable the IC.

## BIAS Pin (CS5124 Only)

The bias pin can be used to control $\mathrm{V}_{\mathrm{CC}}$ as shown in the main application diagram in Figure 1. In order to provide adequate phase margin for the bias control loop, the pole created by the series pass transistor and the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor should be kept above 10 kHz . The frequency of this pole can be calculated by Formula (1).
Pole Frequency $=\frac{\text { Transconductance of pass Transistor }}{2 \times \pi \times \mathrm{CV}(\mathrm{CC})}$
The Line BIAS pin shows a significant change in the regulated $\mathrm{V}_{\mathrm{CC}}$ voltage when sinking large currents. This will show up as poor line regulation with a low value pull-up resistor. Typical regulated $\mathrm{V}_{\mathrm{CC}}$ vs BIAS pin sink current is shown in Figure 3.


Figure 3. Regulated V $_{\text {Cc }}$ vs. BIAS Sink Current
The BIAS pin and associated components form a high impedance node. Care should be taken during PCB layout to avoid connections that could couple noise into this node.

## Clock Synchronization Pin (CS5126 Only)

The CS5126 can be synchronized to signals ranging from $30 \%$ slower to several times faster than the internal oscillator frequency. If the part is synchronized to a fast signal, maximum duty cycle will be reduced as the frequency increases as shown in Figure 4.


Figure 4. CS5126 Maximum Duty Cycle vs. Frequency (Synchronized Operation)
If the converter is initially free running and a sync signal is applied, the current oscillator cycle will terminate and the oscillator will lock on to the sync signal. The SYNC pin works with a positive edge triggered signal. When the sync signal transitions high the current PWM cycle terminates and a new cycle begins as shown in Figure 5. The typical phase lag between the rising edge of the SYNC signal and the rising edge of the Gate is shown in Figure 6. When this pin is held high or low the internal clock determines the oscillator frequency.


Figure 5. Synchronized Operation


Figure 6. Typical Phase Lag between SYNC and GATE on

## Gate Drive

Rail to rail gate driver operation can be obtained (up to 13.5 V) over a range of MOSFET input capacitance if the gate resistor value is kept low. Figure 5 shows the high gate drive level vs. the series gate resistance with $\mathrm{V}_{\mathrm{CC}}=8.0 \mathrm{~V}$ driving an IRF220.


Figure 7. Gate Drive vs. Gate Resistor Driving an IRF220 ( $\mathrm{V}_{\mathrm{CC}}=8.0 \mathrm{~V}$ )

A large negative $\mathrm{dv} / \mathrm{dt}$ on the power MOSFET drain will couple current into the gate driver through the gate to drain capacitance. If this current is kept within absolute maximum ratings for the GATE pin it will not damage the IC. However if a high negative dv/dt coincides with the start of a PWM duty cycle, there will be small variations in oscillator frequency due to current in the controller substrate. If required, this can be avoided by choosing the transformer ratio and reset circuit so that a high dv/dt does not coincide with the start of a PWM cycle, or by clamping the negative voltage on the GATE pin with a schottky diode

## First Current Sense Threshold

During normal operation the peak primary current is controlled by the level of the $\mathrm{V}_{\mathrm{FB}}$ pin (as determined by the control loop) and the current sense network. Once the signal on the $\mathrm{I}_{\text {SENSE }}$ pin exceeds the level determined by $\mathrm{V}_{\mathrm{FB}}$ pin the PWM cycle terminates. During high output currents the $\mathrm{V}_{\mathrm{FB}}$ pin will rise until it reaches the $\mathrm{V}_{\mathrm{FB}}$ clamp. The first current sense threshold determines the maximum signal allowed on the I ISENSE pin before the PWM cycle is terminated. Under this condition the maximum peak current is determined by the $\mathrm{V}_{\mathrm{FB}}$ Clamp, the slope compensation ramp, the PWM comparator offset voltage and the PWM on time. The nominal first current threshold varies with on time and can be calculated from Formulas (2) \& (3) below.

CS5124
1st Threshold $=\frac{2.9 \mathrm{~V}-170 \mathrm{mV} / \mu \mathrm{s} \times \text { TON }}{10}-60 \mathrm{mV}$
CS5126
1st Threshold $=\frac{2.65 \mathrm{~V}-85 \mathrm{mV} / \mu \mathrm{s} \times \mathrm{T} \mathrm{ON}}{5.0}-125 \mathrm{mV}$

When the output current is high enough for the I ISENSE pin to exceed the first threshold, the PWM cycle terminates early and the converter begins to function more like a current source. The current sense network must be chosen so that the peak current during normal operation does not exceed the first current sense threshold.

## Second Current Sense Threshold

The second threshold is intended to protect the converter from over-heating by switching to a low duty cycle mode when there are abnormally high fast rise currents in the converter. If the second current sense threshold is tripped, the converter will shut off and restart in Soft Start mode until the high current condition is removed. The dead time after a second threshold over-current condition will primarily be determined by the time required to charge the Soft Start cap from 0.275 V nominal to 1.32 V .

The second threshold will only be reached when a high $\mathrm{dv} / \mathrm{dt}$ is present at the current sense pin. The signal must be fast enough to reach the second threshold before the first threshold turns off the driver. This will normally happen if the forward inductor saturates or when there is a shorted load.

Excessive filtering of the current sense signal, a low value current sense resistor, or even an inductor that does not saturate during heavy output currents can prevent the second threshold from being reached. In this case the first current sense threshold will trip during each cycle of high output current conditions. The first threshold will limit output current but some components, especially the output rectifier, can overheat due to higher than normal average output current.

## Slope Compensation

Current mode converters operating at duty cycles in excess of $50 \%$ require an artificial ramp to be added to the current waveform or subtracted from the feedback waveform. For the current loop to be stable the artificial ramp must be equivalent to at least $50 \%$ of the inductor current down slope and is typically chosen between $75 \%$ to $100 \%$ of the inductor down current down slope.
To choose an inductor value such that the internal slope compensation ramp will be equal to a certain fraction of the inductor down current slope use the Formula (4).
$\frac{1}{\text { Internal Ramp }} \times\left(\right.$ V OUT $\left.+\mathrm{V}_{\text {RECTIFIER }}\right) \times \frac{\mathrm{N}_{\text {SECONDARY }}}{\mathrm{NPRIMARY}} \times$
RSENSE $\times$ Slope Value Factor $=$ Inductor Value $(\mathrm{H})$
Calculating the nominal inductor value for an artificial ramp equivalent to $100 \%$ of the current inductor down slope at CS5126 nominal conditions, a 5.0 V output, a $200 \mathrm{~m} \Omega$ current sense resistor and a $4: 1$ transformer ratio yields
$\frac{1}{20 \mathrm{mV} / \mu \mathrm{s}} \times(5.0 \mathrm{~V}+0.3 \mathrm{~V}) \times \frac{1}{4} \times 0.2 \Omega \times 1.0=13.2 \mu \mathrm{H}$

To check that the slope compensation ramp will be greater than $50 \%$ of the inductor down under all conditions, substitute the minimum internal slope compensation value and use 0.5 for the slope compensation value. Then check that the actual inductor value will always be greater than the inductor value calculated.

During synchronized operation of the CS5126 the slope compensation ramp is reduced by $33 \%$. If the CS5126 will be used in synchronized operation, the inductor value should be recalculated to work with the slope compensation ramp reduced to $67 \%$ of the normal value.

## Powering the CS5124/6 from a Transformer Winding

There are numerous ways to power the CS5124/6 from a transformer winding to enable the converter to be operated at high efficiency over a wide input range. Two ways are shown in the application circuits.

The CS5124 application circuit in Figure 1 is a flyback converter that uses a second flyback winding to power $\mathrm{V}_{\mathrm{CC}}$. R 4 improves $\mathrm{V}_{\mathrm{CC}}$ regulation with load changes by snubbing the turn off spike. Once the turn off spike has subsided the voltage of this winding is voltage proportional to the voltage on the main flyback winding. This voltage is regulated because the main winding is clamped by the regulated output voltage.

In the CS5126 application circuit in Figure 8 an extra winding is added to the forward inductor to power $\mathrm{V}_{\mathrm{CC}}$. This winding is phased to conduct during the off time of the forward converter and performs the same function as the flyback winding above.

A flyback winding from a forward transformer can also be used to power $\mathrm{V}_{\mathrm{CC}}$. Ideally the transformer volt-second product of a forward converter would be constant over the range of line voltages and load currents; and the transformer inductance could be chosen to store the required level of energy during each cycle to power $\mathrm{V}_{\mathrm{CC}}$. Even though the flyback energy is not directly regulated it would remain constant. Unfortunately in a real converter there are many non-ideal effects that degrade regulation. Transformer inductance varies, converter frequency varies, energy stored in primary leakage inductance varies with output current, stray transformer capacitances and various parasitics all effect the level of energy available for $\mathrm{V}_{\mathrm{CC}}$. If too little energy is provided to $\mathrm{V}_{\mathrm{CC}}$, the bootstrapping circuit must provide power and efficiency will be reduced. If too much energy is provided $\mathrm{V}_{\mathrm{CC}}$ rises and may damage the controller. If this approach is taken the circuit must be carefully designed and component values must be controlled for good regulation.


Figure 8. Additional Application Diagram, 48 V to 5.0 V, 5.0 A Forward Converter using the CS5126

## CS5124, CS5126

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 45 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 165 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

MC44603A

## Enhanced Mixed Frequency Mode GreenLine ${ }^{T M}$ PWM Controller: <br> Fixed Frequency, Variable Frequency, Standby Mode

The MC44603A is an enhanced high performance controller that is specifically designed for off-line and dc-to-dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded, unloaded, or shorted, offering the designer additional protection for increased system reliability. The MC44603A has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetization detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters ( $<150 \mathrm{~W}$ ). It is optimized to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

## Current or Voltage Mode Controller

- Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Oscillator with Precise Frequency Control


## High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis


## Safety/Protection Features

- Overvoltage Protection Against Open Current and Open Voltage Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft-Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference
- Enhanced Output Drive


## GreenLine Controller: Low Power Consumption in Standby Mode

- Low Startup and Operating Current
- Fully Programmable Standby Mode
- Controlled Frequency Reduction in Standby Mode
- Low dV/dT for Low EMI Radiations

GreenLine is a trademark of Motorola, Inc.

## MIXED FREQUENCY MODE GREENLINE PWM* CONTROLLER:

VARIABLE FREQUENCY, FIXED FREQUENCY, STANDBY MODE

* PWM = Pulse Width Modulation


P SUFFIX PLASTIC PACKAGE CASE 648

16

DW SUFFIX
PLASTIC PACKAGE CASE 751G (SOP-16L)

## PIN CONNECTIONS



## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Total Power Supply and Zener Current | $\left(\mathrm{I}_{\mathrm{CC}}+\mathrm{I}_{\mathrm{z}}\right.$ ) | 30 | mA |
| Supply Voltage with Respect to Ground (Pin 4) | $\begin{aligned} & \mathrm{V}_{\mathrm{C}} \\ & \mathrm{~V}_{\mathrm{CC}} \end{aligned}$ | 18 | V |
| Output Current (Note 1) <br> Source <br> Sink | IO(Source) lo(Sink) | $\begin{gathered} -750 \\ 750 \end{gathered}$ | mA |
| Output Energy (Capacitive Load per Cycle) | W | 5.0 | $\mu \mathrm{J}$ |
| $\mathrm{R}_{\mathrm{F} \text { Stby }}, \mathrm{C}_{\mathrm{T}}$, Soft-Start, $\mathrm{R}_{\text {ref }}, \mathrm{R}_{\mathrm{P} \text { Stby }}$ Inputs | $V_{\text {in }}$ | -0.3 to 5.5 | V |
| Foldback Input, Current Sense Input, E/A Output, Voltage Feedback Input, Overvoltage Protection, Synchronization Input | $V_{\text {in }}$ | $\begin{gathered} -0.3 \text { to } \\ v_{C C}+0.3 \end{gathered}$ | V |
| Synchronization Input <br> High State Voltage <br> Low State Reverse Current | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}+0.3 \\ -20 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Demagnetization Detection Input Current Source <br> Sink | Idemag-ib (Source) $I_{\text {demag-ib (Sink) }}$ | $\begin{gathered} -4.0 \\ 10 \end{gathered}$ | mA |
| Error Amplifier Output Sink Current | $\mathrm{I}_{\mathrm{E} / \mathrm{A}}$ (Sink) | 20 | mA |
| Power Dissipation and Thermal Characteristics P Suffix, Dual-In-Line, Case 648 Maximum Power Dissipation at $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air DW Suffix, Surface Mount, Case 751G Maximum Power Dissipation at $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{gathered} 0.6 \\ 100 \\ \\ 0.45 \\ 145 \end{gathered}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\text {A }}$ | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |

NOTES: 1. Maximum package power dissipation limits must be observed. 2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{Cc}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$, [Note 3], $\mathrm{R}_{\mathrm{ref}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=820 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ [Note 4], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OUTPUT SECTION |  |  |  |  |  |
| $\begin{array}{r} \hline \text { Output Voltage (Note 5) } \\ \text { Low State }\left(I_{\text {Sink }}=100 \mathrm{~mA}\right) \\ \text { (ISink }=500 \mathrm{~mA}) \\ \text { High State }\left(I_{\text {Source }}=200 \mathrm{~mA}\right) \\ \left(I_{\text {Source }}=500 \mathrm{~mA}\right) \end{array}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{OL}} \\ & \mathrm{v}_{\mathrm{OH}} \end{aligned}$ | - | $\begin{aligned} & 1.0 \\ & 1.4 \\ & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 1.2 \\ & 2.0 \\ & 2.0 \\ & 2.7 \end{aligned}$ | V |
| $\begin{aligned} & \text { Output Voltage During Initialization Phase } \\ & \mathrm{V}_{\mathrm{CC}}=0 \text { to } 1.0 \mathrm{~V}, I_{\text {Sink }}=10 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=1.0 \text { to } 5.0 \mathrm{~V}, I_{\text {Sink }}=100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \text { to } 13 \mathrm{~V}, I_{\text {Sink }}=1.0 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & -\overline{1} \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.0 \\ & 1.0 \end{aligned}$ | V |
| Output Voltage Rising Edge Slew-Rate ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | dVo/dT | - | 300 | - | V/ $/ \mathrm{s}$ |
| Output Voltage Falling Edge Slew-Rate ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | dVo/dT | - | -300 | - | V/us |

## ERROR AMPLIFIER SECTION

| Voltage Feedback Input $\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=2.5 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{FB}}$ | 2.42 | 2.5 | 2.58 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{FB}}=2.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{FB}-\mathrm{ib}}$ | -2.0 | -0.6 | - | $\mu \mathrm{A}$ |
| Open Loop Voltage Gain $\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=2.0\right.$ to 4.0 V$)$ | $\mathrm{A}_{\mathrm{VoL}}$ | 65 | 70 | - | dB |

NOTES: 3. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the startup threshold before setting to 12 V .
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. $\mathrm{V}_{\mathrm{C}}$ must be greater than 5.0 V .

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$, [Note 3], $\mathrm{R}_{\text {ref }}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=820 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for $\mathrm{min} / \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ [Note 4], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER SECTION (continued) |  |  |  |  |  |
| Unity Gain Bandwidth $\begin{aligned} & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | BW | - | $4.0$ | $5.5$ | MHz |
| Voltage Feedback Input Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=10$ to 15 V ) | $V_{\text {FBline-reg }}$ | -10 | - | 10 | mV |
| $\begin{aligned} & \text { Output Current } \\ & \text { Sink }\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \\ & \text { Source }\left(\mathrm{V}_{\mathrm{E} / \mathrm{A}} \text { out }=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $I_{\text {Sink }}$ <br> $I_{\text {Source }}$ | $\begin{array}{r} 2.0 \\ -2.0 \end{array}$ | 12 | $-0.2$ | mA |
| Output Voltage Swing <br> High State ( $\mathrm{I}_{\mathrm{E} / \mathrm{A} \text { out }}$ (source) $=0.5 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) Low State ( $\mathrm{I}_{\mathrm{E} / \mathrm{A}}$ out (sink) $=0.33 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ |  | $\begin{aligned} & 6.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 1.1 \\ & \hline \end{aligned}$ | V |

## REFERENCE SECTION

| Reference Output Voltage $\left(\mathrm{V}_{\mathrm{CC}}=10\right.$ to 15 V$)$ | $\mathrm{V}_{\text {ref }}$ | 2.4 | 2.5 | 2.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Reference Current Range $\left(\mathrm{I}_{\text {ref }}=\mathrm{V}_{\text {ref }} / \mathrm{R}_{\text {ref }}, \mathrm{R}=5.0 \mathrm{k}\right.$ to $\left.25 \mathrm{k} \Omega\right)$ | $\mathrm{I}_{\text {ref }}$ | -500 | - | -100 | $\mu \mathrm{~A}$ |
| Reference Voltage Over $\mathrm{I}_{\text {ref }}$ Range | $\Delta \mathrm{V}_{\text {ref }}$ | -40 | - | 40 | mV |

## OSCILLATOR AND SYNCHRONIZATION SECTION

| Frequency $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | fosc | $\begin{gathered} 44.5 \\ 44 \end{gathered}$ | 48 | $\begin{gathered} 51.5 \\ 52 \end{gathered}$ | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage ( $\mathrm{V}_{\mathrm{CC}}=10$ to 15 V ) | $\Delta \mathrm{f}_{\mathrm{Osc}} / \Delta \mathrm{V}$ | - | 0.05 | - | \%/V |
| Frequency Change with Temperature ( $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ ) | $\Delta \mathrm{f}_{\mathrm{OSc}} / \Delta \mathrm{T}$ | - | 0.05 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| Oscillator Voltage Swing (Peak-to-Peak) | V Osc(pp) | 1.65 | 1.8 | 1.95 | V |
| Ratio Charge Current/Reference Current $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C}\left(\mathrm{~V}_{\mathrm{CT}}=2.0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\text {charge }} / \mathrm{Iref}$ | $\begin{gathered} 0.375 \\ 0.37 \end{gathered}$ |  | $\begin{gathered} 0.425 \\ 0.43 \end{gathered}$ | - |
| Fixed Maximum Duty Cycle $=I_{\text {discharge }} /\left(I_{\text {discharge }}+I_{\text {charge }}\right)$ | D | 78 | 80 | 82 | \% |
| Ratio Standby Discharge Current versus IR F Stby (Note 6) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \text { (Note 8) } \end{aligned}$ | Idisch-Stby/ IRFStby | $\begin{aligned} & 0.46 \\ & 0.43 \end{aligned}$ | $0.53$ | $\begin{gathered} 0.6 \\ 0.63 \end{gathered}$ | - |
| $\mathrm{V}_{\text {R F Stby }}\left(\mathrm{l}_{\text {R F Stby }}=100 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\text {R F Stby }}$ | 2.4 | 2.5 | 2.6 | V |
| Frequency in Standby Mode ( $\left.\mathrm{R}_{\mathrm{F} \text { Stby }}(\mathrm{Pin} 15)=25 \mathrm{k} \Omega\right)$ | $\mathrm{F}_{\text {Stby }}$ | 18 | 21 | 24 | kHz |
| Current Range | IRFStby | -200 | - | -50 | $\mu \mathrm{A}$ |
| Synchronization Input Threshold Voltage (Note 7) | $\begin{aligned} & \hline \mathrm{V}_{\text {inthH }} \\ & \mathrm{V}_{\text {inthL }} \end{aligned}$ | $\begin{gathered} \hline 3.2 \\ 0.45 \end{gathered}$ | $\begin{aligned} & 3.7 \\ & 0.7 \end{aligned}$ | $\begin{aligned} & 4.3 \\ & 0.9 \end{aligned}$ | V |
| Synchronization Input Current | $I_{\text {Sync-in }}$ | -5.0 | - | 0 | $\mu \mathrm{A}$ |
| Minimum Synchronization Pulse Width (Note 8) | $t_{\text {Sync }}$ | - | - | 0.5 | $\mu \mathrm{s}$ |

## UNDERVOLTAGE LOCKOUT SECTION

| Startup Threshold | $\mathrm{V}_{\text {stup-th }}$ | 13.6 | 14.5 | 15.4 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Disable Voltage After Threshold Turn-On (UVLO 1) | $\mathrm{V}_{\text {disable1 }}$ |  |  |  | V |
| $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ |  | 8.6 | 9.0 | 9.4 |  |
| $\mathrm{~T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  | 8.3 | - | 9.6 |  |
| Reference Disable Voltage After Threshold Turn-On (UVLO 2) | $\mathrm{V}_{\text {disable2 }}$ | 7.0 | 7.5 | 8.0 | V |

NOTES: 3. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the startup threshold before setting to 12 V .
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. Standby is disabled for $\mathrm{V}_{\text {R P Stby }}<25 \mathrm{mV}$ typical.
7. If not used, Synchronization input must be connected to Ground.
8. Synchronization Pulse Width must be shorter than $\mathrm{t}_{\mathrm{OSC}}=1 / \mathrm{f}$ OSc .

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$, [Note 3], $\mathrm{R}_{\text {ref }}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=820 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ [Note 4], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DEMAGNETIZATION DETECTION SECTION (Note 9) |  |  |  |  |  |
| Demagnetization Detect Input <br> Demagnetization Comparator Threshold ( $\mathrm{V}_{\text {Pin } 9}$ Decreasing) <br> Propagation Delay (Input to Output, Low to High) <br> Input Bias Current ( $\mathrm{V}_{\text {demag }}=65 \mathrm{mV}$ ) | $\begin{gathered} \mathrm{V}_{\text {demag-th }} \\ - \\ \mathrm{I}_{\text {demag-lb }} \end{gathered}$ | $\begin{gathered} 50 \\ - \\ -0.5 \end{gathered}$ | $\begin{gathered} 65 \\ 0.25 \end{gathered}$ | 80 - | $\begin{aligned} & \mathrm{mV} \\ & \mu \mathrm{~s} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Negative Clamp Level ( $\mathrm{l}_{\text {demag }}=-2.0 \mathrm{~mA}$ ) | $\mathrm{C}_{\mathrm{L} \text { (neg) }}$ | - | -0.38 | - | V |
| Positive Clamp Level ( $\mathrm{l}_{\text {demag }}=2.0 \mathrm{~mA}$ ) | $\mathrm{C}_{\mathrm{L}(\mathrm{pos})}$ | - | 0.72 | - | V |

SOFT-START SECTION (Note 11)

| Ratio Charge Current/ $/$ ref |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | $\mathrm{I}_{\mathrm{ss}(\text { ch })} / I_{\text {ref }}$ |  |  |  | - |
| $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  | 0.37 | 0.4 | 0.43 |  |
| Discharge Current $\left(\mathrm{V}_{\text {soft-start }}=1.0 \mathrm{~V}\right)$ |  | 0.36 | - | 0.44 |  |
| Clamp Level | $\mathrm{I}_{\text {discharge }}$ | 1.5 | 5.0 | - | mA |
| Duty Cycle $\left(\mathrm{R}_{\text {soft-start }}=12 \mathrm{k} \Omega\right)$ |  |  |  |  |  |
| $\left(\mathrm{V}_{\text {soft-start }}(\right.$ Pin 11$\left.)=0.1 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {ss(CL) }}$ | 2.2 | 2.4 | 2.6 | V |

## OVERVOLTAGE SECTION

| Protection Threshold Level on $\mathrm{V}_{\text {OVP }}$ | $\mathrm{V}_{\text {OVP-th }}$ | 2.42 | 2.5 | 2.58 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay ( $\mathrm{V}_{\text {OVP }}>2.58 \mathrm{~V}$ to $\mathrm{V}_{\text {out }}$ Low) |  | 1.0 | - | 3.0 | $\mu \mathrm{s}$ |
| $\begin{aligned} & \text { Protection Level on } \mathrm{V}_{\mathrm{CC}} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {CC prot }}$ | $\begin{aligned} & 16.1 \\ & 15.9 \end{aligned}$ |  | $\begin{aligned} & 17.9 \\ & 18.1 \end{aligned}$ | V |
| Input Resistance $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | - | $\begin{aligned} & 1.5 \\ & 1.4 \end{aligned}$ | 2.0 | $\begin{aligned} & 3.0 \\ & 3.4 \end{aligned}$ | k $\Omega$ |

FOLDBACK SECTION (Note 10)

| Current Sense Voltage Threshold $\left(\mathrm{V}_{\text {foldback }}(\right.$ Pin 5$\left.)=0.9 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {CS-th }}$ | 0.86 | 0.89 | 0.9 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Foldback Input Bias Current $\left(\mathrm{V}_{\text {foldback }}(\operatorname{Pin} 5)=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {foldback-lb }}$ | -6.0 | -2.0 | - | $\mu \mathrm{A}$ |

## STANDBY SECTION

| Ratio IR P Stby $/ I_{\text {ref }}$ $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\text {P P Stby }} / I_{\text {ref }}$ | $\begin{aligned} & 0.37 \\ & 0.36 \end{aligned}$ |  | $\begin{aligned} & 0.43 \\ & 0.44 \end{aligned}$ | - |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Ratio Hysteresis ( $\mathrm{V}_{\mathrm{h}}$ Required to Return to Normal Operation from Standby Operation) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{h}} / \mathrm{V}_{\mathrm{R}} \mathrm{P}$ Stby | $\begin{gathered} 1.42 \\ 1.4 \end{gathered}$ | $1.5$ | $\begin{gathered} 1.58 \\ 1.6 \end{gathered}$ | - |
| Current Sense Voltage Threshold ( $\mathrm{V}_{\text {R P Stby (Pin 12) }}=1.0 \mathrm{~V}$ ) | $\mathrm{V}_{\text {CS-Stby }}$ | 0.28 | 0.31 | 0.34 | V |

CURRENT SENSE SECTION

| Maximum Current Sense Input Threshold <br> $\left(V_{\text {feedback (Pin 14) }}=2.3 \mathrm{~V}\right.$ and $\left.\mathrm{V}_{\text {foldback (Pin 6) }}=1.2 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {CS-th }}$ | 0.96 | 1.0 | 1.04 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | $\mathrm{I}_{\text {CS-ib }}$ | -10 | -2.0 | - | $\mu \mathrm{A}$ |
| Propagation Delay (Current Sense Input to Output at $\mathrm{V}_{\text {TH }}$ of <br> MOS transistor $=3.0 \mathrm{~V})$ | - | - | 120 | 200 | ns |

TOTAL DEVICE

| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Startup $\left(\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}\right.$ with $\mathrm{V}_{\mathrm{CC}}$ Increasing) <br> Operating $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}($ Note 3$)$ |  | - | 0.3 | 0.45 |  |
| Power Supply Zener Voltage $\left(\mathrm{I}_{\mathrm{CC}}=25 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{Z}}$ | 13.5 | - | - | V |
| Thermal Shutdown | - | - | 155 | - | ${ }^{\circ} \mathrm{C}$ |

NOTES: 3. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the startup threshold before setting to 12 V .
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
9. This function can be inhibited by connecting Pin 8 to Gnd. This allows a continuous current mode operation.
10. This function can be inhibited by connecting Pin 5 to $\mathrm{V}_{\mathrm{Cc}}$.
11. The MC44603A can be shut down by connecting the Soft-Start pin (Pin 11) to Ground.

Representative Block Diagram


This device contains 243 active transistors.


Figure 1. Timing Resistor versus Oscillator Frequency


Figure 3. Oscillator Frequency versus Temperature


Figure 2. Standby Mode Timing Capacitor versus Oscillator Frequency


Figure 4. Ratio Charge Current/Reference Current versus Temperature


Figure 5. Output Waveform


Figure 7. Oscillator Discharge Current versus Temperature


Figure 9. Sink Output Saturation Voltage versus Sink Current


Figure 11. Voltage Feedback Input versus Temperature


Figure 8. Source Output Saturation Voltage versus Load Current


Figure 10. Error Amplifier Gain and Phase versus Frequency


Figure 12. Demag Comparator Threshold versus Temperature


Figure 13. Current Sense Gain versus Temperature


Figure 15. Propagation Delay Current Sense Input to Output versus Temperature


Figure 16. Startup Current versus $\mathrm{V}_{\mathrm{Cc}}$


Figure 17. Supply Current versus Supply Voltage


Figure 18. Power Supply Zener Voltage versus Temperature

## MC44603A



Figure 19. Startup Threshold Voltage versus Temperature


Figure 21. Disable Voltage After Threshold Turn-On (UVLO2) versus Temperature


Figure 23. Protection Level on $\mathrm{V}_{\mathrm{CC}}$ versus Temperature


Figure 20. Disable Voltage After Threshold Turn-On (UVLO1) versus Temperature


Figure 22. Protection Threshold Level on V ovp versus Temperature


Figure 24. Propagation Delay (Vovp > 2.58 V to $\mathrm{V}_{\text {out }}$ Low) versus Temperature


Figure 25. Standby Reference Current versus Temperature


Figure 26. Current Sense Voltage Threshold Standby Mode versus Temperature

PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
| :---: | :---: | :---: |
| 1 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the IC. The operating voltage range after startup is 9.0 to 14.5 V . |
| 2 | $\mathrm{V}_{\mathrm{C}}$ | The output high state $\left(\mathrm{V}_{\mathrm{OH}}\right)$ is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching noise on the control circuitry. |
| 3 | Output | Peak currents up to 750 mA can be sourced or sunk, suitable for driving either MOSFET or Bipolar transistors. This output pin must be shunted by a Schottky diode, 1N5819 or equivalent. |
| 4 | Gnd | The ground pin is a single return, typically connected back to the power source; it is used as control and power ground. |
| 5 | Foldback Input | The foldback function provides overload protection. Feeding the foldback input with a portion of the $\mathrm{V}_{\mathrm{CC}}$ voltage ( 1.0 V max) establishes on the system control loop a foldback characteristic allowing a smoother startup and sharper overload protection. Above 1.0 V the foldback input is inactive. |
| 6 | Overvoltage Protection | When the overvoltage protection pin receives a voltage greater than 17 V , the device is disabled and requires a complete restart sequence. The overvoltage level is programmable. |
| 7 | Current Sense Input | A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer when working in a current mode of operation. A maximum level of 1.0 V allows either current or voltage mode operation. |
| 8 | Demagnetization Detection | A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback transformer. A zero voltage detection corresponds to complete core saturation. The demagnetization detection ensures a discontinuous mode of operation. This function can be inhibited by connecting Pin 8 to Gnd. |
| 9 | Synchronization Input | The synchronization input pin can be activated with either a negative pulse going from a level between 0.7 V and 3.7 V to Gnd or a positive pulse going from a level between 0.7 V and 3.7 V up to a level higher than 3.7 V . The oscillator runs free when Pin 9 is connected to Gnd. |
| 10 | $\mathrm{C}_{\text {T }}$ | The normal mode oscillator frequency is programmed by the capacitor $\mathrm{C}_{\mathrm{T}}$ choice together with the $\mathrm{R}_{\text {ref }}$ resistance value. $\mathrm{C}_{\mathrm{T}}$, connected between Pin 10 and Gnd, generates the oscillator sawtooth. |
| 11 | Soft-Start/ $D_{\text {max }} /$ Voltage-Mode | A capacitor, resistor or a voltage source connected to this pin limits the switching duty-cycle. This pin can be used as a voltage mode control input. By connecting Pin 11 to Ground, the MC44603A can be shut down. |
| 12 | RP Standby | A voltage level applied to the $R_{P}$ Standby pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation (i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at a higher output power level. |
| 13 | E/A Out | The error amplifier output is made available for loop compensation. |
| 14 | Voltage Feedback | This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or other) feedback loop. |
| 15 | $\mathrm{R}_{\mathrm{F} \text { Standby }}$ | The reduced frequency or standby frequency programming is made by the $\mathrm{R}_{F}$ Standby resistance choice. |
| 16 | $\mathrm{R}_{\text {ref }}$ | $\mathrm{R}_{\text {ref }}$ sets the internal reference current. The internal reference current ranges from $100 \mu \mathrm{~A}$ to $500 \mu \mathrm{~A}$. This requires that $5.0 \mathrm{k} \Omega \leq \mathrm{R}_{\mathrm{ref}} \leq 25 \mathrm{k} \Omega$. |



Figure 27. Starting Behavior and Overvoltage Management


Figure 28. Demagnetization


Figure 29. Switching Off Behavior


Figure 30. Oscillator


Figure 31. Soft-Start \& $D_{\text {max }}$
OPERATING DESCRIPTION

## Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 70 dB . The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is $-2.0 \mu \mathrm{~A}$. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diode drops $(\approx 1.4 \mathrm{~V})$ and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 3) when Pin 13 is at its lowest state ( $\mathrm{V}_{\mathrm{OL}}$ ). The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current $(0.2 \mathrm{~mA})$ and the required output voltage $\left(\mathrm{V}_{\mathrm{OH}}\right)$ to reach the current sense comparator's 1.0 V clamp level:

$$
\mathrm{R}_{\mathrm{f}(\min )} \approx \frac{3.0(1.0 \mathrm{~V})+1.4 \mathrm{~V}}{0.2 \mathrm{~mA}}=22 \mathrm{k} \Omega
$$



## Figure 32. Error Amplifier Compensation

## Current Sense Comparator and PWM Latch

The MC44603A can operate as a current mode controller or as a voltage mode controller. In current mode operation, the MC44603A uses the current sense comparator. The output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output
(Pin 13). Thus, the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle.

The inductor current is converted to a voltage by inserting the ground referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ in series with the power switch Q1.

This voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$
\mathrm{I}_{\mathrm{pk}} \approx \frac{\mathrm{~V}(\operatorname{Pin} 13)-1.4 \mathrm{~V}}{3 \mathrm{RS}_{\mathrm{S}}}
$$

The Current Sense Comparator threshold is internally clamped to 1.0 V . Therefore, the maximum peak switch current is:

$$
\operatorname{lpk}(\max ) \approx \frac{1.0 \mathrm{~V}}{\mathrm{R}_{\mathrm{S}}}
$$



Figure 33. Output Totem Pole

Series gate resistor, R2, will dampen any high frequency oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. Diode $D$ is required if the negative current into the output drive pin exceeds 15 mA .

## Oscillator

The oscillator is a very accurate sawtooth generator that can work either in free mode or in synchronization mode. In this second mode, the oscillator stops in the low state and waits for a demagnetization or a synchronization pulse to start a new charging cycle.

## - The Sawtooth Generation:

In the steady state, the oscillator voltage varies between about 1.6 V and 3.6 V .

The sawtooth is obtained by charging and discharging an external capacitor $\mathrm{C}_{\mathrm{T}}$ (Pin 10), using two distinct current sources $=I_{\text {charge }}$ and $\mathrm{I}_{\text {discharge }}$. In fact, $\mathrm{C}_{\mathrm{T}}$ is permanently connected to the charging current source ( $0.4 \mathrm{I}_{\mathrm{ref}}$ ) and so,
the discharge current source has to be higher than the charge current to be able to decrease the $\mathrm{C}_{\mathrm{T}}$ voltage (refer to Figure 35).

This condition is performed, its value being ( $2.0 \mathrm{I}_{\mathrm{ref}}$ ) in normal working and ( $0.4 \mathrm{I}_{\mathrm{ref}}+0.5 \mathrm{I}_{\mathrm{F} \text { Stby }}$ in standby mode).


Figure 34. Oscillator


Figure 35. Simplified Block Oscillator

Two comparators are used to generate the sawtooth. They compare the $\mathrm{C}_{\mathrm{T}}$ voltage to the oscillator valley $(1.6 \mathrm{~V})$ and peak reference ( 3.6 V ) values. A latch $\left(\mathrm{L}_{\text {disch }}\right)$ memorizes the oscillator state.

In addition to the charge and discharge cycles, a third state can exist. This phase can be produced when, at the end of the discharge phase, the oscillator has to wait for a synchronization or demagnetization pulse before restarting. During this delay, the $\mathrm{C}_{\mathrm{T}}$ voltage must remain equal to the oscillator valley value ( $\simeq 1.6 \mathrm{~V}$ ). So, a third regulated current source $\mathrm{I}_{\text {Regul }}$ controlled by $\mathrm{C}_{\mathrm{OSC}}$ Regul, is connected to $\mathrm{C}_{\mathrm{T}}$ in order to perfectly compensate the ( $0.4 \mathrm{I}_{\mathrm{ref}}$ ) current source that permanently supplies $\mathrm{C}_{\mathrm{T}}$.

The maximum duty cycle is $80 \%$. Indeed, the on-time is allowed only during the oscillator capacitor charge.

Consequently:
$\mathrm{T}_{\text {charge }}=\mathrm{C}_{\mathrm{T}} \times \Delta \mathrm{V} / \mathrm{I}_{\text {charge }}$
$\mathrm{T}_{\text {discharge }}=\mathrm{C}_{\mathrm{T}} \times \Delta \mathrm{V} / \mathrm{I}_{\text {discharge }}$
where:
$\mathrm{T}_{\text {charge }}$ is the oscillator charge time
$\Delta \mathrm{V}$ is the oscillator peak-to-peak value
$\mathrm{I}_{\text {charge }}$ is the oscillator charge current and
$\mathrm{T}_{\text {discharge }}$ is the oscillator discharge time
$\mathrm{I}_{\text {discharge }}$ is the oscillator discharge current
So, as $\mathrm{f}_{\mathrm{S}}=1 /\left(\mathrm{T}_{\text {charge }}+\mathrm{T}_{\text {discharge }}\right)$ when the Regul arrangement is not activated, the operating frequency can be obtained from the graph in Figure 1.
NOTE: The output is disabled by the signal $V_{\text {OSC prot }}$ when $\mathrm{V}_{\mathrm{CT}}$ is lower than 1.0 V (refer to Figure 30).

## Synchronization and Demagnetization Blocks

To enable the output, the L ${ }_{\text {OSC }}$ latch complementary output must be low. Reset is activated by the $\mathrm{L}_{\text {disch }}$ output during the discharge phase. To restart, the L OSC has to be set (refer to Figure 34). To perform this, the demagnetization signal and the synchronization must be low.

## - Synchronization:

The synchronization block consists of two comparators that compare the synchronization signal (external) to 0.7 and 3.7 V (typical values). The comparators' outputs are connected to the input of an AND gate so that the final output of the block should be:

- high when $0.7<$ SYNC $<3.7 \mathrm{~V}$
- low in the other cases.

As a low level is necessary to enable the output, synchronized low level pulses have to be generated on the output of the synchronization block. If synchronization is not required, the Pin 9 must be connected to the ground.


Figure 36. Synchronization

## - Demagnetization:

In flyback applications, a good means to detect magnetic saturation of the transformer core, or demagnetization, consists in using the auxiliary winding voltage. This voltage is:

- negative during the on-time,
- positive during the off-time,
- equal to zero for the dead-time with generally some ringing (refer to Figure 37).
That is why, the MC44603A demagnetization detection consists of a comparator that can compare the auxiliary winding voltage to a reference that is typically equal to 65 mV .


Figure 37. Demagnetization Detection

A diode D has been incorporated to clamp the positive applied voltages while an active clamping system limits the negative voltages to typically -0.33 V . This negative clamp level is sufficient to avoid the substrate diode switching on.
In addition to the comparator, a latch system has been incorporated in order to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output) (refer to Figure 38). This process prevents ringing on the signal at Pin 8 from disrupting the demagnetization detection. This results in a very accurate demagnetization detection.

The demagnetization block output is also directly connected to the output, disabling it during the demagnetization phase (refer to Figure 33).
NOTE: The demagnetization detection can be inhibited by connecting Pin 8 to the ground.


Figure 38. Demagnetization Block

## Standby

## - Power Losses in a Classical Flyback Structure



Figure 39. Power Losses in a Classical Flyback Structure

In a classical flyback (as depicted in Figure 39), the standby losses mainly consist of the energy waste due to:

- the startup resistor $\mathrm{R}_{\text {startup }} \quad \rightarrow \mathrm{P}_{\text {startup }}$
- the consumption of the IC and the power switch control $\rightarrow P_{\text {control }}$
- the inrush current limitation resistor $\mathrm{R}_{\mathrm{ICL}} \rightarrow \mathrm{P}_{\mathrm{ICL}}$
- the switching losses in the power switch $\rightarrow \mathrm{P}_{\mathrm{SW}}$
- the snubber and clamping network $\quad \rightarrow \mathrm{P}_{\mathrm{SN}-\mathrm{CLN}}$
$P_{\text {startup }}$ is nearly constant and is equal to:

$$
\left(\left(\mathrm{V}_{\mathrm{in}}-\mathrm{V}_{\mathrm{CC}}\right)^{2} / \mathrm{R}_{\text {startup }}\right)
$$

$\mathrm{P}_{\mathrm{ICL}}$ only depends on the current drawn from the mains. Losses can be considered constant. This waste of energy decreases when the standby losses are reduced.
$P_{\text {control }}$ increases when the oscillator frequency is increased (each switching requires some energy to turn on the power switch).
$\mathrm{P}_{\mathrm{SW}}$ and $\mathrm{P}_{\mathrm{SN}-\mathrm{CLN}}$ are proportional to the switching frequency.

Consequently, standby losses can be minimized by decreasing the switching frequency as much as possible.

The MC44603A was designed to operate at a standby frequency lower than the normal working one.

## - Standby Power Calculations with MC44603A

During a switching period, the energy drawn by the transformer during the on-time to be transferred to the output during the off-time, is equal to:

$$
E=\frac{1}{2} \times L \times l_{p k}^{2}
$$

where:

- L is the transformer primary inductor,
$-l_{p k}$ is the inductor peak current.
Input power is labelled $\mathrm{P}_{\mathrm{in}}$ :

$$
P_{\text {in }}=0.5 \times L \times l_{p k}{ }^{2} \times f \text { S }
$$

where $f_{S}$ is the normal working switching frequency.
Also,

$$
\mathrm{I}_{\mathrm{pk}}=\frac{\mathrm{V}_{\mathrm{CS}}}{\mathrm{R}_{\mathrm{S}}}
$$

where $\mathrm{R}_{\mathrm{S}}$ is the resistor used to measure the power switch current.

Thus, the input power is proportional to $\mathrm{V}_{\mathrm{CS}}{ }^{2}\left(\mathrm{~V}_{\mathrm{CS}}\right.$ being the internal current sense comparator input).

That is why the standby detection is performed by creating a $\mathrm{V}_{\mathrm{CS}}$ threshold. An internal current source ( $0.4 \times \mathrm{I}_{\mathrm{ref}}$ ) sets the threshold level by connecting a resistor to Pin 12.
As depicted in Figure 40, the standby comparator noninverting input voltage is typically equal to $\left(3.0 \times \mathrm{V}_{\mathrm{CS}}+\right.$ $\left.V_{F}\right)$ while the inverter input value is $\left(V_{R} P\right.$ Stby $\left.+V_{F}\right)$.


Figure 40. Standby

The $V_{C S}$ threshold level is typically equal to $\left[\left(\mathrm{V}_{\mathrm{R}}\right.\right.$ P Stby $\left.) / 3\right]$ and if the corresponding power threshold is labelled $\mathrm{P}_{\mathrm{thL}}$ :

$$
P_{\text {thL }}=0.5 \times L \times\left(\frac{V_{R} P \text { Stby }}{3.0 R_{S}}\right)^{2} \times \mathrm{fs}
$$

And as:

$$
\begin{array}{r}
V_{R ~ P ~ S t b y}=R_{\text {P Stby }} \times 0.4 \times I_{\text {ref }} \\
=R_{R} P \text { Stby } \times 0.4 \times \frac{V_{\text {ref }}}{R_{\text {ref }}} \\
R_{\text {R Stby }}=\frac{10.6 \times R_{\text {S }} \times R_{\text {ref }}}{V_{\text {ref }}} \times \sqrt{\frac{P_{\text {thL }}}{L \times f S}}
\end{array}
$$

Thus, when the power drawn by the converter decreases, $\mathrm{V}_{\mathrm{CS}}$ decreases and when $\mathrm{V}_{\mathrm{CS}}$ becomes lower than [ $\mathrm{V}_{\text {CS-th }}$ $\mathrm{x}\left(\mathrm{V}_{\mathrm{R}}\right.$ P Stby $\left.) / 3\right]$, the standby mode is activated. This results in an oscillator discharge current reduction in order to increase the oscillator period and to diminish the switching frequency. As it is represented in Figure 40, the ( $0.8 \times \mathrm{I}_{\mathrm{ref}}$ ) current source is disconnected and is replaced by a lower value one ( $0.25 \times \mathrm{I}_{\mathrm{F} \text { Stby }}$ ).
Where: $\mathrm{I}_{\mathrm{F} \text { Stby }}=\mathrm{V}_{\text {ref }} / \mathrm{R}_{\mathrm{F} \text { Stby }}$
In order to prevent undesired mode switching when power is close to the threshold value, a hysteresis that is
proportional to $\mathrm{V}_{\mathrm{R}}$ P Stby is incorporated creating a second $\mathrm{V}_{\mathrm{CS}}$ threshold level that is equal to [2.5 $\times\left(\mathrm{V}_{\mathrm{R}} \mathrm{P}\right.$ Stby $\left.) / 3\right]$. When the standby comparator output is high, a second current source ( $0.6 \mathrm{x}_{\mathrm{ref}}$ ) is connected to Pin 12 .

Finally, the standby mode function can be shown graphically in Figure 41.


Figure 41. Dynamic Mode Change
This curve shows that there are two power threshold levels:

- the low one:

$$
P_{\text {thL }} \text { fixed by } V_{R} \text { P Stby }
$$

- the high one:

$$
\begin{aligned}
& P_{\text {thH }}=(2.5)^{2} \times P_{\text {thL }} \times \frac{\mathrm{f}_{\text {thy }}}{\mathrm{f}_{\mathrm{S}}} \\
& P_{\mathrm{thH}}=6.25 \times \mathrm{P}_{\mathrm{thL}} \times \frac{\mathrm{f}_{\mathrm{Stby}}}{\mathrm{f}_{\mathrm{S}}}
\end{aligned}
$$

## Maximum Duty Cycle and Soft-Start Control

Maximum duty cycle can be limited to values less than $80 \%$ by utilizing the $\mathrm{D}_{\text {max }}$ and soft-start control. As depicted in Figure 42, the Pin 11 voltage is compared to the oscillator sawtooth.


Figure 42. $\mathrm{D}_{\text {max }}$ and Soft-Start


Figure 43. Maximum Duty Cycle Control

Using the internal current source ( $0.4 \mathrm{I}_{\mathrm{ref}}$ ), the Pin 11 voltage can easily be set by connecting a resistor to this pin.

If a capacitor is connected to Pin 11, the voltage increases from 0 to its maximum value progressively (refer to Figure 44), thereby, implementing a soft-start. The soft-start capacitor is discharged internally when the $\mathrm{V}_{\mathrm{CC}}$ (Pin 1) voltage drops below 9.0 V .


Figure 44. Different Possible Uses of Pin 11
If no external component is connected to Pin 11, an internal zener diode clamps the Pin 11 voltage to a value $\mathrm{V}_{\mathrm{Z}}$ that is higher than the oscillator peak value, disabling soft-start and maximum duty cycle limitation.

## Foldback

As depicted in Figures 32 and 48, the foldback input (Pin 5) can be used to reduce the maximum $V_{C S}$ value, providing foldback protection. The foldback arrangement is a programmable peak current limitation.

If the output load is increased, the required converter peak current becomes higher and $\mathrm{V}_{\mathrm{CS}}$ increases until it reaches its maximum value (normally, $\mathrm{V}_{\mathrm{CS} \text { max }}=1.0 \mathrm{~V}$ ).

Then, if the output load keeps on increasing, the system is unable to supply enough energy to maintain the output voltages in regulation. Consequently, the decreasing output can be applied to Pin 5, in order to limit the maximum peak current. In this way, the well known foldback characteristic can be obtained (refer to Figure 45).


Figure 45. Foldback Characteristic

NOTE: Foldback is disabled by connecting Pin 5 to $\mathrm{V}_{\mathrm{CC}}$.

## Overvoltage Protection

The overvoltage arrangement consists of a comparator that compares the Pin 6 voltage to $\mathrm{V}_{\text {ref }}(2.5 \mathrm{~V})$ (refer to Figure 46).

If no external component is connected to Pin 6, the comparator noninverting input voltage is nearly equal to:

$$
\left(\frac{2.0 \mathrm{k} \Omega}{11.6 \mathrm{k} \Omega+2.0 \mathrm{k} \Omega}\right) \times \mathrm{V}_{\mathrm{CC}}
$$

The comparator output is high when:

$$
\begin{gathered}
\left(\frac{2.0 \mathrm{k} \Omega}{11.6 \mathrm{k} \Omega+2.0 \mathrm{k} \Omega}\right) \times \mathrm{V}_{\mathrm{CC}} \geq 2.5 \mathrm{~V} \\
\Leftrightarrow \mathrm{~V}_{\mathrm{CC}} \geq 17 \mathrm{~V}
\end{gathered}
$$

A delay latch $(2.0 \mu \mathrm{~s})$ is incorporated in order to sense overvoltages that last at least $2.0 \mu \mathrm{~s}$.

If this condition is achieved, $\mathrm{V}_{\mathrm{OVP}}$ out, the delay latch output, becomes high. As this level is brought back to the input through an OR gate, $\mathrm{V}_{\text {OVP out }}$ remains high (disabling the IC output) until $\mathrm{V}_{\text {ref }}$ is disabled.

Consequently, when an overvoltage longer than $2.0 \mu \mathrm{~s}$ is detected, the output is disabled until $\mathrm{V}_{\mathrm{CC}}$ is removed and then re-applied.

The $\mathrm{V}_{\mathrm{CC}}$ is connected after $\mathrm{V}_{\text {ref }}$ has reached steady state in order to limit the circuit startup consumption.

The overvoltage section is enabled $5.0 \mu$ s after the regulator has started to allow the reference $\mathrm{V}_{\text {ref }}$ to stabilize.

By connecting an external resistor to Pin 6, the threshold $\mathrm{V}_{\mathrm{CC}}$ level can be changed.


Figure 46. Overvoltage Protection

## Undervoltage Lockout Section



Figure 47. $\mathrm{V}_{\mathrm{CC}}$ Management
As depicted in Figure 47, an undervoltage lockout has been incorporated to garantee that the IC is fully functional before allowing system operation.

This block particularly, produces $\mathrm{V}_{\text {ref }}$ (Pin 16 voltage) and $\mathrm{I}_{\text {ref }}$ that is determined by the resistor $\mathrm{R}_{\text {ref }}$ connected between Pin 16 and the ground:

$$
I_{\text {ref }}=\frac{V_{\text {ref }}}{R_{\text {ref }}} \text { where } V_{\text {ref }}=2.5 \mathrm{~V} \text { (typically) }
$$

Another resistor is connected to the Reference Block: $\mathrm{R}_{\mathrm{F} \text { Stby }}$ that is used to fix the standby frequency.

In addition to this, $\mathrm{V}_{\mathrm{CC}}$ is compared to a second threshold level that is nearly equal to $9.0 \mathrm{~V}\left(\mathrm{~V}_{\text {disable1 }}\right)$. UVLO1 is generated to reset the maximum duty cycle and soft-start block disabling the output stage as soon as $\mathrm{V}_{\mathrm{CC}}$ becomes lower than $\mathrm{V}_{\text {disable1 }}$. In this way, the circuit is reset and made ready for the next startup, before the reference block is disabled (refer to Figure 29). Finally, the upper limit for the minimum normal operating voltage is 9.4 V (maximum value of $\mathrm{V}_{\text {disable1 }}$ ) and so the minimum hysteresis is 4.2 V . $\left(\left(\mathrm{V}_{\text {stup-th }}\right)_{\text {min }}=13.6 \mathrm{~V}\right)$.

The large hysteresis and the low startup current of the MC44603A make it ideally suited for off-line converter applications where efficient bootstrap startup techniques are required.


* Diode D15 is required if the negative current into the output pin exceeds 15 mA .

Figure 48. 250 W Input Power Off-Line Flyback Converter with MOSFET Switch

## MC44603A

## 250 W Input Power Fly-Back Converter <br> 185 V - 270 V Mains Range <br> MC44603AP \& MTP6N60E

| Tests | Conditions | Results |
| :---: | :---: | :---: |
| Line Regulation $\begin{gathered} 150 \mathrm{~V} \\ 30 \mathrm{~V} \\ 14 \mathrm{~V} \\ 7.0 \mathrm{~V} \end{gathered}$ | $\begin{aligned} & \mathrm{V}_{\text {in }}=185 \mathrm{Vac} \text { to } 270 \mathrm{Vac} \\ & \mathrm{~F}_{\text {mains }}=50 \mathrm{~Hz} \\ & \mathrm{I}_{\text {out }}=0.6 \mathrm{~A} \\ & \mathrm{I}_{\text {out }}=2.0 \mathrm{~A} \\ & \mathrm{I}_{\text {out }}=2.0 \mathrm{~A} \\ & \mathrm{I}_{\text {out }}=2.0 \mathrm{~A} \end{aligned}$ | $\begin{aligned} & 10 \mathrm{mV} \\ & 10 \mathrm{mV} \\ & 10 \mathrm{mV} \\ & 20 \mathrm{mV} \end{aligned}$ |
| Load Regulation 150 V | $\begin{aligned} & \mathrm{V}_{\text {in }}=220 \mathrm{Vac} \\ & \mathrm{I}_{\text {out }}=0.3 \mathrm{~A} \text { to } 0.6 \mathrm{~A} \end{aligned}$ | 50 mV |
| Cross Regulation $150 \mathrm{~V}$ | $\begin{aligned} & \mathrm{V}_{\text {in }}=220 \mathrm{Vac} \\ & \mathrm{I}_{\text {out }}(150 \mathrm{~V})=0.6 \mathrm{~A} \\ & \mathrm{I}_{\text {out }}(30 \mathrm{~V})=0 \mathrm{~A} \text { to } 2.0 \mathrm{~A} \\ & \mathrm{I}_{\text {out }}(14 \mathrm{~V})=2.0 \mathrm{~A} \\ & \mathrm{I}_{\text {out }}(7.0 \mathrm{~V})=2.0 \mathrm{~A} \end{aligned}$ | $<1.0 \mathrm{mV}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=220 \mathrm{Vac}, \mathrm{P}_{\text {in }}=250 \mathrm{~W}$ | 81\% |
| Standby Mode $P$ input <br> Switching Frequency | $\mathrm{V}_{\text {in }}=220 \mathrm{Vac}, \mathrm{P}_{\text {out }}=0 \mathrm{~W}$ | 3.3 W <br> 20 kHz fully stable |
| Output Short Circuit | $\mathrm{P}_{\text {out }(\text { max }}=270 \mathrm{~W}$ | Safe on all outputs |
| Startup | $\mathrm{P}_{\text {in }}=250 \mathrm{~W}$ | $\mathrm{Vac}=160 \mathrm{~V}$ |

## MC44604

## High Safety Pulsed Mode Standby GreenLine ${ }^{\text {TM }}$ PWM Controller

The MC44604 is an enhanced high performance controller that is specifically designed for off-line and dc-to-dc converter applications. Its high current totem pole output is ideally suited for driving a power MOSFET.

The MC44604 is an evolution of the MC44603A. Like the MC44603A, the MC44604 has been optimized to operate with universal ac mains voltage from 80 V to 280 V . It also offers enhanced safety and reliable power management thanks to its protection features (foldback, overvoltage detection, soft-start, accurate demagnetization detection).

In addition, the MC44604 offers a new efficient way to reduce the standby operating power by means of a so-called pulsed mode standby operation of the converter, significantly reducing the converter consumption in standby mode.

## Current Mode Controller

- Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Oscillator with Precise Frequency Control


## High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis


## Safety/Protection Features

- Overvoltage Protection Facility Against Open Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft-Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference


## GreenLine ${ }^{T \mathrm{M}}$ Controller $^{\mathrm{TM}}$

- Low Start-Up and Operating Current
- Pulsed Mode Standby for Low Standby Losses
- Low dV/dT for Low EMI

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com

(Top View)

ORDERING INFORMATION
ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC44604P | PDIP-16 | 25 Units/Rail |



## MC44604

## Block Diagram



MAXIMUM RATINGS

| Rating | Pin \# | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Total Power Supply and Zener Current |  | $\left(\mathrm{I}_{\mathrm{Cc}}+\mathrm{I}_{\mathrm{z}}\right.$ ) | 30 | mA |
| Output Supply Voltage with Respect to Ground | $\begin{aligned} & 2 \\ & 1 \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{C}} \\ & \mathrm{~V}_{\mathrm{CC}} \end{aligned}$ | 18 | V |
| Output Current* <br> Source <br> Sink | 3 | $\mathrm{I}_{\mathrm{O}}$ (Source) $\mathrm{I}_{\text {(Sink) }}$ | $\begin{gathered} -750 \\ 750 \end{gathered}$ | mA |
| Output Energy (Capacitive Load per Cycle) |  | W | 5.0 | $\mu \mathrm{J}$ |
| Soft-Start | 11 | $\mathrm{V}_{S S}$ | -0.3 to 2.2 | V |
| Clamp Error Amp Input | 12 | $\mathrm{V}_{\text {CLEA }}$ | -0.3 to 4.5 | V |
| Foldback Input, Stand-by Management |  |  | -0.3 to $\mathrm{V}_{\mathrm{CC}}+0.3$ | V |
| Overvoltage Protection, Current Sense Input, $\mathrm{R}_{\text {ref }}$, Error Amp Input, Error Amp Output, $\mathrm{C}_{\mathrm{T}}$, Stand-by Current Set |  | $V_{\text {in }}$ | -0.3 to 5.5 | V |
| Demagnetization Detection Input Current Source <br> Sink | 8 | $I_{\text {demag-ib (Source) }}$ $I_{\text {demag-ib (Sink) }}$ | $\begin{gathered} -4.0 \\ 10 \end{gathered}$ | mA |
| Error Amplifier Output Sink Current | 13 | $\mathrm{I}_{\mathrm{E} / \mathrm{A}}$ (Sink) | 20 | mA |
| Power Dissipation and Thermal Characteristics Maximum Power Dissipation at $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air |  | $P_{D}$ $\mathrm{R}_{\theta \mathrm{JA}}$ | $\begin{aligned} & 0.6 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature |  | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature |  | $\mathrm{T}_{\text {A }}$ | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |

*Maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$ [Note 1], $\mathrm{R}_{\text {ref }}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=820 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ [Note 2], unless otherwise noted.)

| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OUTPUT SECTION (Note 3) |  |  |  |  |  |  |
| $\begin{array}{ll} \hline \begin{array}{l} \text { Output Voltage* } \\ \text { Low Level Drop Voltage } \\ \left(\begin{array}{l} \left(I_{\text {Sink }}=100 \mathrm{~mA}\right) \\ \left(I_{\text {Sink }}=500 \mathrm{~mA}\right) \end{array}\right. \\ \text { High Level Drop Voltage }\left(I_{\text {Source }}=200 \mathrm{~mA}\right) \\ \\ \\ \left(I_{\text {Source }}=500 \mathrm{~mA}\right) \end{array} \end{array}$ | 3 | $\begin{aligned} & \mathrm{v}_{\mathrm{OL}} \\ & \mathrm{v}_{\mathrm{OH}} \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.4 \\ & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 1.2 \\ & 2.0 \\ & 2.0 \\ & 2.7 \end{aligned}$ | V |
| Output Voltage During Initialization Phase $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=0 \text { to } 1.0 \mathrm{~V}, I_{\text {Sink }}=10 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=1.0 \text { to } 5.0 \mathrm{~V}, I_{\text {Sink }}=100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \text { to } 13 \mathrm{~V}, I_{\text {Sink }}=1.0 \mathrm{~mA} \end{aligned}$ | 3 | $\mathrm{V}_{\text {OL }}$ | - | $\begin{aligned} & -\overline{1} \\ & 0.1 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.0 \\ & 1.0 \end{aligned}$ | V |
| Output Voltage Rising Edge Slew-Rate ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | 3 | dVo/dT | - | 300 | - | V/us |
| Output Voltage Falling Edge Slew-Rate ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ ) | 3 | dVo/dT | - | -300 | - | V/us |

## ERROR AMPLIFIER SECTION

| Voltage Feedback Input $\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=2.5 \mathrm{~V}\right)$ | 14 | $\mathrm{~V}_{\mathrm{FB}}$ | 2.4 | 2.5 | 2.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{FB}}=2.5 \mathrm{~V}\right)$ | 14 | $\mathrm{I}_{\mathrm{FB}-\mathrm{ib}}$ | -2.0 | -0.6 | - | $\mu \mathrm{A}$ |
| Open Loop Voltage Gain $\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=2.0 \mathrm{~V}\right.$ to 4.0 V$)$ |  | $\mathrm{A}_{\mathrm{VOL}}$ | 65 | 70 | - | dB |
| Unity Gain Bandwidth | BW |  |  |  | MHz |  |
| $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  |  | - | - | - |  |
| Voltage Feedback Input Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 15 V$)$ | 14 | $\mathrm{~V}_{\mathrm{FB}} \mathrm{Cline-reg}$ | -10 | - | 10 | mV |

${ }^{*} \mathrm{~V}_{\mathrm{C}}$ must be greater than 5.0 V .

1. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V .
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. No output signal when the Error Amplifier is in Low State, i.e., $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$ [Note 1], $\mathrm{R}_{\text {ref }}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=820 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ [Note 2], unless otherwise noted.)

| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER SECTION (continued) |  |  |  |  |  |  |
| $\begin{aligned} & \text { Output Current } \\ & \text { Sink }\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \\ & \text { Source }\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 13 | $I_{\text {Sink }}$ <br> ISource | $\begin{array}{r} 2.0 \\ -2.0 \end{array}$ | $12$ | $-0.2$ | mA |
| Output Voltage Swing <br> High State ( $\mathrm{I}_{\mathrm{E} / \mathrm{A}}$ out $($ source $)=0.5 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) <br> Low State ( $\mathrm{E}_{\mathrm{E} / \mathrm{A} \text { out }(\text { sink })}=0.33 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) | 13 | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $5.5$ | $\begin{aligned} & 6.5 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 1.1 \\ & \hline \end{aligned}$ | V |

## REFERENCE SECTION

| Reference Output Voltage $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 15 V$)$ | 16 | $\mathrm{~V}_{\text {ref }}$ | 2.4 | 2.5 | 2.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Reference Current Range $\left(\mathrm{I}_{\text {ref }}=\mathrm{V}_{\text {ref }} / \mathrm{R}_{\text {ref, }} \mathrm{R}=5.0 \mathrm{k}\right.$ to $\left.25 \mathrm{k} \Omega\right)$ | 16 | $\mathrm{I}_{\text {ref }}$ | -500 | - | -100 | $\mu \mathrm{~A}$ |
| Reference Voltage Over $\mathrm{I}_{\text {ref }}$ Range |  | $\Delta \mathrm{V}_{\text {ref }}$ | -40 | - | 40 | mV |

OSCILLATOR SECTION

| Frequency <br> $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ <br> $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  | FOSC |  |  | kHz |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 15 V$)$ |  | 40.5 <br> 40 | 46 <br> - | 48.5 <br> 49 |  |  |
| Frequency Change with Temperature $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ |  | $\Delta \mathrm{Fosc}^{\circ} / \Delta \mathrm{V}$ | - | 0.05 | - | $\% / \mathrm{V}$ |
| Oscillator Voltage Swing (Peak-to-Peak) | $\Delta \mathrm{FOSC}^{\prime} / \Delta \mathrm{T}$ | - | 0.05 | - | $\% /{ }^{\circ} \mathrm{C}$ |  |
| Ratio Charge Current/Reference Current $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ |  | $\mathrm{I}_{\text {charge }} / \mathrm{I}_{\text {ref }}$ | 0.35 | - | 0.43 | - |
| Fixed Maximum Duty Cycle $=\mathrm{I}_{\text {discharge }} /\left(\mathrm{I}_{\text {discharge }}+\mathrm{I}_{\text {charge }}\right)$ |  | D | 78 | 80 | 82 | $\%$ |

UNDERVOLTAGE LOCKOUT SECTION

| Start-up Threshold | 1 | $\mathrm{~V}_{\text {stup-th }}$ | 13.6 | 14.5 | 15.4 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Disable Voltage After Threshold Turn-On | 1 | $\mathrm{~V}_{\text {disable1 }}$ |  |  |  | V |
| $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ |  |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  |  | 8.6 | 9.0 | 9.4 |  |
| Disable Voltage After Threshold Turn-On | 1 | $\mathrm{~V}_{\text {disable2 }}$ | 7.0 | 7.5 | 8.0 | V |
| Delta $\mathrm{V}_{\mathrm{CC}}$ During Standby $\left(\mathrm{V}_{\text {stup-th }}-\mathrm{V}_{\text {disable2 }}\right)$ <br> $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ} \mathrm{C}\right.$ to $\left.85^{\circ} \mathrm{C}\right)$ | 1 | $\mathrm{V}_{\text {stup-th }}$ <br> $-\mathrm{V}_{\text {disable2 }}$ | 1.8 | 2.0 | 2.2 | V |

DEMAGNETIZATION DETECTION SECTION

| Demagnetization Detect Input <br> Demagnetization Comparator Threshold ( $\mathrm{V}_{\text {pin8 }}$ Decreasing) <br> Propagation Delay (Input to Output, Low to High) <br> Input Bias Current ( $\mathrm{V}_{\text {demag }}=65 \mathrm{mV}$ ) | 8 | $V_{\text {demag-th }}$ <br> $I_{\text {demag-lb }}$ | $\begin{gathered} 50 \\ - \\ -0.5 \end{gathered}$ | $\begin{gathered} 65 \\ 0.25 \end{gathered}$ | $80$ | $\begin{gathered} \mathrm{mV} \\ \mu \mathrm{~s} \\ \mu \mathrm{~A} \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Negative Clamp Level ( $\mathrm{l}_{\text {demag }}=-2.0 \mathrm{~mA}$ ) |  | $\mathrm{C}_{\mathrm{L} \text { (neg) }}$ | - | -0.38 | - | V |
| Positive Clamp Level ( $\mathrm{I}_{\text {demag }}=+2.0 \mathrm{~mA}$ ) |  | $\mathrm{C}_{\mathrm{L} \text { (pos) }}$ | - | 0.72 | - | V |

## SOFT-START SECTION

| $\begin{aligned} & \text { Ratio Charge Current/ } / I_{\text {ref }} \\ & \mathrm{T}_{\mathrm{A}}=0^{\circ} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ |  | $\mathrm{l}_{\text {ss(ch) }} / I_{\text {ref }}$ | $\begin{array}{r} 0.37 \\ 0.36 \\ \hline \end{array}$ |  | $\begin{aligned} & 0.43 \\ & 0.44 \end{aligned}$ | - |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Discharge Current ( $\mathrm{V}_{\text {soft-start }}=1.0 \mathrm{~V}$ ) | 11 | $\mathrm{I}_{\text {discharge }}$ | 1.5 | 5.0 | - | mA |
| Clamp Level |  | $\mathrm{V}_{\mathrm{ss}(\mathrm{CL})}$ | 2.2 | 2.4 | 2.6 | V |
| $\left.\begin{array}{l} \text { Duty Cycle }\left(\mathrm{R}_{\text {soft-start }}=12 \mathrm{k} \Omega\right) \\ \\ \left(\mathrm{V}_{\text {soft-start }}(\text { pin11 })\right. \end{array}=0.1 \mathrm{~V}\right)$ |  | $\begin{aligned} & \mathrm{D}_{\text {soft-start } 12 \mathrm{k}} \\ & \mathrm{D}_{\text {soft-start }} \end{aligned}$ | 36 | 42 | $\begin{gathered} 49 \\ 0 \end{gathered}$ | \% |

1. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V .
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$ [Note 1], $\mathrm{R}_{\text {ref }}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=820 \mathrm{pF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ [Note 2], unless otherwise noted.)

| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CURRENT SENSE SECTION |  |  |  |  |  |  |
| Maximum Current Sense Input Threshold $\left(\mathrm{V}_{\text {Feedback }}\left(\right.\right.$ pin14) $=2.3 \mathrm{~V}$ and $\left.\mathrm{V}_{\text {foldback (pin6) }}=1.2 \mathrm{~V}\right)$ | 7 | $\mathrm{V}_{\text {cs-th }}$ | 0.93 | 0.96 | 1.00 | V |
| Input Bias Current | 7 | $\mathrm{I}_{\text {cs-ib }}$ | -10 | -2.0 | - | $\mu \mathrm{A}$ |
| Propagation Delay* in Normal Mode <br> in Standby Mode |  | tcs-NM <br> tcs-stby | - | $\begin{aligned} & \hline 120 \\ & 120 \end{aligned}$ | $\begin{aligned} & \hline 200 \\ & 200 \end{aligned}$ | ns |

*Current Sense Input to Output at $\mathrm{V}_{\mathrm{TH}}$ of MOS transistor $=3.0 \mathrm{~V}$.
OVERVOLTAGE SECTION

| Protection Threshold Level on $\mathrm{V}_{\text {OVP }}$ | 6 | $\mathrm{~V}_{\text {OVP-th }}$ | 2.42 | 2.5 | 2.58 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay (V $\mathrm{V}_{\text {OPP }}>2.58 \mathrm{~V}$ to $\mathrm{V}_{\text {out }}$ Low $)$ |  |  | 1.0 | - | 3.0 | $\mu \mathrm{~s}$ |
| Protection Level on $\mathrm{V}_{\mathrm{CC}}$ |  | $\mathrm{V}_{\mathrm{CC} \text { prot }}$ |  |  |  | V |
| $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ |  |  | 16.1 | 17 | 17.9 |  |
| $\mathrm{~T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  |  | 15.9 | - | 18.1 |  |
| Input Resistance |  | - |  |  |  | $\mathrm{k} \Omega$ |
| $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ |  |  | 1.5 | 2.0 | 3.0 |  |
| $\mathrm{~T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  |  | 1.4 | - | 3.4 |  |

## FOLDBACK SECTION (Note 3)

| Current Sense Voltage Threshold ( $\mathrm{V}_{\text {foldback ( }}$ (pin5) $=0.9 \mathrm{~V}$ ) | 5 | $\mathrm{V}_{\text {cs-th }}$ | 0.84 | 0.88 | 0.89 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Foldback Input Bias Current ( $\mathrm{V}_{\text {foldback }}($ (pin5) $=0 \mathrm{~V}$ ) | 5 | $I_{\text {foldback-lb }}$ | -6.0 | -2.0 | - | $\mu \mathrm{A}$ |

CLAMP ERROR AMPLIFIER INPUT

| Clamp Level (@I = 30 mA) | 12 | Vcl | 4.5 | 4.7 | 4.9 | V |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

STANDBY PULSED MODE SECTION

| Standby Initialization Current Ratio (S1 closed) | 15 | $\mathrm{I}_{\text {init }} / I_{\text {ref }}$ | 126 | 140 | 154 | - |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Minimum Initialization Current Pulse Width* |  | $\mathrm{T}_{\text {init }}$ | - | - | 1.0 | $\mu \mathrm{~s}$ |
| Standby On Detection Current Ratio | 15 | $\mathrm{I}_{\text {det }} / I_{\text {ref }}$ | 0.34 | 0.38 | 0.42 | - |
| Standby Regulation Current Ratio | 15 | $\mathrm{I}_{\text {reg }} / \mathrm{I}_{\text {ref }}$ | 18 | 20.5 | 23 | - |
| Standby <br> $0 \mathrm{Vias} \mathrm{Current}(S 1$ and <br> < $\left.\mathrm{V}_{\text {pin15 }}<\mathrm{V}_{\text {stup-th }}\right)^{* *}$ | 15 | $\mathrm{I}_{\text {stby-ib }}$ | -1.0 | - | 2.0 | $\mu \mathrm{~A}$ |

* This is the minimum time during which the pin 15 current must be higher than $\mathrm{l}_{\text {init }}$ to enable the detection of the transition normal to standby mode. ${ }^{* *}$ Tested using $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, 9.0 \mathrm{~V}, 13.5 \mathrm{~V}$, the MC44604 being off.


## STANDBY CURRENT SET

| Peak Standby Current Setting Ratio | 9 |  |  |  |  | - |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ |  | $\mathrm{I}_{\mathrm{pk}-\text { stby }} / \mathrm{I}_{\text {ref }}$ | 0.37 | 0.4 | 0.43 |  |
| $\mathrm{~T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ |  | - | 0.36 | 0.4 | 0.44 |  |
| Standby Current Sense Threshold Ratio |  |  |  |  |  |  |

${ }^{*}$ Tested using $\mathrm{V}_{\text {pin9 }}=0.2 \mathrm{~V}, 0.4 \mathrm{~V}, 0.6 \mathrm{~V}, 0.8 \mathrm{~V}, 1.0 \mathrm{~V}$.
TOTAL DEVICE

| Power Supply Current <br> Startup* <br> Operating $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ (Note 2) | $\mathrm{I}_{\mathrm{CC}}$ | $16$ | $\begin{aligned} & 0.3 \\ & 20 \end{aligned}$ | $\begin{gathered} 0.45 \\ 24 \end{gathered}$ | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply Zener Voltage ( $\mathrm{I}_{\mathrm{CC}}=25 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{Z}}$ | 18.5 | - | - | V |
| Thermal Shutdown | - | - | 155 | - | ${ }^{\circ} \mathrm{C}$ |

*Tested using $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, 9.0 \mathrm{~V}, 13.5 \mathrm{~V}$, the MC44604 being off.

1. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V .
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

3 . This function can be inhibited by connecting pin 5 to $\mathrm{V}_{\mathrm{CC}}$.


Figure 1. Propagation Delay Current Sense Input vs. Temperature


Figure 3. Current Sense Gain vs. Temperature


Figure 5. Delta $\mathbf{V}_{\mathrm{Cc}}$ During Standby

Figure 2. Propagation Delay Current Sense Input in Standby vs. Temperature


Figure 4. Propagation Delay Current ( $\mathrm{V}_{\text {ovp }}>2.58 \mathrm{~V}$ to $\mathrm{V}_{\text {out }}$ Low) vs. Temperature


Figure 6. Demag Comparator Threshold vs. Temperature


Figure 7. Error Amplifier Gain and Phase vs. Frequency


Figure 9. Oscillator Frequency vs. Temperature


Figure 11. Standby Initialization Current Ratio vs. Temperature


Figure 8. Current Sense Voltage Threshold vs. Temperature


Figure 10. Standby On Detection Current Ratio vs. Temperature


Figure 12. Standby Current Sense Threshold Ratio


Figure 13. Peak Standby Current Setting Ratio vs. Temperature


Figure 15. Sink Output Saturation Voltage vs. Sink Current


Figure 17. Start-up Current vs. $\mathrm{V}_{\mathrm{CC}}$


Figure 14. Standby Regulation Current Ratio vs. Temperature


Figure 16. Source Output Saturation Voltage vs. Source Current


Figure 18. Supply Current vs. Supply Voltage


Figure 19. Start-up Threshold, UVLO1, UVLO2 Voltage vs. Temperature


Figure 21. Clamp Error Amplifier Input vs.


Figure 20. Protection Level on $\mathrm{V}_{\mathrm{Cc}}$ vs. Temperature


Figure 22. Reference Voltage vs. Temperature Temperature


Figure 23. Power Supply Zener Voltage vs. Temperature

| Pin | Name | Pin Description |
| :---: | :---: | :---: |
| 1 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the IC. |
| 2 | $\mathrm{V}_{\mathrm{C}}$ | The output high state, $\mathrm{V}_{\mathrm{OH}}$, is set by the voltage applied to this pin. With a separate connection to the power source, it gives the possibility to set by means of an external resistor the output source current at a different value than the sink current. |
| 3 | Output | The output current capability is suited for driving a power MOSFET. A Bipolar transistor can also be driven for low power applications. The maximum on-time of the duty cycle can last up to $80 \%$ of the switching period. |
| 4 | Gnd | The ground pin is a single return typically connected back to the power source, it is used as control and power ground. |
| 5 | Foldback Input | The foldback function ensures an overload protection. Feeding the foldback input with a portion of the $\mathrm{V}_{\mathrm{CC}}$ voltage ( 1 V max) establishes on the system control loop a foldback characteristic allowing a smoother start-up and a sharper overload protection. The foldback action performs an active current sense clamping reduction. Above 1 V the foldback input is no more active. |
| 6 | Overvoltage Protection | When the overvoltage protection pin receives a voltage greater than 17 V the device gets disabled and requires a complete restart sequence. The overvoltage level is programmable. |
| 7 | Current Sense Input | A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer when operating in current mode. A maximum level of 1 V allows to limit the inductor current either in current or voltage mode of operation. |
| 8 | Demagnetization Detection | A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback energy reservoir. A zero voltage detection corresponds to a complete core demagnetization. The demagnetization detection ensures a discontinuous mode of operation. This function can be inhibited by connecting Pin 8 to GND. |
| 9 | Standby Current Set | Using an external resistor connected to this pin, the standby burst mode peak current can be adjusted. |
| 10 | $\mathrm{C}_{\mathrm{T}}$ | The normal mode oscillator frequency is programmed by the capacitor $\mathrm{C}_{\boldsymbol{T}}$ choice together with the $\mathrm{R}_{\mathrm{ref}}$ resistance value. $\mathrm{C}_{\mathrm{T}}$, connected between pin 10 and GND, generates the oscillator sawtooth. |
| 11 | Soft-Start/D ${ }_{\text {max }} /$ Voltage-Mode | A capacitor or a resistor or a voltage source connected to this pin can temporary or permanently control the effective switching duty-cycle. This pin can be used as a voltage mode control input. By connecting pin 11 to Ground, the MC44604 can be shut down. |
| 12 | Clamp Error Amplifier Input | In normal mode, the current drawn from this pin, is used by the Error Amplifier to perform the regulation. A 4.7 V zener diode clamps the voltage of this pin. |
| 13 | E/A Out | The error amplifier output is made available for loop compensation. |
| 14 | Voltage Feedback | This is the inverting input of the Error Amplifier. It uses a voltage that is built up using the current drawn from the pin 12. |
| 15 | Standby Management | This block is designed to detect the standby mode. It particularly determines if the circuit must work in standby or in normal mode at each start-up. For that, it uses an information given by an external arrangement consisting of an opto-coupler. In standby mode, this block makes the circuit work in the standby configuration, and the current injected in the pin 15 is used to perform the regulation. In normal mode, this pin is internally connected to the pin 12. |
| 16 | $\mathrm{R}_{\text {REF }}$ | The $R_{\text {REF }}$ values fixes the internal reference current which is used to perform the precise oscillator waveform. The current range goes from $100 \mu \mathrm{~A}$ up to $500 \mu \mathrm{~A}$. |

## MC44604

Operating Description Schematics


Figure 24. Switching Off Behavior

## Operating Description Schematics



Figure 25. Starting Behavior and Overvoltage

## Operating Description Schematics



Figure 26. Soft-Start and $D_{\text {max }}$


Figure 27. Demagnetization

## Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 70 dB . The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is $-2.0 \mu \mathrm{~A}$. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diodes drops ( $\approx 1.4 \mathrm{~V}$ ) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 3) when Pin 13 is at its lowest state $\left(\mathrm{V}_{\mathrm{OL}}\right)$. This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current $(0.2 \mathrm{~mA})$ and the required output voltage $\left(\mathrm{VOH}_{\mathrm{OH}}\right)$ to reach the current sense comparator's 1.0 V clamp level:

$$
\mathrm{R}_{\mathrm{f}(\text { min })} \approx \frac{3 \cdot 0(1.0 \mathrm{~V})+1.4 \mathrm{~V}}{0.2 \mathrm{~mA}}=22 \mathrm{k} \Omega
$$



Figure 28. Error Amplifier Compensation

In a preferred embodiment, the feedback signal (current) is drawn from the pin 12 that is connected to the pin 15 in normal mode (Note 1). Using a resistor connected on pin 12, this current generates a voltage that is the input signal of the error amplifier arrangement.

Note 1. The error amplifier is not used in the standby mode regulation.

## Current Sense Comparator and PWM Latch

The MC44604 can operate as a current mode controller and/or as a voltage mode controller. In current mode operation, the MC44604 uses the current sense comparator, where the output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output (Pin 13). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle.

The inductor current is converted to a voltage by inserting the ground referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ in series with the power switch Q1.
In normal mode, this voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$
I_{p k} \approx \frac{V_{(\text {pin13 })}-1.4 \mathrm{~V}}{3 R_{S}}
$$

The Current Sense Comparator threshold is internally clamped to 1.0 V . Therefore the maximum peak switch current is:

$$
I_{\mathrm{pk}(\max )} \approx \frac{1.0 \mathrm{~V}}{\mathrm{R}_{\mathrm{S}}}
$$



Figure 29. Output Totem Pole

## Oscillator

The oscillator is a very accurate sawtooth generator.

## The Sawtooth Generation

In the steady state, the oscillator voltage varies between about 1.6 V and 3.6 V .

Indeed, the sawtooth is obtained by charging and discharging an external capacitor $\mathrm{C}_{\mathrm{T}}$ (Pin 10), using two distinct current sources $=I_{\text {charge }}$ and $\mathrm{I}_{\text {discharge }}$. In fact, $\mathrm{C}_{\mathrm{T}}$ is permanently connected to the charging current source ( $0.4 \mathrm{I}_{\mathrm{ref}}$ ) and so, the discharge current source has to be higher than the charge one to be able to decrease the $\mathrm{C}_{\mathrm{T}}$ voltage. This condition is performed, its value being ( $2 \mathrm{I}_{\mathrm{ref}}$ ).

Two comparators are used to generate the sawtooth. They compare the $\mathrm{C}_{\mathrm{T}}$ voltage to the oscillator valley and peak values. The comparison to the low value enables to detect the end of the discharge phase while the comparison to the high value determines when the charge cycle must be stopped. A latch ( $\mathrm{L}_{\mathrm{DISCH}}$ ) memorizes the oscillator state.


Figure 30. Oscillator
Now, in addition to the charge and discharge cycles, a third state can exist. This phase can be produced when at the end of the discharge phase, the oscillator has to wait for a demagnetization pulse before re-starting. During this delay, the $\mathrm{C}_{\mathrm{T}}$ voltage must remain equal to the oscillator valley value ( $\sim 1.6 \mathrm{~V}$ ). So, a third regulated current source $\mathrm{I}_{\text {REGUL }}$ controlled by $\mathrm{C}_{\text {OSC REGUL }}$, is connected to $\mathrm{C}_{\mathrm{T}}$ in
order to perfectly compensate the ( $0.4 \mathrm{I}_{\mathrm{ref}}$ ) current source that permanently supplies $\mathrm{C}_{\mathrm{T}}$.

On-time is only allowed during the oscillator capacitor charge. So, the maximum duty cycle is $80 \%$. (Note 1 )

The demagnetization condition is taken into account by a second latch ( $\mathrm{L}_{\mathrm{osc}}$ ). (Refer to demagnetization $\S$ for further details.)

## Oscillator Frequency

The oscillator frequency can be deducted using the following equations:

$$
\begin{aligned}
\mathrm{T}_{\text {charge }} & =\mathrm{C}_{\mathrm{T}} \cdot \Delta \mathrm{~V} / \mathrm{I}_{\text {charge }} \\
\mathrm{T}_{\text {discharge }} & =\mathrm{C}_{\mathrm{T}} \cdot \Delta \mathrm{~V} / \mathrm{I}_{\text {discharge }}
\end{aligned}
$$

where:
$\mathrm{T}_{\text {charge }}$ is the oscillator charge time
$\Delta \mathrm{V}$ is the oscillator peak to peak value
$\mathrm{I}_{\text {charge }}$ is the oscillator charge current
and
$\mathrm{T}_{\text {discharge }}$ is the oscillator discharge time
$\mathrm{I}_{\text {discharge }}$ is the oscillator discharge current So, as:
$\mathrm{f}_{\text {osc }}=1 /\left(\mathrm{T}_{\text {charge }}+\mathrm{T}_{\text {discharge }}\right)$ if the REGUL arrangement is not activated, the following equation can be obtained:

$$
\mathrm{f}_{\mathrm{osc}} \sim \frac{0.395}{\mathrm{R}_{\mathrm{ref}} \cdot \mathrm{C}_{\mathrm{T}}}
$$

## Demagnetization Block (Note 2)

To enable the output, the $\mathrm{L}_{\text {osc }}$ latch complementary output must be low. Now, this latch reset is activated by the $\mathrm{L}_{\text {DISCH }}$ output during the discharge phase. So, to restart, the $\mathrm{L}_{\text {osc }}$ has to be set (refer to Figure 30). To perform this, the demagnetization signal must be low.

In a fly-back, a good means to detect the demagnetization consists in using the $\mathrm{V}_{\mathrm{CC}}$ winding voltage. Indeed this voltage is:

- negative during the on-time,
- positive during the off-time,
- equal to zero for the dead-time with generally a ringing (refer to Figure 31).
That is why, the MC44604 demagnetization detection consists of a comparator that can compare the $\mathrm{V}_{\mathrm{CC}}$ winding voltage to a reference that is typically equal to 65 mV .

Note 1 . The output is disabled by the signal $\mathrm{V}_{\text {osc prot }}$ when $\mathrm{V}_{\mathrm{CT}}$ is lower than 1 V. (Refer to Figure 29 and Figure 30.)
Note 2. The demagnetization detection can be inhibited by connecting pin 8 to the ground.


Figure 31. Demagnetization Detection

A diode D has been incorporated to clamp the positive applied voltages while an active clamping system limits the negative voltages to typically -0.33 V . This negative clamp level is sufficient to avoid the substrate diode switching on.

In addition to the comparator, a latch system has been incorporated in order to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output) (refer to Figure 33). This process avoids that any ringing on the signal used on the pin 8 , disrupts the demagnetization detection. Finally, this method results in a very accurate demagnetization detection.

For a higher safety, the demagnetization block output is also directly connected to the output, disabling it during the demagnetization phase (refer to Figure 29).



Figure 33. $\mathrm{D}_{\text {max }}$ and Soft-Start Block Diagram

## Maximum Duty Cycle and Soft-Start Control

As explained in the paragraph "oscillator", the duty cycle cannot be more than $80 \%$. Now, using the $D_{\max }$ and soft-start control, this duty cycle can be limited to a lower value. Indeed as depicted in Figure 34, the pin 11 voltage is compared to the oscillator sawtooth, so that the MC44604 output should be disabled as soon as the pin 11 level becomes lower than the oscillator voltage (refer to Figure 27 and to Figure 25).


Figure 34. Maximum Duty Cycle Control
Now, using the internal current source $\left(0,4 \mathrm{I}_{\text {ref }}\right)$, the pin 11 voltage can easily be fixed by connecting a resistor to this pin.
If a capacitor is connected to pin 11 (without any resistor or in parallel to a resistor for instance), the pin 11 voltage increases from 0 to its maximum value progressively (refer to Figure 26).

Thus, the allowed maximum duty cycle grows for a delay depending on the capacitor value (and the resistor value when a resistor is connected).

So, this pin can be used to limit the duty cycle during the start-up phase and thus, to perform a soft-start.

Figure 32. Demagnetization Block


Figure 35. Different Possible Uses of Pin 11

In any case (particularly if no external component is connected to pin 11), an internal zener diode ( $\mathrm{D}_{\mathrm{Z}}$, refer to Figure 34) is able to clamp the pin 11 voltage to a value $V_{Z}$ that is higher than the oscillator value and so, that results in no max duty cycle limitation.

As soon as $\mathrm{V}_{\text {disable1 }}$ is detected, a signal UVLO1 is generated until the $\mathrm{V}_{\mathrm{CC}}$ voltage falls down to $\mathrm{V}_{\text {disable2 }}$ (refer to the undervoltage lockout section paragraph). During the delay between the disable 1 and the disable 2, using a transistor controlled by UVLO1, the pin 11 voltage is made equal to zero in order to make the max duty cycle and soft-start arrangement ready to work for the next restart.

In standby mode, this block is inhibited in order not to interfere with the Standby Current Set.

## Protection

The MC44604 can ensure a high converter reliability thanks to the protection it offers.

## Demagnetization Detection (Refer to Demag §) <br> Foldback

As depicted in Figure 28, the foldback input (pin 5) enables to reduce the maximum $\mathrm{V}_{\mathrm{CS}}$ value that would be equal to 1 typically, if there was no foldback action. Finally, the foldback arrangement is a programmable peak current limitation.


Figure 36. Foldback Characteristic
It could be used as a soft-start (by connecting to pin 5, a gradually increasing voltage) but in fact, it has been designed to provide the system with an effective overload protection.

Indeed, as the output load gradually increases, the required converter peak current becomes higher and so,
$\mathrm{V}_{\mathrm{CS}}$ grows up till it reaches its maximum value (normally, $\mathrm{V}_{\mathrm{CS} \max }=1 \mathrm{~V}$ ).

Then if the output load keeps on increasing, the system is not able to supply enough energy to maintain the output regulation. Consequently, the decreasing output can be used to apply a voltage that diminishes to a value lower than 1 V , to pin 5, in order to limit the maximum peak current. In this way, the well known foldback characteristic is obtained (refer to Figure 36).

The foldback action can be inhibited by connecting the pin 5 to $\mathrm{V}_{\mathrm{CC}}$.

## Overvoltage Protection

The overvoltage arrangement consists of a comparator that compares the pin 6 voltage to $\mathrm{V}_{\text {ref }}(2,5 \mathrm{~V})$ (refer to Figure 37).


Figure 37. Overvoltage Protection
If no external component is connected to pin 6 , the comparator non inverting input voltage is nearly equal to:

$$
\left(\frac{2 \mathrm{k} \Omega}{11,6 \mathrm{k} \Omega+2 \mathrm{k} \Omega}\right) \cdot \mathrm{V}_{\mathrm{CC}}
$$

So, the comparator output is high when:

$$
\begin{gathered}
\left(\frac{2 \mathrm{k} \Omega}{11,6 \mathrm{k} \Omega+2 \mathrm{k} \Omega}\right) \cdot \mathrm{V}_{\mathrm{CC}} \geq 2,5 \mathrm{~V} \\
\mathrm{~V}_{\mathrm{CC}} \geq 17 \mathrm{~V}
\end{gathered}
$$

A delay latch $(2 \mu \mathrm{~s})$ is incorporated in order to only take into account the overvoltages that last at least $2 \mu \mathrm{~s}$.
If this condition is achieved, $\mathrm{V}_{\text {OVPout }}$ the delay latch output becomes high and as this level is brought back to the input through an OR gate, V OVPout remains high (and so, the IC output is disabled) until $\mathrm{V}_{\text {ref }}$ is disabled.
Consequently when an overvoltage longer than $2 \mu \mathrm{~s}$ is detected, the output is disabled until a new circuit restart.

The $\mathrm{V}_{\mathrm{CC}}$ is connected when once the circuit has started-up in order to limit the circuit start-up consumption ( T is switched on when once $\mathrm{V}_{\text {ref }}$ has been generated).

The overvoltage section is enabled $5 \mu$ s after the regulator has started to allow the reference $\mathrm{V}_{\text {ref }}$ to stabilize.

By connecting external resistors to pin 6, the threshold $\mathrm{V}_{\mathrm{CC}}$ level can be changed.


Figure 38. $\mathrm{V}_{\mathrm{Cc}}$ Management

## Undervoltage Lockout Section

As depicted in Figure 39, an undervoltage lockout has been incorporated to guarantee that the IC is fully functional before allowing operation of the system.

Indeed, the $\mathrm{V}_{\mathrm{CC}}$ is connected to the non inverting input of a comparator that has an upper threshold equal to $14,5 \mathrm{~V}$ ( $\mathrm{V}_{\text {stup-th }}$ ) and a lower one equal to $7.5 \mathrm{~V}\left(\mathrm{~V}_{\text {disable2 }}\right)$ in normal mode and 14.5 V and 12.5 V in Standby mode (typical values) (Note 1).

This hysteresis comparator enables or disables the reference block that generates the voltage and current sources required by the system.

This block particularly, produces $\mathrm{V}_{\text {ref }}$ (pin 16 voltage) and $I_{r e f}$ that is determined by the resistor $R_{\text {ref }}$ connected between pin 16 and the ground:

$$
I_{\text {ref }}=\frac{V_{\text {ref }}}{R_{\text {ref }}} \text { where } V_{\text {ref }}=2.5 \mathrm{~V} \text { (typically) }
$$

In addition to this, $\mathrm{V}_{\mathrm{CC}}$ is compared to a second threshold level that is nearly equal to $9 \mathrm{~V}\left(\mathrm{~V}_{\text {disable1 }}\right)$ so that in normal mode, a signal UVLO1 is generated to reset the maximum duty cycle and soft-start block and so, to disable the output stage (refer to Max. Duty Cycle and Soft-Start §) as soon as $\mathrm{V}_{\mathrm{CC}}$ becomes lower than $\mathrm{V}_{\text {disable1 }}$. In this way, the circuit is reset and made ready for a next start-up, before the reference block is disabled (refer to Figure 26). In standby, UVLO1 is not active (there is no need to discharge the soft-start capacitor as the soft-start pin is maintained short circuited).
Note 1. In standby the difference between $\mathrm{V}_{\text {disable2 }}$ and $\mathrm{V}_{\text {stup-th }}$ is decreased not to have too low pulsed mode frequencies.

Thus, finally in normal mode, the upper $\mathrm{V}_{\mathrm{cc}}$ limit that enables the output to be active, is 9.4 V (maximum value of $\mathrm{V}_{\text {disable1 }}$ ) and so the minimum hysteresis is 4.2 V . $\left[\left(\mathrm{V}_{\text {stup-th }}\right)_{\min }=13.6 \mathrm{~V}\right]$.
The large hysteresis and the low start-up current of the MC44604 make it ideally suited for off-line converter applications where efficient bootstrap start-up techniques are required.

## Standby Management

The MC44604 has been designed to detect the transitions between the standby and normal mode and to manage each mode in an optimal way.

In standby, the device monitors a pulsed mode that enables to drastically reduce the power consumption.

## Pulsed Mode

The MC44604 standby is preferably associated to a flyback configuration as depicted in Figure 39.


Figure 39. Standby Flyback Configuration

In effect, by this means, all the output regulation levels are divided by the ratio:

where $\mathrm{V}_{\mathrm{HV}}$ is the normal mode high voltage regulation level, $\mathrm{V}_{\text {stby }}$ is the standby $\mu \mathrm{P}$ supply voltage.

For instance, in the case of TV or monitors applications, the output levels (except the $\mu \mathrm{P}$ supply voltage, $\mathrm{V}_{\text {stby }}$ ) are drastically reduced by a ratio in the range of 10 .

Consequently, as the output voltages are reduced, the losses due to the output leakage consumption, are practically eliminated, without having to disconnect the loads.

## Start-up Operations

The choice of the right configuration (normal or standby) is performed at each start-up.

That is why, as explained in the transitions $\S$, at each change of mode, the MC44604 is first turned off so that a new start-up should be performed.


Figure 40. Start-up Operation
At each start-up, the circuit detects if it must work in standby or in normal mode configuration.

To do that, the circuit compares the current $\mathrm{I}_{\mathrm{pin} 15}$ to $\mathrm{I}_{\text {det }}$ so that, if:

- $\mathrm{I}_{\mathrm{pin} 15}>\mathrm{I}_{\text {det }}:$ Standby mode
- $\mathrm{I}_{\mathrm{pin} 15}<\mathrm{I}_{\text {det }}$ : Normal mode

According to the detected mode, the circuit configuration is set (refer to Figure 40).

This detection phase takes place during the first $5 \mu \mathrm{~s}$ of circuit operation in order to have the internal signals well stabilized before the decision is taken.

Figure 41. Standby Pin 15 Arrangement


## Standby Management

The standby operation consists of two main phases:

- the off phase during which the MC44604 is off. During this sequence, the circuit $\mathrm{V}_{\mathrm{cc}}$ is being charged and no energy is transferred to the output.
- the active phase during which the MC44604 is on. At this moment, some power can be drawn from the mains.
During the active phase, the power conversion is controlled so that:
- the normal mode regulation means (error amplifier) and the soft-start are inhibited
- the $\mathrm{V}_{\mathrm{cc}}$ undervoltage lockout $\left(\mathrm{V}_{\text {disable2 }}\right)$ level is increased from 9 V up to 12.5 V . This limitation of the $\mathrm{V}_{\mathrm{cc}}$ hysteresis enables to increase the pulsed mode frequency
- the peak inductor current is forced to be constant and equal to the level programmable by the external resistor $\mathrm{R}_{\text {Ipmax }}$ connected to the pin 9 so that:

$$
I_{\mathrm{pmax}}=\frac{0,4 \times I_{\mathrm{ref}} \times \mathrm{R}_{\text {lpmax }}}{2,6 \times \mathrm{R}_{\mathrm{S}}}
$$

where: $I_{p m a x}$ is the standby inductor peak current, $R_{S}$ is the current sense resistor.

- when the pin 15 current gets higher than the threshold $\mathrm{I}_{\mathrm{reg}}\left(20.5 \times \mathrm{I}_{\mathrm{ref}}\right)$, this operating mode stops and the circuit output is latched off.
So, in fact, the active phase is split into two distinct sequences and finally three phases can be defined (refer to Figure 32):
- the off phase: the MC44604 is off and the $\mathrm{V}_{\text {cc }}$ capacitor is being charged. When the $\mathrm{V}_{\mathrm{cc}}$ gets higher than $V_{\text {stup-th }}$, the circuit turns on and the switching sequence starts
- the switching phase: the circuit is on and forces a constant peak inductor current. This sequence lasts until $\mathrm{I}_{\mathrm{pin} 15}$ gets higher than $\mathrm{I}_{\text {reg }}$
- the latched phase: the circuit is on but the output is disabled. This sequence lasts until the standby $\mathrm{V}_{\mathrm{cc}}$ undervoltage lockout voltage ( 12.5 V ) is reached. A new off phase is then initialized.


Figure 42. Standby Regulation
As a consequence, $\mathrm{V}_{\text {stby }}$ varies between a peak value (obtained at the end of the switching phase) and a valley level (reached at the end of the off phase).

The level of the peak value is controlled by forcing a current higher than $I_{\text {reg }}$ in pin 15 when this level has reached the desired value.

The arrangement in Figure 41 allows to obtain this operation. A zener diode Z is connected so that a current limited by $R_{\text {reg }}$, is drawn by this device, when the $\mu \mathrm{P}$ supply voltage gets higher than $\mathrm{V}_{\mathrm{Z}}$. By this way, the current injected in the pin 15 increases and when this current is detected as higher than $\mathrm{I}_{\text {reg }}$, the output gets disabled until the next start-up (Note 1).

Practically, the pin 15 current can be expressed as follows (when the zener is activated):

$$
\mathrm{I}_{\text {pin15 }}=\mathrm{CTR} \times \frac{\mathrm{V}_{\text {stby }}-\mathrm{V}_{\text {opto }}-\mathrm{V}_{\mathrm{z}}}{R_{\text {reg }}}
$$

where: CTR is the opto coupler gain, $\mathrm{V}_{\text {opto }}$ is opto coupler voltage drop.
So, as the Vstby peak value is obtained when $\left(\mathrm{I}_{\mathrm{pin} 15}=\right.$ $\mathrm{I}_{\text {reg }}$ ), it can be calculated using the following equation:

$$
V_{\text {stby pk }}=V_{z}+V_{\text {opto }}+\frac{R_{\text {reg }} \times I_{\text {reg }}}{\text { CTR }}
$$

Practically, $\mathrm{R}_{\text {reg }}$ is chosen very low (in the range of $10 \Omega$ low resistance just to limit the current when $\mathrm{V}_{\text {stby }} \mathrm{pk}$ gets higher than $\mathrm{V}_{\mathrm{Z}}$ ):

$$
V_{\text {stby pk }} \cong V_{z}+V_{\text {opto }}
$$

Note 1. If the pin 15 current is higher than $\mathrm{I}_{\text {reg }}$ at start-up, the output is just shutdown but not latched. The circuit must
detect a sequence during which $\mathrm{I}_{\mathrm{pin} 15}$ lower than $\mathrm{I}_{\text {reg }}$ before being able to latch gets higher than $\mathrm{V}_{\mathrm{z}}$ ).

## Transitions Between Normal Mode and Standby Mode

 (Refer to Figure 43)The MC44604 detects a transition by comparing the pin 15 current to:

- $\mathrm{I}_{\text {det }}$ (transition standby to normal mode)
- $\mathrm{I}_{\text {init }}$ (transition normal mode to standby)

Each transition detection results in the circuit turning off, so that the device can work in the new mode after the following restart.

## - transition normal mode to standby:

This transition is detected by comparing the $\mathrm{I}_{\mathrm{pin} 15}$ current to the threshold current ( $\mathrm{I}_{\mathrm{init}}$ ).
$\mathrm{I}_{\text {init }}$ is high enough so that the opto coupler current used for the regulation, never exceeds this value.

The arrangement in Figure 41 is well adapted to this mode of operation. The $\mu \mathrm{P}$ initializes the standby mode by turning on the switch T . This results in the C capacitor charge that produces a peak current in the primary side of the opto coupler. C and $\mathrm{R}_{\text {init }}$ must be dimensioned so that the opto coupler primary side generates a pin 15 current higher than $\mathrm{I}_{\text {init }}$ during more than $1 \mu \mathrm{~s}$.

## - transition standby to normal mode:

If the circuit detects that ( $\mathrm{I}_{\mathrm{pin} 15}<\mathrm{I}_{\mathrm{det}}$ ) during standby operation, the circuit is turned off. So, if the normal mode is maintained at the following start-up, the circuit will re-start in a normal mode configuration.

The arrangement in Figure 41 allows to perform this detection. When the $\mu \mathrm{P}$ detects the end of the standby, it turns off the switch T and the opto coupler stops supplying current to the circuit.


The transition stand-by to normal mode occurs while the circuit is off ( $\mathrm{V}_{\mathrm{CC}}$ charge phase)


The transition stand-by to normal mode occurs while the circuit is on (working phase)

Figure 43. Transitions Between Modes

Application Schematic


## MC44605

## High Safety, Latched Mode, GreenLine ${ }^{\text {TM }}$ PWM Controller for (Multi)Synchronized Applications

The MC44605 is a high performance current mode controller that is specifically designed for off-line converters. This circuit has several distinguishing features that make it particularly suitable for multisynchronized monitor applications.

The MC44605 synchronization arrangement enables operation from 16 kHz up to 130 kHz . This product was optimized to operate with universal mains voltage, i.e., from 80 V to 280 V , and its high current totem pole output makes it ideally suited for driving a power MOSFET.

The MC44605 protections enable a well-controlled and safe power management. Four major faults while detected, activate the analogic counter of a disabling block designed to perform a latched circuit output inhibition.

## Current Mode Controller

- Current Mode Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Oscillator with Precise Frequency Control
- Externally Programmable Reference Current
- Secondary or Primary Sensing (Availability of Error Amplifier Output)
- Synchronization Facility
- High Current Totem Pole Output
- $\mathrm{V}_{\mathrm{cc}}$ Undervoltage Lockout with Hysteresis
- Low Output dV/dT for Low EMI Radiations
- Low Start-Up and Operating Current


## Safety/Protection Features

- Soft-Start Feature
- Demagnetization (Zero Current Detection) Protection
- Overvoltage Protection Facility against Open Loop
- EHT Overvoltage Protection (E.H.T.OVP): Detection of too High Synchronization Pulses
- Winding Short Circuit Detection (W.S.C.D.)
- Limitation of the Maximum Input Power (M.P.L.): Calculation of Input Power for Overload Protection
- Overheating Detection (O.H.D.): to Prevent the Power Switch from an Excessive Heating
Latched Disabling Mode
- When one of the following faults is detected: EHT overvoltage, Winding Short Circuit (WSCD), a too high input power (M.P.L.), power switch overheating (O.H.D.), an analogic counter is activated
- If the counter is activated for a time that is long enough, the circuit gets definitively disabled. The latch can only be reset by making decrease the $\mathrm{V}_{\mathrm{cc}}$ down to about 3 V , i.e., practically by unplugging or turning off the SMPS.


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


PIN CONNECTIONS

(Top View)

* Winding Short Circuit Detection
ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC44605P | PDIP-16 | 25 Units/Rail |

## Block Diagram



## MAXIMUM RATINGS

| Rating | Pin \# | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Total Power Supply and Zener Current |  | $\left(\mathrm{I}_{\mathrm{CC}}+\mathrm{I}_{\mathrm{z}}\right.$ ) | 40 | mA |
| Output Supply Voltage with Respect to Ground <br> Output Current* <br> Source <br> Sink | $\begin{aligned} & 2 \\ & 1 \\ & 3 \end{aligned}$ | $\begin{gathered} \mathrm{V}_{\mathrm{C}} \\ \mathrm{~V}_{\mathrm{CC}} \\ \\ \mathrm{I}_{\mathrm{O}(\text { Source })} \\ \mathrm{l}_{\mathrm{O}(\text { Sink }} \end{gathered}$ | $\begin{gathered} 18 \\ \\ -750 \\ 750 \end{gathered}$ | V <br> mA |
| Output Energy (Capacitive Load per Cycle) |  | W | 5.0 | $\mu \mathrm{J}$ |
| Soft-Start |  | $\mathrm{V}_{\mathrm{SS}}$ | -0.3 to 2.2 V | V |
| Current Sense, Voltage Feedback, E/A Output, $\mathrm{C}_{\mathrm{T}}, \mathrm{R}_{\text {ref }}, \mathrm{MPL}, \mathrm{OHD}, \mathrm{C}_{\text {ext }}$, WSCD |  | $\mathrm{V}_{\text {in }}$ | -0.3 to 5.5 V | V |
| E.H.T.OVP, Sync Input Current Source <br> Sink | $\begin{aligned} & 9 \\ & 6 \\ & 9 \\ & 6 \end{aligned}$ | $I_{\text {sync ( }}$ (Source) <br> ${ }_{\text {EHT }}$ (Source) <br> Isync (Sink) <br> IEHT (Sink) | $\begin{gathered} -4.0 \\ 10 \end{gathered}$ | mA |
| Demagnetization Detection Input Current <br> Source <br> Sink | 8 | $I_{\text {demag-ib (Source) }}$ $I_{\text {demag-ib (Sink) }}$ | $\begin{gathered} -4.0 \\ 10 \end{gathered}$ | mA |
| Error Amplifier Output Sink Current | 13 | $\mathrm{I}_{\mathrm{E} / \mathrm{A}}$ (Sink) | 20 | mA |
| Power Dissipation and Thermal Characteristics Maximum Power Dissipation at $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air |  | $\begin{array}{r} \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\theta \mathrm{JJA}} \\ \hline \end{array}$ | $\begin{aligned} & 0.6 \\ & 100 \end{aligned}$ | $\begin{gathered} W \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature |  | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature |  | $\mathrm{T}_{\text {A }}$ | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |

*Maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$, $\mathrm{R}_{\text {ref }}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=2.2 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ unless otherwise noted.) (Note 1)

| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

OUTPUT SECTION (Note 2)

| $\begin{array}{ll} \hline \begin{array}{l} \text { Output Voltage } \\ \text { Low Level Drop Voltage } \\ \\ \\ \left(I_{\text {Sink }}=100 \mathrm{~mA}\right) \\ \left(I_{\text {Sink }}=500 \mathrm{~mA}\right) \end{array} \\ \text { High Level Drop Voltage }\left(I_{\text {Source }}=200 \mathrm{~mA}\right) \\ & \left(I_{\text {Source }}=500 \mathrm{~mA}\right) \end{array}$ | 3 | $\begin{aligned} & \mathrm{v}_{\mathrm{OL}} \\ & \mathrm{v}_{\mathrm{OH}} \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.4 \\ & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 1.2 \\ & 2.0 \\ & 2.0 \\ & 2.7 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage During Initialization Phase $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=0 \text { to } 1.0 \mathrm{~V}, I_{\text {Sink }}=10 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=1.0 \text { to } 5.0 \mathrm{~V}, I_{\text {Sink }}=100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \text { to } 13 \mathrm{~V}, I_{\text {Sink }}=1.0 \mathrm{~mA} \end{aligned}$ | 3 | $\mathrm{V}_{\text {OL }}$ | $\begin{aligned} & - \\ & \text { - } \end{aligned}$ | $\begin{aligned} & - \\ & 0.1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.0 \\ & 1.0 \end{aligned}$ | V |
| Output Voltage Rising Edge Slew-Rate ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) |  | dVo/dT | - | 300 | - | V/ $\mu \mathrm{s}$ |
| Output Voltage Falling Edge Slew-Rate ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) |  | dVo/dT | - | -300 | - | $\mathrm{V} / \mu \mathrm{s}$ |

${ }^{*} \mathrm{~V}_{\mathrm{C}}$ must be greater than 5.0 V .

1. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V . Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. No output signal when the Error Amplifier output is in Low State, i.e., when for instance, $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$, $\mathrm{R}_{\mathrm{ref}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=2.2 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ unless otherwise noted.) (Note 1)

| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER SECTION |  |  |  |  |  |  |
| Voltage Feedback Input ( $\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=2.5 \mathrm{~V}$ ) | 14 | $V_{\text {FB }}$ | 2.4 | 2.5 | 2.6 | V |
| Input Bias Current ( $\mathrm{V}_{\mathrm{FB}}=2.5 \mathrm{~V}$ ) | 14 | $\mathrm{I}_{\text {FB-ib }}$ | -2.0 | -0.6 | - | $\mu \mathrm{A}$ |
| Open Loop Voltage Gain ( $\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=2.0 \mathrm{~V}$ to 4.0 V ) |  | Avol | 65 | 70 | - | dB |
| Unity Gain Bandwidth $\begin{aligned} & \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ |  | BW | - | - | $5.5$ | MHz |
| Voltage Feedback Input Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 15 V ) |  | $V_{\text {FBline-reg }}$ | -10 | - | 10 | mV |
| $\begin{aligned} & \text { Output Current } \\ & \text { Sink }\left(\mathrm{V}_{\mathrm{E} / \mathrm{A} \text { out }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \\ & \text { Source }\left(\mathrm{V}_{\mathrm{E} / \mathrm{A}} \text { out }=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-25^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 13 | $I_{\text {Sink }}$ <br> $I_{\text {Source }}$ | $\begin{gathered} 2.0 \\ -2.0 \end{gathered}$ | $12$ | $-0.2$ | mA |
| Output Voltage Swing <br> High State ( $\mathrm{I}_{\mathrm{E} / \mathrm{A}}$ out (source) $=0.5 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ ) <br> Low State ( $\mathrm{I}_{\mathrm{E} / \mathrm{A} \text { out }(\text { sink })}=0.33 \mathrm{~mA}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ ) | 13 | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ |  | $\begin{aligned} & 6.5 \\ & 1.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 1.1 \end{aligned}$ | V |

CURRENT SENSE SECTION

| Maximum Current Sense Input Threshold <br> $\left(V_{\text {Feedback (pin14) }}=2.3 \mathrm{~V}\right.$ and $\left.\mathrm{V}_{\text {Soft-Start (pin11) }}=1.2 \mathrm{~V}\right)$ | 7 | $\mathrm{~V}_{\text {cs-th }}$ | 0.96 | 1.0 | 1.04 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | 7 | $\mathrm{I}_{\text {cs-ib }}$ | -10 | -2.0 | - | $\mu \mathrm{A}$ |
| Propagation Delay (Current Sense Input to Output at $\mathrm{V}_{\text {TH }}$ of <br> MOS transistor $=3.0 \mathrm{~V})$ |  | $\mathrm{t}_{\text {PLH(In/Out }}$ | - | 120 | 200 | ns |

OSCILLATOR AND SYNCHRONIZATION SECTION

| Frequency $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ |  | $\mathrm{F}_{\mathrm{OSC}}$ | 16 | - | 20 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 15 V$)$ |  | $\Delta \mathrm{F}_{\mathrm{OSC}} / \Delta \mathrm{V}$ | - | 0.05 | - | $\% / \mathrm{V}$ |
| Frequency Change with Temperature $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ |  | $\Delta \mathrm{F}_{\mathrm{OSC}} / \Delta \mathrm{T}$ | - | 0.05 | - | $\% /{ }^{\circ} \mathrm{C}$ |
| Ratio Charge Current/Reference Current $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ |  | $\mathrm{I}_{\text {charge }} / \mathrm{I}_{\text {ref }}$ | 0.39 | - | 0.48 | - |
| Free Mode Oscillator Ratio $=\mathrm{I}_{\text {discharge }} /\left(\mathrm{I}_{\text {discharge }}+\mathrm{I}_{\text {charge }}\right)$ |  | D | 72 | 75 | 78 | $\%$ |
| Synchronization Input Threshold Voltage | 9 | $\mathrm{~V}_{\text {syncth }}$ | -250 | -200 | -150 | mV |
| Negative Clamp Level ( $\left.\mathrm{I}_{\text {syncth-in }}=2.0 \mathrm{~mA}\right)$ |  | $\mathrm{NEG}-\mathrm{SYNC}$ | -0.65 | -0.5 | -0.34 | V |

UNDERVOLTAGE LOCKOUT SECTION

| Start-up Threshold | 1 | $\mathrm{~V}_{\text {stup-th }}$ | 13.6 | 14.5 | 15.4 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Disable Voltage After Threshold Turn-On (UVLO 1) <br> $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $+85^{\circ} \mathrm{C}$ ) | 1 | $\mathrm{~V}_{\text {disable1 }}$ | 8.3 | - | 9.6 | V |
| Disable Voltage After Threshold Turn-On (UVLO 2) <br> $\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $+85^{\circ} \mathrm{C}$ ) | 1 | $\mathrm{~V}_{\text {disable2 }}$ | 7.0 | 7.5 | 8.0 | V |

1. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V . Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$, $\mathrm{R}_{\mathrm{ref}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=2.2 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ unless otherwise noted.) (Note 1)

| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |  |
| Reference Output Voltage ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 15 V ) | 16 | $\mathrm{V}_{\text {ref }}$ | 2.4 | 2.5 | 2.6 | V |
| Reference Current Range ( $\mathrm{I}_{\text {ref }}=\mathrm{V}_{\text {ref }} / \mathrm{R}_{\text {ref }}, \mathrm{R}=5.0 \mathrm{k}$ to $25 \mathrm{k} \Omega$ ) | 16 | $I_{\text {ref }}$ | -500 | - | -100 | $\mu \mathrm{A}$ |
| Reference Voltage Over $\mathrm{I}_{\text {ref }}$ Range |  | $\Delta \mathrm{V}_{\text {ref }}$ | -40 | - | 40 | mV |

## DEMAGNETIZATION DETECTION SECTION (Note 2)

| Demagnetization Detect Input <br> Demagnetization Comparator Threshold ( $\mathrm{V}_{\text {pin9 }}$ Decreasing) <br> Propagation Delay (Input to Output, Low to High) <br> Input Bias Current ( $\mathrm{V}_{\text {demag }}=65 \mathrm{mV}$ ) | 8 | $V_{\text {demag-th }}$ <br> tplif(In/Out) $I_{\text {demag-lb }}$ | $\begin{gathered} 50 \\ - \\ -0.5 \end{gathered}$ | $\begin{aligned} & 65 \\ & 0.5 \end{aligned}$ | $80$ | $\begin{aligned} & \mathrm{mV} \\ & \mu \mathrm{~s} \\ & \mu \mathrm{~A} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Minimum Off-Time when the pin 8 is grounded |  | T DEM-GND | 1.5 | 3.0 | 4.5 | $\mu \mathrm{s}$ |
| Negative Clamp Level ( $\mathrm{l}_{\text {demag }}=-2.0 \mathrm{~mA}$ ) |  | CLVL-neg | -0.50 | -0.38 | -0.25 | V |
| Positive Clamp Level ( $\mathrm{I}_{\text {demag }}=+2.0 \mathrm{~mA}$ ) |  | CLVL-pos | 0.50 | 0.72 | 0.85 | V |

SOFT-START SECTION (Note 3)

| Ratio Charge Current $/ I_{\text {ref }}\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ |  | $\mathrm{I}_{\text {SS-ch }} / I_{\text {ref }}$ | 0.37 | - | 0.43 | - |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Discharge Current $\left(\mathrm{V}_{\text {soft-start }}=1.0 \mathrm{~V}\right)$ |  | $\mathrm{I}_{\text {discharge }}$ | 1.5 | 5.0 | - | mA |
| Clamp Level |  | $\mathrm{V}_{\text {SS-CLVL }}$ | 2.2 | 2.4 | 2.6 | V |
| Circuit Inhibition Threshold |  |  |  |  |  |  |
| $\mathrm{V}_{\text {CS }}$ Soft-Start Clamp Level $\left(\mathrm{R}_{\text {soft-start }}=5 \mathrm{k} \Omega\right)$ |  | $\mathrm{V}_{\text {SSinhi }}$ | 30 | - | 150 | mV |

*The circuit is shutdown if the Soft-Start pin voltage is lower than this level.

1. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V . Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. This function can be inhibited by connecting pin 8 to GND. In this case, there is a minimum off-time equal to $\mathrm{T}_{\text {DEM-GND }}$.
3. The MC44605 can be shut down by connecting Soft-Start pin (pin 11) to Ground.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{C}}=12 \mathrm{~V}$, $\mathrm{R}_{\text {ref }}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=2.2 \mathrm{nF}$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/ \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}=-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ unless otherwise noted.) (Note 1)

| Characteristic |
| :--- |
| \begin{tabular}{\|l|c|c|c|c|c|c|c|}
\hline
\end{tabular} |
|  Pin \# Symbol Min Typ Max Unit <br> OVERVOLTAGE SECTION  $T_{\text {PHL(In/Out })}$ 1.0 - 4.0 $\mu \mathrm{~s}$ <br> Protection Level on $\mathrm{V}_{\mathrm{CC}}\left(\mathrm{T}_{\mathrm{A}}=-25^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$  $\mathrm{V}_{\mathrm{CC} \text { prot }}$ 15.9 - 18.1 V |

## EHT OVP SECTION (Note 2)

| Negative Clamp Level $\left(\mathrm{I}_{\text {synch-in }}=-2.0 \mathrm{~mA}\right)$ |  | NEG-SYNC | -0.65 | -0.5 | -0.35 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| EHT OVP Input Threshold |  | $\mathrm{V}_{\text {ref }}$ | 7.0 | 7.4 | 7.8 | V |
| EHT OVP Input Bias Current $\left(\mathrm{V}_{\text {EHT }}\right.$ OVP(pin 9) $\left.=0 \mathrm{~V}\right)$ | 9 | $\mathrm{I}_{\text {EHTOVP }}$ | -5.0 | - | 0 | $\mu \mathrm{~A}$ |

WINDING SHORT CIRCUIT DETECTION SECTION

| WSCD Threshold with $\mathrm{I}_{\text {pin } 15}=200 \mu \mathrm{~A}$ |  | Vshift | 70 | 100 | 120 | mV |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |

MPL \& OHD SECTION

| MPL Parameter* |  | $\Gamma_{\text {MPL }}$ | 0.185 | 0.240 | 0.295 | $\mathrm{~V}^{-1}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| MPL Comparator Threshold ${ }^{* *}$ |  | $\mathrm{~V}_{\text {MPL-th }}$ | 2.4 | 2.5 | 2.6 | V |
| OHD Parameter*** |  | $\Gamma_{\text {OHD }}$ | 1.15 | 1.50 | 1.85 | $\mathrm{~V}^{-1}$ |
| OHD Comparator Threshold ${ }^{* * * *}$ |  | $\mathrm{~V}_{\text {OHD-th }}$ | 2.4 | 2.5 | 2.6 | V |

*This parameter is defined in the MPL §. This parameter is obtained by measuring the MPL pin average current and dividing this result by the corresponding squared $\mathrm{V}_{\mathrm{CS}}$, the measured frequency value and the $\mathrm{C}_{\mathrm{T}}$ value deducted from the measured frequency value.
Measurement conditions: $\mathrm{V}_{\text {Feedback(pin 14) }}=2.3 \mathrm{~V}, \mathrm{~V}_{\text {soft-start(pin 11) }}=0.5 \mathrm{~V}$ and pins 7,8 , and 9 connected to $G N D$ (the working frequency is typically equal to $18 \mathrm{kHz}-\mathrm{R}_{\mathrm{ref}}=10 \mathrm{k} \Omega \pm 1 \%, \mathrm{C}_{\mathrm{T}}=2.2 \mathrm{nF}$ ).
**The MPL comparator output is DismpL.
${ }^{* * *}$ This parameter is defined in the OHD $\S$. This parameter is obtained by measuring the OHD pin average current and dividing this result by the corresponding squared $\mathrm{V}_{\mathrm{CS}}$ value and multiplying it by the $\mathrm{R}_{\text {ref }}$ value.
Measurement conditions: $\mathrm{V}_{\text {Feedback(pin 14) }}=2.3 \mathrm{~V}, \mathrm{~V}_{\text {soft-start(pin 11) }}=0.5 \mathrm{~V}$ and pins 7, 8, and 9 connected to GND (the working frequency is typically equal to $18 \mathrm{kHz}-\mathrm{R}_{\mathrm{ref}}=10 \mathrm{k} \Omega \pm 1 \%, \mathrm{C}_{\mathrm{T}}=2.2 \mathrm{nF}$ ).
****The OHD comparator output is DisohD.
DISABLING BLOCK SECTION

| Delay Pulse Width |  | $T_{\text {WSCD }}$ | - | 4.0 | - | $\mu \mathrm{s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Ratio (EHTOVP and WSCD Disabling Capacitor Charge <br> Current) $I_{\text {ref }}$ |  | $I_{\text {Dis-H }} / I_{\text {ref }}$ | 90 | 100 | 110 | $\%$ |
| Ratio (MPL and OHD Disabling Capacitor Charge Current) $I_{\text {ref }}$ |  | $I_{\text {Dis-L }} / I_{\text {ref }}$ | 2.7 | 3.1 | 3.5 | $\%$ |
| Minimum $V_{\text {CC }}$ Value Enabling the Disabling Block Latch |  |  | $V_{\text {CCDis }}$ | 1.0 | - | 5.0 |

*Once a fault detection activated it, the Disabling Block Latch gets reset when the $V_{C C}$ becomes lower than this threshold.
TOTAL DEVICE

| Power Supply Current |  | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Startup-Up $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right.$ with $\mathrm{V}_{\mathrm{CC}}$ increasing $)$ |  | - | 0.35 | 0.55 |  |  |
| Startup-Up $\left(\mathrm{V}_{\mathrm{CC}}=9.0 \mathrm{~V}\right.$ with $\mathrm{V}_{\mathrm{CC}}$ increasing $)$ |  | - | 0.35 | 0.55 |  |  |
| Startup-Up $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$ with $\mathrm{V}_{\mathrm{CC}}$ increasing $)$ |  |  |  |  |  |  |
| Operating $\mathrm{T}_{\mathrm{A}}=-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}^{*}$ |  |  | 0.35 | 0.55 |  |  |
| Disabling Mode $\left(\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}\right)^{* *}$ |  |  | - | 20 | 25 |  |
| Power Supply Zener Voltage $\left(\mathrm{I}_{\mathrm{CC}}=35 \mathrm{~mA}\right)$ |  | $\mathrm{V}_{\mathrm{Z}}$ | 18.5 | - | - | V |
| Thermal Shutdown |  | - | - | 155 | - | ${ }^{\circ} \mathrm{C}$ |

*Refer to Note 1.
**This consumption is measured while the circuit is inhibited by the Definitive Latch.

1. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the start-up threshold before setting to 12 V . Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. This function can be inhibited by connecting pin 9 to GND. In this case, the synchronization block is inhibited too and the MC44605 works in free mode.

| Pin | Name | Pin Description |
| :---: | :---: | :---: |
| 1 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the IC. |
| 2 | $\mathrm{V}_{\mathrm{C}}$ | The output high state, $\mathrm{V}_{\mathrm{OH}}$, is set by the voltage applied to this pin. With a separate connection to the power source, it gives the possibility to set by means of an external resistor the output source current at a different value than the sink current. |
| 3 | Output | The output current capability is suited for driving a power MOSFET. |
| 4 | GND | The ground pin is a single return typically connected back to the power source. It is used as control and power ground. |
| 5 | Maximum Power Limitation | This block enables to estimate the input power. When this calculated power is detected as too high, a fault information is sent to the disabling block in order to definitively disable the circuit. |
| 6 | Over-Heating Detection | This block estimates the MOSFET heating. When this calculated heating is too high, the device gets definitively disabled (disabling block action). |
| 7 | Current Sense Input | A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer. A maximum level of 1 V allows to limit the inductor current. |
| 8 | Demagnetization Detection | A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback energy reservoir. A zero voltage detection corresponds to a complete core demagnetization. The demagnetization detection prevents the oscillator from a re-start and so the circuit from a new conduction phase, if the fly-back is not in a dead-time state. This function can be inhibited by connecting Pin 8 to GND but in this case, there is a minimum off-time typically equal to $3 \mu \mathrm{~s}$. |
| 9 | Synchronization and E.H.T.OVP Input | Activating the synchronization input pin with a pulse higher or equal to the negative threshold (typically -200 mV ) allows the next switching period to be reinitialized. The oscillator is free when connecting Pin 9 to GND. When the E.H.T.OVP pin receives a voltage that is greater than 7.5 V , the disabling block $\mathrm{C}_{\text {ext }}$ capacitor is charged so that the circuit gets definitively disabled if the $\mathrm{C}_{\text {ext }}$ voltage becomes higher than $\mathrm{V}_{\text {ref }}$. This block is incorporated to detect and disable the device when the synchronization pulses are too high. |
| 10 | Oscillator Capacitor $\mathrm{C}_{\boldsymbol{T}}$ | The free mode oscillator frequency is programmed by the capacitor $\mathrm{C}_{\mathrm{T}}$ choice together with the $\mathrm{R}_{\text {ref }}$ resistance value. $\mathrm{C}_{\mathrm{T}}$, connected between pin 10 and GND, generates the oscillator sawtooth. |
| 11 | Soft-Start | A capacitor connected to this pin can temporary reduce the maximum inductor peak current. By this way, a soft-start can be performed. By connecting pin 11 to Ground, the MC44605 is shut down. |
| 12 | $\mathrm{C}_{\text {ext }}$ (Disabling Block) | When a too high synchronization pulse voltage (E.H.T.OVP) or a winding short circuit (WSCD) is detected, the capacitor $\mathrm{C}_{\text {ext }}$ is charged using a current source $\mathrm{I}_{\text {Dis- }}$. In the case of a MPL or OHD fault detection, $\mathrm{C}_{\text {ext }}$ is charged using $\mathrm{I}_{\text {Dis-L. }}$. If the $\mathrm{C}_{\text {ext }}$ capacitor voltage gets higher than $\mathrm{V}_{\text {ref }}$, the circuit is definitively disabled. Then, to restart, the converter must be switched off in order to make $\mathrm{V}_{\mathrm{CC}}$ decrease down to about 0 V . |
| 13 | E/A Output | The error amplifier output is made available for loop compensation. |
| 14 | Voltage Feedback | This is the inverting input of the Error Amplifier. It can be connected to the Switching Mode Power Supply output through an optical (or else) feedback loop or to the subdivided $\mathrm{V}_{\mathrm{CC}}$ voltage in case of primary sensing technic. |
| 15 | Winding Short Circuit Detection Programmation | The W.S.C.D. block is incorporated to detect the transformer Winding Short Circuits. This function is performed by detecting the inductor overcurrents thanks to a comparator which threshold is programmable to be well adapted to any application. |
| 16 | $\mathrm{R}_{\text {ref }}$ | The $\mathrm{R}_{\text {ref }}$ value fixes the internal reference current that is particularly used to perform the precise oscillator waveform. The current range goes from 100 $\mu \mathrm{A}$ up to $500 \mu \mathrm{~A}$. |

## MC44605

## Summary of the Main Design Equations

The following table consists of equations enabling to dimension a multisynchronized SMPS operating in discontinuous mode.

| $\operatorname{Pin}_{\max }=\frac{\text { Pout }_{\max }}{\eta}$ | Pout $_{\text {max }}$ is the maximum power the load may draw in normal working. <br> The maximum input power $\mathrm{Pin}_{\text {max }}$ is easily deducted by dividing Pout ${ }_{\text {max }}$ by the efficiency $(\eta)$. In this kind of application, the efficiency is generally taken equal to $80 \%$. |
| :---: | :---: |
| $\mathrm{Lp}_{\max }=\frac{\left[\frac{\sqrt{2} \cdot \mathrm{Vac}_{\text {min }} \times \mathrm{NVo}}{\sqrt{2} \cdot \mathrm{Vac}_{\text {min }}+\mathrm{NVo}}\right]^{2}}{2 \times \mathrm{Pin}_{\max } \times \mathrm{fsync}_{\max }}$ | The inductor value Lp must be chosen lower than $\mathrm{Lp} \mathrm{p}_{\max }$ or ideally equal to this value (to optimize the application design-in). <br> In effect, if $L p$ was higher than $L p_{\text {max }}$, a synchronized and discontinuous working could not be guaranteed (in some cases, the demagnetization phase would not be finished while a new conduction phase should start to follow the synchronization). |
|  | $\mathrm{Ipk}_{\text {max }}$ is the maximum inductor peak current. This current is obtained when the power to transfer is maximum at the minimum synchronization frequency ( 60 W output, 30 kHz in the proposed application). |
| $\mathrm{d}_{\text {max }}=\frac{\sqrt{\mathrm{Pin}_{\text {max }} \times \mathrm{Lp} \times \text { fsync }_{\text {max }}}}{\mathrm{Vac}_{\text {min }}}$ | $d_{\text {max }}$ is the maximum duty cycle. The duty cycle is maximum at the lowest input voltage when the power demand is maximum while the synchronization frequency also is maximum. |
| $\mathrm{Pon}_{\text {max }}=\frac{1}{3} \times \mathrm{Rds}_{\text {on }} \times \mathrm{lpk}_{\text {max }}{ }^{2} \times \mathrm{d}_{\text {max }}$ | $\mathrm{Pon}_{\text {max }}$ is the maximum Mosfet on-time losses that are proportional to $\mathrm{Ipk}_{\text {max }}, \mathrm{d}_{\text {max }}$ and Rds ${ }_{\text {on }}$ (on-time Mosfet resistor). <br> This conduction losses estimation enables to dimension the power Mosfet. |
| $\left(\mathrm{V}_{\mathrm{DS}}\right) \max =\left(\sqrt{2} \times \mathrm{Vac}_{\text {max }}\right)+(\mathrm{N} \times$ Vout $)$ | $\left(V_{\mathrm{DS}}\right)$ max is the maximum voltage the power switch must be able to face. In fact, this calculation does not take into account the turnings off spikes. So, it is necessary to take a margin of at least about 50 V . |
| $\left(\mathrm{V}_{\mathrm{D}}\right) \max =\left(\sqrt{2} \times \frac{\mathrm{Vac}_{\text {max }}}{\mathrm{N}}\right)+$ Vout | $\left(\mathrm{V}_{\mathrm{D}}\right)$ max is the maximum voltage the high voltage secondary diode must be able to face. Because of the turning off spikes, a margin must also be taken. |
| (ni) $\max =\mathrm{N} \times \mathrm{n}_{\text {Vout }} \times \mathrm{Ipk}_{\max }$ | ( $\mathrm{A}_{\mathrm{L}}$ ) and (ni) are the magnetic parameters. <br> (ni) max must not exceed the ferrite (ni). Otherwise, the transformer may get saturated when the peak current is high. |
| $A_{L}=\frac{L_{P}}{\left(N \times n_{\text {Vout }}\right)^{2}}$ | $\left(A_{L}\right)$ is the ferrite constant that links the primary inductor value to the squared number of primary turns: $L p=A_{L} \times n_{p}{ }^{2}$. |

## Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 70 dB . The non inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is $-2.0 \mu \mathrm{~A}$. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.


Figure 1. Error Amplifier Compensation

The Error Amp Output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diodes drops ( $\approx 1.4 \mathrm{~V}$ ) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 3) when Pin 13 is at its lowest state $\left(\mathrm{V}_{\mathrm{OL}}\right)$. This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current ( 0.2 mA ) and the required output voltage $\left(\mathrm{V}_{\mathrm{OH}}\right)$ to reach the current sense comparator's 1.0 V clamp level:

$$
\mathrm{R} 1(\mathrm{~min})=\frac{(3 \times 1 \mathrm{~V})+1.4 \mathrm{~V}}{0.2 \mathrm{~mA}}=22 \mathrm{k} \Omega
$$

## Current Sense Comparator and PWM Latch

The MC44605 operates as a current mode controller. The circuit uses a current sense comparator to compare the inductor current to the threshold level established by the Error Amplifier output (Pin 13). When the current reaches the threshold, the current sense comparator terminates the output switch conduction that has been initiated by the oscillator, by resetting the PWM Latch. Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. This configuration ensures that only one single pulse appears at the Source Output during the appropriate oscillator cycle.


Figure 2. Output Totem Pole
The inductor current is converted to a voltage by inserting the ground referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ in series with the power switch Q1.

This voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$
\mathrm{I}_{\mathrm{pk}} \approx \frac{\mathrm{~V}_{(\mathrm{pin} 13)}-1.4 \mathrm{~V}}{3 \times \mathrm{R}_{\mathrm{S}}}
$$

The Current Sense Comparator threshold is internally clamped to 1.0 V . Therefore the maximum peak switch current is:

$$
\mathrm{I}_{\mathrm{pk}(\max )}=\frac{1 \mathrm{~V}}{\mathrm{R}_{\mathrm{S}}}
$$

## Undervoltage Lockout Section

As depicted in Figure 3, an undervoltage lockout has been incorporated to guarantee that the IC is fully functional before allowing the system working.

In effect, the $\mathrm{V}_{\mathrm{CC}}$ is connected to the non inverting input of a comparator that has an upper threshold equal to $14,5 \mathrm{~V}$ (typical $\mathrm{V}_{\text {stup-th }}$ ) and a lower one equal to 7.5 V (typical $\mathrm{V}_{\text {disable 2). This }}$ hysteresis comparator enables or disables the reference block that generates the voltage and current sources required by the system.

This block particularly, produces $\mathrm{V}_{\text {ref }}$ (pin 16 voltage) and $\mathrm{I}_{\text {ref }}$ that is determined by the resistor $\mathrm{R}_{\text {ref }}$ connected between pin 16 and the ground:

$$
I_{\text {ref }}=\frac{V_{\text {ref }}}{R_{\text {ref }}} \text { where } V_{\text {ref }}=2.5 \mathrm{~V} \text { (typically) }
$$



Figure 3. $\mathrm{V}_{\mathrm{CC}}$ Management
In addition to this, $\mathrm{V}_{\mathrm{CC}}$ is compared to a second threshold level that is nearly equal to $9 \mathrm{~V}\left(\mathrm{~V}_{\text {disable1 }}\right)$ so that a signal UVLO1 is generated to reset the soft start block and so, to disable the output stage (refer to the Soft-Start §) as soon as $\mathrm{V}_{\mathrm{CC}}$ becomes lower than $\mathrm{V}_{\text {disable 1 }}$. In this way, the circuit is reset and made ready for a next start-up, before the reference block is disabled (refer to Figure 3). Thus, finally the upper limit for the minimum normal operating voltage
is 9.4 V (maximum value of $\mathrm{V}_{\text {disable 1 }}$ ) and so the minimum hysteresis is 4.2 V . $\left[\left(\mathrm{V}_{\text {stup-th }}\right)_{\min }=13.6 \mathrm{~V}\right]$.

The large hysteresis and the low start-up current of the MC44605 make it ideally suited for off-line converter applications where efficient bootstrap start-up techniques are required.

## Soft-Start Control Section

The $\mathrm{V}_{\mathrm{cs}}$ value is clamped down to the pin 11 voltage.
So, if a capacitor is connected to this pin, its voltage increases slowly at the start-up (the capacitor is charged by an internal current source $0.4 \mathrm{I}_{\text {ref }}$ ). So, $\mathrm{V}_{\text {cs }}$ is limited during the start-up and then a soft-start is performed.

This pin can be used to inhibit the circuit by applying a voltage that is lower than $\mathrm{V}_{\text {SSinhi }}$ (refer to page 4). Particularly, the MC44605 can be shutdown by connecting the soft-start pin to ground.

As soon as $\mathrm{V}_{\text {dis } 1}$ is detected (that is $\mathrm{V}_{\mathrm{cc}}$ lower than $\mathrm{V}_{\text {disable1 }}$ ), a signal UVLO1 is generated until the $\mathrm{V}_{\mathrm{cc}}$ falls down to $\mathrm{V}_{\mathrm{dis} 2}$ (refer to the undervoltage lockout section §). During the delay between the disable1 and the disable2, using a transistor controlled by UVLO1, the pin 11 voltage is made equal to zero in order to make the soft-start arrangement ready to work for the next re-start.


Figure 4. Soft-Start

## Oscillator Section (Figures 5 \& 5b)

The oscillator and synchronization behavior is represented in Figure 5b.

The MC44605 oscillator achieves four functions:

- it fixes the free mode frequency
- it takes into account the synchronization signal
- it does not allow a new power switch conduction if the flyback is not in a dead-time state when the circuit works in demagnetization mode (pin 8 connected)
- it builds the Sf pulse required by the MPL block

During the operating mode, the oscillator sawtooth can vary between a valley value ( 1.6 V typically) and a peak one (3.6 V typically) and presents three distinct phases:

- the $\mathrm{C}_{\mathrm{T}}$ charge
- the $\mathrm{C}_{\mathrm{T}}$ discharge
- the phase during which the oscillator voltage is maintained equal to its valley value. This happens at the end of a discharge cycle when the synchronization or demagnetization condition does not allow a new $\mathrm{C}_{\mathrm{T}}$ charge phase. During this sequence, $\mathrm{I}_{\text {REGUL }}$ compensates the charge current $\mathrm{I}_{\text {charge }}$.
The oscillator has two working modes:
- a free one when there is no synchronization
- a synchronized one.

In the free working, the oscillator grows up from its valley value to its peak one for the charge phase and when once the peak value is reached, a discharge sequence makes the $\mathrm{C}_{\mathrm{T}}$ voltage decrease down to its valley value. When the decrease phase is finished, a new charge cycle occurs if the demagnetization condition is achieved $\left(\mathrm{V}_{\mathrm{DT}}\right.$ high). Otherwise there is a REGUL phase until $\mathrm{V}_{\text {DT }}$ gets high.

In the synchronized mode, the charge cycle is only allowed when the synchronization signal gets high while a dead time has been detected ( $\mathrm{V}_{\mathrm{DT}}$ high). This charge phase is stopped when the synchronization signal has got low and when the oscillator voltage is higher than $\mathrm{V}_{\mathrm{int}}$, the intermediary voltage level used to generate the calibrated pulse Sf by comparing the $\mathrm{C}_{\mathrm{T}}$ voltage to this threshold. So, when these two conditions are performed, a discharge sequence is set until the oscillator voltage is equal to its valley value. Then, the $\mathrm{C}_{\mathrm{T}}$ voltage is maintained constant thanks to the "REGUL" arrangement until the next synchronization pulse.

In both cases, during the charge phase, a signal $\mathrm{V}_{\mathrm{S}}$ is generated. When Sf becomes high. $\mathrm{V}_{\mathrm{S}}$ gets high and remains in this state until the PWN latch is set of Sf is low. Then, $\mathrm{V}_{\mathrm{S}}$ keeps low until the next Sf high level. This oscillator behavior is obtained using the process described in Figure 5b.

$\square \mathrm{b}$-Synchronized mode


Figure 5b. Oscillator Behavior

In effect, the output of the latch L1 is:

- high during the oscillator capacitor charge and during the REGUL phase
- low for the oscillator capacitor discharge

Now, the latch L2 is set when the L1 output is high and the synchronization condition is performed (that is: sync $=1-$ free mode or synchro signal high state) and during the dead-time ( $\mathrm{V}_{\mathrm{DT}}$ high). So, this latch is set for the $\mathrm{C}_{\mathrm{T}}$ charge.

On the other hand, this latch is reset by the signal used to reset L1. Consequently, it is reset at the end of the charge phase.

So, in any case, $\mathrm{Q}_{\mathrm{L} 2}$ is:

- high during the $\mathrm{C}_{\mathrm{T}}$ charge cycle
- low in the other cases

Thus, this latch enables to obtain a signal that is high for the charge phase and low in the other cases, whatever the mode (synchronized or free) and whatever the synchronization pulses width (higher than the delay necessary for the oscillator to reach its intermediary value or lower than this delay) in the synchronized mode.

That is why:

- the discharge current source must be connected to the oscillator capacitor when $\mathrm{Q}_{\mathrm{L} 1}$ is low. The condition $\left(\mathrm{C}_{\mathrm{T}}\right.$ voltage higher than the valley value) is added to stop the discharge phase as soon as the oscillator voltage is detected as lower than the valley value (without any delay due to the L1 latch propagation time).
- the REGUL current source must be connected when:
- $\mathrm{Q}_{\mathrm{L} 1}$ is high (charge or REGUL phase)
- $\mathrm{Q}_{\mathrm{L} 2}$ is low (the oscillator is not in a charge phase)

On the other hand, the oscillator charge is stopped when:

- the oscillator voltage reaches the peak value in the free mode
- the oscillator voltage is higher than the intermediary value $\left(\mathrm{V}_{\mathrm{int}}\right)$ and the synchronization signal is negative, in the synchronized mode.
Consequently, in any case, $\mathrm{Q}_{\mathrm{L} 2}$ that is high during the oscillator charge phase, is high for the delay during which the oscillator voltage grows from the valley value up to the intermediary one. That is why the signal Sf (refer to the MPL block) that must be high when the oscillator voltage is between the valley value and the intermediary one during the charge phase ( $\mathrm{Q}_{\mathrm{L} 2}$ high), is obtained using an AND gate with the following inputs:
- $\mathrm{Q}_{\mathrm{L} 2}$ ( $\mathrm{Q}_{\mathrm{L} 2}$ high $\Leftrightarrow$ charge phase)
- Coscint (Coscint high $\Leftrightarrow$ the $\mathrm{C}_{\mathrm{T}}$ voltage is lower than the intermediary value).
So, using the output of this AND gate, Sf is obtained.
This signal Sf is connected to a logic block consisting of two AND gates and an OR one. This block aims at supplying a signal VS that:
- gets high as soon as Sf becomes high if the PWM latch output is low
- gets low as soon as the PWM latch is set and then remains low until the next cycle.


Figure 5. Oscillator

## Synchronization Section (Note 1)

The synchronization block consists of a protection arrangement similar to the demagnetization block one (a diode + a negative active clamping system (Note 2)). In addition to this, a high value resistor ( R - about $50 \mathrm{k} \Omega$ ) is incorporated as the pin 9 input is also used by the EHTOVP section.

The signal obtained at the output of this protection arrangement, is compared to a negative threshold ( -200 mV , typically) so that when the synchronization pulse applied to the pin 9 (through a resistor or a resistors divider to adapt this input to the EHTOVP function), is higher than this threshold, the system considers that the synchronization condition is performed (free mode or synchronization signal high level).
Note 1. The synchronization can be inhibited by connecting the pin 9 to the ground. By this means, a free mode is obtained.
Note 2. This negative active clamping system works even if the circuit is off. This feature is really useful as synchronization pulses may be applied while the product is off.


Figure 6. Synchronization

## Demagnetization Section

This block is incorporated to detect the complete core demagnetization in order to prevent the power MOSFET from switching on if the converter is not in a dead time phase. That is why this block inhibits any oscillator re-start as long as the inductor current is not finished (from the beginning of the on-time to the end of the demagnetization phase).

In a fly-back, a good means to detect the demagnetization phase consists in using the $\mathrm{V}_{\mathrm{CC}}$ winding voltage. In effect, this voltage is:

- negative during the on-time,
- positive during the off-time,
- equal to zero for the dead-time with generally a ringing (refer to Figure 7).


Figure 7. Demagnetization Detection

That is why, the MC44605 demagnetization detection consists of a comparator that compares the $\mathrm{V}_{\mathrm{CC}}$ winding voltage to a reference that is typically equal to 65 mV .

A diode D is incorporated to clamp the positive applied voltages while an active clamping system limit the negative voltages to typically -0.33 V . This negative clamp level is high enough to avoid the substrate diode switching on.

A latch system is incorporated to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output (refer to Figure 8). This process avoids that any ringing on the signal used on the pin 8, disrupts the demagnetization detection (refer to Figure 7). Finally, this method results in a very accurate demagnetization phase detection, and the signal $\mathrm{V}_{\mathrm{DT}}$ drawn from this block is high only for the dead time. Therefore, an oscillator re-start and so, a new power switch conduction is only allowed during the dead-time.

For a higher safety, the $V_{\text {demagout }}$ output of the demagnetization block is also directly connected to the output, to disable it during the demagnetization phase (refer to the block diagram).

The demagnetization detection can be inhibited by connecting pin 8 to the ground but in this case, a timer (about $3 \mu \mathrm{~s}$ ) that is incorporated to set the latch when it can not be set by $\mathrm{V}_{\text {demagout }}$, results in a minimum off-time (refer to Figure 8).


Figure 8. Demagnetization Block

## Overvoltage Protection Section

The overvoltage arrangement compares a portion $\mathrm{V}_{\mathrm{cc}}$ to $\mathrm{V}_{\text {ref }}(2,5 \mathrm{~V})$ (refer to Figure 9). In fact, this threshold corresponds to a $\mathrm{V}_{\mathrm{CC}}$ equal to to 17 V . When the $\mathrm{V}_{\mathrm{cc}}$ is higher than this level, the output is latched off until a new circuit re-start.


Figure 9. Overvoltage Protection

A delay $(2 \mu \mathrm{~s})$ is incorporated in order to avoid any activation due to interferences by only taking into account the overvoltages that last at least $2 \mu \mathrm{~s}$.

The $\mathrm{V}_{\mathrm{CC}}$ is connected when once the circuit has started-up in order to limit the circuit start-up consumption ( T is switched on when once $\mathrm{V}_{\text {ref }}$ has been generated).

The overvoltage section is enabled $5 \mu \mathrm{~s}$ after the regulator has started to allow the reference $\mathrm{V}_{\text {ref }}$ to stabilize.

## E.H.T. Overvoltage Protection Section

This block uses the synchronization input as this section is incorporated to detect too high synchronization pulses and then to activate the device definitive latch in this case.


Figure 10. E.H.T. OVP
This block consists of a high impedance resistors bridge ( R is nearly equal to $50 \mathrm{k} \Omega$ - refer to Figure 10) so that the EHTovp threshold is 7.5 V . So, using an external resistors bridge (r1, r2 $\ll \mathrm{R}$ ), the synchronization pulse level above which the working must be considered as wrong, can be adjusted.

For instance, if this threshold value is required to be equal to $30 \mathrm{~V}, \mathrm{~V}_{\text {pin9 }}$ must be equal to 7.5 V when the synchronization pulse value is 30 V .

So, in this case:

$$
30 \times \frac{r 2}{r 1+r 2}=7.5
$$

Then, the ratio ( $\mathrm{r} 1 / \mathrm{r} 2$ ) can be deducted:

$$
\frac{\mathrm{r} 1}{\mathrm{r} 2}=3
$$

So, as r 1 and r 2 must be negligible in relation to R (about $50 \mathrm{k} \Omega$ ), the couple of resistors can be chosen as follows:

$$
\mathrm{r} 1=3 \mathrm{k} \Omega
$$

and:

$$
\mathrm{r} 2=1 \mathrm{k} \Omega
$$

## Winding Short Circuit Detection Section (WSCD)

The MC44605 being designed to control a Fly-Back SMPS, this block is incorporated to detect a short circuit on a transformer winding or on an output diode (refer to Figure 11).


Figure 11. Winding Short Circuit Fault

In the case of a Winding Short Circuit, the primary inductor $L_{p}$ is short circuited and then the current increase is only controlled by the leakage inductor $\mathrm{L}_{\text {leak }}$.

In current mode, the power switch conduction is stopped when the inductor current is detected as high enough, by the controller. In fact, when the current sense resistor ( $\mathrm{R}_{\mathrm{s}}$ ) voltage gets equal to $\mathrm{V}_{\mathrm{cs}}$, the current sense comparator switches to reset the output.
Now, the circuit has a propagation delay and the power switch needs some time to turn off. Consequently, there is a delay $\delta$ t between the moment at which the $\mathrm{R}_{\mathrm{S}}$ voltage gets equal to $\mathrm{V}_{\mathrm{cs}}$ and the actual current increase stop. So, this results in an overcurrent (refer to Figure 12).


Figure 12. Overcurrent in a WSCD Case

Now, in normal working, this overcurrent $\Delta \mathrm{Ipk}$ is equal to:

$$
\Delta \mathrm{lpk}=\frac{\operatorname{Vin} \times \delta \mathrm{t}}{\mathrm{~L}_{\mathrm{P}}}
$$

where: $\mathrm{V}_{\mathrm{in}}$ is the input voltage (rectified a.c. line)
While in a WSCD case:

$$
(\Delta \mathrm{lpk})_{\mathrm{WSCD}}=\frac{\mathrm{Vin} \times \delta \mathrm{t}}{\mathrm{~L}_{\text {Leak }}}
$$

Consequently, as the leakage inductor value is generally much lower than the primary one (less than 5\% generally), the overcurrent is much higher in the WSCD case. That is why this fault can be detected by detecting the high overcurrents.

So, the WSCD block consists of comparing the sensed current to a reference equal to: $\left(\mathrm{V}_{\mathrm{cs}}+\mathrm{V}_{\text {shift }}\right)$, where $\mathrm{V}_{\text {shift }}$ is a voltage proportional to the current injected in the pin 15 (refer to Figure 13).


Figure 13. WSCD
Now, as the overcurrent level depends on the input voltage $\mathrm{V}_{\mathrm{in}}$, it is preferable to use a $\mathrm{V}_{\text {shift }}$ proportional to this input voltage instead of a constant $\mathrm{V}_{\text {shift }}$. So, the WSCD pin must be connected to $\mathrm{V}_{\text {in }}$ through a resistor that fixes $\mathrm{V}_{\text {shift }}$ by adjusting the current injected in this pin 15.

Finally, when there is a winding short circuit, an overcurrent is detected by the WSCD comparator. The output of this comparator, $\mathrm{V}_{\mathrm{WSCD}}$, is connected to the disabling block (refer to the disabling block §).

## Maximum Power Limitation Section (MPL)

The MPL block is designed to calculate this input power using the following equation:

$$
\operatorname{Pin}=\frac{1}{2} \times L_{P} \times \mathrm{lpk}^{2} \times \mathrm{f}
$$

where: Lp is the inductor value
Ipk is the inductor peak current
f is the switching frequency
As $\mathrm{V}_{\mathrm{cs}}$ is proportional to the inductor peak current ( $\mathrm{V}_{\mathrm{cs}}=\mathrm{R}_{\mathrm{s}} \mathrm{x}$ Ipk), the squared Ipk value is estimated by building a current source proportional to $\mathrm{V}_{\mathrm{cs}}{ }^{2}$. This current is chopped by a calibrated pulse Sf , generated at each new oscillator cycle (refer to Figure 14).
Finally, using an external resistor and capacitor network $\left(\mathrm{R}_{\mathrm{MPL}}, \mathrm{C}_{\mathrm{MPL}}\right)$ on the MPL pin, a voltage $\mathrm{V}_{\text {MPL }}$, proportional to the input power can be obtained.
In effect,

$$
V_{M P L}=R_{M P L} \times k_{M P L} \times V_{c s}{ }^{2} \times \frac{(\mathrm{Sf})}{\mathrm{T}}
$$

where: $\mathrm{k}_{\mathrm{MPL}}$ is the multiplier gain
$(\mathrm{Sf})$ is the width of the calibrated pulse
T is the switching (oscillator) period
Now, as Sf is built comparing the oscillator to a constant level, (Sf) is proportional to $\mathrm{R}_{\text {ref }}$ and $\mathrm{C}_{\mathrm{T}}$ :

$$
(\mathrm{Sf})=\mathrm{k} 1 \times \mathrm{R}_{\mathrm{ref}} \times \mathrm{C}_{\mathrm{T}}
$$

where: k 1 is a constant
On the other hand, $\mathrm{k}_{\mathrm{MPL}}$ that is depending on the reference current source $I_{\text {ref }}$, is proportional to $1 / R_{\text {ref }}$ :

$$
\mathrm{k}_{\mathrm{MPL}}=\mathrm{k} 2 \times \frac{1}{\mathrm{R}_{\mathrm{ref}}}
$$

where: k 2 is a constant
So:

$$
\mathrm{V}_{\mathrm{MPL}}=\mathrm{R}_{\mathrm{MPL}} \times \mathrm{k} 1 \times \mathrm{k} 2 \times \mathrm{Vcs}^{2} \times \mathrm{f} \times \mathrm{C}_{\mathrm{T}}
$$

where: $\mathrm{C}_{\mathrm{T}}$ is the oscillator capacitor
Finally:

$$
\mathrm{V}_{\mathrm{MPL}}=\mathrm{R}_{\mathrm{MPL}} \times \Gamma_{\mathrm{MPL}} \times \mathrm{Vcs}^{2} \times \mathrm{f} \times \mathrm{C}_{\mathrm{T}}
$$

where: $\Gamma_{\text {MPL }}$ is the MPL parameter as defined in the specification. This is a constant equal to the product (k1 x k2).

Now, as:

$$
\operatorname{Pin}=\frac{1}{2} \times L_{P} \times \mathrm{lpk}^{2} \times f
$$

and:

$$
\mathrm{Vcs}=\mathrm{R}_{\mathrm{S}} \times \mathrm{lpk}
$$

So:

$$
\mathrm{V}_{\mathrm{MPL}}=\frac{2 \times \mathrm{R}_{\mathrm{MPL}} \times \Gamma_{\mathrm{MPL}} \times \mathrm{C}_{\mathrm{T}} \times \mathrm{R}_{\mathrm{S}}^{2}}{\mathrm{~L}_{\mathrm{P}}} \times \mathrm{Pin}
$$

A comparator is used to compare $\mathrm{V}_{\mathrm{MPL}}$ to $\mathrm{V}_{\text {ref }}$, the output of which, Dis ${ }_{\text {MPL }}$, is connected to the "definitive inhibition latch" of the disabling block. So, when the calculated power is higher than the threshold, the circuit is definitively disabled (the system considers that there is an overload condition).

Finally, replacing $\mathrm{V}_{\mathrm{MPL}}$ by 2.5 V (the threshold value), the $\mathrm{R}_{\mathrm{MPL}}$ value to be used, can be deducted:


Figure 14. OHD and MPL

## Overheating Detection Section (O.H.D.)

In the MPL block, the converter input power is calculated. In the O.H.D. block, that is the power MOSFET heating which is calculated, using the following equation:

$$
\mathrm{p}_{\mathrm{on}}=\frac{1}{3} \times \mathrm{R}_{\mathrm{dson}} \times \mathrm{Ipk}^{2} \times \mathrm{d}
$$

where: $\mathrm{p}_{\mathrm{on}}$ are the power switch on-time losses
$\mathrm{R}_{\text {dson }}$ is the conduction MOSFET resistor d is the duty cycle

As in the MPL section, the squared Ipk term is estimated by building a current source proportional to $\mathrm{Vcs}^{2}$.

The duty cycle is taken into account thanks to the action on this current source of a "chopper" controlled by the circuit output. By this means, the pin 6 average current is proportional to the squared peak current multiplied to the duty cycle (refer to Figure 14).

So, using an external resistor and capacitor network ( $\mathrm{R}_{\mathrm{OHD}}, \mathrm{C}_{\mathrm{OHD}}$ ) on this pin, a voltage $\mathrm{V}_{\mathrm{OHD}}$, proportional to the conduction losses can be obtained.

Like in the MPL block, this voltage $\mathrm{V}_{\mathrm{OHD}}$, is compared to 2.5 V . If $\mathrm{V}_{\mathrm{OHD}}$ gets higher than this threshold, the disabling block is activated by $\mathrm{Dis}_{\mathrm{OHD}}$ (output of the comparator).

The external resistor $\mathrm{R}_{\mathrm{OHD}}$ choice enables to obtain a calculated $\mathrm{V}_{\mathrm{OHD}}$ equal to 2.5 V when the conduction losses are equal to their maximum value.
In effect,

$$
\mathrm{v}_{\mathrm{OHD}}=\mathrm{R}_{\mathrm{OHD}} \times \mathrm{k}_{\mathrm{OHD}} \times \mathrm{Vcs}^{2} \times \mathrm{d}
$$

where: $\mathrm{k}_{\mathrm{OHD}}$ is the multiplier gain
Now, as $\mathrm{k}_{\mathrm{OHD}}$ that is depending on the reference current source $I_{\text {ref }}$, is proportional to $1 / R_{\text {ref }}$ :

$$
\mathrm{k}_{\mathrm{OHD}}=\mathrm{k} 2 \times \frac{1}{\mathrm{R}_{\mathrm{ref}}}
$$

where: k 2 is a constant
So:

$$
\mathrm{V}_{\mathrm{OHD}}=\mathrm{R}_{\mathrm{OHD}} \times \mathrm{k} 2 \times \frac{\mathrm{Vcs}^{2}}{R_{\text {ref }}} \times \mathrm{d}
$$

Finally:

$$
\mathrm{v}_{\mathrm{OHD}}=\frac{\mathrm{R}_{\mathrm{OHD}} \times \Gamma_{\mathrm{OHD}} \times \mathrm{Vcs}^{2} \times \mathrm{d}}{R_{\mathrm{ref}}}
$$

where: $\Gamma_{\text {OHD }}$ is the OHD parameter as defined in the specification. This is a constant equal to k 2 .
Now, as:

$$
\mathrm{Vcs}=\mathrm{R}_{\mathrm{S}} \times \mathrm{lpk}
$$

So, replacing Vcs and using the $\mathrm{p}_{\mathrm{on}}$ equation:

$$
\mathrm{v}_{\mathrm{OHD}}=\frac{3 \times \mathrm{R}_{\mathrm{OHD}} \times \Gamma_{\mathrm{OHD}} \times \mathrm{R}_{\mathrm{S}}^{2}}{\mathrm{R}_{\mathrm{ref}} \times \mathrm{R}_{\mathrm{dson}}} \times \mathrm{p}_{\mathrm{on}}
$$

So, by choosing the value of $\mathrm{R}_{\mathrm{OHD}}$, the heating corresponding to $\mathrm{V}_{\text {ref }}$ is determined. If the MOSFET dissipation is such that the heating is higher than this threshold, the "definitive inhibition latch" of the Disabling Block is activated and so, the output gets definitively disabled.

Consequently, by replacing $\mathrm{V}_{\mathrm{OHD}}$ by 2.5 V (threshold value) in the last equation, the value $\mathrm{R}_{\mathrm{OHD}}$ to use, can be deducted:

$$
\mathrm{R}_{\mathrm{OHD}}=\frac{2.5 \times \mathrm{R}_{\mathrm{ref}} \times \mathrm{R}_{\mathrm{dson}}}{3 \times \Gamma_{\mathrm{OHD}} \times \mathrm{R}_{\mathrm{S}}^{2} \times\left(\mathrm{p}_{\mathrm{on}}\right)_{\max }}
$$

where: $\left(\mathrm{p}_{\mathrm{on}}\right)_{\max }$ are the maximum on time losses that are acceptable.

## Disabling Block Section

This section consists of a "definitive inhibition latch" (directly supplied by the $\mathrm{V}_{\mathrm{cc}}$ ) that disables the output (the output is forced to zero).

In effect, this block aims at definitively disabling the circuit when one of the following faults is detected:
— a Winding Short Circuit

- too high synchronization pulses
- a too high input power
- a too high power switch (MOSFET) heating

The signals corresponding to these faults are high when a fault is detected (for instance, when the input power is detected as too high, DismPL is high).

When one (or several) of these four faults is detected, a current source charges $\mathrm{C}_{\text {ext }}$ (with a certain duty cycle) and when its voltage becomes higher than $\mathrm{V}_{\text {ref }}$, the definitive inhibition latch is activated. Thus, the circuit gets definitively disabled after a delay depending on $\mathrm{C}_{\text {ext }}$.

According to the detected fault, the current that charges $\mathrm{C}_{\text {ext }}$ is not the same:

The typical values are:

- $260 \mu \mathrm{~A}$ for EHTOVP and WSCD
- $8.5 \mu \mathrm{~A}$ for OHD and MPL
when $R_{r e f}$ is equal to $10 \mathrm{k} \Omega$.


Figure 15. Disabling Block
This latch is reset when the $\mathrm{V}_{\mathrm{cc}}$ falls down to about 3 V . In this case, if a new start up is performed, the circuit will work normally (until this fault or another one is detected).
Practically, to re-start after a fault has shutdown the circuit, the converter must be turned off for a time long enough to enable the $\mathrm{V}_{\mathrm{cc}}$ capacitor discharge (repair time...).
Note: As $V_{\text {WSCD }}$ is generally a really narrow pulse, it is necessary to add a latch and a delay to build a $4 \mu$ s width pulse when $\mathrm{V}_{\text {WSCD }}$ becomes high.

## Application Schematic



65 W output SMPS controlled by the MC44605
Mains input range: 90 Vac <-> 264 Vac
Synchronization range: $\mathbf{3 0} \mathbf{~ k H z ~ < - > ~} 100$ kHz
Orega Transformer ref. G5984-00
(Lp = $195 \mu \mathrm{H}$ )

## MC44605

## Performances

| Input Voltage | 90-260 Vac |  |  |
| :---: | :---: | :---: | :---: |
| Synchronization Range | 30 to 100 kHz |  |  |
| Outputs | 160 V |  | 100 mA |
|  | 70 V |  | 200 mA |
|  | 40 V |  | 500 mA |
|  | 13.5 V |  | 650 mA |
|  | 8 V |  | 500 mA |
| Measured Efficiency$\text { (Pout = } 64 \mathrm{~W} \text { ) }$ | 30 kHz | 110 Vac (Input) | 80\% |
|  |  | 220 Vac | 83\% |
|  | 60 kHz | 110 Vac | 81\% |
|  |  | 220 Vac | 82\% |
|  | 100 kHz | 110 Vac | 80\% |
|  |  | 220 Vac | 80\% |
| Standby Losses (No Load - Pout $=0$ ) | 110 Vac |  | 2.0 W |
|  | 220 Vac |  | 3.2 W |
| EHTovp Threshold | 28 V |  |  |
| Maximum Power Limitation | 30 kHz | 110 Vac (Input) | 86 W (Input) |
|  |  | 220 Vac | 87 W |
|  | 60 kHz | 110 Vac | 90 W |
|  |  | 220 Vac | 95 W |
|  | 100 kHz | 110 Vac | 94 W |
|  |  | 220 Vac | 110 W |
| Overheating Detection (Pout = 64 W ): <br> The input rms levels at which the circuit detects an OHD case. | 30 kHz |  | 85 V |
|  | 60 kHz |  | 76 V |
|  | 100 kHz |  | 76 V |
| Winding Short Circuit Detection | Fully Functional (Tested by short circuiting one output diode or one transformer winding) |  |  |

## CS51021A, CS51022A, CS51023A, CS51024A

## Enhanced Current Mode PWM Controller

The CS51021A/2A/3A/4A Fixed Frequency PWM Current Mode Controller family provides all necessary features required for AC-DC or DC-DC primary side control. Several features are included eliminating the additional components needed to implement them externally. In addition to low start-up current $(75 \mu \mathrm{~A})$ and high frequency operation capability, the CS51021A/2A/3A/4A family includes overvoltage and undervoltage monitoring, externally programmable dual threshold overcurrent protection, current sense leading edge blanking, current slope compensation, accurate duty cycle control and an externally available 5.0 V reference. The CS51021A and CS51023A feature bidirectional synchronization capability, while the CS51022A and CS51024A offer a sleep mode with $100 \mu \mathrm{~A}$ maximum IC current consumption. The CS51021A/2A/3A/4A family is available in a 16 lead narrow body SO package.

| Device | Sleep/Synch | $\mathbf{V}_{\text {CC }}$ Start/Stop |
| :--- | :---: | :---: |
| CS51021A | Synch | $8.25 \mathrm{~V} / 7.7 \mathrm{~V}$ |
| CS51022A | Sleep | $8.25 \mathrm{~V} / 7.7 \mathrm{~V}$ |
| CS51023A | Synch | $13 \mathrm{~V} / 7.7 \mathrm{~V}$ |
| CS51024A | Sleep | $13 \mathrm{~V} / 7.7 \mathrm{~V}$ |

## Features

- $75 \mu \mathrm{~A}$ Max. Startup Current
- Fixed Frequency Current Mode Control
- 1.0 MHz Switching Frequency
- Undervoltage Protection Monitor
- Overvoltage Protection Monitor with Programmable Hysteresis
- Programmable Dual Threshold Overcurrent Protection with Delayed Restart
- Programmable Soft Start
- Accurate Maximum Duty Cycle Limit
- Programmable Slope Compensation
- Leading Edge Current Sense Blanking
- 1.0 A Sink/Source Gate Drive
- Bidirectional Synchronization (CS51021A/3A)
- 50 ns PWM Propagation Delay
- $100 \mu \mathrm{~A}$ Max Sleep Current (CS51022A/4A)


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51021AED16 | SO-16 | 48 Units/Rail |
| CS51021AEDR16 | SO-16 | 2500 Tape \& Reel |
| CS51022AED16 | SO-16 | 48 Units/Rail |
| CS51022AEDR16 | SO-16 | 2500 Tape \& Reel |
| CS51023AED16 | SO-16 | 48 Units/Rail |
| CS51023AEDR16 | SO-16 | 2500 Tape \& Reel |
| CS51024AED16 | SO-16 | 48 Units/Rail |
| CS51024AEDR16 | SO-16 | 2500 Tape \& Reel |

[^34]
## CS51021A, CS51022A, CS51023A, CS51024A



Figure 1. Typical Application Diagram, 36-72 V to 5.0 V, 5.0 A DC-DC Converter

MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Power Supply Voltage, $\mathrm{V}_{\mathrm{CC}}$ | $-0.3,20$ | V |
| Driver Supply Voltage, $\mathrm{V}_{\mathrm{C}}$ | $-0.3,20$ | V |
| SYNC, SLEEP, R $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$, SOFT START, $\mathrm{V}_{\text {FB }}$, SLOPE, ISENSE, UV, OV, ISET (Logic Pins) | 0.25 to $\mathrm{V}_{\text {REF }}$ | V |
| Peak GATE Output Current | 1.0 | A |
| Steady State Output Current | $\pm 0.2$ | A |
| Operating Junction Temperature, $\mathrm{T}_{\mathrm{J}}$ | Reflow: (SMD styles only) (Note 1) | 230 peak |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ | ${ }^{\circ} \mathrm{C}$ |  |
| ESD (Human Body Model) | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## CS51021A, CS51022A, CS51023A, CS51024A

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, specifications apply for $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$,
$-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}, 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<20 \mathrm{~V}, 8.2 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Under Voltage Lockout |  |  |  |  |  |
| START Threshold (CS51021A/2A) | - | 7.95 | 8.25 | 8.8 | V |
| START Threshold (CS51023A/4A) | - | 12.4 | 13 | 13.4 | V |
| STOP Threshold | - | 7.4 | 7.7 | 8.2 | V |
| Hysteresis (CS51021A/2A) | - | 0.50 | 0.75 | 1.00 | V |
| Hysteresis (CS51023A/4A) | - | 4.0 | 5.0 | 6.0 | V |
| Icc @ Startup (CS51021A/2A) | $\mathrm{V}_{\text {CC }}<\mathrm{UV}_{\text {START }}$ Threshold | - | 40 | 75 | $\mu \mathrm{A}$ |
| ICC @ Startup (CS51023A/4A) | $\mathrm{V}_{\text {CC }}<\mathrm{UV}_{\text {START }}$ Threshold | - | 45 | 75 | $\mu \mathrm{A}$ |
| ICC Operating (CS51021A/3A) | - | - | 7.0 | 9.0 | mA |
| $I_{\text {CC }}$ Operating (CS51022A/4A) | - | - | 6.0 | 8.0 | mA |
| $I_{\text {CC }}$ Operating | Includes 1.0 nF Load | - | 7.0 | 12 | mA |

Voltage Reference

| Initial Accuracy | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V}$, Note 2 | 4.95 | 5.0 | 5.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Total Accuracy | $1.0 \mathrm{~mA}<\mathrm{I}_{\mathrm{REF}}<10 \mathrm{~mA}$ | 4.9 | 5.0 | 5.15 | V |
| Line Regulation | $8.2 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<18 \mathrm{~V}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA}$ | - | 6.0 | 20 | mV |
| Load Regulation | $1.0 \mathrm{~mA}<\mathrm{I}_{\text {REF }}<10 \mathrm{~mA}$ | - | 6.0 | 15 | mV |
| NOISE Voltage | Note 2 | - | 50 | - | $\mu \mathrm{C}$ |
| OP Life Shift | $\mathrm{T}=1000$ Hours, Note 2 | - | 4.0 | 20 | mV |
| FAULT Voltage | Force $\mathrm{V}_{\text {REF }}$ | $0.90 \times \mathrm{V}_{\text {REF }}$ | $0.93 \times \mathrm{V}_{\text {REF }}$ | $0.95 \times \mathrm{V}_{\text {REF }}$ | V |
| OK Voltage | Force $\mathrm{V}_{\text {REF }}$ | $0.94 \times \mathrm{V}_{\text {REF }}$ | $0.96 \times \mathrm{V}_{\text {REF }}$ | $0.985 \times \mathrm{V}_{\text {REF }}$ | V |
| OK Hysteresis | Force $\mathrm{V}_{\text {REF }}$ | 75 | 165 | 250 | mV |
| Current Limit | Force $\mathrm{V}_{\text {REF }}$ | -20 | - | - | mA |

Error Amplifier

| Initial Accuracy | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{REF}}=2.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}, \mathrm{Note} 2$ | 2.465 | 2.515 | 2.565 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Reference Voltage | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ | 2.440 | 2.515 | 2.590 | V |
| $\mathrm{~V}_{\mathrm{FB}}$ Leakage Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | -0.2 | -2.0 | $\mu \mathrm{~A}$ |
| Open Loop Gain | $1.4 \mathrm{~V}<\mathrm{COMP}<4.0 \mathrm{~V}$, Note 2 | 60 | 90 | - | dB |
| Unity Gain Bandwidth | Note 2 | 1.5 | 2.5 | - | MHz |
| COMP Sink Current | $\mathrm{COMP}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 2.0 | 6.0 | - | mA |
| COMP Source Current | $\mathrm{COMP}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ | -0.2 | -0.5 | - | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=2.3 \mathrm{~V}$ | 4.35 | 4.8 | 5.0 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 0.4 | 0.8 | 1.2 | V |
| PS Ripple Rejection | $\mathrm{FREQ}=120 \mathrm{~Hz}$, Note 2 | 60 | 85 | - | dB |
| SS Clamp, $\mathrm{V}_{\mathrm{COMP}}$ | $\mathrm{V}_{\mathrm{SS}}=2.5 \mathrm{~V}, \mathrm{~V}$ FB $=0 \mathrm{~V}, \mathrm{I}_{\mathrm{SET}}=2.0 \mathrm{~V}$ | 2.4 | 2.5 | 2.6 | V |
| IIM(SET) Clamp | Note 2 | 0.95 | 1.0 | 1.15 | V |

2. Guaranteed by design, not $100 \%$ tested in production.

## CS51021A, CS51022A, CS51023A, CS51024A

ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise stated, specifications apply for $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$, $\left.-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}, 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<20 \mathrm{~V}, 8.2 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}\right)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Oscillator |  |  |  |  |  |
| Accuracy | $\mathrm{R}_{\mathrm{T}}=12 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$ | 230 | 255 | 280 | kHz |
| Voltage Stability | Delta Frequency 8.2 $\mathrm{V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V}$ | - | 2.0 | 3.0 | \% |
| Temperature Stability | $\mathrm{T}_{\text {MIN }}<\mathrm{T}_{\text {A }}<\mathrm{T}_{\text {MAX }}$, Note 3 | - | 8.0 | - | \% |
| Min Charge \& Discharge Time | Note 3 | 0.333 | - | - | $\mu \mathrm{s}$ |
| Duty Cycle Accuracy | $\mathrm{R}_{\mathrm{T}}=12 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$ | 70 | 77 | 83 | \% |
| Peak Voltage | Note 3 | - | 3.0 | - | V |
| Valley Voltage | Note 3 | - | 1.5 | - | V |
| Valley Clamp Voltage | 10 k Resistor to ground on $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ | 1.2 | 1.4 | 1.6 | V |
| Discharge Current | - | 0.8 | 1.0 | 1.2 | mA |
| Discharge Current | TA $=25^{\circ} \mathrm{C}$, Note 3 | 0.925 | 1.0 | 1.075 | mA |

Synchronization (CS51021A/3A)

| Input Threshold | - | 1.0 | 1.5 | 2.7 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Pulsewidth |  | - | 160 | 260 | 400 |
| Output High Voltage | $I_{\text {SYNC }}=100 \mu A$ | 3.5 | 4.3 | 4.8 | V |
| Input Resistance | Note 3 | 35 | 70 | 140 | $\mathrm{k} \Omega$ |
| Drive Delay | SYNC to GATE RESET | 80 | 120 | 150 | ns |
| Output Drive Current | 1.0 k Load | 1.25 | 2.0 | 3.5 | mA |

SLEEP (CS51022A/4A)

| SLEEP Input Threshold | Active High | 1.0 | 1.5 | 2.7 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| SLEEP Input Current | $\mathrm{V}_{\text {SLEEP }}=4.0 \mathrm{~V}$ | 11 | 25 | 46 | $\mu \mathrm{~A}$ |
| $\mathrm{I}_{\text {CC }} @$ SLEEP | $\mathrm{V}_{\text {CC }} \leq 15 \mathrm{~V}$ | - | 50 | 100 | $\mu \mathrm{~A}$ |

## GATE Driver

| HIGH Voltage | Measure $\mathrm{V}_{\mathrm{C}}-\mathrm{GATE}, \mathrm{V}_{\mathrm{C}}=10 \mathrm{~V}, 150 \mathrm{~mA}$ Load | - | 1.5 | 2.2 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| LOW Voltage | Measure GATE - PGND, 150 mA SINK | - | 1.2 | 1.5 | V |
| HIGH Voltage Clamp | $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}, 1.0 \mathrm{nF}$ | 11 | 13.5 | 16 | V |
| LOW Voltage Clamp | Measured at 10 mA Output Current | - | 0.6 | 0.8 | V |
| Peak Current | $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}, 1.0 \mathrm{nF}$, Note 3 | - | 1.0 | - | A |
| UVL Leakage | $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V} \mathrm{measured} \mathrm{at} 0 \mathrm{~V}$ | - | -1.0 | -50 | $\mu \mathrm{~A}$ |
| RISE Time | Load $=1.0 \mathrm{nF}, 1.0 \mathrm{~V}<\mathrm{GATE}<9.0 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 60 | 100 | ns |
| FALL Time | Load $=1.0 \mathrm{nF}, 9.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}$ | - | 15 | 40 | ns |

SLOPE Compensation

| Charge Current | SLOPE = 2.0 V | -63 | -53 | -43 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| COMP Gain | Fraction of slope voltage added to ISENSE, <br> Note 3 | 0.095 | 0.100 | 0.105 | $\mathrm{~V} / \mathrm{V}$ |
| Discharge Voltage | SYNC = 0 V | - | 0.1 | 0.2 | V |

3. Guaranteed by design, not $100 \%$ tested in production.

## CS51021A, CS51022A, CS51023A, CS51024A

ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise stated, specifications apply for $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}$, $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}, 3.0 \mathrm{~V}<\mathrm{V}_{\mathrm{C}}<20 \mathrm{~V}, 8.2 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=12 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{T}}=390 \mathrm{pF}$ )

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Sense |  |  |  |  |  |
| OFFSET Voltage | Note 4 | 0.09 | 0.10 | 0.11 | V |
| Blanking Time | - | - | 55 | 160 | ns |
| Blanking Disable Voltage | Adjust $\mathrm{V}_{\mathrm{FB}}$ | 1.8 | 2.0 | 2.2 | V |
| Second Current Threshold Gain | - | 1.21 | 1.33 | 1.45 | V/V |
| I SENSE Input Resistance | - | - | 5.0 | - | $\mathrm{k} \Omega$ |
| Minimum On Time | GATE High to Low | 30 | 70 | 110 | ns |
| Gain | Note 4 | 0.78 | 0.80 | 0.82 | V/V |

OV \& UV Voltage Monitors

| OV Monitor Threshold | - | 2.4 | 2.5 | 2.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| OV Hysteresis Current | - | -10 | -12.5 | -15 | $\mu \mathrm{~A}$ |
| UV Monitor Threshold | - | 1.38 | 1.45 | 1.52 | V |
| UV Monitor Hysteresis | - | 25 | 75 | 100 | mV |

SOFT START (SS)

| Charge Current | $\mathrm{SS}=2.0 \mathrm{~V}$ | -70 | -55 | -40 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | $\mathrm{SS}=2.0 \mathrm{~V}$ | 250 | 1000 | - | $\mu \mathrm{A}$ |
| Charge Voltage, $\mathrm{V}_{\text {SS }}$ |  | - | 4.4 | 4.7 | 5.0 |
| Discharge Voltage, $\mathrm{V}_{\text {SS }}$ | - | 0.25 | 0.27 | 0.30 | V |

4. Guaranteed by design, not $100 \%$ tested in production.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| 16 Lead SO Narrow |  |  |
| 1 | GATE | External power switch driver with 1.0 A peak capability. |
| 2 | $I_{\text {SENSE }}$ | Current sense amplifier input. |
| 3 | SYNC (CS51021A/3A) | Bi-directional synchronization. Locks to the highest frequency. |
| 3 | SLEEP (CS51022A/4A) | Active high chip disable. In sleep mode, $\mathrm{V}_{\text {REF }}$ and GATE are turned off. |
| 4 | SLOPE | Additional slope to the current sense signal. Internal current source charges the external capacitor. |
| 5 | UV | Undervoltage protection monitor. |
| 6 | OV | Overvoltage protection monitor. |
| 7 | $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ | Timing resistor $\mathrm{R}_{\mathrm{T}}$ and capacitor $\mathrm{C}_{\mathrm{T}}$ determine oscillator frequency and maximum duty cycle, $\mathrm{D}_{\text {MAX }}$. |
| 8 | $I_{\text {SET }}$ | Voltage at this pin sets pulse-by-pulse overcurrent threshold, and second threshold ( 1.33 times higher) with Soft Start retrigger (hiccup mode). |
| 9 | $\mathrm{V}_{\mathrm{FB}}$ | Feedback voltage input. Connected to the error amplifier inverting input. |
| 10 | COMP | Error amplifier output. Frequency compensation network is usually connected between COMP and $\mathrm{V}_{\mathrm{FB}}$ pins. |
| 11 | SS | Charging external capacitor restricts error amplifier output voltage during the start or fault conditions (hiccup). |
| 12 | LGND | Logic ground. |

PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :--- |
| 16 Lead SO Narrow | V $_{\text {REF }}$ | 5.0 V reference voltage output. |
| 13 | $V_{C C}$ | Logic supply voltage. |
| 14 | PGND | Output power stage ground connection. |
| 15 | $V_{C}$ | Output power stage supply voltage. |
| 16 |  |  |



Figure 2. Block Diagram

## CIRCUIT DESCRIPTION



Figure 3. Typical Waveforms

## THEORY OF OPERATION

## Powering the IC

The IC has two supply and two ground pins. $\mathrm{V}_{\mathrm{C}}$ and PGND pins provide high speed power drive for the external power switch. $\mathrm{V}_{\mathrm{CC}}$ and LGND pins power the control portion of the IC. The internal logic monitors the supply voltage, $\mathrm{V}_{\mathrm{CC}}$. During abnormal operating conditions, the output is held low. The CS51021A/2A/3A/4A requires only $75 \mu \mathrm{~A}$ of startup current.

## Voltage Feedback

The output voltage is monitored via the $\mathrm{V}_{\mathrm{FB}}$ pin and is compared with the internal 2.5 V reference. The error amplifier output minus one diode drop is divided by 3 and connected to the negative input of the PWM comparator. The positive input of the PWM comparator is connected to the modified current sense signal. The oscillator turns the external power switch on at the beginning of each cycle. When current sense ramp voltage exceeds the reference side of PWM comparator, the output stage latches off. It is turned on again at the beginning of the next oscillator cycle.

## Current Sense and Protection

The current is monitored at the ISENSE pin. The CS51021A/2A/3A/4A has leading edge blanking circuitry that ignores the first 55 ns of each switching period. Blanking is disabled when $\mathrm{V}_{\mathrm{FB}}$ is less than 2.0 V so that the minimum on-time of the controller does not have an additional 55 ns of delay time during fault conditions. For the remaining portion of the switching period, the current sense signal, combined with a fraction of the slope compensation voltage, is applied to the positive input of the PWM comparator where it is compared with the divided by three error amplifier output voltage. The pulse-by-pulse overcurrent protection threshold is set by the voltage at the $\mathrm{I}_{\text {SET }}$ pin. This voltage is passed through the $\mathrm{I}_{\text {SET }}$ Clamp and appears at the non-inverting input of the PWM comparator, limiting its dynamic range according to the following formula:

$$
\begin{aligned}
\text { Overcurrent Threshold }= & 0.8 \times \mathrm{V}_{\mathrm{I}}(\text { SENSE }) \\
& +0.1 \mathrm{~V}+0.1 \mathrm{~V} \text { SLOPE }
\end{aligned}
$$

where
$\mathrm{V}_{\mathrm{I}}($ SENSE $)$ is voltage at the ISENSE pin.
and
VSLOPE is voltage at the SLOPE pin.
During extreme overcurrent or short circuit conditions, the slope of the current sense signal will become much steeper than during normal operation. Due to loop propagation delay, the sensed signal will overshoot the pulse-by-pulse threshold eventually reaching the second overcurrent protection threshold which is 1.33 times higher than the first threshold and is described by the following equation:

$$
\text { 2nd Threshold }=1.33 \times \mathrm{V}_{\mathrm{I}}(\mathrm{SET})
$$

Exceeding the second threshold will reset the Soft Start capacitor $\mathrm{C}_{\mathrm{SS}}$ and reinitiate the Soft Start sequence, repeating for as long as the fault condition persists.

## Soft Start

During power up, when the output filter capacitor is discharged and the output voltage is low, the voltage across the Soft Start capacitor $\left(\mathrm{V}_{\mathrm{SS}}\right)$ controls the duty cycle. An internal current source of $55 \mu \mathrm{~A}$ charges $\mathrm{C}_{\text {SS }}$. The maximum error amplifier output voltage is clamped by the SS Clamp. When the Soft Start capacitor voltage exceeds the error amplifier output voltage, the feedback loop takes over the duty cycle control. The Soft Start time can be estimated with the following formula:

$$
\mathrm{tSS}=9 \times 10^{4} \times \mathrm{CSS}
$$

The Soft Start voltage, $\mathrm{V}_{\mathrm{SS}}$, charges and discharges between 0.25 V and 4.7 V .

## Slope Compensation

DC-DC converters with current mode control require a current sense signal with slope compensation to avoid instability at duty cycles greater than $50 \%$. Slope capacitor $\mathrm{C}_{\mathrm{S}}$ is charged by an internal $53 \mu \mathrm{~A}$ current source and is discharged during the oscillator discharge time. The slope compensation voltage is divided by 10 and is added to the current sense voltage, $\mathrm{V}_{\mathrm{I} \text { (SENSE). }}$. The signal applied to the input of the PWM comparator is a combination of these two voltages. The slope compensation, $\mathrm{dV}_{\text {SLOPE }} / \mathrm{dt}$, is calculated using the following formula:

$$
\frac{\mathrm{dV} \mathrm{~V}_{\mathrm{SLOPE}}}{\mathrm{dt}}=0.1 \times \frac{53 \mu \mathrm{~A}}{\mathrm{CS}}
$$

It should be noted that internal capacitance of the IC will cause an error when determining slope compensation capacitance $\mathrm{C}_{\mathrm{S}}$. This error is typically small for large values of $C_{S}$, but increases as $C_{S}$ becomes small and comparable to the internal capacitance. The effect is apparent as a reduction in charging current due to the need to charge the internal capacitance in parallel with $\mathrm{C}_{S}$.Figure 4 shows a typical curve indicating this decrease in available charging current.


Figure 4. The Slope Compensation Pin Charge Current Reduces When a Small Capacitor Is Used.

## Undervoltage (UV) and Overvoltage (OV) Monitor

Two independent comparators monitor OV and UV conditions. A string of three resistors is connected in series between the monitored voltage (usually the input voltage) and ground (see Figure 5). When voltage at the OV pin exceeds 2.5 V , an overvoltage condition is detected and GATE shuts down. An internal $12.5 \mu \mathrm{~A}$ current source turns on and feeds current into the external resistor, $\mathrm{R}_{3}$, creating a hysteresis determined by the value of this resistor (the higher the value, the greater the hysteresis). The hysteresis voltage of the OV monitor is determined by the following formula:

$$
\mathrm{V}_{\mathrm{OV}(\mathrm{HYST})}=12.5 \mu \mathrm{~A} \times \mathrm{R}_{3}
$$

where $R_{3}$ is a resistor connected from the OV pin to ground.
When the monitored voltage is low and the UV pin is less than 1.45 V , GATE shuts down. The UV pin has fixed 75 mV hysteresis.
Both OV and UV conditions are latched until the Soft Start capacitor is discharged. This way, every time a fault condition is detected the controller goes through the power up sequence.


Figure 5. UV/OV Monitor Divider

To calculate the OV?UV resistor divider :

1. Solve for $\mathrm{R}_{3}$, based on OV hysteresis requirements.

$$
\mathrm{R}_{3}=\frac{\mathrm{V}_{\mathrm{OV}(\mathrm{HYST})} \times 2.5 \mathrm{~V}}{\mathrm{~V}_{\mathrm{MAX}} \times 12.5 \mu \mathrm{~A}}
$$

where $\mathrm{V}_{\mathrm{OV} \text { (HYST) }}$ is the desired amount of overvoltage hysteresis, and $\mathrm{V}_{\text {MAX }}$ is the input voltage at which the supply will shut down.
2. Find the total impedance of the divider.

$$
\mathrm{RTOT}_{\mathrm{TO}}=\mathrm{R}_{1}+\mathrm{R}_{2}+\mathrm{R}_{3}=\frac{\mathrm{V}_{\mathrm{MAX}} \times \mathrm{R}_{3}}{2.5}
$$

3. Determine the value of $\mathrm{R}_{2}$ from the UV threshold conditions.

$$
\mathrm{R}_{2}=\frac{1.45 \times \mathrm{RTOT}}{\mathrm{~V}_{\mathrm{MIN}}}-\mathrm{R}_{3}
$$

where $\mathrm{V}_{\mathrm{MIN}}$ is the UV voltage at which the supply will shut down.
4. Calculate $\mathrm{R}_{1}$.

$$
\mathrm{R}_{1}=\mathrm{R}_{\mathrm{TOT}}-\mathrm{R}_{2}-\mathrm{R}_{3}
$$

5. The undervoltage hysteresis is given by :

$$
\mathrm{VUV}(\mathrm{HYST})=\frac{\mathrm{V}_{\mathrm{MIN}} \times 0.075}{1.45}
$$

## $\mathbf{V}_{\text {REF }}$ Monitor

The 5.0 V reference voltage is internally monitored to ensure that it remains within specifications. The monitor, which outputs a fault, can be tripped by two methods:

- If the reference voltage drops below 4.75 V
- If $\mathrm{V}_{\mathrm{CC}}$ falls below the STOP threshold

As indicated in the block diagram, any fault causes the output to stop switching and begins the discharge of the Soft Start capacitor $\mathrm{C}_{\text {SS }}$.

## CS51021A, CS51022A, CS51023A, CS51024A

## Synchronization

A bi-directional synchronization is provided to synchronize several controllers. When SYNC pins are connected together, the converters will lock to the highest switching frequency. The fastest controller becomes the master, producing a $4.3 \mathrm{~V}, 200 \mathrm{~ns}$ pulse train. Only one, the highest frequency SYNC signal, will appear on the SYNC line.

## Sleep

The sleep input is an active high input. The CS51022A/4A is placed in sleep mode when SLEEP is driven high. In sleep mode, the controller and MOSFET are turned off. Connect to GND for normal operation. The sleep mode operates at VCC $\leq 15 \mathrm{~V}$.

## Oscillator and Duty Cycle Limit

The switching frequency is set by $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$ connected to the $\mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}$ pin. $\mathrm{C}_{\mathrm{T}}$ charges and discharges between 3.0 V and 1.5 V .

The maximum duty cycle is set by the ratio of the on time, $\mathrm{t}_{\mathrm{ON}}$, and the whole period, $\mathbf{T}=\mathbf{t}_{\mathbf{O N}}+\mathbf{t}_{\mathbf{O F F}}$. Because the timing capacitor's discharge current is trimmed, the maximum duty cycle is well defined. It is determined by the ratio between the timing resistor $\mathrm{R}_{\mathrm{T}}$ and the timing capacitor $\mathrm{C}_{\mathrm{T}}$. Refer to figures 6 and 7 to select appropriate values for $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$.

$$
\mathrm{fSW}=\frac{1}{\mathrm{TSW}} ; \mathrm{TSW}=\mathrm{t} \mathrm{CH}+\mathrm{tDIS}
$$



Figure 7. Duty Cycle vs. $\mathbf{R}_{\boldsymbol{T}}$ for Discrete Capacitor Values

PACKAGE THERMAL DATA

| Parameter |  | SO-16 | Unit |
| :--- | ---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5106

## Multi-Feature, Synchronous plus Auxiliary PWM Controller

The CS5106 is a fixed frequency, current mode controller with one single NFET driver and one dual FET, synchronous driver. The synchronous driver allows for increased efficiency of the main isolated power stage and the single driver allows the designer to develop auxiliary supplies for controller power as well as secondary side house keeping. In addition, because the synchronous drivers have programmable FET non-overlap, the CS5106 is an ideal controller for soft-switched converter topologies.

The CS5106 is specifically designed for isolated topologies where speed, flexibility, reduced size and reduced component count are requirements. The controller contains the following features: Undervoltage Shutdown, Overvoltage Shutdown, Programmable Frequency, Programmable Synchronous Non-Overlap Time, Master/Slave Clocking with Frequency Range Detection, Enable, Output Undervoltage Protection with Timer, 20 mA 5.0 V Output, 80 ns PWM propagation delay, and Controlled Hiccup Mode.

The CS5106 has junction temperature and supply ranges of $-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$ and 9.0 V to 16 V respectively and is available in the 24 lead SSOP package.

## Features

- Programmable Fixed Frequency
- Programmable FET Non-Overlap
- Enable Lead
- 12 V Fixed Auxiliary Supply Control
- Under and Overvoltage Shutdown
- Output Undervoltage Protection with Timer
- Master/Slave Clock Sync Capability
- Sync Frequency Range Detection
- 80 ns PWM Propagation Delay
- 20 mA 5.0 V Reference Output
- Small 24 Lead SSOP Package
- Controlled Hiccup Mode

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SSOP-24
SW SUFFIX
CASE 940D

PIN CONNECTIONS AND MARKING DIAGRAM


| A | $=$ Assembly Location |
| :--- | :--- |
| WL, L | $=$ Wafer Lot |
| YY, Y | $=$ Year |
| WW, W | $=$ Work Week |

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5106LSW24 | SSOP-24 | 59 Units/Rail |
| CS5106LSWR24 | SSOP-24 | 2000 Tape \& Reel |



## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Operating Junction Temperature, $T_{J}$ |  | 150 |
| Operating Temperature Range, $T_{A}$ | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature Range, $\mathrm{T}_{S}$ | Reflow: (SMD styles only) (Note 1$)$ | -40 to 85 |
| ESD Susceptibility (Human Body Model) | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering: | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Undervoltage Shutdown Input | UVSD | 6.0 V | -0.3 V | 1.0 mA | N/A |
| Overvoltage Shutdown Input | OVSD | 6.0 V | -0.3 V | 1.0 mA | N/A |
| 5.0 V Reference Output | $V_{5 R E F}$ | 6.0 V | -0.3 V | 150 mA | 25 mA |
| Error Amp Minus Input | OAM | 6.0 V | -0.3 V | $250 \mu \mathrm{~A}$ | 1.2 mA |
| Error Amp Output | OAOUT | 6.0 V | -0.3 V | $300 \mu \mathrm{~A}$ | 100 mA |
| Output Overcurrent Timer Capacitor | OUVDELAY | 6.0 V | -0.3 V | $15 \mu \mathrm{~A}$ | N/A |
| Auxiliary Primary Side Current Limit Input | ILIM1 | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | N/A |
| Auxiliary Primary Side Current Ramp Input | RAMP1 | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | N/A |
| Auxiliary Voltage Feedback Input | $\mathrm{V}_{\text {FB1 }}$ | 6.0 V | -0.3 V | $5.0 \mu \mathrm{~A}$ | $100 \mu \mathrm{~A}$ |
| Bootstrapped Power Input | $\mathrm{V}_{S S}$ | 20 V | -0.3 V | $2.0 \mu \mathrm{~A}$ | 0.5 A Peak, 300 mA DC |
| Main Power Input | $\mathrm{V}_{\mathrm{CC}}$ | 20 V | -0.3 V | See Note 2 | 0.5 A Peak, 300 mA DC |
| Auxiliary FET Driver Output | GATE1 | 20 V | -0.3 V | 0.5 A Peak, 100 mA DC | 0.5 A Peak, 100 mA DC |
| Ground | GND | 0 V | 0 V | 0.5 A Peak | N/A, 300 mA DC |
| Synchronous FET Driver Output | GATE2 | 20 V | -0.3 V | 0.5 A Peak, 100 mA DC | 0.5 A Peak, 100 mA DC |
| Synchronous FET Driver Output B | GATE2B | 20 V | -0.3 V | 0.5 A Peak, 100 mA DC | 0.5 A Peak, 100 mA DC |
| Synchronous Voltage Feedback Input | $\mathrm{V}_{\mathrm{FB} 2}$ | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | $100 \mu \mathrm{~A}$ |
| Synchronous Primary Side Current Ramp Input | RAMP2 | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | N/A |
| Synchronous Primary Side Current Limit Input | ILIM2 | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | N/A |
| Gate Non-Overlap Programming Input | DLYSET | 2.5 V | -0.3 V | $125 \mu \mathrm{~A}$ | N/A |
| Frequency Programming Input | FADJ | 2.5 V | -0.3 V | $125 \mu \mathrm{~A}$ | N/A |
| Clock Master Output | SYNCOUT | 6.0 V | -0.3 V | 50 mA | 100 mA |
| Clock Slave Input | SYNC ${ }_{\text {IN }}$ | 6.0 V | -0.3 V | N/A | 1.0 mA |
| Enable Programming Input | PROGRAM | 16 V | -0.3 V | $30 \mu \mathrm{~A}$ | N/A |
| Enable Input | ENABLE | 16 V | -0.3 V | $300 \mu \mathrm{~A}$ | N/A |

2. Current out of $\mathrm{V}_{\mathrm{CC}}$ is not limited. Care should be taken to prevent shorting $\mathrm{V}_{\mathrm{CC}}$ to Ground.

## CS5106

ELECTRICAL CHARACTERISTICS $\left(T_{J}=-40^{\circ} \mathrm{C}\right.$ to $125^{\circ} \mathrm{C}, \mathrm{V}_{S S}=9.0$ to $16 \mathrm{~V}, \mathrm{~V}_{\text {5REF }} \mathrm{I}_{\text {LOAD }}=2.0 \mathrm{~mA}$, SYNC $_{\text {OUT }}$ Free Running, unless otherwise specified. For All Specs: UVSD $=6.0 \mathrm{~V}, \mathrm{OVSD}=0 \mathrm{~V}, \mathrm{ENABLE}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{LIM}(1,2)}=0, \mathrm{~V}_{\mathrm{FB}(1,2)}=3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{FADJ}}=$ $R_{\text {DLYSET }}=27.4 \mathrm{k} \Omega$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {SS }}$ Supply Current |  |  |  |  |  |
| $\mathrm{V}_{\text {SS }}$ Supply Current | Measure current into $\mathrm{V}_{\mathrm{SS}}$ when <br> $\mathrm{V}_{5 \text { REF }} \mathrm{I}_{\text {LOAD }}=0 \mathrm{~mA} .9 .0 \mathrm{~V} \leq \mathrm{V}_{\text {SS }} \leq 13 \mathrm{~V}$. <br> Measure current into $\mathrm{V}_{S S}$ when <br> $\mathrm{V}_{\text {5REF }} \mathrm{I}_{\text {LOAD }}=0 \mathrm{~mA} .13 \mathrm{~V}<\mathrm{V}_{\text {SS }} \leq 16 \mathrm{~V}$. <br> Measure current into $\mathrm{V}_{\mathrm{SS}}$ when <br> $\mathrm{V}_{5 \text { REF }} \mathrm{I}_{\text {LOAD }}=0 \mathrm{~mA} .16 \mathrm{~V}<\mathrm{V}_{\text {SS }} \leq 20 \mathrm{~V}$. |  | 16 <br> 16 <br> 16 | $23$ <br> 25 $30$ | mA <br> mA <br> mA |

## Low $\mathrm{V}_{\mathrm{cc}}$ Supply Current

| Low $\mathrm{V}_{\text {CC }}$ Supply Current | Float $\mathrm{V}_{\mathrm{SS}}$. Set $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ \& measure $\mathrm{V}_{\mathrm{CC}}$ current while $\mathrm{V}_{5 \text { REF }}$ LIOAD $=0 \mathrm{~mA}$. | - | 1.5 | 3.5 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {SS }}$ to $\mathrm{V}_{\text {cc }}$ Diode |  |  |  |  |  |
| Diode ON Voltage | Measure $\mathrm{V}_{S S}-\mathrm{V}_{\mathrm{CC}}$ | 0.2 | 0.75 | 1.0 | V |
| Reference |  |  |  |  |  |
| 5.0 V Internal Voltage Reference | Measure $\mathrm{V}_{\text {REF }}$ voltage when $I_{\text {REF }}=0$ and $I_{\text {REF }}=20 \mathrm{~mA}$ | 4.85 | 5.0 | 5.15 | V |
| $\mathrm{V}_{\text {REF }}$ OK Threshold | Adjust $\mathrm{V}_{\text {REF }}$ from $4.8 \mathrm{~V}-4.0 \mathrm{~V}$ until PWM1,2 goes low. | 4.3 | 4.55 | 4.7 | V |

## Low $\mathrm{V}_{\mathrm{CC}}$ Lockout

| $\mathrm{V}_{\text {CC }}$ Turn-on Threshold Voltage | $\mathrm{V}_{\mathrm{CC}}$ increasing until $\mathrm{I}_{\mathrm{CC}}>3.5 \mathrm{~mA}$ <br> $V_{\text {5REF }}$ load $=0 \mathrm{~mA}$ | 7.0 | 7.25 | 7.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ Turn-off Threshold Voltage | $\mathrm{V}_{\mathrm{CC}}$ decreasing until $\mathrm{I}_{\mathrm{CC}}<3.5 \mathrm{~mA}$ $V_{5 \text { REF }} I_{\text {LOAD }}=0 \mathrm{~mA}$ | 6.3 | 6.7 | 7.1 | V |
| Hysteresis | Turn-on - Turn-off | 0.40 | 0.55 | 0.70 | V |

Clock

| Operating Frequency1 | Measure frequency from SYNCout. | 485 | 512 | 540 | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SYNC ${ }_{\text {IN }}$ Input Impedance | Measure input impedance. | 7.0 | 15 | - | k $\Omega$ |
| SYNC Out $^{\text {Output Low Voltage }}$ | $\mathrm{R}_{\text {LOAD }}=2.0 \mathrm{k} \Omega$ to $\mathrm{V}_{5 \text { REF }}$ | - | 1.0 | 1.5 | V |
| SYNC ${ }_{\text {OUT }}$ Output High Voltage | $\mathrm{R}_{\text {LOAD }}=2.0 \mathrm{k} \Omega$ to GND | 3.5 | 4.2 | - | V |
| $\mathrm{SYNC}_{\mathbb{I N}}$ Detect Frequency | Verify SYNC $_{\text {OUT }}=S Y N C_{I N}$, $R_{\text {LOAD }}=2.0 \mathrm{k} \Omega$ to GND | 425 | - | 555 | kHz |
| Max. Low SYNC Rej. Frequency | Verify SYNC $_{\text {OUT }}=$ FCLK when $R_{\text {LOAD }}=2.0 \mathrm{k} \Omega$ to GND | - | - | 340 | kHz |
| Min. High SYNC Rej. Frequency | Verify SYNC $_{\text {OUT }}=$ FCLK when $R_{\text {LOAD }}=2.0 \mathrm{k} \Omega$ to GND | 690 | - | - | kHz |
| SYNC ${ }_{\text {IN }}$ Input Threshold Voltage | Functional Testing Verify FCLK from 1.0 V to 2.8 V | 0.9 | 1.85 | 2.9 | V |
| Main PWM Clock Pulse Width | (GBD) - CLPH1 One Shot Pulse Width | 80 | 100 | 120 | ns |
| Aux PWM Clock Pulse Width | (GBD) - CLPH2 One Shot Pulse Width | 80 | 100 | 120 | ns |

ELECTRICAL CHARACTERISTICS (continued) $\left(T_{J}=-40^{\circ} \mathrm{C}\right.$ to $125^{\circ} \mathrm{C}, \mathrm{V}_{\text {SS }}=9.0$ to $16 \mathrm{~V}, \mathrm{~V}_{5 \text { REF }} \mathrm{I}_{\text {LOAD }}=2.0 \mathrm{~mA}$, SYNC $_{\text {OUT }}$ Free Running, unless otherwise specified. For All Specs: $\mathrm{UVSD}=6.0 \mathrm{~V}, \mathrm{OVSD}=0 \mathrm{~V}, \mathrm{ENABLE}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{LIM}(1,2)}=0, \mathrm{~V}_{\mathrm{FB}(1,2)}=3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{FADJ}}=$ $R_{\text {DLYSET }}=27.4 \mathrm{k} \Omega$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Bias Supply Error Amplifier

| Output Low Voltage | $\mathrm{V}_{\mathrm{SS}}>12.6 \mathrm{~V}$. Measure OAOUT voltage when sinking 1.0 mA . | - | 43 | 85 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output High Voltage | $\mathrm{V}_{\mathrm{SS}}<11.4 \mathrm{~V}$. Measure OAOUT voltage when sourcing $150 \mu \mathrm{~A}$. | 4.55 | 4.75 | - | V |
| Output High Source Current | $\mathrm{V}_{\mathrm{SS}}<11.4 \mathrm{~V}$. Measure OAOUT source current when OAOUT $=0.5 \mathrm{~V}$ | 150 | 225 | 300 | $\mu \mathrm{A}$ |
| Output Low Sink Current | $\mathrm{V}_{\mathrm{SS}}>12.6 \mathrm{~V}$. Measure OAOUT sink current when OAOUT $=2.5 \mathrm{~V}$. | 3.0 | 20 | 50 | mA |
| $\mathrm{V}_{\text {SS }}$ Set Point | Adjust $\mathrm{V}_{\text {SS }}$ until OAOUT goes low. | 11.6 | 12.25 | 12.8 | V |
| Large Signal Gain | (GBD) | 15 | - | - | V/mV |
| Unity Gain Bandwidth | (GBD) | - | 1.0 | - | MHz |
| Common Mode Input Range | (GBD) | 1.0 | - | 2.0 | V |
| $\mathrm{V}_{\text {SS }}$ Voltage |  |  |  |  |  |
| $\mathrm{V}_{\text {SS }}$ Reset Voltage | Toggle ENABLE between $G N D$ \& $\mathrm{V}_{\mathrm{CC}}$, then adjust $\mathrm{V}_{\mathrm{SS}}$ from 2.0 $\mathrm{V}-0.8 \mathrm{~V}$ until OAOUT goes high. | 1.0 | 1.4 | 1.8 | V |
| Undervoltage Lockout |  |  |  |  |  |
| UVSD Turn-On Threshold Voltage | Adjust UVSD from 4.7 V-5.3 V until GATE1,2 goes high. | 4.8 | 5.0 | 5.1 | V |
| UVSD Turn-Off Threshold Voltage | Adjust UVSD from 5.1 V-4.3 V until GATE1,2 goes low. | 4.45 | 4.7 | 4.95 | V |
| Hysteresis | Turn-on - Turn-off | 0.2 | 0.27 | 0.4 | V |
| UVSD Input Bias Current | Set UVSD $=0$ V. Measure Current out of UVSD lead. | - | 0.2 | 0.5 | $\mu \mathrm{A}$ |
| Overvoltage Lockout |  |  |  |  |  |
| OVSD Threshold Voltage | Adjust OVSD from 4.7 V-5.3 V until GATE1,2 goes low. | 4.85 | 5.0 | 5.15 | V |
| OVSD Input Bias Current | Set OVSD $=0 \mathrm{~V}$. Measure Current out of OVSD lead. | - | 0.2 | 0.5 | $\mu \mathrm{A}$ |

ENABLE \& PROGRAM

| ENABLE Lead Output Current | Measure current out of ENABLE <br> when ENABLE $=0 \mathrm{~V}$ | 100 | 266 | 500 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| PROGRAM Lead Output Current | Measure current out of PROGRAM <br> when PROGRAM $=0 \mathrm{~V}$ | 20 | 60 | 100 | $\mu \mathrm{~A}$ |
| PROGRAM Threshold Voltage | ENABLE $=$ GND. Adjust PROGRAM from <br> $1.0 ~ V-1.8 ~ V ~ u n t i l ~ G A T E 1,2 ~ g o e s ~ h i g h . ~$ | 1.2 | 1.4 | 1.6 | V |
| ENABLE Threshold Voltage | PROGRAM = GND. Adjust ENABLE from <br> $1.0 ~ V-1.8 ~ V ~ u n t i l ~ G A T E 1,2 ~ g o e s ~ h i g h . ~$ | 1.2 | 1.4 | 1.6 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(T_{J}=-40^{\circ} \mathrm{C}\right.$ to $125^{\circ} \mathrm{C}, \mathrm{V}_{\text {SS }}=9.0$ to $16 \mathrm{~V}, \mathrm{~V}_{5 \text { REF }} \mathrm{I}_{\text {LOAD }}=2.0 \mathrm{~mA}$, SYNC $_{\text {OUT }}$ Free Running, unless otherwise specified. For All Specs: UVSD $=6.0 \mathrm{~V}$, $\mathrm{OVSD}=0 \mathrm{~V}$, ENABLE $=0 \mathrm{~V}, \mathrm{I}_{\mathrm{LIM}(1,2)}=0, \mathrm{~V}_{\mathrm{FB}(1,2)}=3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{FADJ}}=$ $R_{\text {DLYSET }}=27.4 \mathrm{k} \Omega$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Undervoltage Delay |  |  |  |  |  |
| OUVDELAY Charging Current | Set OUVDELAY $=1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB} 1}=4.4 \mathrm{~V}$ Measure OUVDELAY I Charge. | 7.5 | 10 | 12.5 | $\mu \mathrm{A}$ |
| OUVDELAY Latch-off Voltage | Toggle ENABLE between $G N D \& \mathrm{~V}_{\mathrm{CC}}$, then adjust OUVDELAY from 4.7 V-5.3 V until GATE1,2, goes low. | 4.8 | 5.0 | 5.2 | V |
| OUVDELAY Set Current | OUVDELAY = VOCLO +50 mV . Measure current into OUVDELAY. | - | 0.5 | 1.0 | mA |
| $\mathrm{V}_{\mathrm{FB} 1}$ Charge Threshold | $\mathrm{V}_{\mathrm{SS}}=1.0 \mathrm{~V}$. Toggle ENABLE between GND \& $\mathrm{V}_{\mathrm{CC}}$, adjust $\mathrm{V}_{\mathrm{FB} 1}$ from $3.8 \mathrm{~V}-4.6 \mathrm{~V}$ until GATE1,2 goes low. | 4.05 | 4.22 | 4.4 | V |
| $\mathrm{V}_{\text {FB2 }}$ Charge Threshold | $\mathrm{V}_{\mathrm{SS}}=1.0 \mathrm{~V}$. Toggle ENABLE between GND \& $\mathrm{V}_{\mathrm{CC}}$, adjust $\mathrm{V}_{\mathrm{FB} 2}$ from 3.8 $\mathrm{V}-4.6 \mathrm{~V}$ until GATE1,2 goes low. | 3.9 | 4.15 | 4.35 | V |

## Current Limit Circuits

| ILIM1 Current Limit Threshold Voltage | Adjust lim 1 from $1.0 \mathrm{~V}-1.3 \mathrm{~V}$ until GATE1 goes low. | 1.16 | 1.24 | 1.3 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ILIM1 Short Circuit Threshold Voltage | Adjust ILIM1 from $1.30 \mathrm{~V}-1.50 \mathrm{~V}$ until GATE1 skips 2-cycles with reference to SYNC OUT. | 1.35 | 1.44 | 1.51 | v |
| LIIM1 Input Bias Current | Set $\mathrm{ILIM1}^{\text {a }}=0 \mathrm{~V}$. Measure current out of $\mathrm{ILIM1}$ lead. | - | 0.5 | 5.0 | $\mu \mathrm{A}$ |
| ILIm2 Current Limit Threshold Voltage | Adjust lıım2 from $1.0 \mathrm{~V}-1.3 \mathrm{~V}$ until GATE2 goes low. | 1.16 | 1.24 | 1.3 | V |
| ILIM2 Short Circuit Threshold Voltage | Adjust llim2 from $1.30 \mathrm{~V}-1.50 \mathrm{~V}$ until GATE2 skips 2-cycles with reference to SYNCout. | 1.35 | 1.44 | 1.51 | V |
| LIIM2 Input Bias Current | Set $\mathrm{I}_{\text {LIM2 }}=0 \mathrm{~V}$. Measure current out of $\mathrm{ILIM2}^{\text {l }}$ lead. | - | 0.5 | 5.0 | $\mu \mathrm{A}$ |

Voltage Feedback Control

| RAMP1 Offset Voltage | $\mathrm{V}_{\mathrm{FB} 1}=0 \mathrm{~V}$. Adjust RAMP1 from $0 \mathrm{~V}-0.3 \mathrm{~V}$ until GATE1 goes low. Measure $\mathrm{V}_{\text {RAMP1. }}$. | 0.08 | 0.13 | 0.2 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RAMP1 Input Bias Current | Set RAMP1 $=0 \mathrm{~V}$. Measure Current out of RAMP1 lead. | - | 0.5 | 5.0 | $\mu \mathrm{A}$ |
| RAMP2 Offset Voltage | $\mathrm{V}_{\mathrm{FB} 2}=0 \mathrm{~V}$. Adjust RAMP2 from $0 \mathrm{~V}-3.0 \mathrm{~V}$ until GATE2 goes low. Measure $\mathrm{V}_{\text {RAMP2 }}$. | 0.08 | 0.13 | 0.2 | V |
| RAMP2 Input Bias Current | Set RAMP2 $=0 \mathrm{~V}$. Measure Current out of RAMP2 lead. | - | 0.5 | 5.0 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {FB1 }}$ Input Impedance | Measure input impedance. | 60 | 120 | 220 | k $\Omega$ |
| $\mathrm{V}_{\text {FB2 }}$ Input Impedance | Measure input impedance. | 60 | 120 | 220 | k $\Omega$ |

ELECTRICAL CHARACTERISTICS (continued) $\left(T_{J}=-40^{\circ} \mathrm{C}\right.$ to $125^{\circ} \mathrm{C}, \mathrm{V}_{\text {SS }}=9.0$ to $16 \mathrm{~V}, \mathrm{~V}_{5 \text { REF }} \mathrm{I}_{\text {LOAD }}=2.0 \mathrm{~mA}$, SYNC $_{\text {OUT }}$ Free Running, unless otherwise specified. For All Specs: UVSD $=6.0 \mathrm{~V}, \mathrm{OVSD}=0 \mathrm{~V}, \mathrm{ENABLE}=0 \mathrm{~V}, \mathrm{I}_{\mathrm{LIM}(1,2)}=0, \mathrm{~V}_{\mathrm{FB}(1,2)}=3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{FADJ}}=$ $R_{\text {DLYSET }}=27.4 \mathrm{k} \Omega$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gate1, 2, 2B, Output Voltages | $\mathrm{V}_{\mathrm{SS}}=12 \mathrm{~V} . \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{SS}}-\mathrm{V}_{\text {DON }}$ |  |  |  |  |
| GATE1 Low State | PROGRAM = 0 V. Measure GATE1 voltage when sinking 1.0 mA . | - | 0.15 | 0.8 | V |
| GATE2 Low State | PROGRAM = 0 V. Measure GATE2 voltage when sinking 1.0 mA . | - | 0.18 | 0.8 | V |
| GATE2B Low State | PROGRAM = 0 V. Measure GATE2B voltage when sinking 1.0 mA . | - | 0.18 | 0.8 | V |
| GATE2B High State | Measure $\mathrm{V}_{\mathrm{CC}}-\mathrm{GATE} 2 \mathrm{~B}$ voltage when sourcing 1.0 mA . | - | 1.65 | 2.0 | V |
| GATE2 High State | Measure $\mathrm{V}_{\mathrm{CC}}$ - GATE2 voltage when sourcing 1.0 mA . | - | 1.65 | 2.0 | V |
| GATE1 High State | Measure $\mathrm{V}_{\mathrm{CC}}$ - GATE1 voltage when sourcing 1.0 mA . | - | 1.65 | 2.0 | V |

## Propagation Delays

| LIM1 Delay to Output GATE1 | Measure delay from ILIM1 going high to GATE1 <br> going low. | - | 80 | 120 | ns |
| :--- | :--- | :--- | :--- | :---: | :---: |
| LIM2 Delay to Output GATE2 | Measure delay from ILIM2 going high to GATE2 <br> going low. | - | 80 | 100 | ns |
| RAMP1 Delay to Output GATE1 | Measure delay from RAMP1 going high to <br> GATE1 going low. | - | 80 | 115 | ns |
| RAMP2 Delay to Output GATE2 | Measure delay from RAMP2 going high to <br> GATE2 going low. | - | 80 | 100 | ns |

GATE2, 2B Non-Overlap Delay

| GATE2 Turn-on Delay from <br> GATE2B | Measure delay from GATE2B going low @ 1.7 V <br> to GATE2 going high @ 1.7 V. | 20 | 45 | 70 | ns |
| :--- | :---: | :---: | :---: | :---: | :---: |
| GATE2B Turn-on Delay from <br> GATE2 | Measure delay from GATE2 going low @ 1.7 V to <br> GATE2B going high @ 1.7 V. | 20 | 45 | 70 | ns |

GATE1, 2, 2B Rise \& Fall Times $\quad \mathrm{V}_{\mathrm{SS}}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{SS}}-\mathrm{V}_{\mathrm{DON}}$

| GATE1 Rise Time | Measure GATE1 Rise Time from $90 \%$ to $10 \%$. <br> CLOAD $=150 \mathrm{pF}$. | - | 50 | 80 | ns |
| :--- | :--- | :--- | :--- | :---: | :---: |
| GATE1 Fall Time | Measure GATE1 Fall Time from $10 \%$ to $90 \%$. <br> CLOAD $=150 \mathrm{pF}$. | - | 30 | 60 | ns |
| GATE2 Rise Time | Measure GATE2 Rise Time from $90 \%$ to $10 \%$. <br> CLOAD $=50 \mathrm{pF}$. | - | 50 | 80 | ns |
| GATE2 Fall Time | Measure GATE2 Fall Time from $10 \%$ to $90 \%$. <br> CLOAD $=50 \mathrm{pF}$. | - | 15 | 30 | ns |
| GATE2B Rise Time | Measure GATE2B Rise Time from $90 \%$ to $10 \%$. <br> CLOAD $=50 \mathrm{pF}$. | - | 50 | 80 | ns |
| GATE2B Fall Time | Measure GATE2B Rise Time from $10 \%$ to $90 \%$. <br> CLOAD $=50 \mathrm{pF}$. | - | 15 | 30 | ns |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SSOP-24 | PIN SYMBOL | FUNCTION |
| 1 | UVSD | Undervoltage shutdown lead. Typically this lead is connected through a resistor divider to the main high voltage $\left(\mathrm{V}_{\mathbb{N}}\right)$ line. If the voltage on this lead is less than 5.0 V then a fault is initiated such that GATE1, GATE2 and GATE2B go low. |
| 2 | OVSD | Overvoltage shutdown lead. Typically this lead is connected through a resistor divider to the main high voltage $\left(\mathrm{V}_{\text {IN }}\right)$ line. If the voltage on this lead exceeds 5.0 V then a fault is initiated such that GATE1, GATE2 and GATE2B go low. |
| 3 | $\mathrm{V}_{\text {SREF }}$ | 5.0 V reference output lead. Capable of 20 mA nominal output. If this lead falls to 4.5 V , a fault is initiated such that GATE1, GATE2 and GATE2B go low. |
| 4 | OAM | Auxiliary error amplifier minus input. This lead is compared to 1.2 V nominal on the auxiliary error amp plus lead and represents the $\mathrm{V}_{S S}$ voltage divided by ten. |
| 5 | OAOUT | Auxiliary error amplifier output lead. Source current $300 \mu \mathrm{~A}$ max. |
| 6 | OUVDELAY | Output undervoltage timing capacitor lead. If the controlled output voltages of either the main or the auxiliary supply are such that either $\mathrm{V}_{\mathrm{FB} 1}$ or $\mathrm{V}_{\mathrm{FB} 2}$ is greater that 4.1 V nominal, then capacitor from OUVDELAY to ground will begin charging. If the over voltage duration is such that the OUVDELAY voltage exceeds 5.0 V , then a fault will be initiated such that GATE1, GATE2 and GATE2B will go low. |
| 7 | ILIM1 | Pulse by pulse over current protection lead for the auxiliary PWM. A voltage exceeding 1.2 V nominal on ILIM1 will cause GATE1 to go low. A voltage exceeding 1.4 V nominal on ILIM1 will cause GATE1 to go low for at least two clock cycles. |
| 8 | RAMP1 | Current Ramp Input Lead for the Auxiliary PWM. A voltage which is linear with respect to current in the primary side of the auxiliary transformer is usually represented on this lead. A voltage exceeding $\mathrm{V}_{\mathrm{FB} 1}-0.13$ on RAMP1 will cause GATE1 to go low. |
| 9 | $\mathrm{V}_{\text {FB1 }}$ | Voltage Feedback Lead for the Auxiliary PWM. A voltage which represents the auxiliary power supply output voltage is fed to this lead. A voltage less than RAMP1+0.13 on $\mathrm{V}_{\mathrm{FB} 1}$ will cause GATE1 to go low. |
| 10 | $\mathrm{V}_{S S}$ | $\mathrm{V}_{S S}$ power/feedback input lead. See $\mathrm{V}_{\mathrm{CC}}$ for description of power operation. In addition, this lead is fed to a divide by ten resistor divider and compared to 1.2 V nominal at the positive side of the error amplifier. |
| 11 | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}}$ power input lead. This input runs off a Zener referenced supply until $\mathrm{V}_{S S}>\mathrm{V}_{\mathrm{CC}}$. Then an internal diode which runs between $\mathrm{V}_{\mathrm{SS}}$ and $\mathrm{V}_{\mathrm{CC}}$ turns on and all main power is derived from $\mathrm{V}_{\mathrm{SS}}$. |
| 12 | GATE1 | Auxiliary PWM gate drive lead. This output normally drives the FET which drives the auxiliary transformer. |
| 13 | GND | Ground lead. |
| 14 | GATE2 | Synchronous PWM gate drive lead. This output normally drives the FET which drives the main transformer. |
| 15 | GATE2B | Synchronous PWM gate drive lead. This output normally drives the FET for the gate drive transformer used for synchronous rectification. |
| 16 | $\mathrm{V}_{\text {FB2 }}$ | Voltage feedback lead for the synchronous PWM. A voltage which represents the main power supply output voltage is fed to this lead. A voltage less than RAMP2 +0.13 on $\mathrm{V}_{\mathrm{FB} 2}$ will cause GATE2 to go low and GATE2B to go high. |
| 17 | RAMP2 | Current ramp input lead for the synchronous PWM. A voltage which is linear with respect to current in the primary side of the main transformer is usually represented on this lead. A voltage exceeding $\mathrm{V}_{\mathrm{FB} 2}-0.13$ on RAMP2 will cause GATE2 to go low and GATE2B to go high. |
| 18 | ILIM2 | Pulse by pulse over current protection lead for the synchronous PWM. A voltage exceeding 1.2 V nominal on $\mathrm{I}_{\text {LIM2 }}$ will cause GATE2 to go low and GATE2B to go high. A voltage exceeding 1.4 V nominal on ILIM2 will cause GATE2 to go low and GATE2B to go high for at least two clock cycles. |
| 19 | DLYSET | GATE2, GATE2B non-overlap time adjustment lead. A $27 \mathrm{k} \Omega$ resistor from DLYSET to ground sets the non-overlap time to 45 ns nominal. |

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| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SSOP-24 | PIN SYMBOL | FUNCTION |
| 20 | FADJ | Frequency adjustment lead. A $27 \mathrm{k} \Omega$ resistor from FADJ to ground sets the clock frequency to 512 kHz nominal. |
| 21 | SYNCOUT | Clock output lead. This is a $50 \%$ duty cycle, 1.0 V to 5.0 V pulse whose rising edge is in phase with GATE1. This signal can be used to synchronize other power supplies. |
| 22 | $\mathrm{SYNC}_{\mathrm{IN}}$ | Clock synchronization lead. The internal clock frequency can be adjusted $+10 \%,-15 \%$ by the onset of positive edges of an external clock occurring on the $\mathrm{SYNC}_{\mathbb{I N}}$ lead. If the external clock frequency is outside the internal clock frequency by $+25 \%,-35 \%$ the external clock is ignored and the internal clock free runs. |
| 23 | PROGRAM | ENABLE programming input. See ENABLE for programming states. PROGRAM has at least $20 \mu \mathrm{~A}$ min. of available source current. |
| 24 | ENABLE | PWM enable input. If PROGRAM is HIGH then a LOW on ENABLE will allow GATE1, GATE2 and GATE2B to switch. If PROGRAM is LOW then a HIGH on ENABLE will allow GATE1, GATE2 and GATE2B to switch. If ENABLE is left floating, it will pull up to a HIGH level. ENABLE has at least $100 \mu \mathrm{~A}(\mathrm{~min})$ of available source current. |



CS5106

## THEORY OF APPLICATION

## THEORY OF OPERATION

## Powering the IC

The IC has one supply, $\mathrm{V}_{\mathrm{CC}}$, and one Ground lead. If $\mathrm{V}_{\mathrm{SS}}$ is used for a bootstrapped supply the diode between $\mathrm{V}_{\mathrm{SS}}$ and $\mathrm{V}_{\mathrm{CC}}$ is forward biased, and the IC will derive its power from $\mathrm{V}_{\mathrm{SS}}$. The internal logic monitors the supply voltage, $\mathrm{V}_{\mathrm{CC}}$. During abnormal operating conditions, all GATE drivers are held in a low state. The CS5106 requires 1.5 mA nominal of startup current.

## Startup

Assume the part is enabled and there are no over voltage or under voltage faults present. Also, assume that all auxiliary and main regulated output voltages start at 0 V . An 8.0 V , Zener referenced supply is typically applied to $\mathrm{V}_{\mathrm{CC}}$. When $\mathrm{V}_{\mathrm{CC}}$ exceeds 7.5 V , the 5.0 V reference is enabled and the OSC begins switching. If the $\mathrm{V}_{5 \text { REF }}$ lead is not excessively loaded such that $\mathrm{V}_{5 \mathrm{REF}}<4.5 \mathrm{~V}$ nominal, ' $\mathrm{V}_{\text {REF }} \mathrm{OK}$ ' goes 'high' and 'RUN1' will go 'high', releasing GATE1 from its low state. After GATE1 is released, it begins switching according to conditions set by the auxiliary control loop and the auxiliary supply, $\mathrm{V}_{\mathrm{SS}}$ begins to rise. When $V_{S S}>V_{C C}+V(D 1)$, P1 turns on and 'RUN2' goes 'high', releasing GATE2 and GATE2B from their low state. GATE2 and GATE2B begin switching according to conditions set by the main control loop and the main regulated output begins to rise. See startup waveforms in Figure 3.

## Soft Start

Soft Start for the auxiliary power supply is accomplished by placing a capacitor between OAOUT and Ground. The error amplifier has $200 \mu \mathrm{~A}$ of nominal of source current and is ideal for setting up a Soft Start condition for the auxiliary regulator. Care should be taken to make sure that the Soft Start timing requirements are not in conflict with any transient load requirements for the auxiliary supply as large capacitors on OAOUT will slow down the loop response. Also, the Soft Start capacitor must be chosen such that during start or restart, both outputs will come into regulation before the OUVDELAY timer trips. Soft Start for the main supply is accomplished by charging Soft Start capacitor C6 through D5 and R7 at start up. After the main supply has come into regulation C 6 continues to charge and is disconnected from the feedback loop by D8.


Figure 3. Startup Waveforms

## Voltage and Current Ramp PWM Comparator Inputs ( $\mathrm{V}_{\mathrm{FB} 1,2}$ and RAMP1,2 leads)

C10 and C11 are the PWM comparators for the auxiliary and main supplies. The feedback voltage $\left(\mathrm{V}_{\mathrm{FB}}\right)$ is divided by three and compared with a linear, voltage representation of the current in the primary side of the transformer (RAMP). When the output of the feedback comparator goes 'high', a reset signal is sent to the PWM flip-flop and the GATE driver is driven 'low'. A 130 mV offset on the RAMP leads allows the drivers to go to $0 \%$ duty cycle in the presence of light loads.

## Feedback Voltage for GATE1 Driver ( $\mathbf{V}_{\mathrm{FB} 1}$ )

Typically the output of the auxiliary error amplifier (A1) is tied to $\mathrm{V}_{\mathrm{FB} 1}$. The $\mathrm{V}_{\mathrm{SS}}$ output is programmed to 12 V by a 10:1 resistive divider on the negative input of the error amplifier and a fixed 1.2 V reference on the positive input of the error amplifier.

## Pulse by Pulse Over Current Protection and Hiccup Mode (lim1,2 leads)

C 12 and C 13 are the pulse by pulse current limit comparators for the auxiliary and main supplies. When the current in the primary side of the transformer increases such that the voltage across the current sense resistor exceeds 1.2 V nominal, the output of the current limit comparator goes
'high' and a reset signal is sent to the PWM flip-flop and the GATE driver is driven 'low'.

C16 and C17 are the second threshold, pulse by pulse current limit comparators for the auxiliary and main supplies. If the current in the primary side of the transformer increases so quickly that the current sense voltage is not limited by C12 or C13 and the voltage across the current sense resistor exceeds 1.4 V , the second threshold comparator will trip a delay circuit and force the GATE driver stage to go low and stay low for the next two clock cycles.

## Undervoltage and Overvoltage Thresholds

C5 and C8 are the undervoltage and overvoltage detection comparators. Typically, these inputs are tied across the middle resistor in a three resistor divider with the top resistor to $\mathrm{V}_{\text {IN }}$ and bottom resistor to Ground. The under voltage comparator has 200 mV of built in hysteresis with respect to a direct input on the UVSD lead. The under voltage comparator has its positive input referenced to 5.0 V while the over voltage comparator has its negative input referenced to 5.0 V . The output of both comparators are ORed at (G4) with the over current and enable inputs. The output of G4 feeds the input to the fault latch (F2).

## PROGRAM and ENABLE Leads

The PROGRAM lead controls the polarity of the ENABLE lead. If the PROGRAM lead is 'high' or floating, the GATE outputs will go low if the ENABLE input is tied 'high' or floating. If the PROGRAM lead is tied low, the GATE outputs will go low if the ENABLE input is tied 'low'. If the part is then enabled after switching the outputs low, the part will restart according to the procedure outlined in the "Startup" section.

## FAULT Logic

If a $\mathrm{V}_{\text {REF }}$, UVSD or OVSD fault occurs at any time, G4 resets the fault latch (F2). RUN1 goes low and all gate drivers cease switching and return to their 'low' state. When RUN1 goes low, the output of the auxiliary op-amp (A1) discharges the Soft Start capacitor and holds it low while RUN1 is low. If the fault condition is removed before the OUVDELAY timer is tripped, the IC will restart the power supplies when $\mathrm{V}_{\mathrm{SS}}<1.4 \mathrm{~V}$. If the OUVDELAY timer trips, the power supply must be restarted as explained in the following section.

## Output Undervoltage Delay Timer for the Main and Auxiliary Regulated Outputs

C7 and C4 are the output under voltage monitor comparators for the auxiliary and main supplies. If a regulated output drops such that its associated $\mathrm{V}_{\mathrm{FB}}$ voltage exceeds 4.1 V , the output undervoltage monitor comparator goes 'high' and the OUVDELAY capacitor begins charging from 0 V . A timing relation is set up by a $10 \mu \mathrm{~A}$ nominal current source, the OUVDELAY capacitor and a 5.0 V fault threshold at the input of C2 (see Figure 4). If any regulated output drops and stays low for the entire charge time of the OUVDELAY capacitor, a fault is triggered and all GATE drivers will go into a low state.

Once this fault is triggered, the IC will restart the power supplies only if the OUVDELAY fault is reset and ENABLE or UVSD is toggled while $\mathrm{V}_{\mathrm{SS}}<1.4 \mathrm{~V}$. To reset the OUVDELAY fault, both the $\mathrm{V}_{\mathrm{FB}}$ inputs must be less than 4.1 V. In the application circuit shown, $\mathrm{V}_{\mathrm{FB} 1}$ is brought low by OAOUT when RUN1 stops the oscillators. $\mathrm{V}_{\mathrm{FB} 2}$ is brought low when $\mathrm{V}_{\mathrm{AUXP}}$ bleeds down and the $\mathrm{V}_{\mathrm{FB}}$ 2 opto-isolator is no longer powered.


Figure 4. OUVDELAY Time vs. OUVDELAY Capacitance

## FADJ and DLYSET Leads

Amplifier A2 and transistor N3 create a current source follower whose output is FADJ. An external resistor from FADJ to ground completes the loop. The voltage across the resistor is set by a buffered, trimmed, precision reference. In this fashion, an accurate current is created which is used to charge and discharge an internal capacitor thereby creating an oscillator with a tight frequency tolerance. For FADJ resistor value selection, see Figure 5. Transistor N2 is in parallel with N3 and is used to created an independent current across the resistor from DLYSET to ground. This current is used to program the GATE non-overlap delay blocks in the main PWM drivers. For DLYSET resistor value selection, see Figure 6.


Figure 5. SYNC Out Frequency vs. FADJ Resistors


Figure 6. GATE Non-Overlap Time vs. DLYSET Resistance

## Oscillator

The oscillator generates two clock signals which are 180 degrees out of phase with respect to time. One clock signal feeds the main driver and the other feeds the auxiliary driver. Because the drivers are never turned on at the same time, ground noise and supply noise is minimized. The clock signals are actually 100 ns pulse spikes. These spikes create a narrow driver turn-on window. This narrow window prevents the driver from spurious turn on in the middle of a clock cycle. The oscillator can be synchronized by an external clock (slave) or drive the clocks of other controllers (master). See Figure 7 for the relationship between SYNC, CLK, and GATE waveforms.


Figure 7. SYNC, GATE and CLOCK Waveforms

## SYNC $_{\text {IN }}$ and SYNC OUt Leads

Multiple supplies can be synchronized to one supply by using the SYNC leads. The SYNC ${ }_{\text {IN }}$ and SYNCOUT pulses are always 180 degrees out of phase. The SYNC IN input is always in phase with the clock signal for the main driver and the SYNC OUT output is always in phase with the clock signal for the auxiliary driver. If the IC is being used as a slave, the incoming frequency must be within $+10 \%,-20 \%$ of the programmed frequency set by its own FADJ resistor. If the frequency on the $\mathrm{SYNC}_{\text {IN }}$ lead is outside the internal frequency by $+25 \%,-35 \%$, the $\mathrm{SYNC}_{\text {IN }}$ input will be ignored. If the SYNC signal stops while the power supplies are in synchronized operation, the synchronized supplies
will stop and restart free running. If the $\mathrm{SYNC}_{\text {IN }}$ signal drifts out of frequency specification while the power supplies are in synchronized operation, the synchronized supplies will begin to free run without restarting.

## Slope Compensation

DC-DC converters with current mode control require slope compensation to avoid instability at duty cycles greater than $50 \%$. A slope is added to the current sense waveform (or subtracted from the voltage waveform) that is equal to a percentage ( $75 \%$ typical) of the down slope of the inductor current. In the application diagram shown, the bootstrap (flyback) transformer inductance can be chosen so that the duty cycle never exceeds $50 \%$ and therefore does not require slope compensation. The buck indicator in the forward converter would typically be chosen to work in continuous conduction mode with a maximum duty cycle of $50-60 \%$ and would require slope compensation. Slope compensation is accomplished as follows: R9 and C9 form a ramp waveform rising each time GATE 2 turns on. C9 is discharged through D3 to the same level each cycle regardless of duty cycle. R10 and R11 are chosen to control the amount of slope compensation. C10 provides filtering for noise and turn-on spikes. To calculate the required slope compensation, calculate the buck indicator down current and the corresponding voltage slope at the current sense resistor-R12.

The buck inductor down slope is:

$$
\text { Inductor_Slope }=\frac{\mathrm{V}_{\mathrm{OUT}}+\mathrm{V}_{\mathrm{Q} 5}}{\mathrm{~L} 1(\mu \mathrm{H})}\left(\frac{\mathrm{A}}{\mu \mathrm{~S}}\right)
$$

The equivalent down slope at the current sense resistor for this application circuit is:
Slope @ R12 $=$ Inductor_Slope $\times \frac{\mathrm{NST}_{2}}{\text { NPT2 }} \times \frac{\mathrm{NPT} 3}{\mathrm{NST} 3} \times$ R12 $\left(\frac{\mathrm{V}}{\mu \mathrm{S}}\right)$
After choosing R9 and C9 to generate a ramp with a time constant of about 5 times the oscillator period, R10 and R11 can be chosen for the voltage at RAMP2 to be 1.75 of the voltage across R12.

## Synchronous Rectification

Synchronous rectification was chosen to reduce losses in the forward converter. Improvements in efficiency will be most significant in low voltage, medium and high current converters where improvement in conduction loss offsets any added losses for gate drive.

In the application circuit Q4 is turned on and off by the forward transformer. Q5 is turned on and off through pulse transformer T4 and the gate driver formed by Q6 and Q7. Because Q4 and Q5 are driven through different types of components, differences in propagation delay must be considered. The DLYSET resistor should be chosen to avoid shoot-through or excessive off time.

## Gate Drive Capability

All GATE drive outputs have nominal peak currents of 0.5A. See Figures 8 and 9 for typical rise and fall times.


Figure 8. Typical GATE2, 2B Switching Times


## Design Considerations

The circuit board should utilize high frequency layout techniques to avoid pulse width jitter and false triggering of high impedance inputs. Ground plane(s) should be employed. Signal grounds and power grounds should be run separately. Portions of the circuit with high slew rates or current pulses should be segregated from sensitive areas. Shields and decoupling capacitors should be used as required.

Special care should be taken to prevent coupling between the SYNC leads and the surrounding leads. Depending on the circuit board layout and component values, decoupling capacitors or reduction in resistor values might be required to reduce noise pick-up on the FADJ and DLYSET resistors. Decoupling capacitors or active pull-up/down might be required to prevent false triggering of the ENABLE and PROGRAM leads.

Figure 9. Typical GATE1 Switching Times
PACKAGE THERMAL DATA

| Parameter |  | SSOP-24 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 23 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 117 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC34067, MC33067

## High Performance <br> Resonant Mode Controllers

The MC34067/MC33067 are high performance zero voltage switch resonant mode controllers designed for off-line and dc-to-dc converter applications that utilize frequency modulated constant off-time or constant deadtime control. These integrated circuits feature a variable frequency oscillator, a precise retriggerable one-shot timer, temperature compensated reference, high gain wide bandwidth error amplifier, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator, programmable soft-start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

These devices are available in dual-in-line and surface mount packages.

- Zero Voltage Switch Resonant Mode Operation
- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Precision One-Shot Timer for Controlled Off-Time
- Internally Trimmed Bandgap Reference
- 4.0 MHz Error Amplifier
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft-Start Circuitry
- Low Startup Current for Off-Line Operation


Figure 1. Simplified Block Diagram

## ON Semiconductor

http://onsemi.com


PIN CONNECTIONS

(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC34067DW | SO-16W | 47 Units/Rail |
| MC34067DWR2 | SO-16W | 1000 Tape \& Reel |
| MC34067P | PDIP-16 | 25 Units/Rail |
| MC33067DW | SO-16W | 47 Units/Rail |
| MC33067DWR2 | SO-16W | 1000 Tape \& Reel |
| MC33067P | PDIP-16 | 25 Units/Rail |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 20 | V |
| Drive Output Current, Source or Sink (Note 1) Continuous Pulsed ( $0.5 \mu \mathrm{~s}, 25 \%$ Duty Cycle | Io | $\begin{aligned} & 0.3 \\ & 1.5 \end{aligned}$ | A |
| Error Amplifier, Fault, One-Shot, Oscillator and Soft-Start Inputs | $V_{\text {in }}$ | -1.0 to + 6.0 | V |
| UVLO Adjust Input | $\mathrm{V}_{\text {in(UVLO) }}$ | -1.0 to $\mathrm{V}_{C C}$ | V |
| Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package, Case 751G $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> P Suffix, Plastic Package, Case 648 $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 862 \\ & 145 \\ & \\ & 1.25 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | + 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature MC34067 <br> MC33067 | $\mathrm{T}_{\mathrm{A}}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ [Note 2], $\mathrm{R}_{\mathrm{OSC}}=18.2 \mathrm{k}, \mathrm{R}_{\mathrm{VFO}}=2940, \mathrm{C}_{\mathrm{OSC}}=300 \mathrm{pF}, \mathrm{R}_{\mathrm{T}}=2370 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=300 \mathrm{pF}$, $C_{L}=1.0 \mathrm{nF}$. For typical values $T_{A}=25^{\circ} \mathrm{C}$, for min/max values $T_{A}$ is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| Reference Output Voltage ( $\mathrm{l}_{0}=0 \mathrm{~mA}, \mathrm{~T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {ref }}$ | 5.0 | 5.1 | 5.2 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=10$ to 18 V ) | Regline | - | 1.0 | 20 | mV |
| Load Regulation ( $\mathrm{l}_{0}=0 \mathrm{~mA}$ to 10 mA ) | Regload | - | 1.0 | 20 | mV |
| Total Output Variation Over Line, Load, and Temperature | $\mathrm{V}_{\text {ref }}$ | 4.9 | - | 5.3 | V |
| Output Short Circuit Current | 10 | 25 | 100 | 190 | mA |
| Reference Undervoltage Lockout Threshold | $\mathrm{V}_{\text {th }}$ | 3.8 | 4.3 | 4.8 | V |

ERROR AMPLIFIER

| Input Offset Voltage $\left(\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{IO}}$ | - | 1.0 | 10 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 0.2 | 1.0 | $\mu \mathrm{~A}$ |
| Input Offset Current $\left(\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IO}}$ | - | 0 | 0.5 | $\mu \mathrm{~A}$ |
| Open Loop Voltage Gain $\left(\mathrm{V}_{\mathrm{CM}}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=2.0 \mathrm{~V}\right)$ | $\mathrm{A}_{\mathrm{VOL}}$ | 70 | 100 | - | dB |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz})$ | GBW | 3.0 | 5.0 | - | MHz |
| Input Common Mode Rejection Ratio $\left(\mathrm{V}_{\mathrm{CM}}=1.5\right.$ to 5.0 V$)$ | CMR | 70 | 95 | - | dB |
| Power Supply Rejection Ratio $\left(\mathrm{V}_{\mathrm{CC}}=10\right.$ to $\left.18 \mathrm{~V}, \mathrm{f}=120 \mathrm{~Hz}\right)$ | PSR | 80 | 100 | - | dB |
| Output Voltage Swing <br> High State <br> Low State | $\mathrm{V}_{\mathrm{OH}}$ | 2.8 | 3.2 | - | V |

1. Maximum package power dissipation limits must be observed.
2. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 12 V .
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34067 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34067
$=-40^{\circ} \mathrm{C}$ for MC33067 $=+85^{\circ} \mathrm{C}$ for MC33067

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ [Note 6], $\mathrm{R}_{\mathrm{OSC}}=18.2 \mathrm{k}, \mathrm{R}_{\mathrm{VFO}}=2940, \mathrm{C}_{\mathrm{OSC}}=300 \mathrm{pF}$, $R_{T}=2370 \mathrm{k}, \mathrm{C}_{T}=300 \mathrm{pF}, \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 7], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Frequency (Error Amp Output Low) <br> Total Variation ( $\mathrm{V}_{\mathrm{CC}}=10$ to $18 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {Low }}$ to $\mathrm{T}_{\text {High, }}, 25^{\circ} \mathrm{C}$ | ${ }^{\text {fosc(low) }}$ | 490 | - | 550 | kHz |
| Frequency (Error Amp Output High) <br> Total Variation ( $\mathrm{V}_{\mathrm{CC}}=10$ to $18 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {Low }}$ to $\mathrm{T}_{\text {High, }}, 25^{\circ} \mathrm{C}$ | $\mathrm{f}_{\text {OSC (high) }}$ | 1850 | - | 2200 | kHz |
| Oscillator Control Input Voltage, Pin 3 @ $25^{\circ} \mathrm{C}$ | $V_{\text {in }}$ | - | 2.5 | - | V |

## ONE-SHOT

| Drive Output Off-Time |  |  |  |  | ns |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  |  |  |  |  |
| Total Variation $\left(\mathrm{V}_{\mathrm{CC}}=10\right.$ to $18 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {Low }}$ to $\mathrm{T}_{\text {High }}$ | $\mathrm{t}_{\text {Blank }}$ | 235 | 250 | 270 |  |

DRIVE OUTPUTS

| Output Voltage |  |  |  |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low State ( $\mathrm{I}_{\text {Sink }}=20 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {OL }}$ | - | 0.8 | 1.2 |  |
| $\left(I_{\text {Sink }}=200 \mathrm{~mA}\right)$ |  | - | 1.5 | 2.0 |  |
| High State ( ${ }_{\text {Source }}=20 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{OH}}$ | 9.5 | 10.3 | - |  |
| ( Source $^{\text {a }} 200 \mathrm{~mA}$ ) |  | 9.0 | 9.7 | - |  |
| Output Voltage with UVLO Activated ( $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$, $\left.\mathrm{I}_{\text {Sink }}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {OL(UVLO) }}$ | - | 0.8 | 1.2 | V |
| Output Voltage Rise Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ ) | $\mathrm{t}_{\mathrm{r}}$ | - | 20 | 50 | ns |
| Output Voltage Fall Time ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ ) | $\mathrm{t}_{\mathrm{f}}$ | - | 15 | 50 | ns |

FAULT COMPARATOR

| Input Threshold | $\mathrm{V}_{\text {th }}$ | 0.93 | 1.0 | 1.07 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\text {Pin } 10}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | -2.0 | -10 | $\mu \mathrm{~A}$ |
| Propagation Delay to Drive Outputs (100 mV Overdrive) | $\mathrm{t}_{\text {PLH }}(\mathrm{In} / \mathrm{Out})$ | - | 60 | 100 | ns |

## SOFT-START

| Capacitor Charge Current $\left(V_{\text {Pin 11 }}=2.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {chg }}$ | 4.5 | 9.0 | 14 | $\mu \mathrm{~A}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Capacitor Discharge Current $\left(\mathrm{V}_{\text {Pin 11 }}=2.5 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {dischg }}$ | 3.0 | 8.0 | - | mA |

UNDERVOLTAGE LOCKOUT

| Startup Threshold, $\mathrm{V}_{\mathrm{CC}}$ Increasing Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\text {th(UVLO) }}$ | $\begin{gathered} 14.8 \\ 8.0 \end{gathered}$ | $\begin{aligned} & 16 \\ & 9.0 \end{aligned}$ | $\begin{gathered} 17.2 \\ 10 \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On <br> Enable/UVLO Adjust Pin Open <br> Enable/UVLO Adjust Pin Connected to $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{CC}(\text { min })}$ | $\begin{aligned} & 8.0 \\ & 7.6 \end{aligned}$ | $\begin{aligned} & 9.0 \\ & 8.6 \end{aligned}$ | $\begin{aligned} & 10 \\ & 9.6 \end{aligned}$ | V |
| Enable/UVLO Adjust Shutdown Threshold Voltage | $\mathrm{V}_{\text {th(Enable) }}$ | 6.0 | 7.0 | - | V |
| Enable/UVLO Adjust Input Current (Pin $9=0 \mathrm{~V}$ ) | $\mathrm{I}_{\text {in(Enable) }}$ | - | $-0.2$ | -1.0 | mA |

TOTAL DEVICE

| Power Supply Current (Enable/UVLO Adjust Pin Open) |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Startup (VCC $=13.5 \mathrm{~V})$ | I CC | - | 0.5 | 0.8 | mA |
| Operating (fosc $=500 \mathrm{kHz})($ Note 6) |  | - | 27 | 35 |  |

5. Maximum package power dissipation limits must be observed.
6. Adjust $\mathrm{V}_{\mathrm{CC}}$ above the Startup threshold before setting to 12 V .
7. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
8. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34067 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34067

$$
=-40^{\circ} \mathrm{C} \text { for MC33067 } \quad=+85^{\circ} \mathrm{C} \text { for MC33067 }
$$



Figure 2. Oscillator Timing Resistor versus Discharge Time


Figure 4. Error Amp Output Saturation Voltage versus Oscillator Control Current


Figure 3. Oscillator Frequency versus Oscillator Control Current


Figure 5. One-Shot Timing Resistor versus Period


Figure 6. Open Loop Voltage Gain and Phase versus Frequency


Figure 7. Reference Output Voltage Change versus Temperature


Figure 8. Reference Voltage Change versus Source Current


Figure 10. Drive Output Waveform


Figure 12. Operating Frequency versus Supply Current


Figure 9. Drive Output Saturation Voltage versus Load Current


Figure 11. Soft-Start Saturation Voltage versus Capacitor Discharge Current


Figure 13. Supply Current versus Supply Voltage


Figure 14. MC34067 Representative Block Diagram


Error Amp output high, minimum losc current occurring at minimum input voltage, maximum load.

Error Amp output low, maximum losc current occurring at maximum input voltage, minimum load.

Figure 15. Timing Diagram

## Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional pulse-width modulated control. When compared to pulse-width modulated converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. A new integrated circuit has been developed to support this trend in power supply design. The MC34067 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz . This integrated circuit provides the features and performance specifically for zero voltage switching resonant mode power supply applications.

The primary purpose of the control chip is to provide a fixed off-time to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the front page, which identifies the main functional blocks and the block-to-block interconnects. Figure 14 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency. Included in this section are a variable frequency Oscillator, a One-Shot, a pulse Steering Flip-Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft-Start circuit, and a fault detector.

## Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One-Shot timer and Error Amplifier. The Oscillator triggers the One-Shot which generates a pulse that is alternately steered to a pair of totem pole output drivers by a toggle Flip-Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

## Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One-Shot timer and initiating the output deadtime, the oscillator also determines the initial voltage for the one-shot capacitor. The Oscillator is designed to operate at
frequencies exceeding 1.0 MHz . The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components.

The functional diagram of the Oscillator and One-Shot timer is shown in Figure 16. The oscillator capacitor ( $\mathrm{C}_{\mathrm{OSC}}$ ) is initially charged by transistor Q1. When COSC exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing COSC to discharge through the external resistor, ( $\mathrm{R}_{\mathrm{OSC}}$ ), and the oscillator control current, ( $\mathrm{I}_{\mathrm{OSC}}$ ). When the voltage on $\mathrm{C}_{\mathrm{OSC}}$ falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges Cosc.

Cosc charges from 3.6 V to 5.1 V in less than 50 ns . The high slew rate of COSC and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through a diode to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V .


Figure 16. Oscillator and One-Shot Timer

The frequency of the Oscillator is modulated by varying the current flowing out of the Oscillator Control Current (I $\mathrm{I}_{\mathrm{OSC}}$ ) pin. The $\mathrm{I}_{\text {OSC }}$ pin is the output of a voltage regulator. The input of the voltage regulator is tied to the variable frequency oscillator. The discharge current of the Oscillator increases by increasing the current out of the IOSC pin. Resistor R VFO is used in conjunction with the Error Amp output to change the $\mathrm{I}_{\mathrm{OSC}}$ current. Maximum frequency occurs when the Error Amplifier output is at its low state with a saturation voltage of 0.1 V at 1.0 mA .

The minimum oscillator frequency will result when the IOSC current is zero, and CosC is discharged through the external resistor ( $\mathrm{R}_{\mathrm{OSC}}$ ). This occurs when the Error Amplifier output is at its high state of 2.5 V . The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor $\mathrm{R}_{\mathrm{OSC}}$ and $\mathrm{R}_{\mathrm{VFO}}$. The minimum frequency is programmed by $\mathrm{R}_{\mathrm{OSC}}$ using Equation 1:

$$
\begin{equation*}
\mathrm{R}_{\mathrm{OSC}}=\frac{\frac{1}{f_{(\min )}}-\mathrm{t}_{\text {PD }}}{\mathrm{C}_{\mathrm{OSC}} \ln \left(\frac{5.1}{3.6}\right)}=\frac{\mathrm{t}_{(\mathrm{max})}-70 \mathrm{~ns}}{0.348 \mathrm{C}_{\mathrm{OSC}}} \tag{1}
\end{equation*}
$$

where $t_{P D}$ is the internal propagation delay.
The maximum oscillator frequency is set by the current through resistor $\mathrm{R}_{\mathrm{VFO}}$. The current required to discharge $\mathrm{C}_{\text {OSC }}$ at the maximum oscillator frequency can be calculated by Equation 2:

$$
\begin{equation*}
I_{(\max )}=\operatorname{CoSC}_{\text {OSC }} \frac{5.1-3.6}{\frac{1}{f_{(\max )}}}=1.5 \mathrm{C}_{\text {OSC }^{f}} f_{(\max )} \tag{2}
\end{equation*}
$$

The discharge current through R $_{\text {OSC }}$ must also be known and can be calculated by Equation 3:

$$
\left.\begin{array}{rl}
\mathrm{I}_{\mathrm{OSC}}= & \frac{5.1-3.6}{\mathrm{R}_{\mathrm{OSC}}} \varepsilon  \tag{3}\\
& =\frac{1.5}{\mathrm{R}_{\mathrm{OSC}}} \varepsilon^{\left(-\frac{1}{f_{(\text {min })}}\right.} \mathrm{R}_{\mathrm{OSC}} \mathrm{C}_{\mathrm{OSC}}
\end{array}\right)
$$

Resistor R VFO can now be calculated by Equation 4:

$$
\begin{equation*}
\mathrm{R}_{\text {VFO }}=\frac{2.5-\mathrm{V}_{\text {EAsat }}}{I_{(\max )}-\mathrm{I}_{\mathrm{R}}} \tag{4}
\end{equation*}
$$

## One-Shot Timer

The One-Shot is designed to disable both outputs simultaneously providing a deadtime before either output is enabled. The One-Shot capacitor $\left(\mathrm{C}_{\mathrm{T}}\right)$ is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 16. The one-shot period begins when the oscillator comparator turns off Q 1 , allowing $\mathrm{C}_{\mathrm{T}}$ to discharge. The period ends when resistor $\mathrm{R}_{\mathrm{T}}$ discharges $\mathrm{C}_{\mathrm{T}}$ to the threshold of the One-Shot comparator. The lower threshold of the One-Shot is 3.6 V . By choosing $\mathrm{C}_{\mathrm{T}}, \mathrm{R}_{\mathrm{T}}$ can by solved by Equation 5:

$$
\begin{equation*}
\mathrm{R}_{\mathrm{T}}=\frac{\mathrm{t} O \mathrm{OS}}{\mathrm{C}_{\mathrm{T}} \ln \left(\frac{5.1}{3.6}\right)}=\frac{\mathrm{t}_{\mathrm{OS}}}{0.348 \mathrm{C}_{\mathrm{T}}} \tag{5}
\end{equation*}
$$

Errors in the threshold voltage and propagation delays through the output drivers will affect the One-Shot period. To guarantee accuracy, the output pulse of the control chip is trimmed to within $5 \%$ of 250 ns with nominal values of $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$.

The outputs of the Oscillator and One-Shot comparators are OR'd together to produce the pulse tos, which drives the Flip-Flop and output drivers. The output pulse ( $\mathrm{t}_{\mathrm{OS}}$ ) is initiated by the Oscillator and terminated by the One-Shot comparator. With zero-voltage resonant mode converters, the oscillator discharge time should never be set less than the one-shot period.

## Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features dc open loop gain greater than 70 dB , input offset voltage of less than 10 mV and a guaranteed minimum gain-bandwidth product of 2.5 MHz . The input common mode range extends from 1.5 V to 5.1 V , which includes the reference voltage.


Figure 17. Error Amplifier and Clamp
When the Error Amplifier output is coupled to the $\mathrm{I}_{\mathrm{OSC}}$ pin by $\mathrm{R}_{\mathrm{VFO}}$, as illustrated in Figure 17, it provides the Oscillator Control Current, IOSC. The output swing of the Error Amplifier is restricted by a clamp circuit to improve its transient recovery time.

## Output Section

The pulse( $\mathrm{t}_{\mathrm{OS}}$ ), generated by the Oscillator and One-Shot timer is gated to dual totem-pole output drives by the Steering Flip-Flop shown in Figure 18. Positive transitions of $\mathrm{t}_{\mathrm{OS}}$ toggle the Flip-Flop, which causes the pulses to alternate between Output A and Output B. The flip-flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.


Figure 18. Steering Flip-Flop and Output Drivers

The totem-pole output drivers are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem-pole driver normally increases the risk of high cross conduction
current during output transitions. The MC34067 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate power ground pin is provided to isolate the sensitive analog circuitry from large transient currents.


Figure 19. Undervoltage Lockout and Reference

## PERIPHERAL SUPPORT FUNCTIONS

The MC34067 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft-start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a controlled manner and that the system will be quickly disabled when a fault condition occurs.

## Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input $\mathrm{V}_{\mathrm{CC}}$ voltage and the regulated reference voltage as illustrated in Figure 19. When $\mathrm{V}_{\mathrm{CC}}$ increases to the upper threshold voltage, the $\mathrm{V}_{\mathrm{CC}}$ UVLO comparator enables the Reference Regulator. After the $\mathrm{V}_{\text {ref }}$ output of the Reference Regulator rises to 4.2 V , the $\mathrm{V}_{\text {ref }} \mathrm{UVLO}$ comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing $\mathrm{V}_{\mathrm{CC}}$ to the lower threshold voltage causes the $\mathrm{V}_{\mathrm{CC}}$ UVLO comparator to disable the Reference Regulator. The $\mathrm{V}_{\text {ref }}$ UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

The Enable/UVLO Adjust pin allows the power supply designer to select the $\mathrm{V}_{\mathrm{CC}}$ UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V . If this pin is connected to the $\mathrm{V}_{\mathrm{CC}}$ terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V , respectively. Forcing the Enable/UVLO Adjust pin low will pull the $\mathrm{V}_{\mathrm{CC}}$ UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than $2 \%$ initial accuracy and includes active short circuit protection.

## Fault Detector

The high speed Fault Comparator illustrated in Figure 20 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. The Fault Comparator output connects to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Comparator output is also OR'd with the UVLO output from the $\mathrm{V}_{\text {ref }}$ UVLO comparator to produce the logic output labeled "UVLO+Fault". This signal disables the Oscillator and One-Shot by forcing both the $\mathrm{C}_{\text {OSC }}$ and $\mathrm{C}_{\mathrm{T}}$ capacitors to be continually charged.


Figure 20. Fault Detector and Soft-Start

## Soft-Start Circuit

The Soft-Start circuit shown in Figure 20 forces the variable frequency Oscillator to start at the maximum frequency and ramp downward until regulated by the feedback control loop. The external capacitor at the C Soft-Start terminal is initially discharged by the UVLO+Fault signal. The low voltage on the capacitor passes through the Soft-Start Buffer to hold the Error

Amplifier output low. After UVLO+Fault switches to a logic zero, the soft-start capacitor is charged by a $9.0 \mu \mathrm{~A}$ current source. The buffer allows the Error Amplifier output to follow the soft-start capacitor until it is regulated by the Error Amplifier inputs. The soft-start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $\mathrm{C}_{\text {Soft-Start }}$ terminal.

## APPLICATIONS INFORMATION

The MC34067 is specifically designed for zero voltage switching (ZVS) quasi-resonant converter (QRC) applications. The IC is optimized for double-ended push-pull or bridge type converters operating in continuous conduction mode. Operation of this type of ZVS with resonant properties is similar to standard push-pull or bridge circuits in that the energy is transferred during the transistor on-time. The difference is that a series resonant tank is usually introduced to shape the voltage across the power transistor prior to turn-on. The resonant tank in this topology is not used to deliver energy to the output as is the case with zero current switch topologies. When the power transistor is enabled the voltage across it should already be zero, yielding minimal switching loss. Figure 21 shows a timing diagram for a half-bridge ZVS QRC. An application circuit is shown in Figure 22. The circuit built is a dc to dc half-bridge converter delivering 75 W to the output from a 48 V source.

When building a zero voltage switch (ZVS) circuit, the objective is to waveshape the power transistor's voltage waveform so that the voltage across the transistor is zero when the device is turned on. The purpose of the control IC is to allow a resonant tank to waveshape the voltage across the power transistor while still maintaining regulation. This is accomplished by maintaining a fixed deadtime and by varying the frequency; thus the effective duty cycle is changed.

Primary side resonance can be used with ZVS circuits. In the application circuit, the elements that make the resonant tank are the primary leakage inductance of the transformer $\left(\mathrm{L}_{\mathrm{L}}\right)$ and the average output capacitance ( $\mathrm{C}_{\mathrm{OSS}}$ ) of a power $\operatorname{MOSFET}\left(\mathrm{C}_{\mathrm{R}}\right)$. The desired resonant frequency for the application circuit is calculated by Equation 6:

$$
\begin{equation*}
f_{r}=\frac{1}{2 \pi \sqrt{L_{L}{ }^{2 C_{R}}}} \tag{6}
\end{equation*}
$$

In the application circuit, the operating voltage is low and the value of Coss versus Drain Voltage is known. Because the C COSS of a MOSFET changes with drain voltage, the value of the $C_{R}$ is approximated as the average CoSS of the MOSFET. For the application circuit the average Coss can be calculated by Equation 7:

$$
\begin{equation*}
C_{R}=\sqrt{2} * C_{\text {OSS }} \text { measured at } \frac{1}{2} V_{\text {in }} \tag{7}
\end{equation*}
$$

The MOSFET chosen fixes $\mathrm{C}_{\mathrm{R}}$ and that $\mathrm{L}_{\mathrm{L}}$ is adjusted to achieve the desired resonant frequency.

However, the desired resonant frequency is less critical than the leakage inductance. Figure 21 shows the primary current ramping toward its peak value during the resonant transition. During this time, there is circulating current flowing through the secondary inductance, which effectively makes the primary inductance appear shorted. Therefore, the current through the primary will ramp to its peak value at a rate controlled by the leakage inductance and the applied voltage. Energy is not transferred to the secondary during this stage, because the primary current has not overcome the circulating current in the secondary. The larger the leakage inductance, the longer it takes for the primary current to slew. The practical effect of this is to lower the duty cycle, thus reducing the operating range.

The maximum duty cycle is controlled by the leakage inductance, not by the MC34067. The One-Shot in the MC34067 only assures that the power switch is turned on under a zero voltage condition. Adjust the one-shot period so that the output switch is activated while the primary current is slewing but before the current changes polarity. The resonant stage should then be designed to be as long as the time for the primary current to go to zero amps.

MC34067, MC33067


Figure 21. Application Timing Diagram


| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=40 \mathrm{~V}$ to $56 \mathrm{~V}, \mathrm{I}=15 \mathrm{~A}$ | $20 \mathrm{mV}= \pm 0.198 \%$ |
| Load Regulation | $\mathrm{V}_{\text {in }}=48 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~A}$ to 15 A | $4.0 \mathrm{mV}= \pm 0.039 \%$ |
| Output Ripple | $\mathrm{V}_{\text {in }}=48 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=15 \mathrm{~A}, \mathrm{f}_{\text {switch }}=1.0 \mathrm{MHz}$ | $25 \mathrm{mV} \mathrm{V}_{\mathrm{p}-\mathrm{p}}$ |
| Efficiency | $\mathrm{V}_{\text {in }}=48 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=10 \mathrm{~A}, \mathrm{f}_{\text {switch }}=1.7 \mathrm{MHz}$ | $83.5 \%$ |
|  | $\mathrm{~V}_{\text {in }}=48 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=15 \mathrm{~A}, \mathrm{f}_{\text {switch }}=1.0 \mathrm{MHz}$ | $84.2 \%$ |

, 8 leakage Inductance $=1.0 \mu$
= All windings: 8 turns \#36 AWG Core: Philips 3F3 EP7-3F3 Bobbin: Philips EP7PCB1-6

T3 = Coilcraft D1870 (100 turns)
L1 $=2$ turns \#48 AWG (1300 strands litz wire) Core: Philips 3F3 EP10-3F3 Bobbin: Philips EP10PCB1-8 Inductance $=1.8 \mu \mathrm{H}$
L2 = 5 turns \#48 AWG (1300 strands litz wire) Core: $0.5^{\prime \prime}$ diameter air code nductance $=100 \mathrm{nH}$

Heatsinks = AAVID Engineering Inc. 533402B02552 with clip MC34067-5803
nsulators $=$ Berquist Sil-Pad 1500

Figure 22. Application Circuit

(Top View)
Figure 23. Printed Circuit Board and Component Layout

## MAX1720

## Switched Capacitor Voltage Inverter with Shutdown

The MAX1720 is a CMOS charge pump voltage inverter that is designed for operation over an input voltage range of 1.15 V to 5.5 V with an output current capability in excess of 50 mA . The operating current consumption is only $67 \mu \mathrm{~A}$, and a power saving shutdown input is provided to further reduce the current to a mere $0.4 \mu \mathrm{~A}$. The device contains a 12 kHz oscillator that drives four low resistance MOSFET switches, yielding a low output resistance of $26 \Omega$ and a voltage conversion efficiency of $99 \%$. This device requires only two external $10 \mu \mathrm{~F}$ capacitors for a complete inverter making it an ideal solution for numerous battery powered and board level applications. The MAX1720 is available in the space saving TSOP-6 (SOT-23-6) package.

## Features

- Operating Voltage Range of 1.15 V to 5.5 V
- Output Current Capability in Excess of 50 mA
- Low Current Consumption of $67 \mu \mathrm{~A}$
- Power Saving Shutdown Input for a Reduced Current of $0.4 \mu \mathrm{~A}$
- Operation at 12 kHz
- Low Output Resistance of $26 \Omega$
- Space Saving TSOP-6 (SOT-23-6) Package


## Typical Applications

- LCD Panel Bias
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand Held Instruments


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## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MAX1720EUT | TSOP-6 | 3000 Tape \& Reel |



This device contains 77 active transistors.

Figure 1. Typical Application

## MAX1720

MAXIMUM RATINGS*

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage Range ( $\mathrm{V}_{\text {in }}$ to GND) | $V_{\text {in }}$ | -0.3 to 6.0 | V |
| Output Voltage Range (V $\mathrm{V}_{\text {out }}$ to GND) | $V_{\text {out }}$ | -6.0 to 0.3 | V |
| Output Current (Note 1) | Iout | 100 | mA |
| Output Short Circuit Duration (V out $^{\text {to GND, Note 1) }}$ | $\mathrm{t}_{\text {Sc }}$ | Indefinite | sec |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation and Thermal Characteristics Thermal Resistance, Junction to Air Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ | $\begin{gathered} \mathrm{R}_{\text {QJA }} \\ \mathrm{P}_{\mathrm{D}} \end{gathered}$ | $\begin{aligned} & 256 \\ & 313 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ mW |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |

*ESD Ratings
ESD Machine Model Protection up to 200 V, Class B
ESD Human Body Model Protection up to 2000 V, Class 2
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}, \mathrm{C}_{1}=10 \mu \mathrm{~F}, \mathrm{C}_{2}=10 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right.$ to $85^{\circ} \mathrm{C}$, typical values shown are for $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted. See Figure 14 for Test Setup.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Supply Voltage Range (SHDN $=\mathrm{V}_{\mathrm{in}}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ ) | $V_{\text {in }}$ | 1.5 to 5.5 | 1.15 to 6.0 | - | V |
| $\begin{aligned} & \text { Supply Current Device Operating ( } \left.\overline{\mathrm{SHDN}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty\right) \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C} \end{aligned}$ | 1 l | - | $\begin{aligned} & 67 \\ & 72 \end{aligned}$ | $\begin{gathered} 90 \\ 100 \end{gathered}$ | $\mu \mathrm{A}$ |
| Supply Current Device Shutdown (SHDN $=0 \mathrm{~V}$ ) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C} \end{aligned}$ | ISHDN | - | $\begin{aligned} & 0.4 \\ & 1.6 \end{aligned}$ | - | $\mu \mathrm{A}$ |
| Oscillator Frequency $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \end{aligned}$ | fosc | $\begin{aligned} & 8.4 \\ & 6.0 \end{aligned}$ | 12 | $\begin{gathered} 15.6 \\ 21 \end{gathered}$ | kHz |
| Output Resistance ( $\mathrm{l}_{\text {out }}=25 \mathrm{~mA}$, Note 2) | $\mathrm{R}_{\text {out }}$ | - | 26 | 50 | $\Omega$ |
| Voltage Conversion Efficiency ( $\mathrm{R}_{\mathrm{L}}=\infty$ ) | $\mathrm{V}_{\text {EfF }}$ | 99 | 99.9 | - | \% |
| Power Conversion Efficiency ( $\mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k}$ ) | $\mathrm{P}_{\text {EfF }}$ | - | 96 | - | \% |
| Shutdown Input Threshold Voltage ( $\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}$ to 5.5 V ) High State, Device Operating Low State, Device Shutdown | $\left.\mathrm{V}_{\text {th( }} \overline{\text { SHDN }}\right)$ | - | $\begin{aligned} & 0.6 \mathrm{~V}_{\text {in }} \\ & 0.5 \mathrm{~V}_{\text {in }} \end{aligned}$ | - | V |
| Shutdown Input Bias Current <br> High State, Device Operating, SHDN $=5.0 \mathrm{~V}$ $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C} \end{aligned}$ <br> Low State, Device Shutdown, $\overline{\text { SHDN }}=0 \mathrm{~V}$ $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C} \end{aligned}$ | $I_{\mathrm{IH}}$ <br> IIL |  | $\begin{gathered} 5.0 \\ 100 \\ \\ 5.0 \\ 100 \end{gathered}$ | - | pA |
| Wake-Up Time from Shutdown ( $\mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k}$ ) | twKUP | - | 1.2 | - | ms |

1. Maximum Package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.
$T_{J}=T_{A}+\left(P_{D} R_{\theta J A}\right)$
2. Capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ contribution is approximately $20 \%$ of the total output resistance.


Figure 2. Output Resistance vs. Supply Voltage


Figure 4. Output Current vs. Capacitance


Figure 6. Supply Current vs. Supply Voltage


Figure 3. Output Resistance vs. Ambient Temperature


Figure 5. Output Voltage Ripple vs. Capacitance


Figure 7. Oscillator Frequency vs. Ambient Temperature


Figure 8. Output Voltage vs. Output Current


TIME $=25 \mu \mathrm{~s} /$ Div.
Figure 10. Output Voltage Ripple and Noise


Figure 12. Supply Voltage vs. Shutdown Input Voltage Threshold


Figure 9. Power Conversion Efficiency vs. Output Current


Figure 11. Shutdown Supply Current vs. Ambient Temperature

Figure 13. Wakeup Time From Shutdown

## MAX1720



Figure 14. Test Setup/Voltage Inverter

## DETAILED OPERATING DESCRIPTION

The MAX1720 charge pump converter inverts the voltage applied to the $\mathrm{V}_{\text {in }}$ pin. Conversion consists of a two-phase operation (Figure 15). During the first phase, switches $S_{2}$ and $S_{4}$ are open and $S_{1}$ and $S_{3}$ are closed. During this time, $\mathrm{C}_{1}$ charges to the voltage on $\mathrm{V}_{\text {in }}$ and load current is supplied from $C_{2}$. During the second phase, $S_{2}$ and $S_{4}$ are closed, and $S_{1}$ and $S_{3}$ are open. This action connects $C_{1}$ across $C_{2}$, restoring charge to $\mathrm{C}_{2}$.


Figure 15. Ideal Switched Capacitor Charge Pump

## APPLICATIONS INFORMATION

## Output Voltage Considerations

The MAX1720 performs voltage conversion but does not provide regulation. The output voltage will drop in a linear manner with respect to load current. The value of this equivalent output resistance is approximately $26 \Omega$ nominal at $25^{\circ} \mathrm{C}$ with $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}$. $\mathrm{V}_{\text {out }}$ is approximately -5.0 V at light loads, and drops according to the equation below:

$$
\begin{gathered}
V_{D R O P}=I_{\text {out }} \times R_{\text {out }} \\
V_{\text {out }}=-\left(V_{\text {in }}-V_{\text {DROP }}\right)
\end{gathered}
$$

## Charge Pump Efficiency

The overall power conversion efficiency of the charge pump is affected by four factors:

1. Losses from power consumed by the internal oscillator, switch drive, etc. (which vary with input voltage, temperature and oscillator frequency).
2. I 2 R losses due to the on-resistance of the MOSFET switches on-board the charge pump.
3. Charge pump capacitor losses due to Equivalent Series Resistance (ESR).
4. Losses that occur during charge transfer from the commutation capacitor to the output capacitor when a voltage difference between the two capacitors exists.
Most of the conversion losses are due to factors 2, 3 and 4. These losses are given by Equation 1.

$$
\begin{gather*}
\mathrm{P}_{\text {LOSS }(2,3,4)}=\mathrm{I}_{\text {out }}^{2} \times \mathrm{R}_{\text {out }} \cong \mathrm{I}_{\text {out }}^{2} \times \\
{\left[\frac{1}{\left(\mathrm{f}_{\mathrm{OSC}}\right) \mathrm{C}_{1}}+8 \mathrm{R}_{\text {SWITCH }}+4 \mathrm{ESR}_{\mathrm{C}_{1}}+\mathrm{ESR}_{\mathrm{C}_{2}}\right]} \tag{eq.1}
\end{gather*}
$$

The $1 /\left(\mathrm{f}_{\mathrm{OSC}}\right)\left(\mathrm{C}_{1}\right)$ term in Equation 1 is the effective output resistance of an ideal switched capacitor circuit (Figures 16 and 17).

The losses due to charge transfer above are also shown in Equation 2. The output voltage ripple is given by Equation 3.

$$
\begin{align*}
\mathrm{P}_{\text {LOSS }} & =\left[0.5 \mathrm{C}_{1}\left(\mathrm{~V}_{\text {in }^{2}}-\mathrm{V}_{\text {out }}{ }^{2}\right)\right. \\
& \left.+0.5 \mathrm{C}_{2}\left(\mathrm{~V}_{\text {RIPPLE }}{ }^{2}-2 \mathrm{~V}_{\text {out }} \mathrm{V}_{\text {RIPPLE }}\right)\right] \times \mathrm{f}_{\text {OSC }} \tag{eq.2}
\end{align*}
$$

$V_{\text {RIPPLE }}=\frac{I_{\text {out }}}{\left(\mathrm{f}_{\mathrm{OSC}}\right)\left(\mathrm{C}_{2}\right)}+2\left(\mathrm{I}_{\text {out }}\right)\left(\mathrm{ESR}_{\mathrm{C}_{2}}\right)$


Figure 16. Ideal Switched Capacitor Model


Figure 17. Equivalent Output Resistance

## Capacitor Selection

In order to maintain the lowest output resistance and output ripple voltage, it is recommended that low ESR capacitors be used. Additionally, larger values of $\mathrm{C}_{1}$ will lower the output resistance and larger values of $\mathrm{C}_{2}$ will reduce output voltage ripple. (See Equation 3).

Table 1 shows various values of $\mathrm{C}_{1}, \mathrm{C}_{2}$ and $\mathrm{C}_{3}$ with the corresponding output resistance values at $25^{\circ} \mathrm{C}$. Table 2 shows the output voltage ripple for various values of $\mathrm{C}_{1}, \mathrm{C}_{2}$ and $\mathrm{C}_{3}$. The data in Tables 1 and 2 was measured not calculated.

Table 1. Output Resistance vs. Capacitance $\left(C_{1}=C_{2}=C_{3}\right), V_{\text {in }}=4.75 \mathrm{~V}$ and $\mathrm{V}_{\text {out }}=-4.0 \mathrm{~V}$

| $\mathbf{C}_{1}=\mathbf{C}_{\mathbf{2}}=\mathbf{C}_{\mathbf{3}}$ <br> $(\mu \mathrm{F})$ | $\mathbf{R}_{\text {out }}$ <br> $(\mathbf{\Omega})$ |
| :---: | :---: |
| 0.7 | 129.1 |
| 1.4 | 69.5 |
| 3.3 | 37.0 |
| 7.3 | 26.5 |
| 10 | 25.9 |
| 24 | 24.1 |
| 50 | 24 |

Table 2. Output Voltage Ripple vs. Capacitance $\left(C_{1}=C_{2}=C_{3}\right), V_{\text {in }}=4.75 \mathrm{~V}$ and $V_{\text {out }}=-4.0 \mathrm{~V}$

| $\mathbf{C}_{\mathbf{1}}=\mathbf{C}_{\mathbf{2}}=\mathbf{C}_{\mathbf{3}}$ <br> $(\mu \mathrm{F})$ | Output Voltage Ripple <br> $(\mathbf{m V})$ |
| :---: | :---: |
| 0.7 | 382 |
| 1.4 | 342 |
| 3.3 | 255 |
| 7.3 | 164 |
| 10 | 132 |
| 24 | 59 |
| 50 | 38 |

## Input Supply Bypassing

The input voltage, $\mathrm{V}_{\text {in }}$ should be capacitively bypassed to reduce AC impedance and minimize noise effects due to the
switching internals in the device. If the device is loaded from $V_{\text {out }}$ to GND, it is recommended that a large value capacitor (at least equal to $\mathrm{C}_{1}$ ) be connected from $\mathrm{V}_{\text {in }}$ to GND. If the device is loaded from $V_{\text {in }}$ to $V_{\text {out }}$, a small $(0.7 \mu \mathrm{~F})$ capacitor between the pins is sufficient.

## Voltage Inverter

The most common application for a charge pump is the voltage inverter (Figure 14). This application uses two or three external capacitors. The $\mathrm{C}_{1}$ (pump capacitor) and $\mathrm{C}_{2}$ (output capacitor) are required. The input bypass capacitor, $\mathrm{C}_{3}$, may be necessary depending on the application. The output is equal to $-\mathrm{V}_{\text {in }}$ plus any voltage drops due to loading. Refer to Tables 1 and 2 for capacitor selection. The test setup used for the majority of the characterization is shown in Figure 14.

## Layout Considerations

As with any switching power supply circuit, good layout practice is recommended. Mount components as close together as possible to minimize stray inductance and capacitance. Also, use a large ground plane to minimize noise leakage into other circuitry.

## Capacitor Resources

Selecting the proper type of capacitor can reduce switching loss. Low ESR capacitors are recommended. The MAX1720 was characterized using the capacitors listed in Table 3. This list identifies low ESR capacitors for the voltage inverter application.

Table 3. Capacitor Types

| Manufacturer/Contact | Part Types/Series |
| :--- | :---: |
| AVX | TPS |
| 843-448-9411 |  |
| www.avxcorp.com | ESRD |
| Cornell Dubilier |  |
| 508-996-8561 |  |
| www.cornell-dubilier.com | SN |
| Sanyo/Os-con | SVP |
| 619-661-6835 |  |
| www.sanyovideo.com/oscon.htm |  |
| Vishay | 593D |
| 603-224-1961 |  |
| www.vishay.com | 594 |



Figure 18. Voltage Inverter

The MAX1720 primary function is a voltage inverter. The device will convert 5.0 V into -5.0 V with light loads. Two capacitors are required for the inverter to function. A third capacitor, the input bypass capacitor, may be required depending on the power source for the inverter. The performance for this device is illustrated below.


Figure 19. Inverter Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 20. Cascaded Devices for Increased Negative Output Voltage

Two or more devices can be cascaded for increased output voltage. Under light load conditions, the output voltage is approximately equal to $-\mathrm{V}_{\text {in }}$ times the number of stages. The converter output resistance increases dramatically with each additional stage. This is due to a reduction of input voltage to each successive stage as the converter output is loaded. Note that the ground connection for each successive stage must connect to the negative output of the previous stage. The performance characteristics for a converter consisting of two cascaded devices are shown below.


| Curve | $\mathbf{V}_{\text {in }}(\mathbf{V})$ | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: |
| A | 5.0 | 140 |
| B | 3.0 | 174 |

Figure 21. Cascade Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 22. Negative Output Voltage Doubler
A single device can be used to construct a negative voltage doubler. The output voltage is approximately equal to $-2 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | All Diodes | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: |
| A | 3.0 | 1N4148 | 124 |
| B | 3.0 | MBRA120E | 115 |
| C | 5.0 | 1N4148 | 96 |
| D | 5.0 | MBRA120E | 94 |

Figure 23. Doubler Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 24. Negative Output Voltage Tripler

A single device can be used to construct a negative voltage tripler. The output voltage is approximately equal to $-3 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | All Diodes | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: |
| A | 3.0 | 1 N4148 | 267 |
| B | 3.0 | MBRA120E | 250 |
| C | 5.0 | 1N4148 | 205 |
| D | 5.0 | MBRA120E | 195 |

Figure 25. Tripler Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 26. Positive Output Voltage Doubler
A single device can be used to construct a positive voltage doubler. The output voltage is approximately equal to $2 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | All Diodes | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: |
| A | 3.0 | 1 N4148 | 32 |
| B | 3.0 | MBRA120E | 26 |
| C | 5.0 | 1N4148 | 26 |
| D | 5.0 | MBRA120E | 21 |

Figure 27. Doubler Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 28. Positive Output Voltage Tripler
A single device can be used to construct a positive voltage tripler. The output voltage is approximately equal to $3 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | All Diodes | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: |
| A | 3.0 | 1N4148 | 111 |
| B | 3.0 | MBRA120E | 97 |
| C | 5.0 | 1N4148 | 85 |
| D | 5.0 | MBRA120E | 75 |

Figure 29. Tripler Load Regulation, Output Voltage vs. Output Current


Figure 30. Load Regulated Negative Output Voltage

A zener diode can be used with the shutdown input to provide closed loop regulation performance. This significantly reduces the converter's output resistance and dramatically enhances the load regulation. For closed loop operation, the desired regulated output voltage must be lower in magnitude than $-\mathrm{V}_{\mathrm{in}}$. The output will regulate at a level of $-\mathrm{V}_{\mathrm{Z}}+\mathrm{V}_{\mathrm{th}(\overline{\mathrm{SHDN}})}$. Note that the shutdown input voltage threshold is typically $0.5 \mathrm{~V}_{\mathrm{in}}$ and therefore, the regulated output voltage will change proportional to the converter's input. This characteristic will not present a problem when used in applications with constant input voltage. In this case the zener breakdown was measured at $25 \mu \mathrm{~A}$. The performance characteristics for the above converter are shown below. Note that the dashed curve sections represent the converter's open loop performance.


| Curve | $\mathrm{V}_{\text {in }}(\mathrm{V})$ | $\mathrm{V}_{\mathbf{z}}(\mathrm{V})$ | $\mathrm{V}_{\text {out }}(\mathrm{V})$ |
| :---: | :---: | :---: | :---: |
| A | 3.3 V | 4.5 | -2.8 |
| B | 5.0 V | 6.5 | -3.8 |

Figure 31. Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 32. Line and Load Regulated Negative Output Voltage

An adjustable shunt regulator can be used with the shutdown input to give excellent closed loop regulation performance. The shunt regulator acts as a comparator with a precise input offset voltage which significantly reduces the converter's output resistance and dramatically enhances the line and load regulation. For closed loop operation, the desired regulated output voltage must be lower in magnitude than $-\mathrm{V}_{\mathrm{in}}$. The output will regulate at a level of $-\mathrm{V}_{\text {ref }}\left(\mathrm{R}_{2} / \mathrm{R}_{1}+1\right)$. The adjustable shunt regulator can be from either the TLV431 or TL431 families. The comparator offset or reference voltage is 1.25 V or 2.5 V respectively. The performance characteristics for the converter are shown below. Note that the dashed curve sections represent the converter's open loop performance.


Figure 33. Load Regulation, Output Voltage vs. Output Current


Figure 34. Line Regulation, Output Voltage vs. Input Current

| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | $\mathbf{R}_{\mathbf{1}}(\Omega)$ | $\mathbf{R}_{\mathbf{2}}(\Omega)$ | $\mathbf{V}_{\text {out }}(\mathrm{V})$ |
| :---: | :---: | :---: | :---: | :---: |
| A | 3.0 | 10 k | 5.0 k | -1.8 |
| B | 5.0 | 10 k | 20 k | -3.6 |

## MAX1720



Figure 35. Paralleling Devices for Increased Negative Output Current
An increase in converter output current capability with a reduction in output resistance can be obtained by paralleling two or more devices. The output current capability is approximately equal to the number of devices paralleled. A single shared output capacitor is sufficient for proper operation but each device does require it's own pump capacitor. Note that the output ripple frequency will be complex since the oscillators are not synchronized. The performance characteristics for a converter consisting of two paralleled devices is shown below.


| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: |
| $A$ | 5.0 | 14.5 |
| $B$ | 3.0 | 17 |

Figure 36. Parallel Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 37. External Switch for Increased Negative Output Current

The output current capability of the MAX1720 can be extended beyond 600 mA with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $-\mathrm{V}_{\text {in }}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter are shown below. Note that the output resistance is reduced to 0.9 ohms.


Figure 38. Current Boosted Load Regulation, Output Voltage vs. Output Current


Figure 39. Line and Load Regulated Negative Output Voltage with High Current Capability

This converter is a combination of Figures 37 and 32. It provides a line and load regulated output of -2.36 V at up to 450 mA with an input voltage of 5.0 V . The output will regulate at a level of $-\mathrm{V}_{\text {ref }}\left(\mathrm{R}_{2} / \mathrm{R}_{1}+1\right)$. The performance characteristics are shown below. Note, the dashed line is the open loop and the solid line is the closed loop performance.


Figure 40. Current Boosted Load Regulation, Output Voltage vs. Output Current


Figure 41. Current Boosted Line Regulation, Output Voltage vs. Input Voltage

## MAX1720



Figure 42. Positive Output Voltage Doubler with High Current Capability
The MAX1720 can be configured to produce a positive output voltage doubler with current capability in excess of 500 mA . This is accomplished with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $2 \mathrm{~V}_{\text {in }}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter is shown below. Note that the output resistance is reduced to 1.9 ohms.


Figure 43. Positive Doubler with Current Boosted Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 44. Line and Load Regulated Positive Output Voltage Doubler with High Current Capability
This converter is a combination of Figures 42 and the shunt regulator to close the loop. In this case the anode of the regulator is connected to ground. This convert provides a line and load regulated output of 7.6 V at up to 300 mA with an input voltage of 5.0 V . The output will regulate at a level of $\mathrm{V}_{\text {ref }}\left(\mathrm{R}_{2} / \mathrm{R}_{1}+1\right)$. The open loop configuration is the dashed line and the closed loop is the solid line. The performance characteristics are shown below.


Figure 45. Current Boosted Close Loop Load Regulation, Output Voltage vs. Output Current


Figure 46. Current Boosted Close Loop Line Regulation, Output Voltage vs. Input Voltage

## MAX1720



Figure 47. Negative Input Voltage Splitter

A single device can be used to split a negative input voltage. The output voltage is approximately equal to $-\mathrm{V}_{\text {in }} / 2$. The performance characteristics are shown below. Note that the converter has an output resistance of 10 ohms.


Figure 48. Negative Voltage Splitter Load Regulation, Output Voltage vs. Output Current

## MAX1720



Figure 49. Combination of a Closed Loop Negative Inverter with a Positive Output Voltage Doubler

All of the previously shown converter circuits have only single outputs. Applications requiring multiple outputs can be constructed by incorporating combinations of the former circuits. The converter shown above combines Figures 26 and 32 to form a regulated negative output inverter with a non-regulated positive output doubler. The magnitude of $-\mathrm{V}_{\text {out }}$ is controlled by the resistor values and follows the relationship $-V_{\text {ref }}\left(R_{2} / R_{1}+1\right)$. Since the positive output is not within the feedback loop, its output voltage will increase as the negative output load increases. This cross regulation characteristic is shown in the upper portion of Figure 50. The dashed line is the open loop and the solid line is the closed loop configuration for the load regulation. The load regulation for the positive doubler with a constant load on the $-\mathrm{V}_{\text {out }}$ is shown in Figure 51.


Figure 50. Load Regulation, Output Voltage vs. Output Current


Figure 51. Load Regulation, Output Voltage vs. Output Current

## MAX1720



Inverter Size $=0.5$ in $\times 0.2$ in Area $=0.10 \mathrm{in}^{2}, 64.5 \mathrm{~mm}^{2}$

Figure 52. Inverter Circuit Board Layout, Top View Copper Side

## TAPING FORM

Component Taping Orientation for TSOP-6 Devices


Tape \& Reel Specifications Table

| Package | Tape Width (W) | Pitch (P) | Part Per Full Reel | Diameter |
| :---: | :---: | :---: | :---: | :---: |
| TSOP-6 | 8 mm | 4 mm | 3000 | 7 inches |

## MAX828, MAX829

## Switched Capacitor Voltage Converter

The MAX828 and MAX829 are CMOS charge pump voltage inverters that are designed for operation over an input voltage range of 1.15 V to 5.5 V with an output current capability in excess of 50 mA . The operating current consumption is only $68 \mu \mathrm{~A}$ for the MAX828 and $118 \mu \mathrm{~A}$ for the MAX829. The devices contain an internal oscillator that operates at 12 kHz for the MAX828 and 35 kHz for the MAX829. The oscillator drives four low resistance MOSFET switches, yielding a low output resistance of $26 \Omega$ and a voltage conversion efficiency of $99.9 \%$. These devices require only two external capacitors, $10 \mu \mathrm{~F}$ for the MAX828 and $3.3 \mu \mathrm{~F}$ for the MAX829, for a complete inverter making it an ideal solution for numerous battery powered and board level applications. The MAX828 and MAX829 are available in the space saving Thin SOT-23-5 package.

## Features

- Operating Voltage Range of 1.15 V to 5.5 V
- Output Current Capability in Excess of 50 mA
- Low Current Consumption of $68 \mu \mathrm{~A}$ (MAX828) or $118 \mu \mathrm{~A}$ (MAX829)
- Operation at 12 kHz (MAX828) or 35 kHz (MAX829)
- Low Output Resistance of $26 \Omega$
- Space Saving Thin SOT-23-5 Package


## Typical Applications

- LCD Panel Bias
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand Held Instruments


This device contains 77 active transistors.

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONFIGURATION


Thin SOT-23-5*
(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MAX828EUK | Thin <br> SOT-23-5 | 3000 Tape/Reel |
| MAX829EUK | Thin <br> SOT-23-5 | 3000 Tape/Reel |

## MAX828, MAX829

MAXIMUM RATINGS*

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage Range ( $\mathrm{V}_{\text {in }}$ to GND) | $\mathrm{V}_{\text {in }}$ | -0.3 to 6.0 | V |
| Output Voltage Range (Vout to GND) | $V_{\text {out }}$ | -6.0 to 0.3 | V |
| Output Current (Note 1) | $\mathrm{I}_{\text {out }}$ | 100 | mA |
| Output Short Circuit Duration (V out $^{\text {to }}$ GND, Note 1) | tsc | Indefinite | sec |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation and Thermal Characteristics Thermal Resistance, Junction to Air Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ | $\begin{gathered} \mathrm{R}_{\theta \mathrm{BA}} \\ \mathrm{P}_{\mathrm{D}} \end{gathered}$ | $\begin{aligned} & 256 \\ & 313 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ mW |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |

*ESD Ratings
ESD Machine Model Protection up to 200 V, Class B
ESD Human Body Model Protection up to 2000 V, Class 2
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right.$ for MAX828 $\mathrm{C}_{1}=\mathrm{C}_{2}=10 \mu \mathrm{~F}$, for MAX829 $\mathrm{C}_{1}=\mathrm{C}_{2}=3.3 \mu \mathrm{~F}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$, typical values shown are for $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted. See Figure 20 for test setup.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Supply Voltage Range ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ ) | $V_{\text {in }}$ | 1.5 to 5.5 | 1.15 to 6.0 | - | V |
| Supply Current Device Operating ( $\mathrm{R}_{\mathrm{L}}=\infty$ ) $\begin{array}{r} \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \text { MAX828 } \\ \text { MAX829 } \\ \mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C} \\ \text { MAX828 } \\ \text { MAX829 } \end{array}$ | $\mathrm{lin}^{\text {n }}$ |  | $\begin{gathered} 68 \\ 118 \\ \\ 73 \\ 128 \end{gathered}$ | $\begin{gathered} 90 \\ 200 \\ \\ 100 \\ 200 \end{gathered}$ | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Oscillator Frequency } \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \text { MAX828 } \\ & \text { MAX829 } \\ & \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\ & \text { MAX828 } \\ & \text { MAX829 } \end{aligned}$ | fosc | $\begin{gathered} 8.4 \\ 24.5 \\ 6.0 \\ 19 \end{gathered}$ | $\begin{aligned} & 12 \\ & 35 \\ & - \end{aligned}$ | $\begin{gathered} 15.6 \\ 45.6 \\ 21 \\ 54 \end{gathered}$ | kHz |
| $\begin{aligned} & \text { Output Resistance ( } \left.\mathrm{l}_{\text {out }}=25 \mathrm{~mA} \text {, Note } 2\right) \\ & \text { MAX828 } \\ & \text { MAX829 } \end{aligned}$ | $\mathrm{R}_{\text {out }}$ | - | $\begin{aligned} & 26 \\ & 26 \end{aligned}$ | $\begin{aligned} & 50 \\ & 50 \end{aligned}$ | $\Omega$ |
| Voltage Conversion Efficiency ( $\mathrm{R}_{\mathrm{L}}=\infty$ ) | $\mathrm{V}_{\text {EFF }}$ | 99 | 99.9 | - | \% |
| Power Conversion Efficiency ( $\mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k}$ ) | $\mathrm{P}_{\text {EFF }}$ | - | 96 | - | \% |

1. Maximum Package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded. $T_{J}=T_{A}+\left(P_{D} R_{\theta J A}\right)$
2. Capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ contribution is approximately $20 \%$ of the total output resistance.


Figure 2. Output Resistance vs. Supply Voltage MAX828


Figure 4. Output Resistance vs. Ambient Temperature MAX828


Figure 6. Output Current vs. Capacitance MAX828


Figure 3. Output Resistance vs. Supply Voltage MAX829


Figure 5. Output Resistance vs. Ambient Temperature MAX829


Figure 7. Output Current vs. Capacitance MAX829


Figure 8. Output Voltage Ripple vs. Capacitance MAX828


Figure 10. Supply Current vs. Supply Voltage MAX828


Figure 12. Oscillator Frequency vs. Ambient Temperature MAX828


Figure 9. Output Voltage Ripple vs. Capacitance MAX829


Figure 11. Supply Current vs. Supply Voltage MAX829


Figure 13. Oscillator Frequency vs. Ambient Temperature MAX829


Figure 14. Output Voltage vs. Output Current MAX828


Figure 16. Power Conversion Efficiency vs.
OUTPUT VOLTAGE RIPPLE \& NOISE $=10 \mathrm{mV} / \mathrm{Div}$.


Figure 18. Output Voltage Ripple and Noise MAX828


Figure 15. Output Voltage vs. Output Current MAX829


Figure 17. Power Conversion Efficiency vs. Output Current MAX829
 AC COUPLED


TIME $=10 \mu \mathrm{~s} / \mathrm{div}$
Figure 19. Output Voltage Ripple and Noise MAX829


Figure 20. Test Setup/Voltage Inverter

## DETAILED OPERATING DESCRIPTION

The MAX828/829 charge pump converters inverts the voltage applied to the $\mathrm{V}_{\text {in }}$ pin. Conversion consists of a two-phase operation (Figure 21). During the first phase, switches $S_{2}$ and $S_{4}$ are open and $S_{1}$ and $S_{3}$ are closed. During this time, $\mathrm{C}_{1}$ charges to the voltage on $\mathrm{V}_{\text {in }}$ and load current is supplied from $C_{2}$. During the second phase, $S_{2}$ and $S_{4}$ are closed, and $S_{1}$ and $S_{3}$ are open. This action connects $C_{1}$ across $C_{2}$, restoring charge to $C_{2}$.


Figure 21. Ideal Switched Capacitor Charge Pump

## APPLICATIONS INFORMATION

## Output Voltage Considerations

The MAX828/829 performs voltage conversion but does not provide regulation. The output voltage will drop in a linear manner with respect to load current. The value of this equivalent output resistance is approximately $26 \Omega$ nominal at $25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}$. $\mathrm{V}_{\text {out }}$ is approximately -5.0 V at light loads, and drops according to the equation below:

$$
\begin{gathered}
V_{\text {DROP }}=I_{\text {out }} \times R_{\text {out }} \\
V_{\text {out }}=-\left(V_{\text {in }}-V_{\text {DROP }}\right)
\end{gathered}
$$

## Charge Pump Efficiency

The overall power efficiency of the charge pump is affected by four factors:

1. Losses from power consumed by the internal oscillator, switch drive, etc. (which vary with input voltage, temperature and oscillator frequency).
2. I ${ }^{2}$ R losses due to the on-resistance of the MOSFET switches on-board the charge pump.
3. Charge pump capacitor losses due to Equivalent Series Resistance (ESR).
4. Losses that occur during charge transfer from the commutation capacitor to the output capacitor when a voltage difference between the two capacitors exists.
Most of the conversion losses are due to factors 2, 3 and 4. These losses are given by Equation 1.

$$
\begin{gather*}
\mathrm{P}_{\text {LOSS }(2,3,4)}=\mathrm{I}_{\text {out }}^{2} \times \mathrm{R}_{\text {out }} \cong \mathrm{I}_{\text {out }}{ }^{2} \times \\
{\left[\frac{1}{\left(\mathrm{f}_{\mathrm{OSC}}\right) \mathrm{C}_{1}}+8 \mathrm{R}_{\text {SWITCH }}+4 \mathrm{ESR}_{\mathrm{C}_{1}}+\mathrm{ESR}_{\mathrm{C}_{2}}\right]} \tag{eq.1}
\end{gather*}
$$

The $1 /\left(\mathrm{f}_{\mathrm{OSC}}\right)\left(\mathrm{C}_{1}\right)$ term in Equation 1 is the effective output resistance of an ideal switched capacitor circuit (Figures 22 and 23).

The losses due to charge transfer above are also shown in Equation 2. The output voltage ripple is given by Equation 3.

$$
\begin{align*}
\mathrm{P}_{\text {LOSS }} & =\left[0.5 \mathrm{C}_{1}\left(\mathrm{~V}_{\text {in }^{2}}-\mathrm{V}_{\text {out }}{ }^{2}\right)\right. \\
& \left.+0.5 \mathrm{C}_{2}\left(\mathrm{~V}_{\text {RIPPLE }}{ }^{2}-2 \mathrm{~V}_{\text {out }} \mathrm{V}_{\text {RIPPLE }}\right)\right] \times \mathrm{f} \text { OSC } \tag{eq.2}
\end{align*}
$$

$\mathrm{V}_{\text {RIPPLE }}=\frac{\mathrm{I}_{\text {out }}}{\left(\mathrm{f}_{\mathrm{OSC}}\right)\left(\mathrm{C}_{2}\right)}+2\left(\mathrm{I}_{\text {out }}\right)\left(\mathrm{ESR}_{\mathrm{C}_{2}}\right)$


Figure 22. Ideal Switched Capacitor Model


Figure 23. Equivalent Output Resistance

## Capacitor Selection

In order to maintain the lowest output resistance and output ripple voltage, it is recommended that low ESR capacitors be used. Additionally, larger values of $\mathrm{C}_{1}$ will lower the output resistance and larger values of $\mathrm{C}_{2}$ will reduce output voltage ripple. (See Equation 3).

Table 1 shows various values of $\mathrm{C}_{1}, \mathrm{C}_{2}$ and $\mathrm{C}_{3}$ with the corresponding output resistance values at $25^{\circ} \mathrm{C}$. Table 2 shows the output voltage ripple for various values of $\mathrm{C}_{1}, \mathrm{C}_{2}$ and $\mathrm{C}_{3}$. The data in Tables 1 and 2 was measured not calculated.

Table 1. Output Resistance vs. Capacitance $\left(C_{1}=C_{2}=C_{3}\right), V_{\text {in }}=4.75 \mathrm{~V}$ and $\mathrm{V}_{\text {out }}=-4.0 \mathrm{~V}$

| $\mathbf{C}_{\mathbf{1}}=\mathbf{C}_{\mathbf{2}}=\mathbf{C}_{\mathbf{3}}$ | $\mathbf{M A X} \mathbf{F})$ <br> $(\boldsymbol{\Omega})$ | $\mathbf{M A X 8 2 9}$ <br> $(\boldsymbol{\Omega})$ |
| :---: | :---: | :---: |
| 0.7 | 127.2 | 55.7 |
| 1.4 | 67.7 | 36.8 |
| 3.3 | 36 | 26.0 |
| 7.3 | 26.7 | 24.9 |
| 10 | 25.9 | 25.1 |
| 24 | 24.3 | 25.2 |
| 50 | 24 | 24 |

Table 2. Output Voltage Ripple vs. Capacitance $\left(C_{1}=C_{2}=C_{3}\right), V_{\text {in }}=4.75 \mathrm{~V}$ and $V_{\text {out }}=-4.0 \mathrm{~V}$

| $\mathbf{C}_{\mathbf{1}}=\mathbf{C}_{\mathbf{2}}=\mathbf{C}_{\mathbf{3}}$ <br> $(\mu \mathbf{F})$ | MAX828 Ripple <br> $(\mathbf{m V})$ | MAX829 Ripple <br> $(\mathbf{m V})$ |
| :---: | :---: | :---: |
| 0.7 | 377.5 | 320 |
| 1.4 | 360.5 | 234 |
| 3.3 | 262 | 121 |
| 7.3 | 155 | 62.1 |
| 10 | 126 | 51.25 |
| 24 | 55.1 | 25.2 |
| 50 | 36.6 | 27.85 |

## Input Supply Bypassing

The input voltage, $\mathrm{V}_{\text {in }}$ should be capacitively bypassed to reduce AC impedance and minimize noise effects due to the switching internals in the device. If the device is loaded from $V_{\text {out }}$ to GND, it is recommended that a large value capacitor (at least equal to $\mathrm{C}_{1}$ ) be connected from $\mathrm{V}_{\text {in }}$ to GND. If the device is loaded from $\mathrm{V}_{\text {in }}$ to $\mathrm{V}_{\text {out }}$ a small $(0.7 \mu \mathrm{~F})$ capacitor between the pins is sufficient.

## Voltage Inverter

The most common application for a charge pump is the voltage inverter (Figure 20). This application uses two or three external capacitors. The capacitors $\mathrm{C}_{1}$ (pump capacitor) and $\mathrm{C}_{2}$ (output capacitor) are required. The input bypass capacitor $\mathrm{C}_{3}$, may be necessary depending on the application. The output is equal to $-\mathrm{V}_{\text {in }}$ plus any voltage drops due to loading. Refer to Tables 1 and 2 for capacitor selection. The test setup used for the majority of the characterization is shown in Figure 20.

## Layout Considerations

As with any switching power supply circuit, good layout practice is recommended. Mount components as close together as possible to minimize stray inductance and capacitance. Also use a large ground plane to minimize noise leakage into other circuitry.

## Capacitor Resources

Selecting the proper type of capacitor can reduce switching loss. Low ESR capacitors are recommended. The MAX828 and MAX829 were characterized using the capacitors listed in Table 3. This list identifies low ESR capacitors for the voltage inverter application.

Table 3. Capacitor Types

| Manufacturer/Contact | Part Types/Series |
| :--- | :---: |
| AVX | TPS |
| 843-448-9411 |  |
| www.avxcorp.com |  |
| Cornell Dubilier |  |
| 508-996-8561 |  |
| www.cornell-dubilier.com | ESRD |
| Sanyo/Os-con |  |
| 619-661-6835 |  |
| www.sanyovideo.com/oscon.htm | SN |
| Vishay |  |
| 603-224-1961 |  |
| www.vishay.com | $593 D$ |



MAX828: Capacitors $=10 \mu \mathrm{~F}$
MAX829: Capacitors $=3.3 \mu \mathrm{~F}$
Figure 24. Voltage Inverter

The MAX828 / 829 primary function is a voltage inverter. The device will convert 5.0 V into -5.0 V with light loads. Two capacitors are required for the inverter to function. A third capacitor, the input bypass capacitor, may be required depending on the power source for the inverter. The performance for this device is illustrated below.


Figure 25. Voltage Inverter Load Regulation Output Voltage vs. Output Current MAX828


Figure 26. Voltage Inverter Load Regulation Output Voltage vs. Output Current MAX829

## MAX828, MAX829



Figure 27. Cascade Devices for Increased Negative Output Voltage

Two or more devices can be cascaded for increased output voltage. Under light load conditions, the output voltage is approximately equal to $-\mathrm{V}_{\text {in }}$ times the number of stages. The converter output resistance increases dramatically with each additional stage. This is due to a reduction of input voltage to each successive stage as the converter output is loaded. Note that the ground connection for each successive stage must connect to the negative output of the previous stage. The performance characteristics for a converter consisting of two cascaded devices are shown below.


Figure 28. Cascade Load Regulation, Output Voltage vs. Output Current MAX828


Figure 29. Cascade Load Regulation, Output Voltage vs. Output Current MAX829

| Curve | $\mathrm{V}_{\text {in }}(\mathrm{V})$ | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: |
| A | 3.0 | 173 |
| B | 5.0 | 141 |
| C | 3.0 | 179 |
| D | 5.0 | 147 |

## MAX828, MAX829



Figure 30. Negative Output Voltage Doubler
A single device can be used to construct a negative voltage doubler. The output voltage is approximately equal to $-2 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


Figure 31. Doubler Load Regulation, Output Voltage vs. Output Current MAX828


Figure 32. Doubler Load Regulation, Output Voltage vs. Output Current MAX829

| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | Diodes | MAX828 <br> $\mathbf{R}_{\text {out }}(\Omega)$ | MAX829 <br> $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: | :---: |
| A | 3.0 | 1 N4148 | 122 | 118 |
| B | 3.0 | MBRA120E | 114 | 106 |
| C | 5.0 | 1N4148 | 96 | 90 |
| D | 5.0 | MBRA120E | 91 | 87 |

## MAX828, MAX829



Figure 33. Negative Output Voltage Tripler

A single device can be used to construct a negative voltage tripler. The output voltage is approximately equal to $-3 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


Figure 34. Tripler Load Regulation, Output Voltage vs. Output Current MAX828


Figure 35. Tripler Load Regulation, Output Voltage vs. Output Current MAX829

| Curve | $\mathbf{V}_{\text {in }}(\mathrm{V})$ | Diodes | MAX828 <br> $\mathbf{R}_{\text {out }}(\Omega)$ | MAX829 <br> $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: | :---: |
| A | 3.0 | 1 N4148 | 259 | 246 |
| B | 3.0 | MBRA120E | 251 | 237 |
| C | 5.0 | 1N4148 | 209 | 198 |
| D | 5.0 | MBRA120E | 192 | 185 |



Figure 36. Positive Output Voltage Doubler

A single device can be used to construct a positive voltage doubler. The output voltage is approximately equal to $2 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


Figure 37. Doubler Load Regulation, Output Voltage vs. Output Current MAX828


Figure 38. Doubler Load Regulation, Output Voltage vs. Output Current MAX829

| Curve | $\mathbf{V}_{\mathbf{i n}}(\mathrm{V})$ | Diodes | $\mathbf{M A X 8 2 8}^{\mathbf{R}_{\text {out }}(\Omega)}$ | MAX829 <br> $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: | :---: |
| A | 3.0 | 1 N4148 | 32.5 | 32.2 |
| B | 3.0 | MBRA120E | 27.1 | 25.7 |
| C | 5.0 | 1N4148 | 26.0 | 25.1 |
| D | 5.0 | MBRA120E | 21.2 | 19.0 |

## MAX828, MAX829



Figure 39. Positive Output Voltage Tripler

A single device can be used to construct a positive voltage tripler. The output voltage is approximately equal to $3 \mathrm{~V}_{\text {in }}$ minus the forward voltage drop of each external diode. The performance characteristics for the above converter are shown below. Note that curves A and C show the circuit performance with economical 1N4148 diodes, while curves B and D are with lower loss MBRA120E Schottky diodes.


Figure 40. Tripler Load Regulation, Output Voltage vs. Output Current MAX828


Figure 41. Tripler Load Regulation, Output Voltage vs. Output Current MAX829

| Curve | $\mathbf{V}_{\text {in }}(\mathbf{V})$ | Diodes | MAX828 <br> $\mathbf{R}_{\text {out }}(\Omega)$ | MAX829 <br> $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: | :---: | :---: |
| A | 3.0 | 1 N4148 | 110 | 111 |
| B | 3.0 | MBRA120E | 96.5 | 96.7 |
| C | 5.0 | 1N4148 | 84.5 | 87.3 |
| D | 5.0 | MBRA120E | 78.2 | 77.1 |



Figure 42. Paralleling Devices for Increased Negative Output Current

An increase in converter output current capability with a reduction in output resistance can be obtained by paralleling two or more devices. The output current capability is approximately equal to the number of devices paralleled. A single shared output capacitor is sufficient for proper operation but each device does require it's own pump capacitor. Note that the output ripple frequency will be complex since the oscillators are not synchronized. The output resistance is approximately equal to the output resistance of one device divided by the total number of devices paralleled. The performance characteristics for a converter consisting of two paralleled devices is shown below.


Figure 43. Parallel Load Regulation, Output Voltage vs. Output Current MAX828


Figure 44. Parallel Load Regulation, Output Voltage vs. Output Current MAX829

| Curve | $\mathbf{V}_{\text {in }}(\mathbf{V})$ | $\mathbf{R}_{\text {out }}(\Omega)$ |
| :---: | :---: | :---: |
| A | 5.0 | 13.3 |
| B | 3.0 | 17.3 |
| C | 5.0 | 14.4 |
| D | 3.0 | 17.3 |



Figure 45. External Switch for Increased Negative Output Current

The output current capability of the MAX828 and MAX829 can be extended beyond 600 mA with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $-\mathrm{V}_{\mathrm{in}}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter are shown below. Note that the output resistance is reduced to 0.9 and 1.0 ohms for the 828 and 829 respectively.


Figure 46. Current Boosted Load Regulation, Output Voltage vs. Output Current MAX828


Figure 47. Current Boosted Load Regulation, Output Voltage vs. Output Current MAX829


Figure 48. Positive Output Voltage Doubler with High Current Capability

The MAX828 / 829 can be configured to produce a positive output voltage doubler with current capability in excess of 500 mA . This is accomplished with the addition of two external switch transistors and two Schottky diodes. The output voltage is approximately equal to $2 \mathrm{~V}_{\text {in }}$ minus the sum of the base emitter drops of both transistors and the forward voltage of both diodes. The performance characteristics for the converter are shown below. Note that the output resistance is reduced to 1.8 ohms.


Figure 49. Positive Doubler with Current Boosted Load Regulation, Output Voltage vs. Output Current, MAX828


Figure 50. Positive Doubler with Current Boosted Load Regulation, Output Voltage vs. Output Current, MAX829


Figure 51. A Positive Doubler, with a Negative Inverter
All of the previously shown converter circuits have only single outputs. Applications requiring multiple outputs can be constructed by incorporating combinations of the former circuits. The converter shown above combines Figures 24 and 36 to form a negative output inverter with a positive output doubler. Different combinations of load regulation are shown below. In Figures 52 and 53 the positive doubler has a constant $\mathrm{I}_{\mathrm{out}}=15 \mathrm{~mA}$ while the negative inverter has the variable load. In Figures 54 and 55 the negative inverter has the constant $\mathrm{I}_{\mathrm{out}}=15 \mathrm{~mA}$ and the positive doubler has the variable load.


Figure 52. Negative Inverter Load Regulation, Output Voltage vs. Output Current, MAX828


Figure 54. Positive Doubler Load Regulation, Output Voltage vs. Output Current, MAX828


Figure 53. Negative Inverter Load Regulation, Output Voltage vs. Output Current, MAX829


Figure 55. Positive Doubler Load Regulation, Output Voltage vs. Output Current, MAX829


Figure 56. Inverter Circuit Board Layout, Top View Copper Side

## TAPING FORM

## Component Taping Orientation for Thin SOT-23-5 Devices



Tape \& Reel Specifications Table

| Package | Tape Width (W) | Pitch (P) | Part Per Full Reel | Diameter |
| :---: | :---: | :---: | :---: | :---: |
| Thin SOT-23-5 | 8 mm | 4 mm | 3000 | 7 inches |

## CS5150H

## CPU 4-Bit Synchronous Buck Controller

The CS5150H is a 4-bit synchronous dual N -Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5150H is designed to operate over a $4.25-20 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V or 12 V as the main supply for conversion.

The CS5150H is specifically designed to power Pentium ${ }^{\circledR}$ Pro processors and other high performance core logic. It includes the following features: on board, 4-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5150H is upward compatible with the 5-bit CS5155H, allowing the mother board designer the capability of using either the CS5150H or the CS5155H with no change in layout. The CS5150H is available in 16 pin surface mount.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 4-Bit DAC
- Upward Compatible with 5-Bit CS5155H/CS5156H
- 30 ns Gate Rise/Fall Times
- $1.0 \%$ DAC Accuracy
- 5.0 V \& 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- 25 ns FET Nonoverlap Time
- Adaptive Voltage Positioning
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Current Sharing
- Overvoltage Protection


PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5150HGD16 | SO-16 | 48 Units/Rail |
| CS5150HGDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, Switching Power Supply for Core Logic - Pentium ${ }^{\circledR}$ Pro Processor

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :--- | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ | Reflow: (SMD styles only) (Note 1$)$ | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $25 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $20 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $V_{F B}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\text {OFF }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $V_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {ID } 0}-\mathrm{V}_{\text {ID }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {GATE(H) }}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\text {GATE(L) }}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.3 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Open Loop Gain | $1.25 \mathrm{~V}<\mathrm{V}_{\mathrm{COMP}}<4.0 \mathrm{~V} ; \mathrm{Note} 2$ | 50 | 60 | - | dB |
| Unity Gain Bandwidth | Note 2 | 500 | 3000 | - | kHz |
| COMP SINK Current | $\mathrm{V}_{\mathrm{COMP}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}>2.0 \mathrm{~V}$ | 0.4 | 2.5 | 8.0 | mA |
| COMP SOURCE Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 30 | 50 | 80 | $\mu \mathrm{~A}$ |
| COMP CLAMP Current | $\mathrm{V}_{\mathrm{COMP}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 4.0 | 4.3 | 5.0 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}$ | - | 160 | 600 | mV |
| PSRR | $8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} @ 1.0 \mathrm{kHz} ;$ Note 2 | 60 | 85 | - | dB |

$\mathrm{V}_{\mathrm{CC} 1}$ Monitor

| Start Threshold | Output switching | 3.75 | 3.90 | 4.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 3.70 | 3.85 | 4.00 | V |
| Hysteresis | Start-Stop | - | 50 | - | mV |

DAC

| Input Threshold |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID2 }}, \mathrm{V}_{\text {ID }}$ | 1.00 | 1.25 | 2.40 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Pull Up Resistance |  |  |  | $\mathrm{V}_{\mathrm{ID} 0}, \mathrm{~V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID } 2}, \mathrm{~V}_{\text {ID }}$ | 25 | 50 | 110 | k $\Omega$ |
| Pull Up Voltage |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy (all codes except 11111) |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}, 25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ | - | - | 1.0 | \% |
| VID3 | $V_{\text {ID2 }}$ | VID1 | VIDO |  |  |  |  |  |
| 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 0 | - | 2.1186 | 2.1400 | 2.1614 | V |
| 1 | 1 | 0 | 1 | - | 2.2176 | 2.2400 | 2.2624 | V |
| 1 | 1 | 0 | 0 | - | 2.3166 | 2.3400 | 2.3634 | V |
| 1 | 0 | 1 | 1 | - | 2.4156 | 2.4400 | 2.4644 | V |
| 1 | 0 | 1 | 0 | - | 2.5146 | 2.5400 | 2.5654 | V |
| 1 | 0 | 0 | 1 | - | 2.6136 | 2.6400 | 2.6664 | V |
| 1 | 0 | 0 | 0 | - | 2.7126 | 2.7400 | 2.7674 | V |
| 0 | 1 | 1 | 1 | - | 2.8116 | 2.8400 | 2.8684 | V |
| 0 | 1 | 1 | 0 | - | 2.9106 | 2.9400 | 2.9694 | V |
| 0 | 1 | 0 | 1 | - | 3.0096 | 3.0400 | 3.0704 | V |
| 0 | 1 | 0 | 0 | - | 3.1086 | 3.1400 | 3.1714 | V |
| 0 | 0 | 1 | 1 | - | 3.2076 | 3.2400 | 3.2724 | V |
| 0 | 0 | 1 | 0 | - | 3.3066 | 3.3400 | 3.3734 | V |
| 0 | 0 | 0 | 1 | - | 3.4056 | 3.4400 | 3.4744 | V |
| 0 | 0 | 0 | 0 | - | 3.5046 | 3.5400 | 3.5754 | V |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V}\right.$;
$5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}$; DAC Code: $\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\text {GATE(L) }}$ |  |  |  |  |  |
| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1}-\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} ; \mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}}(\mathrm{H})$ | - | 1.2 | 2.0 | V |
| Out SINK Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}-\mathrm{V}_{\text {PGND }} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}-\mathrm{V}_{\text {PGND }}$ | - | 1.0 | 1.5 | V |
| Out Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; \\ & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}<9.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \\ & \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; \\ & 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}>1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \\ & \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Shoot-Through Current | Note 3 | - | - | 50 | mA |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\text {GATE(L) }}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to $2.0 \mathrm{~V}_{\text {; }} \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ <br> $V_{G A T E(L)}$ rising to 2.0 V | - | 25 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to $2.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ <br> $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ rising to 2.0 V | - | 25 | 50 | ns |
| $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}, \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ Resistance | Resistor to LGND. Note 3 | 20 | 50 | 100 | k $\Omega$ |
| $\mathrm{V}_{\text {GATE(H), }} \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})} @ 10 \mathrm{~mA}$; LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ @ 10 mA | - | 600 | 800 | mV |

Soft Start (SS)

| Charge Time | - | 1.6 | 3.3 | 5.0 | ms |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | (Charge Time /Pulse Period) $\times 100$ | 1.0 | 3.3 | 6.0 | \% |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | v |
| $V_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

## PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

## Supply Current

| $\mathrm{I}_{\mathrm{CC} 1}$ | No Switching | - | 8.5 | 13.5 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{CC} 2}$ | No Switching | - | 1.6 | 3.0 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 1}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 8.0 | 13 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 2}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.0 | 5.0 | mA |

Coff

| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Extension Charge Time | $\mathrm{V}_{\mathrm{SS}}=\mathrm{V}_{\mathrm{FFB}}=0$ | 5.0 | 8.0 | 11.0 | $\mu \mathrm{~s}$ |
| Discharge Current | $\mathrm{C}_{\mathrm{OFF}}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |

Time Out Timer

| Time Out Time | $V_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ;$ <br> Record $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ Pulse High Duration | 10 | 30 | 65 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 70 | $\%$ |

3. Guaranteed by design, not $100 \%$ tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| 16 Lead SO Narrow |  |  |
| 1, 2, 3, 4 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID3 }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. The DAC range is 2.14 V to 3.54 V with 100 mV increments. $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID3 }}$ select the desired DAC output voltage. Leaving all 4 DAC input pins open results in a DAC output voltage of 1.244 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 6 | NC | No Connection. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE(H) }}$ | High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ from being in high state simultaneously. |
| 11 | PGND | High current ground for the IC. The MOSFET drivers are referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 1.5 A peak switching current. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC and low side gate driver. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{F B}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. V ${ }^{2}$ Control Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5150H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu \mathrm{~s}$ timer, minimizing stress to the power components.

## Programmable Output

The CS5150H is designed to provide two methods for programming the output voltage of the power supply. A four bit on board digital to analog converter (DAC) is used to program the output voltage from 2.14 V to 3.54 V in 100 mV steps, depending on the digital input code. If all four bits are left open, the CS5150H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers. The CS5150H is specifically designed to be upwards compatible with the CS5155H, which uses a five bit DAC code.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the $\operatorname{GATE}(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.
When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C CoFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.
The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP
capacitor charging to its final value. Its voltage is limited by the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ and $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (1.0 V/div.)
Figure 4. CS5150H Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5150H Demonstration Board Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1- Regulator Output Voltage (5.0 V/div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 6. CS5150H Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C OFF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.) Trace 2- Inductor Switching Node (5.0 V/div.)

Figure 7. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=0.5 \mathrm{~A}$ (Light Load)


Trace 1- Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 8. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$,

$$
\text { lout = } 13 \text { A (Heavy Load) }
$$

## Transient Response

The CS5150H V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "adaptive voltage positioning". This technique pre-positions the output capacitor's voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifier's reference voltage to be targeted +40 mV high without compromising DC accuracy. A "droop resistor", implemented through a PC board trace, connects the error amplifier's feedback pin $\left(\mathrm{V}_{\mathrm{FB}}\right)$ to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the error amplifier's, including the +40 mV offset. When the full load current is delivered, an 80 mV drop is developed across this resistor. This results in output voltage being offset -40 mV low.

The result of adaptive voltage positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre-positioned +40 mV . Conversely, when load current suddenly decreases from its maximum
level, the output capacitor is pre-positioned -40 mV (see Figures 9, 10, and 11). For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.
If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Figure 9. CS5150H Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V)


Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Trace 3- Output Current ( 0.5 to 13 Amps ) ( $20 \mathrm{~V} / \mathrm{div}$.)
Figure 10. CS5150H Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V ). Upon Completing a Normal Off Time, The V² Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100\% Duty Cycle. Regulation is Achieved in Less Than 20 us


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} /$ div.)
Trace 3- Output Current ( 13 to $0,5 \mathrm{Amps}$ ) ( $20 \mathrm{mV} /$ div.)
Figure 11. CS5150H Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V). V ${ }^{2}$ Control Topology Immediately Connects Inductor to Ground, Providing 0\% Duty Cycle. Regulation is Achieved in Less Than $10 \mu \mathrm{~s}$

## PROTECTION AND MONITORING FEATURES

## $\mathrm{V}_{\mathrm{C} 1}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0$ V ), the $\mathrm{V}_{\mathrm{FFB}}$ low comparator sets the FAULT latch. This causes the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board
traces than occurs with constant NO TAGcurrent limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3-Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5150H Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15). The regulator will remain in this state until the overvoltage
condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.


Figure 14. OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Trace 4-5.0 V from PC Power Supply (2.0 V/div.)
Trace 1- Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Figure 15. OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\mathrm{FFB}}$ pin low, emulating a short circuit condition.


Figure 16. Implementing Shutdown with the CS5150H

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
\text { VPower Good }=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $\mathrm{V}_{\text {Power Good }}$.


Figure 17. Implementing Power Good with the CS5150H


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) (10 V/div.)
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 18. CS5150H Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Selecting External Components

The CS5150H can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. A charge pump may be easily implemented to permit use of standard MOSFETs or support 5.0 V or 12 V only systems (maximum of 20 V ). Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\mathrm{VGATE}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{~L})=12 \mathrm{~V}
$$



Figure 19. CS5150H Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is RDS $_{\mathrm{ON}}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\mathrm{ILOAD}^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\mathrm{I}_{\text {LOAD }}{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =

$$
\frac{\text { VOUT }+(\text { LLOAD } \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\text { VIN }+(\mathrm{ILOAD} \times \text { RDSON OF SYNCH FET }) \\
-(\mathrm{ILOAD} \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (Coff)

The C CFF timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

When the $\mathrm{V}_{\text {FFB }}$ pin is less than 1.0 V , the current charging the $\mathrm{C}_{\text {OFF }}$ capacitor is reduced. The extended off time can be calculated as follows:

$$
\text { TOFF }=\text { COFF } \times 24,242.5
$$

Off time will be determined by either the $\mathrm{T}_{\mathrm{OFF}}$ time, or the time out timer, whichever is longer.
(see Figure 19.)

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the COFF timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. The CS5150H reference circuit does not use this device due to its excellent design. Instead, the body diode of the synchronous MOSFET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=\mathrm{V}_{\mathrm{BD}} \times$ LLOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5150H demonstration board as shown in Figure 8;
Power $=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}$
This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## "Droop" Resistor for Adaptive Voltage Positioning

Adaptive voltage positioning is used to reduce output voltage excursions during abrupt changes in load current. Regulator output voltage is offset +40 mV when the regulator is unloaded, and -40 mV at full load. This results in increased margin before encountering minimum and maximum transient voltage limits, allowing use of less capacitance on the regulator output (see Figure 9).

To implement adaptive voltage positioning, a "droop" resistor must be connected between the output inductor and output capacitors and load. This is normally implemented by a PC board trace of the following value:

$$
\mathrm{RDROOP}=\frac{80 \mathrm{mV}}{\operatorname{l} \mathrm{MAX}}
$$

Adaptive voltage positioning can be disabled for improved $D C$ regulation by connecting the $V_{F B}$ pin directly to the load using a separate, non-load current carrying circuit trace.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to
provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:
Thermal Impedance $=\frac{\text { TJUNCTION }(\text { MAX })-\text { TAMBIENT }}{\text { Power }}$
A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 20. Filter Components


Figure 21. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. To implement adaptive voltage positioning, connect both slow and fast feedback pins $16\left(\mathrm{~V}_{\mathrm{FB}}\right)$ and 8 $\left(\mathrm{V}_{\mathrm{FFB}}\right)$ to the regulator output right at the inductor terminal. Connect inductor to the output capacitors via a trace with the following resistance:

$$
\text { RTRACE }=\frac{80 \mathrm{mV}}{\mathrm{I}_{\mathrm{MAX}}}
$$

This causes the output voltage to be +40 mV with no load, and -40 mV with a full load, improving regulator transient response. This trace must be wide enough to carry the full output current. (Typical trace is 1.0 inch long, 0.17 inch wide). Care should be taken to minimize any additional losses after the feedback connection point to maximize regulation.
7. If DC regulation is to be optimized (at the expense of degraded transient regulation), adaptive voltage positioning can be disabled by connecting to $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
8. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.

Route gate drive signals $\mathrm{V}_{\text {GATE(H) }}$ (pin 10) and $\mathrm{V}_{\text {GATE(L) }}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.


Figure 22. Layout Guidelines


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter


Figure 24. Additional Application Diagram, 12 V to 3.3 V/5.0 V Converter with Remote Sense


Figure 26. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing


Figure 25. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias

## CS5150H

PACKAGE THERMAL DATA

| Parameter |  | 16-SO | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5151H

## CPU 4-Bit Nonsynchronous Buck Controller

The CS5151H is a 4-bit nonsynchronous N-Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5151H is designed to operate over a $4.25-20 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V or 12 V as the main supply for conversion.

The CS5151H is specifically designed to power Pentium ${ }^{\circledR}$ processors with $\mathrm{MMX}^{\mathrm{TM}}$ Technology and other high performance core logic. It includes the following features: on board, 4-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5151H is upwards compatible with the 5-bit CS5156H, allowing the mother board designer the capability of using either the CS5151H or the CS5156H with no change in layout. The CS5151H is available in 16 pin surface mount package.

## Features

- N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 4-Bit DAC
- Upward Compatible with 5-Bit CS5155H/CS5156H
- 30 ns Gate Rise/Fall Times
- $1.0 \%$ DAC Accuracy
- 5.0 V \& 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- Adaptive Voltage Positioning
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Current Sharing
- Overvoltage Protection


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com
MARKING
DIAGRAM

PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5151HGD16 | SO-16 | 48 Units/Rail |
| CS5151HGDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, Switching Power Supply for Core Logic - Pentium ${ }^{\circledR}$ Processor with MMX Technology

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ABSOLUTE MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $25 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $20 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {FB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\mathrm{OFF}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {ID0 }}-\mathrm{V}_{\text {ID3 }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {GATE }}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\text {ID2 }}=\mathrm{V}_{I D 1}=\mathrm{V}_{I D 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\text {GATE }}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.3 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Open Loop Gain | $1.25 \mathrm{~V}<\mathrm{V}_{\mathrm{COMP}}<4.0 \mathrm{~V} ;$ Note 2 | 50 | 60 | - | dB |
| Unity Gain Bandwidth | Note 2 | 500 | 3000 | - | kHz |
| COMP SINK Current | $\mathrm{V}_{\mathrm{COMP}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}>2.0 \mathrm{~V}$ | 0.4 | 2.5 | 8.0 | mA |
| COMP SOURCE Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 30 | 50 | 80 | $\mu \mathrm{~A}$ |
| COMP CLAMP Current | $\mathrm{V}_{\mathrm{COMP}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 4.0 | 4.3 | 5.0 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}$ | - | 160 | 600 | mV |
| PSRR | $8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} @ 1.0 \mathrm{kHz}$; Note 2 | 60 | 85 | - | dB |

$\mathrm{V}_{\mathrm{CC} 1}$ Monitor

| Start Threshold | Output switching | 3.75 | 3.90 | 4.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 3.70 | 3.85 | 4.00 | V |
| Hysteresis | Start-Stop | - | 50 | - | mV |

DAC

| Input Threshold |  |  |  | $\mathrm{V}_{\text {IDO, }} \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}$ | 1.00 | 1.25 | 2.40 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Pull Up Resistance |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}$ | 25 | 50 | 100 | k $\Omega$ |
| Pull Up Voltage |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy (all codes except 1111) |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}}, 25^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ | - | - | 1.0 | \% |
| $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID } 2}$ | VID1 | $\mathrm{V}_{\text {IDO }}$ |  |  |  |  |  |
| 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 0 | - | 2.1186 | 2.1400 | 2.1614 | V |
| 1 | 1 | 0 | 1 | - | 2.2176 | 2.2400 | 2.2624 | V |
| 1 | 1 | 0 | 0 | - | 2.3166 | 2.3400 | 2.3634 | V |
| 1 | 0 | 1 | 1 | - | 2.4156 | 2.4400 | 2.4644 | V |
| 1 | 0 | 1 | 0 | - | 2.5146 | 2.5400 | 2.5654 | V |
| 1 | 0 | 0 | 1 | - | 2.6136 | 2.6400 | 2.6664 | V |
| 1 | 0 | 0 | 0 | - | 2.7126 | 2.7400 | 2.7674 | V |
| 0 | 1 | 1 | 1 | - | 2.8116 | 2.8400 | 2.8684 | V |
| 0 | 1 | 1 | 0 | - | 2.9106 | 2.9400 | 2.9694 | V |
| 0 | 1 | 0 | 1 | - | 3.0096 | 3.0400 | 3.0704 | V |
| 0 | 1 | 0 | 0 | - | 3.1086 | 3.1400 | 3.1714 | V |
| 0 | 0 | 1 | 1 | - | 3.2076 | 3.2400 | 3.2724 | V |
| 0 | 0 | 1 | 0 | - | 3.3066 | 3.3400 | 3.3734 | V |
| 0 | 0 | 0 | 1 | - | 3.4056 | 3.4400 | 3.4744 | V |
| 0 | 0 | 0 | 0 | - | 3.5046 | 3.5400 | 3.5754 | V |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V}\right.$;
$5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}$; DAC Code: $\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {GATE }}$ |  |  |  |  |  |
| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}}$ | - | 1.2 | 2.0 | V |
| Out SINK Sat at 100 mA | Measure $\mathrm{V}_{\text {GATE }}-\mathrm{V}_{\text {PGND }}$ | - | 1.0 | 1.5 | V |
| Out Rise Time | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}}<9.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 30 | 50 | ns |
| Out Fall Time | $9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}}>1.0 \mathrm{~V}$; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 30 | 50 | ns |
| Shoot-Through Current | Note 3 | - | - | 50 | mA |
| $\mathrm{V}_{\text {GATE }}$ Resistance | Resistor to LGND. Note 3 | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE }}$ Schottky | LGND to $\mathrm{V}_{\text {GATE }} @ 10 \mathrm{~mA}$ | - | 600 | 800 | mV |
| Soft Start (SS) |  |  |  |  |  |
| Charge Time | - | 1.6 | 3.3 | 5.0 | ms |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | (Charge Time /Pulse Period) $\times 100$ | 1.0 | 3.3 | 6.0 | \% |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\text {SS }}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\text {GATE }}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

PWM Comparator

| Transient Response | $V_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

## Supply Current

| $\mathrm{I}_{\mathrm{CC} 1}$ | No Switching | - | 8.5 | 13.5 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{CC} 2}$ | No Switching | - | 1.6 | 3.0 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 1}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 8.0 | 13 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 2}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.0 | 5.0 | mA |

## Coff

| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Extension Charge Time | $\mathrm{V}_{\mathrm{SS}}=\mathrm{V}_{\mathrm{FFB}}=0$ | 5.0 | 8.0 | 11.0 | $\mu \mathrm{~s}$ |
| Discharge Current | $\mathrm{C}_{\mathrm{OFF}}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |

## Time Out Timer

$\left.\begin{array}{|l|l|c|c|c|c|}\hline \text { Time Out Time } & \begin{array}{l}V_{\text {FB }}=V_{\text {COMP }} ; V_{\text {FFB }}=2.0 ~ V ; \\ \text { Record } \\ \text { GATE }\end{array} & 10 & 30 & 65 & \mu \mathrm{~s} \\ \hline \text { Fault Mode Digh Duration }\end{array}\right]$
3. Guaranteed by design, not $100 \%$ tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| 16 Lead SO Narrow |  |  |
| 1, 2, 3, 4 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID3 }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. The DAC range is 2.14 V to 3.54 V with 100 mV increments. $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID3 }}$ select the desired DAC output voltage. Leaving all 4 DAC input pins open results in a DAC output voltage of 1.244 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 6, 12 | NC | No Connection. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the gate driver. |
| 10 | $\mathrm{V}_{\text {GATE }}$ | MOSFET driver pin capable of 1.5 A peak switching current. |
| 11 | PGND | High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground and the anode of the Schottky diode should be tied to this pin. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{\text {FB }}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. V ${ }^{2}$ Control Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5151H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu \mathrm{~s}$ timer, minimizing stress to the power components.

## Programmable Output

The CS5151H is designed to provide two methods for programming the output voltage of the power supply. A four bit on board digital to analog converter (DAC) is used to program the output voltage from 2.14 V to 3.54 V in 100 mV steps, depending on the digital input code. If all four bits are left open, the CS5151H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers. The CS5151H is specifically designed to be upwards compatible with the CS5156H, which uses a five bit DAC code.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE output is activated, and the Soft Start capacitor begins charging. The GATE output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.
If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE pin drives low for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. Then, the GATE pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C CoFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.
The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by
the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ and $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Figure 4. CS5151H Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3-COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5151H Demonstration Board Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1-Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Figure 6. CS5151H Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} /$ div.) Trace 2- Inductor Switching Node (5.0 V/div.)

Figure 7. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, lout $=0.5$ A (Light Load)


Trace 1-Regulator Output Voltage ( $10 \mathrm{~V} /$ div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 8. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, IOUT = 13 A (Heavy Load)

## Transient Response

The CS5151H V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "adaptive voltage positioning". This technique pre-positions the output capacitor's voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifier's reference voltage to be targeted +40 mV high without compromising DC accuracy. A "droop resistor", implemented through a PC board trace, connects the error amplifier's feedback pin $\left(\mathrm{V}_{\mathrm{FB}}\right)$ to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the error amplifier's, including the +40 mV offset. When the full load current is delivered, an 80 mV drop is developed across this resistor. This results in output voltage being offset -40 mV low.

The result of adaptive voltage positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre-positioned +40 mV . Conversely, when load current suddenly decreases from its maximum
level, the output capacitor is pre-positioned -40 mV (see Figures 9, 10, and 11). For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.
If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Regulator Output Voltage ( $20 \mathrm{~V} / \mathrm{div}$.)
Figure 9. CS5151H Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V)


Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Trace 3- Output Current ( 0.5 to 13 Amps ) ( $20 \mathrm{~V} / \mathrm{div}$.)
Figure 10. CS5151H Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V ). Upon Completing a Normal Off Time, The V ${ }^{2}$ Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100\% Duty Cycle. Regulation is Achieved in Less Than 20 us


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} /$ div.)
Trace 3- Output Current ( 13 to $0,5 \mathrm{Amps}$ ) ( $20 \mathrm{mV} /$ div.)
Figure 11. CS5151H Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V). V ${ }^{2}$ Control Topology Immediately Connects Inductor to Ground, Providing 0\% Duty Cycle. Regulation is Achieved in Less Than $10 \mu \mathrm{~s}$

## PROTECTION AND MONITORING FEATURES

## $\mathrm{V}_{\mathrm{C} 1}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\mathrm{FFB}}$ low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board
traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3-Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5151H Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the MOSFET to shut off, disconnecting the regulator from it's input voltage.

## External Output Enable Circuit

On/off control of the regulator can be implemented through two additional discrete components (see Figure 14).

This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\mathrm{FFB}}$ pin low, emulating a short circuit condition.


Figure 14. Implementing Shutdown with the CS5151H

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 15). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power Good }}$.


Figure 15. Implementing Power Good with the CS5151H


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $10 \mathrm{~V} /$ div. )
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 16. CS5151H Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Selecting External Components

The CS5151H can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and use logic level MOSFETs. A charge pump may be easily implemented to permit use of standard MOSFETs or support 5.0 V or 12 V only systems (maximum of 20 V ). Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. The gate driver output is specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of its bias supply when in the high state. In practice, the MOSFET gate will be driven rail to rail due to overshoot caused by the capacitive load it presents to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=$ $\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\mathrm{V}_{\mathrm{GATE}}=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}
$$

(see Figure 17.)


Figure 17. CS5151H Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is RDS $_{\text {ON }}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFET and the Schottky diode may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\text { LLOAD }^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Schottky diode:

$$
\text { Power }=\text { VFORWARD } \times \text { ILOAD } \times(1-\text { duty cycle })
$$

Duty Cycle =
VOUT + VFORWARD
$\overline{\mathrm{V}_{\text {IN }}}+\mathrm{V}_{\text {FORWARD }}-($ ILOAD $\times$ RDSON OF SYNCH FET) $)$

## Off Time Capacitor (Coff)

The C Coff timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

When the $\mathrm{V}_{\text {FFB }}$ pin is less than 1.0 V , the current charging the $\mathrm{C}_{\mathrm{OFF}}$ capacitor is reduced. The extended off time can be calculated as follows:

$$
\text { TOFF }=\text { COFF } \times 24,242.5
$$

Off time will be determined by either the $\mathrm{T}_{\mathrm{OFF}}$ time, or the time out timer, whichever is longer.

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\mathrm{OFF}}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:
Period $=\frac{1}{\text { switching frequency }}$
"Droop" Resistor for Adaptive Voltage Positioning
Adaptive voltage positioning is used to reduce output voltage excursions during abrupt changes in load current. Regulator output voltage is offset +40 mV when the regulator is unloaded, and -40 mV at full load. This results in increased margin before encountering minimum and maximum transient voltage limits, allowing use of less capacitance on the regulator output (see Figure 9).

To implement adaptive voltage positioning, a "droop" resistor must be connected between the output inductor and output capacitors and load. This is normally implemented by a PC board trace of the following value:

$$
\text { RDROOP }=\frac{80 \mathrm{mV}}{\mathrm{I} \mathrm{MAX}}
$$

Adaptive voltage positioning can be disabled for improved DC regulation by connecting the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load using a separate, non-load current carrying circuit trace.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:
Thermal Impedance $=\frac{\text { TJUNCTION(MAX) }- \text { TAMBIENT }}{\text { Power }}$
A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 18. Filter Components


Figure 19. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. To implement adaptive voltage positioning, connect both slow and fast feedback pins $16\left(\mathrm{~V}_{\mathrm{FB}}\right)$ and 8 $\left(\mathrm{V}_{\mathrm{FFB}}\right)$ to the regulator output right at the inductor terminal. Connect inductor to the output capacitors via a trace with the following resistance:

$$
\text { RTRACE }=\frac{80 \mathrm{mV}}{\mathrm{I}_{\mathrm{MAX}}}
$$

This causes the output voltage to be +40 mV with no load, and -40 mV with a full load, improving regulator transient response. This trace must be wide enough to carry the full output current. (Typical trace is 1.0 inch long, 0.17 inch wide). Care should be taken to minimize any additional losses after the feedback connection point to maximize regulation.
7. If DC regulation is to be optimized (at the expense of degraded transient regulation), adaptive voltage positioning can be disabled by connecting to $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
8. Place 5.0 V input capacitors close to the switching MOSFET.

Route gate drive signals $\mathrm{V}_{\text {GATE }}$ (pin 10) with a trace that is a minimum of 0.025 inches wide.


Figure 20. Layout Guidelines


Figure 21. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter


Figure 22. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing
PACKAGE THERMAL DATA

| Parameter |  | 16-SO | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5155H

## CPU 5-Bit Synchronous Buck Controller

The CS5155H is a 5 -bit synchronous dual N -Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5155H is designed to operate over a $4.25-20 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V or 12 V as the main supply for conversion.

The CS5155H is specifically designed to power Pentium ${ }^{\circledR}$ II processors and other high performance core logic. It includes the following features: on board, 5-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5155H is backwards compatible with the 4-bit CS5150, allowing the mother board designer the capability of using either the CS5150 or the CS5155H with no change in layout. The CS5155H is available in 16 pin surface mount packages.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5-Bit DAC
- Backward Compatible with 4-Bit CS5150H/CS5151H
- 30 ns Gate Rise/Fall Times
- $1.0 \%$ DAC Accuracy
- 5.0 V \& 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- 25 ns FET Nonoverlap Time
- Adaptive Voltage Positioning
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Current Sharing
- Overvoltage Protection


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


A = Assembly Location
WL, L = Wafer Lot
$\mathrm{YY}, \mathrm{Y}=$ Year
WW, W = Work Week

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5155HGD16 | SO-16 | 48 Units/Rail |
| CS5155HGDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, Switching Power Supply for Core Logic - Pentium ${ }^{\circledR}$ II Processor

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{\mathrm{J}}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow: (SMD styles only) (Note 2) | 260 peak 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\text {S }}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ABSOLUTE MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $25 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $20 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | -100 $\mu \mathrm{A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\mathrm{FB}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| CofF | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {GATE( }}(\mathrm{H})$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\text {GATE(L) }}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

## CS5155H

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V} ; \mathrm{DAC}\right.$ Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | 

$\mathrm{V}_{\mathrm{CC} 1}$ Monitor

| Start Threshold | Output switching | 3.75 | 3.90 | 4.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 3.70 | 3.85 | 4.00 | V |
| Hysteresis | Start-Stop | - | 50 | - | mV |

$\mathrm{V}_{\text {GATE( }}$ ) and $\mathrm{V}_{\text {GATE(L) }}$

| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1}-\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} ; \mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | - | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Out SINK Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}-\mathrm{V}_{\text {PGND }} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}-\mathrm{V}_{\text {PGND }}$ | - | 1.0 | 1.5 | V |
| Out Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}<9.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}>1.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Shoot-Through Current | Note 3 | - | - | 50 | mA |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to 2.0 V ; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ rising to 2.0 V | - | 25 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to 2.0 V ; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\text {GATE(H) }}$ rising to 2.0 V | - | 25 | 50 | ns |
| $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}, \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ Resistance | Resistor to LGND. Note 3 | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE(H) }}, \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ @ 10 mA LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} @ 10 \mathrm{~mA}$ | - | 600 | 800 | mV |

## Soft Start (SS)

| Charge Time |  | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | (Charge Time /Pulse Period) $\times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}}(\mathrm{L})=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

## PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

3. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V} ;\right.$ DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |  |  |  |  | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC |  |  |  |  |  |  |  |  |  |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID0, }} \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID } 4}$ | 1.00 | 1.25 | 2.40 | V |
| Input Pull Up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID } 0, ~} \mathrm{~V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID } 2}, \mathrm{~V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID } 4}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Pull Up Voltage |  |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy (all codes except 11111) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}}, 25^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ | - | - | 1.0 | \% |
| VID4 | VID3 | VID2 | VID1 | VID0 |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | - | 1.3266 | 1.3400 | 1.3534 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.3761 | 1.3900 | 1.4039 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.4256 | 1.4400 | 1.4544 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.4751 | 1.4900 | 1.5049 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.5246 | 1.5400 | 1.5554 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.5741 | 1.5900 | 1.6059 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.6236 | 1.6400 | 1.6564 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.6731 | 1.6900 | 1.7069 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.7226 | 1.7400 | 1.7574 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.7721 | 1.7900 | 1.8079 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.8216 | 1.8400 | 1.8584 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.8711 | 1.8900 | 1.9089 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.9206 | 1.9400 | 1.9594 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.9701 | 1.9900 | 2.0099 | V |
| 0 | 0 | 0 | 0 | 1 | - | 2.0196 | 2.0400 | 2.0604 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.0691 | 2.0900 | 2.1109 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.1186 | 2.1400 | 2.1614 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.2176 | 2.2400 | 2.2624 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.3166 | 2.3400 | 2.3634 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.4156 | 2.4400 | 2.4644 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.5146 | 2.5400 | 2.5654 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.6136 | 2.6400 | 2.6664 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.7126 | 2.7400 | 2.7674 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.8116 | 2.8400 | 2.8684 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.9106 | 2.9400 | 2.9694 | V |
| 1 | 0 | 1 | 0 | 1 | - | 3.0096 | 3.0400 | 3.0704 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.1086 | 3.1400 | 3.1714 | V |
| 1 | 0 | 0 | 1 | 1 | - | 3.2076 | 3.2400 | 3.2724 | V |
| 1 | 0 | 0 | 1 | 0 | - | 3.3066 | 3.3400 | 3.3734 | V |
| 1 | 0 | 0 | 0 | 1 | - | 3.4056 | 3.4400 | 3.4744 | V |
| 1 | 0 | 0 | 0 | 0 | - | 3.5046 | 3.5400 | 3.5754 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V} ; \mathrm{DAC}\right.$ Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDD}}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current |  |  |  |  |  |
| $I_{\text {CC1 }}$ | No Switching | - | 8.5 | 13.5 | mA |
| ICC2 | No Switching | - | 1.6 | 3.0 | mA |
| Operating $\mathrm{I}_{\text {CC1 }}$ | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 8.0 | 13 | mA |
| Operating ICC2 | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.0 | 5.0 | mA |
| $\mathrm{C}_{\text {OFF }}$ |  |  |  |  |  |
| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {SS }}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{s}$ |
| Extension Charge Time | $\mathrm{V}_{\text {SS }}=\mathrm{V}_{\text {FFB }}=0$ | 5.0 | 8.0 | 11.0 | $\mu \mathrm{s}$ |
| Discharge Current | $\mathrm{C}_{\text {OFF }}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\text {FB }}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |
| Time Out Timer |  |  |  |  |  |
| Time Out Time | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ; \\ & \text { Record } \mathrm{V}_{\mathrm{GATE}(\mathrm{H})} \text { Pulse High Duration } \end{aligned}$ | 10 | 30 | 65 | $\mu \mathrm{s}$ |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 70 | \% |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-16 | PIN SYMBOL | FUNCTION |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is High (logic one), the DAC range is 2.14 V to 3.54 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is Low (logic zero), the DAC range is 1.34 V to 2.09 V with 50 mV increments. $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID4 }}$ select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.244 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE(H) }}$ | High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ from being in high state simultaneously. |
| 11 | PGND | High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 1.5 A peak switching current. |
| 13 | $\mathrm{V}_{\text {CC1 }}$ | Input power for the IC and low side gate driver. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{F B}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. V ${ }^{2}$ Control Diagram

The $V^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5155H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu \mathrm{~s}$ timer, minimizing stress to the power components.

## Programmable Output

The CS5155H is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.14 V to 3.54 V in 100 mV steps, the second is 1.34 V to 2.09 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5155H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers. The CS5155H is specifically designed to be backwards compatible with the CS5150, which uses a four bit DAC code.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.
When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C CoFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.
The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP
capacitor charging to its final value. Its voltage is limited by the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ and $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (1.0 V/div.)
Figure 4. CS5155H Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5155H Demonstration Board Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1- Regulator Output Voltage (5.0 V/div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 6. CS5155H Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C OFF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1- Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.) Trace 2- Inductor Switching Node (5.0 V/div.)

Figure 7. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=0.5 \mathrm{~A}$ (Light Load)


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 8. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, lout = 13 A (Heavy Load)

## Transient Response

The CS5155H V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "adaptive voltage positioning". This technique pre-positions the output capacitor's voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifier's reference voltage to be targeted +40 mV high without compromising DC accuracy. A "droop resistor", implemented through a PC board trace, connects the error amplifier's feedback pin $\left(\mathrm{V}_{\mathrm{FB}}\right)$ to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the error amplifier's, including the +40 mV offset. When the full load current is delivered, an 80 mV drop is developed across this resistor. This results in output voltage being offset -40 mV low.

The result of adaptive voltage positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre-positioned +40 mV . Conversely, when load current suddenly decreases from its maximum
level, the output capacitor is pre-positioned -40 mV (see Figures 9, 10, and 11). For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.
If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Regulator Output Voltage ( $20 \mathrm{~V} / \mathrm{div}$.)
Figure 9. CS5155H Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V)


Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Trace 3- Output Current ( 0.5 to 13 Amps ) ( $20 \mathrm{~V} / \mathrm{div}$.)
Figure 10. CS5155H Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V ). Upon Completing a Normal Off Time, The V ${ }^{2}$ Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100\% Duty Cycle. Regulation is Achieved in Less Than 20 us


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} /$ div.)
Trace 3- Output Current ( 13 to $0,5 \mathrm{Amps}$ ) ( $20 \mathrm{mV} /$ div.)
Figure 11. CS5155H Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V). V ${ }^{2}$ Control Topology Immediately Connects Inductor to Ground, Providing 0\% Duty Cycle. Regulation is Achieved in Less Than $10 \mu \mathrm{~s}$

## PROTECTION AND MONITORING FEATURES

## $\mathrm{V}_{\mathrm{C} 1}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\mathrm{FFB}}$ low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board
traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3-Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5155H Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15 ). The regulator will remain in this state until the overvoltage
condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.


Figure 14. OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Trace 4-5.0 V from PC Power Supply (2.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Figure 15. OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\mathrm{FFB}}$ pin low, emulating a short circuit condition.


Figure 16. Implementing Shutdown with the CS5155H

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
\text { VPower Good }=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $\mathrm{V}_{\text {Power Good }}$.


Figure 17. Implementing Power Good with the CS5155H


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) (10 V/div.)
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 18. CS5155H Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Selecting External Components

The CS5155H can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and use logic level MOSFETs. A charge pump may be easily implemented to support 5.0 V or 12 V only systems (maximum of 20 V ). Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\operatorname{VGATE}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{~L})=12 \mathrm{~V}
$$



Figure 19. CS5155H Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is RDS $_{\mathrm{ON}}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\mathrm{ILOAD}^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\mathrm{I}_{\text {LOAD }}{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =

$$
\frac{\text { VOUT }+(\text { LLOAD } \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\text { VIN }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET }) \\
-(\text { ILOAD } \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (Coff)

The C CFF timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

When the $\mathrm{V}_{\text {FFB }}$ pin is less than 1.0 V , the current charging the $\mathrm{C}_{\text {OFF }}$ capacitor is reduced. The extended off time can be calculated as follows:

$$
\text { TOFF }=\text { COFF } \times 24,242.5
$$

Off time will be determined by either the $\mathrm{T}_{\mathrm{OFF}}$ time, or the time out timer, whichever is longer.
(see Figure 19.)

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\text {OFF }}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. The CS5155H reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous MOSFET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=V_{B D} \times$ LLOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5155H demonstration board as shown in Figure 8;
Power $=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}$
This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## "Droop" Resistor for Adaptive Voltage Positioning

Adaptive voltage positioning is used to reduce output voltage excursions during abrupt changes in load current. Regulator output voltage is offset +40 mV when the regulator is unloaded, and -40 mV at full load. This results in increased margin before encountering minimum and maximum transient voltage limits, allowing use of less capacitance on the regulator output (see Figure 9).

To implement adaptive voltage positioning, a "droop" resistor must be connected between the output inductor and output capacitors and load. This is normally implemented by a PC board trace of the following value:

$$
\text { RDROOP }=\frac{80 \mathrm{mV}}{\mathrm{I}_{\mathrm{MAX}}}
$$

Adaptive voltage positioning can be disabled for improved $D C$ regulation by connecting the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load using a separate, non-load current carrying circuit trace.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to
provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:
Thermal Impedance $=\frac{\left.\text { TJUNCTION }^{\text {MAX }}\right)- \text { TAMBIENT }}{\text { Power }}$
A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 20. Filter Components


Figure 21. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. To implement adaptive voltage positioning, connect both slow and fast feedback pins $16\left(\mathrm{~V}_{\mathrm{FB}}\right)$ and 8 $\left(\mathrm{V}_{\mathrm{FFB}}\right)$ to the regulator output right at the inductor terminal. Connect inductor to the output capacitors via a trace with the following resistance:

$$
\text { RTRACE }=\frac{80 \mathrm{mV}}{\mathrm{I}_{\mathrm{MAX}}}
$$

This causes the output voltage to be +40 mV with no load, and -40 mV with a full load, improving regulator transient response. This trace must be wide enough to carry the full output current. (Typical trace is 1.0 inch long, 0.17 inch wide). Care should be taken to minimize any additional losses after the feedback connection point to maximize regulation.
7. If DC regulation is to be optimized (at the expense of degraded transient regulation), adaptive voltage positioning can be disabled by connecting to $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
8. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.

Route gate drive signals $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ (pin 10) and $\mathrm{V}_{\text {GATE(L) }}$ (pin 12 when used) with a trace that are a minimum of 0.025 inches wide.


Figure 22. Layout Guidelines


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter


Figure 24. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias


Figure 25. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing


Figure 26. Additional Application Diagram, 12 V to 3.3 V/5.0 A Converter with Remote Sense

## CS5155H

PACKAGE THERMAL DATA

| Parameter |  | 16-SO | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5156H

## CPU 5-Bit Nonsynchronous Buck Controller

The CS5156H is a 5 -bit nonsynchronous N-Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5156H is designed to operate over a $4.25-20 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V or 12 V as the main supply for conversion.

The CS5156H is specifically designed to power Pentium ${ }^{\circledR}$ II processors and other high performance core logic. It includes the following features: on board, 5-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5156H is backwards compatible with the 4-bit CS5151, allowing the mother board designer the capability of using either the CS5151 or the CS5156H with no change in layout. The CS5156H is available in 16 pin surface mount packages.

## Features

- N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5-Bit DAC
- Backward Compatible with 4-Bit CS5150H/CS5151H
- 30 ns Gate Rise/Fall Times
- $1.0 \%$ DAC Accuracy
- 5.0 V \& 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- Adaptive Voltage Positioning
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Current Sharing
- Overvoltage Protection

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


A = Assembly Location
WL, L = Wafer Lot
YY, $Y=$ Year
WW, W = Work Week

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5156HGD16 | SO-16 | 48 Units/Rail |
| CS5156HGDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, Switching Power Supply for Core Logic - Pentium ${ }^{\circledR}$ II Processor

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :--- | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ | Reflow: (SMD styles only) (Note 1$)$ | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $25 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $20 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {FB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\mathrm{OFF}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {IDO }}-\mathrm{V}_{\text {ID } 4}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{GATE}}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDO}}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- |

Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.3 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Open Loop Gain | $1.25 \mathrm{~V}<\mathrm{V}_{\mathrm{COMP}}<4.0 \mathrm{~V} ; \mathrm{Note} 2$ | 50 | 60 | - | dB |
| Unity Gain Bandwidth | Note 2 | 500 | 3000 | - | kHz |
| COMP SINK Current | $\mathrm{V}_{\mathrm{COMP}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}>2.0 \mathrm{~V}$ | 0.4 | 2.5 | 8.0 | mA |
| COMP SOURCE Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 30 | 50 | 80 | $\mu \mathrm{~A}$ |
| COMP CLAMP Current | $\mathrm{V}_{\mathrm{COMP}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 4.0 | 4.3 | 5.0 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}$ | - | 160 | 600 | mV |
| PSRR | $8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} @ 1.0 \mathrm{kHz} ;$ Note 2 | 60 | 85 | - | dB |

$\mathrm{V}_{\mathrm{CC} 1}$ Monitor

| Start Threshold | Output switching | 3.75 | 3.90 | 4.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 3.70 | 3.85 | 4.00 | V |
| Hysteresis | Start-Stop | - | 50 | - | mV |

$V_{\text {GATE }}$

| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}}$ | - | 1.2 | 2.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Out SINK Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{GATE}}-\mathrm{V}_{\mathrm{PGND}}$ | - | 1.0 | 1.5 | V |
| Out Rise Time | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}}<9.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 30 | 50 | ns |
| Out Fall Time | $9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}}>1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 30 | 50 | ns |
| Shoot-Through Current | Note 2 | - | - | 50 | mA |
| $\mathrm{~V}_{\text {GATE }}$ Resistance | Resistor to LGND. Note 2 | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE }}$ Schottky | LGND to $\mathrm{V}_{\text {GATE }} @ 10 \mathrm{~mA}$ | - | 600 | 800 | mV |

## Soft Start (SS)

| Charge Time | - | 1.6 | 3.3 | 5.0 | ms |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | (Charge Time /Pulse Period) $\times 100$ | 1.0 | 3.3 | 6.0 | \% |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\text {GATE }}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

## PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDD}}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |  |  |  |  | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC |  |  |  |  |  |  |  |  |  |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID4 }}$ | 1.00 | 1.25 | 2.40 | V |
| Input Pull Up Resistance |  |  |  |  | $\mathrm{V}_{I D 0}, \mathrm{~V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID }}, \mathrm{V}_{\text {ID } 4}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Pull Up Voltage |  |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy (all codes except 11111) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}, 25^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ | - | - | 1.0 | \% |
| $\mathrm{V}_{\text {ID4 }}$ | $\mathrm{V}_{\text {ID3 }}$ | VID2 | $\mathrm{V}_{\text {ID } 1}$ | VIDO |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | - | 1.3266 | 1.3400 | 1.3534 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.3761 | 1.3900 | 1.4039 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.4256 | 1.4400 | 1.4544 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.4751 | 1.4900 | 1.5049 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.5246 | 1.5400 | 1.5554 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.5741 | 1.5900 | 1.6059 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.6236 | 1.6400 | 1.6564 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.6731 | 1.6900 | 1.7069 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.7226 | 1.7400 | 1.7574 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.7721 | 1.7900 | 1.8079 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.8216 | 1.8400 | 1.8584 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.8711 | 1.8900 | 1.9089 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.9206 | 1.9400 | 1.9594 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.9701 | 1.9900 | 2.0099 | V |
| 0 | 0 | 0 | 0 | 1 | - | 2.0196 | 2.0400 | 2.0604 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.0691 | 2.0900 | 2.1109 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.1186 | 2.1400 | 2.1614 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.2176 | 2.2400 | 2.2624 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.3166 | 2.3400 | 2.3634 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.4156 | 2.4400 | 2.4644 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.5146 | 2.5400 | 2.5654 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.6136 | 2.6400 | 2.6664 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.7126 | 2.7400 | 2.7674 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.8116 | 2.8400 | 2.8684 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.9106 | 2.9400 | 2.9694 | V |
| 1 | 0 | 1 | 0 | 1 | - | 3.0096 | 3.0400 | 3.0704 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.1086 | 3.1400 | 3.1714 | V |
| 1 | 0 | 0 | 1 | 1 | - | 3.2076 | 3.2400 | 3.2724 | V |
| 1 | 0 | 0 | 1 | 0 | - | 3.3066 | 3.3400 | 3.3734 | V |
| 1 | 0 | 0 | 0 | 1 | - | 3.4056 | 3.4400 | 3.4744 | V |
| 1 | 0 | 0 | 0 | 0 | - | 3.5046 | 3.5400 | 3.5754 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDO}}=1 ; \mathrm{V}_{\mathrm{ID}}=0 ; \mathrm{CV}_{\mathrm{GATE}}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified. .

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Supply Current | No Switching | - | 8.5 | 13.5 | mA |
| $\mathrm{I}_{\mathrm{CC} 1}$ | No Switching | - | 1.6 | 3.0 | mA |
| $\mathrm{I}_{\mathrm{CC} 2}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 8.0 | 13 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 1}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.0 | 5.0 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 2}$ |  |  |  |  |  |

$\mathrm{C}_{\text {OFF }}$

| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Extension Charge Time | $\mathrm{V}_{\mathrm{SS}}=\mathrm{V}_{\mathrm{FFB}}=0$ | 5.0 | 8.0 | 11.0 | $\mu \mathrm{~s}$ |
| Discharge Current | $\mathrm{C}_{\mathrm{OFF}}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |

Time Out Timer

| Time Out Time | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ;$ <br> Record $\mathrm{V}_{\mathrm{GATE}}$ Pulse High Duration | 10 | 30 | 65 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 70 | $\%$ |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| SO-16 |  |  |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is High (logic one), the DAC range is 2.14 V to 3.54 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is Low (logic zero), the DAC range is 1.34 V to 2.09 V with 50 mV increments. $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID4 }}$ select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.244 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\text {CC2 }}$ | Boosted power for the gate driver. |
| 10 | $\mathrm{V}_{\text {GATE }}$ | MOSFET driver pin capable of 1.5 A peak switching current. |
| 11 | PGND | High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground and the anode of the Schottky diode should be tied to this pin. |
| 12 | NC | No connection. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{\text {FB }}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. ${ }^{2}$ ºntrol Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5156H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu \mathrm{~s}$ timer, minimizing stress to the power components.

## Programmable Output

The CS5156H is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.14 V to 3.54 V in 100 mV steps, the second is 1.34 V to 2.09 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5156H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers. The CS5156H is specifically designed to be backwards compatible with the CS5151H, which uses a four bit DAC code.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE output is activated, and the Soft Start capacitor begins charging. The GATE output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.
If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE pin drives low for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. Then, the GATE pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C $\mathrm{C}_{\mathrm{OFF}}$ capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by
the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ and $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (1.0 V/div.)
Figure 4. CS5156H Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5156H Demonstration Board Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1-Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 6. CS5156H Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C CopF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} /$ div.) Trace 2- Inductor Switching Node (5.0 V/div.)

Figure 7. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=0.5 \mathrm{~A}$ (Light Load)


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 8. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$,

$$
\text { lout = } 13 \text { A (Heavy Load) }
$$

## Transient Response

The CS5156H V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "adaptive voltage positioning". This technique pre-positions the output capacitor's voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifier's reference voltage to be targeted +40 mV high without compromising DC accuracy. A "droop resistor", implemented through a PC board trace, connects the error amplifier's feedback pin $\left(\mathrm{V}_{\mathrm{FB}}\right)$ to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the error amplifier's, including the +40 mV offset. When the full load current is delivered, an 80 mV drop is developed across this resistor. This results in output voltage being offset -40 mV low.

The result of adaptive voltage positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre-positioned +40 mV . Conversely, when load current suddenly decreases from its maximum
level, the output capacitor is pre-positioned -40 mV (see Figures 9, 10, and 11). For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.
If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Regulator Output Voltage ( $20 \mathrm{~V} / \mathrm{div}$.)
Figure 9. CS5156H Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V)


Trace 1-Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Trace 3- Output Current ( 0.5 to 13 Amps ) ( $20 \mathrm{~V} / \mathrm{div}$.)
Figure 10. CS5156H Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V ). Upon Completing a Normal Off Time, The V ${ }^{2}$ Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100\% Duty Cycle. Regulation is Achieved in Less Than $20 \mu \mathrm{~s}$


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} /$ div.)
Trace 3- Output Current ( 13 to $0,5 \mathrm{Amps}$ ) ( $20 \mathrm{mV} /$ div.)
Figure 11. CS5156H Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V). V ${ }^{2}$ Control Topology Immediately Connects Inductor to Ground, Providing 0\% Duty Cycle. Regulation is Achieved in Less Than $10 \mu \mathrm{~s}$

## PROTECTION AND MONITORING FEATURES

## $\mathrm{V}_{\mathrm{C} 1}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\mathrm{FFB}}$ low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board
traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3-Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5156H Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage.

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components
(see Figure 14). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\mathrm{FFB}}$ pin low, emulating a short circuit condition.


Figure 14. Implementing Shutdown with the CS5156H

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 15). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power Good }}$.


Figure 15. Implementing Power Good with the CS5156H


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) (10 V/div.)
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 16. CS5156H Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Selecting External Components

The CS5156H can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and use logic level MOSFETs. A charge pump may be easily implemented to permit use of standard MOSFETs or support 5.0 V or 12 V only systems (maximum of 20 V ). Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. The gate driver output is specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of its bias supply when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=$ $\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\text { VGATE }=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}
$$

(see Figure 17.)


Figure 17. CS5156H Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is $\mathrm{RDS}_{\mathrm{ON}}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs and the Schottky diode may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\text { LLOAD }^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Schottky diode:

$$
\text { Power }=\text { VFORWARD } \times \text { ILOAD } \times(1-\text { duty cycle })
$$

Duty Cycle =
VOUT + VFORWARD
$\overline{\mathrm{V}_{\text {IN }}}+\mathrm{V}_{\text {FORWARD }}-($ ILOAD $\times$ RDSON OF SYNCH FET) $)$

## Off Time Capacitor (Coff)

The C CFF timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

When the $\mathrm{V}_{\text {FFB }}$ pin is less than 1.0 V , the current charging the $\mathrm{C}_{\mathrm{OFF}}$ capacitor is reduced. The extended off time can be calculated as follows:

$$
\text { TOFF }=\text { COFF } \times 24,242.5
$$

Off time will be determined by either the $\mathrm{T}_{\mathrm{OFF}}$ time, or the time out timer, whichever is longer.

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\mathrm{OFF}}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:
Period $=\frac{1}{\text { switching frequency }}$
"Droop" Resistor for Adaptive Voltage Positioning
Adaptive voltage positioning is used to reduce output voltage excursions during abrupt changes in load current. Regulator output voltage is offset +40 mV when the regulator is unloaded, and -40 mV at full load. This results in increased margin before encountering minimum and maximum transient voltage limits, allowing use of less capacitance on the regulator output (see Figure 9).
To implement adaptive voltage positioning, a "droop" resistor must be connected between the output inductor and output capacitors and load. This is normally implemented by a PC board trace of the following value:

$$
\text { RDROOP }=\frac{80 \mathrm{mV}}{\mathrm{I} \mathrm{MAX}}
$$

Adaptive voltage positioning can be disabled for improved DC regulation by connecting the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load using a separate, non-load current carrying circuit trace.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:
Thermal Impedance $=\frac{\text { TJUNCTION(MAX) }- \text { TAMBIENT }}{\text { Power }}$
A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 18. Filter Components


Figure 19. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. To implement adaptive voltage positioning, connect both slow and fast feedback pins $16\left(\mathrm{~V}_{\mathrm{FB}}\right)$ and 8 $\left(\mathrm{V}_{\mathrm{FFB}}\right)$ to the regulator output right at the inductor terminal. Connect inductor to the output capacitors via a trace with the following resistance:

$$
\text { RTRACE }=\frac{80 \mathrm{mV}}{\mathrm{I}_{\mathrm{MAX}}}
$$

This causes the output voltage to be +40 mV with no load, and -40 mV with a full load, improving regulator transient response. This trace must be wide enough to carry the full output current. (Typical trace is 1.0 inch long, 0.17 inch wide). Care should be taken to minimize any additional losses after the feedback connection point to maximize regulation.
7. If DC regulation is to be optimized (at the expense of degraded transient regulation), adaptive voltage positioning can be disabled by connecting to $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
8. Place 5.0 V input capacitors close to the switching MOSFET.

Route gate drive signals $\mathrm{V}_{\text {GATE }}$ (pin 10) with a trace that is a minimum of 0.025 inches wide.


Figure 20. Layout Guidelines


Figure 21. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter


Figure 22. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing
PACKAGE THERMAL DATA

| Parameter |  | SO-16 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5161, CS5161H

## CPU 5-Bit Synchronous Buck Controller

The CS5161/5161H are 5-bit synchronous dual N-Channel buck controllers designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. They operate using a proprietary control method which allows a 100 ns response time to load transients. The CS5161 is designed to operate over a $9-16 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V as the main supply for conversion.

The CS5161H operates from a 12 V input as the main supply for conversion using a discrete charge pump circuit to provide up to 20 V for $\mathrm{V}_{\mathrm{CC} 2}$ and high side gate drive.

The CS5161/5161H are specifically designed to power Pentium ${ }^{\circledR}$ III processors and other high performance core logic. They include the following features: on board 5-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5161/5161H are available in 16 pin surface mount packages.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5-Bit DAC
- Backward Compatible with CS515X Family
- 30 ns Gate Rise/Fall Times
- $1.0 \%$ DAC Accuracy
- $5.0 \mathrm{~V} \& 12 \mathrm{~V}$ Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- 50 ns FET Nonoverlap Time
- $V^{2 \mathrm{TM}}$ Control Topology
- Current Sharing
- Overvoltage Protection

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5161GD16 | SO-16 | 48 Units/Rail |
| CS5161GDR16 | SO-16 | 2500 Tape \& Reel |
| CS5161HGD16 | SO-16 | 48 Units/Rail |
| CS5161HGDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram,5.0 V to 1.5 V/15 A Core Logic Converter with 12 V Bias

## MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ | RMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\mathrm{CC} 2}(\mathrm{CS5161})$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| $\mathrm{V}_{\mathrm{CC} 2}(\mathrm{CS5161H})$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |

MAXIMUM RATINGS (continued)

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{FB}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\mathrm{OFF}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{FFB}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {IDO }}-\mathrm{V}_{\text {ID4 }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{GATE}(\mathrm{H})}(\mathrm{CS5161)}$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}(\mathrm{CS5161H})$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| LGnd | 0 V | 25 mA |
| PGnd | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5A} \mathrm{peak}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C}\right.$; CS5161: $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C}$; CS5161H: $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C}$;
$9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V}$; CS5161: 5.0 $\mathrm{V}<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}$; CS5161H: $5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}$; DAC Code: $\mathrm{V}_{\text {ID4 }}=\mathrm{V}_{\text {ID2 }}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\text {ID0 }}=1$; $\mathrm{V}_{\text {ID3 }}=0$; $\mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\operatorname{GATE}(H)}=1.0 \mathrm{nF} ; \mathrm{C}_{\text {OFF }}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Error Amplifier

| $V_{\text {FB }}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.3 | 1.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Open Loop Gain | $\begin{aligned} & 1.25 \mathrm{~V}<\mathrm{V}_{\mathrm{COMP}}, 4.0 \mathrm{~V} ; \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F} \\ & \text { Note? } \end{aligned}$ | - | 80 | - | dB |
| Unity Gain Bandwidth | $\mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F}$; Note 2 | - | 50 | - | kHz |
| COMP SINK Current | $\mathrm{V}_{\mathrm{COMP}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V} ; \mathrm{V}_{\text {SS }}>2.0 \mathrm{~V}$ | 30 | 60 | 120 | $\mu \mathrm{A}$ |
| COMP SOURCE Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP CLAMP Current | $\mathrm{V}_{\mathrm{COMP}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 4.0 | 4.3 | 5.0 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}$ | - | 1.0 | 1.15 | V |
| PSRR | $\begin{gathered} 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} @ 1.0 \mathrm{kHz} ; \\ \mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F} ; \text { Note } 2 \end{gathered}$ | - | 70 | - | dB |
| Transconductance | - | - | 33 | - | mmho |

## $\mathrm{V}_{\text {CC1 }}$ Monitor

| Start Threshold | Output switching | 8.70 | 9.05 | 9.40 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 8.55 | 8.90 | 9.25 | V |
| Hysteresis | Start-Stop | - | 150 | - | mV |

Soft Start (SS)

| Charge Time |  | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | (Charge Time /Pulse Period) $\times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C}\right.$; CS5161: $0^{\circ} \mathrm{C}<\mathrm{T}_{J}<+85^{\circ} \mathrm{C}$; CS5161H: $0^{\circ} \mathrm{C}<\mathrm{T}_{J}<+125^{\circ} \mathrm{C}$; $9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V}$; CS5161:5.0 V $<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}$; CS5161H: $5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}$; DAC Code: $\mathrm{V}_{\text {ID4 }}=\mathrm{V}_{\text {ID2 }}=\mathrm{V}_{\text {ID1 }}=\mathrm{V}_{\text {ID } 0}=1$; $\mathrm{V}_{\text {ID } 3}=0$; $\mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PWM Comparator |  |  |  |  |  |
| Transient Response | $\begin{aligned} & \mathrm{V}_{\mathrm{FFB}}=0 \text { to } 5.0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=9.0 \mathrm{~V} \text { to } 1.0 \mathrm{~V} ; \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 100 | 125 | ns |
| $\mathrm{V}_{\text {FFB }}$ Bias Current | $\mathrm{V}_{\text {FFB }}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

DAC

| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {IDO, }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID4 }}$ | 1.00 | 1.25 | 2.40 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Pull Up Resistance |  |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID4 }}$ | 25 | 50 | 110 | k $\Omega$ |
| Pull Up Voltage |  |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| ```Accuracy (all codes except 11111, 10110, 10101, 10100, 10011, 10010, 10001, 10000)``` |  |  |  |  | ```Measure V }\mp@subsup{\textrm{FB}}{\mathrm{ F COMP}}{ CS5161:25*'C \leq TJ < 85* C CS5161H:25``` | - | - | $\pm 1.0$ | \% |
| VID4 | $V_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $\mathrm{V}_{\text {ID }}$ |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | - | 1.2870 | 1.3000 | 1.3130 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.3365 | 1.3500 | 1.3635 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.3860 | 1.4000 | 1.4140 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.4355 | 1.4500 | 1.4645 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.4850 | 1.5000 | 1.5150 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.5345 | 1.5500 | 1.5655 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.5840 | 1.6000 | 1.6160 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.6335 | 1.6500 | 1.6665 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.6830 | 1.7000 | 1.7170 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.7325 | 1.7500 | 1.7675 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.7820 | 1.8000 | 1.8180 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.8315 | 1.8500 | 1.8685 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.8810 | 1.9000 | 1.9190 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.9305 | 1.9500 | 1.9695 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.9800 | 2.0000 | 2.0200 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.0295 | 2.0500 | 2.0705 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.0790 | 2.1000 | 2.1210 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.1780 | 2.2000 | 2.2220 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.2770 | 2.3000 | 2.3230 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.3760 | 2.4000 | 2.4240 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.4750 | 2.5000 | 2.5250 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.5740 | 2.6000 | 2.6260 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.6730 | 2.7000 | 2.7270 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.7720 | 2.8000 | 2.8280 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.8420 | 2.9000 | 2.9580 | V |
| 1 | 0 | 1 | 0 | 1 | - | 2.9400 | 3.0000 | 3.0600 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C}\right.$; CS5161: $0^{\circ} \mathrm{C}<\mathrm{T}_{J}<+85^{\circ} \mathrm{C}$; CS5161H: $0^{\circ} \mathrm{C}<\mathrm{T}_{J}<+125^{\circ} \mathrm{C}$; $9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V}$; CS5161: 5.0 $\mathrm{V}<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}$; CS5161H: $5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}$; DAC Code: $\mathrm{V}_{\text {ID4 }}=\mathrm{V}_{\text {ID2 }}=\mathrm{V}_{\text {ID } 1}=\mathrm{V}_{\text {ID } 0}=1 ; \mathrm{V}_{\text {ID3 }}=0$; $\mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |  |  |  |  |  |  |  |  | Test Conditions | Min |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC | Map | Max | Unit |  |  |  |  |  |  |  |
| 1 | 0 | 1 | 0 | 0 | - | 3.0380 | 3.1000 | 3.1620 | V |  |
| 1 | 0 | 0 | 1 | 1 | - | 3.1360 | 3.2000 | 3.2640 | V |  |
| 1 | 0 | 0 | 1 | 0 | - | 3.2340 | 3.3000 | 3.3660 | V |  |
| 1 | 0 | 0 | 0 | 1 | - | 3.3320 | 3.4000 | 3.4680 | V |  |
| 1 | 0 | 0 | 0 | 0 | - | 3.4300 | 3.5000 | 3.5700 | V |  |

$\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$

| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1}-\mathrm{V}_{\mathrm{GATE}}(\mathrm{L}) ; \mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}}(\mathrm{H})$ | - | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Out SINK Sat at 100 mA |  | - | 1.0 | 1.5 | V |
| Out Rise Time | $\left.\begin{array}{rl} 1.0 & \mathrm{~V} \end{array}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}\right)$ | - | 30 | 50 | ns |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})} \\ & \\ & >1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to $2.0 \mathrm{~V}_{\text {; }} \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ <br> $\mathrm{V}_{\text {GATE(L) }}$ rising to 2.0 V | 20 | 50 | 90 | ns |
| Delay $\mathrm{V}_{\text {GATE }(\mathrm{L})}$ to $\mathrm{V}_{\text {GATE(H) }}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to $2.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ <br> $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ rising to 2.0 V | 20 | 50 | 90 | ns |
| $\mathrm{V}_{\text {GATE(H), }} \mathrm{V}_{\text {GATE(L) }}$ Resistance | Resistor to LGnd. Note 3 | 20 | 50 | 100 | k $\Omega$ |
| $\mathrm{V}_{\text {GATE(H), }} \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGnd to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ @ 10 mA ; LGnd to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} @ 10 \mathrm{~mA}$ | - | 600 | 800 | mV |

## Supply Current

| $\mathrm{I}_{\mathrm{CC} 1}$ No Switching | - | - | 9.5 | 14.5 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{CC} 2}$ No Switching | - | - | 2.0 | 3.5 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 1}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 9.0 | 14 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 2}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.5 | 5.5 | mA |

## Coff

| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | $\mathrm{C}_{\mathrm{OFF}}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |

## Time Out Timer

| Time Out Time | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ;$ <br> Record $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ Pulse High Duration | 10 | 30 | 65 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 70 | $\%$ |

3. Guaranteed by design, not $100 \%$ tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| 16 Lead SO Narrow |  |  |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID0 }}-\mathrm{V}_{\text {ID4 }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is High (logic one), the DAC range is 2.10 V to 3.50 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is Low (logic zero), the DAC range is 1.30 V to 2.05 V with 50 mV increments. $\mathrm{V}_{\text {ID0 }}-\mathrm{V}_{\text {ID4 }}$ select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.2440 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGnd in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | CofF | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $V_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE }}(\mathrm{H})$ | High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ from being in high state simultaneously. |
| 11 | PGnd | High current ground for the IC. The MOSFET drivers are referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 1.5 A peak switching current. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC and low side gate driver. |
| 14 | LGnd | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $\mathrm{V}_{\mathrm{FB}}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## V $^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. V ${ }^{2}$ Control Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5161/5161H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the C CoFF capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu \mathrm{~s}$ timer, minimizing stress to the power components.

## Programmable Output

The CS5161/5161H is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.10 V to 3.50 V in 100 mV steps, the second is 1.30 V to 2.05 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5161/5161H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 9.05 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the $\operatorname{GATE}(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.
When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C CoFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.
The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP

## CS5161, CS5161H

capacitor charging to its final value. Its voltage is limited by the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input (VCC1 and VCC2) (5.0 V/div.)
Trace 4-5.0 V Input (1.0 V/div.)
Figure 4. CS5161/5161H Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1- Regulator Output Voltage ( $1.0 \mathrm{~V} /$ div.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5161/5161H Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1-Regulator Output Voltage ( $5.0 \mathrm{~V} /$ div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 6. CS5161/5161H Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C OFF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1- Regulator Output Voltage ( $10 \mathrm{mV} /$ div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 7. CS5161/5161H Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=0.5 \mathrm{~A}$ (Light Load)


Trace 1- Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 8. CS5161/5161H Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=13 \mathrm{~A}$ (Heavy Load)

## Transient Response

The CS5161/5161H V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Trace 2- Regulator Output Voltage (output set for $1.55 \mathrm{~V}, 20 \mathrm{mV} /$ div.)
Figure 9. CS5161/5161H Pentium ${ }^{\circledR}$ III Converter Output Voltage Response to a 12 A Load Pulse.


Trace 1- Inductor Switching Node (5.0 V/div.)
Trace 2- Regulator Output Voltage (output set for $1.55 \mathrm{~V}, 20 \mathrm{mV} /$ div.)
Figure 10. CS5161/5161H Pentium ${ }^{\circledR}$ III Converter Output Voltage Response to a 0 to 12 A Load Increase


Figure 11. CS5161/5161H Pentium ${ }^{\circledR}$ III Converter Output Voltage Response to a 12 to 0 A Load Decrease

## PROTECTION AND MONITORING FEATURES

## $V_{\text {CC1 }}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 8.70 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 8.55 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\mathrm{FFB}}$ low comparator sets the FAULT
latch. This causes the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=3.3 \%)$, while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.) Trace 3- Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5161/5161H Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. CS5161/5161H Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.


Figure 14. CS5161/5161H OVP Response to an Input-to-Output Short Circuit by Immediately
Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Figure 15. CS5161/5161H OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\text {FFB }}$ pin low, emulating a short circuit condition.


Figure 16. Implementing Shutdown with the CS5161/5161H

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power Good. }}$


Figure 17. Implementing Power Good with the CS5161/5161H


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) (10 V/div.)
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 18. CS5161/5161H During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Slope Compensation

The $\mathrm{V}^{2}$ control method uses a ramp signal, generated by the ESR of the output capacitors, that is proportional to the ripple current through the inductor. To maintain regulation, the $\mathrm{V}^{2}$ control loop monitors this ramp signal, through the PWM comparator, and terminates the switch on-time.
The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope presented to the PWM comparator, due to the very low ESR, can lead to pulse width jitter and variation caused by both random or synchronous noise.

Adding slope compensation to the control loop, avoids erratic operation of the PWM circuit, particularly at lower duty cycles and higher frequencies, where there is not enough ramp signal, and provides a more stable switchpoint.
The scheme that prevents that switching noise prematurely triggers the PWM circuit consists of adding a positive voltage slope to the output of the Error Amplifier (COMP pin) during an off-time cycle.

The circuit that implements this function is shown in Figure 19.


Figure 19. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of each On-Time Cycle
The ramp waveform is generated through a small RC filter that provides the proper voltage ramp at the beginning of each on-time cycle. The resistors R1 and R2 in the circuit of Figure 14 form a voltage divider from the GATE(L) output, superimposing a small artificial ramp on the output of the error amplifier. It is important that the series combination $\mathrm{R} 1 / \mathrm{R} 2$ is high enough in resistance not to load down and negatively affect the slew rate on the GATE(L) pin.

## Selecting External Components

The CS5161/5161H can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\operatorname{VGATE}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{~L})=12 \mathrm{~V}
$$

(see Figure 20.)


Figure 20. CS5161/5161H Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is RDS $_{\text {ON }}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\mathrm{ILOAD}^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\mathrm{I}_{\mathrm{LOAD}}{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =

$$
\frac{\text { VOUT }+(\text { LLOAD } \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\text { VIN }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET }) \\
-(\text { LLOAD } \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (COFF)

The C CFF timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\text {OFF }}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=V_{B D} \times I$ LOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5161/5161H demonstration board as shown in Figure 8;

$$
\text { Power }=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}
$$

This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

Thermal Impedance $=\frac{\text { TJUNCTION(MAX) }- \text { TAMBIENT }}{\text { Power }}$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 21. Filter Components


Figure 22. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGnd).
2. Connect pin 11 (PGnd) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGnd).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGnd).
6. Connect the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
7. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.
Route gate drive signals $\mathrm{V}_{\text {GATE(H) }}$ (pin 10) and $\mathrm{V}_{\text {GATE(L) }}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.


Figure 23. Layout Guidelines

## CS5161, CS5161H

## ADDITIONAL APPLICATION DIAGRAMS



Figure 24. 12 V to 3.3 V/10 A Converter with Remote Sense and Current Sharing


Figure 25. 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias.

## CS5161, CS5161H

## ADDITIONAL APPLICATION DIAGRAMS



Figure 26. Pentium ${ }^{\circledR}$ III Converter with Slope Compensation and Adaptive Voltage Positioning PACKAGE THERMAL DATA

| Parameter |  | 16 Lead SO Narrow | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5165H

## 5-Bit Synchronous CPU Buck Controller

The CS5156H synchronous 5-bit NFET buck controller is optimized to manage the power of the next generation Pentium II processors. It's $V^{2 \mathrm{TM}}$ control architecture delivers the fastest transient response ( 100 ns ), and best overall voltage regulation in the industry today. It's feature rich design gives end users the maximum flexibility to implement the best price/performance solutions for their end products.

The CS5156H has been carefully crafted to maximize performance and protect the processor during operation. It has a 5-bit DAC on board that holds a $\pm 1.0 \%$ tolerance over temperature. Its on board programmable Soft Start insures a control start up, and the FET nonoverlap circuitry ensures that both FETs do not conduct simultaneously.

The on board oscillator can be programmed up to 1.0 MHz to give the designer maximum flexibility in choosing external components and setting systems costs.

The CS5156H protects the processor during potentially catastrophic events like overvoltage (OVP) and short circuit. The OVP feature is part of the $\mathrm{V}^{2}$ architecture and does not require any additional components. During short circuit, the controller pulses the MOSFETs in a "hiccup" mode ( $3.0 \%$ duty cycle) until the fault is removed. With this method, the MOSFETs do not overheat or self destruct.

The CS5156H is designed for use in both single processor desktop and multiprocessor workstation and server applications. The IC can be powered from either single or dual $5.0 \mathrm{~V}, 12 \mathrm{~V}$ power supplies. The CS5156H's current sharing capability allows the designer to build multiple parallel and redundant power solutions for multiprocessor systems.

The CS5156H contains other control and protection features such as Power Good, ENABLE, and adaptive voltage positioning. It is available in a 16 lead SOIC wide body package.

## Features

- $\mathrm{V}^{2}$ Control Topology
- 100 ns Controller Transient Response
- Excess of 1.0 MHz Operation
- 5-Bit DAC with $1.0 \%$ Tolerance
- Power Good Output With Internal Delay
- Enable Input Provides Micropower Shutdown Mode
- 5.0 V \& 12 V Operation Using Either Dual or Single Supplies
- Adaptive Voltage Positioning
- Remote Sense Capability
- Current Sharing Capability
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- Hiccup Mode Short Circuit Protection
- Overvoltage Protection (OVP)
- Programmable Soft Start
- 150 ns PWM Blanking
- 65 ns FET Nonoverlap Time
- 40 ns Gate Rise and Fall Times (3.3 nF Load)


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5165HGDW16 | SO-16L | 46 Units/Rail |
| CS5165HGDWR16 | SO-16L | 1000 Tape \& Reel |

## CS5165H



Figure 1. Application Diagram, 5.0 V to 2.8 V @ 14.2 A for 300 MHz Pentium II

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {Source }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\text {CC }}$ | 20 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | 1.5 A peak, 200 mA DC |
| Soft Start Capacitor | SS | 6.0 V | -0.3 V | $200 \mu \mathrm{~A}$ | $10 \mu \mathrm{~A}$ |
| Compensation Capacitor | COMP | 6.0 V | -0.3 V | 10 mA | 1.0 mA |
| Voltage Feedback Input | $\mathrm{V}_{\text {FB }}$ | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | $10 \mu \mathrm{~A}$ |
| Off-Time Capacitor | C $_{\text {OFF }}$ | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| Voltage ID DAC Inputs | $\mathrm{V}_{\text {IDo }}-\mathrm{V}_{\text {ID4 }}$ | 6.0 V | -0.3 V | 1.0 mA | $10 \mu \mathrm{~A}$ |
| High-Side FET Driver | GATE(H) | 20 V | -0.3 V | 1.5 A peak, 200 mA DC | 1.5 A peak, 200 mA DC |
| Low-Side FET Driver | GATE(L) | 20 V | -0.3 V | 1.5 A peak, 200 mA DC | 1.5 A peak, 200 mA DC |
| Enable Input | ENABLE | 6.0 V | -0.3 V | $100 \mu \mathrm{~A}$ | 1.0 mA |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | 30 mA |
| Power Ground | PGND | 0 V | 0 V | 1.5 A peak, 200 mA DC | $\mathrm{N} / \mathrm{A}$ |
| Logic Ground | LGND | 0 V | 0 V | 100 mA | $\mathrm{~N} / \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ; 2.8\right.$ DAC Code: $\left(\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{I D 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0\right) ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ Supply Current |  |  |  |  |  |
| Operating | $1.0 \vee<V_{F B}<V_{\text {DAC }}(\max$ on-time) <br> No Loads on GATE(H) and GATE(L) | - | 12 | 20 | mA |

$\mathrm{V}_{\mathrm{CC}}$ Monitor

| Start Threshold | GATE $(\mathrm{H})$ switching | 3.75 | 3.95 | 4.15 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | GATE $(\mathrm{H})$ not switching | 3.65 | 3.87 | 4.05 | V |
| Hysteresis | Start-Stop | - | 80 | - | mV |

## Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| COMP Source Current | $\mathrm{COMP}=1.2 \mathrm{~V}$ to $3.6 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| COMP CLAMP Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$, Adjust COMP voltage for Comp <br> current $=50 \mu \mathrm{~A}$ | 0.85 | 1.0 | 1.15 | V |
| COMP Clamp Current | $\mathrm{COMP}=0 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP Sink Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}>2.5 \mathrm{~V}$ | 180 | 400 | 800 | $\mu \mathrm{~A}$ |
| Open Loop Gain | Note 2 | 50 | 60 | - | dB |
| Unity Gain Bandwidth | Note 2 | 0.5 | 2.0 | - | MHz |
| PSRR @ 1.0 kHz | Note 2 | 60 | 85 | - | dB |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ; 2.8\right.$ DAC Code: $\left(\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{I D 2}=\mathrm{V}_{\text {ID1 }}=\mathrm{V}_{\text {ID0 }}=1 ; \mathrm{V}_{\text {ID3 }}=0\right) ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATE(H) and GATE(L) |  |  |  |  |  |
| High Voltage at 100 mA | Measure V ${ }_{\text {CC }}$ - GATE | - | 1.2 | 2.0 | V |
| Low Voltage at 100 mA | Measure GATE | - | 1.0 | 1.5 | V |
| Rise Time | 1.6 V < GATE < ( $\left.\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right), 8 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$ | - | 40 | 80 | ns |
| Fall Time | $\left(\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right)>$ GATE $>1.6 \mathrm{~V}, 8 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$ | - | 40 | 80 | ns |
| GATE(H) to GATE(L) Delay | $\begin{aligned} & \operatorname{GATE}(\mathrm{H})<2.0 \mathrm{~V} \text {; GATE }(\mathrm{L})>2.0 \mathrm{~V}, \\ & 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} \end{aligned}$ | 30 | 65 | 100 | ns |
| GATE(L) to GATE(H) Delay | $\begin{aligned} & \text { GATE }(\mathrm{L})<2.0 \mathrm{~V} \text {; GATE }(\mathrm{H})>2.0 \mathrm{~V}, \\ & 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} \end{aligned}$ | 30 | 65 | 100 | ns |
| GATE pull-down | Resistor to PGND, Note 3 | 20 | 50 | 115 | k $\Omega$ |

Fault Protection

| SS Charge Time | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| SS Pulse Period | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 25 | 100 | 200 | ms |
| SS Duty Cycle | $($ Charge Time/Period $) \times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| SS COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$; $\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V}$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\mathrm{FB}}$ Low Comparator | Increase $\mathrm{V}_{\mathrm{FB}}$ till no SS pulsing and normal Off-time | 0.9 | 1.0 | 1.1 | V |

PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FB}}=1.2$ to 5.0 V .500 ns after $\operatorname{GATE}(\mathrm{H})$ <br> (after Blanking time) to $\operatorname{GATE}(\mathrm{H})=\left(\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}\right)$ <br> to $1.0 \mathrm{~V}, 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$ | - | 100 | 150 | ns |
| :--- | :--- | :--- | :--- | :--- | :---: |
| Minimum Pulse Width <br> (Blanking Time) | Drive $\mathrm{V}_{\mathrm{FB}} 1.2$ to 5.0 V upon $\operatorname{GATE}(H)$ rising edge <br> ( $>\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}$, measure $\operatorname{GATE}(H)$ pulse <br> width, $8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$ | 50 | 150 | 250 | ns |

## Coff

| Normal Off-Time | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 1.0 | 1.6 | 2.3 | $\mu \mathrm{~s}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Extended Off-Time | $\mathrm{V}_{\mathrm{SS}}=\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 5.0 | 8.0 | 12.0 | $\mu \mathrm{~s}$ |

Time-Out Timer

| Time-Out Time | $\mathrm{V}_{\mathrm{FB}}=2.7$ V, Measure GATE(H) Pulse Width | 10 | 30 | 50 | $\mu \mathrm{~s}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Fault Duty Cycle | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 30 | 50 | 70 | $\%$ |

Enable Input

| ENABLE Threshold | GATE(H) Switching | 0.8 | 1.15 | 1.30 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Shutdown delay (Note 3) | ENABLE-to-GATE(H) < 2.0 V | - | 3.0 | - | $\mu \mathrm{s}$ |
| Pull-up Current | ENABLE $=0 \mathrm{~V}$ | 3.0 | 7.0 | 15 | $\mu \mathrm{~A}$ |
| Pull-up Voltage | No load on ENABLE pin | 1.30 | 1.8 | 3.0 | V |
| Input Resistance | ENABLE $=5.0 \mathrm{~V}, \mathrm{R}=\left(5.0 \mathrm{~V}-\mathrm{V}_{\text {PULLUP }}\right) / I_{\text {ENABLE }}$ | 10 | 20 | 50 | $\mathrm{k} \Omega$ |

## Power Good Output

| Low to High Delay | $\mathrm{V}_{\mathrm{FB}}=\left(0.8 \times \mathrm{V}_{\mathrm{DAC}}\right)$ to $\mathrm{V}_{\mathrm{DAC}}$ | 30 | 65 | 110 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| High to Low Delay | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{DAC}}$ to $\left(0.8 \times \mathrm{V}_{\mathrm{DAC}}\right)$ | 30 | 75 | 120 | $\mu \mathrm{~s}$ |
| Output Low Voltage | $\mathrm{V}_{\mathrm{FB}}=2.4 \mathrm{~V}, \mathrm{I}_{\mathrm{PWRGD}}=500 \mu \mathrm{~A}$ | - | 0.2 | 0.3 | V |
| Sink Current Limit | $\mathrm{V}_{\mathrm{FB}}=2.4 \mathrm{~V}, \mathrm{PWRGD}=1.0 \mathrm{~V}$ | 0.5 | 4.0 | 15.0 | mA |

3. Guaranteed by design, not $100 \%$ tested in production.

## CS5165H

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ; 2.8\right.$ DAC Code: $\left(\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0\right) ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Voltage Identification DAC

| Accuracy (all codes except 11111) |  |  |  |  | Measure $\mathrm{V}_{\text {FB }}=\mathrm{COMP}\left(\mathrm{C}_{\text {OFF }}=0 \mathrm{~V}\right)$ | -1.0 | - | +1.0 | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {ID } 4}$ | VID3 | VID2 | $\mathrm{V}_{\text {ID } 1}$ | VIDO |  |  |  |  |  |
| 1 | 0 | 0 | 0 | 0 | - | 3.505 | 3.540 | 3.575 | V |
| 1 | 0 | 0 | 0 | 1 | - | 3.406 | 3.440 | 3.474 | V |
| 1 | 0 | 0 | 1 | 0 | - | 3.307 | 3.340 | 3.373 | V |
| 1 | 0 | 0 | 1 | 1 | - | 3.208 | 3.240 | 3.272 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.109 | 3.140 | 3.171 | V |
| 1 | 0 | 1 | 0 | 1 | - | 3.010 | 3.040 | 3.070 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.911 | 2.940 | 2.969 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.812 | 2.840 | 2.868 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.713 | 2.740 | 2.767 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.614 | 2.640 | 2.666 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.515 | 2.540 | 2.565 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.416 | 2.440 | 2.464 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.317 | 2.340 | 2.363 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.218 | 2.240 | 2.262 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.119 | 2.140 | 2.161 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.069 | 2.090 | 2.111 | V |
| 0 | 0 | 0 | 0 | 1 | - | 2.020 | 2.040 | 2.060 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.970 | 1.990 | 2.010 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.921 | 1.940 | 1.959 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.871 | 1.890 | 1.909 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.822 | 1.840 | 1.858 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.772 | 1.790 | 1.808 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.723 | 1.740 | 1.757 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.673 | 1.690 | 1.707 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.624 | 1.640 | 1.656 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.574 | 1.590 | 1.606 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.525 | 1.540 | 1.555 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.475 | 1.490 | 1.505 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.426 | 1.440 | 1.455 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.376 | 1.390 | 1.405 | V |
| 0 | 1 | 1 | 1 | 1 | - | 1.327 | 1.340 | 1.353 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.223 | 1.247 | 1.273 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 1.000 | 1.250 | 2.400 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\mathrm{ID} 3}, \mathrm{~V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID0 }}$ | 25 | 50 | 100 | k $\Omega$ |
| Input Pull-up Voltage |  |  |  |  |  | 4.85 | 5.00 | 5.15 | V |

## CS5165H

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; 2.8\right.$ DAC Code: $\left(\mathrm{V}_{\text {ID4 }}=\mathrm{V}_{\text {ID2 }}=\mathrm{V}_{\text {ID1 }}=\mathrm{V}_{\text {ID0 }}=1 ; \mathrm{V}_{\text {ID3 }}=0\right) ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified. $)$

| Threshold Accuracy | Lower Threshold |  |  | Upper Threshold |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min | Typ | Max | Min | Typ | Max | Unit |

## DAC CODE

| \% of Nominal DAC Output |  |  |  |  | -12 | -8.5 | -5.0 | 5.0 | 8.5 | 12 | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {ID } 4}$ | $V_{\text {ID } 3}$ | $\mathrm{V}_{\text {ID2 }}$ | VID1 | VIDO |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 0 | 0 | 3.115 | 3.239 | 3.363 | 3.717 | 3.841 | 3.965 | V |
| 1 | 0 | 0 | 0 | 1 | 3.027 | 3.148 | 3.268 | 3.612 | 3.732 | 3.853 | V |
| 1 | 0 | 0 | 1 | 0 | 2.939 | 3.056 | 3.173 | 3.507 | 3.624 | 3.741 | V |
| 1 | 0 | 0 | 1 | 1 | 2.851 | 2.965 | 3.078 | 3.402 | 3.515 | 3.629 | V |
| 1 | 0 | 1 | 0 | 0 | 2.763 | 2.873 | 2.983 | 3.297 | 3.407 | 3.517 | V |
| 1 | 0 | 1 | 0 | 1 | 2.675 | 2.782 | 2.888 | 3.192 | 3.298 | 3.405 | V |
| 1 | 0 | 1 | 1 | 0 | 2.587 | 2.690 | 2.793 | 3.087 | 3.190 | 3.293 | V |
| 1 | 0 | 1 | 1 | 1 | 2.499 | 2.599 | 2.698 | 2.982 | 3.081 | 3.181 | V |
| 1 | 1 | 0 | 0 | 0 | 2.411 | 2.507 | 2.603 | 2.877 | 2.973 | 3.069 | V |
| 1 | 1 | 0 | 0 | 1 | 2.323 | 2.416 | 2.508 | 2.772 | 2.864 | 2.957 | V |
| 1 | 1 | 0 | 1 | 0 | 2.235 | 2.324 | 2.413 | 2.667 | 2.756 | 2.845 | V |
| 1 | 1 | 0 | 1 | 1 | 2.147 | 2.233 | 2.318 | 2.562 | 2.647 | 2.733 | V |
| 1 | 1 | 1 | 0 | 0 | 2.059 | 2.141 | 2.223 | 2.457 | 2.539 | 2.621 | V |
| 1 | 1 | 1 | 0 | 1 | 1.971 | 2.050 | 2.128 | 2.352 | 2.430 | 2.509 | V |
| 1 | 1 | 1 | 1 | 0 | 1.883 | 1.958 | 2.033 | 2.250 | 2.322 | 2.397 | V |
| 0 | 0 | 0 | 0 | 0 | 1.839 | 1.912 | 1.986 | 2.195 | 2.268 | 2.341 | V |
| 0 | 0 | 0 | 0 | 1 | 1.795 | 1.867 | 1.938 | 2.142 | 2.213 | 2.285 | V |
| 0 | 0 | 0 | 1 | 0 | 1.751 | 1.821 | 1.810 | 2.090 | 2.159 | 2.229 | V |
| 0 | 0 | 0 | 1 | 1 | 1.707 | 1.775 | 1.843 | 2.037 | 2.105 | 2.173 | V |
| 0 | 0 | 1 | 0 | 0 | 1.663 | 1.729 | 1.796 | 1.985 | 2.051 | 2.117 | V |
| 0 | 0 | 1 | 0 | 1 | 1.619 | 1.684 | 1.748 | 1.932 | 1.996 | 2.061 | V |
| 0 | 0 | 1 | 1 | 0 | 1.575 | 1.638 | 1.701 | 1.880 | 1.942 | 2.005 | V |
| 0 | 0 | 1 | 1 | 1 | 1.531 | 1.592 | 1.653 | 1.827 | 1.888 | 1.949 | V |
| 0 | 1 | 0 | 0 | 0 | 1.487 | 1.546 | 1.606 | 1.775 | 1.834 | 1.893 | V |
| 0 | 1 | 0 | 0 | 1 | 1.443 | 1.501 | 1.558 | 1.722 | 1.779 | 1.837 | V |
| 0 | 1 | 0 | 1 | 0 | 1.399 | 1.455 | 1.511 | 1.670 | 1.725 | 1.781 | V |
| 0 | 1 | 0 | 1 | 1 | 1.355 | 1.409 | 1.463 | 1.617 | 1.671 | 1.724 | V |
| 0 | 1 | 1 | 0 | 0 | 1.311 | 1.363 | 1.416 | 1.565 | 1.617 | 1.669 | V |
| 0 | 1 | 1 | 0 | 1 | 1.267 | 1.318 | 1.368 | 1.512 | 1.562 | 1.613 | V |
| 0 | 1 | 1 | 1 | 0 | 1.223 | 1.272 | 1.321 | 1.460 | 1.508 | 1.557 | V |
| 0 | 1 | 1 | 1 | 1 | 1.179 | 1.226 | 1.273 | 1.407 | 1.454 | 1.501 | V |
| 1 | 1 | 1 | 1 | 1 | 1.097 | 1.141 | 1.185 | 1.309 | 1.353 | 1.397 | V |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-16L | PIN SYMBOL | FUNCTION |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID0 }}-\mathrm{V}_{\text {ID4 }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is high (logic one), the Error Amp reference range is 2.14 V to 3.45 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is low (logic zero), the Error Amp reference voltage 1.34 V to 2.09 V with 50 mV increments. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND sets the Soft Start and fault timing. |
| 7 | COFF | Off-Time Capacitor Pin. A capacitor from this pin to LGND sets both the normal and extended off time. |
| 8 | ENABLE | Output Enable Input. This pin is internally pulled up to 1.8 V . A logic Low ( $<0.8 \mathrm{~V}$ ) on this pin disables operation and places the CS5156H into a low current sleep mode. |
| 9 | $\mathrm{V}_{\mathrm{CC}}$ | Input Power Supply Pin. |
| 10 | GATE(H) | High Side Switch FET driver pin. |
| 11 | PGND | High current ground for the GATE(H) and GATE(L) pins. |
| 12 | GATE(L) | Low Side Synchronous FET driver pin. |
| 13 | PWRGD | Power Good Output. Open collector output drives low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. Active when ENABLE input is low. |
| 14 | LGND | Reference ground. All control circuits are referenced to this pin. |
| 15 | COMP | Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation. |
| 16 | $\mathrm{V}_{\mathrm{FB}}$ | Error Amp, PWM Comparator, and Low $\mathrm{V}_{\text {FB }}$ Comparator feedback input. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. GATE(L) Risetime vs. Load Capacitance


Figure 4. GATE(H) Risetime vs. Load Capacitance


Figure 6. DAC Output Voltage vs. Temperature, DAC Code $=10111, V_{\text {CC }}=12 \mathrm{~V}$


DAC Output Voltage Setting (V)
Figure 7. Percent Output Error vs. DAC Voltage Setting, $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{ID} 4}=0$


DAC Output Voltage Setting (V)
Figure 8. Percent Output Error vs. DAC Output Voltage Setting $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{ID} 4}=1$

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 9. $\mathbf{V}^{2}$ Control Diagram
The $\mathrm{V}^{2}$ control method is illustrated in Figure 9. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop.

The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.
Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $V^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5156H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the C CFF capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.
Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.
Switch on time is limited by an internal $30 \mu \mathrm{~s}$ (typical) timer, minimizing stress to the power components.

## Programmable Output

The CS5156H is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.14 V to 3.54 V in 100 mV steps, the second is 1.34 V to 2.09 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5156H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ pin, as in traditional controllers. The CS5156H is specifically designed to meet or exceed Intel's Pentium II specifications.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC}}$ supply pin exceeds the 3.95 V monitor threshold, the Soft Start and GATE pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC}}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the CofF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by the Soft Start COMP clamp and the voltage on the Soft Start pin.

## Power Supply Sequencing

The CS5156H offers inherent protection from undefined start up conditions, regardless of the 12 V and 5.0 V supply power up sequencing. The turn on slew rates of the 12 V and 5.0 V power supplies can be varied over wide ranges without affecting the output voltage or causing detrimental effects to the buck regulator.


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC}}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (1.0 V/div.)
Figure 10. Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Figure 11. Demonstration Board Startup Waveforms


Trace 1- Regulator Output Voltage ( $1.0 \mathrm{~V} /$ div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 12. Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C CofF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working and the ESR of the output capacitors (see Figures 13 and 14).


Figure 13. Normal Operation Showing Output Inductor Ripple Current and Output Voltage Ripple, 0.5 A Load, $\mathrm{V}_{\text {OUT }}=+2.84 \mathrm{~V}(\mathrm{DAC}=10111)$


Trace 1- GATE(H) (10 V/div.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Trace 3- Output Inductor Ripple Current (2.0 A/div.)
Trace 4-V VUT ripple ( $20 \mathrm{mV} /$ div.)
Figure 14. Normal Operation Showing Output Inductor Ripple Current and Output Voltage Ripple, $\mathrm{I}_{\text {LOAD }}=14 \mathrm{~A}, \mathrm{~V}_{\text {OUT }}=+2.84 \mathrm{~V}(\mathrm{DAC}=10111)$

## Transient Response

The CS5156H V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "Adaptive Voltage Positioning". This technique pre-positions the output capacitors voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifiers reference voltage to be targeted +40 mV high without compromising DC accuracy. A "Droop Resistor", implemented through a PC board trace, connects the Error Amps feedback pin $\left(\mathrm{V}_{\mathrm{FB}}\right)$ to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +40 mV offset. When the full load current is delivered, an 80 mV drop is developed across this resistor. This results in output voltage being offset -40 mV low.

The result of Adaptive Voltage Positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load
current suddenly increases from its minimum level, the output capacitor is pre-positioned +40 mV . Conversely, when load current suddenly decreases from its maximum level, the output capacitor is pre-positioned -40 mV (see Figures 15, 16, and 17). For best Transient Response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the Maximum On-Time is exceeded while responding to a sudden increase in Load current, a normal off-time occurs to prevent saturation of the output inductor.


Trace 3-Load Current (5.0 A/10 mV/div.)
Trace 4- V OUT ( $100 \mathrm{mV} / \mathrm{div}$.)
Figure 15. Output Voltage Transient Response to a 14 A Load Pulse, $\mathrm{V}_{\text {OUT }}=+2.84 \mathrm{~V}(\mathrm{DAC}=10111)$


Figure 16. Output Voltage Transient Response to a 14 A Load Step, $\mathrm{V}_{\text {OUT }}=+2.84 \mathrm{~V}(\mathrm{DAC}=10111)$


Figure 17. Output Voltage Transient Response to a 14 A Load Turn-Off, $\mathrm{V}_{\text {OUT }}=+2.84 \mathrm{~V}(\mathrm{DAC}=10111)$

## PROTECTION AND MONITORING FEATURES

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs the $\mathrm{V}_{\mathrm{FB}}$ low comparator sets the FAULT latch. This causes the top FET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).
This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 18 and 19).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3-Soft Start Timing Capacitor ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 18. Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Trace 4-5.0 V from PC Power Supply ( $2.0 \mathrm{~V} /$ div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 19. Demonstration Board Startup with Regulator Output Shorted To Ground

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 20 and 21 ). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to
implement the OVP function. If a dedicated OVP output is required, it can be implemented using the circuit in Figure 22. In this figure the OVP signal will go high (overvoltage condition), if the output voltage ( $\mathrm{V}_{\mathrm{CORE}}$ ) exceeds $20 \%$ of the voltage set by the particular DAC code and provided that PWRGD is low. It is also required that the overvoltage condition be present for at least the PWRGD delay time for the OVP signal to be activated. The resistor values shown in Figure 22 are for $\mathrm{V}_{\mathrm{DAC}}=+2.8 \mathrm{~V}(\mathrm{DAC}=10111)$. The $\mathrm{V}_{\mathrm{OVP}}$ (overvoltage trip-point) can be set using the following equation:

$$
\mathrm{V}_{\mathrm{OVP}}=\mathrm{V}_{\mathrm{BEQ}}\left(1+\frac{\mathrm{R} 2}{\mathrm{R1}}\right)
$$



Figure 20. OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Figure 21. OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground


Figure 22. Circuit To Implement A Dedicated OVP Output Using The CS5156H

## Output Enable Circuit

The Enable pin (pin 8) is used to enable or disable the regulator output voltage, and is consistent with TTL DC specifications. It is internally pulled-up. If pulled low (below 0.8 V ), the output voltage is disabled. At the same time the Power Good and Soft Start pins are pulled low, so that when normal operation resumes power-up of the CS5156H goes through the Soft Start sequence. Upon pulling the Enable pin low, the internal IC bias is completely shut off, resulting in total shutdown of the Controller IC.

## Power Good Circuit

The Power Good pin (pin 13) is an open-collector signal consistent with TTL DC specifications. It is externally pulled-up, and is pulled low (below 0.3 V ) when the regulator output voltage typically exceeds $\pm 8.5 \%$ of the
nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is $\pm 12 \%$.


Trace 2- PWRGD (2.0 V/div.)
Trace 4- V
Figure 23. PWRGD Signal Becomes Logic High as $V_{\text {OUT }}$ Enters -8.5\% of Lower PWRGD Threshold, $\mathrm{V}_{\text {OUT }}=+\mathbf{2 . 8 4} \mathrm{V}(\mathrm{DAC}=10111)$


Figure 24. Power Good Response to an Out of Regulation Condition
Figure 24 shows the relationship between the regulated output voltage $\mathrm{V}_{\mathrm{FB}}$ and the Power Good signal. To prevent Power Good from interrupting the CPU unnecessarily, the CS5156H has a built-in delay to prevent noise at the $\mathrm{V}_{\mathrm{FB}}$ pin from toggling Power Good. The internal time delay is designed to take about $75 \mu$ s for Power Good to go low and $65 \mu$ s for it to recover. This allows the Power Good signal to be completely insensitive to out of regulation conditions that are present for a duration less than the built in delay (see Figure 25).

It is therefore required that the output voltage attains an out of regulation or in regulation level for at least the built-in delay time duration before the Power Good signal can change state.


Trace 2- PWRGD (2.0 V/div.)
Trace 4- VFB ( $1.0 \mathrm{~V} /$ div.)
Figure 25. Power Good is Insensitive to Out of Regulation Conditions that are Present for a Duration Less Than the Built In Delay

## Selecting External Components

The CS5156H buck regulator can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard FETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level FETs. A charge pump may be easily implemented to permit use of standard FET's or support 5.0 V or 12 V only systems (maximum of 20 V ). Multiple FET's may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided:

$$
\begin{gathered}
\mathrm{VGS}_{\mathrm{GS}}(\mathrm{TOP})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V} \\
\mathrm{VGS}(\mathrm{BOTTOM})=12 \mathrm{~V}
\end{gathered}
$$

(see Figure 26)


Figure 26. Gate Drive Waveforms Depicting Rail to Rail Swing


Trace $1=\operatorname{GATE}(\mathrm{H})(5.0 \mathrm{~V} /$ div. $)$
Trace $2=\operatorname{GATE}(\mathrm{L})(5.0 \mathrm{~V} /$ div. $)$
Figure 27. Normal Operation Showing the Guaranteed Non-Overlap Time Between the High and Low-Side MOSFET Gate Drives, I LOAD $=14 \mathrm{~A}$
The CS5156H provides adaptive control of the external NFET conduction times by guaranteeing a typical 65 ns non-overlap between the upper and lower MOSFET gate drive pulses. This feature eliminates the potentially catastrophic effect of "shoot-through current", a condition during which both FETs conduct causing them to overheat, self-destruct, and possibly inflict irreversible damage to the processor.
The most important aspect of FET performance is $\mathrm{RDS}_{\mathrm{ON}}$, which effects regulator efficiency and FET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows:

Switching MOSFET:

$$
\text { Power }=I_{\text {LOAD }}{ }^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\text { LLOAD }{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =

$$
\frac{\mathrm{V}_{\text {OUT }}+(\mathrm{ILOAD} \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\mathrm{V}_{\text {IN }}+(\mathrm{ILOAD} \times \mathrm{RDSON} \text { OF SYNCH FET }) \\
-(\mathrm{ILOAD} \times \mathrm{RDSON} \text { OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (Coff)

The Coff timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\text {OFF }}$ timing capacitor:

$$
\mathrm{C}_{\mathrm{OFF}}=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous FET

For synchronous operation, a Schottky diode may be placed in parallel with the synchronous FET to conduct the inductor current upon turn off of the switching FET to improve efficiency. The CS5156H reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous FET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense. The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=V_{B D} \times$ LIOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5156H demonstration board:

$$
\text { Power }=1.6 \mathrm{~V} \times 14.2 \mathrm{~A} \times 100 \mathrm{~ns} \times 200 \mathrm{kHz}=0.45 \mathrm{~W}
$$

This is only $1.1 \%$ of the 40 W being delivered to the load.

## "Droop" Resistor for Adaptive Voltage Positioning

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met. An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation causes the thickness of the PCB layer to vary. 2) the mismatch of L/W, and 3) temperature variation.

1. Sheet Resistivity for one ounce copper, the thickness variation typically 1.15 mil to 1.35 mil . Therefore the error due to sheet resistivity is:

$$
\frac{1.35-1.15}{1.25}=16 \%
$$

2. Mismatch due to $\mathbf{L} / \mathbf{W}$. The variation in $\mathrm{L} / \mathrm{W}$ is governed by variations due to the PCB manufacturing process that affect the geometry and the power dissipation capability of the droop resistor. The error due to $\mathrm{L} / \mathrm{W}$ mismatch is typically $1.0 \%$.
3. Thermal Considerations. Due to $I^{2} \times R$ power losses the surface temperature of the droop resistor will increase causing the resistance to increase. Also, the ambient temperature variation will contribute to the increase of the resistance, according to the formula:

$$
R=R_{20}\left[1+\alpha_{20}(T-20)\right]
$$

where:
$\mathrm{R}_{20}=$ resistance at $20^{\circ} \mathrm{C}$
$\alpha=\frac{0.00393}{{ }^{\circ} \mathrm{C}}$
$\mathrm{T}=$ operating temperature
$\mathrm{R}=$ desired droop resistor value
For temperature $\mathrm{T}=50^{\circ} \mathrm{C}$, the $\% \mathrm{R}$ change $=12 \%$
Droop Resistor Tolerance
Tolerance due to sheet resistivity variation $16 \%$
Tolerance due to L/W error $1.0 \%$
Tolerance due to temperature variation $12 \%$
Total tolerance for droop resistor $29 \%$
In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage full load is above the minimum DC tolerance spec.

Example: for a 300 MHz PentiumII, the DC accuracy spec is $2.74<\mathrm{V}_{\mathrm{CC}(\text { CORE })}<2.9 \mathrm{~V}$, and the AC accuracy spec is $2.67 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}<2.93 \mathrm{~V}$. The CS5156H DAC output voltage is $+2.812 \mathrm{~V}<\mathrm{V}_{\text {DAC }}<+2.868 \mathrm{~V}$. In order not to exceed the DC accuracy spec, the voltage drop developed across the resistor must be calculated as follows:

$$
\begin{aligned}
\mathrm{V}_{\text {DROOP }}(\mathrm{TYP}) & =\frac{\left[\mathrm{V}_{\mathrm{DAC}}(\mathrm{MIN})-\mathrm{V}_{\mathrm{DC}} \text { PENTIUMII(MIN) }\right]}{1+\mathrm{RDROOP}_{\mathrm{D}}(\text { TOLERANCE })} \\
& =\frac{2.812 \mathrm{~V}-2.74 \mathrm{~V}}{1.3}=56 \mathrm{mV}
\end{aligned}
$$

With the CS5156H DAC accuracy being $1.0 \%$, the internal error amplifier's reference voltage is trimmed so that the output voltage will be 40 mV high at no load. With no load, there is no DC drop across the resistor, producing an output voltage tracking the error amplifier output voltage, including the offset. When the full load current is delivered, a drop of -56 mV is developed across the resistor. Therefore,
the regulator output is pre-positioned at 40 mV above the nominal output voltage before a load turn-on. The total voltage drop due to a load step is $\Delta \mathrm{V}-40 \mathrm{mV}$ and the deviation from the nominal output voltage is 40 mV smaller than it would be if there was no droop resistor. Similarly at full load the regulator output is pre-positioned at 16 mV below the nominal voltage before a load turn-off. The total voltage increase due to a load turn-off is $\Delta \mathrm{V}-16 \mathrm{mV}$ and the deviation from the nominal output voltage is 16 mV smaller than it would be if there was no droop resistor. This is because the output capacitors are pre-charged to value that is either 40 mV above the nominal output voltage before a load turn-on or, 16 mV below the nominal output voltage before a load turn-off (see Figure 15).

Obviously, the larger the voltage drop across the droop resistor ( the larger the resistance), the worse the DC and load regulation, but the better the AC transient response.

## Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$
R_{A R}=\rho \times \frac{L}{A} \text { or } R=\rho \times \frac{L}{(W \times t)}
$$

where:
$\mathrm{A}=\mathrm{W} \times \mathrm{t}=$ cross-sectional area
$\rho=$ the copper resistivity $(\mu \Omega-$ mil $)$
$\mathrm{L}=$ length (mils)
$\mathrm{W}=$ width (mils)
$\mathrm{t}=$ thickness (mils)
For most PCBs the copper thickness, t , is $35 \mu \mathrm{~m}(1.37$ mils) for one ounce copper. $\rho=717.86 \mu \Omega$-mil

For a Pentium II load of 14.2 A the resistance needed to create a 56 mV drop at full load is:

$$
\text { Response Droop }=\frac{56 \mathrm{mV}}{\mathrm{IOUT}}=\frac{56 \mathrm{mV}}{14.2 \mathrm{~A}}=3.9 \mathrm{~m} \Omega
$$

The resistivity of the copper will drift with the temperature according to the following guidelines:

$$
\begin{gathered}
\Delta R=12 \% @ T_{A}=+50^{\circ} \mathrm{C} \\
\Delta R=34 \% @ T_{A}=+100^{\circ} \mathrm{C}
\end{gathered}
$$

## Droop Resistor Width Calculations

The droop resistor must have the ability to handle the load current and therefore requires a minimum width which is calculated as follows (assume one ounce copper thickness):

$$
W=\frac{\mathrm{L} O A D}{0.05}
$$

where:
$\mathrm{W}=$ minimum width (in mils) required for proper power dissipation, and $\mathrm{I}_{\text {LOAD }}$ Load Current Amps.

The Pentium ${ }^{\circledR}$ II maximum load current is 14.2 A Therefore:

$$
\mathrm{W}=\frac{14.2 \mathrm{~A}}{0.05}=284 \mathrm{mils}=0.7213 \mathrm{~cm}
$$

Droop Resistor Length Calculation

$$
\begin{aligned}
\mathrm{L} & =\frac{\mathrm{R}_{\mathrm{DROOP}} \times \mathrm{W} \times \mathrm{t}}{\rho} \\
& =\frac{0.0039 \times 284 \times 1.37}{717.86}=2113 \mathrm{mil}=5.36 \mathrm{~cm}
\end{aligned}
$$

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## Inductor Ripple Current

$$
\text { Ripple Current }=\frac{\left[\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{V}_{\mathrm{OUT}}\right]}{\left(\text { Switching Frequency } \times \mathrm{L} \times \mathrm{V}_{\text {IN }}\right)}
$$

Example: $\mathrm{V}_{\mathrm{IN}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=+2.8 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=14.2 \mathrm{~A}$, $\mathrm{L}=1.2 \mu \mathrm{H}$, Freq $=200 \mathrm{kHz}$

$$
\text { Ripple Current }=\frac{[(5.0 \mathrm{~V}-2.8 \mathrm{~V}) \times 2.8 \mathrm{~V}]}{[200 \mathrm{kHz} \times 1.2 \mu \mathrm{H} \times 5.0 \mathrm{~V}]}=5.1 \mathrm{~A}
$$

## Output Ripple Voltage

VRIPPLE $=$ Inductor Ripple Current $\times$ Output Capacitor ESR
Example:
$\mathrm{V}_{\text {IN }}=+5.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=+2.8 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=14.2 \mathrm{~A}, \mathrm{~L}=1.2 \mu \mathrm{H}$, Switching Frequency $=200 \mathrm{kHz}$
Output Ripple Voltage $=5.1 \mathrm{~A} \times$ Output Capacitor ESR (from manufacturer's specs)

ESR of Output Capacitors to limit Output Voltage Spikes

$$
\mathrm{ESR}=\frac{\Delta \mathrm{V} \text { OUT }}{\Delta \mathrm{I} \mathrm{OUT}}
$$

This applies for current spikes that are faster than regulator response time. Printed Circuit Board resistance will add to the ESR of the output capacitors.

In order to limit spikes to 100 mV for a 14.2 A Load Step, $\mathrm{ESR}=0.1 / 14.2=0.007 \Omega$

## Inductor Peak Current

Peak Current $=$ Maximum Load Current $+\left(\frac{\text { Ripple Current }}{2}\right)$
Example: $\mathrm{V}_{\mathrm{IN}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=+2.8 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=14.2 \mathrm{~A}$, $\mathrm{L}=1.2 \mu \mathrm{H}$, Freq $=200 \mathrm{kHz}$

$$
\text { Peak Current }=14.2 \mathrm{~A}+(5.1 / 2)=16.75 \mathrm{~A}
$$

A key consideration is that the inductor must be able to deliver the Peak Current at the switching frequency without saturating.

## Response Time to Load Increase

(limited by Inductor value unless Maximum On-Time is exceeded)

$$
\text { Response Time }=\frac{\mathrm{L} \times \Delta \mathrm{I} \mathrm{OUT}}{\left(\mathrm{~V} \mathrm{~V}-\mathrm{V}_{\mathrm{OUT}}\right)}
$$

Example: $\mathrm{V}_{\mathrm{IN}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=+2.8 \mathrm{~V}, \mathrm{~L}=1.2 \mu \mathrm{H}, 14.2 \mathrm{~A}$ change in Load Current

$$
\text { Response Time }=\frac{1.2 \mu \mathrm{H} \times 14.2 \mathrm{~A}}{(5.0 \mathrm{~V}-2.8 \mathrm{~V})}=7.7 \mu \mathrm{~s}
$$

## Response Time to Load Decrease

(limited by Inductor value)

$$
\text { Response Time }=\frac{\mathrm{L} \times \text { Change in IOUT }}{\text { VOUT }}
$$

Example: $\mathrm{V}_{\text {OUT }}=+2.8 \mathrm{~V}, 14.2$ A change in Load Current, $\mathrm{L}=1.2 \mu \mathrm{H}$

$$
\text { Response Time }=\frac{1.2 \mu \mathrm{H} \times 14.2 \mathrm{~A}}{2.8 \mathrm{~V}}=6.1 \mu \mathrm{~s}
$$

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$
\text { Thermal Impedance }=\frac{T_{J(M A X)}-T_{A M B I E N T}}{\text { Power }}
$$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter
and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

## Layout Guidelines

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS5156H.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of logic grounds.
3. Avoid ground loops as they pick up noise. Use star or single point grounding. The source of the lower (synchronous FET) is an ideal point where the input and output GND planes can be connected.
4. For double-sided PCBs a single large ground plane is not recommended, since there is little control of where currents flow and the large surface area can act as an antenna.
5. Even though double sided PCBs are usually sufficient for a good layout, four-layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the +5.0 V and GND planes, and the top and bottom layers for the vias.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The FET gate traces to the IC must be as short, straight, and wide as possible. Ideally, the IC has to be placed right next to the FETs.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching FET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the $\mathrm{V}_{\mathrm{FB}}$ filter resistor in series with the $\mathrm{V}_{\mathrm{FB}}$ pin (pin 16) right at the pin.
12. Place the $\mathrm{V}_{\mathrm{FB}}$ filter capacitor right at the $\mathrm{V}_{\mathrm{FB}}$ pin (pin 16).
13. The "Droop" Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
14. Place the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor as close as possible to the $\mathrm{V}_{\mathrm{CC}}$ pin.


Figure 28. Additional Application Diagram, +12 V to +2.8 V @ 14.2 A for 300 MHz Pentium II


Figure 29. Additional Application Diagram, +5.0 V to +2.8 V @ 14.2 A for 300 MHz Pentium II

## CS5165H

PACKAGE THERMAL DATA

| Parameter |  | SO-16L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 23 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 105 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5166H

## 5-Bit Synchronous CPU Controller with Power Good and Current Limit

The CS5166H is a synchronous dual NFET buck controller. It is designed to power the core logic of the latest high performance CPUs. It uses $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation. It incorporates many additional features required to ensure the proper operation and protection of the CPU and power system. The CS5166H provides the industry's most highly integrated solution, minimizing external component count, total solution size, and cost.

The CS5166H is specifically designed to power Intel's Pentium ${ }^{\circledR}$ II processor and includes the following features: 5-bit DAC with $1.0 \%$ tolerance, Power Good output, adjustable hiccup mode overcurrent protection, $\mathrm{V}_{\mathrm{CC}}$ monitor, Soft Start, adaptive voltage positioning, overvoltage protection, remote sense and current sharing capability.

The CS5166H will operate over a 4.15 to 20 V range using either single or dual input voltage and is available in a 16 lead wide body surface mount package.

## Features

- $\mathrm{V}^{2}$ Control Topology
- Dual N-Channel Design
- 125 ns Controller Transient Response
- Excess of 1.0 MHz Operation
- 5-Bit DAC with $1.0 \%$ Tolerance
- Power Good Output With Internal Delay
- Adjustable Hiccup Mode Overcurrent Protection
- Complete Pentium II System Requires Just 21 Components
- 5.0 V \& 12 V Operation Using Either Dual or Single Supplies
- Adaptive Voltage Positioning
- Remote Sense Capability
- Current Sharing Capability
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- Overvoltage Protection (OVP)
- Programmable Soft Start
- 200 ns PWM Blanking
- 65 ns FET Nonoverlap Time
- 40 ns Gate Rise and Fall Times (3.3 nF Load)

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


A = Assembly Location
WL, L = Wafer Lot
$\mathrm{Y} Y, \mathrm{Y}=\mathrm{Year}$
WW, W = Work Week

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5166HGDW16 | SO-16L | 46 Units/Rail |
| CS5166HGDWR16 | SO-16L | 1000 Tape \& Reel |

## CS5166H



Figure 1. Application Diagram, 5.0 V to 2.8 V @ 14.2 A for 300 MHz Pentium II

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{\mathrm{J}}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1$)$ | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\mathrm{CC}}$ | 20 V | -0.3 V | N/A | 1.5 A peak, 200 mA DC |
| Soft Start Capacitor | SS | 6.0 V | -0.3 V | $200 \mu \mathrm{~A}$ | $10 \mu \mathrm{~A}$ |
| Compensation Capacitor | COMP | 6.0 V | -0.3 V | 10 mA | 1.0 mA |
| Voltage Feedback and Current Sense Comparator Input | $V_{\text {FB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Off-Time Capacitor | $\mathrm{C}_{\text {OFF }}$ | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| Voltage ID DAC Inputs | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | 6.0 V | -0.3 V | 1.0 mA | $10 \mu \mathrm{~A}$ |
| High-Side FET Driver | GATE(H) | 20 V | -0.3 V | 1.5 A peak, 200 mA DC | 1.5 A peak, 200 mA DC |
| Low-Side FET Driver | GATE(L) | 20 V | -0.3 V | 1.5 A peak, 200 mA DC | 1.5 A peak, 200 mA DC |
| Current Sense Comparator Input | Isense | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | $10 \mu \mathrm{~A}$ | 30 mA |
| Power Ground | PGND | 0 V | 0 V | 1.5 A peak, 200 mA DC | N/A |
| Logic Ground | LGND | 0 V | 0 V | 100 mA | N/A |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ; 2.0\right.$ DAC Code:
$\left(\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1\right), \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ Supply Current |  |  |  |  |  |
| Operating | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<\mathrm{V}_{\mathrm{DAC}}(\max$ on-time $)$, <br> No Loads on GATE(H) and GATE(L) | - | 12 | 20 | mA |

## $\mathrm{V}_{\mathrm{cc}}$ Monitor

| Start Threshold | GATE $(\mathrm{H})$ switching | 3.75 | 3.95 | 4.15 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | GATE $(\mathrm{H})$ not switching | 3.65 | 3.87 | 4.05 | V |
| Hysteresis | Start-Stop | - | 80 | - | mV |

Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| COMP Source Current | $\mathrm{COMP}=1.2 \mathrm{~V}$ to $3.6 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| COMP CLAMP Voltage | $\mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V}$, Adjust COMP voltage for Comp <br> current $=60 \mu \mathrm{~A}$ | 0.85 | 1.0 | 1.15 | V |
| COMP Clamp Current | COMP $=0 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP Sink Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}>2.5 \mathrm{~V}$ | 180 | 400 | 800 | $\mu \mathrm{~A}$ |
| Open Loop Gain | Note 2 | 50 | 60 | - | dB |
| Unity Gain Bandwidth | Note 2 | 0.5 | 2.0 | - | MHz |
| PSRR @ 1.0 kHz | Note 2 | 60 | 85 | - | dB |

Overcurrent Detection

| Current Limit Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ to $3.5 \mathrm{~V}, 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<12 \mathrm{~V}+10 \%$ | 55 | 76 | 130 | mV |
| :--- | :--- | :--- | :--- | :--- | :---: |
| $\mathrm{I}_{\text {SENSE }}$ Bias Current | $\mathrm{I}_{\text {SENSE }}=2.8 \mathrm{~V}$ | 13 | 30 | 50 | $\mu \mathrm{~A}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ; 2.0\right.$ DAC Code: $\left(\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{I D 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1\right), \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATE(H) and GATE(L) |  |  |  |  |  |
| High Voltage at 100 mA | Measure V ${ }_{\text {CC }}$ - GATE | - | 1.2 | 2.0 | V |
| Low Voltage at 100 mA | Measure GATE | - | 1.0 | 1.5 | V |
| Rise Time | $1.6 \mathrm{~V}<\mathrm{GATE}<\left(\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right), 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$ | - | 40 | 80 | ns |
| Fall Time | $\left(\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right)>$ GATE $>1.6 \mathrm{~V}, 8.0 \mathrm{~V}<\mathrm{V}_{C C}<14 \mathrm{~V}$ | - | 40 | 80 | ns |
| GATE(H) to GATE(L) Delay | $\begin{aligned} & \operatorname{GATE}(\mathrm{H})<2.0 \mathrm{~V} ; \operatorname{GATE}(\mathrm{L})>2.0 \mathrm{~V}, \\ & 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} \end{aligned}$ | 30 | 65 | 100 | ns |
| GATE(L) to GATE(H) Delay | $\begin{aligned} & \operatorname{GATE}(\mathrm{L})<2.0 \mathrm{~V} \text {; } \operatorname{GATE}(\mathrm{H})>2.0 \mathrm{~V}, \\ & 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} \end{aligned}$ | 30 | 65 | 100 | ns |
| GATE pull-down | Resistor to PGND, Note 3 | 20 | 50 | 115 | k $\Omega$ |

Fault Protection

| SS Charge Time | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {ISENSE }}=2.8 \mathrm{~V}$ | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| SS Pulse Period | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}, \mathrm{~V}_{\text {ISENSE }}=2.8 \mathrm{~V}$ | 25 | 100 | 200 | ms |
| SS Duty Cycle | $($ Charge Time/Period $) \times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| SS COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V}$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\mathrm{FB}}$ Low Comparator | Increase $\mathrm{V}_{\mathrm{FB}}$ till normal off-time | 0.9 | 1.0 | 1.1 | V |

PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FB}}=1.2$ to 5.0 V .500 ns after $\operatorname{GATE}(\mathrm{H})$ <br> (after Blanking time) to $\operatorname{GATE}(\mathrm{H})=\left(\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}\right)$ <br> to $1.0 \mathrm{~V}, 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$ | - | 115 | 175 | ns |
| :--- | :--- | :--- | :--- | :--- | :---: |
| Minimum Pulse Width <br> (Blanking Time) | Drive $\mathrm{V}_{\mathrm{FB}} 1.2 \mathrm{~V}$ to 5.0 V upon $\mathrm{GATE}(\mathrm{H})$ rising <br> edge $\left(>\mathrm{V}_{\mathrm{CC}}-1.0 \mathrm{~V}\right)$, measure $\mathrm{GATE}(H)$ pulse <br> width, $8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$ | 100 | 200 | 300 | ns |

## Coff

| Normal Off-Time | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 1.0 | 1.6 | 2.3 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Extended Off-Time | $\mathrm{V}_{\mathrm{SS}}=\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 5.0 | 8.0 | 12.0 | $\mu \mathrm{~s}$ |

Time-Out Timer

| Time-Out Time | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$, Measure GATE(H) Pulse Width | 10 | 30 | 50 | $\mu \mathrm{~s}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Fault Duty Cycle | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 30 | 50 | 70 | $\%$ |

Power Good Output

| Low to High Delay | $\mathrm{V}_{\mathrm{FB}}=\left(0.8 \times \mathrm{V}_{\mathrm{DAC}}\right)$ to $\mathrm{V}_{\mathrm{DAC}}$ | 30 | 65 | 110 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| High to Low Delay | $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{DAC}}$ to $\left(0.8 \times \mathrm{V}_{\mathrm{DAC}}\right)$ | 30 | 75 | 120 | $\mu \mathrm{~s}$ |
| Output Low Voltage | $\mathrm{V}_{\mathrm{FB}}=2.4 \mathrm{~V}, \mathrm{I}_{\mathrm{PWRGD}}=500 \mu \mathrm{~A}$ | - | 0.2 | 0.3 | V |
| Sink Current Limit | $\mathrm{V}_{\mathrm{FB}}=2.4 \mathrm{~V}, \mathrm{PWRGD}=1.0 \mathrm{~V}$ | 0.5 | 4.0 | 15.0 | mA |

3. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ; 2.0 \mathrm{DAC}\right.$ Code: $\left(\mathrm{V}_{\text {ID4 }}=\mathrm{V}_{\text {ID3 }}=\mathrm{V}_{\text {ID2 }}=\mathrm{V}_{\text {ID1 }}=0, \mathrm{~V}_{\text {ID }}=1\right), \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |


| Voltage Identification DAC |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Accuracy (all codes except 11111) |  |  |  |  | $\begin{gathered} \text { Measure } \mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}\left(\mathrm{C}_{\mathrm{OFF}}=\mathrm{GND}\right) \\ 25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V} \end{gathered}$ | -1.0 | - | +1.0 | \% |
| VID4 | VID3 | VID2 | VID1 | VID0 |  |  |  |  |  |
| 1 | 0 | 0 | 0 | 0 | - | 3.489 | 3.525 | 3.560 | V |
| 1 | 0 | 0 | 0 | 1 | - | 3.390 | 3.425 | 3.459 | V |
| 1 | 0 | 0 | 1 | 0 | - | 3.291 | 3.325 | 3.358 | v |
| 1 | 0 | 0 | 1 | 1 | - | 3.192 | 3.225 | 3.257 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.093 | 3.125 | 3.156 | V |
| 1 | 0 | 1 | 0 | 1 | - | 2.994 | 3.025 | 3.055 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.895 | 2.925 | 2.954 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.796 | 2.825 | 2.853 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.697 | 2.725 | 2.752 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.598 | 2.625 | 2.651 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.499 | 2.525 | 2.550 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.400 | 2.425 | 2.449 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.301 | 2.325 | 2.348 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.202 | 2.225 | 2.247 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.103 | 2.125 | 2.146 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.054 | 2.075 | 2.095 | V |
| 0 | 0 | 0 | 0 | 1 | - | 2.004 | 2.025 | 2.045 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.955 | 1.975 | 1.994 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.905 | 1.925 | 1.944 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.856 | 1.875 | 1.893 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.806 | 1.825 | 1.843 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.757 | 1.775 | 1.792 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.707 | 1.725 | 1.742 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.658 | 1.675 | 1.691 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.608 | 1.625 | 1.641 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.559 | 1.575 | 1.590 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.509 | 1.525 | 1.540 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.460 | 1.475 | 1.489 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.410 | 1.425 | 1.439 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.361 | 1.375 | 1.388 | V |
| 0 | 1 | 1 | 1 | 1 | - | 1.311 | 1.325 | 1.338 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.219 | 1.247 | 1.269 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID }}$ | 1.000 | 1.250 | 2.400 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID }}$ | 25 | 50 | 100 | k $\Omega$ |
| Input Pull-up Voltage |  |  |  |  |  | 4.85 | 5.00 | 5.15 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<20 \mathrm{~V} ; 2.0 \mathrm{DAC}\right.$ Code: $\left(\mathrm{V}_{I D 4}=\mathrm{V}_{I D 3}=\mathrm{V}_{\mathrm{ID2}}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\text {ID0 }}=1\right) ; \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified. $)$

| Threshold Accuracy | Lower Threshold |  |  | Upper Threshold |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Min | Typ | Max | Min | Typ | Max |  |

## DAC CODE

| \% of Nominal DAC Output |  |  |  |  | -12 | -8.5 | -5.0 | 5.0 | 8.5 | 12 | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {ID } 4}$ | $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | VID1 | VIDO |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 0 | 0 | 3.102 | 3.225 | 3.348 | 3.701 | 3.824 | 3.948 | V |
| 1 | 0 | 0 | 0 | 1 | 3.014 | 3.133 | 3.253 | 3.596 | 3.716 | 3.836 | V |
| 1 | 0 | 0 | 1 | 0 | 2.926 | 3.042 | 3.158 | 3.491 | 3.607 | 3.724 | V |
| 1 | 0 | 0 | 1 | 1 | 2.838 | 2.950 | 3.063 | 3.386 | 3.499 | 3.612 | V |
| 1 | 0 | 1 | 0 | 0 | 2.750 | 2.859 | 2.968 | 3.281 | 3.390 | 3.500 | V |
| 1 | 0 | 1 | 0 | 1 | 2.662 | 2.767 | 2.873 | 3.176 | 3.282 | 3.388 | V |
| 1 | 0 | 1 | 1 | 0 | 2.574 | 2.676 | 2.778 | 3.071 | 3.173 | 3.276 | V |
| 1 | 0 | 1 | 1 | 1 | 2.486 | 2.584 | 2.683 | 2.966 | 3.065 | 3.164 | V |
| 1 | 1 | 0 | 0 | 0 | 2.398 | 2.493 | 2.588 | 2.861 | 2.956 | 3.052 | V |
| 1 | 1 | 0 | 0 | 1 | 2.310 | 2.401 | 2.493 | 2.756 | 2.848 | 2.940 | V |
| 1 | 1 | 0 | 1 | 0 | 2.222 | 2.310 | 2.398 | 2.651 | 2.739 | 2.828 | V |
| 1 | 1 | 0 | 1 | 1 | 2.134 | 2.218 | 2.303 | 2.546 | 2.631 | 2.716 | V |
| 1 | 1 | 1 | 0 | 0 | 2.046 | 2.127 | 2.208 | 2.441 | 2.522 | 2.604 | V |
| 1 | 1 | 1 | 0 | 1 | 1.958 | 2.035 | 2.113 | 2.336 | 2.414 | 2.492 | V |
| 1 | 1 | 1 | 1 | 0 | 1.870 | 1.944 | 2.018 | 2.231 | 2.305 | 2.380 | V |
| 0 | 0 | 0 | 0 | 0 | 1.826 | 1.898 | 1.971 | 2.178 | 2.251 | 2.324 | V |
| 0 | 0 | 0 | 0 | 1 | 1.782 | 1.8520 | 1.923 | 2.126 | 2.197 | 2.268 | V |
| 0 | 0 | 0 | 1 | 0 | 1.738 | 1.807 | 1.876 | 2.073 | 2.142 | 2.212 | V |
| 0 | 0 | 0 | 1 | 1 | 1.694 | 1.761 | 1.828 | 2.021 | 2.088 | 2.156 | V |
| 0 | 0 | 1 | 0 | 0 | 1.650 | 1.715 | 1.781 | 1.968 | 2.034 | 2.100 | V |
| 0 | 0 | 1 | 0 | 1 | 1.606 | 1.669 | 1.733 | 1.916 | 1.980 | 2.044 | V |
| 0 | 0 | 1 | 1 | 0 | 1.562 | 1.624 | 1.686 | 1.863 | 1.925 | 1.988 | V |
| 0 | 0 | 1 | 1 | 1 | 1.518 | 1.578 | 1.638 | 1.811 | 1.871 | 1.932 | V |
| 0 | 1 | 0 | 0 | 0 | 1.474 | 1.532 | 1.591 | 1.758 | 1.817 | 1.876 | V |
| 0 | 1 | 0 | 0 | 1 | 1.430 | 1.486 | 1.543 | 1.706 | 1.763 | 1.820 | V |
| 0 | 1 | 0 | 1 | 0 | 1.386 | 1.441 | 1.496 | 1.653 | 1.708 | 1.764 | V |
| 0 | 1 | 0 | 1 | 1 | 1.342 | 1.395 | 1.448 | 1.601 | 1.654 | 1.708 | V |
| 0 | 1 | 1 | 0 | 0 | 1.298 | 1.349 | 1.401 | 1.548 | 1.600 | 1.652 | V |
| 0 | 1 | 1 | 0 | 1 | 1.254 | 1.303 | 1.353 | 1.496 | 1.546 | 1.596 | V |
| 0 | 1 | 1 | 1 | 0 | 1.210 | 1.258 | 1.306 | 1.443 | 1.491 | 1.540 | V |
| 0 | 1 | 1 | 1 | 1 | 1.166 | 1.212 | 1.258 | 1.391 | 1.437 | 1.484 | V |
| 1 | 1 | 1 | 1 | 1 | 1.094 | 1.138 | 1.181 | 1.306 | 1.349 | 1.393 | V |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-16L | PIN SYMBOL | FUNCTION |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID0 }}-\mathrm{V}_{\text {ID4 }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID }}$ is high (logic one), the Error Amp reference range is 2.125 V to 3.525 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is low (logic zero), the Error Amp reference voltage is 1.325 V to 2.075 V with 50 mV increments. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND sets the Soft Start and fault timing. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | Off-Time Capacitor Pin. A capacitor from this pin to LGND sets both the normal and extended off time. |
| 8 | ISENSE | Current Sense Comparator Inverting Input. |
| 9 | $\mathrm{V}_{\mathrm{CC}}$ | Input Power Supply Pin. |
| 10 | GATE(H) | High Side Switch FET driver pin. |
| 11 | PGND | High current ground for the GATE $(\mathrm{H})$ and GATE $(\mathrm{L})$ pins. |
| 12 | GATE(L) | Low Side Synchronous FET driver pin. |
| 13 | PWRGD | Power Good Output. Open collector output drives low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. |
| 14 | LGND | Reference ground. All control circuits are referenced to this pin. |
| 15 | COMP | Error Amp output. PWM Comparator reference input. A capacitor to LGND provides Error Amp compensation. |
| 16 | $\mathrm{V}_{\mathrm{FB}}$ | Error Amp, PWM Comparator feedback input, Current Sense Comparator Non-Inverting input, and PWRGD Comparator input. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. GATE(L) Risetime vs. Load Capacitance

Figure 5. GATE(H) \& GATE(L) Falltime vs. Load Capacitance


Figure 4. GATE(H) Risetime vs. Load Capacitance


Figure 6. DAC Output Voltage vs. Temperature, DAC Code $=10111, V_{\text {CC }}=12 \mathrm{~V}$


Figure 7. Percent Output Error vs. DAC Voltage Setting, $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{ID} 4}=0$


Figure 8. Percent Output Error vs. DAC Output Voltage Setting $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{ID} 4}=1$

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 9. ${ }^{2}$ Control Diagram
The $V^{2}$ control method is illustrated in Figure 9. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved,
since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.
The Bode plot in Figure 10 shows the gain and phase margin of the CS5166H single pole feedback loop and demonstrates the overall stability of the CS5166H-based regulator.


Figure 10. Feedback Loop Bode Plot
Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation.
A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5166H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the CofF capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.
Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu$ s (typical) timer, minimizing stress to the power components.

## Programmable Output

The CS5166H is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.125 V to 3.525 V in 100 mV steps, the second is 1.325 V to 2.075 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5166H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ pin, as in traditional controllers. The CS5166H is specifically designed to meet or exceed Intel's Pentium II specifications.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC}}$ supply pin exceeds the 3.95 V monitor threshold, the Soft Start and GATE pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC}}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C CoFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by the Soft Start COMP clamp and the voltage on the Soft Start pin.


Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC}}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (1.0 V/div.)
Figure 11. Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1- Regulator Output Voltage ( $1.0 \mathrm{~V} /$ div.).
Trace 3- COMP PIn (error amplifier output) ( $1.0 \mathrm{~V} /$ div. ). Trace 4- Soft Start Pin (2.0 V/div.).
Figure 12. Demonstration Board Startup Waveforms


Trace 1-Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 13. Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C CofF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working and the ESR of the output capacitors (see Figures 14 and 15).


Figure 14. Normal Operation Showing Output Inductor Ripple Current and Output Voltage Ripple, 0.5 A Load, $\mathrm{V}_{\text {OUT }}=+2.825 \mathrm{~V}(\mathrm{DAC}=10111)$


Figure 15. Normal Operation Showing Output Inductor Ripple Current and Output
Voltage Ripple, $\mathrm{I}_{\text {LOAD }}=14 \mathrm{~A}, \mathrm{~V}_{\text {OUT }}=+2.825 \mathrm{~V}$ ( $D A C=10111$ )

## Transient Response

The CS5166H V ${ }^{2}$ control loop's 150 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "Adaptive Voltage Positioning". This technique pre-positions the output capacitors voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifiers reference voltage to be targeted +25 mV high without compromising DC accuracy. A "Droop Resistor", implemented through a PC board trace, connects the Error Amps feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ) to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +25 mV offset. When the full load current is delivered, an 50 mV drop is developed across this resistor. This results in output voltage being offset -25 mV low.

The result of Adaptive Voltage Positioning is that additional margin is provided for a load transient before
reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre-positioned +25 mV . Conversely, when load current suddenly decreases from its maximum level, the output capacitor is pre-positioned -25 mV (see Figures 16, 17, and 18). For best Transient Response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the Maximum On-Time is exceeded while responding to a sudden increase in Load current, a normal off-time occurs to prevent saturation of the output inductor.


Ch4 Max
2.914 V
Ch4 Min
2.718 V
Ch4 Pk-Pk
196 mV
Trace 3- Load Current (5.0 A/10 mV/div.)
Trace 4- Vout ( $100 \mathrm{mV} / \mathrm{div}$.)
Figure 16. Output Voltage Transient Response to a 14 A Load Pulse, $\mathrm{V}_{\text {OUT }}=+2.825 \mathrm{~V}(\mathrm{DAC}=10111)$


Figure 17. Output Voltage Transient Response to a 14 A Load Step, $\mathrm{V}_{\text {OUT }}=+2.825 \mathrm{~V}(\mathrm{DAC}=10111)$


Figure 18. Output Voltage Transient Response to a 14 A Load Turn-Off, $\mathrm{V}_{\text {OUT }}=+2.825 \mathrm{~V}$ (DAC = 10111)

## Power Supply Sequencing

The CS5166H offers inherent protection from undefined start up conditions, regardless of the 12 V and 5.0 V supply power up sequencing. The turn on slew rates of the 12 V and 5.0 V power supplies can be varied over wide ranges without affecting the output voltage or causing detrimental effects to the buck regulator.

## PROTECTION AND MONITORING FEATURES

## Overcurrent Protection

A loss-less hiccup mode current limit protection feature is provided, requiring only the Soft Start capacitor to implement. The CS5166H provides overcurrent protection by sensing the current through a "Droop" resistor, using an internal current sense comparator. The comparator compares this voltage drop to an internal reference voltage of 76 mV (typical).

If the voltage drop across the "Droop" resistor exceeds this threshold, the current sense comparator allows the fault latch to be set. This causes the regulator to stop switching. During this overcurrent condition, the CS5166H stays off for the time it takes the Soft Start capacitor to slowly discharge by a $2.0 \mu \mathrm{~A}$ current source until it reaches its lower 0.7 V threshold.

At that time the regulator attempts to restart normally by delivering short gate pulses to both FET's. The CS5166H will operate initially in its extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a 60 mA charge current. The gates will switch on while
the Soft Start capacitor is charged to its upper 2.7 V threshold. During an overload condition the Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=3.3 \%)$, while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ) when $\mathrm{V}_{\mathrm{FB}}$ is less than 1.0 V . The Soft Start hiccup pulses last for a 3.0 ms period at the end of which the duty cycle repeats if a fault is detected, otherwise normal operation resumes.

The protection scheme minimizes thermal stress to the regulator components, input power supply, and PC board traces, as the overcurrent condition persists. Upon removal of the overload, the fault latch is cleared, allowing normal operation to resume. The current limit trip point can be adjusted through an external resistor, providing the user with the current limit set-point flexibility.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3- Soft Start Timing Capacitor ( $1.0 \mathrm{~V} /$ div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 19. Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Trace 4-5.0 V from PC Power Supply (2.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 20. Demonstration Board Startup with Regulator Output Shorted To Ground

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top

MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 21 and 22 ). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function. If a dedicated OVP output is required, it can be implemented using the circuit in Figure 23. In this figure the OVP signal will go high (overvoltage condition), if the output voltage ( $\mathrm{V}_{\mathrm{CORE}}$ ) exceeds $20 \%$ of the voltage set by the particular DAC code and provided that PWRGD is low. It is also required that the overvoltage condition be present for at least the PWRGD delay time for the OVP signal to be activated. The resistor values shown in Figure 23 are for $\mathrm{V}_{\mathrm{DAC}}=+2.8 \mathrm{~V}(\mathrm{DAC}=10111)$. The $\mathrm{V}_{\mathrm{OVP}}$ (overvoltage trip-point) can be set using the following equation:

$$
\mathrm{V}_{\mathrm{OVP}}=\mathrm{V}_{\mathrm{BEQ}}\left(1+\frac{\mathrm{R} 2}{\mathrm{R} 1}\right)
$$



Trace 4-5.0 V from PC Power Supply (5.0 V/div.)
Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} /$ div.)
Trace 2- Inductor Switching Node 5.0 V/div.)
Figure 21. OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Trace 4-5.0 V from PC Power Supply (2.0 V/div.)
Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Figure 22. OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground


Figure 23. Circuit To Implement A Dedicated OVP Output Using The CS5166H

## Power Good Circuit

The Power Good pin (pin 13) is an open-collector signal consistent with TTL DC specifications. It is externally pulled-up, and is pulled low (below 0.3 V ) when the regulator output voltage typically exceeds $\pm 8.5 \%$ of the nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is $\pm 12 \%$.


Ch2 Max 5.28 V

Ch4 Max 2.825 V

Trace 2- PWRGD (2.0 V/div.)
Trace 4- V OUT (1.0 V/div.)
Figure 24. PWRGD Signal Becomes Logic High as $V_{\text {OUT }}$ Enters -8.5\% of Lower PWRGD Threshold, $\mathrm{V}_{\text {OUT }}=+2.825 \mathrm{~V}(\mathrm{DAC}=10111)$


Trace $4-\mathrm{V}_{\mathrm{FB}}$ ( $1.0 \mathrm{~V} /$ div.)
Figure 25. Power Good Response to an Out of Regulation Condition
Figure 25 shows the relationship between the regulated output voltage $\mathrm{V}_{\mathrm{FB}}$ and the Power Good signal. To prevent Power Good from interrupting the CPU unnecessarily, the CS5166H has a built-in delay to prevent noise at the $V_{\text {FB }}$ pin from toggling Power Good. The internal time delay is designed to take about $75 \mu$ s for Power Good to go low and $65 \mu \mathrm{~s}$ for it to recover. This allows the Power Good signal to be completely insensitive to out of regulation conditions that are present for a duration less than the built in delay (see Figure 26).
It is therefore required that the output voltage attains an out of regulation or in regulation level for at least the built-in delay time duration before the Power Good signal can change state.


Trace 2- PWRGD (2.0 V/div.)
Trace 4- $\mathrm{V}_{\mathrm{FB}}$ (1.0 V/div.)
Figure 26. Power Good is Insensitive to Out of Regulation Conditions that are Present for a Duration Less Than the Built In Delay

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure ). This circuit operates by pulling the Soft Start pin high, and the I SENSE pin low, emulating a current limit condition.


Figure 27. Implementing Shutdown with the CS5166H

## Selecting External Components

The CS5166H buck regulator can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard FETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level FETs. A charge pump may be easily implemented to permit use of standard FET's or support 5.0 V or 12 V only systems (maximum of 20 V ). Multiple FET's may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided:

$$
\begin{gathered}
\mathrm{VGS}_{\mathrm{GS}}(\mathrm{TOP})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V} \\
\mathrm{VGS}(\mathrm{BOTTOM})=12 \mathrm{~V}
\end{gathered}
$$

(see Figure 28)


Figure 28. Gate Drive Waveforms Depicting Rail to Rail Swing


Trace $1=\operatorname{GATE}(\mathrm{H})(5.0 \mathrm{~V} /$ div. $)$
Trace $2=$ GATE(L) (5.0 V/div.)
Figure 29. Normal Operation Showing the Guaranteed Non-Overlap Time Between the High and Low-Side MOSFET Gate Drives, I LOAD = 14 A
The CS5166H provides adaptive control of the external NFET conduction times by guaranteeing a typical 65 ns non-overlap (as seen in Figure 29) between the upper and lower MOSFET gate drive pulses. This feature eliminates the potentially catastrophic effect of "shoot-through current", a condition during which both FETs conduct causing them to overheat, self-destruct, and possibly inflict irreversible damage to the processor.

The most important aspect of FET performance is RDS $_{\text {ON }}$, which effects regulator efficiency and FET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows:

Switching MOSFET:

$$
\text { Power }=\text { ILOAD }{ }^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\begin{aligned}
& \text { Power }=\text { ILOAD }^{2} \times \text { RDSON } \times(1-\text { duty cycle }) \\
& \text { Duty Cycle }= \\
& \frac{\text { VOUT }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\text { VIN }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET }) \\
-(\text { ILOAD } \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
\end{aligned}
$$

## Off Time Capacitor (COFF)

The $\mathrm{C}_{\mathrm{OFF}}$ timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the CofF timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous FET

For synchronous operation, a Schottky diode may be placed in parallel with the synchronous FET to conduct the inductor current upon turn off of the switching FET to improve efficiency. The CS5166H reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous FET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense. The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=V_{B D} \times$ LLOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5166H demonstration board:

$$
\text { Power }=1.6 \mathrm{~V} \times 14.2 \mathrm{~A} \times 100 \mathrm{~ns} \times 200 \mathrm{kHz}=0.45 \mathrm{~W}
$$

This is only $1.1 \%$ of the 40 W being delivered to the load.

## "Droop" Resistor for Adaptive Voltage Positioning

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor
and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met. An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation causes the thickness of the PCB layer to vary. 2) the mismatch of L/W, and 3) temperature variation.

1. Sheet Resistivity for one ounce copper, the thickness variation typically 1.15 mil to 1.35 mil . Therefore the error due to sheet resistivity is:

$$
\frac{1.35-1.15}{1.25}=16 \%
$$

2. Mismatch due to $L / W$. The variation in $L / W$ is governed by variations due to the PCB manufacturing process that affect the geometry and the power dissipation capability of the droop resistor. The error due to $\mathrm{L} / \mathrm{W}$ mismatch is typically $1.0 \%$.
3. Thermal Considerations. Due to $\mathrm{I}^{2} \times \mathrm{R}$ power losses the surface temperature of the droop resistor will increase causing the resistance to increase. Also, the ambient temperature variation will contribute to the increase of the resistance, according to the formula:

$$
R=R_{20}\left[1+\alpha_{20}(T-20)\right]
$$

where:
$\mathrm{R}_{20}=$ resistance at $20^{\circ} \mathrm{C}$
$\alpha=\frac{0.00393}{{ }^{\circ} \mathrm{C}}$

$$
\mathrm{T}=\text { operating temperature }
$$

$\mathrm{R}=$ desired droop resistor value
For temperature $\mathrm{T}=50^{\circ} \mathrm{C}$, the $\% \mathrm{R}$ change $=12 \%$

## Droop Resistor Tolerance

Tolerance due to sheet resistivity variation $16 \%$
Tolerance due to L/W error $1.0 \%$
Tolerance due to temperature variation $12 \%$
Total tolerance for droop resistor 29\%
In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage full load is above the minimum DC tolerance spec.

$$
\mathrm{V}_{\mathrm{DROOP}}(\mathrm{TYP})=\frac{\left[\mathrm{V}_{\mathrm{DAC}}(\mathrm{MIN})-\mathrm{V}_{\mathrm{DC}}(\mathrm{MIN})\right]}{1+\mathrm{RDROOP}^{(T O L E R A N C E)}}
$$

Example: for a 300 MHz PentiumII, the DC accuracy spec is $2.74<\mathrm{V}_{\mathrm{CC}(\text { CORE })}<2.9 \mathrm{~V}$, and the AC accuracy spec is $2.67 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}<2.93 \mathrm{~V}$. The CS5166H DAC output voltage is $+2.796 \mathrm{~V}<\mathrm{V}_{\mathrm{DAC}}<+2.853 \mathrm{~V}$. In order not to exceed the DC accuracy spec, the voltage drop developed across the resistor must be calculated as follows:

$$
\begin{aligned}
\mathrm{V}_{\text {DROOP(TYP) }} & =\frac{\left[\mathrm{V}_{\mathrm{DAC}(\mathrm{MIN})}-\mathrm{V}_{\mathrm{DC}}\right. \text { PENTIUMII(MIN)] }}{1+\mathrm{RDROOP}(\mathrm{TOLERANCE})} \\
& =\frac{2.796 \mathrm{~V}-2.74 \mathrm{~V}}{1.3}=43 \mathrm{mV}
\end{aligned}
$$

With the CS5166H DAC accuracy being $1.0 \%$, the internal error amplifier's reference voltage is trimmed so that the output voltage will be 25 mV high at no load. With no load, there is no DC drop across the resistor, producing an output voltage tracking the error amplifier output voltage, including the offset. When the full load current is delivered, a drop of -43 mV is developed across the resistor. Therefore, the regulator output is pre-positioned at 25 mV above the nominal output voltage before a load turn-on. The total voltage drop due to a load step is $\Delta \mathrm{V}-25 \mathrm{mV}$ and the
deviation from the nominal output voltage is 25 mV smaller than it would be if there was no droop resistor. Similarly at full load the regulator output is pre-positioned at 18 mV below the nominal voltage before a load turn-off. The total voltage increase due to a load turn-off is $\Delta \mathrm{V}-18 \mathrm{mV}$ and the deviation from the nominal output voltage is 18 mV smaller than it would be if there was no droop resistor. This is because the output capacitors are pre-charged to value that is either 25 mV above the nominal output voltage before a load turn-on or, 18 mV below the nominal output voltage before a load turn-off (see Figure 16).
Obviously, the larger the voltage drop across the droop resistor (the larger the resistance), the worse the DC and load regulation, but the better the AC transient response.


Figure 30. Circuit Used to Determine the Voltage Across the Droop Resistor that will Trip the Internal Current Sense Comparator

## Current Limit Setpoint Calculations

The following is the design equations used to set the current limit trip point by determining the value of the embedded PCB trace used as a current sensing element.

The current limit setpoint has to be higher than the normal full load current. Attention has to be paid to the current rating of the external power components as these are the first to fail during an overload condition. The MOSFET continuous and pulsed drain current rating at a given case temperature has to be accounted for when setting the current limit trip point. For example the IRL 3103S ( $\mathrm{D}^{2}$ PAK) MOSFET has a continuous drain current rating of 45 A at $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V}$ and $\mathrm{T}_{\mathrm{C}}=100^{\circ} \mathrm{C}$. Temperature curves on MOSFET manufacturers' data sheets allow the designer to determine the MOSFET drain current at a particular $\mathrm{V}_{\mathrm{GS}}$ and $\mathrm{T}_{\mathrm{J}}$ (junction temperature). This, in turn, will assist the designer to set a proper current limit, without causing device breakdown during an overload condition.

For 300 MHz Pentium II CPU the full load is 14.2 A . The internal current sense comparator current limit voltage
limits are: $55 \mathrm{mV}<\mathrm{V}_{\mathrm{TH}}<130 \mathrm{mV}$. Also, there is a $29 \%$ total variation in $\mathrm{R}_{\text {SENSE }}$ as discussed in the previous section.

We select the value of the current sensing element (embedded PCB trace) for the minimum current limit setpoint:

$$
\begin{gathered}
\operatorname{RSENSE}(\mathrm{MAX})=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{MIN})} \mathrm{I} \mathrm{CL}(\mathrm{MIN})}{\mathrm{R}} \Rightarrow \mathrm{RSENSE} \times 1.29=\frac{55 \mathrm{mV}}{14.2 \mathrm{~A}} \Rightarrow \\
\text { RSENSE } \times 1.29=3.87 \mathrm{~m} \Omega \Rightarrow \text { RSENSE }=3.0 \mathrm{~m} \Omega
\end{gathered}
$$

We calculate the range of load currents that will cause the internal current sense comparator to detect and overload condition.

From the overcurrent detection data section on page 2095. Nominal Current Limit Setpoint

$$
\begin{gathered}
\mathrm{V}_{\mathrm{TH}(\mathrm{TYP})}=76 \mathrm{mV} \\
\mathrm{I}_{\mathrm{CL}(\mathrm{NOM})}=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{TYP})}}{\operatorname{RSENSE}(\mathrm{NOM})}
\end{gathered}
$$

Maximum Current Limit Setpoint

$$
\begin{aligned}
& \text { Therefore, } \operatorname{ICL}(\mathrm{NOM})=\frac{76 \mathrm{mV}}{3.0 \mathrm{~m} \Omega}=25.3 \\
& \mathrm{~V}_{\mathrm{TH}(\mathrm{MAX})}=110 \mathrm{mV}
\end{aligned}
$$

Therefore,
$\operatorname{ICL}(\mathrm{MAX})=$
$\frac{110 \mathrm{mV}}{\operatorname{RSENSE}_{(M I N)}}=\frac{110 \mathrm{mV}}{\text { RSENSE } \times 0.71}=\frac{110 \mathrm{mV}}{3.0 \mathrm{~m} \Omega \times 0.71}=51.6 \mathrm{~A}$
Therefore, the range of load currents that will cause the internal current sense comparator to detect an overload condition through a $3.0 \mathrm{~m} \Omega$ embedded PCB trace is: 14.2 A $<\mathrm{I}_{\mathrm{CL}}<51.6 \mathrm{~A}$, with 25.3 A being the nominal overload condition.

There may be applications whose layout will require the use of two extra filter components, a $510 \Omega$ resistor in series with the $\mathrm{I}_{\text {SENSE }}$ pin, and a $0.1 \mu \mathrm{~F}$ capacitor between the $I_{\text {SENSE }}$ and $\mathrm{V}_{\text {FB }}$ pins. These are needed for proper current limit operation and the resistor value is layout dependent.

This series resistor affects the calculation of the current limit setpoint, and has to be taken into account when determining an effective current limit.

The calculations below show how the current limit setpoint is determined when this $510 \Omega$ is taken into consideration.
$\mathrm{V}_{\text {TRIP }}=\mathrm{V}_{\mathrm{TH}}+\left(\mathrm{I}_{\text {SENSE }} \times \mathrm{R}_{\text {ISENSE }}\right)-\left(\mathrm{R}_{\mathrm{FB}} \times \mathrm{I}_{\mathrm{FB}}\right)$
Where:
$\mathrm{V}_{\text {TRIP }}=$ voltage across the droop resistor that trips the $\mathrm{I}_{\text {SENSE }}$ comparator.
$\mathrm{V}_{\mathrm{TH}}=$ internal $\mathrm{I}_{\text {SENSE }}$ comparator threshold
$\mathrm{I}_{\text {SENSE }}=\mathrm{I}_{\text {SENSE }}$ bias current
$\mathrm{R}_{\text {ISENSE }}=\mathrm{I}_{\text {SENSE }}$ pin $510 \Omega$ filter resistor
$\mathrm{R}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{FB}}$ pin 3.3 k filter resistor
$\mathrm{I}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{FB}}$ bias current
Minimum current sense resistor (droop resistor) voltage drop required for current limit when $\mathrm{R}_{\text {ISENSE }}$ is used

$$
\begin{aligned}
\mathrm{V}_{\mathrm{TRIP}(\mathrm{MIN})} & =55 \mathrm{mV}+(13 \mu \mathrm{~A} \times 510)-(3.3 \mathrm{k} \times 1.0 \mu \mathrm{~A}) \\
& =55 \mathrm{mV}+6.6 \mathrm{mV}-3.3 \mathrm{mV}=58.3 \mathrm{mV}
\end{aligned}
$$

Nominal current sense resistor (droop resistor) voltage drop required for current limit when $\mathrm{R}_{\text {ISENSE }}$ is used

$$
\begin{aligned}
\mathrm{V} \text { TRIP(NOM) } & =76 \mathrm{mV}+(30 \mu \mathrm{~A} \times 510)-(3.3 \mathrm{k} \times 0.1 \mu \mathrm{~A}) \\
& =76 \mathrm{mV}+15.3 \mathrm{mV}-0.33 \mathrm{mV}=90.97 \mathrm{mV}
\end{aligned}
$$

Maximum current sense resistor (droop resistor) voltage drop required for current limit when $\mathrm{R}_{\text {ISENSE }}$ is used

$$
\begin{aligned}
\mathrm{V} \operatorname{TRIP}(\mathrm{NOM}) & =110 \mathrm{mV}+(50 \mu \mathrm{~A} \times 510) \\
& =110 \mathrm{mV}+25.5 \mathrm{mV}=135.5 \mathrm{mV}
\end{aligned}
$$

The value of $\mathrm{R}_{\text {SENSE }}$ (current sense PCB trace) is then calculated:

$$
\begin{gathered}
\operatorname{RSENSE}(\mathrm{MAX})=\frac{58.3 \mathrm{mV}}{14.2 \mathrm{~A}}=4.1 \mathrm{~m} \Omega \\
\operatorname{RSENSE}(\mathrm{NOM})=\frac{\operatorname{RSENSE}(\mathrm{MAX})}{1.29}=\frac{4.1 \mathrm{~m} \Omega \mathrm{~m}}{1.29}=3.18 \mathrm{~m} \Omega
\end{gathered}
$$

The range of load currents that will cause the internal current sense comparator to detect an overload condition is as follows:
Nominal Current Limit Setpoint

$$
\operatorname{ICL}(\mathrm{NOM})=\frac{\mathrm{V}_{\operatorname{TRIP}(\mathrm{NOM})}}{\operatorname{RSENSE}(\mathrm{NOM})}
$$

Therefore,

$$
\mathrm{ICL}(\mathrm{NOM})=\frac{90.97 \mathrm{mV}}{3.18 \mathrm{~m} \Omega}=28.6 \mathrm{~A}
$$

## Maximum Current Limit Setpoint

$$
\mathrm{I}_{\mathrm{CL}(\mathrm{MAX})}=\frac{\mathrm{V} \operatorname{TRIP}(\mathrm{MAX})}{\operatorname{RSENSE}(\mathrm{MAX})}
$$

Therefore,

$$
\mathrm{ICL}(\mathrm{MAX})=\frac{135 \mathrm{mV}}{3.18 \mathrm{~m} \Omega \times 0.71}=60 \mathrm{~A}
$$

Therefore, the range of load currents that will cause the internal current sense comparator to detect an overload condition through a $3.0 \mathrm{~m} \Omega$ embedded PCB trace is: 14.2 A < ICL 60 A, with 28.6 A being the nominal overload condition.

## Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$
R_{A R}=\rho \times \frac{L}{A} \text { or } R=\rho \times \frac{L}{(W \times t)}
$$

where:

$$
\begin{aligned}
& A=W \times t=\text { cross-sectional area } \\
& \rho=\text { the copper resistivity }(\mu \Omega-\text { mil }) \\
& L=\text { length (mils) } \\
& W=\text { width (mils) } \\
& t=\text { thickness (mils) }
\end{aligned}
$$

For most PCBs the copper thickness, t , is $35 \mu \mathrm{~m}(1.37$ mils) for one ounce copper. $\rho=717.86 \mu \Omega-$ mil

For a Pentium II load of 14.2 A the resistance needed to create a 43 mV drop at full load is:

$$
\text { Response Droop }=\frac{43 \mathrm{mV}}{\mathrm{IOUT}}=\frac{43 \mathrm{mV}}{14.2 \mathrm{~A}}=3.0 \mathrm{~m} \Omega
$$

The resistivity of the copper will drift with the temperature according to the following guidelines:

$$
\begin{gathered}
\Delta R=12 \% @ T_{A}=+50^{\circ} \mathrm{C} \\
\Delta R=34 \% @ T_{A}=+100^{\circ} \mathrm{C}
\end{gathered}
$$



Figure 31. Current Sharing of a 2.8 V/30 A Power Supply Using Two CS5166H Synchronous Buck Regulators

## Droop Resistor Width Calculations

The droop resistor must have the ability to handle the load current and therefore requires a minimum width which is calculated as follows (assume one ounce copper thickness):

$$
W=\frac{\mathrm{L} \text { LOAD }}{0.05}
$$

where:
$\mathrm{W}=$ minimum width (in mils) required for proper power dissipation, and $\mathrm{I}_{\text {LOAD }}$ Load Current Amps.

The Pentium II maximum load current is 14.2 A . Therefore:

$$
\mathrm{W}=\frac{14.2 \mathrm{~A}}{0.05}=284 \mathrm{mils}=0.7213 \mathrm{~cm}
$$

Droop Resistor Length Calculation

$$
\begin{aligned}
\mathrm{L} & =\frac{\mathrm{RDROOP} \times \mathrm{W} \times \mathrm{t}}{\rho} \\
& =\frac{0.0030 \times 284 \times 1.37}{717.86}=1626 \mathrm{mil}=4.13 \mathrm{~cm}
\end{aligned}
$$

## Implementing Current Sharing Using the "Droop Resistor"

In addition to improving load transient performance, the CS5166H V ${ }^{2}$ control method allows the droop resistor to provide the additional capability to easily implement current sharing. Figure 31 shows a simplified schematic of two current sharing synchronous buck regulators. Each buck
regulator's droop resistor is terminated at the load. The PWM control signal from each Error Amp is connected together, causing the inner PWM loop to regulate to a common voltage. Since the voltage at each resistor terminal is the same, this configuration results in equal voltage being applied across each matched droop resistor. The result is equal current flowing through each buck regulator. An additional benefit is that synchronization to a common switching frequency tends to be achieved because each regulator shares a common PWM ramp signal.

In practice, each buck regulator will regulate to a slightly different output voltage due to mismatching of the PWM comparators, slope of the PWM ramp (output voltage ripple), and propagation delays. At light loads, the results can be very poor current sharing. With zero output current, some regulators may be sourcing current while others may be sinking current.

This results in additional power dissipation and lower efficiency than would be obtained by a single regulator. This is usually not an issue since efficiency is most important when a supply is fully loaded.

This effect is similar to the difference in efficiency between synchronous and non-synchronous buck regulators. Synchronous buck regulators have lower efficiency at light loads because inductor current is always continuous, flowing from the load to ground during switch off-time through the synchronous rectifier. Under full load conditions, the synchronous design is more efficient due to the lower voltage drop across the synchronous rectifier. Likewise, the efficiency of droop sharing regulators will be lower at light loads due to the continuous current flow in the droop resistors. Efficiency at heavy loads tends to be higher due to reduced $\mathrm{I}^{2} \mathrm{R}$ losses.

The output current of each regulator can be calculated from:

$$
\mathrm{I}_{\mathrm{N}}=\frac{(\mathrm{VOUT}(\mathrm{~N})-\mathrm{VOUT})}{\operatorname{RDROOP}(\mathrm{N})}
$$

where: $\mathrm{V}_{\mathrm{OUT}(\mathrm{N})}$ and $\mathrm{R}_{\mathrm{DROOP}(\mathrm{N})}$ are the output voltage and droop resistance of a particular regulator and $\mathrm{V}_{\text {OUT }}$ is the system output voltage. Output current is the sum of each regulator's current:

$$
\text { IOUT }=\mathrm{I} 1+\mathrm{I} 2+\ldots+\mathrm{IN}
$$

Current sharing improves with increasing load current. The increasing voltage drop across the droop resistor due to increasing load current eventually swamps out the differences in regulator output voltages. If a large enough voltage can be developed across the droop resistors, current sharing accuracy will be determined solely by their matching. To realize the benefits of current sharing, it is not
necessary to obtain perfect matching. Keeping output currents within $\pm 10 \%$ is usually acceptable.
For microprocessor applications, the value of the droop resistor must be selected to optimize adaptive voltage positioning, current sharing, current limit and efficiency. Current sharing is realized by simply connecting the COMP pins of the respective buck regulators, as shown in Figure 31.

Figure 32 shows operation with no load. In this case, there is insufficient output voltage ripple across the droop resistor to produce complete synchronization. Duty Cycle is close to the theoretical $56 \%\left(\mathrm{~V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}}\right)$ resulting in a switching frequency of approximately 275 kHz .
Figure 34 shows operation with a 30 Amp load. Synchronization between the two regulators is now obtained due to increased ripple voltage. Increases losses cause the $\mathrm{V}^{2}$ control loop to increase on-time to compensate. This results in a larger duty cycle and a corresponding decrease in switching frequency to 233 kHz .


Trace 1 = Output voltage ripple.
Trace 2 = Buck regulator \#1 inductor switching node.
Trace 3 = Buck regulator \#2 inductor switching node.
Figure 32. No Load Waveforms


Trace 1 = Output voltage ripple.
Trace 2 = Buck regulator \#1 inductor switching node. Trace 3 = Buck regulator \#2 inductor switching node.

Figure 33. 15 A Load Transient Waveforms


Trace 1 = Output voltage ripple.
Trace 2 = Buck regulator \#1 inductor switching node.
Trace 3 = Buck regulator \#2 inductor switching node.
Figure 34. 30 A Load Waveforms
Figure 33 shows supply response to a 15 A load step with a $30 \mathrm{~A} / \mu \mathrm{s}$ slew rate. The $\mathrm{V}^{2}$ control loop immediately forces the duty cycle to $100 \%$, ramping the current in both inductors up. A voltage spike of 136 mV due to output capacitor impedance occurs. The inductive component of the spike due to ESL recovers within several microseconds. The resistive component due to ESR decreases as inductor current replaces capacitor current.

The benefit of adaptive voltage positioning in reducing the voltage spike can readily be seen. The difference in DC voltage and duty cycle can also be observed. This particular transient occurred near the beginning of regulator off time, resulting in a longer recovery time and increased voltage spike.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## Inductor Ripple Current

$$
\text { Ripple Current }=\frac{\left[\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{V}_{\mathrm{OUT}}\right]}{\left(\text { Switching Frequency } \times \mathrm{L} \times \mathrm{V}_{\mathrm{IN}}\right)}
$$

Example: $\mathrm{V}_{\mathrm{IN}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=+2.8 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=14.2 \mathrm{~A}$, $\mathrm{L}=1.2 \mu \mathrm{H}$, Freq $=200 \mathrm{kHz}$

$$
\text { Ripple Current }=\frac{[(5.0 \mathrm{~V}-2.8 \mathrm{~V}) \times 2.8 \mathrm{~V}]}{[200 \mathrm{kHz} \times 1.2 \mu \mathrm{H} \times 5.0 \mathrm{~V}]}=5.1 \mathrm{~A}
$$

## Output Ripple Voltage

VRIPPLE $=$ Inductor Ripple Current $\times$ Output Capacitor ESR

## Example:

$\mathrm{V}_{\text {IN }}=+5.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=+2.8 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=14.2 \mathrm{~A}, \mathrm{~L}=1.2 \mu \mathrm{H}$, Switching Frequency $=200 \mathrm{kHz}$

Output Ripple Voltage $=5.1 \mathrm{~A} \times$ Output Capacitor ESR (from manufacturer's specs)

ESR of Output Capacitors to limit Output Voltage Spikes

$$
\mathrm{ESR}=\frac{\Delta \mathrm{V} \mathrm{OUT}}{\Delta \mathrm{I} \mathrm{OUT}}
$$

This applies for current spikes that are faster than regulator response time. Printed Circuit Board resistance will add to the ESR of the output capacitors.

In order to limit spikes to 100 mV for a 14.2 A Load Step, $\mathrm{ESR}=0.1 / 14.2=0.007 \Omega$

## Inductor Peak Current

Peak Current $=$ Maximum Load Current $+\left(\frac{\text { Ripple Current }}{2}\right)$
Example: $\mathrm{V}_{\mathrm{IN}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=+2.8 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=14.2 \mathrm{~A}$, $\mathrm{L}=1.2 \mu \mathrm{H}$, Freq $=200 \mathrm{kHz}$

$$
\text { Peak Current }=14.2 \mathrm{~A}+(5.1 / 2)=16.75 \mathrm{~A}
$$

A key consideration is that the inductor must be able to deliver the Peak Current at the switching frequency without saturating.

## Response Time to Load Increase

(limited by Inductor value unless Maximum On-Time is exceeded)

$$
\text { Response Time }=\frac{\mathrm{L} \times \Delta \mathrm{l} \text { OUT }}{\left(\mathrm{V} \mathrm{~V}, ~-\mathrm{V}_{\mathrm{OUT}}\right)}
$$

Example: $\mathrm{V}_{\mathrm{IN}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=+2.8 \mathrm{~V}, \mathrm{~L}=1.2 \mu \mathrm{H}, 14.2 \mathrm{~A}$ change in Load Current

$$
\text { Response Time }=\frac{1.2 \mu \mathrm{H} \times 14.2 \mathrm{~A}}{(5.0 \mathrm{~V}-2.8 \mathrm{~V})}=7.7 \mu \mathrm{~s}
$$

## Response Time to Load Decrease

(limited by Inductor value)

$$
\text { Response Time }=\frac{\mathrm{L} \times \text { Change in IOUT }}{\text { VOUT }}
$$

Example: $\mathrm{V}_{\text {OUT }}=+2.8 \mathrm{~V}, 14.2$ A change in Load Current, $\mathrm{L}=1.2 \mu \mathrm{H}$

$$
\text { Response Time }=\frac{1.2 \mu \mathrm{H} \times 14.2 \mathrm{~A}}{2.8 \mathrm{~V}}=6.1 \mu \mathrm{~s}
$$

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$
\text { Thermal Impedance }=\frac{\mathrm{T}_{\mathrm{J}}(\mathrm{MAX})-\mathrm{T}_{\mathrm{A}}}{\text { Power }}
$$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 35. Filter Components


Figure 36. Input Filter

## Layout Guidelines

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS5166H.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections. Avoid connecting the IC GND (LGND) between the source of the lower FET and the input capacitor GND.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double-sided PCBs a single large ground plane (usually the bottom) is recommended.
5. Even though double sided PCBs are usually sufficient for a good layout, four-layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the +5.0 V and GND planes, the top layer for the power connections and component vias, and the bottom layer for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The FET gate traces to the IC must be as short, straight, and wide as possible. Ideally, the IC has to be placed right next to the FETs.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching FET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the $\mathrm{V}_{\mathrm{FB}}$ filter resistor in series with the $\mathrm{V}_{\mathrm{FB}}$ pin (pin 16) right at the pin.
12. Place the $\mathrm{V}_{\mathrm{FB}}$ filter capacitor right at the $\mathrm{V}_{\mathrm{FB}}$ pin (pin 16).
13. The "Droop" Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
14. Place the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor as close as possible to the $\mathrm{V}_{\mathrm{CC}}$ pin and connect it to the PGND pin of the IC. Connect the PGND pin directly to the GND plane.
15. Create a subground (local GND) plane preferably on the PCB top layer and under the IC controller. Connect all logic capacitor returns and the LGND pin of the IC to this place. Connect the subground plane to the main GND plane using a minimum of four (4) vias.


Figure 37. Additional Application Diagram, +12 V to +2.8 V @ 14.2 A for 300 MHz Pentium II


Figure 38. Additional Application Diagram, +5.0 V to +2.8 V @ 14.2 A for 300 MHz Pentium II

## CS5166H

PACKAGE THERMAL DATA

| Parameter |  | SO-16L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 23 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {OJA }}$ | Typical | 105 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS51312

## Synchronous CPU Buck Controller for 12 V Only Applications

The CS51312 is a synchronous dual NFET Buck Regulator Controller. It is designed to power the core logic of the latest high performance CPUs and ASICs from a single 12 V input. It uses the $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation. It incorporates many additional features required to ensure the proper operation and protection of the CPU and Power system. The CS51312 provides the industry's most highly integrated solution, minimizing external component count, total solution size, and cost.

The CS51312 is specifically designed to power Intel's Pentium® II processor and includes the following features: 5-bit DAC with $1.2 \%$ tolerance, Power-Good output, overcurrent hiccup mode protection, overvoltage protection, $\mathrm{V}_{\mathrm{CC}}$ monitor, Soft Start, adaptive voltage positioning, adaptive FET non-overlap time, and remote sense. The CS51312 will operate over a 9.0 V to $20 \mathrm{~V}\left(\mathrm{~V}_{\mathrm{CC} 2}\right)$ range using either single or dual input voltage and is available in 16 lead narrow body surface mount package.

## Features

- Synchronous Switching Regulator Controller for CPU VCORE
- Dual N-Channel MOSFET Synchronous Buck Design
- $\mathrm{V}^{2}$ Control Topology
- 200 ns Transient Loop Response
- 5-Bit DAC with $1.2 \%$ Tolerance
- Hiccup Mode Overcurrent Protection
- 40 ns Gate Rise and Fall Times (3.3nF Load)
- 65 ns Adaptive FET Non-Overlap Time
- Adaptive Voltage Positioning
- Power Good Output Monitors Regulator Output
- 5.0 V/12 V or $12 \mathrm{~V}-$ Only Operation
- $\mathrm{V}_{\mathrm{CC}}$ Monitor Provides Undervoltage Lockout
- OVP Output Monitors Regulator Output
- Multifunctional COMP Pin Provides ENABLE, Soft Start, and Hiccup Timing in Addition to Control Loop Compensation


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51312GD16 | SO-16 | 48 Units/Rail |
| CS51312GDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, 12 V to 16 A High Performance Converter

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility | 2.0 | kV |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Bias and Low Side Driver Power Input | $\mathrm{V}_{\mathrm{CC} 1}$ | 16 | -0.3 | N/A | 1.5 A Peak, 200 mA DC |
| IC High Side Driver Power Input | $\mathrm{V}_{\mathrm{CC} 2}$ | 20 V | -0.3 V | N/A | 1.5 A Peak, 200 mA DC |
| Compensation Pin | COMP | 6.0 V | -0.3 V | 1.0 mA | 5.0 mA |
| Voltage Feedback Input, Output Voltage Sense Pin, Voltage ID DAC Inputs | $\mathrm{V}_{\text {FB }}, \mathrm{V}_{\text {OUT }}, \mathrm{V}_{\text {IDO-4 }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Off-Time Pin | $\mathrm{C}_{\text {OFF }}$ | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| High-Side FET Driver | GATE(H) | 20 V | -0.3 V DC | 1.5 A Peak, 200 mA DC | 1.5 A Peak, 200 mA DC |
| Low-Side FET Driver | GATE(L) | 16 V | -0.3 V DC | 1.5 A Peak, 200 mA DC | 1.5 A Peak, 200 mA DC |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | 1.0 mA | 30 mA |
| Overvoltage Protection | OVP | 15 V | -0.3 V | 30 mA | 1.0 mA |
| Ground | GND | 0 V | 0 V | 1.5 A Peak, 200 mA DC | N/A |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC} 2} \leq 20 \mathrm{~V}\right.$;
2.0 V DAC Code ( $\left.\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified. .

| Characteristic | Test Conditions |  |
| :---: | :---: | :---: |

Voltage Identification DAC

|  |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}}, \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$. Note 2 |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  | $75^{\circ} \mathrm{C} \leq \mathrm{T}$ | $\leq 125^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C} \leq$ | $\leq 75^{\circ} \mathrm{C}$ |  |  |
| $\mathrm{V}_{\text {ID4 }}$ | $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $\mathrm{V}_{\text {IDO }}$ | Min | Typ | Max | $\pm$ Tol | Min | Typ | Max | $\pm$ Tol | Unit |
| 1 | 0 | 0 | 0 | 0 | 3.483 | 3.525 | 3.567 | 1.2\% | 3.455 | 3.525 | 3.596 | 2.0\% | V |
| 1 | 0 | 0 | 0 | 1 | 3.384 | 3.425 | 3.466 | 1.2\% | 3.357 | 3.425 | 3.494 | 2.0\% | V |
| 1 | 0 | 0 | 1 | 0 | 3.285 | 3.325 | 3.365 | 1.2\% | 3.259 | 3.325 | 3.392 | 2.0\% | V |
| 1 | 0 | 0 | 1 | 1 | 3.186 | 3.225 | 3.264 | 1.2\% | 3.161 | 3.225 | 3.290 | 2.0\% | V |
| 1 | 0 | 1 | 0 | 0 | 3.087 | 3.125 | 3.163 | 1.2\% | 3.063 | 3.125 | 3.188 | 2.0\% | V |
| 1 | 0 | 1 | 0 | 1 | 2.989 | 3.025 | 3.061 | 1.2\% | 2.965 | 3.025 | 3.086 | 2.0\% | V |
| 1 | 0 | 1 | 1 | 0 | 2.890 | 2.925 | 2.960 | 1.2\% | 2.875 | 2.925 | 2.975 | 1.7\% | V |
| 1 | 0 | 1 | 1 | 1 | 2.791 | 2.825 | 2.859 | 1.2\% | 2.777 | 2.825 | 2.873 | 1.7\% | V |
| 1 | 1 | 0 | 0 | 0 | 2.692 | 2.725 | 2.758 | 1.2\% | 2.679 | 2.725 | 2.771 | 1.7\% | V |
| 1 | 1 | 0 | 0 | 1 | 2.594 | 2.625 | 2.657 | 1.2\% | 2.580 | 2.625 | 2.670 | 1.7\% | V |
| 1 | 1 | 0 | 1 | 0 | 2.495 | 2.525 | 2.555 | 1.2\% | 2.482 | 2.525 | 2.568 | 1.7\% | V |
| 1 | 1 | 0 | 1 | 1 | 2.396 | 2.425 | 2.454 | 1.2\% | 2.389 | 2.425 | 2.461 | 1.5\% | V |
| 1 | 1 | 1 | 0 | 0 | 2.297 | 2.325 | 2.353 | 1.2\% | 2.290 | 2.325 | 2.360 | 1.5\% | V |
| 1 | 1 | 1 | 0 | 1 | 2.198 | 2.225 | 2.252 | 1.2\% | 2.192 | 2.225 | 2.258 | 1.5\% | V |
| 1 | 1 | 1 | 1 | 0 | 2.099 | 2.125 | 2.151 | 1.2\% | 2.093 | 2.125 | 2.157 | 1.5\% | V |
| 0 | 0 | 0 | 0 | 0 | 2.050 | 2.075 | 2.100 | 1.2\% | 2.044 | 2.075 | 2.106 | 1.5\% | V |
| 0 | 0 | 0 | 0 | 1 | 2.001 | 2.025 | 2.049 | 1.2\% | 1.995 | 2.025 | 2.055 | 1.5\% | V |
| 0 | 0 | 0 | 1 | 0 | 1.953 | 1.975 | 1.997 | 1.1\% | 1.945 | 1.975 | 2.005 | 1.5\% | V |
| 0 | 0 | 0 | 1 | 1 | 1.904 | 1.925 | 1.946 | 1.1\% | 1.896 | 1.925 | 1.954 | 1.5\% | V |
| 0 | 0 | 1 | 0 | 0 | 1.854 | 1.875 | 1.896 | 1.1\% | 1.847 | 1.875 | 1.903 | 1.5\% | V |
| 0 | 0 | 1 | 0 | 1 | 1.805 | 1.825 | 1.845 | 1.1\% | 1.798 | 1.825 | 1.852 | 1.5\% | V |
| 0 | 0 | 1 | 1 | 0 | 1.755 | 1.775 | 1.795 | 1.1\% | 1.748 | 1.775 | 1.802 | 1.5\% | V |
| 0 | 0 | 1 | 1 | 1 | 1.706 | 1.725 | 1.744 | 1.1\% | 1.699 | 1.725 | 1.751 | 1.5\% | V |
| 0 | 1 | 0 | 0 | 0 | 1.656 | 1.675 | 1.694 | 1.1\% | 1.650 | 1.675 | 1.700 | 1.5\% | V |
| 0 | 1 | 0 | 0 | 1 | 1.607 | 1.625 | 1.643 | 1.1\% | 1.601 | 1.625 | 1.649 | 1.5\% | V |
| 0 | 1 | 0 | 1 | 0 | 1.558 | 1.575 | 1.593 | 1.1\% | 1.551 | 1.575 | 1.599 | 1.5\% | V |
| 0 | 1 | 0 | 1 | 1 | 1.508 | 1.525 | 1.542 | 1.1\% | 1.502 | 1.525 | 1.548 | 1.5\% | V |
| 0 | 1 | 1 | 0 | 0 | 1.459 | 1.475 | 1.491 | 1.1\% | 1.453 | 1.475 | 1.497 | 1.5\% | V |
| 0 | 1 | 1 | 0 | 1 | 1.409 | 1.425 | 1.441 | 1.1\% | 1.404 | 1.425 | 1.446 | 1.5\% | V |
| 0 | 1 | 1 | 1 | 0 | 1.360 | 1.375 | 1.390 | 1.1\% | 1.354 | 1.375 | 1.396 | 1.5\% | V |
| 0 | 1 | 1 | 1 | 1 | 1.310 | 1.325 | 1.340 | 1.1\% | 1.305 | 1.325 | 1.345 | 1.5\% | V |
| 1 | 1 | 1 | 1 | 1 | 1.225 | 1.250 | 1.275 | 2.0\% | 1.225 | 1.250 | 1.275 | 2.0\% | V |

2. The IC power dissipation in a typical application with $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$, switching frequency $\mathrm{f}_{\mathrm{SW}}=250 \mathrm{kHz}, 50 \mathrm{nc}$ MOSFETs and $\mathrm{R}_{\theta \mathrm{JA}}=115^{\circ} \mathrm{C} / \mathrm{W}$ yields an operating junction temperature rise of approximately $52^{\circ} \mathrm{C}$, and a junction temperature of $77^{\circ} \mathrm{C}$ with an ambient temperature of $25^{\circ} \mathrm{C}$.

## CS51312

ELECTRICAL CHARACTERISTICS (continued) ( $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}$; $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$; $9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC} 2} \leq 20 \mathrm{~V}$; 2.0 V DAC Code ( $\left.\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}$, $\mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| VoItage Identification DAC (continued) | $9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 14 \mathrm{~V}$ | - | 0.01 | - | $\% / \mathrm{V}$ |
| Line Regulation | $\mathrm{V}_{\mathrm{ID} 4}, \mathrm{~V}_{\mathrm{ID} 3}, \mathrm{~V}_{\mathrm{ID} 2}, \mathrm{~V}_{\mathrm{ID} 1}, \mathrm{~V}_{\mathrm{ID} 0}$ | 1.0 | 1.25 | 2.4 | V |
| Input Threshold | $\mathrm{V}_{\mathrm{ID} 4}, \mathrm{~V}_{\mathrm{ID} 3}, \mathrm{~V}_{\mathrm{ID} 2}, \mathrm{~V}_{\mathrm{ID} 1}, \mathrm{~V}_{\mathrm{ID} 0}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Input Pull-Up Resistance | - | 5.48 | 5.65 | 5.82 | V |
| Pull-Up Voltage |  |  |  |  |  |

## Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $0.2 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 3.5 \mathrm{~V}$ | -7.0 | 0.1 | 7.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| COMP Source Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V}$ to $3.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.9 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| COMP Sink Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.1 \mathrm{~V}$ | 30 | 60 | 120 | $\mu \mathrm{~A}$ |
| Open Loop Gain | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 80 | - | dB |
| Unity Gain Bandwidth | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 50 | - | kHz |
| PSRR @ 1.0 kHz | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 70 | - | dB |
| Transconductance |  | - | 32 | - | mmho |
| Output Impedance | - | - | 0.5 | - | $\mathrm{M} \Omega$ |

GATE(H) and GATE(L)

| High Voltage at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1 / 2}-\mathrm{GATE}(\mathrm{L}) /(\mathrm{H})$ | - | 1.2 | 2.1 | V |
| :--- | :--- | :--- | :--- | :--- | :---: |
| Low Voltage at 100 mA | Measure $\mathrm{GATE}(\mathrm{L}) /(\mathrm{H})$ | - | 1.0 | 1.5 | V |
| Rise Time | $1.6 \mathrm{~V}<\mathrm{GATE}(\mathrm{H}) /(\mathrm{L})<\left(\mathrm{V}_{\mathrm{CC} 1 / 2}-2.5 \mathrm{~V}\right)$ | - | 40 | 80 | ns |
| Fall Time | $\left(\mathrm{V}_{\mathrm{CC} 1 / 2}-2.5 \mathrm{~V}\right)>\operatorname{GATE}(\mathrm{L}) /(\mathrm{H})>1.6 \mathrm{~V}$ | - | 40 | 80 | ns |
| GATE $(\mathrm{H})$ to GATE(L) Delay | $\mathrm{GATE}(\mathrm{H})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{~L})>2.0 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{CC} 1 / 2}=12 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE(L) to GATE(H) Delay | $\mathrm{GATE}(\mathrm{L})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{H})>2.0 \mathrm{~V}$, <br> $V_{\mathrm{CC} 1 / 2}=12 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-Down | Resistance to GND. Note 3 | 20 | 50 | 115 | $\mathrm{k} \Omega$ |

Overcurrent Protection

| OVC Comparator Offset Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 3.5 \mathrm{~V}$ | 77 | 86 | 101 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Threshold Voltage | - | 0.2 | 0.25 | 0.3 | V |
| $V_{\text {OUT }}$ Bias Current | $0.2 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 3.5 \mathrm{~V}$ | -7.0 | 0.1 | 7.0 | $\mu \mathrm{~A}$ |
| OVC Latch Discharge Current | $\mathrm{V}_{\text {COMP }}=1.0 \mathrm{~V}$ | 100 | 800 | 2500 | $\mu \mathrm{~A}$ |

## PWM Comparator

| PWM Comparator Offset Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 3.5 \mathrm{~V}$ | 0.99 | 1.1 | 1.23 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Transient Response | $\mathrm{V}_{\mathrm{FB}}=0$ to 3.5 V | - | 200 | 300 | ns |

Coff

| Off-Time |  | 1.0 | 1.6 | 2.3 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Charge Current | $\mathrm{V}_{\text {COFF }}=1.5 \mathrm{~V}$ | - | 550 | - | $\mu \mathrm{A}$ |
| Discharge Current | $\mathrm{V}_{\text {COFF }}=1.5 \mathrm{~V}$ | - | 25 | - | mA |

3. Guaranteed by design, not $100 \%$ tested in production.

## CS51312

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}\right.$; $9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC} 2} \leq 20 \mathrm{~V}$; 2.0 V DAC Code ( $\left.\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}$, $\mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output |  |  |  |  |  |
| PWRGD Sink Current | $\mathrm{V}_{\mathrm{FB}}=1.7 \mathrm{~V}, \mathrm{~V}_{\text {PWRGD }}=1.0 \mathrm{~V}$ | 0.5 | 4.0 | 15 | mA |
| PWRGD Upper Threshold | \% of Nominal DAC Code | 5.0 | 8.5 | 12 | \% |
| PWRGD Lower Threshold | \% of Nominal DAC Code | -12 | -8.5 | -5.0 | \% |
| PWRGD Output Low Voltage | $\mathrm{V}_{\text {FB }}=1.7 \mathrm{~V}, \mathrm{I}_{\text {PWRGD }}=500 \mu \mathrm{~A}$ | - | 0.2 | 0.3 | V |

## Overvoltage Protection (OVP) Output

| OVP Source Current | OVP $=1.0 \mathrm{~V}$ | 1.0 | 10 | 25 |
| :--- | :--- | :---: | :---: | :---: |
| OVP Threshold | $\%$ of Nominal DAC Code | 5.0 | 8.5 | 12 |
| OVP Pull-Up Voltage | IOVP $=1.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC} 1}-\mathrm{V}_{\text {OVP }}$ | - | 1.1 | 1.5 |

General Electrical Specifications

| $\mathrm{V}_{\mathrm{CC} 1}$ Monitor Start Threshold | 8 | 7.9 | 8.4 | 8.9 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{CC} 1}$ Monitor Stop Threshold | - | 7.6 | 8.1 | 8.6 | V |
| Hysteresis | Start-Stop | 0.15 | 0.3 | 0.6 | V |
| $\mathrm{~V}_{\mathrm{CC} 1}$ Supply Current | No Load on GATE(H), GATE(L) | - | 9.5 | 16 | mA |
| $\mathrm{~V}_{\mathrm{CC} 2}$ Supply Current | No Load on GATE(H), GATE(L) | - | 2.5 | 4.5 | mA |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-16 | PIN SYMBOL | FUNCTION |
| 1, 2, 3, 4, 5 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | Voltage ID DAC inputs. These pins are internally pulled up to 5.65 V if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is high (logic one), the Error Amp reference range is 2.125 V to 3.525 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is low (logic zero), the Error Amp reference voltage is 1.325 V to 2.075 V with 50 mV increments. |
| 6 | $V_{F B}$ | Error amp inverting input, PWM comparator non-inverting input, current limit comparator non-inverting input, PWRGD and OVP comparator input. |
| 7 | Vout | Current limit comparator inverting input. |
| 8 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power supply pin for the internal circuitry and low side gate driver. Decouple with filter capacitor to GND. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Input power supply pin for the high side gate driver. Decouple with filter capacitor to GND. |
| 10 | GATE(H) | High side switch FET driver pin. |
| 11 | GND | Ground pin and IC substrate connection. |
| 12 | GATE(L) | Low side synchronous FET driver pin. |
| 13 | OVP | Overvoltage protection pin. Drives high when overvoltage condition is detected on $V_{F B}$. |
| 14 | PWRGD | Power Good Output. Open collector output drives low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. |
| 15 | $\mathrm{C}_{\text {OFF }}$ | Off-Time Capacitor pin. A capacitor from this pin to GND sets the off time for the regulator. |
| 16 | COMP | Error amp output. PWM comparator inverting input. A capacitor on this pin provides error amp compensation, and determines the Soft Start and hiccup timing. Pulling COMP below $1.1 \mathrm{~V}(\mathrm{typ})$ turns off both GATE drivers and shuts down the regulator. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. GATE(H) and GATE(L) Falltime vs. Load Capacitance


Figure 5. DAC Output Voltage vs. Temperature, DAC Code = 00001


Figure 4. GATE(H) and GATE(L) Risetime vs. Load Capacitance


Figure 6. Percent Output Error vs. DAC Output Voltage Setting, VID4 $=0$


Figure 7. Percent Output Error vs. DAC Output Voltage Setting, VID4 $=1$

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## V $^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

The $\mathrm{V}^{2}$ control method is illustrated in Figure 8. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.


Figure 8. $\mathbf{V}^{2}$ Control Diagram
A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop.

The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.
Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation.
A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off-Time

To minimize transient response, the CS51312 uses a Constant Off-Time method to control the rate of output pulses. During normal operation, the Off-Time of the high side switch is terminated after a fixed period, set by the C OFF capacitor. Every time the $\mathrm{V}_{\mathrm{FB}}$ pin exceeds the COMP pin voltage an Off-Time is initiated. To maintain regulation, the $\mathrm{V}^{2}$ Control Loop varies switch On-Time. The PWM comparator monitors the output voltage ramp, and terminates the switch On-Time.
Constant Off-Time provides a number of advantages. Switch Duty Cycle can be adjusted from 0 to $100 \%$ on a pulse-by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ Duty Cycle operation can be maintained for extended periods of time in response to Load or Line transients.

## Programmable Output

The CS51312 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.125 V to 3.525 V in 100 mV steps, the second is 1.325 V to 2.075 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS51312 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ pin, as in traditional controllers. The CS51312 is specifically designed to meet or exceed Intel's Pentium II specifications.

## Error Amplifier

The COMP pin is the output of the error amplifier. A capacitor to GND compensates the error amplifier loop.

Additionally, the built in offset on the PWM Comparator non-inverting input provides the hiccup timing for the Overcurrent Protection, Soft Start function, and regulator output enable.

## $\mathrm{V}_{\mathrm{CC} 2}$ Charge Pump

In order to fully turn on the high side NFET, a voltage greater than the input voltage must be applied to $\mathrm{V}_{\mathrm{CC} 2}$ to bias the GATE(H) driver. Referring to the application diagram on page 2120; a simple charge pump circuit can be implemented for this purpose through capacitor C6, resistor R1, and diodes D1 and D2. The input voltage, less the drop in D1 is stored in C6 during the off-time period. When the high-side FET turns on, it drives the inductor switching node and C6 high causing Schottky diode D1 to reverse bias. The charge stored in C 6 is transferred to $\mathrm{V}_{\mathrm{CC} 2}$ through R1. Zener diode D 2 clamps the $\mathrm{V}_{\mathrm{CC} 2}$ voltage to 18 V to prevent the $\mathrm{V}_{\mathrm{CC} 2}$ from exceeding its 20 V Max rating (see Figure 9).


Figure 9. $\mathrm{V}_{\mathrm{CC} 2}$ Charge Pump Operation ( $1.0 \mu \mathrm{~s} / \mathrm{div}$ )

## Startup

The CS51312 provides a controlled startup of regulator output voltage and features Programmable Soft Start implemented through the Error Amp and external Compensation Capacitor. This feature, combined with overcurrent protection, prevents stress to the regulator power components and overshoot of the output voltage during startup.

As Power is applied to the regulator, the CS51312 Undervoltage Lockout circuit (UVL) monitors the ICs supply voltage ( $\mathrm{V}_{\mathrm{CC} 1}$ ) which is typically connected to the +12 V input. The UVL circuit prevents the NFET gates from being activated until $\mathrm{V}_{\mathrm{CC} 1}$ exceeds the 8.4 V (typ) threshold. Hysteresis of 300 mV (typ) is provided for noise immunity.

The Error Amp Capacitor connected to the COMP pin is charged by a $30 \mu \mathrm{~A}$ current source. This capacitor must be charged to 1.1 V (typ) so that it exceeds the PWM comparator's offset before the $\mathrm{V}^{2}$ PWM control loop permits switching to occur.
When $\mathrm{V}_{\mathrm{CC} 1}$ has exceeded 8.4 V and COMP has charged to 1.1 V , the upper Gate driver ( $\operatorname{GATE}(\mathrm{H})$ ) is activated, turning on the upper FET. This causes current to flow through the output inductor and into the output capacitors and load according to the following equation:

$$
\mathrm{I}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{T}}{\mathrm{~L}}
$$

GATE(H) and the upper NFET remain on and inductor current ramps up until the initial pulse is terminated by either the PWM control loop or the overcurrent protection. This initial surge of in-rush current minimizes startup time, but avoids overstressing of the regulator's power components.
The PWM comparator will terminate the initial pulse if the regulator output exceeds the voltage on the COMP pin plus the 1.1 V PWM comparator offset prior to the drop across the current sense resistor exceeding the current limit threshold. In this case, the PWM control loop has achieved regulation and the initial pulse is then followed by a constant off time as programmed by the C $\mathrm{C}_{\text {OFF }}$ capacitor. The COMP capacitor will continue to slowly charge and the regulator output voltage will follow it, less the 1.1 V PWM offset, until it achieves the voltage programmed by the DAC's VID input. The Error Amp will then source or sink current to the COMP cap as required to maintain the correct regulator DC output voltage. Since the rate of increase of the COMP pin voltage is typically set much slower than the regulator's slew capability, inrush current, output voltage, and duty cycle all gradually increase from zero. (See Figures 10 and 11).


Channel 1 - Regulator Input Voltage and $\mathrm{V}_{\mathrm{CC} 1}$ (10 V/div)
Channel 2 - COMP (2.0 V/div)
Channel 3 - Regulator Output Voltage (1.0 V/div)
Figure 10. Normal Startup ( $5.0 \mathrm{~ms} / \mathrm{div}$ )


Channel 1 - VCC2 (10 V/div)
Channel 2 - GATE(H) (10 V/div)
Channel 3 - Inductor Switching Node (10 V/div)
Channel 4 - Regulator Output Voltage ( $2.0 \mathrm{~V} / \mathrm{div}$ )
Figure 11. Normal Startup Showing Initial Pulse Followed by Soft Start ( $5.0 \mu \mathrm{~s} / \mathrm{div}$ )

If the voltage across the Current Sense resistor generates a voltage difference between the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ pins that exceeds the OVC Comparator Offset Voltage ( 86 mV typical), the Fault latch is set. This causes the COMP pin to be quickly discharged, turning off $\operatorname{GATE}(\mathrm{H})$ and the upper NFET since the voltage on the COMP pin is now less than the 1.1 V PWM comparator offset. The Fault latch is reset when the voltage on the COMP decreases below the discharge threshold voltage ( 0.25 V typical). The COMP capacitor will again begin to charge, and when it exceeds the 1.1 V PWM comparator offset, the regulator output will Soft Start normally (see Figure 12).


Channel 1 - Regulator Output Voltage (1.0 V/div)
Channel 2 - COMP Pin (1.0 V/div)
Channel 3 - $\mathrm{V}_{\mathrm{CC}}$ ( $10 \mathrm{~V} / \mathrm{div}$ )
Figure 12. Startup with COMP Pre-Charged to 2.0 V ( $2.0 \mathrm{~ms} / \mathrm{div}$ )

When driving large capacitive loads, the COMP must charge slowly enough to avoid tripping the CS51312 overcurrent protection. The following equation can be used to ensure unconditional startup:

$$
\frac{\text { ICHG }}{\text { CCOMP }}<\frac{\text { ILIM }- \text { ILOAD }^{\text {COUT }}}{}
$$

where:
$\mathrm{I}_{\mathrm{CHG}}=$ COMP Source Current ( $30 \mu \mathrm{~A}$ typical);
$\mathrm{C}_{\text {COMP }}=$ COMP Capacitor value ( $0.1 \mu \mathrm{~F}$ typical);
$\mathrm{I}_{\text {LIM }}=$ Current Limit Threshold;
$\mathrm{I}_{\text {LOAD }}=$ Load Current during startup;
CouT $=$ Total Output Capacitance.

## Normal Operation

During normal operation, Switch Off-Time is constant and set by the C CofF capacitor. Switch On-Time is adjusted by the $\mathrm{V}^{2}$ Control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current and the ESR of the output capacitors

## Transient Response

The CS51312 V ${ }^{2}$ Control Loop's 200 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "Adaptive Voltage Positioning". This technique pre-positions the output capacitors voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifiers reference voltage to be targeted +25 mV high without compromising DC accuracy. A "Droop Resistor" connects the Error Amps feedback pin $\left(\mathrm{V}_{\mathrm{FB}}\right)$ to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +25 mV offset. When the full load current is delivered, a 50 mV drop is developed across this resistor. This results in output voltage being offset -25 mV low.
The benefit of Adaptive Voltage Positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre-positioned +25 mV . Conversely, when load current suddenly decreases from its maximum level, the output capacitor is pre-positioned -25 mV . For
best Transient Response, a combination of a number of high frequency and bulk output capacitors are usually used.

## PROTECTION AND MONITORING FEATURES

## Overcurrent Protection

A hiccup mode current limit protection feature is provided, requiring only the COMP capacitor to implement. The CS51312 provides overcurrent protection by sensing the current through a "Droop" resistor, using an internal current sense comparator. The comparator compares the voltage drop through the "Droop" resistor to an internal reference voltage of 86 mV (typical).

If the voltage drop across the "Droop" resistor exceeds this threshold, the current sense comparator allows the fault latch to be set. This causes the regulator to stop switching.

During this over current condition, the CS51312 stays off for the time it takes the COMP pin capacitor to discharge to its lower 0.25 V threshold. As soon as the COMP pin reaches 0.25 V , the Fault latch is reset (no overcurrent condition present) and the COMP pin is charged with a $30 \mu \mathrm{~A}$ current source to a voltage 1.1 V greater than the $\mathrm{V}_{\mathrm{FB}}$ voltage. Only at this point the regulator attempts to restart normally by delivering short gate pulses to both FETs. This protection scheme minimizes thermal stress to the regulator components, input power supply, and PC board traces, as the over current condition persists. Upon removal of the overload, the fault latch is cleared, allowing normal operation to resume.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns , causing the top MOSFET to shut off, disconnecting the regulator from its input voltage. This results in a "crowbar" action to clamp the output voltage and prevents damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. Additionally, a dedicated Overvoltage protection (OVP) output pin (pin 13) is provided in the CS51312. The OVP signal will go high (overvoltage condition), if the output voltage ( $\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}$ ) exceeds the regulation voltage by $8.5 \%$ of the voltage set by the particular DAC code. The OVP pin can source up to 25 mA of current that can be used to drive an SCR to crowbar the power supply.

## Power Good Circuit

The Power Good pin (pin 14) is an open-collector signal consistent with TTL DC specifications. It is externally pulled up, and is pulled low (below 0.3 V ) when the regulator output voltage typically exceeds $\pm 8.5 \%$ of the nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is $\pm 12 \%$.

## Output Enable

On/off control of the regulator outputs can be implemented by pulling the COMP pins low. It is required to pull the COMP pins below the 1.1 V PWM comparator offset voltage in order to disable switching on the GATE drivers.

## Adaptive FET Non-Overlap

The CS51312 includes circuitry to prevent the simultaneous conduction of both the high and low side NFETs. This is necessary to prevent efficiency reducing "shoot-through" current from flowing from the input voltage to ground through the two NFETs. Prior to either GATE(H) or GATE(L) driving high, the other GATE must reach its low state. Since GATE rise and fall times vary with loading, this results in a variable delay from the start of turn-off until the start of turn-on (see Figure 13).


Channel 1 - GATE(H) (5.0 V/div)
Channel 2 - GATE(L) (5.0 V/div)
Channel 3 - Inductor Switching Node ( $10 \mathrm{~V} /$ div)
Figure 13. Adaptive FET Non-Overlap (100 ns/div)

## CS51312-BASED $V_{\text {CC(CORE) }}$ BUCK REGULATOR DESIGN EXAMPLE

## Step 1: Definition of the Design Specifications

The output voltage tolerance can be affected by any or all of the following reasons:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide an output voltage that will meet the specified tolerance at the load.

The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature.

## Step 2: Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I} \mathrm{OUT} \times\left(\frac{\mathrm{ESL}}{\Delta \mathrm{t}}+\mathrm{ESR}+\frac{\mathrm{tTR}}{\mathrm{COUT}}\right)
$$

where:
$\Delta \mathrm{I}_{\mathrm{OUT}} / \Delta \mathrm{t}=$ load current slew rate;
$\Delta \mathrm{I}_{\text {OUT }}=$ load transient;
$\Delta \mathrm{t}=$ load transient duration time;
$\mathrm{ESL}=$ Maximum allowable ESL including capacitors,
circuit traces, and vias;
ESR = Maximum allowable ESR including capacitors and circuit traces;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time.
The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESR}}}{\Delta \mathrm{I}_{\mathrm{OUT}}}
$$

where $\Delta \mathrm{V}_{\mathrm{ESR}}=$ change in output voltage due to ESR (assigned by the designer).

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESR }}
$$

where:
$E S R_{C A P}=$ maximum ESR per capacitor (specified in manufacturer's data sheet);
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$
\Delta \mathrm{V}_{\mathrm{ESR}}=\Delta \mathrm{I} \text { OUT } \times \mathrm{ESR}_{\mathrm{MAX}}
$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$
\mathrm{ESL}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESL}} \times \Delta \mathrm{t}}{\Delta \mathrm{I}}
$$

where:
$\Delta \mathrm{I} / \Delta \mathrm{T}=$ load current slew rate (as high as $20 \mathrm{~A} / \mu \mathrm{s}$ );
$\Delta \mathrm{V}_{\mathrm{ESL}}=$ change in output voltage due to ESL.
The actual maximum allowable ESL can be determined by using the equation:

$$
\text { ESLMAX }=\frac{E S L C A P}{\text { Number of output capacitors }}
$$

where $\mathrm{ESL}_{\mathrm{CAP}}=$ maximum ESL per capacitor (it is estimated that a $10 \times 12 \mathrm{~mm}$ Aluminum Electrolytic capacitor has approximately 4.0 nH of package inductance).
The actual output voltage deviation due to the actual maximum ESL can then be verified:

$$
\Delta \mathrm{V}_{\mathrm{ESL}}=\frac{\mathrm{ESL}}{\mathrm{MAX} \times \Delta \mathrm{I}}
$$

The designer now must determine the change in output voltage due to output capacitor discharge during the transient:

$$
\Delta \mathrm{V}_{\mathrm{CAP}}=\frac{\Delta \mathrm{l} \times \Delta \mathrm{t} \mathrm{TR}}{\mathrm{COUT}}
$$

where:
$\Delta \mathrm{t}_{\mathrm{TR}}=$ the output voltage transient response time (assigned by the designer);
$\Delta \mathrm{V}_{\mathrm{CAP}}=$ output voltage deviation due to output capacitor discharge;
$\Delta \mathrm{I}=$ Load step.
The total change in output voltage as a result of a load current transient can be verified by the following formula:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{V}_{\mathrm{ESR}}+\Delta \mathrm{V}_{\mathrm{ESL}}+\Delta \mathrm{V}_{\mathrm{CAP}}
$$

## Step 3: Selection of the Duty Cycle, Switching Frequency, Switch On-Time (Ton) and Switch Off-Time (TOfF)

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$
\text { Duty Cycle }=\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\left(\mathrm{V}_{\mathrm{HFET}}+\mathrm{V}_{\mathrm{L}}+\mathrm{V}_{\mathrm{DROOP}}\right)}{\mathrm{V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{LFET}}-\mathrm{V}_{\mathrm{HFET}}-\mathrm{V}_{\mathrm{L}}}
$$

where:
$\mathrm{V}_{\text {OUT }}=$ buck regulator output voltage;
$\mathrm{V}_{\mathrm{HFET}}=$ high side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$;
$\mathrm{V}_{\mathrm{L}}=$ output inductor voltage drop due to inductor wire DC resistance;
$\mathrm{V}_{\text {DROOP }}=$ droop $($ current sense) resistor voltage drop;
$\mathrm{V}_{\mathrm{IN}}=$ buck regulator input voltage;
$\mathrm{V}_{\mathrm{LFET}}=$ low side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$.

## Step3a: Calculation of Switch On-Time

The Switch On-Time (time during which the switching MOSFET in a synchronous buck topology is conducting) is determined by:

$$
\text { TON }=\frac{\text { Duty Cycle }}{\text { FSW }}
$$

where $\mathrm{F}_{\text {SW }}=$ regulator switching frequency selected by the designer.

Higher operating frequencies allow the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

## Step 3b: Calculation of Switch Off-Time

The Switch Off-Time (time during which the switching MOSFET is not conducting) can be determined by:

$$
\text { TOFF }=\frac{1.0}{\mathrm{FSW}}-\mathrm{TON}
$$

The $\mathrm{C}_{\mathrm{OFF}}$ capacitor value has to be selected in order to set the Off-Time, $\mathrm{T}_{\text {OFF }}$, above:

$$
\text { COFF }=\frac{\text { Period } \times(1.0-\mathrm{D})}{3980}
$$

where:
3980 is a characteristic factor of the CS51312;
D = Duty Cycle.

## Step 4: Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due to their high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The inductor value can be determined by:

$$
\mathrm{L}=\frac{\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{tTR}}{\Delta \mathrm{I}}
$$

where:
$\mathrm{V}_{\mathrm{IN}}=$ input voltage;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time (assigned by the designer);
$\Delta \mathrm{I}=$ load transient.
The inductor ripple current can then be determined:

$$
\Delta \mathrm{I}_{\mathrm{L}}=\frac{\mathrm{VOUT} \times \mathrm{TOFF}}{\mathrm{~L}}
$$

where:
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{T}_{\mathrm{OFF}}=$ switch Off-Time;
$\mathrm{L}=$ inductor value.
The designer can now verify if the number of output capacitors from Step 2 will provide an acceptable output voltage ripple ( $1.0 \%$ of output voltage is common). The formula below is used:

$$
\Delta \mathrm{l}_{\mathrm{L}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\mathrm{ESR} \mathrm{MAX}^{2}}
$$

Rearranging we have:

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{I}_{\mathrm{L}}}
$$

where
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR ;
$\Delta \mathrm{V}_{\text {OUT }}=1.0 \% \times \mathrm{V}_{\text {OUT }}=$ maximum allowable output voltage ripple ( budgeted by the designer );
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage .
The number of output capacitors is determined by:

$$
\text { Number of capacitors }=\frac{\mathrm{ESR}_{\mathrm{CAP}}}{\mathrm{ESR}_{\mathrm{MAX}}}
$$

where $\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$
\mathrm{I}(\mathrm{PEAK})=\mathrm{IOUT}+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2.0}
$$

where:
$\mathrm{I}_{\mathrm{L}(\mathrm{PEAK})}=$ inductor peak current;
$\mathrm{I}_{\text {OUT }}=$ load current;
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current.

$$
\mathrm{IL}(\mathrm{VALLEY})=\mathrm{IOUT}-\frac{\Delta \mathrm{IL}}{2.0}
$$

where $\mathrm{I}_{\mathrm{L}(\mathrm{VALLEY})}=$ inductor valley current .

## Step 5: Selection of the Input Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines. A key specification for input capacitors is their ripple current rating. The input capacitor should also be able to handle the input RMS current $\mathrm{I}_{\mathrm{IN}(\mathrm{RMS})}$.

The combination of the input capacitors $\mathrm{C}_{\text {IN }}$ discharges during the on-time.

The input capacitor discharge current is given by:
ICINDIS(RMS) =

$$
\sqrt{\frac{\left(\begin{array}{l}
\mathrm{IL}(\mathrm{PEAK})^{2} \\
+(\mathrm{IL}(\mathrm{PEAK}) \times \operatorname{IL}(\mathrm{VALLEY})) \\
+\mathrm{IL}(\mathrm{VALLEY})^{2}
\end{array}\right.}{} \sqrt{3.0}}
$$

where:
$\mathrm{I}_{\mathrm{CINDIS}(\mathrm{RMS})}=$ input capacitor discharge current;
$\mathrm{I}_{\mathrm{L}(\text { PEAK })}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current.
$\mathrm{C}_{\text {IN }}$ charges during the off-time, the average current through the capacitor over one switching cycle is zero:

$$
\operatorname{ICIN}(C H)=\operatorname{ICIN}(D I S) \times \frac{D}{1.0-D}
$$

where:
$\mathrm{I}_{\mathrm{CIN}(\mathrm{CH})}=$ input capacitor charge current;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{DIS})}=$ input capacitor discharge current;
D = Duty Cycle.
The total Input RMS current is:

$$
\operatorname{ICIN}(\mathrm{RMS})=\sqrt{\begin{array}{l}
\left(\mathrm{I} \mathrm{CIN}(\mathrm{DIS})^{2} \times \mathrm{D}\right) \\
+\left(\mathrm{I} \mathrm{CIN}(\mathrm{CH})^{2} \times(1.0-\mathrm{D})\right)
\end{array}}
$$

The number of input capacitors required is then determined by:

$$
\mathrm{N}_{\mathrm{CIN}}=\frac{\mathrm{I} \mathrm{CIN}(\mathrm{RMS})}{\mathrm{I}_{\mathrm{RIPPLE}}}
$$

where:
$\mathrm{N}_{\mathrm{CIN}}=$ number of input capacitors;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{I}_{\text {RIPPLE }}=$ input capacitor ripple current rating (specified in manufacturer's data sheets).

The total input capacitor ESR needs to be determined in order to calculate the power dissipation of the input capacitors:

$$
\mathrm{ESR}_{\mathrm{CIN}}=\frac{\mathrm{ESR} \mathrm{CAP}}{\mathrm{~N}_{\mathrm{CIN}}}
$$

where:
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR;
$\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheets);
$\mathrm{N}_{\mathrm{CIN}}=$ number of input capacitors.
Once the total ESR of the input capacitors is known, the input capacitor ripple voltage can be determined using the formula:

$$
\mathrm{V}_{\mathrm{CIN}(\mathrm{RMS})}=\operatorname{ICIN(RMS)} \times \mathrm{ESR}_{\mathrm{CIN}}
$$

where:
$\mathrm{V}_{\mathrm{CIN}(\mathrm{RMS})}=$ input capacitor RMS voltage;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR.
The designer must determine the input capacitor power loss in order to ensure there isn't excessive power dissipation through these components. The following formula is used:

$$
\operatorname{PCIN}(\mathrm{RMS})=\operatorname{ICIN}(\mathrm{RMS})^{2} \times \mathrm{ESRCIN}
$$

where:
$\mathrm{P}_{\mathrm{CIN}(\mathrm{RMS})}=$ input capacitor RMS power dissipation;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR .

## Step 6: Selection of the Input Inductor

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$
\mathrm{L}_{\mathrm{IN}}=\frac{\Delta \mathrm{V}}{(\mathrm{dl} / \mathrm{dt}) \mathrm{MAX}}
$$

where:
$\mathrm{L}_{\mathrm{IN}}=$ input inductor value;
$\Delta \mathrm{V}=$ voltage seen by the input inductor during a full load swing;
$(\mathrm{dI} / \mathrm{dt})_{\mathrm{MAX}}=$ maximum allowable input current slew rate.
The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2.0 , a roll-off rate of $-40 \mathrm{~dB} / \mathrm{dec}$, and a corner frequency:

$$
\mathrm{f}_{\mathrm{C}}=\frac{1.0}{2.0 \pi \sqrt{\mathrm{LC}}}
$$

where:
$\mathrm{L}=$ input inductor;
$\mathrm{C}=$ input capacitor(s).

## Step 7: Selection of the Switching FET FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) Its very high input impedance; and 2) Its very fast switching times. The electrical characteristics of a MOSFET are considered to be those of a perfect switch.

Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of $\mathrm{V}_{\mathrm{GS}}$, and the faster the turn-on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn-on switching losses, 4) turn-off switching losses, and 5) gate-transitions losses. The latter three losses are proportional to frequency. For the conducting power dissipation rms values of current and resistance are used for true power calculations. The fast switching speed of the MOSFET makes it indispensable for high-frequency power supply applications. Not only are switching power losses minimized, but also the maximum usable switching frequency is considerably higher. Switching time is independent of temperature. Also, at higher frequencies, the use of smaller and lighter components (transformer, filter choke, filter capacitor) reduces overall component cost while using less space for more efficient packaging at lower weight.

The MOSFET has purely capacitive input impedance. No DC current is required. It is important to keep in mind the drain current of the FET has a negative temperature coefficient. Increase in temperature causes higher on-resistance and greater leakage current. $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}$ should be low to minimize power dissipation at a given $\mathrm{I}_{\mathrm{D}}$, and $\mathrm{V}_{\mathrm{GS}}$ should be high to accomplish this. MOSFET switching times are determined by device capacitance, stray capacitance, and the impedance of the gate drive circuit. Thus the gate driving circuit must have high momentary peak current sourcing and sinking capability for switching the MOSFET. The input capacitance, output capacitance and reverse-transfer capacitance also increase with increased device current rating.

Two considerations complicate the task of estimating switching times. First, since the magnitude of the input capacitance, $\mathrm{C}_{\mathrm{ISS}}$, varies with $\mathrm{V}_{\mathrm{DS}}$, the RC time constant determined by the gate-drive impedance and $\mathrm{C}_{\text {ISS }}$ changes during the switching cycle. Consequently, computation of the rise time of the gate voltage by using a specific gate-drive impedance and input capacitance yields only a rough estimate. The second consideration is the effect of the "Miller" capacitance, $\mathrm{C}_{\text {RSS }}$, which is referred to as $\mathrm{C}_{\text {DG }}$ in the following discussion. For example, when a device is on, $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}$ is fairly small and $\mathrm{V}_{\mathrm{GS}}$ is about $12 \mathrm{~V} . \mathrm{C}_{\mathrm{DG}}$ is charged to $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}-\mathrm{V}_{\mathrm{GS}}$, which is a negative potential if the drain is considered the positive electrode. When the drain is "off", $\mathrm{C}_{\mathrm{DG}}$ is charged to quite a different potential. In this case the voltage across $C_{D G}$ is a positive value since the potential from gate-to-source is near zero volts and $\mathrm{V}_{\mathrm{DS}}$ is essentially the drain supply voltage. During turn-on and turn-off, these large swings in gate-to-drain voltage tax the current sourcing and sinking capabilities of the gate drive. In addition to charging and discharging $\mathrm{C}_{\mathrm{GS}}$, the gate drive must also supply the displacement current required by
$\mathrm{C}_{\mathrm{DG}}\left(\mathrm{I}_{\text {GATE }}=\mathrm{C}_{\mathrm{DG}} \mathrm{dV}_{\mathrm{DG}} / \mathrm{dt}\right)$. Unless the gate-drive impedance is very low, the $\mathrm{V}_{\mathrm{GS}}$ waveform commonly plateaus during rapid changes in the drain-to-source voltage.
The most important aspect of FET performance is the Static Drain-To-Source On-Resistance ( $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ ), which effects regulator efficiency and FET thermal management requirements. The On-Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On-Resistance also increases. Its positive temperature coefficient is between $+0.6 \% / \mathrm{C}$ and $+0.85 \% / \mathrm{C}$. The higher the On-Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.
Both logic level and standard FETs can be used.
Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail-to-rail due to overshoot caused by the capacitive load they present to the controller IC.

## Step 7a: Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed $150^{\circ} \mathrm{C}$.

The maximum RMS current through the switch can be determined by the following formula:

$$
\begin{aligned}
& \operatorname{IRMS}(H)= \\
& \sqrt{\frac{\left(\begin{array}{l}
\operatorname{lL}(\mathrm{PEAK})^{2} \\
+(\mathrm{IL}(P E A K) \\
+\operatorname{IL}(V A L L E Y)^{2}
\end{array}\right.}{3.0}}
\end{aligned}
$$

where:
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{I}_{\mathrm{L}(\mathrm{PEAK})}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current;
D = Duty Cycle.
Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$
\operatorname{PRMS}(\mathrm{H})=\operatorname{IRMS}(\mathrm{H})^{2} \times \operatorname{RDS}(\mathrm{ON})
$$

where:
$\mathrm{P}_{\mathrm{RMS}(\mathrm{H})}=$ switching MOSFET conduction losses;
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=\mathrm{FET}$ drain-to-source on-resistance
The upper MOSFET switching losses are caused during MOSFET switch-on and switch-off and can be determined by using the following formula:

$$
\begin{aligned}
\mathrm{PSWH} & =\mathrm{PSWH}(\mathrm{ON})+\mathrm{PSWH}(\mathrm{OFF}) \\
& =\frac{\mathrm{V}_{\mathrm{IN}} \times \mathrm{IOUT} \times(\mathrm{tRISE}+\mathrm{tFALL})}{6.0 \mathrm{~T}}
\end{aligned}
$$

where:
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses;
$\mathrm{V}_{\mathrm{IN}}=$ input voltage;
IOUT $=$ load current;
$\mathrm{t}_{\text {RISE }}=$ MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{t}_{\text {FALL }}=$ MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{T}=1 / \mathrm{F}_{\mathrm{SW}}=$ period.
The total power dissipation in the switching MOSFET can then be calculated as:
PHFET(TOTAL) $=$ PRMSH $+\operatorname{PSWH}(O N)+$ PSWH $(O F F)$
where:
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) MOSFET losses;
$\mathrm{P}_{\text {RMSH }}=$ upper MOSFET switch conduction Losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses.
Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$
T_{J}=T_{A}+\left(\text { PhFET }(T O T A L) \times R_{\theta J A}\right)
$$

where:
$\mathrm{T}_{\mathrm{J}}=\mathrm{FET}$ junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) FET losses;
$\mathrm{R}_{\theta \mathrm{JA}}=$ upper FET junction-to-ambient thermal resistance.

## Step 7b: Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$
\begin{aligned}
\mathrm{PRMSL} & =\mathrm{IRMS}^{2} \times \mathrm{RDS}(\mathrm{ON}) \\
& =(\mathrm{IOUT} \times \sqrt{(1.0-\mathrm{D})})^{2} \times \mathrm{RDS}(\mathrm{ON})
\end{aligned}
$$

where:
$\mathrm{P}_{\mathrm{RMSL}}=$ lower MOSFET conduction losses;
$\mathrm{I}_{\text {OUT }}=$ load current;
D = Duty Cycle;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=$ lower FET drain-to-source on-resistance.
The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non-overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$
\text { PSWL }=V_{S D} \times \operatorname{lLOAD} \times \text { non-overlap time } \times \text { FSW }
$$

where:
$\mathrm{P}_{\text {SWL }}=$ lower FET switching losses;
$\mathrm{V}_{\mathrm{SD}}=$ lower FET source-to-drain voltage;
$\mathrm{I}_{\text {LOAD }}=$ load current
Non-overlap time $=$ GATE(L)-to-GATE(H) or GATE(H)-to-GATE(L) delay (from CS51312 data sheet Electrical Characteristics section);
$\mathrm{F}_{\text {SW }}=$ switching frequency .
The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:
PLFET(TOTAL) = PRMSL + PSWL
where:
$P_{\text {LFET }}($ TOTAL $) ~=~ S y n c h r o n o u s ~(l o w e r) ~ F E T ~ t o t a l ~ l o s s e s ; ~ ; ~$
$\mathrm{P}_{\text {RMSL }}=$ Switch Conduction Losses;
$P_{\text {SWL }}=$ Switching losses.
Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$
T_{J}=T_{A}+\left(P_{L F E T}(T O T A L) \times R_{\theta J A}\right)
$$

where:
$\mathrm{T}_{\mathrm{J}}=$ MOSFET junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\mathrm{P}_{\text {LFET }}($ TOTAL $) ~=~ t o t a l ~ s y n c h r o n o u s ~(l o w e r) ~ F E T ~ l o s s e s ; ~ ; ~$
$\mathrm{R}_{\theta \mathrm{JA}}=$ lower FET junction-to-ambient thermal resistance.

## Step 8: Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, $\mathrm{V}_{\mathrm{CC}}$, and the CS51312 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:

$$
\text { PCONTROLIC }=\operatorname{ICC1} \mathrm{V}_{\mathrm{CC} 1}+\operatorname{PGATE}(\mathrm{H})+\mathrm{PGATE}(\mathrm{~L})
$$

where:
$\mathrm{P}_{\text {CONTROLIC }}=$ control IC power dissipation;
$\mathrm{I}_{\mathrm{CC} 1}=\mathrm{IC}$ quiescent supply current;
$\mathrm{V}_{\mathrm{CC} 1}=\mathrm{IC}$ supply voltage;
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{P}_{\mathrm{GATE}(\mathrm{L})}=$ lower MOSFET gate driver (IC) losses.

The upper (switching) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{H})=\mathrm{Q}_{\mathrm{GATE}}(\mathrm{H}) \times \mathrm{F}_{S W} \times \mathrm{V}_{\mathrm{GATE}}(\mathrm{H})
$$

where:
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{H})}=$ total upper MOSFET gate charge;
$\mathrm{F}_{\text {SW }}=$ switching frequency;
$\mathrm{V}_{\text {GATE }}(\mathrm{H})=$ upper MOSFET gate voltage.
The lower (synchronous) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{L})=\text { QGATE }^{\text {G }} \text { L) } \times \text { FSW } \times \mathrm{V}_{\text {GATE }}(\mathrm{L})
$$

where:
$\mathrm{P}_{\text {GATE(L) }}=$ lower MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{L})}=$ total lower MOSFET gate charge;
$\mathrm{F}_{\mathrm{SW}}=$ switching frequency;
$\mathrm{V}_{\text {GATE(L) }}=$ lower MOSFET gate voltage.
The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

## Step 9: Slope Compensation

Voltage regulators for today's advanced processors are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR at the CPU input supply pins. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that there's very little voltage ramp at the control IC feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ) and regulator sensitivity to noise and loop instability are two undesirable effects that can surface. The performance of the CS51312-based CPU $\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}$ regulator is improved when a fixed amount of slope compensation is added to the output of the PWM Error Amplifier (COMP pin) during the regulator Off-Time. Referring to Figure 14, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1and R2.

$$
\mathrm{V}_{\text {SLOPECOMP }}=\mathrm{V}_{\operatorname{GATE}}(\mathrm{L}) \times\left(\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}\right) \times\left(1.0-\mathrm{e}^{\frac{-t}{\tau}}\right)
$$

where:
$\mathrm{V}_{\text {SLOPECOMP }}=$ amount of slope added;
$\mathrm{V}_{\text {GATE(L) }}=$ lower MOSFET gate voltage;
$\mathrm{R} 1, \mathrm{R} 2=$ voltage divider resistors;
$\mathrm{t}=\mathrm{t}_{\text {OFF }}$ (switch off-time);
$\tau=\mathrm{RC}$ constant determined by C 1 and the parallel combination of R1, R2 (Figure 14), neglecting the low driver output impedance.


Figure 14. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off-time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin.

## Step 10: Selection of Current Limit Filter Components

In some applications, the current limit comparator may falsely trigger due to noise, load transients, or high inductor ripple currents. A filter circuit such as the one shown in Figure 15 can be added to prevent this. The RC time constant of this filter is equal to $\left(\mathrm{R}_{\mathrm{FB}}+\mathrm{R}_{\mathrm{OUT}}\right) \times \mathrm{C}_{\text {SENSE }}$. Increasing the RC time constant will reduce the sensitivity of the circuit, but increase the time required to detect an overcurrent condition. The value of $\mathrm{R}_{\mathrm{FB}}+\mathrm{R}_{\mathrm{OUT}}$ should be kept to $510 \Omega$ or lower to avoid significant DC offsets due to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ bias currents.


Figure 15. Current Limit Filter Circuit

## "DROOP" RESISTOR FOR ADAPTIVE VOLTAGE POSITIONING AND CURRENT LIMIT

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met.

In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage at full load is above the minimum DC tolerance spec:

$$
V_{D R O O P}(T Y P)=\frac{V_{D A C}(M I N)-V_{D C}(M I N)}{1.0+R_{D R O O P}(T O L E R A N C E)}
$$

## Current Limit

The current limit setpoint has to be higher than the normal full load current. Attention has to be paid to the current rating of the external power components as these are the first to fail during an overload condition. The MOSFET continuous and pulsed drain current rating at a given case temperature has to be accounted for when setting the current limit trip point.

## Nominal Current Limit Setpoint

From the overcurrent detection data in the electrical characteristics table:

$$
\begin{gathered}
\mathrm{V}_{\mathrm{TH}}(\mathrm{TYP})=86 \mathrm{mV} \\
\mathrm{I}_{\mathrm{CL}(\mathrm{NOM})}=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{TYP})}}{\operatorname{RSENSE}(\mathrm{NOM})}
\end{gathered}
$$

## Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$
R_{A R}=\rho \times \frac{L}{A} \text { or } R=\rho \times \frac{L}{(W \times t)}
$$

where:
$\mathrm{A}=\mathrm{W} \times \mathrm{t}=$ cross-sectional area;
$\rho=$ the copper resistivity ( $\mu \Omega-$ mil $)$;
$\mathrm{L}=$ length (mils);
$\mathrm{W}=$ width (mils);
$\mathrm{t}=$ thickness (mils).
An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation caused by variation in the thickness of the PCB layer; 2) the mismatch of $\mathrm{L} / \mathrm{W}$; and 3) temperature variation.

## 1) Sheet Resistivity

For one ounce copper, the thickness variation is typically 1.26 mil to 1.48 mil . Therefore the error due to sheet resistivity is:

$$
\frac{1.48-1.26}{1.37}= \pm 8.0 \%
$$

## 2) Mismatch Due to L/W

The variation in $\mathrm{L} / \mathrm{W}$ is governed by variations due to the PCB manufacturing process. The error due to L/W mismatch is typically $1.0 \%$.

## 3) Thermal Considerations

Due to $I^{2} \times R$ power losses the surface temperature of the droop resistor will increase causing the resistance to increase. Also, the ambient temperature variation will contribute to the increase of the resistance, according to the formula:

$$
R=R_{20}\left[1.0+\alpha_{20}(T-20)\right]
$$

where:
$\mathrm{R}_{20}=$ resistance at $20^{\circ} \mathrm{C}$;
$\alpha=0.00393 /{ }^{\circ} \mathrm{C}$
$\mathrm{T}=$ operating temperature;
$\mathrm{R}=$ desired droop resistor value.
For temperature $\mathrm{T}=50^{\circ} \mathrm{C}$, the $\% \mathrm{R}$ change $=12 \%$.

## Droop Resistor Tolerance

Tolerance due to sheet resistivity variation $\pm 8.0 \%$
Tolerance due to L/W error $1.0 \%$
Tolerance due to temperature variation $12 \%$
Total tolerance for droop resistor $21 \%$

## Droop Resistor Length, Width, and Thickness

The minimum width and thickness of the droop resistor should primarily be determined on the basis of the current-carrying capacity required, and the maximum permissible droop resistor temperature rise. PCB manufacturer design charts can be used in determining current-carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$
\text { Thermal Impedance }=\frac{T_{\mathrm{J}(\mathrm{MAX})}-\mathrm{T}_{\mathrm{A}}}{\text { Power }}
$$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for
compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

## LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS51312.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double-sided PCBs a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCBs are usually sufficient for a good layout, four-layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layer for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be as short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}$ filter resistors $(510 \Omega)$ in series with the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ pins as close as possible to the pins.
12. Place the C Coff and COMP capacitors as close as possible to the $\mathrm{C}_{\mathrm{OFF}}$ and COMP pins.
13. Place the current limit filter capacitor between the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{OUT}}$ pins, as close as possible to the pins.
14. Connect the filter components of the following pins: $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}, \mathrm{C}_{\mathrm{OFF}}$, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
15. The "Droop" Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
16. Place the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor as close as possible to the IC.


Figure 16. Additional Application Circuit, 5.0 V/12 V to 2.0 V/19 A Converter

PACKAGE THERMAL DATA

| Parameter |  | SO-16 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5157H

## CPU 5-Bit Synchronous Buck Controller

The CS5157H is a 5 -bit synchronous dual N -Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5157H is designed to operate over a $4.25-20 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V or 12 V as the main supply for conversion.

The CS5157H is specifically designed to power Pentium ${ }^{\circledR}$ II processors and other high performance core logic. It includes the following features: on board, 5-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5157H is available in 16 pin surface mount.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5-Bit DAC
- 30 ns Gate Rise/Fall Times
- $1.0 \%$ DAC Accuracy
- 5.0 V \& 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- 25 ns FET Nonoverlap Time
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Current Sharing
- Overvoltage Protection


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5157HGD16 | SO-16 | 48 Units/Rail |
| CS5157HGDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, Switching Power Supply for Core Logic - Pentium ${ }^{\circledR}$ II Processor

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :--- | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ | Reflow: (SMD styles only) (Note 1$)$ | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $25 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $20 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $V_{F B}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\text {OFF }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $V_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {ID } 0}-\mathrm{V}_{\text {ID } 4}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {GATE(H) }}$ | $20 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\text {GATE(L) }}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

ELECTRICAL CHARACTERISTICS
$\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V}\right.$;DAC
Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDD}}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | 

$\mathrm{V}_{\mathrm{CC} 1}$ Monitor

| Start Threshold | Output switching | 3.75 | 3.90 | 4.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 3.70 | 3.85 | 4.00 | V |
| Hysteresis | Start-Stop | - | 50 | - | mV |

$\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$

| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1}-\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} ; \mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | - | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Out SINK Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}-\mathrm{V}_{\text {PGND }} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}-\mathrm{V}_{\text {PGND }}$ | - | 1.0 | 1.5 | V |
| Out Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}<9.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{C} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}>1.0 \mathrm{~V} ; \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to 2.0 V ; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ rising to 2.0 V | - | 25 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to 2.0 V ; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\text {GATE(H) }}$ rising to 2.0 V | - | 25 | 50 | ns |
| $\mathrm{V}_{\text {GATE(H) }}, \mathrm{V}_{\text {GATE(L) }}$ Resistance | Resistor to LGND. Note 2 | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE(H) }}, \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})} @ 10 \mathrm{~mA}$ LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} @ 10 \mathrm{~mA}$ | - | 600 | 800 | mV |

## Soft Start (SS)

| Charge Time |  | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | $($ Charge Time $/$ Pulse Period $) \times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V} ;\right.$ DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |  |  |  |  | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC |  |  |  |  |  |  |  |  |  |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID0, }} \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID } 4}$ | 1.00 | 1.25 | 2.40 | V |
| Input Pull Up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID } 0, ~} \mathrm{~V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID } 2}, \mathrm{~V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID } 4}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Pull Up Voltage |  |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy (all codes except 11111) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}}, 25^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 125^{\circ} \mathrm{C}$ | - | - | 1.0 | \% |
| VID4 | VID3 | VID2 | VID1 | VID0 |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | - | 1.2870 | 1.3000 | 1.3130 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.3365 | 1.3500 | 1.3635 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.3860 | 1.4000 | 1.4140 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.4355 | 1.4500 | 1.4645 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.4850 | 1.5000 | 1.5150 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.5345 | 1.5500 | 1.5655 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.5840 | 1.6000 | 1.6160 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.6335 | 1.6500 | 1.6665 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.6830 | 1.7000 | 1.7170 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.7325 | 1.7500 | 1.7675 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.7820 | 1.8000 | 1.8180 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.8315 | 1.8500 | 1.8685 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.8810 | 1.9000 | 1.9190 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.9305 | 1.9500 | 1.9695 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.9800 | 2.0000 | 2.0200 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.0295 | 2.0500 | 2.0705 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.0790 | 2.1000 | 2.1210 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.1780 | 2.2000 | 2.2220 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.2770 | 2.3000 | 2.3230 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.3760 | 2.4000 | 2.4240 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.4750 | 2.5000 | 2.5250 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.5740 | 2.6000 | 2.6260 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.6730 | 2.7000 | 2.7270 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.7720 | 2.8000 | 2.8280 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.8710 | 2.9000 | 2.9290 | V |
| 1 | 0 | 1 | 0 | 1 | - | 2.9700 | 3.0000 | 3.0300 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.0690 | 3.1000 | 3.1310 | V |
| 1 | 0 | 0 | 1 | 1 | - | 3.1680 | 3.2000 | 3.2320 | V |
| 1 | 0 | 0 | 1 | 0 | - | 3.2670 | 3.3000 | 3.3330 | V |
| 1 | 0 | 0 | 0 | 1 | - | 3.3660 | 3.4000 | 3.4340 | V |
| 1 | 0 | 0 | 0 | 0 | - | 3.4650 | 3.5000 | 3.5350 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+125^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<20 \mathrm{~V} ; \mathrm{DAC}\right.$ Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current |  |  |  |  |  |
| $I_{\text {CC1 }}$ | No Switching | - | 8.5 | 13.5 | mA |
| ICC2 | No Switching | - | 1.6 | 3.0 | mA |
| Operating $\mathrm{I}_{\text {CC1 }}$ | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 8.0 | 13 | mA |
| Operating ICC2 | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.0 | 5.0 | mA |
| $\mathrm{C}_{\text {OFF }}$ |  |  |  |  |  |
| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {SS }}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{s}$ |
| Extension Charge Time | $\mathrm{V}_{\text {SS }}=\mathrm{V}_{\text {FFB }}=0$ | 5.0 | 8.0 | 11.0 | $\mu \mathrm{s}$ |
| Discharge Current | $\mathrm{C}_{\text {OFF }}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\text {FB }}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |
| Time Out Timer |  |  |  |  |  |
| Time Out Time | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ; \\ & \text { Record } \mathrm{V}_{\mathrm{GATE}(\mathrm{H})} \text { Pulse High Duration } \end{aligned}$ | 10 | 30 | 65 | $\mu \mathrm{s}$ |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 70 | \% |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-16 | PIN SYMBOL | FUNCTION |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is High (logic one), the DAC range is 2.10 V to 3.50 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is Low (logic zero), the DAC range is 1.30 V to 2.05 V with 50 mV increments. $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID4 }}$ select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.2440 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE(H) }}$ | High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ from being in high state simultaneously. |
| 11 | PGND | High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 1.5 A peak switching current. |
| 13 | $\mathrm{V}_{\text {CC1 }}$ | Input power for the IC and low side gate driver. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{F B}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. V ${ }^{2}$ Control Diagram

The $V^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5157H uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $25 \mu$ s timer, minimizing stress to the power components.

## Programmable Output

The CS5157H is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.10 V to 3.50 V in 100 mV steps, the second is 1.30 V to 2.05 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5157H enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE $(\mathrm{H})$ pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the COFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.
The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by
the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ and $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (1.0 V/div.)
Figure 4. CS5157H Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5157H Demonstration Board Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1-Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 6. CS5157H Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C CopF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} /$ div.) Trace 2- Inductor Switching Node (5.0 V/div.)

Figure 7. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=0.5 \mathrm{~A}$ (Light Load)


Trace 1- Regulator Output Voltage ( $10 \mathrm{mV} /$ div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Figure 8. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$,

$$
\mathrm{I}_{\text {OUT }}=13 \text { A (Heavy Load) }
$$

## Transient Response

The CS5157H V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Trace 1- Regulator Output Voltage ( $100 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Regulator Output Voltage ( $10 \mathrm{~A} / \mathrm{div}$.)
Figure 9. CS5157H Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V )


Trace 1- Regulator Output Voltage ( $100 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$. )
Trace 3- Output Current ( 0.5 to 13 Amps ) ( $10 \mathrm{~A} / \mathrm{div}$.)
Figure 10. CS5157H Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V). Upon Completing a Normal Off Time, The $\mathrm{V}^{2}$ Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100\% Duty Cycle. Regulation is Achieved in Less Than $20 \mu \mathrm{~s}$


Figure 11. CS5157H Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V). V² Control Topology Immediately Connects Inductor to Ground, Providing 0\% Duty Cycle. Regulation is Achieved in Less Than $10 \mu \mathrm{~s}$

## PROTECTION AND MONITORING FEATURES

## $V_{\text {CC1 }}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\text {FFB }}$ low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.)
Trace 3- Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5157H Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 13. Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15 ). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.


Figure 14. OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Trace 4-5.0 V from PC Power Supply (2.0 V/div.)
Trace 1 - Regulator Output Voltage (1.0 V/div.)
Figure 15. OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\mathrm{FFB}}$ pin low, emulating a short circuit condition.


Figure 16. Implementing Shutdown with the CS5157H

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power }}$ Good.


Figure 17. Implementing Power Good with the CS5157H


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $10 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 18. CS5157H Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Selecting External Components

The CS5157H can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the
capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\operatorname{VGATE}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{~L})=12 \mathrm{~V}
$$

(see Figure 19.)


Figure 19. CS5157H Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is $\mathrm{RDS}_{\mathrm{ON}}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\text { LLOAD }^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\text { LLOAD }{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =
VOUT + (ILOAD $\times$ RDSON OF SYNCH FET) $\left[\begin{array}{l}\text { VIN }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET }) \\ -(\text { LLOAD } \times \text { RDSON OF SWITCH FET })\end{array}\right]$

## Off Time Capacitor (Coff)

The Coff timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

When the $\mathrm{V}_{\mathrm{FFB}}$ pin is less than 1.0 V , the current charging the $\mathrm{C}_{\text {OFF }}$ capacitor is reduced. The extended off time can be calculated as follows:

$$
\text { TOFF }=\text { COFF } \times 24,242.5
$$

Off time will be determined by either the $\mathrm{T}_{\text {OFF }}$ time, or the time out timer, whichever is longer.

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\text {OFF }}$ timing capacitor:

$$
\text { CoFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. The CS5157H reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous MOSFET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=\mathrm{V}_{\mathrm{BD}} \times$ ILOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5157H demonstration board as shown in Figure 8;

$$
\text { Power }=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}
$$

This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal
impedance (junction to ambient) required to meet this requirement can be calculated as follows:

Thermal Impedance $=\frac{\text { TJUNCTION(MAX) }- \text { TAMBIENT }}{\text { Power }}$
A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 20. Filter Components


Figure 21. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. Connect the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
7. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.
Route gate drive signals $\mathrm{V}_{\text {GATE(H) }}$ (pin 10) and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.


Figure 22. Layout Guidelines


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter


Figure 24. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias


Figure 25. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing


Figure 26. Additional Application Diagram, 12 V to 3.3 V/5.0 A Converter with Remote Sense

## CS5157H

PACKAGE THERMAL DATA

| Parameter |  | 16-SO | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5158

## CPU 5-Bit Synchronous Buck Controller

The CS5158 is a 5-bit synchronous dual N-Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5158 is designed to operate over a $4.25-16 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V as the main supply for conversion.

The CS5158 is specifically designed to power Pentium ${ }^{\circledR}$ II processors and other high performance core logic. It includes the following features: on board, 5-bit DAC, short circuit protection, $0.8 \%$ output tolerance for the 01111 DAC code ( 1.3 V ) and $1.0 \%$ for the remaining DAC codes, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5158 is available in 16 pin surface mount.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5-Bit DAC
- 30 ns Gate Rise/Fall Times
- $0.8 \%$ Accuracy for the 01111 DAC Code and $1.0 \%$ for the Remaining DAC Codes
- $5.0 \mathrm{~V} \& 12 \mathrm{~V}$ Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- 25 ns FET Nonoverlap Time
- $V^{2 \mathrm{Tm}}$ Control Topology
- Current Sharing
- Overvoltage Protection


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


A = Assembly Location
WL, L = Wafer Lot
YY, $Y=$ Year
WW, W = Work Week

## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5158GD16 | SO-16 | 48 Units/Rail |
| CS5158GDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, Switching Power Supply for Core Logic - Pentium ${ }^{\circledR}$ II Processor

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $V_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $25 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $20 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {FB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\mathrm{OFF}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {IDO }}-\mathrm{V}_{\text {ID4 }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\text {GATE(H) }}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\text {GATE(L) }}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

## CS5158

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<14 \mathrm{~V}\right.$;DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDD}}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | 

$\mathrm{V}_{\mathrm{CC} 1}$ Monitor

| Start Threshold | Output switching | 3.75 | 3.90 | 4.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 3.70 | 3.85 | 4.00 | V |
| Hysteresis | Start-Stop | - | 50 | - | mV |

$\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$

| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1}-\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} ; \mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | - | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Out SINK Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}-\mathrm{V}_{\text {PGND }} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}-\mathrm{V}_{\text {PGND }}$ | - | 1.0 | 1.5 | V |
| Out Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}<9.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}>1.0 \mathrm{~V} ; \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to 2.0 V ; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\text {GATE(L) }}$ rising to 2.0 V | - | 25 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to 2.0 V ; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ rising to 2.0 V | - | 25 | 50 | ns |
| $\mathrm{V}_{\text {GATE(H) }}, \mathrm{V}_{\text {GATE(L) }}$ Resistance | Resistor to LGND | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE(H) }}, \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ @ 10 mA LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ @ 10 mA | - | 600 | 800 | mV |

## Soft Start (SS)

| Charge Time |  | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | $($ Charge Time $/$ Pulse Period $) \times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<14 \mathrm{~V}\right.$;DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |  |  |  |  | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC |  |  |  |  |  |  |  |  |  |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID } 2}, \mathrm{~V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID }}$ | 1.00 | 1.25 | 2.40 | V |
| Input Pull Up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID }}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Pull Up Voltage |  |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy <br> (all codes except 01111 at $0.8 \%$ ) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP},} 25^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 85^{\circ} \mathrm{C}$ | - | - | 1.0 | \% |
| $\mathrm{V}_{\text {ID } 4}$ | VID3 | VID2 | $\mathrm{V}_{\text {ID } 1}$ | $\mathrm{V}_{\text {ID }}$ |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | - | 1.2896 | 1.3000 | 1.3104 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.3365 | 1.3500 | 1.3635 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.3860 | 1.4000 | 1.4140 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.4355 | 1.4500 | 1.4645 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.4850 | 1.5000 | 1.5150 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.5345 | 1.5500 | 1.5655 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.5840 | 1.6000 | 1.6160 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.6335 | 1.6500 | 1.6665 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.6830 | 1.7000 | 1.7170 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.7325 | 1.7500 | 1.7675 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.7820 | 1.8000 | 1.8180 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.8315 | 1.8500 | 1.8685 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.8810 | 1.9000 | 1.9190 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.9305 | 1.9500 | 1.9695 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.9800 | 2.0000 | 2.0200 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.0295 | 2.0500 | 2.0705 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.2315 | 1.2440 | 1.2564 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.0790 | 2.1000 | 2.1210 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.1780 | 2.2000 | 2.2220 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.2770 | 2.3000 | 2.3230 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.3760 | 2.4000 | 2.4240 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.4750 | 2.5000 | 2.5250 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.5740 | 2.6000 | 2.6260 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.6730 | 2.7000 | 2.7270 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.7720 | 2.8000 | 2.8280 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.8710 | 2.9000 | 2.9290 | V |
| 1 | 0 | 1 | 0 | 1 | - | 2.9700 | 3.0000 | 3.0300 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.0690 | 3.1000 | 3.1310 | V |
| 1 | 0 | 0 | 1 | 1 | - | 3.1680 | 3.2000 | 3.2320 | V |
| 1 | 0 | 0 | 1 | 0 | - | 3.2670 | 3.3000 | 3.3330 | V |
| 1 | 0 | 0 | 0 | 1 | - | 3.3660 | 3.4000 | 3.4340 | V |
| 1 | 0 | 0 | 0 | 0 | - | 3.4650 | 3.5000 | 3.5350 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<14 \mathrm{~V} ; \mathrm{DAC}\right.$ Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDD}}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current |  |  |  |  |  |
| $I_{\text {CC1 }}$ | No Switching | - | 8.5 | 13.5 | mA |
| ICC2 | No Switching | - | 1.6 | 3.0 | mA |
| Operating $\mathrm{I}_{\text {CC1 }}$ | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 8.0 | 13 | mA |
| Operating ICC2 | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.0 | 5.0 | mA |
| $\mathrm{C}_{\text {OFF }}$ |  |  |  |  |  |
| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {SS }}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{s}$ |
| Extension Charge Time | $\mathrm{V}_{\text {SS }}=\mathrm{V}_{\text {FFB }}=0$ | 5.0 | 8.0 | 11.0 | $\mu \mathrm{s}$ |
| Discharge Current | $\mathrm{C}_{\text {OFF }}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\text {FB }}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |
| Time Out Timer |  |  |  |  |  |
| Time Out Time | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ; \\ & \text { Record } \mathrm{V}_{\mathrm{GATE}(\mathrm{H})} \text { Pulse High Duration } \end{aligned}$ | 10 | 30 | 50 | $\mu \mathrm{s}$ |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 65 | \% |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| SO-16 |  |  |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is High (logic one), the DAC range is 2.10 V to 3.50 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is Low (logic zero), the DAC range is 1.30 V to 2.05 V with 50 mV increments. $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID4 }}$ select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.2440 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE(H) }}$ | High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ from being in high state simultaneously. |
| 11 | PGND | High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 1.5 A peak switching current. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC and low side gate driver. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{\text {FB }}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## V $^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. V ${ }^{\mathbf{2}}$ Control Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5158 uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu \mathrm{~s}$ timer, minimizing stress to the power components.

## Programmable Output

The CS5158 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.10 V to 3.50 V in 100 mV steps, the second is 1.30 V to 2.05 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5158 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.
If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE $(\mathrm{H})$ pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the COFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by
the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $2.0 \mathrm{~V} /$ div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ and $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $5.0 \mathrm{~V} /$ div. )
Trace 4-5.0 V Input ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Figure 4. CS5158 Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5158 Demonstration Board Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1-Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 6. CS5158 Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} /$ div.) Trace 2- Inductor Switching Node (5.0 V/div.)

Figure 7. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=0.5 \mathrm{~A}$ (Light Load)


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 8. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$,

$$
\text { lout = } 13 \text { A (Heavy Load) }
$$

## Transient Response

The CS5158 V ${ }^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


[^35]Figure 9. CS5158 Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V)


Trace 1-Regulator Output Voltage ( $100 \mathrm{mV} /$ div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$. )
Trace 3- Output Current ( 0.5 to 13 Amps ) ( $10 \mathrm{~A} / \mathrm{div}$.)
Figure 10. CS5158 Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V ). Upon Completing a Normal Off Time, The V ${ }^{2}$ Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100\% Duty Cycle. Regulation is Achieved in Less Than $20 \mu \mathrm{~s}$


Trace 1-Regulator Output Voltage ( $100 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- Output Current ( 13 to 0,5 Amps) ( $10 \mathrm{~A} / \mathrm{div}$.)
Figure 11. CS5158 Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V). V ${ }^{2}$ Control Topology Immediately Connects Inductor to Ground, Providing 0\% Duty Cycle. Regulation is Achieved in Less Than $10 \mu \mathrm{~s}$

## PROTECTION AND MONITORING FEATURES

## $V_{\text {CC1 }}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\text {FFB }}$ low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.) Trace 3- Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5158 Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15 ). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.


Trace 4-5.0 V from PC Power Supply (5.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node 5.0 V/div.)
Figure 14. OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Figure 15. OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\mathrm{FFB}}$ pin low, emulating a short circuit condition.


Figure 16. Implementing Shutdown with the CS5158

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power }}$ Good .


Figure 17. Implementing Power Good with the CS5158


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $10 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} /$ div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 18. CS5158 Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Selecting External Components

The CS5158 can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.
Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the
typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\operatorname{VGATE}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{~L})=12 \mathrm{~V}
$$

(see Figure 19.)


Figure 19. CS5158 Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is $\mathrm{RDS}_{\mathrm{ON}}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\text { ILOAD }^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\operatorname{ILOAD}{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =

$$
\frac{\mathrm{V}_{\text {OUT }}+(\mathrm{lLOAD} \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\mathrm{V}_{\text {IN }}+(\mathrm{ILOAD} \times \mathrm{RDS} \text { ON OF SYNCH FET }) \\
-(\mathrm{ILOAD} \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (COFF)

The Coff timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

When the $\mathrm{V}_{\mathrm{FFB}}$ pin is less than 1.0 V , the current charging the $\mathrm{C}_{\mathrm{OFF}}$ capacitor is reduced. The extended off time can be calculated as follows:

$$
\text { TOFF }=\text { COFF } \times 24,242.5
$$

Off time will be determined by either the $\mathrm{T}_{\mathrm{OFF}}$ time, or the time out timer, whichever is longer.

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\mathrm{OFF}}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. The CS5158 reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous MOSFET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=\mathrm{V}_{\mathrm{BD}} \times$ ILOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5158 demonstration board as shown in Figure 8;

$$
\text { Power }=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}
$$

This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:
Thermal Impedance $=\frac{\text { TJUNCTION }(M A X)-\text { TAMBIENT }}{\text { Power }}$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 20. Filter Components


Figure 21. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. Connect the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
7. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.
Route gate drive signals $\mathrm{V}_{\text {GATE(H) }}$ (pin 10) and $\mathrm{V}_{\text {GATE(L) }}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.


Figure 22. Layout Guidelines


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter


Figure 24. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias


Figure 25. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing PACKAGE THERMAL DATA

| Parameter |  | 16-SO | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {OJA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5159

## CPU 5-Bit Synchronous Buck Controller

The CS5159 is a 5 -bit synchronous dual N-Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5159 is designed to operate over a $4.25-16 \mathrm{~V}$ range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V or 12 V as the main supply for conversion.

The CS5159 is specifically designed to power Pentium ${ }^{\circledR}$ II processors and other high performance core logic. It includes the following features: on board, 5-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5159 is available in 16 pin surface mount.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5-Bit DAC
- Backward Compatible with Adjustable CS5157
- 30 ns Gate Rise/Fall Times
- $1.0 \%$ DAC Accuracy
- $5.0 \mathrm{~V} \& 12 \mathrm{~V}$ Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- 25 ns FET Nonoverlap Time
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Current Sharing
- Overvoltage Protection


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5159GD16 | SO-16 | 48 Units/Rail |
| CS5159GDR16 | SO-16 | 2500 Tape \& Reel |



Figure 1. Application Diagram, Switching Power Supply for Core Logic - Pentium ${ }^{\circledR}$ II Processor

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $25 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $20 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |
| $V_{\text {FB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | -0.2 $\mu \mathrm{A}$ |
| COFF | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {FFB }}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | -0.2 $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {ID } 0}-\mathrm{V}_{\text {ID } 4}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{V}_{\text {GATE(H) }}$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| $\mathrm{V}_{\text {GATE(L) }}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |
| LGND | 0 V | 25 mA |
| PGND | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

## CS5159

ELECTRICAL CHARACTERISTICS
$\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<18 \mathrm{~V} ; \mathrm{DAC}\right.$
Code: $\mathrm{V}_{I D 4}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | 

$\mathrm{V}_{\mathrm{CC} 1}$ Monitor

| Start Threshold | Output switching | 3.75 | 3.90 | 4.05 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 3.70 | 3.85 | 4.00 | V |
| Hysteresis | Start-Stop | - | 50 | - | mV |

$\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$

| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1}-\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} ; \mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | - | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Out SINK Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}-\mathrm{V}_{\text {PGND }} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}-\mathrm{V}_{\text {PGND }}$ | - | 1.0 | 1.5 | V |
| Out Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}<9.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})}>1.0 \mathrm{~V} \text {; } \\ & \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to 2.0 V ; $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\text {GATE(L) }}$ rising to 2.0 V | - | 25 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to $2.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$; <br> $\mathrm{V}_{\text {GATE(H) }}$ rising to 2.0 V | - | 25 | 50 | ns |
| $\mathrm{V}_{\text {GATE(H) }}, \mathrm{V}_{\text {GATE(L) }}$ Resistance | Resistor to LGND, Note 2 | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE(H) }}, \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})} @ 10 \mathrm{~mA}$ LGND to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ @ 10 mA | - | 600 | 800 | mV |

## Soft Start (SS)

| Charge Time |  | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | (Charge Time /Pulse Period) $\times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\text {FFB }}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

PWM Comparator

| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}(H)}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{FFB}}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<18 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID2}}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDD}}=1 ; \mathrm{V}_{\mathrm{ID3}}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |  |  |  |  | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC |  |  |  |  |  |  |  |  |  |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID } 4}$ | 1.00 | 1.25 | 2.40 | V |
| Input Pull Up Resistance |  |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID }}, \mathrm{V}_{\text {ID } 4}$ | 25 | 50 | 100 | k $\Omega$ |
| Pull Up Voltage |  |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy (all codes except 11111, 10110, 10101, 10100, 10011, 10010, 10001, 10000) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\text {COMP }}, 25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 85^{\circ} \mathrm{C}$ | - | - | 1.0 | \% |
| $\mathrm{V}_{\text {ID4 }}$ | VID3 | $\mathrm{V}_{\text {ID } 2}$ | VID1 | VIDO |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | - | 1.2870 | 1.3000 | 1.3130 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.3365 | 1.3500 | 1.3635 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.3860 | 1.4000 | 1.4140 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.4355 | 1.4500 | 1.4645 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.4850 | 1.5000 | 1.5150 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.5345 | 1.5500 | 1.5655 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.5840 | 1.6000 | 1.6160 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.6335 | 1.6500 | 1.6665 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.6830 | 1.7000 | 1.7170 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.7325 | 1.7500 | 1.7675 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.7820 | 1.8000 | 1.8180 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.8315 | 1.8500 | 1.8685 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.8810 | 1.9000 | 1.9190 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.9305 | 1.9500 | 1.9695 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.9800 | 2.0000 | 2.0200 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.0295 | 2.0500 | 2.0705 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.0790 | 2.1000 | 2.1210 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.1780 | 2.2000 | 2.2220 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.2770 | 2.3000 | 2.3230 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.3760 | 2.4000 | 2.4240 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.4750 | 2.5000 | 2.5250 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.5740 | 2.6000 | 2.6260 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.6730 | 2.7000 | 2.7270 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.7720 | 2.8000 | 2.8280 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.8420 | 2.9000 | 2.9580 | V |
| 1 | 0 | 1 | 0 | 1 | - | 2.9400 | 3.0000 | 3.0600 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.0380 | 3.1000 | 3.1620 | V |
| 1 | 0 | 0 | 1 | 1 | - | 3.1360 | 3.2000 | 3.2640 | V |
| 1 | 0 | 0 | 1 | 0 | - | 3.2340 | 3.3000 | 3.3660 | V |
| 1 | 0 | 0 | 0 | 1 | - | 3.3320 | 3.4000 | 3.4680 | V |
| 1 | 0 | 0 | 0 | 0 | - | 3.4300 | 3.5000 | 3.5700 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<18 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{IDD}}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current |  |  |  |  |  |
| $I_{\text {CC1 }}$ | No Switching | - | 8.5 | 13.5 | mA |
| ICC2 | No Switching | - | 1.6 | 3.0 | mA |
| Operating $\mathrm{I}_{\text {CC1 }}$ | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 8.0 | 13 | mA |
| Operating ICC2 | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.0 | 5.0 | mA |
| $\mathrm{C}_{\text {OFF }}$ |  |  |  |  |  |
| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\text {SS }}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{s}$ |
| Extension Charge Time | $\mathrm{V}_{\text {SS }}=\mathrm{V}_{\text {FFB }}=0$ | 5.0 | 8.0 | 11.0 | $\mu \mathrm{s}$ |
| Discharge Current | $\mathrm{C}_{\text {OFF }}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\text {FB }}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |
| Time Out Timer |  |  |  |  |  |
| Time Out Time | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ; \\ & \text { Record } \mathrm{V}_{\mathrm{GATE}(\mathrm{H})} \text { Pulse High Duration } \end{aligned}$ | 10 | 30 | 65 | $\mu \mathrm{s}$ |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 70 | \% |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| SO-16 |  |  |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID4 }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is High (logic one), the DAC range is 2.10 V to 3.50 V with 100 mV increments. When $\mathrm{V}_{\text {ID } 4}$ is Low (logic zero), the DAC range is 1.30 V to 2.05 V with 50 mV increments. $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID4 }}$ select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.2440 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal $60 \mu$ A current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE(H) }}$ | High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ from being in high state simultaneously. |
| 11 | PGND | High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 1.5 A peak switching current. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC and low side gate driver. |
| 14 | LGND | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{F B}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## $\mathrm{V}^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. ${ }^{2}$ Control Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5159 uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $25 \mu$ s timer, minimizing stress to the power components.

## Programmable Output

The CS5159 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.10 V to 3.50 V in 100 mV steps, the second is 1.30 V to 2.05 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5159 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.
If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE $(\mathrm{H})$ pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.
When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the COFF capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by
the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $2.0 \mathrm{~V} /$ div.)
Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ and $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $5.0 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Figure 4. CS5159 Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4- Soft Start Pin (2.0 V/div.)
Figure 5. CS5159 Demonstration Board Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1-Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 6. CS5159 Demonstration Board Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the C CopF capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} /$ div.) Trace 2- Inductor Switching Node (5.0 V/div.)

Figure 7. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=0.5 \mathrm{~A}$ (Light Load)


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node (5.0 V/div.)
Figure 8. Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$,

$$
\text { lout = } 13 \text { A (Heavy Load) }
$$

## Transient Response

The CS5159 $\mathrm{V}^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


[^36]Figure 9. CS5159 Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V)


Trace 1-Regulator Output Voltage ( $100 \mathrm{mV} /$ div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$. )
Trace 3- Output Current ( 0.5 to 13 Amps ) ( $10 \mathrm{~A} / \mathrm{div}$.)
Figure 10. CS5159 Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V). Upon Completing a Normal Off Time, The V ${ }^{2}$ Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100\% Duty Cycle. Regulation is Achieved in Less Than $20 \mu \mathrm{~s}$


Trace 1- Regulator Output Voltage ( $100 \mathrm{mV} /$ div.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- Output Current (13 to 0,5 Amps) (10 A/div.)
Figure 11. CS5159 Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V ). V² Control Topology Immediately Connects Inductor to Ground, Providing 0\% Duty Cycle. Regulation is Achieved in Less Than $10 \mu \mathrm{~s}$

## PROTECTION AND MONITORING FEATURES

## $V_{\text {CC1 }}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs ( $\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}$ ), the $\mathrm{V}_{\text {FFB }}$ low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=$ $3.3 \%$ ), while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.) Trace 3- Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5159 Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. Startup with Regulator Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15 ). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.


Trace 4-5.0 V from PC Power Supply (5.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node 5.0 V/div.)
Figure 14. OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Figure 15. OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\text {FFB }}$ pin low, emulating a short circuit condition.


Figure 16. Implementing Shutdown with the CS5159

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power Good }}$.


Figure 17. Implementing Power Good with the CS5159


Trace 3-12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) ( $10 \mathrm{~V} /$ div.)
Trace 4-5.0 V Input (2.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 18. CS5159 Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

## Selecting External Components

The CS5159 can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.
Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the
typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\operatorname{VGATE}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{~L})=12 \mathrm{~V}
$$

(see Figure 19.)


Figure 19. CS5159 Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is RDS $_{\text {ON }}$, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\text { ILOAD }^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\operatorname{ILOAD}{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =

$$
\frac{\mathrm{V}_{\text {OUT }}+(\mathrm{lLOAD} \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\mathrm{V}_{\text {IN }}+(\mathrm{ILOAD} \times \mathrm{RDS} \text { ON OF SYNCH FET }) \\
-(\mathrm{ILOAD} \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (COFF)

The Coff timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { COFF } \times 4848.5
$$

When the $\mathrm{V}_{\mathrm{FFB}}$ pin is less than 1.0 V , the current charging the $\mathrm{C}_{\mathrm{OFF}}$ capacitor is reduced. The extended off time can be calculated as follows:

$$
\text { TOFF }=\text { COFF } \times 24,242.5
$$

Off time will be determined by either the $\mathrm{T}_{\mathrm{OFF}}$ time, or the time out timer, whichever is longer.

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\mathrm{OFF}}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. The CS5159 reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous MOSFET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=\mathrm{V}_{\mathrm{BD}} \times$ ILOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5159 demonstration board as shown in Figure 8;

$$
\text { Power }=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}
$$

This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:
Thermal Impedance $=\frac{\text { TJUNCTION }(M A X)-\text { TAMBIENT }}{\text { Power }}$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 20. Filter Components


Figure 21. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. Connect the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
7. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.
Route gate drive signals $\mathrm{V}_{\text {GATE(H) }}$ (pin 10) and $\mathrm{V}_{\text {GATE(L) }}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.


Figure 22. Layout Guidelines

CS5159


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing


Figure 24. Additional Application Diagram, 12 V to 3.3 V/5.0 A Converter With Remote Sense


Figure 25. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias

## CS5159

PACKAGE THERMAL DATA

| Parameter |  | 16-SO | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\Theta J A}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5160

## CPU 5-Bit Synchronous Buck Controller

The CS5160 is a 5 -bit synchronous dual N -Channel buck controllers designed to provide unprecedented transient response for today's demanding high-density, high-speed logic. It operates using a proprietary control method which allows a 100 ns response time to load transients. The CS5160 is designed to operate over a 9-16 V range $\left(\mathrm{V}_{\mathrm{CC}}\right)$ using 12 V to power the IC and 5.0 V as the main supply for conversion.

The CS5160 is specifically designed to power Pentium® III processors and other high performance core logic. They include the following features: on board 5-bit DAC, short circuit protection, $1.0 \%$ output tolerance, $\mathrm{V}_{\mathrm{CC}}$ monitor, and programmable Soft Start capability. The CS5160 is available in a 16 pin surface mount package.

## Features

- Dual N-Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5-Bit DAC
- Backward Compatible with CS515X Family
- 30 ns Gate Rise/Fall Times
- $0.8 \%$ DAC Accuracy for the 01111 DAC Code
- 5.0 V \& 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- $\mathrm{V}_{\mathrm{CC}}$ Monitor
- $\mathrm{V}^{2 \mathrm{Tm}}$ Control Topology
- Overvoltage Protection

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


## PIN CONNECTIONS



## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5160GD16 | SO-16 | 48 Units/Rail |
| CS5160GDR16 | SO-16 | 2500 Tape \& Reel |

## CS5160



Figure 1. Application Diagram, 5.0 V to 1.5 V/15 A Core Logic Converter with 12 V Bias

MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 0 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC} 1}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| $\mathrm{V}_{\mathrm{CC} 2}$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| SS | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-100 \mu \mathrm{~A}$ |
| COMP | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $200 \mu \mathrm{~A}$ |

## CS5160

MAXIMUM RATINGS (continued)

| Pin Name | Max Operating Voltage | Max Current |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{FB}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{C}_{\mathrm{OFF}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{FFB}}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-0.2 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{IDO}}-\mathrm{V}_{\mathrm{ID} 4}$ | $6.0 \mathrm{~V} /-0.3 \mathrm{~V}$ | $-50 \mu \mathrm{~A}$ |
| $\mathrm{~V}_{\mathrm{GATE}(\mathrm{H})}$ | $18 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $16 \mathrm{~V} /-0.3 \mathrm{~V}$ | $100 \mathrm{~mA} \mathrm{DC} / 1.5 \mathrm{~A}$ peak |
| LGnd | 0 V | 25 mA |
| PGnd | 0 V | $100 \mathrm{~mA} \mathrm{DC/1.5} \mathrm{~A} \mathrm{peak}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=\mathrm{V}_{\mathrm{ID} 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |


| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.3 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Open Loop Gain | $1.25 \mathrm{~V}<\mathrm{V}_{\mathrm{COMP}}, 4.0 \mathrm{~V} ; \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F} ;$ <br> Note 2 | - | 80 | - | dB |
| Unity Gain Bandwidth | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F} ; \mathrm{Note} 2$ | - | 50 | - | kHz |
| COMP SINK Current | $\mathrm{V}_{\mathrm{COMP}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}>2.0 \mathrm{~V}$ | 30 | 60 | 120 | $\mu \mathrm{~A}$ |
| COMP SOURCE Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| COMP CLAMP Current | $\mathrm{V}_{\mathrm{COMP}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V}$ | 0.4 | 1.0 | 1.6 | mA |
| COMP High Voltage | $\mathrm{V}_{\mathrm{FB}}=2.7 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 4.0 | 4.3 | 5.0 | V |
| COMP Low Voltage | $\mathrm{V}_{\mathrm{FB}}=3.0 \mathrm{~V}$ | - | 1.00 | 1.15 | V |
| PSRR | $8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} @ 1.0 \mathrm{kHz} ;$ <br> C | - | 70 | - | dB |
| Transconductance $=0.1 \mu \mathrm{~F} ; \mathrm{Note} 2$ |  |  |  |  |  |

## $\mathrm{V}_{\text {cC1 }}$ Monitor

| Start Threshold | Output switching | 8.60 | 8.95 | 9.30 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Stop Threshold | Output not switching | 8.45 | 8.80 | 9.15 | V |
| Hysteresis | Start-Stop | - | 150 | - | mV |

## Soft Start (SS)

| Charge Time | 1 | 1.6 | 3.3 | 5.0 | ms |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Pulse Period | - | 25 | 100 | 200 | ms |
| Duty Cycle | $($ Charge Time $/$ Pulse Period $) \times 100$ | 1.0 | 3.3 | 6.0 | $\%$ |
| COMP Clamp Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=0$ | 0.50 | 0.95 | 1.10 | V |
| $\mathrm{~V}_{\mathrm{FFB}}$ SS Fault Disable | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ Low; $\mathrm{V}_{\mathrm{GATE}}(\mathrm{L})=$ Low | 0.9 | 1.0 | 1.1 | V |
| High Threshold | - | - | 2.5 | 3.0 | V |

2. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{I D 2}=\mathrm{V}_{I D 1}=\mathrm{V}_{I D 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| PWM Comparator |  |  |  |  |  |
| Transient Response | $\mathrm{V}_{\mathrm{FFB}}=0$ to 5.0 V to $\mathrm{V}_{\mathrm{GATE}(H)}=9.0 \mathrm{~V}$ to $1.0 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ | - | 100 | 125 | ns |
| $\mathrm{~V}_{\text {FFB }}$ Bias Current | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | - | 0.3 | - | $\mu \mathrm{A}$ |

DAC

| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID4 }}$ | 1.00 | 1.25 | 2.40 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Pull Up Resistance |  |  |  |  | $\mathrm{V}_{\text {IDO }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID } 4}$ | 25 | 50 | 110 | k $\Omega$ |
| Pull Up Voltage |  |  |  |  | - | 4.85 | 5.00 | 5.15 | V |
| Accuracy (all codes except 11111, 10110, 10101, 10100, 10011, 10010, 10001, 10000, and 01111) |  |  |  |  | $\begin{aligned} & \text { Measure } V_{F B}=C O M P, \\ & C S 5160: 25^{\circ} \mathrm{C} \leq T_{J} \leq 85^{\circ} \mathrm{C} \end{aligned}$ | - | - | 1.0 | \% |
| $V_{\text {ID4 }}$ | $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID } 1}$ | $\mathrm{V}_{\text {ID }}$ |  |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | - | 1.2896 | 1.3000 | 1.3104 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.3365 | 1.3500 | 1.3635 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.3860 | 1.4000 | 1.4140 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.4355 | 1.4500 | 1.4645 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.4850 | 1.5000 | 1.5150 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.5345 | 1.5500 | 1.5655 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.5840 | 1.6000 | 1.6160 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.6335 | 1.6500 | 1.6665 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.6830 | 1.7000 | 1.7170 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.7325 | 1.7500 | 1.7675 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.7820 | 1.8000 | 1.8180 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.8315 | 1.8500 | 1.8685 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.8810 | 1.9000 | 1.9190 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.9305 | 1.9500 | 1.9695 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.9800 | 2.0000 | 2.0200 | V |
| 0 | 0 | 0 | 0 | 0 | - | 2.0295 | 2.0500 | 2.0705 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.2191 | 1.2440 | 1.2689 | V |
| 1 | 1 | 1 | 1 | 0 | - | 2.0790 | 2.1000 | 2.1210 | V |
| 1 | 1 | 1 | 0 | 1 | - | 2.1780 | 2.2000 | 2.2220 | V |
| 1 | 1 | 1 | 0 | 0 | - | 2.2770 | 2.3000 | 2.3230 | V |
| 1 | 1 | 0 | 1 | 1 | - | 2.3760 | 2.4000 | 2.4240 | V |
| 1 | 1 | 0 | 1 | 0 | - | 2.4750 | 2.5000 | 2.5250 | V |
| 1 | 1 | 0 | 0 | 1 | - | 2.5740 | 2.6000 | 2.6260 | V |
| 1 | 1 | 0 | 0 | 0 | - | 2.6730 | 2.7000 | 2.7270 | V |
| 1 | 0 | 1 | 1 | 1 | - | 2.7720 | 2.8000 | 2.8280 | V |
| 1 | 0 | 1 | 1 | 0 | - | 2.8420 | 2.9000 | 2.9580 | V |
| 1 | 0 | 1 | 0 | 1 | - | 2.9400 | 3.0000 | 3.0600 | V |
| 1 | 0 | 1 | 0 | 0 | - | 3.0380 | 3.1000 | 3.1620 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<+85^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 1}<14 \mathrm{~V} ; 5.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC} 2}<16 \mathrm{~V}\right.$; DAC Code: $\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{I D 2}=\mathrm{V}_{I D 1}=\mathrm{V}_{I D 0}=1 ; \mathrm{V}_{\mathrm{ID} 3}=0 ; \mathrm{CV}_{\mathrm{GATE}(\mathrm{L})}$ and $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=1.0 \mathrm{nF} ; \mathrm{C}_{\mathrm{OFF}}=330 \mathrm{pF} ; \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, unless otherwise specified.)

| Characteristic |  |  |  |  |  |  |  |  | Test Conditions | Min |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DAC | Typ | Max | Unit |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 1 | 1 | - | 3.1360 | 3.2000 | 3.2640 | V |  |
| 1 | 0 | 0 | 1 | 0 | - | 3.2340 | 3.3000 | 3.3660 | V |  |
| 1 | 0 | 0 | 0 | 1 | - | 3.3320 | 3.4000 | 3.4680 | V |  |
| 1 | 0 | 0 | 0 | 0 | - | 3.4300 | 3.5000 | 3.5700 | V |  |

$\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$

| Out SOURCE Sat at 100 mA | Measure $\mathrm{V}_{\mathrm{CC} 1}-\mathrm{V}_{\mathrm{GATE}(\mathrm{L})} ; \mathrm{V}_{\mathrm{CC} 2}-\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ | - | 1.2 | 2.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Out SINK Sat at 100 mA |  | - | 1.0 | 1.5 | V |
| Out Rise Time | $\begin{aligned} & 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}<9.0 \mathrm{~V} ; 1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})} \\ & <9.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Out Fall Time | $\begin{aligned} & 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}>1.0 \mathrm{~V} ; 9.0 \mathrm{~V}>\mathrm{V}_{\mathrm{GATE}(\mathrm{~L})} \\ & >1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V} \end{aligned}$ | - | 30 | 50 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ falling to $1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ rising to 1.0 V | 45 | 70 | 95 | ns |
| Delay $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ to $\mathrm{V}_{\operatorname{GATE}(\mathrm{H})}$ | $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ falling to $1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=8.0 \mathrm{~V}$ $\mathrm{CV}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF} ; \mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ rising to 1.0 V | 45 | 70 | 95 | ns |
| $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})} \mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ Resistance | Resistor to LGnd. Note 3 | 20 | 50 | 100 | $\mathrm{k} \Omega$ |
| $\mathrm{V}_{\text {GATE(H), }} \mathrm{V}_{\text {GATE(L) }}$ Schottky | LGnd to $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})} @ 10 \mathrm{~mA}$; LGnd to $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ @ 10 mA | - | 600 | 800 | mV |

## Supply Current

| $\mathrm{I}_{\mathrm{CC} 1}$ No Switching | - | - | 9.5 | 14.5 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{CC} 2}$ No Switching | - | - | 2.0 | 3.5 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 1}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 9.0 | 14 | mA |
| Operating $\mathrm{I}_{\mathrm{CC} 2}$ | $\mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}=\mathrm{V}_{\mathrm{FFB}}$ | - | 2.5 | 5.5 | mA |

CofF

| Normal Charge Time | $\mathrm{V}_{\mathrm{FFB}}=1.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{SS}}=5.0 \mathrm{~V}$ | 1.0 | 1.6 | 2.2 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Current | C $_{\text {OFF }}$ to $5.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}>1.0 \mathrm{~V}$ | 5.0 | - | - | mA |

Time Out Timer

| Time Out Time | $V_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} ; \mathrm{V}_{\mathrm{FFB}}=2.0 \mathrm{~V} ;$ <br> Record $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ Pulse High Duration | 10 | 30 | 65 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Fault Mode Duty Cycle | $\mathrm{V}_{\mathrm{FFB}}=0 \mathrm{~V}$ | 35 | 50 | 70 | $\%$ |

3. Guaranteed by design, not $100 \%$ tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| 16 Lead SO Narrow |  |  |


| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID }}$ | Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is High (logic one), the DAC range is 2.10 V to 3.50 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is Low (logic zero), the DAC range is 1.30 V to 2.05 V with 50 mV increments. $\mathrm{V}_{\text {IDO }}-\mathrm{V}_{\text {ID4 }}$ select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.2440 V , allowing for adjustable output voltage, using a traditional resistor divider. |
| :---: | :---: | :---: |
| 5 | SS | Soft Start Pin. A capacitor from this pin to LGnd in conjunction with internal $60 \mu \mathrm{~A}$ current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal $2.0 \mu \mathrm{~A}$ current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted. |
| 7 | $\mathrm{C}_{\text {OFF }}$ | A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture. |
| 8 | $\mathrm{V}_{\text {FFB }}$ | Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time. |
| 9 | $\mathrm{V}_{\mathrm{CC} 2}$ | Boosted power for the high side gate driver. |
| 10 | $\mathrm{V}_{\text {GATE(H) }}$ | High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}$ and $\mathrm{V}_{\mathrm{GATE}(\mathrm{L})}$ from being in high state simultaneously. |
| 11 | PGnd | High current ground for the IC. The MOSFET drivers are referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin. |
| 12 | $\mathrm{V}_{\text {GATE(L) }}$ | Low FET driver pin capable of 1.5 A peak switching current. |
| 13 | $\mathrm{V}_{\mathrm{CC} 1}$ | Input power for the IC and low side gate driver. |
| 14 | LGnd | Signal ground for the IC. All control circuits are referenced to this pin. |
| 15 | COMP | Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier. |
| 16 | $V_{\text {FB }}$ | Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace. |



Figure 2. Block Diagram

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## V $^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.


Figure 3. V ${ }^{2}$ Control Diagram

The $\mathrm{V}^{2}$ control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off Time

To maximize transient response, the CS5160 uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. To maintain regulation, the $\mathrm{V}^{2}$ control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to $100 \%$ on a pulse by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub-harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal $30 \mu \mathrm{~s}$ timer, minimizing stress to the power components.

## Programmable Output

The CS5160 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.10 V to 3.50 V in 100 mV steps, the second is 1.30 V to 2.05 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5160 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{FFB}}$ pins, as in traditional controllers.

## Start Up

Until the voltage on the $\mathrm{V}_{\mathrm{CC} 1}$ supply pin exceeds the 9.05 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the $\mathrm{V}_{\mathrm{CC} 1}$ pin exceeds the monitor threshold, the GATE $(\mathrm{H})$ output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a $50 \%$ duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C $\mathrm{C}_{\mathrm{OFF}}$ capacitor. The $\mathrm{V}^{2}$ control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.
The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by
the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).


Figure 4. CS5160 Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output


Trace 1-Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$.)
Trace 3- COMP PIn (error amplifier output) (1.0 V/div.) Trace 4- Soft Start Pin (2.0 V/div.)

Figure 5. CS5160 Startup Waveforms
If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).


Trace 1- Regulator Output Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} /$ div.)
Figure 6. CS5160 Enable Startup Waveforms

## Normal Operation

During normal operation, switch off time is constant and set by the $\mathrm{C}_{\mathrm{OFF}}$ capacitor. Switch on time is adjusted by the $\mathrm{V}^{2}$ control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).


Figure 7. CS5160 Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, lout $=0.5$ A (Light Load)


Trace 1-Regulator Output Voltage ( $10 \mathrm{mV} / \mathrm{div}$.)
Trace 2- Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$.)
Figure 8. CS5160 Peak-to-Peak Ripple on $\mathrm{V}_{\text {OUT }}=2.8 \mathrm{~V}$, $\mathrm{l}_{\text {OUT }}=13$ A (Heavy Load)

## Transient Response

The CS5160 $\mathrm{V}^{2}$ control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.


Trace 2- Regulator Output Voltage (output set for $1.55 \mathrm{~V}, 20 \mathrm{mV} /$ div.)
Figure 9. CS5160 Pentium ${ }^{\circledR}$ III Converter Output Voltage Response to a 12 A Load Pulse


Figure 10. CS5160 Pentium ${ }^{\circledR}$ III Converter Output Voltage Response to a 0 to 12 A Load Increase


Trace 2- Regulator Output Voltage (output set for $1.55 \mathrm{~V}, 20 \mathrm{mV} / \mathrm{div}$.)
Figure 11. CS5160 Pentium ${ }^{\circledR}$ III Converter Output Voltage Response to a 12 to 0 A Load Decrease

## PROTECTION AND MONITORING FEATURES

## $V_{\text {CC1 }}$ Monitor

To maintain predictable startup and shutdown characteristics an internal $\mathrm{V}_{\mathrm{CC} 1}$ monitor circuit is used to prevent the part from operating below 8.95 V minimum startup. The $\mathrm{V}_{\mathrm{CC} 1}$ monitor comparator provides hysteresis and guarantees a 8.80 V minimum shutdown threshold.

## Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs $\left(\mathrm{V}_{\mathrm{FFB}}<1.0 \mathrm{~V}\right)$, the $\mathrm{V}_{\mathrm{FFB}}$ low comparator sets the FAULT
latch. This causes the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a $2.0 \mu \mathrm{~A}$ current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a $50 \%$ duty cycle, while the Soft Start capacitor is charged with a $60 \mu \mathrm{~A}$ charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low $\mathrm{V}_{\mathrm{FFB}}$ comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses $(2.0 \mu \mathrm{~A} / 60 \mu \mathrm{~A}=3.3 \%)$, while actual duty cycle is half that due to the extended off time mode ( $1.65 \%$ ).

This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.


Trace 4-5.0 V Supply Voltage (2.0 V/div.) Trace 3- Soft Start Timing Capacitor (1.0 V/div.)
Trace 2- Inductor Switching Node (2.0 V/div.)
Figure 12. CS5160 Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge


Figure 13. CS5160 Startup with Regulator
Output Shorted

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns , causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.


Trace 4-5.0 V from PC Power Supply (5.0 V/div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Inductor Switching Node 5.0 V/div.)
Figure 14. CS5160 OVP Response to an Input-to-Output Short Circuit by Immediately Providing 0\% Duty Cycle, Crow-Barring the Input Voltage to Ground


Figure 15. CS5160 OVP Response to an Input-to-Output Short Circuit by Pulling the Input Voltage to Ground

## External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 14). This circuit operates by pulling the Soft Start pin high, and the $\mathrm{V}_{\text {FFB }}$ pin low, emulating a short circuit condition.


Figure 16. Implementing Shutdown with the CS5160

## External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$
V_{\text {Power Good }}=\frac{(\mathrm{R} 1+\mathrm{R} 2) \times 0.65 \mathrm{~V}}{\mathrm{R} 2}
$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{\text {Power Good }}$.


Figure 17. Implementing Power Good with the CS5160


Trace 3 - 12 V Input ( $\mathrm{V}_{\mathrm{CC} 1}$ ) and ( $\mathrm{V}_{\mathrm{CC} 2}$ ) (10 V/div.)
Trace 4-5.0 V Input ( $2.0 \mathrm{~V} /$ div.)
Trace 1- Regulator Output Voltage (1.0 V/div.)
Trace 2- Power Good Signal (2.0 V/div.)
Figure 18. CS5160 During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V

## Slope Compensation

The $\mathrm{V}^{2}$ control method uses a ramp signal, generated by the ESR of the output capacitors, that is proportional to the ripple current through the inductor. To maintain regulation, the $\mathrm{V}^{2}$ control loop monitors this ramp signal, through the PWM comparator, and terminates the switch on-time.
The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope presented to the PWM comparator, due to the very low ESR, can lead to pulse width jitter and variation caused by both random or synchronous noise.
Adding slope compensation to the control loop, avoids erratic operation of the PWM circuit, particularly at lower duty cycles and higher frequencies, where there is not enough ramp signal, and provides a more stable switchpoint.
The scheme that prevents that switching noise prematurely triggers the PWM circuit consists of adding a positive voltage slope to the output of the Error Amplifier (COMP pin) during an off-time cycle.

The circuit that implements this function is shown in Figure 19.


Figure 19. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of each On-Time Cycle
The ramp waveform is generated through a small RC filter that provides the proper voltage ramp at the beginning of each on-time cycle. The resistors R1 and R2 in the circuit of Figure 14 form a voltage divider from the GATE(L) output, superimposing a small artificial ramp on the output of the error amplifier. It is important that the series combination $\mathrm{R} 1 / \mathrm{R} 2$ is high enough in resistance not to load down and negatively affect the slew rate on the GATE(L) pin.

## Selecting External Components

The CS5160 can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

## NFET Power Transistors

Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the typical application where $\mathrm{V}_{\mathrm{CC} 1}=\mathrm{V}_{\mathrm{CC} 2}=12 \mathrm{~V}$ and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$
\operatorname{VGATE}(\mathrm{H})=12 \mathrm{~V}-5.0 \mathrm{~V}=7.0 \mathrm{~V}, \mathrm{VGATE}(\mathrm{~L})=12 \mathrm{~V}
$$

(see Figure 20.)


Figure 20. CS5160 Gate Drive Waveforms Depicting Rail to Rail Swing
The most important aspect of MOSFET performance is RDS $_{\mathrm{ON}}$, which effects regulator efficiency and MOSFET thermal management requirements.
The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$
\text { Power }=\operatorname{lLOAD}^{2} \times \text { RDSON } \times \text { duty cycle }
$$

Synchronous MOSFET:

$$
\text { Power }=\mathrm{I}_{\mathrm{LOAD}}{ }^{2} \times \text { RDSON } \times(1-\text { duty cycle })
$$

Duty Cycle =

$$
\frac{\text { VOUT }+(\text { LLOAD } \times \text { RDSON OF SYNCH FET })}{\left[\begin{array}{l}
\text { VIN }+(\text { ILOAD } \times \text { RDSON OF SYNCH FET }) \\
-(\text { ILOAD } \times \text { RDSON OF SWITCH FET })
\end{array}\right]}
$$

## Off Time Capacitor (Coff)

The C CFF timing capacitor sets the regulator off time:

$$
\text { TOFF }=\text { CofF } \times 4848.5
$$

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the $\mathrm{C}_{\text {OFF }}$ timing capacitor:

$$
\text { COFF }=\frac{\text { Perioid } \times(1-\text { duty cycle })}{4848.5}
$$

where:

$$
\text { Period }=\frac{1}{\text { switching frequency }}
$$

## Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. For a design operating at 200 kHz or so, the low non-overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:
Power $=\mathrm{V}_{\mathrm{BD}} \times$ ILOAD $\times$ conduction time $\times$ switching frequency
Where $\mathrm{V}_{\mathrm{BD}}=$ the forward drop of the MOSFET body diode. For the CS5160 demonstration board as shown in Figure 8;
Power $=1.6 \mathrm{~V} \times 13 \mathrm{~A} \times 100 \mathrm{~ns} \times 233 \mathrm{kHz}=0.48 \mathrm{~W}$
This is only $1.3 \%$ of the 36.4 W being delivered to the load.

## Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

## Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:
Thermal Impedance $=\frac{\text { TJUNCTION } \text { MAX })- \text { TAMBIENT }}{\text { Power }}$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.


Figure 21. Filter Components


Figure 22. Input Filter

## Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGnd).
2. Connect pin 11 (PGnd) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin $8\left(\mathrm{~V}_{\mathrm{FFB}}\right)$ and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGnd).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGnd).
6. Connect the $\mathrm{V}_{\mathrm{FB}}$ pin directly to the load with a separate trace (remote sense).
7. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.
Route gate drive signals $\mathrm{V}_{\text {GATE(H) }}$ (pin 10) and $\mathrm{V}_{\text {GATE(L) }}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.


Figure 23. Layout Guidelines

## ADDITIONAL APPLICATION DIAGRAMS



Figure 24. 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias


Figure 25. Pentium ${ }^{\circledR}$ III Converter with Slope Compensation and Adaptive Voltage Positioning

PACKAGE THERMAL DATA

| Parameter |  | 16 Lead SO Narrow | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS51311

## Synchronous CPU <br> Buck Controller for 12 V and 5.0 V Applications

The CS51311 is a synchronous dual NFET Buck Regulator Controller. It is designed to power the core logic of the latest high performance CPUs. It uses the $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation. It incorporates many additional features required to ensure the proper operation and protection of the CPU and Power system. The CS51311 provides the industry's most highly integrated solution, minimizing external component count, total solution size, and cost.

The CS51311 is specifically designed to power Intel's Pentium ${ }^{\circledR}$ II processor and includes the following features: 5-bit DAC with $1.2 \%$ tolerance, Power Good output, overcurrent hiccup mode protection, $\mathrm{V}_{\mathrm{CC}}$ monitor, soft start, adaptive voltage positioning, adaptive FET non-overlap time, and remote sense. The CS51311 will operate over an 8.4 V to 14 V range and is available in 14 lead narrow body surface mount package.

## Features

- Synchronous Switching Regulator Controller for CPU VCORE
- Dual N-Channel MOSFET Synchronous Buck Design
- $\mathrm{V}^{2}$ Control Topology
- 200 ns Transient Loop Response
- 5-Bit DAC with $1.2 \%$ Tolerance
- Hiccup Mode Overcurrent Protection
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- 65 ns Adaptive FET Non-Overlap Time
- Adaptive Voltage Positioning
- Power Good Output Monitors Regulator Output
- $\mathrm{V}_{\mathrm{CC}}$ Monitor Provides Undervoltage Lockout
- Enable Through Use of the COMP Pin

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com



A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51311GD14 | SO-14 | 55 Units/Rail |
| CS51311GDR14 | SO-14 | 2500 Tape \& Reel |



Figure 1. Application Diagram

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Uperating Junction Temperature, $T_{J}$ | Reflow: (SMD styles only) (Note 1 ) | 230 peak |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature Range, $\mathrm{T}_{S}$ | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility |  | 2.0 |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| IC Power Input | $\mathrm{V}_{\mathrm{CC}}$ | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | 1.5 A Peak, 200 mA DC |
| Compensation Pin | COMP | 6.0 V | -0.3 V | 1.0 mA | 5.0 mA |
| Voltage Feedback Input, <br> Output Voltage Sense Pin, <br> Voltage ID DAC Inputs | $\mathrm{V}_{\text {FB }}, \mathrm{V}_{\text {OUT }}, \mathrm{V}_{\text {IDO-4 }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Off-Time Pin | COFF | 6.0 V | -0.3 V | 1.0 mA |  |
| High-Side, Low-Side FET Drivers | GATE(H), GATE(L) | 16 V | -0.3 V DC | 1.5 A Peak, 200 mA DC | 1.5 A Peak, 200 mA DC |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | 1.0 mA | 30 mA |
| Ground | GND | 0 V | 0 V | 1.5 A Peak, 200 mA DC | $\mathrm{N} / \mathrm{A}$ |

## CS51311

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$;
2.0 V DAC Code ( $\left.\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}$, $\mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions |  |
| :---: | :---: | :---: |

Voltage Identification DAC

|  |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}}, \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$. Note 2 |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  | $75^{\circ} \mathrm{C} \leq \mathrm{T}$ | $\leq 125^{\circ} \mathrm{C}$ |  |  | $25^{\circ} \mathrm{C} \leq$ | $\leq 75^{\circ} \mathrm{C}$ |  |  |
| $\mathrm{V}_{\text {ID4 }}$ | $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $\mathrm{V}_{\text {IDO }}$ | Min | Typ | Max | $\pm$ Tol | Min | Typ | Max | $\pm$ Tol | Unit |
| 1 | 0 | 0 | 0 | 0 | 3.483 | 3.525 | 3.567 | 1.2\% | 3.455 | 3.525 | 3.596 | 2.0\% | V |
| 1 | 0 | 0 | 0 | 1 | 3.384 | 3.425 | 3.466 | 1.2\% | 3.357 | 3.425 | 3.494 | 2.0\% | V |
| 1 | 0 | 0 | 1 | 0 | 3.285 | 3.325 | 3.365 | 1.2\% | 3.259 | 3.325 | 3.392 | 2.0\% | V |
| 1 | 0 | 0 | 1 | 1 | 3.186 | 3.225 | 3.264 | 1.2\% | 3.161 | 3.225 | 3.290 | 2.0\% | V |
| 1 | 0 | 1 | 0 | 0 | 3.087 | 3.125 | 3.163 | 1.2\% | 3.063 | 3.125 | 3.188 | 2.0\% | V |
| 1 | 0 | 1 | 0 | 1 | 2.989 | 3.025 | 3.061 | 1.2\% | 2.965 | 3.025 | 3.086 | 2.0\% | V |
| 1 | 0 | 1 | 1 | 0 | 2.890 | 2.925 | 2.960 | 1.2\% | 2.875 | 2.925 | 2.975 | 1.7\% | V |
| 1 | 0 | 1 | 1 | 1 | 2.791 | 2.825 | 2.859 | 1.2\% | 2.777 | 2.825 | 2.873 | 1.7\% | V |
| 1 | 1 | 0 | 0 | 0 | 2.692 | 2.725 | 2.758 | 1.2\% | 2.679 | 2.725 | 2.771 | 1.7\% | V |
| 1 | 1 | 0 | 0 | 1 | 2.594 | 2.625 | 2.657 | 1.2\% | 2.580 | 2.625 | 2.670 | 1.7\% | V |
| 1 | 1 | 0 | 1 | 0 | 2.495 | 2.525 | 2.555 | 1.2\% | 2.482 | 2.525 | 2.568 | 1.7\% | V |
| 1 | 1 | 0 | 1 | 1 | 2.396 | 2.425 | 2.454 | 1.2\% | 2.389 | 2.425 | 2.461 | 1.5\% | V |
| 1 | 1 | 1 | 0 | 0 | 2.297 | 2.325 | 2.353 | 1.2\% | 2.290 | 2.325 | 2.360 | 1.5\% | V |
| 1 | 1 | 1 | 0 | 1 | 2.198 | 2.225 | 2.252 | 1.2\% | 2.192 | 2.225 | 2.258 | 1.5\% | V |
| 1 | 1 | 1 | 1 | 0 | 2.099 | 2.125 | 2.151 | 1.2\% | 2.093 | 2.125 | 2.157 | 1.5\% | V |
| 0 | 0 | 0 | 0 | 0 | 2.050 | 2.075 | 2.100 | 1.2\% | 2.044 | 2.075 | 2.106 | 1.5\% | V |
| 0 | 0 | 0 | 0 | 1 | 2.001 | 2.025 | 2.049 | 1.2\% | 1.995 | 2.025 | 2.055 | 1.5\% | V |
| 0 | 0 | 0 | 1 | 0 | 1.953 | 1.975 | 1.997 | 1.1\% | 1.945 | 1.975 | 2.005 | 1.5\% | V |
| 0 | 0 | 0 | 1 | 1 | 1.904 | 1.925 | 1.946 | 1.1\% | 1.896 | 1.925 | 1.954 | 1.5\% | V |
| 0 | 0 | 1 | 0 | 0 | 1.854 | 1.875 | 1.896 | 1.1\% | 1.847 | 1.875 | 1.903 | 1.5\% | V |
| 0 | 0 | 1 | 0 | 1 | 1.805 | 1.825 | 1.845 | 1.1\% | 1.798 | 1.825 | 1.852 | 1.5\% | V |
| 0 | 0 | 1 | 1 | 0 | 1.755 | 1.775 | 1.795 | 1.1\% | 1.748 | 1.775 | 1.802 | 1.5\% | V |
| 0 | 0 | 1 | 1 | 1 | 1.706 | 1.725 | 1.744 | 1.1\% | 1.699 | 1.725 | 1.751 | 1.5\% | V |
| 0 | 1 | 0 | 0 | 0 | 1.656 | 1.675 | 1.694 | 1.1\% | 1.650 | 1.675 | 1.700 | 1.5\% | V |
| 0 | 1 | 0 | 0 | 1 | 1.607 | 1.625 | 1.643 | 1.1\% | 1.601 | 1.625 | 1.649 | 1.5\% | V |
| 0 | 1 | 0 | 1 | 0 | 1.558 | 1.575 | 1.593 | 1.1\% | 1.551 | 1.575 | 1.599 | 1.5\% | V |
| 0 | 1 | 0 | 1 | 1 | 1.508 | 1.525 | 1.542 | 1.1\% | 1.502 | 1.525 | 1.548 | 1.5\% | V |
| 0 | 1 | 1 | 0 | 0 | 1.459 | 1.475 | 1.491 | 1.1\% | 1.453 | 1.475 | 1.497 | 1.5\% | V |
| 0 | 1 | 1 | 0 | 1 | 1.409 | 1.425 | 1.441 | 1.1\% | 1.404 | 1.425 | 1.446 | 1.5\% | V |
| 0 | 1 | 1 | 1 | 0 | 1.360 | 1.375 | 1.390 | 1.1\% | 1.354 | 1.375 | 1.396 | 1.5\% | V |
| 0 | 1 | 1 | 1 | 1 | 1.310 | 1.325 | 1.340 | 1.1\% | 1.305 | 1.325 | 1.345 | 1.5\% | V |
| 1 | 1 | 1 | 1 | 1 | 1.225 | 1.250 | 1.275 | 2.0\% | 1.225 | 1.250 | 1.275 | 2.0\% | V |

2. The IC power dissipation in a typical application with $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$, switching frequency $\mathrm{f}_{\mathrm{SW}}=250 \mathrm{kHz}, 50 \mathrm{nc}$ MOSFETs and $\mathrm{R}_{\theta \mathrm{JA}}=115^{\circ} \mathrm{C} / \mathrm{W}$ yields an operating junction temperature rise of approximately $52^{\circ} \mathrm{C}$, and a junction temperature of $77^{\circ} \mathrm{C}$ with an ambient temperature of $25^{\circ} \mathrm{C}$.

## CS51311

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$;
2.0 V DAC Code $\left(\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}$, $\mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Voltage Identification DAC (continued) | $9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 14 \mathrm{~V}$ | - | 0.01 | - | $\% / \mathrm{V}$ |
| Line Regulation | $\mathrm{V}_{\mathrm{ID} 4}, \mathrm{~V}_{\mathrm{ID} 3}, \mathrm{~V}_{I D 2}, \mathrm{~V}_{\mathrm{ID} 1}, \mathrm{~V}_{\mathrm{ID} 0}$ | 1.0 | 1.25 | 2.4 | V |
| Input Threshold | $\mathrm{V}_{\mathrm{ID} 4}, \mathrm{~V}_{\mathrm{ID} 3}, \mathrm{~V}_{\mathrm{ID} 2}, \mathrm{~V}_{\mathrm{ID} 1}, \mathrm{~V}_{\mathrm{ID} 0}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Input Pull-Up Resistance | - | 5.48 | 5.65 | 5.82 | V |
| Pull-Up Voltage |  |  |  |  |  |

## Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $0.2 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 3.5 \mathrm{~V}$ | -7.0 | 0.1 | 7.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| COMP Source Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V}$ to $3.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.9 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| COMP Sink Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.1 \mathrm{~V}$ | 30 | 60 | 120 | $\mu \mathrm{~A}$ |
| Open Loop Gain | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 80 | - | dB |
| Unity Gain Bandwidth | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 50 | - | kHz |
| PSRR @ 1.0 kHz | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 70 | - | dB |
| Transconductance |  | - | 32 | - | mmho |
| Output Impedance | - | - | 0.5 | - | $\mathrm{M} \Omega$ |

GATE(H) and GATE(L)

| High Voltage at 100 mA | Measure $\mathrm{V}_{\mathrm{CC}}-\mathrm{GATE}(\mathrm{L}) /(\mathrm{H})$ | - | 1.2 | 2.1 | V |
| :--- | :--- | :--- | :--- | :--- | :---: |
| Low Voltage at 100 mA | Measure $\operatorname{GATE}(\mathrm{L}) /(\mathrm{H})$ | - | 1.0 | 1.5 | V |
| Rise Time | $1.6 \mathrm{~V}<\mathrm{GATE}(\mathrm{H}) /(\mathrm{L})<\left(\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right)$ | - | 40 | 80 | ns |
| Fall Time | $\left(\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right)>\operatorname{GATE}(\mathrm{L}) /(\mathrm{H})>1.6 \mathrm{~V}$ | - | 40 | 80 | ns |
| GATE $(\mathrm{H})$ to GATE(L) Delay | $\mathrm{GATE}(\mathrm{H})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{~L})>2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE $(\mathrm{L})$ to GATE(H) Delay | GATE $(\mathrm{L})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{H})>2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-Down | Resistance to GND. Note 3 | 20 | 50 | 115 | $\mathrm{k} \Omega$ |

Overcurrent Protection

| OVC Comparator Offset Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 3.5 \mathrm{~V}$ | 77 | 86 | 101 | mV |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Discharge Threshold Voltage | -2.2 |  |  |  |  |  | 0.25 | 0.3 | V |
| $V_{\text {OUT }}$ Bias Current | $0.2 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 3.5 \mathrm{~V}$ | -7.0 | 0.1 | 7.0 | $\mu \mathrm{~A}$ |  |  |  |  |
| OVC Latch Discharge Current | $\mathrm{V}_{\text {COMP }}=1.0 \mathrm{~V}$ | 100 | 800 | 2500 | $\mu \mathrm{~A}$ |  |  |  |  |

PWM Comparator

| PWM Comparator Offset Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 3.5 \mathrm{~V}$ | 0.99 | 1.1 | 1.23 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Transient Response | $\mathrm{V}_{\mathrm{FB}}=0$ to 3.5 V | - | 200 | 300 | ns |

## Coff

| Off-Time |  | 1.0 | 1.6 | 2.3 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Charge Current | $\mathrm{V}_{\text {COFF }}=1.5 \mathrm{~V}$ | - | 550 | - | $\mu \mathrm{A}$ |
| Discharge Current | $\mathrm{V}_{\text {COFF }}=1.5 \mathrm{~V}$ | - | 25 | - | mA |

3. Guaranteed by design, not $100 \%$ tested in production.

## CS51311

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}\right.$; $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}$;
2.0 V DAC Code $\left(\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}$, $\mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output |  |  |  |  |  |
| PWRGD Sink Current | $\mathrm{V}_{\mathrm{FB}}=1.7 \mathrm{~V}, \mathrm{~V}_{\text {PWRGD }}=1.0 \mathrm{~V}$ | 0.5 | 4.0 | 15 | mA |
| PWRGD Upper Threshold | \% of Nominal DAC Code | 5.0 | 8.5 | 12 | \% |
| PWRGD Lower Threshold | \% of Nominal DAC Code | -12 | -8.5 | -5.0 | \% |
| PWRGD Output Low Voltage | $\mathrm{V}_{\mathrm{FB}}=1.7 \mathrm{~V}, \mathrm{I}_{\text {PWRGD }}=500 \mu \mathrm{~A}$ | - | 0.2 | 0.3 | V |

General Electrical Specifications

| $V_{\text {CC }}$ Monitor Start Threshold | - | 7.9 | 8.4 | 8.9 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ Monitor Stop Threshold | - | 7.6 | 8.1 | 8.6 | V |
| Hysteresis | Start-Stop | 0.15 | 0.3 | 0.6 | V |
| $\mathrm{~V}_{\text {CC }}$ Supply Current | No Load on GATE(H), GATE(L) | - | 12 | 20 | mA |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-14 | PIN SYMBOL | FUNCTION |
| 1, 2, 3, 4, 5 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | Voltage ID DAC inputs. These pins are internally pulled up to 5.65 V if left open. $\mathrm{V}_{\text {ID4 }}$ selects the DAC range. When $\mathrm{V}_{I D 4}$ is high (logic one), the Error Amp reference range is 2.125 V to 3.525 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is low (logic zero), the Error Amp reference voltage is 1.325 V to 2.075 V with 50 mV increments. |
| 6 | $\mathrm{V}_{\mathrm{FB}}$ | Error amp inverting input, PWM comparator non-inverting input, current limit comparator non-inverting input, PWRGD comparator input. |
| 7 | $\mathrm{V}_{\text {OUT }}$ | Current limit comparator inverting input. |
| 8 | $\mathrm{V}_{\mathrm{CC}}$ | Input power supply pin for the internal circuitry. Decouple with filter capacitor to GND. |
| 9 | GATE(H) | High side switch FET driver pin. |
| 10 | GND | Ground pin. |
| 11 | GATE(L) | Low side synchronous FET driver pin. |
| 12 | PWRGD | Power Good Output. Open collector output drives low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. |
| 13 | $\mathrm{C}_{\text {OFF }}$ | Off-Time Capacitor pin. A capacitor from this pin to GND sets the off time for the regulator. |
| 14 | COMP | Error amp output. PWM comparator inverting input. A capacitor on this pin provides error amp compensation. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. GATE(H) and GATE(L) Falltime vs. Load Capacitance


Figure 5. DAC Output Voltage vs. Temperature, DAC Code = 00001


Figure 4. GATE(H) and GATE(L) Risetime vs. Load Capacitance


Figure 6. Percent Output Error vs. DAC Output Voltage Setting, VID4 $=0$


Figure 7. Percent Output Error vs. DAC Output Voltage Setting, VID4 = 1

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## V $^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

The $\mathrm{V}^{2}$ control method is illustrated in Figure 8. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.


Figure 8. $\mathbf{V}^{2}$ Control Diagram
A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop.

The main purpose of this "slow" feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.
Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation.
A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off-Time

To minimize transient response, the CS51311 uses a Constant Off-Time method to control the rate of output pulses. During normal operation, the Off-Time of the high side switch is terminated after a fixed period, set by the CofF capacitor. Every time the $\mathrm{V}_{\mathrm{FB}}$ pin exceeds the COMP pin voltage an Off-Time is initiated. To maintain regulation, the $\mathrm{V}^{2}$ Control Loop varies switch On-Time. The PWM comparator monitors the output voltage ramp, and terminates the switch On-Time.
Constant Off-Time provides a number of advantages. Switch Duty Cycle can be adjusted from 0 to $100 \%$ on a pulse-by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ Duty Cycle operation can be maintained for extended periods of time in response to Load or Line transients.

## Programmable Output

The CS51311 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.125 V to 3.525 V in 100 mV steps, the second is 1.325 V to 2.075 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS51311 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ pin, as in traditional controllers. The CS51311 is specifically designed to meet or exceed Intel's Pentium II specifications.

## Error Amplifier

An inherent benefit of the $\mathrm{V}^{2}$ control topology is that there is no large bandwidth requirement on the error amplifier
design. The reaction time to an output load step has no relation to the crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this "slow" feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered. The COMP pin is the output of the error amplifier and a capacitor to GND compensates the error amplifier loop. Additionally, through the built-in offset on the PWM Comparator non-inverting input, the COMP pin provides the hiccup timing for the Overcurrent Protection, the Soft Start function that minimizes inrush currents during regulator power-up and switcher output enable.

## Startup

The CS51311 provides a controlled startup of regulator output voltage and features Programmable Soft Start implemented through the Error Amp and external Compensation Capacitor. This feature, combined with overcurrent protection, prevents stress to the regulator power components and overshoot of the output voltage during startup.

As power is applied to the regulator, the CS51311 Undervoltage Lockout circuit (UVL) monitors the IC's supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) which is typically connected to the +12 V output of the AC-DC power supply. The UVL circuit prevents the NFET gates from being activated until $\mathrm{V}_{\mathrm{CC}}$ exceeds the 8.4 V (typ) threshold. Hysteresis of 300 mV (typ) is provided for noise immunity. The Error Amp Capacitor connected to the COMP pin is charged by a $30 \mu \mathrm{~A}$ current source. This capacitor must be charged to 1.1 V (typ) so that it exceeds the PWM comparator's offset before the $\mathrm{V}^{2}$ PWM control loop permits switching to occur.

When $\mathrm{V}_{\mathrm{CC}}$ has exceeded 8.4 V and COMP has charged to 1.1 V, the upper Gate driver (GATE(H)) is activated, turning on the upper FET. This causes current to flow through the output inductor and into the output capacitors and load according to the following equation:

$$
I=\left(V_{I N}-V_{O U T}\right) \times \frac{T}{L}
$$

GATE(H) and the upper NFET remain on and inductor current ramps up until the initial pulse is terminated by either the PWM control loop or the overcurrent protection. This initial surge of in-rush current minimizes startup time, but avoids overstressing of the regulator's power components.

The PWM comparator will terminate the initial pulse if the regulator output exceeds the voltage on the COMP pin plus the 1.1 V PWM comparator offset prior to the drop across the current sense resistor exceeding the current limit threshold. In this case, the PWM control loop has achieved regulation and the initial pulse is then followed by a constant off time as programmed by the Coff capacitor. The COMP
capacitor will continue to slowly charge and the regulator output voltage will follow it, less the 1.1 V PWM offset, until it achieves the voltage programmed by the DAC's VID input. The Error Amp will then source or sink current to the COMP cap as required to maintain the correct regulator DC output voltage. Since the rate of increase of the COMP pin voltage is typically set much slower than the regulator's slew capability, inrush current, output voltage, and duty cycle all gradually increase from zero. (See Figures 9, 10, and 11).


Figure 9. Normal Startup ( $\mathbf{2 . 0} \mathbf{~ m s} / \mathrm{div}$ )


Channel 1 - Regulator Output Voltage ( $1.0 \mathrm{~V} /$ div)
Channel 2 - Inductor Switching Node (5.0 V/div)
Channel 3 - VCC ( $10 \mathrm{~V} /$ div)
Channel 4 - Regulator Input Voltage ( $5.0 \mathrm{~V} /$ div)
Figure 10. Normal Startup Showing Initial Pulse Followed by Soft Start (20 $\mu \mathrm{s} / \mathrm{div}$ )


Channel 1 - Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$ )
Channel 2 - Inductor Switching Node (5.0 V/div)
Channel 3 - V CC ( $10 \mathrm{~V} /$ div)
Channel 4 - Regulator Input Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$ )
Figure 11. Pulse-By-Pulse Regulation During Soft Start ( $2.0 \mu \mathrm{~s} / \mathrm{div}$ )

If the voltage across the Current Sense resistor generates a voltage difference between the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ pins that exceeds the OVC Comparator Offset Voltage ( 86 mV typical), the Fault latch is set. This causes the COMP pin to be quickly discharged, turning off GATE $(\mathrm{H})$ and the upper NFET since the voltage on the COMP pin is now less than the 1.1 V PWM comparator offset. The Fault latch is reset when the voltage on the COMP decreases below the discharge threshold voltage ( 0.25 V typical). The COMP capacitor will again begin to charge, and when it exceeds the 1.1 V PWM comparator offset, the regulator output will Soft Start normally (see Figure 12).


Figure 12. Startup with COMP Pre-Charge to 2.0 V ( $2.0 \mathrm{~ms} / \mathrm{div}$ )

Because the start-up circuit depends on the current sense function, a current sense resistor should always be used.

When driving large capacitive loads, the COMP must charge slowly enough to avoid tripping the CS51311 overcurrent protection. The following equation can be used to ensure unconditional startup:

$$
\frac{I_{\mathrm{CHG}}}{\mathrm{CCOMP}}<\frac{\mathrm{I}_{\mathrm{LIM}}-\mathrm{I}_{\mathrm{LOAD}}}{\mathrm{COUT}}
$$

where:
$\mathrm{I}_{\mathrm{CHG}}=$ COMP Source Current ( $30 \mu \mathrm{~A}$ typical);
$\mathrm{C}_{\text {COMP }}=$ COMP Capacitor value ( $0.1 \mu \mathrm{~F}$ typical);
$\mathrm{I}_{\text {LIM }}=$ Current Limit Threshold;
$\mathrm{I}_{\text {LOAD }}=$ Load Current during startup;
Cout $=$ Total Output Capacitance .

## Normal Operation

During normal operation, Switch Off-Time is constant and set by the C CofF capacitor. Switch On-Time is adjusted by the $\mathrm{V}^{2}$ Control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current and the ESR of the output capacitors

## Transient Response

The CS51311 V ${ }^{2}$ Control Loop's 200 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "Adaptive Voltage Positioning". This technique pre-positions the output capacitors voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifiers reference voltage to be targeted +25 mV high without compromising DC accuracy. A "Droop Resistor," implemented through a PC board trace, connects the Error Amps feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ) to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +25 mV offset. When the full load current is delivered, a 50 mV drop is developed across this resistor. This results in output voltage being offset -25 mV low.

The result of Adaptive Voltage Positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre-positioned +25 mV . Conversely, when load current suddenly decreases from its maximum level, the output capacitor is pre-positioned -25 mV . For
best Transient Response, a combination of a number of high frequency and bulk output capacitors are usually used.

## Slope Compensation

The $\mathrm{V}^{2}$ control method uses a ramp signal, generated by the ESR of the output capacitors, that is proportional to the ripple current through the inductor. To maintain regulation, the $\mathrm{V}^{2}$ control loop monitors this ramp signal, through the PWM comparator, and terminates the switch on-time.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope presented to the PWM comparator, due to the very low ESR, can lead to pulse width jitter and variation caused by both random or synchronous noise.

Adding slope compensation to the control loop, avoids erratic operation of the PWM circuit, particularly at lower duty cycles and higher frequencies, where there is not enough ramp signal, and provides a more stable switchpoint.

The scheme that prevents that switching noise prematurely triggers the PWM circuit consists of adding a positive voltage slope to the output of the Error Amplifier (COMP pin) during an off-time cycle.

The circuit that implements this function is shown in Figure 13.


Figure 13. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

The ramp waveform is generated through a small RC filter that provides the proper voltage ramp at the beginning of each on-time cycle. The resistors R1 and R2 in the circuit of Figure 13 form a voltage divider from the GATE(L) output, superimposing a small artificial ramp on the output of the error amplifier. It is important that the series combination $\mathrm{R} 1 / \mathrm{R} 2$ is high enough in resistance not to load down and negatively affect the slew rate on the GATE(L) pin.

## PROTECTION AND MONITORING FEATURES

## Overcurrent Protection

A loss-less hiccup mode current limit protection feature is provided, requiring only the COMP capacitor to implement. The CS51311 provides overcurrent protection by sensing the current through a "Droop" resistor, using an internal current sense comparator. The comparator
compares the voltage drop through the "Droop" resistor to an internal reference voltage of 86 mV (typical).

If the voltage drop across the "Droop" resistor exceeds this threshold, the current sense comparator allows the fault latch to be set. This causes the regulator to stop switching.

During this overcurrent condition, the CS51311 stays off for the time it takes the COMP pin capacitor to discharge to its lower 0.25 V threshold. As soon as the COMP pin reaches 0.25 V , the Fault latch is reset (no overcurrent condition present) and the COMP pin is charged with a $30 \mu \mathrm{~A}$ current source to a voltage 1.1 V greater than the $\mathrm{V}_{\mathrm{FB}}$ voltage. Only at this point the regulator attempts to restart normally by delivering short gate pulses to both FETS. The CS51311 will operate initially with a duty cycle whose value depends on how low the $\mathrm{V}_{\mathrm{FB}}$ voltage was during the overcurrent condition (whether hiccup mode was due to excessive current or hard short). This protection scheme minimizes thermal stress to the regulator components, input power supply, and PC board traces, as the overcurrent condition persists. Upon removal of the overload, the fault latch is cleared, allowing normal operation to resume.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns , causing the top MOSFET to shut off, disconnecting the regulator from its input voltage. This results in a "crowbar" action to clamp the output voltage and prevents damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.

## Power Good Circuit

The Power Good pin (pin 12) is an open-collector signal consistent with TTL DC specifications. It is externally pulled up, and is pulled low (below 0.3 V ) when the regulator output voltage typically exceeds $\pm 8.5 \%$ of the nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is $\pm 12 \%$.

## Output Enable

On/off control of the regulator outputs can be implemented by pulling the COMP pins low. It is required to pull the COMP pins below the 1.1 V PWM comparator offset voltage in order to disable switching on the GATE drivers.

## CS51311-BASED $\mathrm{V}_{\mathrm{CC}(\text { (CORE) }}$ BUCK REGULATOR DESIGN PROCEDURE

## Step 1: Definition of the Design Specifications

In computer motherboard applications the input voltage comes from the "silver box" power supply. $5.0 \mathrm{~V} \pm 5.0 \%$ is
used for conversion to output voltage, and $12 \mathrm{~V} \pm 5.0 \%$ is used for the external NFET gate voltage and circuit bias. The CPU V ${ }_{\text {CC(CORE) }}$ tolerance can be affected by any or all of the following reasons:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide a $\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}$ that will meet the specified tolerance at the CPU's inputs.

The designer must also ensure that the regulator component junction temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature. As computer motherboards become increasingly complex, regulator size also becomes important, as there is less space available for the CPU power supply.

## Step 2: Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I} \mathrm{OUT} \times\left(\frac{\mathrm{ESL}}{\Delta \mathrm{t}}+\mathrm{ESR}+\frac{\mathrm{tTR}}{\mathrm{COUT}}\right)
$$

where:
$\Delta \mathrm{I}_{\mathrm{OUT}} / \Delta \mathrm{t}=$ load current slew rate;
$\Delta \mathrm{I}_{\text {OUT }}=$ load transient;
$\Delta t=$ load transient duration time;
$\mathrm{ESL}=$ Maximum allowable ESL including capacitors, circuit traces, and vias;
$\mathrm{ESR}=$ Maximum allowable ESR including capacitors and circuit traces;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time.
The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike
depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESR}}}{\Delta \mathrm{I} \mathrm{OUT}}
$$

where $\Delta \mathrm{V}_{\mathrm{ESR}}=$ change in output voltage due to ESR (assigned by the designer).

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where:
$\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheet);
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR.
The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$
\Delta \mathrm{V}_{\mathrm{ESR}}=\Delta \mathrm{I} \text { OUT } \times \mathrm{ESR}_{\mathrm{MAX}}
$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$
\mathrm{ESLMAX}=\frac{\Delta \mathrm{V}_{\mathrm{ESL}} \times \Delta \mathrm{t}}{\Delta \mathrm{I}}
$$

where:
$\Delta \mathrm{I} / \Delta \mathrm{T}=$ load current slew rate (as high as $20 \mathrm{~A} / \mu \mathrm{s}$ );
$\Delta \mathrm{V}_{\mathrm{ESL}}=$ change in output voltage due to ESL.
The actual maximum allowable ESL can be determined by using the equation:

$$
\text { ESLMAX }=\frac{\text { ESLCAP }}{\text { Number of output capacitors }}
$$

where $\mathrm{ESL}_{\mathrm{CAP}}=$ maximum ESL per capacitor (it is estimated that a $10 \times 12 \mathrm{~mm}$ Aluminum Electrolytic capacitor has approximately 4.0 nH of package inductance).

The actual output voltage deviation due to the actual maximum ESL can then be verified:

$$
\Delta \mathrm{V}_{\mathrm{ESL}}=\frac{\mathrm{ESLMAX} \times \Delta \mathrm{I}}{\Delta \mathrm{t}}
$$

The designer now must determine the change in output voltage due to output capacitor discharge during the transient:

$$
\Delta \mathrm{V}_{\mathrm{CAP}}=\frac{\Delta \mathrm{l} \times \Delta \mathrm{t} \mathrm{TR}}{\mathrm{COUT}}
$$

where:
$\Delta \mathrm{t}_{\mathrm{TR}}=$ the output voltage transient response time (assigned by the designer);
$\Delta \mathrm{V}_{\mathrm{CAP}}=$ output voltage deviation due to output capacitor discharge;
$\Delta \mathrm{I}=$ Load step .

The total change in output voltage as a result of a load current transient can be verified by the following formula:

$$
\Delta \mathrm{V}_{\text {OUT }}=\Delta \mathrm{V}_{\mathrm{ESR}}+\Delta \mathrm{V}_{\mathrm{ESL}}+\Delta \mathrm{V}_{\mathrm{CAP}}
$$

## Step 3: Selection of the Duty Cycle, Switching Frequency, Switch On-Time (TON) and Switch Off-Time (TOfF)

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$
\text { Duty Cycle }=\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\left(\mathrm{V}_{\mathrm{HFET}}+\mathrm{V}_{\mathrm{L}}+\mathrm{V}_{\mathrm{DROOP}}\right)}{\mathrm{V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{LFET}}-\mathrm{V}_{\mathrm{HFET}}-\mathrm{V}_{\mathrm{L}}}
$$

where:
$\mathrm{V}_{\text {OUT }}=$ buck regulator output voltage;
$\mathrm{V}_{\text {HFET }}=$ high side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$;
$\mathrm{V}_{\mathrm{L}}=$ output inductor voltage drop due to inductor wire DC resistance;
$\mathrm{V}_{\text {DROOP }}=$ droop (current sense) resistor voltage drop;
$\mathrm{V}_{\mathrm{IN}}=$ buck regulator input voltage;
$\mathrm{V}_{\mathrm{LFET}}=$ low side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$.

## Step3a: Calculation of Switch On-Time

The Switch On-Time (time during which the switching MOSFET in a synchronous buck topology is conducting) is determined by:

$$
\text { TON }=\frac{\text { Duty Cycle }}{\text { FSW }}
$$

where $\mathrm{F}_{\mathrm{SW}}=$ regulator switching frequency selected by the designer.

Higher operating frequencies allow the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

## Step 3b: Calculation of Switch Off-Time

The Switch Off-Time (time during which the switching MOSFET is not conducting) can be determined by:

$$
\text { TOFF }=\frac{1.0}{\text { FSW }}-\mathrm{TON}
$$

The $\mathrm{C}_{\mathrm{OFF}}$ capacitor value has to be selected in order to set the Off-Time, $\mathrm{T}_{\text {OfF }}$, above:

$$
\text { COFF }=\frac{\text { Period } \times(1.0-\mathrm{D})}{3980}
$$

where:
3980 is a characteristic factor of the CS51311;
D = Duty Cycle.

## Step 4: Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but
degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due to their high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The inductor value can be determined by:

$$
\mathrm{L}=\frac{\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{t} \mathrm{TR}}{\Delta \mathrm{I}}
$$

where:
$\mathrm{V}_{\text {IN }}=$ input voltage;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time (assigned by the designer);
$\Delta \mathrm{I}=$ load transient.
The inductor ripple current can then be determined:

$$
\Delta \mathrm{I}_{\mathrm{L}}=\frac{\mathrm{V}_{\mathrm{OUT}} \times \mathrm{T}_{\mathrm{OFF}}}{\mathrm{~L}}
$$

where:
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{T}_{\mathrm{OFF}}=$ switch Off-Time;
$\mathrm{L}=$ inductor value.
The designer can now verify if the number of output capacitors from Step 2 will provide an acceptable output voltage ripple ( $1.0 \%$ of output voltage is common). The formula below is used:

$$
\Delta \mathrm{I}_{\mathrm{L}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\mathrm{ESR} \mathrm{MAX}^{2}}
$$

Rearranging we have:

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{l}}
$$

where
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR ;
$\Delta \mathrm{V}_{\text {OUT }}=1.0 \% \times \mathrm{V}_{\text {OUT }}=$ maximum allowable output voltage ripple ( budgeted by the designer );
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage .
The number of output capacitors is determined by:

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where $\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$
\mathrm{I}(\mathrm{PEAK})=\mathrm{IOUT}+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2.0}
$$

where:
$\mathrm{I}_{\mathrm{L}(\text { PEAK })}=$ inductor peak current;
I OUT $=$ load current;
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current.

$$
\mathrm{IL}(\mathrm{VALLEY})=\mathrm{IOUT}-\frac{\Delta \mathrm{I}}{2.0}
$$

where $\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current.
Given the requirements of an application such as a buck converter, it is found that a toroid powdered iron core is quite suitable due to its low cost, low core losses at the switching frequency, and low EMI.

## Step 5: Selection of the Input Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines. A key specification for input capacitors is their ripple current rating. The input capacitor should also be able to handle the input RMS current $\mathrm{I}_{\text {IN(RMS) }}$.

The combination of the input capacitors $\mathrm{C}_{\mathrm{IN}}$ discharges during the on-time.

The input capacitor discharge current is given by:
ICINDIS(RMS) $=$

$$
\sqrt{\frac{\left(\begin{array}{l}
\mathrm{IL}(\mathrm{PEAK})^{2} \\
+(\mathrm{IL}(\mathrm{PEAK}) \times \mathrm{L}(\mathrm{VALLEY})) \\
+\mathrm{IL}(\mathrm{VALLEY})^{2}
\end{array}\right.}{3.0}}
$$

where:
$\mathrm{I}_{\mathrm{CINDIS}(\mathrm{RMS})}=$ input capacitor discharge current;
$\mathrm{I}_{\mathrm{L}(\text { PEAK })}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current.
$\mathrm{C}_{\mathrm{IN}}$ charges during the off-time, the average current through the capacitor over one switching cycle is zero:

$$
\operatorname{ICIN}(C H)=\operatorname{ICIN}(D I S) \times \frac{D}{1.0-D}
$$

where:
$\mathrm{I}_{\mathrm{CIN}(\mathrm{CH})}=$ input capacitor charge current;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{DIS})}=$ input capacitor discharge current;
D = Duty Cycle .
The total Input RMS current is:

$$
\mathrm{I} \mathrm{CIN}(\mathrm{RMS})=\sqrt{\begin{array}{l}
\left(\mathrm{I} \mathrm{CIN}(\mathrm{DIS})^{2} \times \mathrm{D}\right) \\
+\left(\operatorname{ICIN}(\mathrm{CH})^{2} \times(1.0-\mathrm{D})\right)
\end{array}}
$$

The number of input capacitors required is then determined by:

$$
N_{\mathrm{CIN}}=\frac{\mathrm{I} \mathrm{I} \operatorname{IN}(\mathrm{RMS})}{\mathrm{I}_{\mathrm{RIPPLE}}}
$$

where:
$\mathrm{N}_{\mathrm{CIN}}=$ number of input capacitors;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{I}_{\text {RIPPLE }}=$ input capacitor ripple current rating (specified in manufacturer's data sheets).

The total input capacitor ESR needs to be determined in order to calculate the power dissipation of the input capacitors:

$$
\mathrm{ESR}_{\mathrm{CIN}}=\frac{\mathrm{ESR} \mathrm{CAP}}{\mathrm{~N}_{\mathrm{CIN}}}
$$

where:
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR;
$\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheets);
$\mathrm{N}_{\mathrm{CIN}}=$ number of input capacitors.
Once the total ESR of the input capacitors is known, the input capacitor ripple voltage can be determined using the formula:

$$
\mathrm{V}_{\mathrm{CIN}(\mathrm{RMS})}=\operatorname{I} \mathrm{CIN}(\mathrm{RMS}) \times \mathrm{ESR}_{\mathrm{CIN}}
$$

where:
$\mathrm{V}_{\mathrm{CIN}(\mathrm{RMS})}=$ input capacitor RMS voltage;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR.
The designer must determine the input capacitor power loss in order to ensure there isn't excessive power dissipation through these components. The following formula is used:

$$
\operatorname{PCIN}(\mathrm{RMS})=\operatorname{ICIN}(\mathrm{RMS})^{2} \times \mathrm{ESR}_{\mathrm{CIN}}
$$

where:
$\mathrm{P}_{\mathrm{CIN}(\mathrm{RMS})}=$ input capacitor RMS power dissipation;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR .

## Step 6: Selection of the Input Inductor

A CPU switching regulator, such as the one in a buck topology, must not disturb the primary +5.0 V supply. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the +5.0 V supply from the noise generated in the switching portion of the microprocessor buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the CPU load changes from no load to full load (load step), a condition under which the highest voltage change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input
bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$
\mathrm{LIN}=\frac{\Delta \mathrm{V}}{(\mathrm{dl} / \mathrm{dt}) \mathrm{MAX}}
$$

where:
$\mathrm{L}_{\mathrm{IN}}=$ input inductor value;
$\Delta \mathrm{V}=$ voltage seen by the input inductor during a full load swing;
$(\mathrm{dI} / \mathrm{dt})_{\text {MAX }}=$ maximum allowable input current slew rate ( $0.1 \mathrm{~A} / \mu$ s for a Pentium II power supply).

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2 , a roll-off rate of $-40 \mathrm{~dB} / \mathrm{dec}$, and a corner frequency:

$$
\mathrm{f}_{\mathrm{C}}=\frac{1.0}{2.0 \pi \sqrt{\mathrm{LC}}}
$$

where:
$\mathrm{L}=$ input inductor;
$\mathrm{C}=$ input capacitor(s).

## Step 7: Selection of the Switching FET FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) Its very high input impedance; and 2) Its very fast switching times. The electrical characteristics of a MOSFET are considered to be those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of $\mathrm{V}_{\mathrm{GS}}$, and the faster the turn-on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn-on switching losses, 4) turn-off switching losses, and 5) gate-transitions losses. The latter three losses are proportional to frequency. For the conducting power dissipation rms values of current and resistance are used for true power calculations. The fast switching speed of the MOSFET makes it indispensable for high-frequency power supply applications. Not only are switching power losses minimized, but also the maximum usable switching frequency is considerably higher. Switching time is independent of temperature. Also, at higher frequencies, the use of smaller and lighter components (transformer, filter choke, filter capacitor) reduces overall component cost while using less space for more efficient packaging at lower weight.

The MOSFET has purely capacitive input impedance. No DC current is required. It is important to keep in mind the drain current of the FET has a negative temperature coefficient. Increase in temperature causes higher on-resistance and greater leakage current. For switching
circuits, $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}$ should be low to minimize power dissipation at a given ID, and $\mathrm{V}_{\mathrm{GS}}$ should be high to accomplish this. MOSFET switching times are determined by device capacitance, stray capacitance, and the impedance of the gate drive circuit. Thus the gate driving circuit must have high momentary peak current sourcing and sinking capability for switching the MOSFET. The input capacitance, output capacitance and reverse-transfer capacitance also increase with increased device current rating.

Two considerations complicate the task of estimating switching times. First, since the magnitude of the input capacitance, $\mathrm{C}_{\text {ISS }}$, varies with $\mathrm{V}_{\mathrm{DS}}$, the RC time constant determined by the gate-drive impedance and $\mathrm{C}_{\text {ISS }}$ changes during the switching cycle. Consequently, computation of the rise time of the gate voltage by using a specific gate-drive impedance and input capacitance yields only a rough estimate. The second consideration is the effect of the "Miller" capacitance, $\mathrm{C}_{\text {RSS }}$, which is referred to as $\mathrm{C}_{\mathrm{DG}}$ in the following discussion. For example, when a device is on, $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}$ is fairly small and $\mathrm{V}_{\mathrm{GS}}$ is about $12 \mathrm{~V} . \mathrm{C}_{\mathrm{DG}}$ is charged to $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}-\mathrm{V}_{\mathrm{GS}}$, which is a negative potential if the drain is considered the positive electrode. When the drain is "off", $\mathrm{C}_{\mathrm{DG}}$ is charged to quite a different potential. In this case the voltage across $C_{D G}$ is a positive value since the potential from gate-to-source is near zero volts and $\mathrm{V}_{\mathrm{DS}}$ is essentially the drain supply voltage. During turn-on and turn-off, these large swings in gate-to-drain voltage tax the current sourcing and sinking capabilities of the gate drive. In addition to charging and discharging $\mathrm{C}_{\mathrm{GS}}$, the gate drive must also supply the displacement current required by $C_{D G}\left(I_{\mathrm{GATE}}=C_{\mathrm{DG}} \mathrm{dV}_{\mathrm{DG}} / \mathrm{dt}\right)$. Unless the gate-drive impedance is very low, the $\mathrm{V}_{\mathrm{GS}}$ waveform commonly plateaus during rapid changes in the drain-to-source voltage.

The most important aspect of FET performance is the Static Drain-To-Source On-Resistance ( $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ ), which effects regulator efficiency and FET thermal management requirements. The On-Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On-Resistance also increases. Its positive temperature coefficient is between $+0.6 \% / \mathrm{C}$ and $+0.85 \% / \mathrm{C}$. The higher the On-Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used. The reference designs derive gate drive from the 12 V supply, which is generally available in most computer systems and utilizes logic level FETs.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias
supplies when in the high state. In practice, the FET gates will be driven rail-to-rail due to overshoot caused by the capacitive load they present to the controller IC.

## Step 7a: Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed $150^{\circ} \mathrm{C}$.

The maximum RMS current through the switch can be determined by the following formula:
IRMS(H) =

where:
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{I}_{\mathrm{L}(\text { PEAK })}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\mathrm{VALLEY})}=$ inductor valley current;
D = Duty Cycle.
Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$
\operatorname{PRMS}(\mathrm{H})=\operatorname{IRMS}(\mathrm{H})^{2} \times \operatorname{RDS}(\mathrm{ON})
$$

where:
$\mathrm{P}_{\mathrm{RMS}(\mathrm{H})}=$ switching MOSFET conduction losses;
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=\mathrm{FET}$ drain-to-source on-resistance
The upper MOSFET switching losses are caused during MOSFET switch-on and switch-off and can be determined by using the following formula:

$$
\begin{aligned}
\mathrm{PSWH} & =\mathrm{PSWH}_{\text {SWN }}(\mathrm{ON}+\mathrm{PSWH}(\mathrm{OFF}) \\
& =\frac{\mathrm{V}_{\mathrm{IN}} \times \mathrm{IOUT} \times(\mathrm{tRISE}+\mathrm{tFALL})}{6.0 \mathrm{~T}}
\end{aligned}
$$

where:
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses;
$\mathrm{V}_{\text {IN }}=$ input voltage;
IOUT $=$ load current;
$\mathrm{t}_{\text {RISE }}=$ MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{t}_{\mathrm{FALL}}=$ MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{T}=1 / \mathrm{F}_{\mathrm{SW}}=$ period.
The total power dissipation in the switching MOSFET can then be calculated as:
PHFET $($ TOTAL $)=$ PRMSH $+\operatorname{PSWH}(O N)+\operatorname{PSWH}(O F F)$
where:
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) MOSFET losses;
$\mathrm{P}_{\text {RMSH }}=$ upper MOSFET switch conduction Losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses.
Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$
T_{J}=T_{A}+\left(P_{H F E T}(T O T A L) \times R_{\theta J A}\right)
$$

where:
$\mathrm{T}_{\mathrm{J}}=\mathrm{FET}$ junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) FET losses;
$\mathrm{R}_{\theta \mathrm{JA}}=$ upper FET junction-to-ambient thermal resistance.

## Step 7b: Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$
\begin{aligned}
\mathrm{PRMSL} & =\mathrm{IRMS}^{2} \times \operatorname{RDS}(\mathrm{ON}) \\
& =(\mathrm{IOUT} \times \sqrt{(1.0-\mathrm{D})})^{2} \times \operatorname{RDS}(\mathrm{ON})
\end{aligned}
$$

where:
$\mathrm{P}_{\text {RMSL }}=$ lower MOSFET conduction losses;
IOUT = load current;
D = Duty Cycle;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=$ lower FET drain-to-source on-resistance.
The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non-overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$
P_{S W L}=V_{S D} \times I_{\text {LOAD }} \times \text { non-overlap time } \times \mathrm{F}_{S W}
$$

where:
$\mathrm{P}_{\text {SWL }}=$ lower FET switching losses;
$\mathrm{V}_{\mathrm{SD}}=$ lower FET source-to-drain voltage;
$\mathrm{I}_{\text {LOAD }}=$ load current
Non-overlap time $=\operatorname{GATE}(\mathrm{L})-$ to-GATE(H) or GATE(H)-to-GATE(L) delay (from CS51311 data sheet Electrical Characteristics section);
$\mathrm{F}_{\text {SW }}=$ switching frequency.
The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$
\text { PLFET }(\text { TOTAL })=\text { PRMSL }+ \text { PSWL }
$$

where:
$\mathrm{P}_{\text {LFET(TOTAL) }}=$ Synchronous (lower) FET total losses;
$P_{\text {RMSL }}=$ Switch Conduction Losses;
$\mathrm{P}_{\text {SWL }}=$ Switching losses.
Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$
T_{J}=T_{A}+\left(\text { PLFET }(T O T A L) \times R_{\theta J A}\right)
$$

where:
$\mathrm{T}_{\mathrm{J}}=$ MOSFET junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\left.\mathrm{P}_{\text {LFET }(\text { TOTAL }}\right)=$ total synchronous (lower) FET losses;
$\mathrm{R}_{\text {OJA }}=$ lower FET junction-to-ambient thermal resistance.

## Step 8: Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, $\mathrm{V}_{\mathrm{CC}}$, and the CS51311 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:
PCONTROLIC $=I_{C C} V_{C C}+\operatorname{PGATE}(H)+\operatorname{PGATE}(L)$
where:
$\mathrm{P}_{\text {CONTROLIC }}=$ control IC power dissipation;
$\mathrm{I}_{\mathrm{CC}}=\mathrm{IC}$ quiescent supply current;
$\mathrm{V}_{\mathrm{CC}}=\mathrm{IC}$ supply voltage;
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{P}_{\text {GATE }(\mathrm{L})}=$ lower MOSFET gate driver (IC) losses.
The upper (switching) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{H})=\operatorname{QGATE}_{(H)} \times \operatorname{FSW} \times \operatorname{VGATE}(\mathrm{H})
$$

where:
$\mathrm{P}_{\text {GATE(H) }}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{H})}=$ total upper MOSFET gate charge;
$\mathrm{F}_{\mathrm{SW}}=$ switching frequency;
$\mathrm{V}_{\text {GATE(H) }}=$ upper MOSFET gate voltage.
The lower (synchronous) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{L})=\text { QGATE }^{\text {GL }} \mathbf{L} \times \text { FSW } \times \mathrm{V}_{\text {GATE }}(\mathrm{L})
$$

where:
$\mathrm{P}_{\text {GATE(L) }}=$ lower MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{L})}=$ total lower MOSFET gate charge;
$\mathrm{F}_{\text {SW }}=$ switching frequency;
$\mathrm{V}_{\text {GATE(L) }}=$ lower MOSFET gate voltage.
The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

## Step 9: Slope Compensation

Voltage regulators for today's advanced processors are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR at the CPU input supply pins. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that there's very little voltage ramp at the control IC feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ) and regulator sensitivity to noise and loop instability are two undesirable effects that can surface. The performance of the CS51311-based CPU $\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}$ regulator is improved when a fixed amount of slope compensation is added to the output of the PWM Error Amplifier (COMP pin) during the regulator Off-Time. Referring to Figure 13, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1 and R2.
$\mathrm{V}_{\text {SLOPECOMP }}=\mathrm{V}_{\text {GATE }}(\mathrm{L}) \times\left(\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}\right) \times\left(1.0-\mathrm{e}^{\frac{-\mathrm{t}}{\tau}}\right)$
where:
$\mathrm{V}_{\text {SLOPECOMP }}=$ amount of slope added;
$\mathrm{V}_{\text {GATE(L) }}=$ lower MOSFET gate voltage;
$\mathrm{R} 1, \mathrm{R} 2=$ voltage divider resistors;
$\mathrm{t}=\mathrm{t}_{\text {OFF }}$ (switch off-time);
$\tau=\mathrm{RC}$ constant determined by C 1 and the parallel combination of R1, R2 (Figure 13), neglecting the low driver output impedance

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off-time cycle duration (time during which the lower MOSFET is conducting).

## Step 10: Selection of Current Limit Filter Components

The current limit filter is implemented by a $0.1 \mu \mathrm{~F}$ ceramic capacitor across and two $510 \Omega$ resistors in series with the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ current limit comparator input pins. They provide a time constant $\tau=\mathrm{RC}=100 \mu \mathrm{~s}$, which enables the circuit to filter out noise and be immune to false triggering, caused by sudden and fast load changes. These load transients can have slew rates as high as $20 \mathrm{~A} / \mu \mathrm{s}$.

## "DROOP" RESISTOR FOR ADAPTIVE VOLTAGE POSITIONING AND CURRENT LIMIT

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met. An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation caused by variation in the thickness of the PCB layer; 2) the mismatch of $\mathrm{L} / \mathrm{W}$; and 3) temperature variation.

## 1) Sheet Resistivity

For one ounce copper, the thickness variation is typically 1.26 mil to 1.48 mil . Therefore the error due to sheet resistivity is:

$$
\frac{1.48-1.26}{1.37}= \pm 8.0 \%
$$

## 2) Mismatch Due to L/W

The variation in $\mathrm{L} / \mathrm{W}$ is governed by variations due to the PCB manufacturing process. The error due to L/W mismatch is typically $1.0 \%$.

## 3) Thermal Considerations

Due to $\mathrm{I}^{2} \times \mathrm{R}$ power losses the surface temperature of the droop resistor will increase causing the resistance to increase. Also, the ambient temperature variation will
contribute to the increase of the resistance, according to the formula:

$$
R=R_{20}\left[1.0+\alpha_{20}(T-20)\right]
$$

where:
$\mathrm{R}_{20}=$ resistance at $20^{\circ} \mathrm{C}$;
$\alpha=0.00393 /{ }^{\circ} \mathrm{C}$
$\mathrm{T}=$ operating temperature;
$\mathrm{R}=$ desired droop resistor value.
For temperature $\mathrm{T}=50^{\circ} \mathrm{C}$, the $\% \mathrm{R}$ change $=12 \%$.

## Droop Resistor Tolerance

Tolerance due to sheet resistivity variation $\pm 8.0 \%$
Tolerance due to L/W error $1.0 \%$
Tolerance due to temperature variation $12 \%$
Total tolerance for droop resistor $21 \%$
In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage at full load is above the minimum DC tolerance spec:

$$
\mathrm{V}_{\mathrm{DROOP}(\mathrm{TYP})}=\frac{\mathrm{V}_{\mathrm{DAC}(\mathrm{MIN})}-\mathrm{V}_{\mathrm{DC}}(\mathrm{MIN})}{1.0+\mathrm{R}_{\mathrm{DROOP}}(\text { TOLERANCE })}
$$

Example: for a 450 MHz Pentium II, the DC accuracy spec is $1.93<\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}<2.07 \mathrm{~V}$, and the AC accuracy spec is $1.9 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}<2.1 \mathrm{~V}$. The CS51311 DAC output voltage is $+2.001 \mathrm{~V}<\mathrm{V}_{\mathrm{DAC}}<+2.049 \mathrm{~V}$. In order not to exceed the DC accuracy spec, the voltage drop developed across the resistor must be calculated as follows:

$$
\begin{aligned}
\mathrm{VDROOP}_{\mathrm{DR}}(\mathrm{TYP}) & =\frac{\left(\mathrm{V}_{\mathrm{DAC}}(\mathrm{MIN})-\mathrm{V}_{\mathrm{DC}}(\mathrm{MIN})\right)}{1.0+\mathrm{R}_{\mathrm{DROOP}}(\mathrm{TOLERANCE})} \\
& =\frac{+2.001 \mathrm{~V}-1.93 \mathrm{~V}}{1.21}=71 \mathrm{mV}
\end{aligned}
$$

With the CS51311 DAC accuracy being $1.0 \%$, the internal error amplifier's reference voltage is trimmed so that the output voltage will be 25 mV high at no load. With no load, there is no DC drop across the resistor, producing an output voltage tracking the error amplifier output voltage, including the offset. When the full load current is delivered, a drop of -50 mV is developed across the resistor. Therefore, the regulator output is pre-positioned at 25 mV above the nominal output voltage before a load turn-on. The total voltage drop due to a load step is $\Delta \mathrm{V}-25 \mathrm{mV}$ and the deviation from the nominal output voltage is 25 mV smaller than it would be if there was no droop resistor. Similarly at full load the regulator output is pre-positioned at 25 mV below the nominal voltage before a load turn-off. the total voltage increase due to a load turn-off is $\Delta \mathrm{V}-25 \mathrm{mV}$ and the deviation from the nominal output voltage is 25 mV smaller than it would be if there was no droop resistor. This is because the output capacitors are pre-charged to a value that is either 25 mV above the nominal output voltage before a load turn-on or, 25 mV below the nominal output voltage before a load turn-off .

Obviously, the larger the voltage drop across the droop resistor (the larger the resistance), the worse the DC and load regulation, but the better the AC transient response.

## Current Limit

The current limit setpoint has to be higher than the normal full load current. Attention has to be paid to the current rating of the external power components as these are the first to fail during an overload condition. The MOSFET continuous and pulsed drain current rating at a given case temperature has to be accounted for when setting the current limit trip point.
Temperature curves on MOSFET manufacturers' data sheets allow the designer to determine the MOSFET drain current at a particular VGS and TJ (junction temperature). This, in turn, will assist the designer to set a proper current limit, without causing device breakdown during an overload condition.
Let's assume the full CPU load is 16 A . The internal current sense comparator current limit voltage limits are: $77 \mathrm{mV}<\mathrm{V}_{\mathrm{TH}}<101 \mathrm{mV}$. Also, there is a $21 \%$ total variation in $\mathrm{R}_{\text {SENSE }}$ as discussed in the previous section.
We compute the value of the current sensing element (embedded PCB trace) for the minimum current limit setpoint:

$$
\begin{gathered}
\operatorname{RSENSE}(\mathrm{MIN})=\operatorname{RSENSE}(\mathrm{TYP}) \times 0.79 \\
\operatorname{RSENSE}(\mathrm{MAX})=\operatorname{RSENSE}(\mathrm{TYP}) \times 1.21 \\
\operatorname{RSENSE}(\mathrm{MAX})=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{MIN})}^{\mathrm{I}(\mathrm{MIN})}=\frac{77 \mathrm{mV}}{16 \mathrm{~A}}=4.8 \mathrm{~m} \Omega}{}
\end{gathered}
$$

We select,

$$
\text { RSENSE(TYP) }=3.3 \mathrm{~m} \Omega
$$

We calculate the range of load currents that will cause the internal current sense comparator to detect an overload condition.

## Nominal Current Limit Setpoint

From the overcurrent detection data in the electrical characteristics table:

$$
\begin{gathered}
\mathrm{V}_{\mathrm{TH}(\mathrm{TYP})}=86 \mathrm{mV} \\
\mathrm{ICL}(\mathrm{NOM})=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{TYP})}}{\operatorname{RSENSE}(\mathrm{NOM})}=\frac{86 \mathrm{mV}}{3.3 \mathrm{~m} \Omega}=26 \mathrm{~A}
\end{gathered}
$$

## Maximum Current Limit Setpoint

From the overcurrent detection data in the electrical characteristics table:

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{TH}}(\mathrm{MAX})=101 \mathrm{mV} \\
& \mathrm{I}_{\mathrm{CL}(\mathrm{MAX})}= \frac{\mathrm{V}_{\mathrm{TH}(\mathrm{MAX})}}{\operatorname{RSENSE}(\mathrm{MIN})}=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{MAX})}}{\operatorname{RSENSE}(\mathrm{NOM}) \times 0.79} \\
&=\frac{101 \mathrm{mV}}{3.3 \mathrm{~m} \Omega \times 0.79}=38.7 \mathrm{~A}
\end{aligned}
$$

Therefore, the range of load currents that will cause the internal current sense comparator to detect an overload condition through a $3.3 \mathrm{~m} \Omega$ embedded PCB trace is: 19.3 A $<\mathrm{I}_{\mathrm{CL}}<38.7 \mathrm{~A}$, with 26 A being the nominal overload condition.

## Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$
R_{A R}=\rho \times \frac{L}{A} \text { or } R=\rho \times \frac{L}{(W \times t)}
$$

where:
$\mathrm{A}=\mathrm{W} \times \mathrm{t}=$ cross-sectional area;
$\rho=$ the copper resistivity ( $\mu \Omega$-mil);
$\mathrm{L}=$ length (mils);
$\mathrm{W}=$ width (mils);
$\mathrm{t}=$ thickness (mils).
For most PCBs the copper thickness, t , is $35 \mu \mathrm{~m}$ (1.37 mils) for one ounce copper; $\rho=717.86 \mu \Omega-$ mil.

For a CPU load of 16 A the resistance needed to create a 50 mV drop at full load is:

$$
\text { RDROOP }=\frac{50 \mathrm{mV}}{\mathrm{IOUT}}=\frac{50 \mathrm{mV}}{16 \mathrm{~A}}=3.1 \mathrm{~m} \Omega
$$

The resistivity of the copper will drift with the temperature according to the following guidelines:

$$
\begin{aligned}
& \Delta R=12 \% @ T_{A}=+50^{\circ} \mathrm{C} \\
& \Delta R=34 \% @ T_{A}=+100^{\circ} \mathrm{C}
\end{aligned}
$$

## Droop Resistor Length, Width, and Thickness

The minimum width and thickness of the droop resistor should primarily be determined on the basis of the current-carrying capacity required, and the maximum permissible droop resistor temperature rise. PCB manufacturer design charts can be used in determining current-carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.

For single conductor applications, such as the use of the droop resistor, PCB design charts show that for a droop resistor with a required current-carrying capacity of 16 A , and a $45^{\circ} \mathrm{C}$ temperature rise above ambient, the recommended cross section is $275 \mathrm{mil}^{2}$.

$$
\mathrm{W} \times \mathrm{t}=275 \mathrm{mil}{ }^{2}
$$

where:
$\mathrm{W}=$ droop resistor width;
$\mathrm{t}=$ droop resistor thickness.
For 1 oz . copper, $\mathrm{t}=1.37 \mathrm{mils}$, therefore $\mathrm{W}=201 \mathrm{mils}=$ 0.201 in.

$$
R=\rho \times \frac{L}{W \times t}
$$

where:
$\mathrm{R}=$ droop resistor value;
$\rho=0.71786 \mathrm{~m} \Omega-\mathrm{mil}$ ( 1 oz. copper);
$\mathrm{L}=$ droop resistor length;
$\mathrm{W}=$ droop resistor width.

$$
\begin{gathered}
\text { RDROOP }=3.3 \mathrm{~m} \Omega \\
3.3 \mathrm{~m} \Omega=0.71786 \mathrm{~m} \Omega-\mathrm{mil} \times \frac{\mathrm{L}}{201 \mathrm{mils} \times 1.37 \mathrm{mils}}
\end{gathered}
$$

Hence, $\mathrm{L}=1265$ mils $=1.265$ in.
In layouts where it is impractical to lay out a droop resistor in a straight line 1265 mils long, the embedded PCB trace can be "snaked" to fit within the available space.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$
\text { Thermal Impedance }=\frac{T_{J}(\mathrm{MAX})-\mathrm{T}_{\mathrm{A}}}{\text { Power }}
$$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

## LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS51311.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double-sided PCBs a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCBs are usually sufficient for a good layout, four-layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layer for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be as short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}$ filter resistors $(510 \Omega)$ in series with the $V_{\text {FB }}$ and $V_{\text {OUT }}$ pins as close as possible to the pins.
12. Place the Coff and COMP capacitors as close as possible to the $\mathrm{C}_{\mathrm{OFF}}$ and COMP pins.
13. Place the current limit filter capacitor between the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ pins, as close as possible to the pins.
14. Connect the filter components of the following pins: $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}, \mathrm{C}_{\mathrm{OFF}}$, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
15. The "Droop" Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
16. Place the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor as close as possible to the IC.

PACKAGE THERMAL DATA

| Parameter |  | SO-14 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 30 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 125 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## Synchronous Rectification DC/DC Converter Programmable Integrated Controller

The MC33470 is a digitally programmable switching voltage regulator, specifically designed for Microprocessor supply, Voltage Regulator Module and general purpose applications, to provide a high power regulated output voltage using a minimum of external parts. A 5-bit digital-to-analog converter defines the dc output voltage.

This product has three additional features. The first is a pair of high speed comparators which monitor the output voltage and expedite the circuit response to load current changes. The second feature is a soft start circuit which establishes a controlled response when input power is applied and when recovering from external circuit fault conditions. The third feature is two output drivers which provide synchronous rectification for optimum efficiency.

This product is ideally suited for computer, consumer, and industrial equipment where accuracy, efficiency and optimum regulation performance is desirable.

MC33470 Features:

- 5-Bit Digital-to-Analog Converter Allows Digital Control of Output Voltage
- High Speed Response to Transient Load Conditions
- Output Enable Pin Provides On/Off Control
- Programmable Soft Start Control
- High Current Output Drives for Synchronous Rectification
- Internally Trimmed Reference with Low Temperature Coefficient
- Programmable Overcurrent Protection
- Overvoltage Fault Indication
- Functionally Similar to the LTC1553

MC33470

## SYNCHRONOUS RECTIFICATION DC/DC CONVERTER PROGRAMMABLE INTEGRATED CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

20


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| MC 33470 DW | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+75^{\circ} \mathrm{C}$ | $\mathrm{SO}-20 \mathrm{~L}$ |

## Simplified Block Diagram



MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 7.0 | V |
| Output Driver Supply Voltage (Operating) | $\mathrm{P}_{\mathrm{V}_{\mathrm{CC}}}$ | 18 | V |
| $I_{\text {max }}, I_{\text {fb }}$ Inputs | $\mathrm{V}_{\text {in }}$ | -0.3 to 18 | V |
| All Other Inputs and Digital (OT, Fault, Power Good) Outputs | $\mathrm{V}_{\text {in }}$ | $\begin{gathered} -0.3 \text { to } \\ v_{C C}+0.3 \end{gathered}$ | V |
| Power Dissipation and Thermal Characteristics Maximum Power Dissipation Case 751D DW Suffix ( $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ ) Thermal Resistance Junction-to-Ambient Thermal Resistance Junction-to-Case | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | $\begin{gathered} 0.60 \\ 91 \\ 60 \end{gathered}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Notes 1 and 2) | $\mathrm{T}_{\mathrm{A}}$ | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{P}_{\mathrm{V}_{\mathrm{CC}}}=12 \mathrm{~V}\right.$ for typical values $\mathrm{T}_{\mathrm{A}}=$ Low to High [Notes 1, 2, 3], for $\mathrm{min} / \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR |  |  |  |  |  |
| Frequency ( $\mathrm{V}_{\mathrm{CC}}=4.5$ to 5.5 V ) | $\mathrm{f}_{\text {osc }}$ | 210 | 300 | 390 | kHz |
| FEEDBACK AMPLIFIER |  |  |  |  |  |
| Voltage Feedback Input Threshold (Note 4) VIDO, VID1, VID2 and VID4 $=$ " 1 " and VID3 $=$ " 0 " VID4 $=$ " 1 " and VID0, VID1, VID2 and VID3 $=$ " 0 " | $\mathrm{V}_{\text {sense }}$ | $\begin{gathered} \hline 1.764 \\ 2.744 \\ 3.43 \end{gathered}$ | $\begin{aligned} & 1.8 \\ & 2.8 \\ & 3.5 \end{aligned}$ | $\begin{gathered} 1.836 \\ 2.856 \\ 3.57 \end{gathered}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \end{aligned}$ |
| Input Bias Current ( $\mathrm{V}_{\mathrm{CM}}=2.8 \mathrm{~V}$ ) | IB | - | 20 | - | $\mu \mathrm{A}$ |
| Transconductance ( $\left.\mathrm{V}_{\mathrm{CM}}=2.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{COMP}}=2.0 \mathrm{~V}\right)$ | $\mathrm{G}_{\mathrm{M}}$ | 400 | 800 | 1200 | $\mu \mathrm{mho}$ |
| Open Loop Voltage Gain ( $\mathrm{V}_{\text {COMP }}=2.0 \mathrm{~V}$ ) | Avol | - | 67 | - | dB |
| Output Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=4.5$ to 5.5 V ) | Regline | - | 7.0 | - | mV |
| Output Load Regulation | Regload | - | 5.0 | - | mV |
| Output Current Source Sink | $\begin{aligned} & \mathrm{I}_{\mathrm{OH}} \\ & \mathrm{I}_{\mathrm{OL}} \\ & \hline \end{aligned}$ | - | $\begin{aligned} & 120 \\ & 120 \end{aligned}$ | - | $\mu \mathrm{A}$ |

PWM SECTION

| Duty Cycle at G1 Output <br> Maximum <br> Minimum | $\mathrm{DC}_{\max }$ | 77 | 88 | 95 | $\%$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay | DC min | - | - | 0 |  |
| Comp Input to G1 Output, $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ |  |  |  |  | $\mu \mathrm{s}$ |
| Comp Input to G2 Output, $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ | $\mathrm{t}_{\text {PLH } 1}$ | - | 0.1 | - |  |

## SOFT-START SECTION

| Charge Current ( $\mathrm{V}_{\text {Soft-Start }}=0 \mathrm{~V}$ ) | $I_{\text {chg }}$ | 7.0 | 10 | 13 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Discharge Current under Current Limit (Note 5) $\left(\mathrm{V}_{\text {Soft-Start }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {sense }}=\mathrm{V}_{\text {out }}, \mathrm{V}_{\text {imax }}=\mathrm{V}_{\mathrm{CC}}, \mathrm{~V}_{\text {ifb }}=0 \mathrm{~V}\right)$ | ISSIL | 30 | 90 | 150 | $\mu \mathrm{A}$ |
| Discharge Current under Hard Current Limit $\left(\mathrm{V}_{\text {Sott-Start }}=2.0 \mathrm{~V}, \mathrm{~V}_{\text {sense }}<\mathrm{V}_{\text {out }} / 2, \mathrm{~V}_{\text {imax }}=\mathrm{V}_{\mathrm{CC}}, \mathrm{~V}_{\text {ifb }}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {SSHIL }}$ | 40 | 64 | - | mA |
| Hard Current Limit Hold Time | $\mathrm{t}_{\text {SSHIL }}$ | 100 | 200 | 300 | $\mu \mathrm{s}$ |
| IMAX INPUT |  |  |  |  |  |
| Sink Current ( $\left.\mathrm{V}_{\text {in max }}=\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\text {ifb }}=\mathrm{V}_{\mathrm{CC}}\right)$ | lOL | 133 | 190 | 247 | $\mu \mathrm{A}$ |

POWER GOOD OUTPUT

| Threshold For Logic "1" to "0" Transition Upper Threshold Lower Threshold | $\mathrm{V}_{\text {th }}$ | $\overline{-}$ | $\begin{aligned} & 1.04 \\ & 0.96 \end{aligned}$ | $1.07$ | $\mathrm{V}_{\text {sense }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Response Time <br> Logic " 0 " to " 1 " ( $\mathrm{V}_{\text {sense }}$ changes from 0 V to $\mathrm{V}_{\mathrm{O}}$ ) Logic "1" to "0" ( $\mathrm{V}_{\text {sense }}$ changes from $\mathrm{V}_{\mathrm{O}}$ to 0 V ) | $t_{\text {rPG }}$ | $\begin{gathered} 200 \\ 50 \end{gathered}$ | $\begin{aligned} & 400 \\ & 100 \end{aligned}$ | $\begin{aligned} & 600 \\ & 150 \end{aligned}$ | $\mu \mathrm{s}$ |
| Sink Current (V) $\mathrm{V}_{\text {OL }}=0.5 \mathrm{~V}$ ) | lolpg | - | 10 | - | mA |
| Output Low Voltage ( $\mathrm{l}_{\text {OL }}=100 \mu \mathrm{~A}$ ) (Note 6) | VoLPG | - | 250 | 500 | mV |

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. VID1, VID3, VID4 = logic 0, and VID0, VID2 = logic 1.
4. $\mathrm{V}_{\text {sense }}$ is provided from a low impedance voltage source or shorted to the output voltage.
5. Under a typical soft current limit, the net soft-start discharge current will be $90 \mu \mathrm{~A}$ ( $\left.\mathrm{I}_{\text {SSIL }}\right)-10 \mu \mathrm{~A}\left(I_{\text {chg }}\right)=80 \mu \mathrm{~A}$. The softstart sink to source current ratio is designed to be 9:1.
6 Sense $($ Pin 6$)=5.0 \mathrm{~V}$, Comp (Pin 10) open, VID4, VID2, VID1, VID0 $=1.0$, VID3 $=0$.
7. OUTEN is internally pulled low if VIDO, $1,2,3$, and 4 are floating.
8. Due to internal pull-up resistors, there will be an additional 0.5 mA per pin if any of the VIDO, 1, 2, 3, or 4 pins are pulled low.

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{P}_{\mathrm{V}_{\mathrm{CC}}}=12 \mathrm{~V}\right.$ for typical values $\mathrm{T}_{\mathrm{A}}=$ Low to High [Notes 1, 2, 3], for $\mathrm{min} / \mathrm{max}$ values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| FAULT OUTPUT |  |  |  |  |  |
| Threshold For Logic "0" to "1" Transition | $\mathrm{V}_{\text {thF }}$ | 1.12 | 1.14 | 1.2 | $\mathrm{V}_{\text {ref }}$ |
| $\mathrm{V}_{\text {sense }}$ Response Time Switches from 2.8 V to $\mathrm{V}_{\text {CC }}$ | $\mathrm{t}_{\mathrm{r}}$ | 50 | 100 | 150 | $\mu \mathrm{s}$ |
| Sink Current (V) ${ }_{\text {OL }}=0.5 \mathrm{~V}$ ) | IoLF | - | 10 | - | mA |

OVERTEMPERATURE OUTPUT

| Threshold For Logic "1" to "0" Transition (OUTEN Voltage Decreasing) | $\mathrm{V}_{\text {thOUTEN }}$ | 1.85 | 2.0 | 2.2 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Delay Time | $\mathrm{t}_{\mathrm{DOT}}$ | 25 | 50 | 100 | $\mu \mathrm{~s}$ |
| Sink Current ( $\mathrm{V}_{\text {OL }}=0.5 \mathrm{~V}$ ) | IOLF | - | 10 | - | mA |

LOGIC INPUTS (VID0, VID1, VID2, VID3, VID4)

| Input Low State | $\mathrm{V}_{\mathrm{IL}}$ | - | - | 0.8 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input High State | $\mathrm{V}_{\mathrm{IH}}$ | 3.5 | - | - | V |
| Input Impedance | $\mathrm{R}_{\mathrm{in}}$ | - | 10 | - | $\mathrm{k} \Omega$ |

## OUTPUT ENABLE CONTROL (OUTEN)

| Over-Temperature Driver Disable and Reset <br> (OUTEN Voltage Decreasing) (Note 7) | V OTDD | 1.55 | 1.70 | 1.85 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

OUTPUT SECTIONS (G1, G2)

| Source Resistance $\left(\mathrm{V}_{\text {sense }}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{G}}=\mathrm{P}_{\mathrm{V}} \mathrm{CC}^{-1.0 \mathrm{~V})}\right.$ | $\mathrm{R}_{\mathrm{OH}}$ | - | 0.5 | - | $\Omega$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Sink Resistance $\left(\mathrm{V}_{\text {sense }}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{G}}=1.0 \mathrm{~V}\right)$ | $\mathrm{R}_{\mathrm{OL}}$ | - | 0.5 | - |  |
| Output Voltage with OUTEN Reset $\left(\mathrm{I}_{\text {sink }}=1.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 0.1 | 0.5 | V |
| Output Voltage Rise Time $\left(\mathrm{C}_{\mathrm{L}}=10 \mathrm{nF}, \mathrm{T}_{J}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\mathrm{r}}$ | - | 70 | 140 | ns |
| Output Voltage Fall Time $\left(\mathrm{C}_{\mathrm{L}}=10 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\mathrm{f}}$ | - | 70 | 140 | ns |
| G1, G2 Non-Overlap Time $\left(\mathrm{C}_{\mathrm{L}}=10 \mathrm{nF}, \mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\mathrm{NOL}}$ | 30 | 150 | 210 | ns |

TOTAL DEVICE

| Minimum Operating Voltage After Turn-OnR $\mathrm{V}_{\text {CC }}$ Decreasing) | $\mathrm{P}_{\mathrm{V}_{\mathrm{CC} \text { min }}}$ | 10.8 | - | - | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Minimum Operating Voltage After Turn-On ( $\mathrm{V}_{\mathrm{CC}}$ Decreasing) | $\mathrm{V}_{\mathrm{CC} \text { min }}$ | 3.0 | - | 4.25 | V |
| $\mathrm{V}_{\mathrm{CC}}$ Current (Note 8) (OUTEN and $\mathrm{P}_{\mathrm{V}_{C C}}$ open, VIDO, 1, 2, 3, 4 Floating) | Icc | - | 3.7 | 8.0 | mA |
| $\mathrm{P}_{\mathrm{V}_{\mathrm{CC}}}$ Current (OUTEN $=5.0 \mathrm{~V}$, VID0, 1, 2, 3, 4 Open, $\mathrm{P}_{\mathrm{V}} \mathrm{CC}=12 \mathrm{~V}$ ) | ${ }^{\mathrm{P}_{\mathrm{l}}}{ }_{\text {CC }}$ | - | 15 | - | mA |

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. VID1, VID3, VID4 = logic 0, and VID0, VID2 = logic 1.
4. $\mathrm{V}_{\text {sense }}$ is provided from a low impedance voltage source or shorted to the output voltage.
5. Under a typical soft current limit, the net soft-start discharge current will be $90 \mu \mathrm{~A}$ (ISSIL) $-10 \mu \mathrm{~A}\left(l_{\text {chg }}\right)=80 \mu \mathrm{~A}$. The softstart sink to source current ratio is designed to be 9:1.
6 Sense $($ Pin 6$)=5.0$ V, Comp (Pin 10) open, VID4, VID2, VID1, VID0 $=1.0$, VID3 $=0$.
7. OUTEN is internally pulled low if VIDO, $1,2,3$, and 4 are floating.
8. Due to internal pull-up resistors, there will be an additional 0.5 mA per pin if any of the VIDO, 1, 2, 3, or 4 pins are pulled low.


Figure 1. Output Drive Waveform


Figure 3. Error Amplifier Transient Response


Figure 5. Feedback Circuit Load Transient Response


Figure 2. 5.0 V Supply Current


Figure 4. Drive Output Source/Sink Saturation Voltage versus Load Current


Figure 6. Feedback Loop Gain and Phase versus Frequency


Figure 7. Drive Output Source/Sink Saturation Voltage versus Load Current


Figure 8. Feedback Threshold Voltage versus Temperature


Figure 9. $I_{\max }$ Current versus Temperature


Figure 10. $\mathrm{V}_{\text {sense }}$ Current Source versus Temperature


Figure 11. $\mathrm{V}_{\mathrm{Cc}}$ Undervoltage Lockout Trip Point versus Temperature


Figure 12. Oscillator Frequency versus Temperature



Figure 14. Timing Diagram

## OPERATING DESCRIPTION

The MC33470 is a monolithic, fixed frequency power switching regulator specifically designed for dc-to-dc converter applications which provide a precise supply voltage for state of the art processors. The MC33470 operates as fixed frequency, voltage mode regulator containing all the active functions required to directly implement digitally programmable step-down synchronous rectification with a minimum number of external components.

## Oscillator

The oscillator frequency is internally programmed to 300 kHz . The charge to discharge ratio is controlled to yield a $95 \%$ maximum duty cycle at the switch outputs. During the fall time of the internal sawtooth waveform, the oscillator generates an internal blanking pulse that disables the G1 output switching MOSFET. The internal sawtooth waveform has a nominal peak voltage of 2.5 V and a valley voltage of 1.5 V .

## Pulse Width Modulator

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied to the inverting input. Output switch conduction is initiated when the ramp waveform is discharged to the valley voltage. As the ramp voltage increases to a voltage that exceeds the error amplifier output, the latch resets, terminating output G1 MOSFET conduction, and turning on output G2 MOSFET,
for the duration of the oscillator ramp. This PWM/latch combination prevents multiple output pulses during a given oscillator cycle.

The sense voltage input at Pin 6 is applied to the noninverting inputs of a pair of high speed comparators. The high speed comparators' inverting inputs are tied $0.96 \times \mathrm{V}_{\text {ref }}$ and $1.04 \mathrm{x}_{\text {ref }}$, respectively, to provide an optimum response to load changes. When load transients which cause the output voltage to fall outside a $\pm 4 \%$ regulation window occur, the high speed comparators override the PWM comparator to force a zero or maximum duty cycle operating condition until the output voltage is once again within the linear window.
When voltages are initially provided to the supply pins, $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{P}_{\mathrm{V}_{\mathrm{CC}}}$, undervoltage lockout circuits monitor each of the supply voltage levels. Both G1 and G2 output pins are held low until the $\mathrm{V}_{\mathrm{CC}}$ pin voltage exceeds 4.0 V and the $\mathrm{P}_{\mathrm{V}_{\mathrm{CC}}}$ pin voltage exceeds 9.0 V .

## Error Amplifier and Voltage Reference

The error amplifier is a transconductance type amplifier, having a nominal transconductance of $800 \mu \mathrm{mho}$. The transconductance has a negative temperature coefficient. Typical transconductance is $868 \mu \mathrm{mho}$ at $0^{\circ} \mathrm{C}$ and $620 \mu \mathrm{mho}$ at $125^{\circ} \mathrm{C}$ junction temperature. The amplifier has a cascode output stage which provides a typical $3.0 \mathrm{Mega-Ohms}$ of
impedance. The typical error amplifier dc voltage gain is 67 dB .

External loop compensation is required for converter stability. Compensation components may be connected from the compensation pin to ground. The error amplifier input is tied to the sense pin which also has an internal $20 \mu \mathrm{~A}$ current source to ground. The current source is intended to provide a 24 mV offset when an external 1.2 k resistor is placed between the output voltage and the sense pin. The 24 mV offset voltage is intended to allow a greater dynamic load regulation range within a given specified tolerance for the output voltage. The offset may be increased by increasing the resistor value. The offset can be eliminated by connecting the sense pin directly to the regulated output voltage.

The voltage reference consists of an internal, low temperature coefficient, reference circuit with an added offset voltage. The offset voltage level is the output of the digital-to-analog converter. Control bits VID0 through VID4 control the amount of offset voltage which sets the value of the voltage reference, as shown in Table 1. The VID0-4 input bits each have internal 10 k pullup resistances. Therefore, the reference voltage, and the output voltage, may be programmed by connecting the VID pins to ground for logic " 0 " or by an open for a logic " 1 ". Typically, a logic " 1 " will be recognized by a voltage $>0.67 \times \mathrm{V}_{\mathrm{CC}}$. A logic " 0 " is a voltage $<\mathrm{V}_{\mathrm{CC}} / 3$.

## MOSFET Switch Outputs

The output MOSFETs are designed to switch a maximum of 18 V , with a peak drain current of 2.0 A . Both G1 and G2 output drives are designed to switch N -channel MOSFETs. Output drive controls to G1 and G2 are phased to prevent cross conduction of the internal IC output stages. Output dead time is typically 100 nanoseconds between G1 and G2 in order to minimize cross conduction of the external switching MOSFETs.

## Current Limit and Soft-Start Controls

The soft-start circuit is used both for initial power application and during current limit operation. A single external capacitor and an internal $10 \mu \mathrm{~A}$ current source control the rate of voltage increase at the error amplifier output, establishing the circuit turn on time. The G1 output will increase from zero duty cycle as the voltage across the soft-start capacitor increases beyond about 0.5 V . When the soft-start capacitor voltage has reached about 1.5 V , normal duty cycle operation of G1 will be allowed.

An overcurrent condition is detected by the current limit amplifier. The current limit amplifier is activated whenever the G1 output is high. The current limit amplifier compares the voltage drop across the external MOSFET driven by G1,
as measured at the $\mathrm{I}_{\mathrm{FB}}$ pin, with the voltage at the $\mathrm{I}_{\max }$ pin. Because the $I_{\text {max }}$ pin draws $190 \mu \mathrm{~A}$ of input current, the overcurrent threshold is programmed by an external resistor. Referring to Figure 13, the current limit resistor value can be determined from the following equation:

$$
\mathrm{R} 1=\frac{\left[\left(\mathrm{I}_{\mathrm{L}(\max )}\right)\left(\mathrm{R}_{\mathrm{DS}(\mathrm{on})}\right)\right]}{\left(\mathrm{I}_{\max }\right)}
$$

where:

$$
\begin{gathered}
\mathrm{I}_{\mathrm{L}(\max )}=\frac{\mathrm{I}_{\mathrm{O}}+\mathrm{I}_{\text {ripple }}}{2} \\
\mathrm{I}_{\mathrm{O}}=\text { Maximum load current } \\
\mathrm{I}_{\text {ripple }}=\text { Inductor peak to peak ripple current }
\end{gathered}
$$

## OUTEN Input and OT Output Pins

On and off control of the MC33470 may be implemented with the OUTEN pin. A logic " 1 " applied the OUTEN pin, where a logic " 1 " is above 2.0 V , will allow normal operation of the MC33470. The OUTEN pin also has multiple thresholds to provide over temperature protection. An negative temperature coefficient thermistor can be connected to the OUTEN pin, as shown in Figure 15. Together with $\mathrm{R}_{\mathrm{S}}$, a voltage divider is formed. The divider voltage will decrease as the thermistor temperature increases. Therefore, the thermistor should be mounted to the hottest part on the circuit board. When the OUTEN voltage drops below 2.0 V typically, the MC33470 OT pin open collector output will switch from a logic " 1 " to a logic " 0 ", providing a warning to the system. If the OUTEN voltage drops below 1.7 V, both G1 and G2 output driver pins are latched to a logic " 0 " state.


Figure 15. OUTEN/OT Overtemperature Function

## APPLICATIONS INFORMATION

## Design Example

Given the following requirements, design a switching dc-to-dc converter:

$$
\begin{aligned}
\mathrm{V}_{\mathrm{CC}} & =5.0 \mathrm{~V} \\
\mathrm{~V}_{\mathrm{CCP}} & =12 \mathrm{~V} \\
\text { VID4-0 bits } & =10111-\text { Output Voltage }=2.8 \mathrm{~V} \\
\text { Output current } & =0.3 \mathrm{~A} \text { to } 14 \mathrm{~A}
\end{aligned}
$$

Efficiency $\geq 80 \%$ at full load
Output ripple voltage $\approx 1 \%$ of output voltage

1. Choose power MOSFETs.

In order to meet the efficiency requirement, MOSFETs should be chosen which have a low value of $\mathrm{R}_{\mathrm{DS}}$ (on). However, the threshold voltage rating of the MOSFET must also be greater than 1.5 V , to prevent turn on of the synchronous rectifier MOSFETs due to dv/dt coupling through the Miller capacitance of the MOSFET drain-to-source junction. Figure 16 shows the gate voltage transient due to this effect.

In this design, choose two parallel MMSF3300 MOSFETs for both the main switch and the synchronous rectifier to maximize efficiency.
2. $\mathrm{D} \approx \mathrm{V}_{\mathrm{O}} / \mathrm{V}_{\text {in }}=2.8 / 5.0=0.56$
3. Inductor selection

In order to maintain continuous mode operation at $10 \%$ of full load current, the minimum value of the inductor will be:
$\mathrm{L}_{\text {min }}=\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{O}}\right)(\mathrm{DTs}) /\left(2 \mathrm{I}_{\mathrm{O} \text { min }}\right)$

$$
=(5-2.8)(0.56 \times 3.3 \mu \mathrm{~s}) /(2 \times 1.4 \mathrm{~A})=1.45 \mu \mathrm{H}
$$

Coilcraft's U6904, or an equivalent, provides a surface mount $1.5 \mu \mathrm{H}$ choke which is rated for for full load current.
4. Output capacitor selection
$\mathrm{V}_{\text {ripple }} \approx \Delta \mathrm{I}_{\mathrm{L}} \times \mathrm{ESR}$, where ESR is the equivalent series resistance of the output capacitance. Therefore:
$\mathrm{ESR}_{\text {max }}=\mathrm{V}_{\text {ripple }} / \Delta \mathrm{I}_{\mathrm{L}}=0.01 \times 2.8 \mathrm{~V} / 1.4 \mathrm{~A}=0.02 \Omega$ maximum

The AVX TPS series of tantalum chip capacitors may be chosen. Or OSCON capacitors may be used if leaded parts are acceptable. In this case, the output capacitance consists of two parallel $820 \mu \mathrm{~F}, 4.0 \mathrm{~V}$ capacitors. Each capacitor has a maximum specified ESR of $0.012 \Omega$.
5. Input Filter

As with all buck converters, input current is drawn in pulses. In this case, the current pulses may be 14 A peak. If a $1.5 \mu \mathrm{H}$ choke is used, two parallel OSCON $150 \mu \mathrm{~F}, 16 \mathrm{~V}$ capacitors will provide a filter cutoff frequency of 7.5 kHz .
6. Feedback Loop Compensation

The corner frequency of the output filter with $\mathrm{L}=1.5 \mu \mathrm{H}$ and $\mathrm{C}_{\mathrm{o}}=1640 \mu \mathrm{~F}$ is 3.2 kHz . In addition, the ESR of each output capacitor creates a zero at:
$\mathrm{f}_{\mathrm{z}}=1 /(2 \pi \mathrm{C}$ ESR $)=1 /(2 \pi \times 820 \mu \mathrm{~F} \times 0.012)=16.2 \mathrm{kHz}$
The dc gain of the PWM is: Gain $=\mathrm{V}_{\mathrm{in}} / \mathrm{V}_{\mathrm{pp}}=5 / 1=5.0$. Where $\mathrm{V}_{\mathrm{pp}}$ is the peak-to-peak sawtooth voltage across the internal timing capacitor. In order to make the feedback loop as responsive as possible to load changes, choose the unity gain frequency to be $10 \%$ of the switching frequency, or 30 kHz . Plotting the PWM gain over frequency, at a frequency of 30 kHz the gain is about $-16.5 \mathrm{~dB}=0.15$. Therefore, to have a 30 kHz unity gain loop, the error amplifier gain at 30 kHz should be $1 / 0.15=6.7$. Choose a design phase margin for the loop of $60^{\circ}$. Also, choose the error amp type to be an integrator for best dc regulation performance. The phase boost needed by the error amplifier is then $60^{\circ}$ for the desired phase margin. Then, the following calculations can be made:

$$
\begin{aligned}
& \mathrm{k}=\tan \left[\text { Boost } / 2+45^{\circ}\right]=\tan [60 / 2+45]=3.73 \\
& \text { Error Amp zero freq }=\mathrm{f}_{\mathrm{c}} / \mathrm{K}=30 \mathrm{kHz} / 3.73=8.0 \mathrm{kHz} \\
& \text { Error Amp pole freq }=\mathrm{K}_{\mathrm{fc}}=3.73 \times 30 \mathrm{kHz}=112 \mathrm{kHz} \\
& \mathrm{R} 2=\text { Error Amp Gain } / \mathrm{G}_{\mathrm{m}}=6.7 / 800 \mu=8.375 \mathrm{k}-\text { use an } \\
& \quad 8.2 \mathrm{k} \text { standard value } \\
& \begin{aligned}
\mathrm{C} 16 & =1 /\left(2 \pi \mathrm{R} 2 \mathrm{f}_{\mathrm{z}}\right)=1 /(2 \pi \times 8.2 \mathrm{k} \times 8.0 \mathrm{kHz}) \\
& =2426 \mathrm{pF}-\text { use } 2200 \mathrm{pF} \\
\mathrm{C} 17= & 1 /\left(2 \pi \mathrm{R} 2 \mathrm{f}_{\mathrm{p}}\right)=1 /(2 \pi \times 8.2 \mathrm{kx} 112 \mathrm{kHz}) \\
& =173 \mathrm{pF}-\text { use } 100 \mathrm{pF}
\end{aligned}
\end{aligned}
$$

The complete design is shown in Figure 13. The PC board top and bottom views are shown in Figures 17 and 18.


Figure 16. Voltage Coupling Through Miller Capacitance

PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
| :---: | :---: | :---: |
| 1 | G2 | This is a high current dual totem pole output Gate Drive for the Lower, or rectifier, N -channel MOSFET. Its output swings from ground to $\mathrm{P}_{\mathrm{Vcc}}$. During initial power application, both G 2 and G 1 are held low until both $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{P}_{\mathrm{VCC}}$ have reached proper levels. |
| 2 | $\mathrm{P}_{\mathrm{V}} \mathrm{CC}$ | This is a separate power source connection for driving N-channel MOSFETs from the G1 and G2 outputs. It may be connected to 12 V . |
| 3 | $\mathrm{P}_{\text {Gnd }}$ | This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry. |
| 4 | $\mathrm{A}_{\text {Gnd }}$ | This pin is the ground for the control circuitry. |
| 5 | $\mathrm{V}_{\mathrm{CC}}$ | This pin is the positive supply of the control IC. |
| 6 | Sense | This pin is used for feedback from the output of the power supply. It has a $20 \mu \mathrm{~A}$ current source to ground which can be used to provide offset in the converter output voltage. |
| 7 | $I_{\text {max }}$ | This pin sets the current limit threshold. $190 \mu \mathrm{~A}$ must be sourced into the pin. The external resistor is determined from the following equation: $\mathrm{R}=\left(\left[\mathrm{R}_{\mathrm{DS}(o n)}\right][\mathrm{LIMM}] /[190 \mu \mathrm{~A}]\right)$ |
| 8 | $\mathrm{I}_{\text {FB }}$ | This pin has two functions. First, it provides cycle-by-cycle current limiting. Second, if the current is excessive, this pin will reinitiate a soft-start cycle. If the voltage at the $I_{\text {FB }}$ pin drops below the voltage at the $I_{\max }$ pin when G 1 is on, the controller will go into current limit. The current limit circuit can be disabled by floating the $I_{\max }$ pin and shorting the $\mathrm{I}_{\mathrm{FB}}$ pin to $\mathrm{V}_{\mathrm{CC}}$. |
| 9 | SS | This is the soft-start pin. A capacitor at this pin, in conjunction with a $10 \mu \mathrm{~A}$ internal current source, sets the soft-start time. During moderate overload (current limit with $\mathrm{V}_{\mathrm{O}}>50 \%$ of the set value), the soft-start capacitor will be discharged by an internal $90 \mu \mathrm{~A}$ current source in order to reduce the duty cycle of G1. During hard current limit (current limit with $\mathrm{V}_{\mathrm{O}}<50 \%$ of set value), the soft-start capacitor will be discharged by a 64 mA current source. |
| 10 | Comp | This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter. |
| 11 | $\overline{\text { OT }}$ | This is the over temperature fault pin. $\overline{\mathrm{OT}}$ is an open drain output that will be pulled low if the OUTEN pin is less than 2.0 V . |
| 12 | Fault | This pin indicates a fault condition. Fault is an open drain output that switches low if $\mathrm{V}_{\mathrm{O}}$ exceeds $115 \%$ of its set value. Once triggered, the controller will remain in this state until the power supply is recycled or the OUTEN pin is toggled. |
| 13 | $P_{\text {wrgd }}$ | This pin is an open drain output which indicates that $\mathrm{V}_{\mathrm{O}}$ is properly regulated. A high level on $P_{\text {wrgd }}$ indicates that $V_{O}$ is within $\pm 4 \%$ of its set value for more than $400 \mu \mathrm{~s}$. $\mathrm{P}_{\text {wrgd }}$ will switch low if $V_{O}$ is outside $\pm 4 \%$ for more than $100 \mu \mathrm{~s}$. |
| 14 | VID4 | Voltage ID pin. This CMOS-compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull-up resistor to $\mathrm{V}_{\mathrm{CC}}$. |
| 15 | VID3 | Voltage ID pin. This CMOS-compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull-up resistor to $\mathrm{V}_{\mathrm{CC}}$. |
| 16 | VID2 | Voltage ID pin. This CMOS-compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull-up resistor to $\mathrm{V}_{\mathrm{CC}}$. |
| 17 | VID1 | Voltage ID pin. This CMOS-compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull-up resistor to $\mathrm{V}_{\mathrm{CC}}$. |
| 18 | VIDO | Voltage ID pin. This CMOS-compatible input programs the output voltage as shown in Table 2. This pin has an internal 10 k pull-up resistor to $\mathrm{V}_{\mathrm{CC}}$. |
| 19 | OUTEN | This is the on/off control pin. A CMOS-compatible logic "1" allows the controller to operate. This pin can also be used as a temperature sensor to trigger the OT pin (when OUTEN drops below 2.0 V OT pulls low). When OUTEN drops below 1.7 V for longer than $50 \mu \mathrm{~s}$, the controller will shut down. |
| 20 | G1 | This is a high current dual totem pole output Gate Drive for the Upper, or switching, N-channel MOSFET. Its output swings from ground to $\mathrm{P}_{\mathrm{Vcc}}$. During initial power application, both G 2 and G 1 are held low until both $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{P}_{\mathrm{Vcc}}$ have reached proper levels. |

## MC33470

Table 1. Voltage Identification Code

| VID4 | VID3 | VID2 | VID1 | VIDO | $\mathrm{v}_{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 1 | 1 | 1 | - |
| 0 | 1 | 1 | 1 | 0 | - |
| 0 | 1 | 1 | 0 | 1 | - |
| 0 | 1 | 1 | 0 | 0 | - |
| 0 | 1 | 0 | 1 | 0 | - |
| 0 | 1 | 0 | 0 | 1 | - |
| 0 | 1 | 0 | 0 | 0 | - |
| 0 | 0 | 1 | 1 | 1 | - |
| 0 | 0 | 1 | 1 | 0 | - |
| 0 | 0 | 1 | 0 | 1 | 1.8 |
| 0 | 0 | 1 | 0 | 0 | 1.85 |
| 0 | 0 | 0 | 1 | 1 | 1.9 |
| 0 | 0 | 0 | 1 | 0 | 1.95 |
| 0 | 0 | 0 | 0 | 1 | 2.0 |
| 0 | 0 | 0 | 0 | 0 | 2.05 |
| 1 | 1 | 1 | 1 | 1 | No CPU |
| 1 | 1 | 1 | 1 | 0 | 2.1 |
| 1 | 1 | 1 | 0 | 1 | 2.2 |
| 1 | 1 | 1 | 0 | 0 | 2.3 |
| 1 | 1 | 0 | 1 | 1 | 2.4 |
| 1 | 1 | 0 | 1 | 0 | 2.5 |
| 1 | 1 | 0 | 0 | 1 | 2.6 |
| 1 | 1 | 0 | 0 | 0 | 2.7 |
| 1 | 0 | 1 | 1 | 1 | 2.8 |
| 1 | 0 | 1 | 1 | 0 | 2.9 |
| 1 | 0 | 1 | 0 | 1 | 3.0 |
| 1 | 0 | 1 | 0 | 0 | 3.1 |
| 1 | 0 | 0 | 1 | 1 | 3.2 |
| 1 | 0 | 0 | 1 | 0 | 3.3 |
| 1 | 0 | 0 | 0 | 1 | 3.4 |
| 1 | 0 | 0 | 0 | 0 | 3.5 |

## MC33470

Table 2. Connector Pin Function

| PIN | ROW A | ROW B |
| :---: | :---: | :---: |
| 1 | $5.0 \mathrm{~V}_{\text {in }}$ | $5.0 \mathrm{~V}_{\text {in }}$ |
| 2 | $5.0 \mathrm{~V}_{\text {in }}$ | $5.0 \mathrm{~V}_{\text {in }}$ |
| 3 | $5.0 \mathrm{~V}_{\text {in }}$ | Reserved |
| 4 | $12 \mathrm{~V}_{\text {in }}$ | $12 \mathrm{~V}_{\text {in }}$ |
| 5 | Reserved | UP\# |
| 6 | $1_{\text {share }}$ | OUTEN |
| 7 | VIDO | VID1 |
| 8 | VID2 | VID3 |
| 9 | VID4 | $\mathrm{P}_{\text {wrgd }}$ |
| 10 | $\mathrm{V}_{\text {CCP }}$ | $V_{\text {SS }}$ |
| 11 | $\mathrm{V}_{\text {SS }}$ | $\mathrm{V}_{\text {CCP }}$ |
| 12 | $\mathrm{V}_{\text {CCP }}$ | $\mathrm{V}_{\text {SS }}$ |
| 13 | $\mathrm{V}_{\text {SS }}$ | $\mathrm{V}_{\text {CCP }}$ |
| 14 | $\mathrm{V}_{\text {CCP }}$ | $\mathrm{V}_{\text {SS }}$ |
| 15 | $\mathrm{V}_{S S}$ | $\mathrm{V}_{\text {CCP }}$ |
| 16 | $\mathrm{V}_{\text {CCP }}$ | $\mathrm{V}_{\text {SS }}$ |
| 17 | $\mathrm{V}_{\text {SS }}$ | $\mathrm{V}_{\mathrm{CCP}}$ |
| 18 | $\mathrm{V}_{\text {CCP }}$ | $\mathrm{V}_{\text {SS }}$ |
| 19 | $\mathrm{V}_{\text {SS }}$ | $\mathrm{V}_{\mathrm{CCP}}$ |
| 20 | $\mathrm{V}_{\text {CCP }}$ | $\mathrm{V}_{S S}$ |



Figure 17. PC Board Top View


Figure 18. PC Board Bottom View

## CS51313

## Synchronous CPU <br> Buck Controller Capable of Implementing Multiple Linear Regulators

The CS51313 is a synchronous dual NFET Buck Regulator Controller. It is designed to power the core logic of the latest high performance CPUs. It uses the $\mathrm{V}^{2 \mathrm{TM}}$ control method to achieve the fastest possible transient response and best overall regulation. It incorporates many additional features required to ensure the proper operation and protection of the CPU and Power system. The CS51313 provides the industry's most highly integrated solution, minimizing external component count, total solution size, and cost.

The CS51313 is specifically designed to power Intel's Pentium® II processor and includes the following features: 5-bit DAC with $1.2 \%$ tolerance, Power Good output, overcurrent hiccup mode protection, overvoltage protection, $\mathrm{V}_{\mathrm{CC}}$ monitor, Soft Start, adaptive voltage positioning and adaptive FET non-overlap time. A precision reference trimmed to $1.0 \%$ is also externally available for use by other regulators. The CS51313 will operate over an 8.4 V to 14 V range and is available in 16 lead narrow body surface mount package.

## Features

- Synchronous Switching Regulator Controller for CPU VCORE
- Dual N-Channel MOSFET Synchronous Buck Design
- $\mathrm{V}^{2}$ Control Topology
- 200 ns Transient Loop Response
- 5-Bit DAC with $1.2 \%$ Tolerance
- Hiccup Mode Overcurrent Protection
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- 65 ns Adaptive FET Non-Overlap Time
- Adaptive Voltage Positioning
- Power Good Output Monitors Regulator Output
- $V_{\text {CC }}$ Monitor Provides Undervoltage Lockout
- OVP Output Monitors Regulator Output
- Enable Through Use of the COMP Pin
- +1.23 V Reference Voltage Available Externally


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http://onsemi.com

$\qquad$

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS51313GD16 | SO-16 | 48 Units/Rail |
| CS51313GDR16 | SO-16 | 2500 Tape \& Reel |

CS51313


Figure 1. Application Diagram

## MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Note 2) | 2.0 | kV |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
2. All pins are rated 2.0 kV except for the $\mathrm{V}_{\text {REF }}$ pin (Pin 5) which is typically rated at 800 V .
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Bandgap Reference Voltage | $\mathrm{V}_{\text {REF }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| IC Power Input | $\mathrm{V}_{\text {CC }}$ | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | $1.5 \mathrm{APeak}, 200 \mathrm{~mA} \mathrm{DC}$ |
| Compensation Pin | COMP | 6.0 V | -0.3 V | 1.0 mA | 5.0 mA |
| Voltage Feedback Input, <br> Output Voltage Sense Pin, <br> Voltage ID DAC Inputs | $\mathrm{V}_{\text {FB }}, \mathrm{V}_{\text {OUT, }} \mathrm{V}_{\text {ID0-4 }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Off-Time Pin | COFF | 6.0 V | -0.3 V | 1.0 mA |  |
| High Side, Low Side FET Drivers | GATE(H), GATE(L) | 16 V | -0.3 V | $1.5 \mathrm{~A} \mathrm{Peak,200} \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{APeak}, 200 \mathrm{~mA} \mathrm{DC}$ |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | 1.0 mA | 30 mA |
| Overvoltage Protection | OVP | 15 V | -0.3 V | 30 mA | 1.0 mA |
| Ground | 0 GND | 0 V | $1.5 \mathrm{APeak}, 200 \mathrm{~mA} \mathrm{DC}$ | $\mathrm{N} / \mathrm{A}$ |  |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$;
2.0 V DAC Code ( $\left.\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}$, $\mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified.)

| Characteristic | Test Conditions |  |
| :--- | :--- | :--- |

Voltage Identification DAC

|  |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{V}_{\mathrm{COMP}} \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$. Note 3 |  |  |  |  |  |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | $75^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$ |  |  |  | $25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 75^{\circ} \mathrm{C}$ |  |  |  |  |
| $\mathrm{V}_{\text {ID4 }}$ | $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | VIDO | Min | Typ | Max | $\pm$ Tol | Min | Typ | Max | $\pm$ Tol |  |
| 1 | 0 | 0 | 0 | 0 | 3.483 | 3.525 | 3.567 | 1.2\% | 3.455 | 3.525 | 3.596 | 2.0\% | V |
| 1 | 0 | 0 | 0 | 1 | 3.384 | 3.425 | 3.466 | 1.2\% | 3.357 | 3.425 | 3.494 | 2.0\% | V |
| 1 | 0 | 0 | 1 | 0 | 3.285 | 3.325 | 3.365 | 1.2\% | 3.259 | 3.325 | 3.392 | 2.0\% | V |
| 1 | 0 | 0 | 1 | 1 | 3.186 | 3.225 | 3.264 | 1.2\% | 3.161 | 3.225 | 3.290 | 2.0\% | V |
| 1 | 0 | 1 | 0 | 0 | 3.087 | 3.125 | 3.163 | 1.2\% | 3.063 | 3.125 | 3.188 | 2.0\% | V |
| 1 | 0 | 1 | 0 | 1 | 2.989 | 3.025 | 3.061 | 1.2\% | 2.965 | 3.025 | 3.086 | 2.0\% | V |
| 1 | 0 | 1 | 1 | 0 | 2.890 | 2.925 | 2.960 | 1.2\% | 2.875 | 2.925 | 2.975 | 1.7\% | V |
| 1 | 0 | 1 | 1 | 1 | 2.791 | 2.825 | 2.859 | 1.2\% | 2.777 | 2.825 | 2.873 | 1.7\% | V |
| 1 | 1 | 0 | 0 | 0 | 2.692 | 2.725 | 2.758 | 1.2\% | 2.679 | 2.725 | 2.771 | 1.7\% | V |
| 1 | 1 | 0 | 0 | 1 | 2.594 | 2.625 | 2.657 | 1.2\% | 2.580 | 2.625 | 2.670 | 1.7\% | V |
| 1 | 1 | 0 | 1 | 0 | 2.495 | 2.525 | 2.555 | 1.2\% | 2.482 | 2.525 | 2.568 | 1.7\% | V |
| 1 | 1 | 0 | 1 | 1 | 2.396 | 2.425 | 2.454 | 1.2\% | 2.389 | 2.425 | 2.461 | 1.5\% | V |
| 1 | 1 | 1 | 0 | 0 | 2.297 | 2.325 | 2.353 | 1.2\% | 2.290 | 2.325 | 2.360 | 1.5\% | V |
| 1 | 1 | 1 | 0 | 1 | 2.198 | 2.225 | 2.252 | 1.2\% | 2.192 | 2.225 | 2.258 | 1.5\% | V |
| 1 | 1 | 1 | 1 | 0 | 2.099 | 2.125 | 2.151 | 1.2\% | 2.093 | 2.125 | 2.157 | 1.5\% | V |
| 0 | 0 | 0 | 0 | 0 | 2.050 | 2.075 | 2.100 | 1.2\% | 2.044 | 2.075 | 2.106 | 1.5\% | V |
| 0 | 0 | 0 | 0 | 1 | 2.001 | 2.025 | 2.049 | 1.2\% | 1.995 | 2.025 | 2.055 | 1.5\% | V |
| 0 | 0 | 0 | 1 | 0 | 1.953 | 1.975 | 1.997 | 1.1\% | 1.945 | 1.975 | 2.005 | 1.5\% | V |
| 0 | 0 | 0 | 1 | 1 | 1.904 | 1.925 | 1.946 | 1.1\% | 1.896 | 1.925 | 1.954 | 1.5\% | V |
| 0 | 0 | 1 | 0 | 0 | 1.854 | 1.875 | 1.896 | 1.1\% | 1.847 | 1.875 | 1.903 | 1.5\% | V |
| 0 | 0 | 1 | 0 | 1 | 1.805 | 1.825 | 1.845 | 1.1\% | 1.798 | 1.825 | 1.852 | 1.5\% | V |
| 0 | 0 | 1 | 1 | 0 | 1.755 | 1.775 | 1.795 | 1.1\% | 1.748 | 1.775 | 1.802 | 1.5\% | V |
| 0 | 0 | 1 | 1 | 1 | 1.706 | 1.725 | 1.744 | 1.1\% | 1.699 | 1.725 | 1.751 | 1.5\% | V |
| 0 | 1 | 0 | 0 | 0 | 1.656 | 1.675 | 1.694 | 1.1\% | 1.650 | 1.675 | 1.700 | 1.5\% | V |
| 0 | 1 | 0 | 0 | 1 | 1.607 | 1.625 | 1.643 | 1.1\% | 1.601 | 1.625 | 1.649 | 1.5\% | V |
| 0 | 1 | 0 | 1 | 0 | 1.558 | 1.575 | 1.593 | 1.1\% | 1.551 | 1.575 | 1.599 | 1.5\% | V |
| 0 | 1 | 0 | 1 | 1 | 1.508 | 1.525 | 1.542 | 1.1\% | 1.502 | 1.525 | 1.548 | 1.5\% | V |
| 0 | 1 | 1 | 0 | 0 | 1.459 | 1.475 | 1.491 | 1.1\% | 1.453 | 1.475 | 1.497 | 1.5\% | V |
| 0 | 1 | 1 | 0 | 1 | 1.409 | 1.425 | 1.441 | 1.1\% | 1.404 | 1.425 | 1.446 | 1.5\% | V |
| 0 | 1 | 1 | 1 | 0 | 1.360 | 1.375 | 1.390 | 1.1\% | 1.354 | 1.375 | 1.396 | 1.5\% | V |
| 0 | 1 | 1 | 1 | 1 | 1.310 | 1.325 | 1.340 | 1.1\% | 1.305 | 1.325 | 1.345 | 1.5\% | V |
| 1 | 1 | 1 | 1 | 1 | 1.225 | 1.250 | 1.275 | 2.0\% | 1.225 | 1.250 | 1.275 | 2.0\% | V |

3. The IC power dissipation in a typical application with $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$, switching frequency $\mathrm{f}_{\mathrm{Sw}}=250 \mathrm{kHz}, 50 \mathrm{nc}$ MOSFETs and $\mathrm{R}_{\theta J \mathrm{~A}}=115^{\circ} \mathrm{C} / \mathrm{W}$ yields an operating junction temperature rise of approximately $52^{\circ} \mathrm{C}$, and a junction temperature of $77^{\circ} \mathrm{C}$ with an ambient temperature of $25^{\circ} \mathrm{C}$.

## CS51313

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$;
2.0 V DAC Code ( $\left.\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Voltage Identification DAC (continued) | $9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 14 \mathrm{~V}$ | - | 0.01 | - | $\% / \mathrm{V}$ |
| Line Regulation | $\mathrm{V}_{\mathrm{ID} 4}, \mathrm{~V}_{\mathrm{ID} 3}, \mathrm{~V}_{\mathrm{ID} 2}, \mathrm{~V}_{\mathrm{ID} 1}, \mathrm{~V}_{\mathrm{ID} 0}$ | 1.0 | 1.25 | 2.4 | V |
| Input Threshold | $\mathrm{V}_{\mathrm{ID} 4}, \mathrm{~V}_{\mathrm{ID} 3}, \mathrm{~V}_{\mathrm{ID} 2}, \mathrm{~V}_{\mathrm{ID} 1}, \mathrm{~V}_{\mathrm{ID} 0}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Input Pull-Up Resistance | - | 5.48 | 5.65 | 5.82 | V |
| Pull-Up Voltage |  |  |  |  |  |

Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current | $0.2 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 3.5 \mathrm{~V}$ | -7.0 | 0.1 | 7.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| COMP Source Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V}$ to $3.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=1.9 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{~A}$ |
| COMP Sink Current | $\mathrm{V}_{\mathrm{COMP}}=1.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{FB}}=2.1 \mathrm{~V}$ | 30 | 60 | 120 | $\mu \mathrm{~A}$ |
| Open Loop Gain | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 80 | - | dB |
| Unity Gain Bandwidth | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 50 | - | kHz |
| PSRR @ 1.0 kHz | $\mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}$ | - | 70 | - | dB |
| Transconductance |  | - | 32 | - | mmho |
| Output Impedance | - | - | 0.5 | - | $\mathrm{M} \Omega$ |

Bandgap Reference Voltage

| $V_{\text {REF }}$ | $I_{\text {VREF }}=10 \mu \mathrm{~A}$ Sourcing, $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ | 1.211 | 1.23 | 1.248 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

GATE(H) and GATE(L)

| High Voltage at 100 mA | Measure $\mathrm{V}_{\mathrm{CC}}-\mathrm{GATE}(\mathrm{L}) /(\mathrm{H})$ | - | 1.2 | 2.1 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Low Voltage at 100 mA | Measure $\operatorname{GATE}(\mathrm{L}) /(\mathrm{H})$ | - | 1.0 | 1.5 | V |
| Rise Time | $1.6 \mathrm{~V}<\mathrm{GATE}(\mathrm{H}) /(\mathrm{L})<\left(\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right)$ | - | 40 | 80 | ns |
| Fall Time | $\left(\mathrm{V}_{\mathrm{CC}}-2.5 \mathrm{~V}\right)>\operatorname{GATE}(\mathrm{L}) /(\mathrm{H})>1.6 \mathrm{~V}$ | - | 40 | 80 | ns |
| GATE $(\mathrm{H})$ to GATE(L) Delay | $\mathrm{GATE}(\mathrm{H})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{~L})>2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE $(\mathrm{L})$ to GATE(H) Delay | $\mathrm{GATE}(\mathrm{L})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{H})>2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-Down | Resistance to GND. Note 4 | 20 | 50 | 115 | $\mathrm{k} \Omega$ |

Overcurrent Protection

| OVC Comparator Offset Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 3.5 \mathrm{~V}$ | 77 | 86 | 101 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Discharge Threshold Voltage | - | 0.2 | 0.25 | 0.3 | V |
| $\mathrm{~V}_{\text {OUT }}$ Bias Current | $0.2 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 3.5 \mathrm{~V}$ | -7.0 | 0.1 | 7.0 | $\mu \mathrm{~A}$ |
| OVC Latch Discharge Current | $\mathrm{V}_{\text {COMP }}=1.0 \mathrm{~V}$ | 100 | 800 | 2500 | $\mu \mathrm{~A}$ |

PWM Comparator

| PWM Comparator Offset Voltage | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{FB}} \leq 3.5 \mathrm{~V}$ | 0.99 | 1.1 | 1.23 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Transient Response | $\mathrm{V}_{\mathrm{FB}}=0$ to 3.5 V | - | 200 | 300 | ns |

Coff

| Off-Time |  | 1.0 | 1.6 | 2.3 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Charge Current | $V_{\text {COFF }}=1.5 \mathrm{~V}$ | - | 550 | - | $\mu \mathrm{A}$ |
| Discharge Current | $V_{\text {COFF }}=1.5 \mathrm{~V}$ | - | 25 | - | mA |

4. Guaranteed by design, not $100 \%$ tested in production.

## CS51313

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$;
2.0 V DAC Code ( $\left.\mathrm{V}_{\mathrm{ID} 4}=\mathrm{V}_{\mathrm{ID} 3}=\mathrm{V}_{\mathrm{ID2} 2}=\mathrm{V}_{\mathrm{ID} 1}=0, \mathrm{~V}_{\mathrm{ID} 0}=1.0\right) \mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=\mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{OFF}}=390 \mathrm{pF}$; unless otherwise specified. $)$

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output |  |  |  |  |  |
| PWRGD Sink Current | $\mathrm{V}_{\mathrm{FB}}=1.7 \mathrm{~V}, \mathrm{~V}_{\text {PWRGD }}=1.0 \mathrm{~V}$ | 0.5 | 4.0 | 15 | mA |
| PWRGD Upper Threshold | \% of Nominal DAC Code | 5.0 | 8.5 | 12 | \% |
| PWRGD Lower Threshold | \% of Nominal DAC Code | -12 | -8.5 | -5.0 | \% |
| PWRGD Output Low Voltage | $\mathrm{V}_{\mathrm{FB}}=1.7 \mathrm{~V}$, $\mathrm{IPWRGD}=500 \mu \mathrm{~A}$ | - | 0.2 | 0.3 | V |

## Overvoltage Protection (OVP) Output

| OVP Source Current | OVP = 1.0 V | 1.0 | 10 | 25 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| OVP Threshold | \% of Nominal DAC Code | 5.0 | 8.5 | 12 | $\%$ |
| OVP Pull-Up Voltage | lovP $=1.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}-\mathrm{V}_{\text {OVP }}$ | - | 1.1 | 1.5 | V |

General Electrical Specifications

| $\mathrm{V}_{\text {CC }}$ Monitor Start Threshold | - | 7.9 | 8.4 | 8.9 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ Monitor Stop Threshold | - | 7.6 | 8.1 | 8.6 | V |
| Hysteresis | Start-Stop | 0.15 | 0.3 | 0.6 | V |
| $\mathrm{V}_{\mathrm{CC}}$ Supply Current | No Load on GATE(H), GATE(L) | - | 12 | 20 | mA |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-16 | PIN SYMBOL | FUNCTION |
| 1, 2, 3, 4, 6 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID } 4}$ | Voltage ID DAC inputs. These pins are internally pulled up to 5.65 V if left open. $\mathrm{V}_{\text {ID4 } 4}$ selects the DAC range. When $\mathrm{V}_{\text {ID4 }}$ is high (logic one), the Error Amp reference range is 2.125 V to 3.525 V with 100 mV increments. When $\mathrm{V}_{\text {ID4 }}$ is low (logic zero), the Error Amp reference voltage is 1.325 V to 2.075 V with 50 mV increments. |
| 5 | $\mathrm{V}_{\text {REF }}$ | Bandgap Reference Voltage. It can be used to generate other regulated output voltages. |
| 7 | $\mathrm{V}_{\mathrm{FB}}$ | Error amp inverting input, PWM comparator non-inverting input, current limit comparator non-inverting input, PWRGD and OVP comparator input. |
| 8 | $\mathrm{V}_{\text {OUT }}$ | Current limit comparator inverting input. |
| 9 | $\mathrm{V}_{\mathrm{CC}}$ | Input power supply pin for the internal circuitry. Decouple with filter capacitor to GND. |
| 10 | GATE(H) | High side switch FET driver pin. |
| 11 | GND | Ground pin. |
| 12 | GATE(L) | Low side synchronous FET driver pin. |
| 13 | OVP | Overvoltage protection pin. Goes high when overvoltage condition is detected on $\mathrm{V}_{\mathrm{FB}}$. |
| 14 | PWRGD | Power Good Output. Open collector output drives low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. |
| 15 | $\mathrm{C}_{\text {OFF }}$ | Off-Time Capacitor pin. A capacitor from this pin to GND sets the off time for the regulator. |
| 16 | COMP | Error amp output. PWM comparator inverting input. A capacitor to GND provides error amp compensation. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. GATE(H) and GATE(L) Falltime vs. Load Capacitance


Figure 5. DAC Output Voltage vs. Temperature, DAC Code = 00001


Figure 4. GATE(H) and GATE(L) Risetime vs. Load Capacitance


Figure 6. Percent Output Error vs. DAC Output Voltage Setting, VID4 $=0$


Figure 7. Percent Output Error vs. DAC Output Voltage Setting, VID4 $=1$

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## V $^{2}$ Control Method

The $\mathrm{V}^{2}$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

The $\mathrm{V}^{2}$ control method is illustrated in Figure 8. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to $0 \%$ or $100 \%$ duty cycle as required.


Figure 8. ${ }^{2}$ Control Diagram

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $\mathrm{V}^{2}$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $\mathrm{V}^{2}$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.
Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation.
A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $\mathrm{V}^{2}$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

## Constant Off-Time

To minimize transient response, the CS51313 uses a Constant Off-Time method to control the rate of output pulses. During normal operation, the Off-Time of the high side switch is terminated after a fixed period, set by the Coff capacitor. Every time the $\mathrm{V}_{\mathrm{FB}}$ pin exceeds the COMP pin voltage an Off-Time is initiated. To maintain regulation, the $\mathrm{V}^{2}$ Control Loop varies switch On-Time. The PWM comparator monitors the output voltage ramp, and terminates the switch On-Time.
Constant Off-Time provides a number of advantages. Switch Duty Cycle can be adjusted from 0 to $100 \%$ on a pulse-by pulse basis when responding to transient conditions. Both $0 \%$ and $100 \%$ Duty Cycle operation can be maintained for extended periods of time in response to Load or Line transients.

## Programmable Output

The CS51313 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.125 V to 3.525 V in 100 mV steps, the second is 1.325 V to 2.075 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS51313 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $\mathrm{V}_{\mathrm{FB}}$ pin, as in traditional controllers. The CS51313 is specifically designed to meet or exceed Intel's Pentium II specifications.

## Error Amplifier

An inherent benefit of the $\mathrm{V}^{2}$ control topology is that there is no large bandwidth requirement on the error amplifier design. The reaction time to an output load step has no relation to the crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this "slow" feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered. The COMP pin is the output of the error amplifier and a capacitor to GND compensates the error amplifier loop. Additionally, through the built-in offset on the PWM Comparator non-inverting input, the COMP pin provides the hiccup timing for the Overcurrent Protection, the Soft Start function that minimizes inrush currents during regulator power-up and switcher output enable.

## Reference Voltage

The CS51313 has a precision reference trimmed to $1.5 \%$ over temperature, which is externally available for use by other power supplies on the motherboard. For instance, the $\mathrm{V}_{\text {REF }}$ pin can be used to configure an LDO controller that drives either a MOSFET or a bipolar transistor. The compensation criteria on this LDO controller is set by the dynamic performance requirement on the overall power supply. The following circuit demonstrates the typical connections required to implement an LDO controller using the CS51313 $\mathrm{V}_{\text {REF }}$ pin.


Figure 9. $\mathrm{V}_{\text {REF }}$ Used in an N-FET LDO Regulator
The applications diagram shows a pair of linear regulators for $\mathrm{V}_{\text {GTL }}$ and $\mathrm{V}_{\text {CLOCK. }}$. The $1.23 \mathrm{~V}_{\mathrm{REF}}$ of the CS51313 is used as the reference for both regulators. The feedback resistors determine the output voltage for each regulator. In this case, it will be $1.5 \mathrm{~V} @ 3.0 \mathrm{~A}$ for $\mathrm{V}_{\mathrm{GTL}}$ and $2.5 \mathrm{~V} @$ 1.0 A for $\mathrm{V}_{\text {Clock. }}$. In Figure 9 the ratio of resistor R1 to resistor R 2 is $\left(\mathrm{V}_{\text {OUT }} / \mathrm{V}_{\text {ReF }}\right)-1$, where $\mathrm{V}_{\text {OUT }}=1.5 \mathrm{~V}$ and $\mathrm{V}_{\text {REF }}=1.23 \mathrm{~V}$. The same formula can be used to determine the ratio of the feedback resistors needed to implement a 2.5 V linear regulator $\left(\mathrm{V}_{\text {Out }}=2.5 \mathrm{~V}\right)$. To negate the bias
current of the operational amplifier, a resistor with a value equal to the parallel combination of the feedback resistors ( $\mathrm{R} 1 / / \mathrm{R} 2$ ) is connected in series with the non-inverting input of this operational amplifier. R2 sets the minimum output current, ( $\left.\mathrm{I}_{\mathrm{MIN}}=\mathrm{V}_{\mathrm{REF}} / \mathrm{R} 2\right)$.
The pass transistor must be able to dissipate the power adequately while keeping the junction temperature below the maximum specified by the manufacturer. For example, with $\mathrm{V}_{\mathrm{GTL}}$ output of 1.5 V , input voltage of 3.3 V , and output DC current of 3.0 A , the pass transistor dissipates $(3.3 \mathrm{~V}-$ $1.5 \mathrm{~V}) \times 3.0 \mathrm{~A}=5.4 \mathrm{~W}$.

Sufficient output capacitance must be added to ensure that the output voltage remains within specification during transient loading. For example, the GTL bus load can ramp from 0 to 2.7 A at a rate of $8 \mathrm{~A} / \mu \mathrm{s}$. The designer needs to verify that the circuit will meet these requirements using the transistor and operational amplifier chosen.

## Startup

The CS51313 provides a controlled startup of regulator output voltage and features Programmable Soft Start implemented through the Error Amp and external Compensation Capacitor. This feature, combined with overcurrent protection, prevents stress to the regulator power components and overshoot of the output voltage during startup.

As power is applied to the regulator, the CS51313 Undervoltage Lockout circuit (UVL) monitors the IC's supply voltage $\left(\mathrm{V}_{\mathrm{CC}}\right)$ which is typically connected to the +12 V output of the AC-DC power supply. The UVL circuit prevents the NFET gates from being activated until $\mathrm{V}_{\mathrm{CC}}$ exceeds the 8.4 V (typ) threshold. Hysteresis of 300 mV (typ) is provided for noise immunity. The Error Amp Capacitor connected to the COMP pin is charged by a $30 \mu \mathrm{~A}$ current source. This capacitor must be charged to 1.1 V (typ) so that it exceeds the PWM comparator's offset before the $\mathrm{V}^{2} \mathrm{PWM}$ control loop permits switching to occur.

When $\mathrm{V}_{\mathrm{CC}}$ has exceeded 8.4 V and COMP has charged to 1.1 V, the upper Gate driver $(\operatorname{GATE}(\mathrm{H}))$ is activated, turning on the upper FET. This causes current to flow through the output inductor and into the output capacitors and load according to the following equation:

$$
I=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{T}}{\mathrm{~L}}
$$

GATE(H) and the upper NFET remain on and inductor current ramps up until the initial pulse is terminated by either the PWM control loop or the overcurrent protection. This initial surge of in-rush current minimizes startup time, but avoids overstressing of the regulator's power components.

The PWM comparator will terminate the initial pulse if the regulator output exceeds the voltage on the COMP pin plus the 1.1 V PWM comparator offset before the voltage drop across the current sense resistor exceeds the current limit threshold voltage. In this case, the PWM control loop has achieved regulation and the initial pulse is then followed by a constant off time as programmed by the Coff capacitor.

The COMP capacitor will continue to slowly charge and the regulator output voltage will follow it, less the 1.1 V PWM offset, until it achieves the voltage programmed by the DAC's VID input. The Error Amp will then source or sink current to the COMP cap as required to maintain the correct regulator DC output voltage. Since the rate of increase of the COMP pin voltage is typically set much slower than the regulator's slew capability, inrush current, output voltage, and duty cycle all gradually increase from zero. (See Figures 10,11 , and 12).


Figure 10. Normal Startup ( $\mathbf{2 . 0} \mathbf{~ m s} / \mathrm{div}$ )


Channel 1 - Regulator Output Voltage ( $0.2 \mathrm{~V} / \mathrm{div}$ )
Channel 2 - Inductor Switching Node ( $5.0 \mathrm{~V} / \mathrm{div}$ )
Channel 3 - VCC (10 V/div)
Channel 4 - Regulator Input Voltage ( $5.0 \mathrm{~V} / \mathrm{div}$ )
Figure 11. Normal Startup Showing Initial Pulse Followed by Soft Start ( $20 \mu \mathrm{~s} / \mathrm{div}$ )


Channel 1 - Regulator Output Voltage ( $0.2 \mathrm{~V} /$ div)
Channel 2 - Inductor Switching Node (5.0 V/div)
Channel 3 - V CC ( $10 \mathrm{~V} /$ div)
Channel 4 - Regulator Input Voltage (5.0 V/div)
Figure 12. Pulse-By-Pulse Regulation During Soft Start ( $2.0 \mu \mathrm{~s} / \mathrm{div}$ )

If the voltage across the Current Sense resistor generates a voltage difference between the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ pins that exceeds the OVC Comparator Offset Voltage ( 86 mV typical), the Fault latch is set. This causes the COMP pin to be quickly discharged, turning off GATE $(\mathrm{H})$ and the upper NFET since the voltage on the COMP pin is now less than the 1.1 V PWM comparator offset. The Fault latch is reset when the voltage on the COMP decreases below the discharge threshold voltage ( 0.25 V typical). The COMP capacitor will again begin to charge, and when it exceeds the 1.1 V PWM comparator offset, the regulator output will Soft Start normally (see Figure 13).


Channel 1 - Regulator Output Voltage ( $1.0 \mathrm{~V} / \mathrm{div}$ )
Channel 2 - COMP Pin (1.0 V/div)
Channel 3 - $\mathrm{V}_{\mathrm{CC}}$ ( $10 \mathrm{~V} /$ div)
Channel 4 - Regulator Input Voltage (5.0 V/div)
Figure 13. Startup with COMP Pre-Charge to 2.0 V ( $2.0 \mathrm{~ms} / \mathrm{div}$ )

Because the start-up circuitry depends on the current sense function, a current sense resistor should always be used.

When driving large capacitive loads, the COMP must charge slowly enough to avoid tripping the CS51313 overcurrent protection. The following equation can be used to ensure unconditional startup:

$$
\frac{I_{C H G}}{\mathrm{C}_{\mathrm{COMP}}}<\frac{\mathrm{ILIM}-\mathrm{I}_{\mathrm{LOAD}}}{\mathrm{COUT}}
$$

where:
$\mathrm{I}_{\mathrm{CHG}}=$ COMP Source Current ( $30 \mu \mathrm{~A}$ typical);
$\mathrm{C}_{\text {COMP }}=$ COMP Capacitor value ( $0.1 \mu \mathrm{~F}$ typical);
$\mathrm{I}_{\text {LIM }}=$ Current Limit Threshold;
$\mathrm{I}_{\text {LOAD }}=$ Load Current during startup;
Cout $=$ Total Output Capacitance .

## Normal Operation

During normal operation, Switch Off-Time is constant and set by the C OFF capacitor. Switch On-Time is adjusted by the $\mathrm{V}^{2}$ Control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current and the ESR of the output capacitors

## Transient Response

The CS51313 V ${ }^{2}$ Control Loop's 200 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse-by-pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called "Adaptive Voltage Positioning." This technique pre-positions the output voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to $1.0 \%$ allows the error amplifiers reference voltage to be targeted +25 mV high without compromising DC accuracy. A "Droop Resistor," implemented through a PC board trace, connects the Error Amps feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ) to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +25 mV offset. When the full load current is delivered, a 50 mV drop is developed across this resistor. This results in output voltage being offset -25 mV low.

The result of Adaptive Voltage Positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output is pre-positioned +25 mV . Conversely, when load current suddenly decreases from its maximum level, the output is pre-positioned -25 mV . For best Transient

Response, a combination of a number of high frequency and bulk output capacitors are usually used.

## Slope Compensation

The $\mathrm{V}^{2}$ control method uses a ramp signal, generated by the ESR of the output capacitors, that is proportional to the ripple current through the inductor. To maintain regulation, the $\mathrm{V}^{2}$ control loop monitors this ramp signal, through the PWM comparator, and terminates the switch on-time.

The stringent load transient requirements of modern microprocessors require the output capacitors to have very low ESR. The resulting shallow slope presented to the PWM comparator, due to the very low ESR, can lead to pulse width jitter and variation caused by both random or synchronous noise.

Adding slope compensation to the control loop, avoids erratic operation of the PWM circuit, particularly at lower duty cycles and higher frequencies, where there is not enough ramp signal, and provides a more stable switchpoint.

The scheme that prevents that switching noise prematurely triggers the PWM circuit consists of adding a positive voltage slope to the output of the Error Amplifier (COMP pin) during an off-time cycle.

The circuit that implements this function is shown in Figure 14.


Figure 14. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On-Time Cycle

The ramp waveform is generated through a small RC filter that provides the proper voltage ramp at the beginning of each on-time cycle. The resistors R1 and R2 in the circuit of Figure 14 form a voltage divider from the GATE(L) output, superimposing a small artificial ramp on the output of the error amplifier. It is important that the series combination $\mathrm{R} 1 / \mathrm{R} 2$ is high enough in resistance not to load down and negatively affect the slew rate on the GATE(L) pin.

## PROTECTION AND MONITORING FEATURES

## Overcurrent Protection

A loss-less hiccup mode current limit protection feature is provided, requiring only the COMP capacitor to implement. The CS51313 provides overcurrent protection by sensing the current through a "Droop" resistor, using an internal current sense comparator. The comparator
compares the voltage drop across the "Droop" resistor to an internal reference voltage of 86 mV (typical).

If the voltage drop across the "Droop" resistor exceeds this threshold, the current sense comparator allows the fault latch to be set. This causes the regulator to stop switching.

During this over current condition, the CS51313 stays off for the time it takes the COMP pin capacitor to discharge to its lower 0.25 V threshold. As soon as the COMP pin reaches 0.25 V , the Fault latch is reset (no overcurrent condition present) and the COMP pin is charged with a $30 \mu \mathrm{~A}$ current source to a voltage 1.1 V greater than the $\mathrm{V}_{\mathrm{FB}}$ voltage. Only at this point the regulator attempts to restart normally. The CS51313 will operate initially with a duty cycle whose value depends on how low the $\mathrm{V}_{\mathrm{FB}}$ voltage was during the overcurrent condition (whether hiccup mode was due to excessive current or hard short). This protection scheme minimizes thermal stress to the regulator components, input power supply, and PC board traces, as the over current condition persists. Upon removal of the overload, the fault latch is cleared, allowing normal operation to resume.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $\mathrm{V}^{2}$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns , causing the top MOSFET to shut off, disconnecting the regulator from its input voltage. This results in a "crowbar" action to clamp the output voltage and prevents damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. Additionally, a dedicated Overvoltage protection (OVP) output pin (pin 13) is provided in the CS51313. The OVP signal will go high (overvoltage condition), if the output voltage ( $\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}$ ) exceeds the regulation voltage by $8.5 \%$ of the voltage set by the particular DAC code. The OVP pin can source up to 25 mA of current that can be used to drive an SCR to crowbar the power supply.

## Power Good Circuit

The Power Good pin (pin 14) is an open-collector signal consistent with TTL DC specifications. It is externally pulled up, and is pulled low (below 0.3 V ) when the regulator output voltage typically exceeds $\pm 8.5 \%$ of the nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is $\pm 12 \%$.

## Output Enable

On/off control of the regulator outputs can be implemented by pulling the COMP pins low. It is required to pull the COMP pins below the 1.1 V PWM comparator offset voltage in order to disable switching on the GATE drivers.

## CS51313-BASED V CC(CORE) $^{\text {BUCK REGULATOR }}$ DESIGN EXAMPLE

## Step 1: Definition of the Design Specifications

In computer motherboard applications the input voltage comes from the "silver box" power supply. $5.0 \mathrm{~V} \pm 5.0 \%$ is used for conversion to output voltage, and $12 \mathrm{~V} \pm 5.0 \%$ is used for the external NFET gate voltage and circuit bias. The CPU $\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}$ tolerance can be affected by any or all of the following reasons:
1.buck regulator output voltage setpoint accuracy;
2.output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3.output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4.output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide a $\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}$ that will meet the specified tolerance at the CPU's inputs.
The designer must also ensure that the regulator component junction temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature. As computer motherboards become increasingly complex, regulator size also becomes important, as there is less space available for the CPU power supply.

## Step 2: Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.
In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{I} \text { OUT } \times\left(\frac{\mathrm{ESL}}{\Delta \mathrm{t}}+\mathrm{ESR}+\frac{\mathrm{tTR}}{\mathrm{COUT}}\right)
$$

where:
$\Delta \mathrm{I}_{\text {OUT }} / \Delta \mathrm{t}=$ load current slew rate;
$\Delta \mathrm{I}_{\text {OUT }}=$ load transient;
$\Delta \mathrm{t}=$ load transient duration time;
$\mathrm{ESL}=$ Maximum allowable ESL including capacitors, circuit traces, and vias;
ESR = Maximum allowable ESR including capacitors and circuit traces;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time.
The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESR}}}{\Delta \mathrm{I}_{\mathrm{OUT}}}
$$

where $\Delta \mathrm{V}_{\mathrm{ESR}}=$ change in output voltage due to ESR (assigned by the designer).

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where:
$E S R_{\text {CAP }}=$ maximum ESR per capacitor (specified in manufacturer's data sheet);
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR.
The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$
\Delta \mathrm{V}_{\mathrm{ESR}}=\Delta \mathrm{l} \text { OUT } \times \mathrm{ESR}_{\mathrm{MAX}}
$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$
\mathrm{ESL}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{ESL}} \times \Delta \mathrm{t}}{\Delta \mathrm{l}}
$$

where:
$\Delta \mathrm{I} / \Delta \mathrm{T}=$ load current slew rate (as high as $20 \mathrm{~A} / \mu \mathrm{s}$ );
$\Delta \mathrm{V}_{\mathrm{ESL}}=$ change in output voltage due to ESL .
The actual maximum allowable ESL can be determined by using the equation:

$$
\text { ESL MAX }=\frac{\text { ESLCAP }}{\text { Number of output capacitors }}
$$

where $\mathrm{ESL}_{\mathrm{CAP}}=$ maximum ESL per capacitor (it is estimated that a $10 \times 12 \mathrm{~mm}$ Aluminum Electrolytic capacitor has approximately 4.0 nH of package inductance).

The actual output voltage deviation due to the actual maximum ESL can then be verified:

$$
\Delta \mathrm{V}_{\mathrm{ESL}}=\frac{\mathrm{ESL}}{\mathrm{MAX} \times \Delta \mathrm{I}} \text { }
$$

The designer now must determine the change in output voltage due to output capacitor discharge during the transient:

$$
\Delta \mathrm{V}_{\mathrm{CAP}}=\frac{\Delta \mathrm{I} \times \Delta \mathrm{t} \mathrm{TR}}{\mathrm{COUT}}
$$

where:
$\Delta \mathrm{t}_{\mathrm{TR}}=$ the output voltage transient response time (assigned by the designer);
$\Delta \mathrm{V}_{\mathrm{CAP}}=$ output voltage deviation due to output capacitor discharge;
$\Delta \mathrm{I}=$ Load step.
The total change in output voltage as a result of a load current transient can be verified by the following formula:

$$
\Delta \mathrm{V}_{\mathrm{OUT}}=\Delta \mathrm{V}_{\mathrm{ESR}}+\Delta \mathrm{V}_{\mathrm{ESL}}+\Delta \mathrm{V}_{\mathrm{CAP}}
$$

## Step 3: Selection of the Duty Cycle, Switching Frequency, Switch On-Time ( $\mathrm{T}_{\mathrm{ON}}$ ) and Switch Off-Time (TOFF)

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$
\text { Duty Cycle }=\mathrm{D}=\frac{\mathrm{V}_{\mathrm{OUT}}+\left(\mathrm{V}_{\mathrm{HFET}}+\mathrm{V}_{\mathrm{L}}+\mathrm{V}_{\mathrm{DROOP}}\right)}{\mathrm{V}_{\mathrm{IN}}+\mathrm{V}_{\mathrm{LFET}}-\mathrm{V}_{\mathrm{HFET}}-\mathrm{V}_{\mathrm{L}}}
$$

where:
$\mathrm{V}_{\text {OUT }}=$ buck regulator output voltage;
$\mathrm{V}_{\text {HFET }}=$ high side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$;
$\mathrm{V}_{\mathrm{L}}=$ output inductor voltage drop due to inductor wire DC resistance;
$\mathrm{V}_{\text {DROOP }}=$ droop (current sense) resistor voltage drop;
$\mathrm{V}_{\mathrm{IN}}=$ buck regulator input voltage;
$\mathrm{V}_{\mathrm{LFET}}=$ low side FET voltage drop due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$.

## Step3a: Calculation of Switch On-Time

The Switch On-Time (time during which the switching MOSFET in a synchronous buck topology is conducting) is determined by:

$$
\text { TON }=\frac{\text { Duty Cycle }}{\text { FSW }}
$$

where $\mathrm{F}_{\mathrm{SW}}=$ regulator switching frequency selected by the designer.

Higher operating frequencies allow the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

## Step 3b: Calculation of Switch Off-Time

The Switch Off-Time (time during which the switching MOSFET is not conducting) can be determined by:

$$
\text { TOFF }=\frac{1.0}{\text { FSW }}-\mathrm{TON}
$$

The C CoFF capacitor value has to be selected in order to set the Off-Time, $\mathrm{T}_{\text {OFF }}$, above:

$$
\text { COFF }=\frac{\text { Period } \times(1.0-D)}{3980}
$$

where:
3980 is a characteristic factor of the CS51313; D = Duty Cycle .

## Step 4: Selection of the Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due to their high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The inductor value can be determined by:

$$
\mathrm{L}=\frac{\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{t} \mathrm{TR}}{\Delta \mathrm{I}}
$$

where:
$\mathrm{V}_{\mathrm{IN}}=$ input voltage;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{t}_{\mathrm{TR}}=$ output voltage transient response time (assigned by the designer);
$\Delta \mathrm{I}=$ load transient.
The inductor ripple current can then be determined:

$$
\Delta \mathrm{I}_{\mathrm{L}}=\frac{\mathrm{V} \mathrm{OUT} \times \mathrm{TOFF}}{\mathrm{~L}}
$$

where:
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage;
$\mathrm{T}_{\mathrm{OFF}}=$ switch Off-Time;
$\mathrm{L}=$ inductor value.
The designer can now verify if the number of output capacitors from Step 2 will provide an acceptable output voltage ripple ( $1.0 \%$ of output voltage is common). The formula below is used:

$$
\Delta l_{\mathrm{L}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\mathrm{ESR} \mathrm{MAX}^{2}}
$$

Rearranging we have:

$$
\mathrm{ESR}_{\mathrm{MAX}}=\frac{\Delta \mathrm{V}_{\mathrm{OUT}}}{\Delta \mathrm{I}_{\mathrm{L}}}
$$

where
$\mathrm{ESR}_{\mathrm{MAX}}=$ maximum allowable ESR;
$\Delta \mathrm{V}_{\text {OUT }}=1.0 \% \times \mathrm{V}_{\text {OUT }}=$ maximum allowable output voltage ripple ( budgeted by the designer );
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current;
$\mathrm{V}_{\text {OUT }}=$ output voltage.

The number of output capacitors is determined by:

$$
\text { Number of capacitors }=\frac{\text { ESRCAP }}{\text { ESRMAX }}
$$

where $\mathrm{ESR}_{\mathrm{CAP}}=$ maximum ESR per capacitor (specified in manufacturer's data sheet).
The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$
\mathrm{IL}(\mathrm{PEAK})=\mathrm{IOUT}+\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2.0}
$$

where:
$\mathrm{I}_{\mathrm{L}(\text { PEAK })}=$ inductor peak current;
$\mathrm{I}_{\text {OUT }}=$ load current;
$\Delta \mathrm{I}_{\mathrm{L}}=$ inductor ripple current.

$$
\mathrm{IL}(\text { VALLEY })=\mathrm{IOUT}-\frac{\Delta \mathrm{I}_{\mathrm{L}}}{2.0}
$$

where $\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current.
Given the requirements of an application such as a buck converter, it is found that a toroid powdered iron core is quite suitable due to its low cost, low core losses at the switching frequency, and low EMI.

## Step 5: Selection of the Input Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines. A key specification for input capacitors is their ripple current rating. The input capacitor should also be able to handle the input RMS current $\mathrm{I}_{\mathrm{IN}(\mathrm{RMS})}$.
The combination of the input capacitors $\mathrm{C}_{\text {IN }}$ discharges during the on-time.
The input capacitor discharge current is given by:

$$
\begin{aligned}
& \operatorname{ICINDIS(RMS)}= \\
& \sqrt{\frac{\left(\begin{array}{l}
\mathrm{I}(\mathrm{PEAK})^{2} \\
+\left(I_{L(P E A K)} \times I_{L(V A L L E Y)}\right) \\
+\mathrm{I}_{\mathrm{L}(\mathrm{VALLEY})^{2}}
\end{array}\right) \times \mathrm{D}}{3.0}}
\end{aligned}
$$

where:
$\mathrm{I}_{\mathrm{CINDIS}(\mathrm{RMS})}=$ input capacitor discharge current;
$\mathrm{I}_{\mathrm{L}(\mathrm{PEAK})}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\text { VALLEY })}=$ inductor valley current.
$\mathrm{C}_{\mathrm{IN}}$ charges during the off-time, the average current through the capacitor over one switching cycle is zero:

$$
\operatorname{ICIN}(C H)=\operatorname{ICIN}(\mathrm{DIS}) \times \frac{D}{1.0-\mathrm{D}}
$$

where:
$\mathrm{I}_{\mathrm{CIN}(\mathrm{CH})}=$ input capacitor charge current;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{DIS})}=$ input capacitor discharge current;
D = Duty Cycle.
The total Input RMS current is:

$$
\operatorname{ICIN(RMS)}=\sqrt{\begin{array}{l}
\left(\mathrm{ICIN}(\mathrm{DIS})^{2} \times \mathrm{D}\right) \\
+\left(\mathrm{ICIN}(\mathrm{CH})^{2} \times(1.0-\mathrm{D})\right)
\end{array}}
$$

The number of input capacitors required is then determined by:

$$
\mathrm{N}_{\mathrm{CIN}}=\frac{\mathrm{ICIN(RMS)}}{\operatorname{IRIPPLE}}
$$

where:
$\mathrm{N}_{\text {CIN }}=$ number of input capacitors;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{I}_{\text {RIPPLE }}=$ input capacitor ripple current rating (specified in manufacturer's data sheets).

The total input capacitor ESR needs to be determined in order to calculate the power dissipation of the input capacitors:

$$
\mathrm{ESR}_{\mathrm{CIN}}=\frac{\mathrm{ESR} \mathrm{CAP}}{\mathrm{~N}_{\mathrm{CIN}}}
$$

where:
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR;
$E S R_{\text {CAP }}=$ maximum ESR per capacitor (specified in manufacturer's data sheets);
$\mathrm{N}_{\mathrm{CIN}}=$ number of input capacitors.
Once the total ESR of the input capacitors is known, the input capacitor ripple voltage can be determined using the formula:

$$
\mathrm{V}_{\mathrm{CIN}(\mathrm{RMS})}=\operatorname{ICIN(RMS)} \times \mathrm{ESR}_{\mathrm{CIN}}
$$

where:
$\mathrm{V}_{\mathrm{CIN}(\mathrm{RMS})}=$ input capacitor RMS voltage;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR.
The designer must determine the input capacitor power loss in order to ensure there isn't excessive power dissipation through these components. The following formula is used:

$$
\operatorname{PCIN}(\mathrm{RMS})=\operatorname{ICIN}(\mathrm{RMS})^{2} \times \operatorname{ESRCIN}
$$

where:
$\mathrm{P}_{\mathrm{CIN}(\mathrm{RMS})}=$ input capacitor RMS power dissipation;
$\mathrm{I}_{\mathrm{CIN}(\mathrm{RMS})}=$ total input RMS current;
$\mathrm{ESR}_{\mathrm{CIN}}=$ total input capacitor ESR.

## Step 6: Selection of the Input Inductor

A CPU switching regulator, such as the one in a buck topology, must not disturb the primary +5.0 V supply. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the +5.0 V supply from the noise generated in the switching portion of the microprocessor buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the CPU load changes from no load to full load (load step), a condition under which the highest voltage
change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.
The minimum inductance value for the input inductor is therefore:

$$
\operatorname{LIN}=\frac{\Delta V}{(\mathrm{~d} / / \mathrm{dt}) \mathrm{MAX}}
$$

where:
$\mathrm{L}_{\mathrm{IN}}=$ input inductor value;
$\Delta \mathrm{V}=$ voltage seen by the input inductor during a full load swing;
$(\mathrm{dI} / \mathrm{dt})_{\mathrm{MAX}}=$ maximum allowable input current slew rate ( $0.1 \mathrm{~A} / \mu \mathrm{s}$ for a Pentium II power supply).
The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double-pole network with a slope of -2 , a roll-off rate of $-40 \mathrm{~dB} / \mathrm{dec}$, and a corner frequency:

$$
\mathrm{f}_{\mathrm{C}}=\frac{1.0}{2.0 \pi \sqrt{\mathrm{LC}}}
$$

where:
$\mathrm{L}=$ input inductor;
$\mathrm{C}=$ input capacitor(s).

## Step 7: Selection of the Switching FET FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) Its very high input impedance; and 2) Its very fast switching times. The electrical characteristics of a MOSFET are considered to be those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of $\mathrm{V}_{\mathrm{GS}}$, and the faster the turn-on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3 ) turn-on switching losses, 4) turn-off switching losses, and 5) gate-transitions losses. The latter three losses are proportional to frequency. For the conducting power dissipation rms values of current and resistance are used for true power calculations. The fast switching speed of the MOSFET makes it indispensable for high-frequency power supply applications. Not only are switching power losses minimized, but also the maximum usable switching frequency is considerably higher. Switching time is independent of temperature. Also, at higher frequencies, the use of smaller and lighter components (transformer, filter choke, filter capacitor) reduces overall component cost while using less space for more efficient packaging at lower weight.
The MOSFET has purely capacitive input impedance. No DC current is required. It is important to keep in mind the
drain current of the FET has a negative temperature coefficient. Increase in temperature causes higher on-resistance and greater leakage current. For switching circuits, $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}$ should be low to minimize power dissipation at a given ID , and $\mathrm{V}_{\mathrm{GS}}$ should be high to accomplish this. MOSFET switching times are determined by device capacitance, stray capacitance, and the impedance of the gate drive circuit. Thus the gate driving circuit must have high momentary peak current sourcing and sinking capability for switching the MOSFET. The input capacitance, output capacitance and reverse-transfer capacitance also increase with increased device current rating.

Two considerations complicate the task of estimating switching times. First, since the magnitude of the input capacitance, $\mathrm{C}_{\mathrm{ISS}}$, varies with $\mathrm{V}_{\mathrm{DS}}$, the RC time constant determined by the gate-drive impedance and $\mathrm{C}_{\text {ISS }}$ changes during the switching cycle. Consequently, computation of the rise time of the gate voltage by using a specific gate-drive impedance and input capacitance yields only a rough estimate. The second consideration is the effect of the "Miller" capacitance, $\mathrm{C}_{\text {RSS }}$, which is referred to as $\mathrm{C}_{\mathrm{DG}}$ in the following discussion. For example, when a device is on, $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}$ is fairly small and $\mathrm{V}_{\mathrm{GS}}$ is about $12 \mathrm{~V} . \mathrm{C}_{\mathrm{DG}}$ is charged to $\mathrm{V}_{\mathrm{DS}(\mathrm{ON})}-\mathrm{V}_{\mathrm{GS}}$, which is a negative potential if the drain is considered the positive electrode. When the drain is "off," $\mathrm{C}_{\mathrm{DG}}$ is charged to quite a different potential. In this case the voltage across $C_{D G}$ is a positive value since the potential from gate-to-source is near zero volts and $\mathrm{V}_{\mathrm{DS}}$ is essentially the drain supply voltage. During turn-on and turn-off, these large swings in gate-to-drain voltage tax the current sourcing and sinking capabilities of the gate drive. In addition to charging and discharging $\mathrm{C}_{\mathrm{GS}}$, the gate drive must also supply the displacement current required by $C_{\text {DG }}\left(I_{\text {GATE }}=C_{\text {DG }} \mathrm{dV}_{\mathrm{DG}} / \mathrm{dt}\right)$. Unless the gate-drive impedance is very low, the $\mathrm{V}_{\mathrm{GS}}$ waveform commonly plateaus during rapid changes in the drain-to-source voltage.

The most important aspect of FET performance is the Static Drain-To-Source On-Resistance ( $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ ), which effects regulator efficiency and FET thermal management requirements. The On-Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On-Resistance also increases. Its positive temperature coefficient is between $+0.6 \% / \mathrm{C}$ and $+0.85 \% / \mathrm{C}$. The higher the On-Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used. The reference designs derive gate drive from the 12 V supply, which is generally available in most computer systems and utilizes logic level FETs.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail-to-rail due to overshoot caused by the capacitive load they present to the controller IC.

## Step 7a: Selection of the Switching (Upper) FET

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed $150^{\circ} \mathrm{C}$.

The maximum RMS current through the switch can be determined by the following formula:

$$
\operatorname{IRMS}(\mathrm{H})=
$$


where:
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{I}_{\mathrm{L}(\text { PEAK })}=$ inductor peak current;
$\mathrm{I}_{\mathrm{L}(\mathrm{VALLEY})}=$ inductor valley current;
D = Duty Cycle.
Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$
\mathrm{P}_{\mathrm{RMS}(\mathrm{H})}=\operatorname{IRMS}(\mathrm{H})^{2} \times \mathrm{RDS}_{\mathrm{DS}(\mathrm{ON})}
$$

where:
$\mathrm{P}_{\mathrm{RMS}(\mathrm{H})}=$ switching MOSFET conduction losses;
$\mathrm{I}_{\mathrm{RMS}(\mathrm{H})}=$ maximum switching MOSFET RMS current;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=\mathrm{FET}$ drain-to-source on-resistance
The upper MOSFET switching losses are caused during MOSFET switch-on and switch-off and can be determined by using the following formula:

$$
\begin{aligned}
\mathrm{PSWH} & =\mathrm{PSWH}(\mathrm{ON})+\mathrm{PSWH}_{\mathrm{SW}}(\mathrm{OFF}) \\
& =\frac{\mathrm{V}_{\mathrm{IN}} \times \mathrm{IOUT} \times\left(\mathrm{t} \text { RISE }+\mathrm{t}_{\mathrm{OALL}}\right)}{6.0 \mathrm{~T}}
\end{aligned}
$$

where:
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses;
$\mathrm{V}_{\text {IN }}=$ input voltage;
IOUT = load current;
$\mathrm{t}_{\text {RISE }}=$ MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{t}_{\text {FALL }}=$ MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
$\mathrm{T}=1 / \mathrm{F}_{\mathrm{SW}}=$ period.
The total power dissipation in the switching MOSFET can then be calculated as:

PhFET $($ TOTAL $)=$ PRMSH + PSWH $(O N)+$ PSWH $(O F F)$
where:
$\mathrm{P}_{\text {HFET(TOTAL) }}=$ total switching (upper) MOSFET losses; $P_{\text {RMSH }}=$ upper MOSFET switch conduction Losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{ON})}=$ upper MOSFET switch-on losses;
$\mathrm{P}_{\mathrm{SWH}(\mathrm{OFF})}=$ upper MOSFET switch-off losses.
Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$
T_{J}=T_{A}+\left(\operatorname{PHFET}(T O T A L) \times R_{\theta J A}\right)
$$

where:
$\mathrm{T}_{\mathrm{J}}=\mathrm{FET}$ junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\mathrm{P}_{\mathrm{HFET}(\mathrm{TOTAL})}=$ total switching (upper) FET losses;
$\mathrm{R}_{\theta \mathrm{JIA}}=$ upper FET junction-to-ambient thermal resistance.

## Step 7b: Selection of the Synchronous (Lower) FET

The switch conduction losses for the lower FET can be calculated as follows:

$$
\begin{aligned}
\mathrm{PRMSL} & =\mathrm{I}_{\mathrm{RMS}^{2}} \times \mathrm{RDS}(\mathrm{ON}) \\
& =(\mathrm{IOUT} \times \sqrt{(1.0-\mathrm{D})})^{2} \times \mathrm{RDS}(\mathrm{ON})
\end{aligned}
$$

where:
$\mathrm{P}_{\text {RMSL }}=$ lower MOSFET conduction losses;
Iout = load current;
D = Duty Cycle;
$\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=$ lower FET drain-to-source on-resistance.
The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non-overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$
\text { PSWL }=V_{S D} \times \text { ILOAD } \times \text { non-overlap time } \times \text { FSW }
$$

where:
$\mathrm{P}_{\mathrm{SWL}}=$ lower FET switching losses;
$\mathrm{V}_{\mathrm{SD}}=$ lower FET source-to-drain voltage;
$\mathrm{I}_{\text {LOAD }}=$ load current
Non-overlap time $=$ GATE(L)-to-GATE(H) or GATE(H)-to-GATE(L) delay (from CS51313 data sheet Electrical Characteristics section);
$\mathrm{F}_{\mathrm{SW}}=$ switching frequency.
The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$
\text { PLFET(TOTAL) }=\text { PRMSL }+ \text { PSWL }
$$

where:
$\mathrm{P}_{\text {LFET(TOTAL) }}=$ Synchronous (lower) FET total losses;
$\mathrm{P}_{\text {RMSL }}=$ Switch Conduction Losses;
$P_{\text {SWL }}=$ Switching losses.
Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$
\mathrm{T}_{\mathrm{J}}=\mathrm{T}_{\mathrm{A}}+\left(\text { PLFET }(\mathrm{TOTAL}) \times \mathrm{R}_{\theta \mathrm{JA}}\right)
$$

where:
$\mathrm{T}_{\mathrm{J}}=$ MOSFET junction temperature;
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature;
$\mathrm{P}_{\text {LFET(TOTAL) }}=$ total synchronous (lower) FET losses;
$\mathrm{R}_{\theta J \mathrm{~A}}=$ lower FET junction-to-ambient thermal resistance.

## Step 8: Control IC Power Dissipation

The power dissipation of the IC varies with the MOSFETs used, $\mathrm{V}_{\mathrm{CC}}$, and the CS51313 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.
The IC power dissipation is determined by the formula:

$$
\text { PCONTROLIC }=\operatorname{ICCVCC}+\operatorname{PGATE}(\mathrm{H})+\operatorname{PGATE}(\mathrm{L})
$$

where:
$\mathrm{P}_{\text {CONTROLIC }}=$ control IC power dissipation;
$\mathrm{I}_{\mathrm{CC}}=\mathrm{IC}$ quiescent supply current;
$\mathrm{V}_{\mathrm{CC}}=$ IC supply voltage;
$\mathrm{P}_{\mathrm{GATE}(\mathrm{H})}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{P}_{\text {GATE(L) }}=$ lower MOSFET gate driver (IC) losses.
The upper (switching) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(H)=Q_{\operatorname{GATE}(H)} \times \mathrm{FSW} \times \mathrm{V}_{\operatorname{GATE}(\mathrm{H})}
$$

where:
$\mathrm{P}_{\mathrm{GATE}(\mathrm{H})}=$ upper MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\text {GATE(H) }}=$ total upper MOSFET gate charge;
$\mathrm{F}_{\text {SW }}=$ switching frequency;
$\mathrm{V}_{\mathrm{GATE}(\mathrm{H})}=$ upper MOSFET gate voltage.
The lower (synchronous) MOSFET gate driver (IC) losses are:

$$
\operatorname{PGATE}(\mathrm{L})=Q_{G A T E}(\mathrm{~L}) \times \mathrm{FSW}_{\mathrm{SW}} \times \mathrm{V}_{\mathrm{GATE}}(\mathrm{~L})
$$

where:
$\mathrm{P}_{\mathrm{GATE}(\mathrm{L})}=$ lower MOSFET gate driver (IC) losses;
$\mathrm{Q}_{\mathrm{GATE}(\mathrm{L})}=$ total lower MOSFET gate charge;
$\mathrm{F}_{\text {SW }}=$ switching frequency;
$\mathrm{V}_{\text {GATE(L) }}=$ lower MOSFET gate voltage.
The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

## Step 9: Slope Compensation

Voltage regulators for today's advanced processors are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR at the CPU input supply pins. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that there's very little voltage ramp at the control IC feedback pin ( $\mathrm{V}_{\mathrm{FB}}$ ) and regulator sensitivity to noise and loop instability are two undesirable effects that can surface. The performance of the CS51313-based CPU V ${ }_{\text {CC(CORE) }}$ regulator is improved when a fixed amount of slope compensation is added to the
output of the PWM Error Amplifier (COMP pin) during the regulator Off-Time. Referring to Figure 14, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1and R2.

$$
\mathrm{V}_{\text {SLOPECOMP }}=\mathrm{V}_{\mathrm{GATE}}(\mathrm{~L}) \times\left(\frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}\right) \times\left(1.0-\mathrm{e}^{\frac{-\mathrm{t}}{\tau}}\right)
$$

where:
$\mathrm{V}_{\text {SLOPECOMP }}=$ amount of slope added;
$\mathrm{V}_{\text {GATE(L) }}=$ lower MOSFET gate voltage;
$\mathrm{R} 1, \mathrm{R} 2=$ voltage divider resistors;
$\mathrm{t}=\mathrm{t}_{\text {OFF }}$ (switch off-time);
$\tau=\mathrm{RC}$ constant determined by C 1 and the parallel combination of R1, R2 (Figure 14), neglecting the low driver output impedance

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off-time cycle duration (time during which the lower MOSFET is conducting).

## Step 10: Selection of Current Limit Filter Components

The current limit filter is implemented by a $0.1 \mu \mathrm{~F}$ ceramic capacitor across and two $510 \Omega$ resistors in series with the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ current limit comparator input pins. They provide a time constant $\tau=\mathrm{RC}=100 \mu \mathrm{~s}$, which enables the circuit to filter out noise and be immune to false triggering, caused by sudden and fast load changes. These load transients can have slew rates as high as $20 \mathrm{~A} / \mu \mathrm{s}$.

## "DROOP" RESISTOR FOR ADAPTIVE VOLTAGE POSITIONING AND CURRENT LIMIT

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met. An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation caused by variation in the thickness of the PCB layer; 2) the mismatch of L/W; and 3) temperature variation.

## 1) Sheet Resistivity

For one ounce copper, the thickness variation is typically 1.26 mil to 1.48 mil. Therefore the error due to sheet resistivity is:

$$
\frac{1.48-1.26}{1.37}= \pm 8.0 \%
$$

## 2) Mismatch Due to L/W

The variation in $\mathrm{L} / \mathrm{W}$ is governed by variations due to the PCB manufacturing process. The error due to $\mathrm{L} / \mathrm{W}$ mismatch is typically $1.0 \%$.

## 3) Thermal Considerations

Due to $I^{2} \times R$ power losses the surface temperature of the droop resistor will increase causing the resistance to increase. Also, the ambient temperature variation will contribute to the increase of the resistance, according to the formula:

$$
R=R_{20}\left[1.0+\alpha_{20}(T-20)\right]
$$

where:
$\mathrm{R}_{20}=$ resistance at $20^{\circ} \mathrm{C}$;
$\alpha=0.00393 /{ }^{\circ} \mathrm{C}$
$\mathrm{T}=$ operating temperature;
$\mathrm{R}=$ desired droop resistor value.
For temperature $\mathrm{T}=50^{\circ} \mathrm{C}$, the $\% \mathrm{R}$ change $=12 \%$.

## Droop Resistor Tolerance

Tolerance due to sheet resistivity variation $\pm 8.0 \%$
Tolerance due to L/W error $1.0 \%$
Tolerance due to temperature variation $12 \%$
Total tolerance for droop resistor $21 \%$
In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage at full load is above the minimum DC tolerance spec:

$$
\mathrm{V}_{\mathrm{DROOP}}(\mathrm{TYP})=\frac{\mathrm{V}_{\mathrm{DAC}}(\mathrm{MIN})-\mathrm{V}_{\mathrm{DC}}(\mathrm{MIN})}{1.0+\mathrm{RDROOP}(\text { TOLERANCE })}
$$

Example: for a 450 MHz Pentium II, the DC accuracy spec is $1.93<\mathrm{V}_{\mathrm{CC}(\text { CORE })}<2.07 \mathrm{~V}$, and the AC accuracy spec is $1.9 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}(\mathrm{CORE})}<2.1 \mathrm{~V}$. The CS51313 DAC output voltage is $+2.001 \mathrm{~V}<\mathrm{V}_{\mathrm{DAC}}<+2.049 \mathrm{~V}$. In order not to exceed the DC accuracy spec, the voltage drop developed across the resistor must be calculated as follows:

$$
\begin{aligned}
\mathrm{VDROOP}_{\text {(TYP })} & =\frac{\left(\mathrm{V} \operatorname{DAC}(\mathrm{MIN})-\mathrm{VDC}_{\mathrm{DIN}}\right)}{1.0+\mathrm{R}_{\mathrm{DROOP}}(\mathrm{TOLERANCE})} \\
& =\frac{+2.001 \mathrm{~V}-1.93 \mathrm{~V}}{1.21}=71 \mathrm{mV}
\end{aligned}
$$

With the CS51313 DAC accuracy being $1.0 \%$, the internal error amplifier's reference voltage is trimmed so that the output voltage will be 25 mV high at no load. With no load, there is no DC drop across the resistor, producing an output voltage tracking the error amplifier output voltage, including the offset. When the full load current is delivered, a drop of -50 mV is developed across the resistor. Therefore, the regulator output is pre-positioned at 25 mV above the nominal output voltage before a load turn-on. The total voltage drop due to a load step is $\Delta \mathrm{V}-25 \mathrm{mV}$ and the deviation from the nominal output voltage is 25 mV smaller than it would be if there was no droop resistor. Similarly at full load the regulator output is pre-positioned at 25 mV below the nominal voltage before a load turn-off. the total voltage increase due to a load turn-off is $\Delta \mathrm{V}-25 \mathrm{mV}$ and the deviation from the nominal output voltage is 25 mV smaller than it would be if there was no droop resistor. This is because the output capacitors are pre-charged to a value that is either 25 mV above the nominal output voltage before
a load turn-on or, 25 mV below the nominal output voltage before a load turn-off .

Obviously, the larger the voltage drop across the droop resistor (the larger the resistance), the worse the DC and load regulation, but the better the AC transient response.

## Current Limit

The current limit setpoint has to be higher than the normal full load current. Attention has to be paid to the current rating of the external power components as these are the first to fail during an overload condition. The MOSFET continuous and pulsed drain current rating at a given case temperature has to be accounted for when setting the current limit trip point.

Temperature curves on MOSFET manufacturers' data sheets allow the designer to determine the MOSFET drain current at a particular VGS and TJ (junction temperature). This, in turn, will assist the designer to set a proper current limit, without causing device breakdown during an overload condition.

Let's assume the full CPU load is 16A. The internal current sense comparator current limit voltage limits are: $77 \mathrm{mV}<\mathrm{V}_{\mathrm{TH}}<101 \mathrm{mV}$. Also, there is a $21 \%$ total variation in $\mathrm{R}_{\text {SENSE }}$ as discussed in the previous section.

We compute the value of the current sensing element (embedded PCB trace) for the minimum current limit setpoint:

$$
\begin{gathered}
\operatorname{RSENSE}(\mathrm{MIN})=\operatorname{RSENSE}(\mathrm{TYP}) \times 0.79 \\
\operatorname{RSENSE}(\mathrm{MAX})=\operatorname{RSENSE}(\mathrm{TYP}) \times 1.21 \\
\operatorname{RSENSE}^{(\mathrm{MAX})}=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{MIN})}}{\mathrm{ICL}(\mathrm{MIN})}=\frac{77 \mathrm{mV}}{16 \mathrm{~A}}=4.8 \mathrm{~m} \Omega
\end{gathered}
$$

We select,

$$
\text { RSENSE(TYP) }=3.3 \mathrm{~m} \Omega
$$

We calculate the range of load currents that will cause the internal current sense comparator to detect an overload condition.

## Nominal Current Limit Setpoint

From the overcurrent detection data in the electrical characteristics table:

$$
\begin{gathered}
\mathrm{V}_{\mathrm{TH}(\mathrm{TYP})}=86 \mathrm{mV} \\
\mathrm{I}_{\mathrm{CL}(\mathrm{NOM})}=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{TYP})}}{\operatorname{RSENSE}(\mathrm{NOM})}=\frac{86 \mathrm{mV}}{3.3 \mathrm{~m} \Omega}=26 \mathrm{~A}
\end{gathered}
$$

## Maximum Current Limit Setpoint

From the overcurrent detection data in the electrical characteristics table:

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{TH}}(\mathrm{MAX})=101 \mathrm{mV} \\
& \mathrm{I}_{\mathrm{CL}(\mathrm{MAX})}= \frac{\mathrm{V}_{\mathrm{TH}(\mathrm{MAX})}}{\operatorname{RSENSE}(\mathrm{MIN})}=\frac{\mathrm{V}_{\mathrm{TH}(\mathrm{MAX})}}{\operatorname{RSENSE}(\mathrm{NOM}) \times 0.79} \\
&=\frac{101 \mathrm{mV}}{3.3 \mathrm{~m} \Omega \times 0.79}=38.7 \mathrm{~A}
\end{aligned}
$$

Therefore, the range of load currents that will cause the internal current sense comparator to detect an overload condition through a $3.3 \mathrm{~m} \Omega$ embedded PCB trace is: 19.3 A $<\mathrm{I}_{\mathrm{CL}}<38.7 \mathrm{~A}$, with 26 A being the nominal overload condition.

## Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$
R_{A R}=\rho \times \frac{L}{A} \text { or } R=\rho \times \frac{L}{(W \times t)}
$$

where:
$\mathrm{A}=\mathrm{W} \times \mathrm{t}=$ cross-sectional area;
$\rho=$ the copper resistivity ( $\mu \Omega$-mil);
$\mathrm{L}=$ length (mils);
$\mathrm{W}=$ width (mils);
$\mathrm{t}=$ thickness (mils).
For most PCBs the copper thickness, t , is $35 \mu \mathrm{~m}(1.37$ mils) for one ounce copper; $\rho=717.86 \mu \Omega-$ mil.

For a CPU load of 16 A the resistance needed to create a 50 mV drop at full load is:

$$
\text { RDROOP }=\frac{50 \mathrm{mV}}{\mathrm{IOUT}}=\frac{50 \mathrm{mV}}{16 \mathrm{~A}}=3.1 \mathrm{~m} \Omega
$$

The resistivity of the copper will drift with the temperature according to the following guidelines:

$$
\begin{aligned}
& \Delta R=12 \% @ T_{A}=+50^{\circ} \mathrm{C} \\
& \Delta R=34 \% @ T_{A}=+100^{\circ} \mathrm{C}
\end{aligned}
$$

## Droop Resistor Length, Width, and Thickness

The minimum width and thickness of the droop resistor should primarily be determined on the basis of the current-carrying capacity required, and the maximum permissible droop resistor temperature rise. PCB manufacturer design charts can be used in determining current-carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.

For single conductor applications, such as the use of the droop resistor, PCB design charts show that for a droop resistor with a required current-carrying capacity of 16 A , and a $45^{\circ} \mathrm{C}$ temperature rise above ambient, the recommended cross section is $275 \mathrm{mil}^{2}$.

$$
\mathrm{W} \times \mathrm{t}=275 \mathrm{mil} 2
$$

where:
$\mathrm{W}=$ droop resistor width;
$\mathrm{t}=$ droop resistor thickness.
For 1 oz . copper, $\mathrm{t}=1.37 \mathrm{mils}$, therefore $\mathrm{W}=201 \mathrm{mils}=$ 0.201 in .

$$
R=\rho \times \frac{L}{W \times t}
$$

where:
$\mathrm{R}=$ droop resistor value;
$\rho=0.71786 \mathrm{~m} \Omega-\mathrm{mil}(1 \mathrm{oz}$. copper);
$\mathrm{L}=$ droop resistor length;
$\mathrm{W}=$ droop resistor width.

$$
\begin{gathered}
\text { RDROOP }=3.3 \mathrm{~m} \Omega \\
3.3 \mathrm{~m} \Omega=0.71786 \mathrm{~m} \Omega-\mathrm{mil} \times \frac{\mathrm{L}}{201 \mathrm{mils} \times 1.37 \mathrm{mils}}
\end{gathered}
$$

Hence, $L=1265$ mils $=1.265$ in.
In layouts where it is impractical to lay out a droop resistor in a straight line 1265 mils long, the embedded PCB trace can be "snaked" to fit within the available space.

## THERMAL MANAGEMENT

## Thermal Considerations for Power MOSFETs

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of $150^{\circ} \mathrm{C}$ or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$
\text { Thermal Impedance }=\frac{\mathrm{T}_{\mathrm{J}}(\mathrm{MAX})-\mathrm{T}_{\mathrm{A}}}{\text { Power }}
$$

A heatsink may be added to TO-220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

## LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS51313.
1.Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3.Avoid ground loops as they pick up noise. Use star or single point grounding.
4.For high power buck regulators on double-sided PCBs a single ground plane (usually the bottom) is recommended.
5.Even though double sided PCBs are usually sufficient for a good layout, four-layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layer for the noise sensitive traces.
6.Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7.The MOSFET gate traces to the IC must be as short, straight, and wide as possible.
8.Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9.Place the switching MOSFET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}$ filter resistors $(510 \Omega)$ in series with the $V_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ pins as close as possible to the pins.
12. Place the CofF and COMP capacitors as close as possible to the $\mathrm{C}_{\mathrm{OFF}}$ and COMP pins.
13. Place the current limit filter capacitor between the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$ pins, as close as possible to the pins.
14. Connect the filter components of the following pins: $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{OUT}}, \mathrm{C}_{\mathrm{OFF}}$, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
15. The "Droop" Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
16. Place the $\mathrm{V}_{\mathrm{CC}}$ bypass capacitor as close as possible to the IC.

PACKAGE THERMAL DATA

| Parameter |  | SO-16 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 28 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 115 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5301

## Three-Phase <br> Buck Controller with Integrated Gate Drivers and Power Good

The CS5301 is a three-phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi-phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced V ${ }^{2 T M}$ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use.

The CS5301 multi-phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in inductor values and a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

## Features

- Enhanced $\mathrm{V}^{2}$ Control Method
- 5-Bit DAC with 1\% Accuracy
- Adjustable Output Voltage Positioning
- 6 On-Board Gate Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors, Sense Resistors, or V-S Control
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On-Board Current Sense Amplifiers
- $3.3 \mathrm{~V}, 1.0 \mathrm{~mA}$ Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through COMP Pin)
- Power Good Output

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5301GDW32 | SO-32L | 22 Units/Rail |
| CS5301GDWR32 | SO-32L | 1000 Tape \& Reel |



Figure 1. Application Diagram for Intel Pentium ${ }^{8} 4$ Processor 12 V to 1.7 V, 42 A

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Thermal Resistance, Junction-to-Case, R @JC |  | 14 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Ambient, R @JA |  | 70 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power for Logic | $\mathrm{V}_{\text {CCL }}$ | 16 V | -0.3 V | N/A | 70 mA DC |
| Power Good Sense | PWRGDS | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | 1.0 mA | 20 mA |
| Return for Logic | LGND | N/A | N/A | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Power for Gate(L)1 | $\mathrm{V}_{\text {CCL1 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for Gate(L)2 and Gate(L)3 | $\mathrm{V}_{\text {CCL23 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for Gate(H)1 and Gate(H)2 | $\mathrm{V}_{\mathrm{CCH} 12}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for Gate(H)3 | $\mathrm{V}_{\mathrm{CCH} 3}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Voltage Feedback Compensation Network | COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Input | $V_{F B}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Output for Adjusting Adaptive Voltage Positioning | $\mathrm{V}_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Frequency Resistor | Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Reference Output | REF | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| High Side FET Drivers | GH1-3 | 20 V | $\begin{aligned} & -0.3 \mathrm{~V} \mathrm{DC} \\ & -2.0 \mathrm{~V} \text { for } \\ & 100 \mathrm{~ns} \end{aligned}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Low Side FET Drivers | GL1-3 | 16 V | $\begin{aligned} & -0.3 \mathrm{~V} \mathrm{DC} \\ & -2.0 \mathrm{~V} \text { for } \\ & 100 \mathrm{~ns} \end{aligned}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Return for \#1 Driver | GND1 | 0.3 V | -0.3 V | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Return for \#2 Driver | GND2 | 0.3 V | -0.3 V | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Return for \#3 Driver | GND3 | 0.3 V | -0.3 V | 2.0 A, 1.0 $\mu \mathrm{s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Current Sense for Phases 1-3 | CS1-CS3 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Limit Set Point | lıIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Output Voltage | $\mathrm{CS}_{\text {REF }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage ID DAC Inputs | $\mathrm{V}_{\text {IDO-4 }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$;
$\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{ROSC}}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{DAC}$ Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $\mathbf{0}=$ Connected to GND; $1=$ Open or Pull-up to internal 3.3 V or external 5.0 V )

| Accuracy (all codes) <br> VID code - 125 mV |  |  |  |  | Connect $\mathrm{V}_{\mathrm{FB}}$ to COMP, Measure COMP | - | - | $\pm 1.0$ | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {ID4 }}$ | $V_{\text {ID3 }}$ | $V_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $V_{\text {IDO }}$ | $\mathrm{V}_{\text {ID }}$ Voltage | DAC Out $^{\text {Voltage }}$ |  |  | - |
| 1 | 1 | 1 | 1 | 1 | - | FAULT Mode-Output Off |  |  | - |
| 1 | 1 | 1 | 1 | 0 | 1.100 | 0.965 | 0.975 | 0.985 | V |
| 1 | 1 | 1 | 0 | 1 | 1.125 | 0.990 | 1.000 | 1.010 | V |
| 1 | 1 | 1 | 0 | 0 | 1.150 | 1.015 | 1.025 | 1.035 | V |
| 1 | 1 | 0 | 1 | 1 | 1.175 | 1.040 | 1.050 | 1.061 | V |
| 1 | 1 | 0 | 1 | 0 | 1.200 | 1.064 | 1.075 | 1.086 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\text {ROSC }}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $\mathbf{0}=$ Connected to GND; $1=$ Open or Pull-up to internal 3.3 V or external 5.0 V )

| 1 | 1 | 0 | 0 | 1 | 1.225 | 1.089 | 1.100 | 1.111 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 0 | 0 | 0 | 1.250 | 1.114 | 1.125 | 1.136 | V |
| 1 | 0 | 1 | 1 | 1 | 1.275 | 1.139 | 1.150 | 1.162 | V |
| 1 | 0 | 1 | 1 | 0 | 1.300 | 1.163 | 1.175 | 1.187 | V |
| 1 | 0 | 1 | 0 | 1 | 1.325 | 1.188 | 1.200 | 1.212 | V |
| 1 | 0 | 1 | 0 | 0 | 1.350 | 1.213 | 1.225 | 1.237 | V |
| 1 | 0 | 0 | 1 | 1 | 1.375 | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 0 | 1 | 0 | 1.400 | 1.263 | 1.275 | 1.288 | V |
| 1 | 0 | 0 | 0 | 1 | 1.425 | 1.287 | 1.300 | 1.313 | V |
| 1 | 0 | 0 | 0 | 0 | 1.450 | 1.312 | 1.325 | 1.338 | V |
| 0 | 1 | 1 | 1 | 1 | 1.475 | 1.337 | 1.350 | 1.364 | V |
| 0 | 1 | 1 | 1 | 0 | 1.500 | 1.361 | 1.375 | 1.389 | V |
| 0 | 1 | 1 | 0 | 1 | 1.525 | 1.386 | 1.400 | 1.414 | V |
| 0 | 1 | 1 | 0 | 0 | 1.550 | 1.411 | 1.425 | 1.439 | V |
| 0 | 1 | 0 | 1 | 1 | 1.575 | 1.436 | 1.450 | 1.465 | V |
| 0 | 1 | 0 | 1 | 0 | 1.600 | 1.460 | 1.475 | 1.490 | V |
| 0 | 1 | 0 | 0 | 1 | 1.625 | 1.485 | 1.500 | 1.515 | V |
| 0 | 1 | 0 | 0 | 0 | 1.650 | 1.510 | 1.525 | 1.540 | V |
| 0 | 0 | 1 | 1 | 1 | 1.675 | 1.535 | 1.550 | 1.566 | V |
| 0 | 0 | 1 | 1 | 0 | 1.700 | 1.560 | 1.575 | 1.591 | V |
| 0 | 0 | 1 | 0 | 1 | 1.725 | 1.584 | 1.600 | 1.616 | V |
| 0 | 0 | 1 | 0 | 0 | 1.750 | 1.609 | 1.625 | 1.641 | V |
| 0 | 0 | 0 | 1 | 1 | 1.775 | 1.634 | 1.650 | 1.667 | V |
| 0 | 0 | 0 | 1 | 0 | 1.800 | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 0 | 0 | 1 | 1.825 | 1.683 | 1.700 | 1.717 | V |
| 0 | 0 | 0 | 0 | 0 | 1.850 | 1.708 | 1.725 | 1.742 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 1.00 | 1.25 | 1.50 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID }}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Pull-up Voltage |  |  |  |  | - | 3.15 | 3.30 | 3.45 | V |

Power Good Output

| Upper Threshold |  | Force PWRGDS | $1.9(-5 \%)$ | 2.0 | $2.1(+5 \%)$ | V |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Lower Threshold |  | Force PWRGDS | $0.95 \times\left(\mathrm{V}_{\mathrm{ID}}-\right.$ <br> $125 \mathrm{mV})$ <br> or $-2.6 \%$ <br> from nominal <br> PWRGD <br> Threshold | $0.975 \times\left(\mathrm{V}_{\text {ID }}-\right.$ <br> $125 \mathrm{mV})$ | $\mathrm{V}_{\text {ID }}-$ <br> 125 mV <br> or $+2.6 \%$ <br> from nominal <br> PWRGD <br> Threshold | V |  |
| $\mathrm{V}_{\text {ID4 }}$ | $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $\mathrm{V}_{\text {ID0 }}$ |  |  |  |
| 1 | 1 | 1 | 1 | 0 |  | 0.926 | 0.951 |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\text {ROSC }}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Power Good Output

| 1 | 1 | 1 | 0 | 1 | - | 0.950 | 0.975 | 1.000 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 1 | 0 | 0 | - | 0.974 | 1.000 | 1.025 | V |
| 1 | 1 | 0 | 1 | 1 | - | 0.998 | 1.024 | 1.050 | V |
| 1 | 1 | 0 | 1 | 0 | - | 1.021 | 1.048 | 1.075 | V |
| 1 | 1 | 0 | 0 | 1 | - | 1.045 | 1.073 | 1.100 | V |
| 1 | 1 | 0 | 0 | 0 | - | 1.069 | 1.097 | 1.125 | V |
| 1 | 0 | 1 | 1 | 1 | - | 1.093 | 1.122 | 1.150 | V |
| 1 | 0 | 1 | 1 | 0 | - | 1.116 | 1.146 | 1.175 | V |
| 1 | 0 | 1 | 0 | 1 | - | 1.140 | 1.170 | 1.200 | V |
| 1 | 0 | 1 | 0 | 0 | - | 1.164 | 1.195 | 1.225 | V |
| 1 | 0 | 0 | 1 | 1 | - | 1.188 | 1.219 | 1.250 | V |
| 1 | 0 | 0 | 1 | 0 | - | 1.211 | 1.243 | 1.275 | V |
| 1 | 0 | 0 | 0 | 1 | - | 1.235 | 1.268 | 1.300 | V |
| 1 | 0 | 0 | 0 | 0 | - | 1.259 | 1.292 | 1.325 | V |
| 0 | 1 | 1 | 1 | 1 | - | 1.283 | 1.316 | 1.350 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.306 | 1.341 | 1.375 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.330 | 1.365 | 1.400 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.354 | 1.389 | 1.425 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.378 | 1.414 | 1.450 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.401 | 1.438 | 1.475 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.425 | 1.463 | 1.500 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.449 | 1.487 | 1.525 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.473 | 1.511 | 1.550 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.496 | 1.536 | 1.575 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.520 | 1.560 | 1.600 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.544 | 1.584 | 1.625 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.568 | 1.609 | 1.650 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.591 | 1.633 | 1.675 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.615 | 1.658 | 1.700 | V |
| 0 | 0 | 0 | 0 | 0 | - | 1.639 | 1.682 | 1.725 | V |
| Switch Leakage Current |  |  |  |  | $\begin{aligned} & \text { PWRGD }=5.5 \mathrm{~V} \\ & \text { PWRGDS }=1.60 \mathrm{~V} \end{aligned}$ | - | 0.1 | 10.0 | $\mu \mathrm{A}$ |
| Delay |  |  |  |  | PWRGDS low to PWRGD low | 25 | 50 | 125 | $\mu \mathrm{s}$ |
| Output Low Voltage |  |  |  |  | $\begin{aligned} & \text { PWRGDS }=1.0 \mathrm{~V} \\ & \text { IPWRGD }=4.0 \mathrm{~mA} \end{aligned}$ | - | 0.15 | 0.40 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\text {ROSC }}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Feedback Error Amplifier

| $\mathrm{V}_{\mathrm{FB}}$ Bias Current, (Note 2) | $0.9 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.8 \mathrm{~V}$ | 5.5 | 6.0 | 6.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | $\begin{aligned} & \mathrm{COMP}=0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ & \mathrm{V}_{\mathrm{FB}}=1.6 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.8 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Discharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3. | 60 | 90 | - | dB |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ COMP Capacitor | - | 400 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |
| COMP Max Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=1.65 \mathrm{~V} \text { COMP Open; } \\ & \mathrm{DAC}=00000 \end{aligned}$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\begin{gathered} \mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V} \text { COMP Open; } \\ \mathrm{DAC}=00000 \end{gathered}$ | - | 0.1 | 0.2 | V |
| Hiccup Latch Discharge Current | - | 2 | 5.0 | 10 | $\mu \mathrm{A}$ |

PWM Comparators

| Minimum Pulse Width | Measured from CSx to GATE(H), $\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS}_{\mathrm{REF}}\right)=0 \mathrm{~V},$ <br> $\mathrm{V}(\mathrm{COMP})=0.5 \mathrm{~V}, 60 \mathrm{mV}$ step applied between $\mathrm{V}_{\text {CSX }}$ and $\mathrm{V}_{\text {CREF }}$ | - | 350 | 515 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Channel Startup Offset | $\begin{gathered} V(C S 1)=V(C S 2)=V(C S 3)= \\ V\left(V_{F B}\right)=V\left(C S_{R E F}\right)=0 V ; \end{gathered}$ Measure V(COMP) when $\text { GATE1(H), } 2(\mathrm{H}), 3(\mathrm{H}) \text { switch high }$ | 0.3 | 0.4 | 0.5 | V |

GATE(H) and GATE(L)

| High Voltage (AC) | Note 3. Measure $\mathrm{V}_{\text {CCLX }}$ - GATE(L) or $\mathrm{V}_{\mathrm{CCHX}}-\mathrm{GATE}(\mathrm{H})$ | - | 0 | 1.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Note 3. Measure GATE(L) or GATE(H) | - | 0 | 0.5 | V |
| Rise Time GATE(H)x | 1.0 V < GATE $<8.0 \mathrm{~V} ; \mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Rise Time GATE(L)x | 1.0 V < GATE $<8.0 \mathrm{~V} ; \mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time GATE(H)x | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V} ; \mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time GATE(L)x | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V} ; \mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| GATE(H) to GATE(L) Delay | $\operatorname{GATE}(\mathrm{H})<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{~L})>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE(L) to GATE(H) Delay | GATE $(\mathrm{L})<2.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{H})>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-down | Force $100 \mu \mathrm{~A}$ into GATE Driver with $\mathrm{V}_{\mathrm{CCHX}}=\mathrm{V}_{\mathrm{CCLX}}=2.0 \mathrm{~V}$ | - | 1.2 | 1.6 | V |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of $\mathrm{R}_{\mathrm{ROSC}}$ per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\text {ROSC }}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Oscillator |  |  |  |  |  |
| Switching Frequency | Measure any phase $\left(R_{\text {ROSC }}=32.4 \mathrm{k}\right)$ <br> Note 4. | 300 | 400 | 500 | kHz |
| Switching Frequency | Measure any phase $\left(\mathrm{R}_{\mathrm{ROSC}}=53.6 \mathrm{k}\right)$ | 220 | 250 | 280 | kHz |
| Switching Frequency | Measure any phase $\left(\mathrm{R}_{\mathrm{ROSC}}=16.2 \mathrm{k}\right)$ <br> Note 4. | 600 | 800 | 1000 | kHz |
| ROSC Voltage | - | - | 1.00 | - | V |
| Phase Delay | - | 105 | 120 | 135 | deg |

Adaptive Voltage Positioning

| $\mathrm{V}_{\text {DRP }}$ Output Voltage to DACOUT Offset | $\begin{gathered} \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS} 3=\mathrm{CS} \\ \mathrm{~V}_{\mathrm{FB}}=\mathrm{CO}, \\ \text { Measure } \mathrm{V}_{\mathrm{DRP}} \text { - } \mathrm{COMP} \end{gathered}$ | -15 | - | 15 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum $\mathrm{V}_{\text {DRP }}$ Voltage | $\begin{gathered} \left\|(C S 1=C S 2=C S 3)=C S_{R E F}\right\|= \\ 50 \mathrm{mV}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \\ \mid \text { Measure } V_{\text {DRP }}-\mathrm{COMP} \mid \end{gathered}$ | 360 | 465 | 570 | mV |
| Current Sense Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.7 | 3.1 | 3.5 | V/V |

Current Sensing and Sharing

| CS REF $^{\text {Input Bias Current }}$ | - | - | 0.6 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS1-CS3 Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifiers Gain | - | 3.7 | 4.2 | 4.7 | V/V |
| Current Sense Amp Mismatch | $0 \mathrm{~V} \leq\left(\mathrm{CSx}-\mathrm{CS}_{\text {REF }}\right) \leq 50 \mathrm{mV}$ | -5.0 | - | 5.0 | mV |
| Current Sense Amplifiers Input Common Mode Range Limit | Note 4. | 0 | - | $\mathrm{V}_{\mathrm{CCL}}-2.0$ | V |
| Current Sense Input to LIIM Gain | $0.25 \mathrm{~V}<\mathrm{I}_{\text {LIM }}<1.20 \mathrm{~V}$ | 5.0 | 6.5 | 8.0 | V/V |
| Current Limit Filter Slew Rate | Note 4. | 4.0 | 10 | 26 | $\mathrm{mV} / \mathrm{\mu s}$ |
| ILIM Bias Current | $0 \mathrm{~V}<\mathrm{I}_{\text {LIM }}<1.0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse by Pulse Current Limit: V(CSx) - V(CS REF ) | - | 75 | 90 | 115 | mV |
| Current Sense Amplifier Bandwidth | Note 4. | 1.0 | - | - | MHz |

## Reference Output

| $\mathrm{V}_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{I}\left(\mathrm{V}_{\mathrm{REF}}\right)<1.0 \mathrm{~mA}$ | 3.15 | 3.25 | 3.35 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}\right.$; $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\text {ROSC }}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

General Electrical Specifications

| $\mathrm{V}_{\mathrm{CCL}}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 22 | 26 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{CCL} 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 4.0 | 5.5 | mA |
| $\mathrm{~V}_{\mathrm{CCL} 23}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 8.0 | 11 | mA |
| $\mathrm{~V}_{\mathrm{CCH} 12}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 5.5 | 7.0 | mA |
| $\mathrm{~V}_{\mathrm{CCH}}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 2.5 | 3.5 | mA |
| $\mathrm{~V}_{\mathrm{CCL}}$ Start Threshold | GATEs switching, COMP charging | 4.05 | 4.50 | 4.70 | V |
| $\mathrm{~V}_{\mathrm{CCL}}$ Stop Threshold | GATEs stop switching, COMP <br> discharging | 3.75 | 4.30 | 4.60 | V |
| $\mathrm{~V}_{\mathrm{CCL}}$ Hysteresis | GATEs not switching, COMP not <br> charging | 100 | 200 | 300 | mV |
| $\mathrm{V}_{\mathrm{CCH} 12}$ Start Threshold | - | 3.2 | 3.5 | 3.8 | V |
| $\mathrm{~V}_{\mathrm{CCH} 12}$ Stop Threshold | - | 2.9 | 3.2 | 3.5 | V |
| $\mathrm{~V}_{\mathrm{CCH} 12}$ Start Hysteresis | - | 200 | 300 | 400 | mV |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 32 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 1 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 2 | $\mathrm{V}_{\mathrm{FB}}$ | Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between $V_{F B}$ and $V_{\text {OUT }}$. The input bias current of the $V_{F B}$ pin and the resistor value determine output voltage offset for zero output current. Short $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\mathrm{OUT}}$ for no AVP. |
| 3 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to set amount AVP or leave this pin open for no AVP. |
| 4-6 | CS1-CS3 | Current sense inputs. Connect current sense network for the corresponding phase to each input. |
| 7 | $\mathrm{CS}_{\text {REF }}$ | Reference for current sense amplifiers. To balance input offset voltages between the inverting and noninverting inputs of the Current Sense Amplifiers, connect a resistor between CS REF and the output voltage. The value should be $1 / 3$ of the value of the resistors connected to the CSx pins. |
| 8 | PWRGD | Power Good Output. Open collector output goes low when $\mathrm{CS}_{\text {REF }}$ is out of regulation. |
| 9-13 | $\mathrm{V}_{\text {ID4 }}-\mathrm{V}_{\text {ID0 }}$ | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |
| 14 | PWRGDS | Power Good Sense. Connect to Output. |
| 15 | ILIM | Sets threshold for current limit. Connect to reference through a resistive divider. |
| 16 | REF | Reference output. Decouple with $0.1 \mu \mathrm{~F}$ to LGND. |
| 17 | LGND | Return for internal control circuits and IC substrate connection. |
| 18 | $\mathrm{V}_{\text {CCH3 }}$ | Power for GATE(H)3. |
| 19 | Gate(H)3 | High side driver \#3. |
| 20 | GND3 | Return for \#3 drivers. |
| 21 | Gate(L)3 | Low side driver \#3. |
| 22 | $\mathrm{V}_{\text {CCL23 }}$ | Power for GATE(L)2 and GATE(L)3. |
| 23 | Gate(L)2 | Low side driver \#2. |
| 24 | GND2 | Return for \#2 driver. |
| 25 | Gate(H)2 | High side driver \#2. |
| 26 | $\mathrm{V}_{\mathrm{CCH} 12}$ | Power for GATE(H)1 and GATE(H)2. UVLO Sense for High Side Driver supply connects to this pin. |
| 27 | Gate(H)1 | High side driver \#1. |
| 28 | GND1 | Return \#1 drivers. |
| 29 | Gate(L)1 | Low side driver \#1. |
| 30 | $\mathrm{V}_{\text {CCL1 }}$ | Power for GATE(L)1. |
| 31 | $\mathrm{V}_{\mathrm{CCL}}$ | Power for internal control circuits and UVLO Sense for Logic. |
| 32 | Rosc | A resistor from this pin to ground sets operating frequency and $V_{F B}$ bias current. |



CS5301

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Oscillator Frequency


Figure 5. Gate(H) Rise-time vs. Load Capacitance measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 7. Gate(L) Rise-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 4. $\mathrm{V}_{\mathrm{FB}}$ Bias Current vs. $\mathrm{R}_{\mathrm{Rosc}}$ Value


Figure 6. Gate(H) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 8. Gate(L) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .

## APPLICATIONS INFORMATION

## FIXED FREQUENCY MULTI-PHASE CONTROL

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5301 uses a three-phase, fixed frequency, Enhanced $\mathrm{V}^{2}$ architecture. Each phase is delayed $120^{\circ}$ from the previous phase. Normally GATE(H) transitions high at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator and bring GATE(H) low. Once GATE $(\mathrm{H})$ goes low, it will remain low until the beginning of the next oscillator cycle. While $\operatorname{GATE}(\mathrm{H})$ is high, the enhanced $\mathrm{V}^{2}$ loop will respond to line and load transients. Once GATE $(\mathrm{H})$ is low, the loop will not respond again until the beginning of the next cycle. Therefore, constant frequency Enhanced $\mathrm{V}^{2}$ will typically respond within $1 / 3$ of the off-time for a three-phase converter.

The Enhanced $\mathrm{V}^{2}$ architecture measures and adjusts current in each phase. An additional input $\left(\mathrm{CS}_{\mathrm{x}}\right)$ for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 9.


Figure 9. Enhanced V ${ }^{2}$ Feedback and Current Sense Scheme

The inductor current is measured across $\mathrm{R}_{\mathrm{S}}$, amplified by CSA and summed with the OFFSET and Output Voltage at the non-inverting input of the PWM comparator. The inductor current provides the PWM ramp and as inductor current increases the voltage on the positive pin of the PWM
comparator rises and terminates the PWM cycle. If the inductor starts the cycle with a higher current, the PWM cycle will terminate earlier providing negative feedback. The CS5301 provides a CS $_{\mathrm{x}}$ input for each phase, but the $\mathrm{CS}_{\mathrm{REF}}, \mathrm{V}_{\mathrm{FB}}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{V}_{\mathrm{FB}}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than phases with a smaller current signal.
Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$
\Delta V=\operatorname{RS} \times \text { CSA Gain } \times \Delta I
$$

The single-phase power stage output impedance is:
Single Stage Impedance $=\Delta \mathrm{V} / \Delta \mathrm{I}=\mathrm{RS} \times$ CSA Gain.
The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few $\mu$ s of a transient before the feedback loop has repositioned the COMP pin.

The peak output current of each phase can also be calculated from;

$$
I_{\text {pkout }}(\text { per phase })=\frac{\mathrm{V}_{\mathrm{COMP}}-\mathrm{V}_{\mathrm{FB}}-\mathrm{V}_{\mathrm{OFFSET}}}{\mathrm{R}_{\mathrm{S}} \times \mathrm{CSA} \text { Gain }}
$$

Figure 10 shows the step response of a single phase with the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides the PWM ramp through the Current Share Amplifier. The PWM cycle ends when the sum of the current signal, voltage signal and OFFSET exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the current signal level is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 10. Open Loop Operation

## Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 11. In the diagram L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal the values of R1 and C 1 are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} 1 \times \mathrm{C} 1$. If this criteria is met the current sense signal will be the same shape as the inductor current, the voltage signal at $\mathrm{CS}_{\mathrm{x}}$ will represent the instantaneous value of inductor current and the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor ( $\mathrm{R}_{\mathrm{S}}$ ).


Figure 11. Lossless Inductive Current Sensing with Enhanced $\mathbf{V}^{2}$
When choosing or designing inductors for use with inductive sensing tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be
considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 9.

## Current Sharing Accuracy

PCB traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at the same point for each phase and the connection to the $\mathrm{CS}_{\text {REF }}$ should be made so that no phase is favored. (In some cases, especially with inductive sensing, resistance of the pcb can be useful for increasing the current sense resistance.) The total current sense resistance used for calculations must include any pcb trace between the $\mathrm{CS}_{\mathrm{x}}$ inputs and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier Input Mismatch and the value of the current sense element will determine the accuracy of current sharing between phases. The worst case Current Sense Amplifier Input Mismatch is 5.0 mV and will typically be within 3.0 mV . The difference in peak currents between phases will be the CSA Input Mismatch divided by the current sense resistance. If all current sense elements are of equal resistance a 3.0 mV mismatch with a $2.0 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## Operation at > 50\% Duty Cycle

For operation at duty cycles above $50 \%$ Enhanced V ${ }^{2}$ will exhibit subharmonic oscillation unless a compensation ramp is added to each phase. A circuit like the one on the left side of Figure 12 can be added to each current sense network to implement slope compensation. The value of R1 can be varied to adjust the ramp size.


Figure 12. External Slope Compensation Circuit

## Ramp Size and Current Sensing

Because the current ramp is used for both the PWM ramp and to sense current, the inductor and sense resistor values will be constrained. A small ramp will provide a quick transient response by minimizing the difference over which the COMP pin must travel between light and heavy loads, but a steady state ramp of 25 mV -p or greater is typically required to prevent pulse skipping and minimize pulse width jitter. For resistive current sensing, the combination of the inductor and sense resistor values must be chosen to provide a large enough steady state ramp. For large inductor values the sense resistor value must also be increased.

For inductive current sensing, the RC network must meet the requirement of $L / R_{L}=R \times C$ to accurately sense the $A C$ and DC components of the current the signal. Again the values for L and $\mathrm{R}_{\mathrm{L}}$ will be constrained in order to provide a large enough steady state ramp with a compensated current sense signal. A smaller $L$, or a larger $R_{L}$ than optimum might be required. But unlike resistive sensing, with inductive sensing, small adjustments can be made easily with the values of R and C to increase the ramp size if needed.

If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R} \times \mathrm{C}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R} \times \mathrm{C}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During transients the COMP pin will be required to overshoot along with the current signal in order to maintain the output voltage. The $\mathrm{V}_{\mathrm{DRP}}$ pin will also overshoot during transients and possibly slow the response. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}$, $\mathrm{R}_{\mathrm{L}}=1.6 \mathrm{~m} \Omega, \mathrm{R} 1=20 \mathrm{k}$ and $\mathrm{C} 1=.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of R1 should be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu \mathrm{~s}$ time constant. With this compensation the $\mathrm{I}_{\text {LIM }}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 13. Inductive Sensing waveform during a Step with Fast RC Time Constant ( $50 \mu \mathrm{~s} / \mathrm{div}$ )

## Current Limit

Two levels of overcurrent protection are provided. Any time the voltage on a Current Sense pin exceeds CS REF by more than the Single Phase Pulse by Pulse Current Limit, the PWM comparator for that phase is turned off. This provides fast peak current protection for individual phases. The outputs of all the currents are also summed and filtered to compare an averaged current signal to the voltage on the $\mathrm{I}_{\text {LIM }}$ pin. If this voltage is exceeded, the fault latch trips and the Soft Start capacitor is discharged by a $5.0 \mu \mathrm{~A}$ source until the COMP pin reaches 0.2 V . Then Soft Start begins. The converter will continue to operate in this mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced $\mathrm{V}^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET's to shut off and the synchronous MOSFET's to turn on. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## UVLO

The CS5301 has undervoltage lockout functions connected to two pins. One intended for the logic and low-side drivers with a 4.5 V turn-on threshold is connected to the $\mathrm{V}_{\mathrm{CCL}}$ pin. A second for the high side drivers has a 3.5 V threshold and is connected to the $\mathrm{V}_{\mathrm{CCH} 12} \mathrm{pin}$.

The UVLO threshold for the high side drivers was chosen at a low value to allow for flexibility in the part. In many applications this function will be disabled or will only check that the applicable supply is on - not that is at a high enough voltage to run the converter.

For the 12 VIN converter (see Figure 1) the UVLO pin for the high side driver is pulled up by the 5.0 V supply (through two diode drops) and the function is not used. The diode between the COMP pin and the 12 V supply holds the COMP pin near GND and prevents start-up while the 12 V supply is off. In an application where a higher UVLO threshold is necessary a circuit like the one in Figure 15 will lock out the converter until the 12 V supply exceeds 8.0 V .

## VID Codes and Power Good

The internal VID and DACOUT levels are set up so that the reference for the control loop is nominally 125 mV below the VID code (see the block diagram). The nominal lower Power Good threshold is $2.5 \%$ below the DACout level. The nominal upper Power Good threshold is fixed at 2.0 V for all VID codes. This scheme is intended to select the VID level as the maximum output voltage and the DAC OUT level as the minimum output voltage.

## TRANSIENT RESPONSE AND ADAPTIVE POSITIONING

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher at light loads to reduce output voltage sag when the load current is stepped up and set lower during heavy loads to reduce overshoot when the load current is stepped up. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example; in a 50 A converter a $1.0 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond quickly to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output
voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 14. Adaptive Positioning
The CS5301 uses two methods to provide fast and accurate adaptive positioning. For low frequency positioning the VFB and VDRP pins are used to adjust the output voltage with varying load currents. For high frequency positioning, the current sense input pins can be used to control the power stage output impedance. The transition between fast and slow positioning is adjusted by the error amp compensation.

The CS5301 can be configured to adjust the output voltage based on the output current of the converter, as shown in Figure 1.
To set the no-load positioning, a resistor (R9) is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to decrease the output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of $\mathrm{R}_{\text {ROSC }}$, as shown in Figure 4.
During no load conditions the $\mathrm{V}_{\mathrm{DRP}}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor (R8). When output current increases the $\mathrm{V}_{\text {DRP }}$ pin increases proportionally and the $\mathrm{V}_{\mathrm{DRP}}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to further decrease.
The $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{DRP}}$ pins take care of the slower and DC voltage positioning. The first few $\mu$ s are controlled primarily by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

Note: Large levels of adaptive positioning can cause pulse width jitter.

## Error Amp Compensation

The transconductance error amplifier can be configured to provide both a slow soft-start and a fast transient response. C 4 in Figure 1 controls soft-start. A $0.1 \mu \mathrm{~F}$ capacitor with the $30 \mu \mathrm{~A}$ error amplifier output capability will allow the output to ramp up at $0.3 \mathrm{~V} / \mathrm{ms}$ or 1.5 V in 5.0 ms .

R 10 is connected in series with C 4 to allow the error amplifier to slew quickly over a narrow range during load transients. Here the $30 \mu \mathrm{~A}$ error amplifier output capability
works against $10 \mathrm{k} \Omega$ (R10) to limit the window of fast slewing to 300 mV - enough to allow for fast transients, but not enough to interfere with soft-start. This window will be noticeable as a step in the COMP pin voltage at startup. The size of this step must be kept smaller than the Channel Startup Offset (nominally 0.4 V ) for proper soft-start operation. If adaptive positioning is used the R9 and R8 form a divider with the $\mathrm{V}_{\mathrm{DRP}}$ end held at the DAC voltage during startup, which effectively makes the Channel Startup Offset larger.

C12 is included for error amp stability. A capacitive load is required on the error amp output. Use of values less than 1.0 nF may result in error amp oscillation of several MHz .

C 11 and the parallel resistance of the $\mathrm{V}_{\mathrm{FB}}$ resistor (R9) and the $\mathrm{V}_{\mathrm{DRP}}$ resistor (R8) are used to roll off the error amp gain. The gain is rolled off at high enough frequency to give a quick transient response, but low enough to cross zero dB well below the switching frequency to minimize ripple and noise on the COMP pin.


Figure 15. External UVLO Circuit

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically, a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to reroute the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

Voltage feedback should be taken from a point of the output or the output filter that doesn't favor any one phase.

If the feedback connection is closer to one inductor than the others the ripple associated with that phase may appear larger than the ripple associated with the other phases and poor current sharing can result.

The current sense signal is typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as switch nodes and gate drive signals. The paths should be matched as well as possible. It is especially important that all current sense signals be picked off at similar points for accurate current sharing. If the current signal is taken from a place other than directly at the inductor any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistance and should be considered in design calculations. Capacitors for the current feedback networks should be placed as close to the current sense pins as practical.

## DESIGN PROCEDURE

## Current Sensing, Power Stage and Output Filter Components

1. Choose the output filter components to meet peak transient requirements. The formula below can be used to provide an approximate starting point for capacitor choice, but will be inadequate to calculate actual values.

$$
\Delta \mathrm{V} \text { PEAK }=(\Delta \mathrm{I} / \Delta \mathrm{T}) \times \mathrm{ESL}+\Delta \mathrm{I} \times \mathrm{ESR}
$$

Ideally the output filter should be simulated with models including ESR, ESL, circuit board parasitics and delays due to switching frequency and converter response. Typically both bulk capacitance (electrolytic, Oscon, etc.,) and low impedance capacitance (ceramic chip) will be required. The bulk capacitance provides "hold up" during the converter response. The low impedance capacitance reduces steady state ripple and bypasses the bulk capacitance during slewing of output current.
2. For inductive current sensing (only) choose the current sense network RC to provide a 25 mV minimum ramp during steady state operation.

$$
R=\left(V_{\text {IN }}-V_{\text {OUT }}\right) \times \frac{V_{\text {OUT }} / V_{I N}}{f \times C \times 25 \mathrm{mV}}
$$

Then choose the inductor value and inherent resistance to satisfy $L / R_{L}=R \times C$.
For ideal current sense compensation the ratio of L and $R_{L}$ is fixed, so the values of $L$ and $R_{L}$ will be a compromise typically with the maximum value $\mathrm{R}_{\mathrm{L}}$ limited by conduction losses or inductor temperature rise and the minimum value of $L$ limited by ripple current.
3. For resistive current sensing choose $L$ and $R_{S}$ to provide a steady state ramp greater than 25 mV .

$$
\mathrm{L} / \mathrm{R}_{\mathrm{S}}=\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{V}_{\mathrm{OUT} /} / \mathrm{V}_{\text {IN }}}{\mathrm{f} \times 25 \mathrm{mV}}
$$

Again the ratio of $L$ and $R_{L}$ is fixed and the values of L and $\mathrm{R}_{\mathrm{S}}$ will be a compromise.
4. Calculate the high frequency output impedance (ConverterZ) of the converter during transients. This is the impedance of the Output filter ESR in parallel with the power stage output impedance (PwrstgZ) and will indicate how far from the original level ( $\Delta \mathrm{VR}$ ) the output voltage will typically recover to within one switching cycle. For a good transient response $\Delta \mathrm{VR}$ should be less than the peak output voltage overshoot or undershoot.

$$
\begin{array}{r}
\Delta \mathrm{VR}=\text { ConverterZ } \times \text { IOUT } \\
\text { ConverterZ }=\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+ \text { ESR }}
\end{array}
$$

where:

$$
\text { PwrstgZ }=\text { RS } \times \text { CSA Gain } / 3
$$

Multiply the converterZ by the output current step size to calculate where the output voltage should recover to within the first switching cycle after a transient. If the ConverterZ is higher than the value required to recover to where the adaptive positioning is set the remainder of the recovery will be controlled by the error amp compensation and will typically recover in 10-20 $\mu \mathrm{s}$.

$$
\Delta \mathrm{VR}=\Delta \mathrm{l} \text { OUT } \times \text { ConverterZ }
$$

Make sure that $\Delta \mathrm{VR}$ is less than the expected peak transient for a good transient response.
5. Adjust L and $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ as required to meet the best combination of transient response, steady state output voltage ripple and pulse width jitter.

## Current Limit

When the sum of the Current Sense amplifiers ( $\mathrm{V}_{\text {ITOTAL }}$ ) exceeds the voltage on the $\mathrm{I}_{\text {LIM }}$ pin the part will enter hiccup mode. For inductive sensing the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor resistance (or current sense resistor) at max temperature and max current. To set the level of the $\mathrm{I}_{\text {LIM }}$ pin:
6. $\mathrm{VILIM}_{\mathrm{IL}}=\mathrm{R} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS}$ to ILIM Gain
where:

$$
\mathrm{R} \text { is } \mathrm{R}_{\mathrm{L}} \text { or } \mathrm{R}_{\mathrm{S}}
$$

$\mathrm{I}_{\mathrm{OUT}(\mathrm{LIM})}$ is the current limit threshold.
For the overcurrent to work properly the inductor time constant (L/R) should be $\leq$ the Current sense RC. If the RC is too fast, during step loads the current waveform will appear larger than it is (typically for a few hundred $\mu \mathrm{s}$ ) and may trip the current limit at a level lower than the DC limit.

## Adaptive Positioning

7. To set the amount of voltage positioning above the DAC setting at no load connect a resistor ( $\mathrm{R}_{\mathrm{VFB}}$ ) between the output voltage and the $\mathrm{V}_{\mathrm{FB}}$ pin. Choose $R_{\text {VFB }}$ as;

$$
\text { RVFB }=\text { NL Position/VFB Bias Current }
$$

See Figure 4 for $\mathrm{V}_{\mathrm{FB}}$ Bias Current.
8. To set the difference in output voltage between no load and full load, connect a resistor (RVDRP) between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pins. $\mathrm{R}_{\mathrm{VDRP}}$ can be calculated in two steps. First calculate the difference between the $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\mathrm{FB}}$ pin at full load. (The $\mathrm{V}_{\mathrm{FB}}$ voltage should be the same as the DAC voltage during closed loop operation.) Then choose the $\mathrm{R}_{\mathrm{VDRP}}$ to source enough current across $\mathrm{R}_{\mathrm{VFB}}$ for the desired change in output voltage.

$$
\Delta V_{V D R P}=\mathrm{R} \times \mathrm{IOUT} \times \mathrm{CS} \text { to } \mathrm{V}_{\mathrm{DRP}} \text { Gain }
$$

where:
$\mathrm{R}=\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ for one phase;
IOUT is the full load output current.

$$
\begin{gathered}
\mathrm{RVDRP}=\Delta \mathrm{V}_{\mathrm{VDRP}} \times \mathrm{RV}(\mathrm{FB}) / \Delta \mathrm{V}_{\mathrm{OUT}} \\
\text { DESIGN EXAMPLE }
\end{gathered}
$$

Choose the component values for lossless current sensing, adaptive positioning and current limit for a $250 \mathrm{kHz}, 1.55 \mathrm{~V}$, 60 A converter. The VID code is set to 1.6 V . Adaptive positioning is set for 100 mV above DACOUT (or 25 mV below VID) at no load and 75 mV below the no load position with a 60 A load. The peak output voltage transient should be less than 100 mV during a 60 A step current. The overcurrent limit is nominally 75 A .

## Current Sensing, Power Stage and Output Filter Components

1. Assume $1.5 \mathrm{~m} \Omega$ of output filter ESR.
2. Choose $\mathrm{C}=0.01 \mu \mathrm{~F}$

$$
\begin{aligned}
& R=\left(V_{\text {IN }}-V_{\text {OUT }}\right) \times \frac{V_{\text {OUT }} / V_{I N}}{f \times C \times 25 \mathrm{mV}} \\
&=(12-1.55) \times \frac{1.55 / 12}{250 \mathrm{k} \times 0.01 \mu \mathrm{~F} \times 25 \mathrm{mV}} \\
&=21.5 \mathrm{k} \Omega \Rightarrow C h o o s e 20 \mathrm{k} \Omega \\
& \mathrm{~L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} \times \mathrm{C}=20 \mathrm{k} \Omega \times 0.01 \mu \mathrm{~F}=200 \mu \mathrm{~s} \\
& \mathrm{Choose} \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{~m} \Omega \\
& \mathrm{~L}=\mathrm{R}_{\mathrm{L}} \times \mathrm{R} \times \mathrm{C}=2.0 \mathrm{~m} \Omega \times 200 \mu \mathrm{~s}=400 \mathrm{nH}
\end{aligned}
$$

3. $\mathrm{n} / \mathrm{a}$
4. PwrstgZ $=R_{L} \times$ CSA Gain $/ 3$

$$
=2.0 \mathrm{~m} \Omega \times 4.2 / 3.0=2.8 \mathrm{~m} \Omega
$$

$$
\begin{aligned}
\text { ConverterZ } & =\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+ \text { ESR }} \\
& =\frac{2.8 \mathrm{~m} \Omega \times 1.5 \mathrm{~m} \mathrm{\Omega}}{2.8 \mathrm{~m} \Omega+1.5 \mathrm{~m} \Omega} \cong 1.0 \mathrm{~m} \Omega
\end{aligned}
$$

$$
\Delta \mathrm{VR}=\text { ConverterZ } \times \text { IOUT }
$$

$$
=1.0 \mathrm{~m} \Omega \times 60 \mathrm{~A}=60 \mathrm{mV}
$$

5. $\mathrm{n} / \mathrm{a}$

## Current Limit

6. $\mathrm{V}_{\mathrm{ILIM}}=\mathrm{R}_{\mathrm{L}} \times \mathrm{IOUT}^{(\mathrm{LIM})}$

$$
\begin{aligned}
& \times \text { CS to ILIM Gain } \\
= & 2.0 \mathrm{~m} \Omega \times 75 \mathrm{~A} \times 6.5 \\
= & 975 \mathrm{mV}
\end{aligned}
$$

Adaptive Positioning
7. RVFB $=$ NL Position/VFB Bias Current

$$
=100 \mathrm{mV} / 6.0 \mu \mathrm{~A}=16.7 \mathrm{k} \Omega
$$

$$
\text { 8. } \begin{aligned}
\Delta V_{\text {DRP }}= & R_{\mathrm{L}} \times \text { IOUT } \\
& \times \text { Current Sense to VDRP Gain } \\
= & 2.0 \mathrm{~m} \Omega \times 60 \mathrm{~A} \times 3.1 \\
= & 372 \mathrm{mV} \\
\text { RVDRP }= & \Delta V_{\mathrm{DRP}} \times \text { RVFB } / \Delta \mathrm{V}_{\mathrm{OUT}} \\
= & 372 \mathrm{mV} \times 16.7 \mathrm{k} \Omega / 75 \mathrm{mV} \\
= & 82 \mathrm{k} \Omega
\end{aligned}
$$



Figure 16. Additional Application Diagram, 12 V to 1.75 V, 45 A for AMD Athlon ${ }^{\text {TM }}$ Processor

## CS5302

## Two-Phase Buck Controller with Integrated Gate Drivers and 4-Bit DAC

The CS5302 is a two-phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi-phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced V ${ }^{2 T M}$ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use.

The CS5302 multi-phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in inductor values and a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

## Features

- Enhanced $\mathrm{V}^{2}$ Control Method
- 4-Bit DAC with $1 \%$ Accuracy
- Adjustable Output Voltage Positioning
- 4 On-Board Gate Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors, Sense Resistors, or V-S Control
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On-Board Current Sense Amplifiers
- 3.3 V, 1.0 mA Reference Output
- On/Off Control (through Soft Start Pin)
- Power Good Output with Internal Delay


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com

SO-28L DW SUFFIX CASE 751F

## MARKING DIAGRAM

28


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5302GDW28 | SO-28L | 27 Units/Rail |
| CS5302GDWR28 | SO-28L | 1000 Tape \& Reel |



Figure 1. Application Diagram, 5.0 V to 1.6 V, 35 A Converter

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :--- | :---: | :---: |
| Operating Junction Temperature | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power for Logic | $\mathrm{V}_{\text {CCL }}$ | 16 V | -0.3 V | N/A | 50 mA |
| Power for Gate(L)1 | $\mathrm{V}_{\text {CCL1 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for Gate(L)2 | $\mathrm{V}_{\text {CCL2 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power Gate(H)1 | $\mathrm{V}_{\mathrm{CCH} 1}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for Gate(H)2 | $\mathrm{V}_{\mathrm{CCH} 2}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |

ABSOLUTE MAXIMUM RATINGS (continued)

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | 1.0 mA | 20 mA |
| Soft Start Capacitor | SS | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Compensation Network | COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Input | $V_{\text {FB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Output for Adjusting Adaptive Voltage Position | $\mathrm{V}_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Frequency Resistor | Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Reference Output | REF | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| High-Side FET Drivers | GATE(H) | 20 V | $\begin{aligned} & -0.3 \mathrm{~V} \text { DC } \\ & -2.0 \mathrm{~V} \text { for } \\ & 100 \mathrm{~ns} \end{aligned}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Low Side FET Drivers | GATE(L) | 16 V | $\begin{aligned} & -0.3 \mathrm{~V} \mathrm{DC} \\ & -2.0 \mathrm{~V} \text { for } \\ & 100 \mathrm{~ns} \end{aligned}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Return for Logic | LGND | N/A | N/A | 50 mA | N/A |
| Return for \#1 Driver | GND1 | 0.3 V | -0.3 V | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Return for \#2 Driver | GND2 | 0.3 V | -0.3 V | 2.0 A, $1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Current Sense for Phases 1-2 | CS1-CS2 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Limit Set Point | ILIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Sense Reference | $\mathrm{CS}_{\text {REF }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage ID DAC Inputs | $\mathrm{V}_{\text {IDO-3 }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 10 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$;
$\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code 1001, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $0=$ Connected to $\mathrm{V}_{\mathrm{SS}} ; 1=$ Open or Pull-up to 3.3 V )

| Accuracy (all codes) |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=$ COMP |  |  | $\pm 1.0$ | $\%$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $\mathrm{V}_{\text {ID0 }}$ |  |  |  |  |  |
| 1 | 1 | 1 | 1 | - | 1.287 | 1.300 | 1.313 | V |
| 1 | 1 | 1 | 0 | - | 1.337 | 1.350 | 1.364 | V |
| 1 | 1 | 0 | 1 | - | 1.386 | 1.400 | 1.414 | V |
| 1 | 1 | 0 | 0 | - | 1.436 | 1.450 | 1.465 | V |
| 1 | 0 | 1 | 1 | - | 1.485 | 1.500 | 1.515 | V |
| 1 | 0 | 1 | 0 | - | 1.535 | 1.550 | 1.566 | V |
| 1 | 0 | 0 | 1 | - | 1.584 | 1.600 | 1.616 | V |
| 1 | 0 | 0 | 0 | - | 1.634 | 1.650 | 1.667 | V |
| 0 | 1 | 1 | 1 | - | 1.683 | 1.700 | 1.717 | V |
| 0 | 1 | 1 | 0 | - | 1.733 | 1.750 | 1.768 | V |
| 0 | 1 | 0 | 1 |  |  | 1.782 | 1.800 | 1.818 |
| 0 | 1 | 0 | 0 | Not Allowed |  | - | - | - |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 10 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{DAC}$ Code 1001, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{l}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $\mathbf{0}=$ Connected to $\mathrm{V}_{\mathrm{SS}} ; 1=$ Open or Pull-up to 3.3 V )

| 0 | 0 | 1 | 1 | Not Allowed | - | - | - | - |
| :---: | :---: | :---: | :---: | :--- | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 0 | Not Allowed | - | - | - | - |
| 0 | 0 | 0 | 1 | Not Allowed | - | - | - | - |
| 0 | 0 | 0 | 0 | Not Allowed | - | - | - | - |
| Input Threshold |  |  |  |  |  |  |  |  |

Power Good Output

| Power Good Fault Delay | $\mathrm{CS}_{\text {REF }}=\mathrm{V}_{\mathrm{DAC}}$ to $\mathrm{V}_{\mathrm{DAC}} \pm 15 \%$ | 25 | 50 | 125 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Low Voltage | $\mathrm{CS}_{\text {REF }}=1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{PWRGD}}=4.0 \mathrm{~mA}$ | - | 0.25 | 0.40 | V |
| Output Leakage Current | $\mathrm{CS}_{\text {REF }}=1.6 \mathrm{~V}, \mathrm{PWRGD}=5.5 \mathrm{~V}$ | - | 0.1 | 10 | $\mu \mathrm{~A}$ |
| Lower Threshold | \% of Nominal VID Code | -14 | -11 | -8 | $\%$ |
| Upper Threshold | \% of Nominal VID Code | 8 | 11 | 14 | $\%$ |

Voltage Feedback Error Amplifier

| $\mathrm{V}_{\text {FB }}$ Bias Current (Note 2) | $1.2 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.9 \mathrm{~V}$ | 9.0 | 10.3 | 11.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.75 \mathrm{~V} ; \mathrm{DAC}=0101 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.85 \mathrm{~V} ; \mathrm{DAC}=0101 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=1.75 \mathrm{~V}$ COMP Open; $\mathrm{DAC}=0101$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.85 \mathrm{~V}$ COMP Open; $\mathrm{DAC}=0101$ | - | 0.1 | 0.2 | V |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3 | 60 | 90 | - | dB |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ COMP Capacitor | - | 400 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |

## Soft Start

| Soft Start Charge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 15 | 30 | 50 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Soft Start Discharge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 4.0 | 7.5 | 13 | $\mu \mathrm{~A}$ |
| Hiccup Mode Charge/Discharge Ratio | - | 3.0 | 4.0 | - | - |
| Peak Soft Start Charge Voltage | - | 3.3 | 4.0 | 4.2 | V |
| Soft Start Discharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of $\mathrm{R}_{\mathrm{OSC}}$ per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 10 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{DAC}$ Code 1001, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{l}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PWM Comparators |  |  |  |  |  |
| Minimum Pulse Width | Measured from CSx to GATE(H) $\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS}_{\mathrm{REF}}\right)=1.0 \mathrm{~V}, \mathrm{~V}(\mathrm{COMP})=1.5 \mathrm{~V}$ <br> 60 mV step applied between $\mathrm{V}_{\mathrm{CSX}}$ and $\mathrm{V}_{\text {CREF }}$ | - | 350 | 515 | ns |
| Channel Start Up Offset | $V(C S 1)=V(C S 2)=V\left(V_{F B}\right)=V\left(C S_{R E F}\right)=0 V \text {; }$ <br> Measure V(COMP) when GATE(H)1, (H)2, switch high | 0.3 | 0.4 | 0.5 | V |

## Gate(H) and Gate(L)

| High Voltage (AC) | Note 4 Measure $\mathrm{V}_{\text {CCLX }}$ - Gate(L)X or $V_{\mathrm{CCHX}} \text { - Gate }(\mathrm{H})_{\mathrm{X}}$ | - | 0 | 1.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Note 4 Measure Gate(L) X or Gate(H) X | - | 0 | 0.5 | V |
| Rise Time Gate(H)X | 1.0 V < GATE $<8.0 \mathrm{~V}$; $\mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Rise Time Gate(L)X | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time Gate(H) X | 8.0 V > GATE > 1.0 V ; $\mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time Gate(L) X | $8.0 \mathrm{~V}>\mathrm{GATE}>1.0 \mathrm{~V}$; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Gate(H) to Gate(L) Delay | Gate(H) $\mathrm{X}<2.0 \mathrm{~V}$, Gate(L) $\mathrm{X}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| Gate(L) to Gate(H) Delay | Gate(L) $\mathrm{x}<2.0 \mathrm{~V}$, Gate(H) $\mathrm{x}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-down | Force $100 \mu \mathrm{~A}$ into Gate Driver with no power applied to $\mathrm{V}_{\mathrm{CCHX}}$ and $\mathrm{V}_{\mathrm{CCLX}}=2 \mathrm{~V}$. | - | 1.2 | 1.6 | V |

## Oscillator

| Switching Frequency | Measure any phase (ROSC $=32.4 \mathrm{k})$ | 300 | 400 | 500 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | Note 4 Measure any phase (ROSC $=63.4 \mathrm{k})$ | 150 | 200 | 250 | kHz |
| Switching Frequency | Note 4 Measure any phase (ROSC $=16.2 \mathrm{k})$ | 600 | 800 | 1000 | kHz |
| ROsc $^{\text {Voltage }}$ | - | - | 1.0 | - | V |
| Phase Delay | - | 165 | 180 | 195 | deg |

Adaptive Voltage Positioning

| $V_{\text {DRP }}$ Output Voltage to DAC Offset | $\begin{aligned} & \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\text {REF }}, \mathrm{V}_{\mathrm{FB}}=\mathrm{COMP} \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | -15 | - | 15 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum V ${ }_{\text {DRP }}$ Voltage | $\begin{aligned} & (\mathrm{CS1}=\mathrm{CS} 2)-\mathrm{C}_{\mathrm{REF}}=50 \mathrm{mV}, \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | 240 | 310 | 380 | mV |
| Current Sense Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.4 | 3.0 | 3.8 | V/V |

Current Sensing and Sharing

| CS REF $^{\text {Input Bias Current }}$ | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.5 | 4.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS1-CS2 Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifiers Gain | - | 2.8 | 3.15 | 3.53 | V/V |
| Current Sense Amp Mismatch | Note $40 \leq\left(C S x-\right.$ CS $\left._{\text {REF }}\right) \leq 50 \mathrm{mV}$ | -5.0 | - | 5.0 | mV |
| Current Sense Amplifiers Input Common Mode Range Limit | Note 4 | 0 | - | $\mathrm{V}_{\mathrm{CCL}}-2$ | V |
| Current Sense Input to ILIM Gain | 0.25 V < $\mathrm{I}_{\text {LIM }}<1.20 \mathrm{~V}$ | 5.0 | 6.25 | 8.0 | V/V |
| Current Limit Filter Slew Rate | Note 4 | 4.0 | 10 | 26 | $\mathrm{mV} / \mathrm{\mu s}$ |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 10 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{DAC}$ Code 1001, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{l}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Sensing and Sharing |  |  |  |  |  |
| ILIM Bias Current | $0<\mathrm{I}_{\text {LIM }}<1.0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse by Pulse Current Limit: V(CSx) - V(CSREF) | - | 90 | 105 | 135 | mV |
| Current Share Amplifier Bandwidth | Note 5 | 1.0 | - | - | MHz |

Reference Output

| $V_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{I}\left(\mathrm{V}_{\mathrm{REF}}\right)<1.0 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

General Electrical Specifications

| $\mathrm{V}_{\mathrm{CCL}}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 20 | 24.5 | mA |
| :--- | :--- | :--- | :--- | :--- | :---: |
| $\mathrm{~V}_{\mathrm{CLL} 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 4.0 | 5.5 | mA |
| $\mathrm{~V}_{\mathrm{CCL2}}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 4.0 | 5.5 | mA |
| $\mathrm{~V}_{\mathrm{CCH} 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 2.8 | 4.0 | mA |
| $\mathrm{~V}_{\mathrm{CCH} 2}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 2.5 | 3.5 | mA |
| $\mathrm{~V}_{\mathrm{CCL}}$ Start Threshold | GATEs switching, Soft Start charging | 4.05 | 4.4 | 4.7 | V |
| $\mathrm{~V}_{\mathrm{CCL}}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 3.75 | 4.2 | 4.6 | V |
| $\mathrm{~V}_{\mathrm{CCL}}$ Hysteresis | GATEs not switching, Soft Start not charging | 100 | 200 | 300 | mV |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Start Threshold | GATEs switching, Soft Start charging | 8.4 | 9.2 | 9.9 | V |
| $\mathrm{~V}_{\mathrm{CCH} 1}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 7.8 | 8.7 | 9.6 | V |
| $\mathrm{~V}_{\mathrm{CCH} 1}$ Hysteresis | GATEs not switching, Soft Start not charging | 300 | 500 | 700 | mV |

5. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 28 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 1 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 2 | $V_{\text {FB }}$ | Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$. The input bias current of the $\mathrm{V}_{\mathrm{FB}}$ pin and the resistor value determine output voltage offset for zero output current. Short $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\mathrm{OUT}}$ for no AVP. |
| 3 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to set amount AVP or leave this pin open for no AVP. |
| 4-5 | CS1-CS2 | Current sense inputs. Connect current sense network for the corresponding phase to each input. |
| 6 | $C S_{\text {REF }}$ | Reference for current sense amplifiers and input for Power Good comparators. To balance input offset voltages between the inverting and non-inverting inputs of the current sense amplifiers, connect a resistor between $\mathrm{CS}_{\text {REF }}$ and the output voltage. The value should be $2 / 5$ of the value of the resistors connected to the CSx pins. |
| 7 | PWRGD | Power Good Output. Open collector output goes low when $\mathrm{CS}_{\text {REF }}$ is out of regulation. |

PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 28 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 8 | N/C | No connection. |
| 9-12 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID }}$ | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |
| 13 | ILIM | Sets threshold for current limit. Connect to reference through a resistive divider. |
| 14 | REF | Reference output. Decouple with $0.1 \mu \mathrm{~F}$ to LGND. |
| 15 | $\mathrm{V}_{\mathrm{CCH} 2}$ | Power for GATE(H)2. |
| 16 | Gate(H)2 | High side driver \#2. |
| 17 | GND2 | Return for \#2 driver. |
| 18 | Gate(L)2 | Low side driver \#2. |
| 19 | $\mathrm{V}_{\text {CCL2 }}$ | Power for GATE(L)2. |
| 20 | SS | Soft Start capacitor pin. The Soft Start capacitor controls both Soft Start time and hiccup mode frequency. The COMP pin is clamped below Soft Start during Start-Up and hiccup mode. |
| 21 | LGND | Return for internal control circuits and IC substrate connection. |
| 22 | $\mathrm{V}_{\mathrm{CCH} 1}$ | Power for GATE(H)1. UVLO Sense for High Side Driver supply connects to this pin. |
| 23 | Gate(H)1 | High side driver \#1. |
| 24 | GND1 | Return \#1 drivers. |
| 25 | Gate(L)1 | Low side driver \#1. |
| 26 | $\mathrm{V}_{\text {CCL1 }}$ | Power for GATE(L)1. |
| 27 | $\mathrm{V}_{\text {CCL }}$ | Power for internal control circuits. UVLO Sense for Logic connects to this pin. |
| 28 | Rosc | A resistor from this pin to ground sets operating frequency and $\mathrm{V}_{\mathrm{FB}}$ bias current. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Oscillator Frequency


Figure 5. Gate(H) Rise-time vs. Load Capacitance measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 7. Gate(L) Rise-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 4. VFB Bias Current vs. Rosc Value


Figure 6. Gate(H) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{cc}}$ at 5.0 V .


Figure 8. Gate(L) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .

## APPLICATIONS INFORMATION

## FIXED FREQUENCY MULTI-PHASE CONTROL

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5302 uses a two-phase, fixed frequency, Enhanced V ${ }^{2}$ architecture. Each phase is delayed $180^{\circ}$ from the previous phase. Normally GATE(H) transitions high at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator and bring GATE(H) low. Once GATE(H) goes low, it will remain low until the beginning of the next oscillator cycle. While $\operatorname{GATE}(\mathrm{H})$ is high, the enhanced $\mathrm{V}^{2}$ loop will respond to line and load transients. Once GATE $(\mathrm{H})$ is low, the loop will not respond again until the beginning of the next cycle. Therefore, constant frequency Enhanced $\mathrm{V}^{2}$ will typically respond within the off-time of the converter.

The Enhanced $\mathrm{V}^{2}$ architecture measures and adjusts current in each phase. An additional input ( Cx ) for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 9.


Figure 9. Enhanced V ${ }^{2}$ Feedback and Current Sense Scheme

The inductor current is measured across $\mathrm{R}_{\mathrm{S}}$, amplified by CSA and summed with the OFFSET and Output Voltage at the non-inverting input of the PWM comparator. The inductor current provides the PWM ramp and as inductor current increases the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts the cycle with a higher current, the PWM
cycle will terminate earlier providing negative feedback. The CS5302 provides a Cx input for each phase, but the $\mathrm{CS}_{\mathrm{REF}}, \mathrm{V}_{\mathrm{FB}}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{V}_{\mathrm{FB}}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than phases with a smaller current signal.
Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be only $1 / 2$ of the steady state ramp height plus the OFFSET above the output voltage. If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$
\Delta \mathrm{V}=\mathrm{RS} \times \mathrm{CSA} \text { Gain } \times \Delta \mathrm{I}
$$

The single-phase power stage output impedance is:
Single Stage Impedance $=\Delta \mathrm{V} / \Delta \mathrm{I}=\mathrm{R}_{\mathrm{S}} \times$ CSA Gain.
The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few $\mu$ s of a transient before the feedback loop has repositioned the COMP pin.

The peak output current of each phase can also be calculated from;

$$
I_{\text {pkout }}(\text { per phase })=\frac{\mathrm{V}_{\mathrm{COMP}}-\mathrm{V}_{\mathrm{FB}}-\mathrm{V}_{\text {OFFSET }}}{\mathrm{R}_{\mathrm{S}} \times \mathrm{CSA} \text { Gain }}
$$

Figure 10 shows the step response of a single phase with the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current signal, voltage signal and OFFSET exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the current signal level is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 10. Open Loop Operation

## Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 11. In the diagram $L$ is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal the values of R1 and C1 are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} 1 \times \mathrm{C} 1$. If this criteria is met the current sense signal will be the same shape as the inductor current, the voltage signal at Cx will represent the instantaneous value of inductor current and the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$.


Figure 11. Lossless Inductive Current Sensing with Enhanced $\mathbf{V}^{2}$
When choosing or designing inductors for use with inductive sensing tolerances and temperature, effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be
considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 9.

## Current Sharing Accuracy

PCB traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at the same point for each phase and the connection to the $\mathrm{CS}_{\text {REF }}$ should be made so that no phase is favored. (In some cases, especially with inductive sensing, resistance of the pcb can be useful for increasing the current sense resistance.) The total current sense resistance used for calculations must include any pcb trace between the CS inputs and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier Input Mismatch and the value of the current sense element will determine the accuracy of current sharing between phases. The worst case Current Sense Amplifier Input Mismatch is 5.0 mV and will typically be within 3.0 mV . The difference in peak currents between phases will be the CSA Input Mismatch divided by the current sense resistance. If all current sense elements are of equal resistance a 3.0 mV mismatch with a $2.0 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## Operation at > 50\% Duty Cycle

For operation at duty cycles above $50 \%$ Enhanced $V^{2}$ will exhibit subharmonic oscillation unless a compensation ramp is added to each phase. A circuit like the one on the left side of Figure 12 can be added to each current sense network to implement slope compensation. The value of R1 can be varied to adjust the ramp size.


Figure 12. External Slope Compensation Circuit

## Ramp Size and Current Sensing

Because the current ramp is used for both the PWM ramp and to sense current, the inductor and sense resistor values will be constrained. A small ramp will provide a quick transient response by minimizing the difference over which the COMP pin must travel between light and heavy loads, but a steady state ramp of 25 mV -p or greater is typically required to prevent pulse skipping and minimize pulse width jitter. For resistive current sensing, the combination of the inductor and sense resistor values must be chosen to provide a large enough steady state ramp. For large inductor values the sense resistor value must also be increased.

For inductive current sensing, the RC network must meet the requirement of $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} \times \mathrm{C}$ to accurately sense the AC and DC components of the current the signal. Again the values for L and $\mathrm{R}_{\mathrm{L}}$ will be constrained in order to provide a large enough steady state ramp with a compensated current sense signal. A smaller $L$, or a larger $R_{L}$ than optimum might be required. But unlike resistive sensing, with inductive sensing, small adjustments can be made easily with the values of R and C to increase the ramp size if needed.

If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R} \times \mathrm{C}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R} \times \mathrm{C}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During transients the COMP pin will be required to overshoot along with the current signal in order to maintain the output voltage. The $V_{\text {DRP }}$ pin will also overshoot during transients and possibly slow the response. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}$, $\mathrm{R}_{\mathrm{L}}=1.6 \mathrm{~m} \Omega, \mathrm{R} 1=20 \mathrm{k}$ and $\mathrm{C} 1=.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of R 1 should be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu \mathrm{~s}$ time constant. With this compensation the $\mathrm{I}_{\mathrm{LIM}}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 13. Inductive Sensing waveform during a Step with Fast RC Time Constant ( $50 \mu \mathrm{~s} / \mathrm{div}$ )

## Current Limit

Two levels of overcurrent protection are provided. Any time the voltage on a Current Sense pin exceeds CS $_{\text {REF }}$ by more than the Single Phase Pulse by Pulse Current Limit, the PWM comparator for that phase is turned off. This provides fast peak current protection for individual phases. The outputs of all the currents are also summed and filtered to compare an averaged current signal to the voltage on the I $_{\text {LIM }}$ pin. If this voltage is exceeded, the fault latch trips and the Soft Start capacitor is discharged by a $7.5 \mu \mathrm{~A}$ source until the COMP pin reaches 0.2 V . Then Soft Start begins. The converter will continue to operate in this mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced $\mathrm{V}^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET's to shut off and the synchronous MOSFET's to turn on. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in
order to reduce voltage excursions during transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is stepped up and set lower than nominal during heavy loads to reduce overshoot when the load current is stepped up. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example; in a 50 A converter a $1.0 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond quickly to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 14. Adaptive Positioning
The CS5302 can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram on page 2278.)

To set the no-load positioning, a resistor is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to increase the output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of $\mathrm{R}_{\mathrm{OSC}}$. See Figure 4.

During no load conditions the $\mathrm{V}_{\text {DRP }}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor. When output current increases the $V_{\text {DRP }}$ pin increases proportionally and the $V_{\text {DRP }}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to decrease.

The $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{DRP}}$ pins take care of the slower and DC voltage positioning. The first few $\mu \mathrm{s}$ are controlled primarily by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition
to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

Note: Large levels of adaptive positioning can cause pulse width jitter.

## Error Amp Compensation

The transconductance error amplifier requires a capacitor between the COMP pin and GND. Use of values less than 1 nF may result in error amp oscillation of several MHz .

The capacitor between the COMP pin and the inverting error amplifier input and the parallel resistance of the $\mathrm{V}_{\mathrm{FB}}$ resistor and the $\mathrm{V}_{\mathrm{DRP}}$ resistor are used to roll off the error amp gain. The gain is rolled off at a high enough frequency to give a quick transient response, but low enough to cross zero dB well below the switching frequency to minimize ripple and noise on the COMP pin.

## UVLO

The CS5302 has undervoltage lockout functions connected to two pins. One, intended for the logic and low-side drivers, with a 4.4 V turn-on threshold is connected to the $\mathrm{V}_{\mathrm{CCL}}$ pin. A second, intended for the high side drivers, powered from 12 V has a 9.0 V threshold is connected to the $\mathrm{V}_{\mathrm{CCH} 1}$ pin.
Both thresholds must be exceeded for the converter to start.

## Soft Start and Hiccup Mode

A capacitor between the Soft Start pin and GND controls Soft Start and hiccup mode slopes. A $0.1 \mu \mathrm{~F}$ capacitor with the $30 \mu \mathrm{~A}$ charge current will allow the output to ramp up at $0.3 \mathrm{~V} / \mathrm{ms}$ or 1.5 V in 5.0 ms at start-up.

When a fault is detected due to overcurrent or UVLO the converter will enter a low duty cycle hiccup mode. During hiccup mode the converter will not switch from the time a fault is detected until the Soft Start capacitor has discharged below the Soft Start Discharge Threshold and then charged back up above the Channel Start Up Offset.

The Soft Start pin will disable the converter when pulled below 0.3 V .

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically, a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to reroute the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate
drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

Voltage feedback should be taken from a point of the output or the output filter that doesn't favor any one phase. If the feedback connection is closer to one inductor than the others the ripple associated with that phase may appear larger than the ripple associated with the other phases and poor current sharing can result.

The current sense signal is typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as switch nodes and gate drive signals. The paths should be matched as well as possible. It is especially important that all current sense signals be picked off at similar points for accurate current sharing. If the current signal is taken from a place other than directly at the inductor any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistance and should be considered in design calculations. Capacitors for the current feedback networks should be placed as close to the current sense pins as practical.

## DESIGN PROCEDURE

## Current Sensing, Power Stage and Output Filter Components

1. Choose the output filter components to meet peak transient requirements. The formula below can be used to provide an approximate starting point for capacitor choice, but will be inadequate to calculate actual values.

$$
\Delta V_{\text {PEAK }}=(\Delta \mathrm{I} / \Delta \mathrm{T}) \times \mathrm{ESL}+\Delta \mathrm{I} \times \mathrm{ESR}
$$

Ideally the output filter should be simulated with models including ESR, ESL, circuit board parasitics and delays due to switching frequency and converter response. Typically both bulk capacitance (electrolytic, Oscon, etc.,) and low impedance capacitance (ceramic chip) will be required. The bulk capacitance provides "hold up" during the converter response. The low impedance capacitance reduces steady state ripple and bypasses the bulk capacitance during slewing of output current.
2. For inductive current sensing (only) choose the current sense network RC to provide a 25 mV minimum ramp during steady state operation.

$$
\mathrm{R}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\text {IN }}}{\mathrm{F} \times \mathrm{C} \times 25 \mathrm{mV}}
$$

Then choose the inductor value and inherent resistance to satisfy $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} \times \mathrm{C}$.

For ideal current sense compensation the ratio of $L$ and $R_{L}$ is fixed, so the values of $L$ and $R_{L}$ will be a compromise typically with the maximum value $\mathrm{R}_{\mathrm{L}}$ limited by conduction losses or inductor temperature rise and the minimum value of L limited by ripple current.
3. For resistive current sensing choose L and $\mathrm{R}_{\mathrm{S}}$ to provide a steady state ramp greater than 25 mV .

$$
\mathrm{L} / \mathrm{RS}_{\mathrm{S}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{TON} / 25 \mathrm{mV}
$$

Again the ratio of $L$ and $R_{L}$ is fixed and the values of L and $\mathrm{R}_{\mathrm{S}}$ will be a compromise.
4. Calculate the high frequency output impedance (ConverterZ) of the converter during transients. This is the impedance of the Output filter ESR in parallel with the power stage output impedance (PwrstgZ) and will indicate how far from the original level ( $\Delta \mathrm{VR}$ ) the output voltage will typically recover to within one switching cycle. For a good transient response $\Delta \mathrm{VR}$ should be less than the peak output voltage overshoot or undershoot.

$$
\begin{array}{r}
\Delta \mathrm{VR}=\text { ConverterZ } \times \mathrm{ESR} \\
\text { ConverterZ }=\frac{\text { PwrstgZ } \times \mathrm{ESR}}{\text { PwrstgZ }+\mathrm{ESR}}
\end{array}
$$

where:

$$
\text { PwrstgZ }=R_{S} \times \text { CSA Gain } / 3.0
$$

Multiply the converterZ by the output current step size to calculate where the output voltage should recover to within the first switching cycle after a transient. If the ConverterZ is higher than the value required to recover to where the adaptive positioning is set the remainder of the recovery will be controlled by the error amp compensation and will typically recover in $10-20 \mu \mathrm{~s}$.

$$
\Delta \mathrm{VR}=\Delta \mathrm{l} \mathrm{OUT} \times \text { ConverterZ }
$$

Make sure that $\Delta \mathrm{VR}$ is less than the expected peak transient for a good transient response.
5. Adjust L and $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ as required to meet the best combination of transient response, steady state output voltage ripple and pulse width jitter.

## Current Limit

When the sum of the Current Sense amplifiers (VITOtaL) exceeds the voltage on the $\mathrm{I}_{\text {LIM }}$ pin the part will enter hiccup mode. For inductive sensing the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor resistance (or current sense resistor) at max temperature and max current. To set the level of the $\mathrm{I}_{\text {LIM }}$ pin:
6. $\mathrm{V}_{\mathrm{I}(\mathrm{LIM})}=\mathrm{R} \times \operatorname{lOUT}(\mathrm{LIM}) \times \mathrm{CS}$ to ILIM Gain
where: R is $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$; $\mathrm{I}_{\mathrm{OUT}(\mathrm{LIM})}$ is the current limit threshold.
For the overcurrent to work properly the inductor time constant $(L / R)$ should be $\leq$ the Current sense RC.

If the RC is too fast, during step loads the current waveform will appear larger than it is (typically for a few hundred $\mu \mathrm{s}$ ) and may trip the current limit at a level lower than the DC limit.

## Adaptive Positioning

7. To set the amount of voltage positioning below the DAC setting at no load connect a resistor $\left(\mathrm{R}_{\mathrm{V}(\mathrm{FB})}\right)$ between the output voltage and the $\mathrm{V}_{\mathrm{FB}}$ pin. Choose $\mathrm{R}_{\mathrm{V}(\mathrm{FB})}$ as;

$$
\mathrm{R}_{\mathrm{V}(\mathrm{FB})}=\mathrm{NL} \text { Position } / \mathrm{V}_{\mathrm{FB}} \text { Bias Current }
$$

See Figure 4 for $V_{F B}$ Bias Current.
8. To set the difference in output voltage between no load and full load, connect a resistor $\left(\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}\right)$ between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pins. $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ can be calculated in two steps. First calculate the difference between the $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\mathrm{FB}}$ pin at full load. (The $\mathrm{V}_{\mathrm{FB}}$ voltage should be the same as the DAC voltage during closed loop operation.) Then choose the $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ to source enough current across $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ for the desired change in output voltage.

$$
\Delta \mathrm{V} V(\mathrm{DRP})=\mathrm{I} \text { OUTFL } \times \mathrm{R} \times \mathrm{CS} \text { to } \mathrm{V} \text { DRP Gain }
$$

where:
$\mathrm{R}=\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ for one phase;
$\mathrm{I}_{\mathrm{OUTFL}}$ is the full load output current.

$$
\mathrm{RV}(\mathrm{DRP})=\Delta \mathrm{V}_{\mathrm{DRP}} \times \mathrm{RV}_{\mathrm{V}(\mathrm{FB})} / \Delta \mathrm{V}_{\mathrm{OUT}}
$$

## Calculate Input Filter Capacitor Current Ripple

The procedure below assumes that phases do not overlap and output inductor ripple current $(\mathrm{P}-\mathrm{P})$ is less than the average output current of one phase.
9. Calculate Input Current
$\mathrm{I}_{\mathrm{IN}}=\frac{\mathrm{V}_{\mathrm{OUT}} \times \mathrm{IOUT}_{\mathrm{OU}}}{\left(\text { Efficiency } \times \mathrm{V}_{\mathrm{IN}}\right)}$
10. Calculate Duty Cycle (per phase).

Duty Cycle $=\frac{\text { VOUT }}{\left(\text { Efficiency } \times \mathrm{V}_{\mathrm{IN}}\right)}$
11. Calculate Apparent Duty Cycle.

## Apparent Duty Cycle $=$ Duty Cycle $\times$ \# of Phases

12. Calculate Input Filter Capacitor Ripple Current. Use the chart in Figure 15 to calculate the normalized ripple current ( $\mathrm{K}_{\mathrm{RMS}}$ ) based on the reciprocal of Apparent Duty Cycle. Then multiply the input current by $K_{\text {RMS }}$ to obtain the Input Filter Capacitor Ripple Current.
Ripple $($ RMS $)=I_{I N} \times K_{R M S}$


Figure 15. Normalized Input Filter Capacitor Ripple Current

DESIGN EXAMPLE
Choose the component values for a 5.0 V to $1.6 \mathrm{~V}, 35 \mathrm{~A}$ converter with lossless current sensing, adaptive positioning and a 45 A current limit. The adaptive positioning is chosen 30 mV above the nominal $\mathrm{V}_{\text {OUT }}$ at no load and 40 mV below the no-load position with 35 A out. The peak output voltage transient is 70 mV max during a 32 A step current.

## Current Sensing, Power Stage and Output Filter Components

1. Assume $1.5 \mathrm{~m} \Omega$ of output filter ESR.
2. 

$$
\begin{aligned}
& \mathrm{R}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}}}{\mathrm{~F} \times \mathrm{C} \times 25 \mathrm{mV}} \\
&=(5.0-1.6) \times \frac{1.6 / 5.0}{250 \mathrm{k} \times 0.01 \mu \mathrm{~F} \times 25 \mathrm{mV}} \\
&=17.4 \mathrm{k} \Omega \\
& \mathrm{~L} / \mathrm{R}_{\mathrm{L}}=.01 \mu \mathrm{~F} \times 17.47 \mathrm{k} \Omega=174 \mu \mathrm{~s} \\
& \mathrm{Choose} \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{~m} \Omega \\
& \mathrm{~L}=2.0 \mathrm{~m} \Omega \times 174 \mu \mathrm{~s}=348 \mathrm{nH} \\
& \text { 3. } \mathrm{n} / \mathrm{a} \\
& \text { 4. }
\end{aligned}
$$

$$
\begin{aligned}
\text { PwrstgZ } & =R_{L} \times C S A \text { Gain } / 2.0 \\
& =2.0 \mathrm{~m} \Omega \times 3.15 / 2.0=3.1 \mathrm{~m} \Omega \\
\text { ConverterZ } & =\frac{\text { PwrstgZ } \times \mathrm{ESR}}{\text { PwrstgZ }+\mathrm{ESR}} \\
& =\frac{3.1 \mathrm{~m} \Omega \times 1.5 \mathrm{~m} \Omega}{3.1 \mathrm{~m} \Omega+1.5 \mathrm{~m} \Omega} \cong 1.0 \mathrm{~m} \Omega
\end{aligned}
$$

$$
\Delta \mathrm{VR}=1.0 \mathrm{~m} \Omega \times 32 \mathrm{~A}=32 \mathrm{mV}
$$

5. $\mathrm{n} / \mathrm{a}$

## Current Limit

6. 

$\mathrm{V}_{\mathrm{I}}(\mathrm{LIM})=\mathrm{R}_{\mathrm{L}} \times \operatorname{IOUT}(\mathrm{LIM})$ $\times$ CS to LLIM Gain
$=2.0 \mathrm{~m} \Omega \times 45 \mathrm{~A} \times 6.25$
$=562 \mathrm{mV}$

## Adaptive Positioning

7. 

RV(FB) $=$ NL Position/VFB Bias Current $=30 \mathrm{mV} / 6.0 \mu \mathrm{~A}=5.0 \mathrm{k} \Omega$
8.
$\Delta \mathrm{V}_{\mathrm{DRP}}=\mathrm{R}_{\mathrm{L}} \times$ IOUT
$\times$ Current Sense to VDRP Gain

$$
=2.0 \mathrm{~m} \Omega \times 35 \mathrm{~A} \times 3.0
$$

$$
=210 \mathrm{mV}
$$

$\mathrm{RV}(\mathrm{DRP})=\Delta \mathrm{V}_{\mathrm{DRP}} \times \mathrm{RV}(\mathrm{FB}) / \Delta \mathrm{V}_{\mathrm{OUT}}$ $=210 \mathrm{mV} \times 5.0 \mathrm{k} \Omega / 40 \mathrm{mV}$ $=26 \mathrm{k} \Omega$
9.
$\mathrm{I}_{\mathrm{IN}}=1.52 \mathrm{~V} \times \frac{41 \mathrm{~A}}{0.85 \times 12 \mathrm{~V} \mathrm{~N}}=6.1 \mathrm{~A}$
10.

Duty Cycle $=\frac{1.52 \mathrm{~V}}{0.85 \times 12 \mathrm{VIN}}=0.15$
11.

Apparent Duty Cycle $=0.15 \times 2.0=0.3$
12.

RMS ripple $=6.1 \mathrm{~A} \times 1.5=9.2 \mathrm{~A}$

PACKAGE THERMAL DATA

| Parameter |  | 28 Lead SO Wide | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 75 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5303

## Three-Phase Buck Controller with Integrated Gate Drivers

The CS5303 is a three-phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi-phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced $\mathrm{V}^{2 \mathrm{TM}}$ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use.

The CS5303 multi-phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in inductor values and a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

## Features

- Enhanced $\mathrm{V}^{2}$ Control Method
- 5-Bit DAC with $1.0 \%$ Accuracy
- Adjustable Output Voltage Positioning
- 6 On-Board Gate Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors, Sense Resistors, or V-S Control
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On-Board Current Sense Amplifiers
- $3.3 \mathrm{~V}, 1.0 \mathrm{~mA}$ Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through COMP Pin)

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com

SO-28L DW SUFFIX CASE 751F

## MARKING DIAGRAM

## 28



| A | $=$ Assembly Location |
| :--- | :--- |
| WL, L | $=$ Wafer Lot |
| YY, Y | $=$ Year |
| WW, $W$ | $=$ Work Week |

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5303GDW28 | SO-28L | 27 Units/Rail |
| CS5303GDWR28 | SO-28L | 1000 Tape \& Reel |



Figure 1. Application Diagram, 12 V to 1.5 V, 60 A Converter

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Operating Junction Temperature | Unit |  |
| Lead Temperature Soldering: : | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range (SMD styles only) (Note 1 ) | 230 peak, | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power for logic and Gate(L)1 | $\mathrm{V}_{\text {CCLL1 }}$ | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for Gate(L)2 and Gate(L)3 | $\mathrm{V}_{\text {CCL23 }}$ | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for Gate(H)1 and Gate(H)2 | $\mathrm{V}_{\text {CCH12 }}$ | 20 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power Gate(H)3 | $\mathrm{V}_{\text {CCH3 }}$ | 20 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |

## ABSOLUTE MAXIMUM RATINGS (continued)

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Voltage Feedback Compensation Network | COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Input | $V_{\text {FB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Output for adjusting adaptive voltage positioning | $\mathrm{V}_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Frequency Resistor | Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Reference Output | REF | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| High-Side FET Drivers | Gate(H)1-3 | 20 V | $\begin{gathered} -0.3 \mathrm{~V} \\ -2 \mathrm{~V} \text { for } 100 \mathrm{nS} \end{gathered}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Low-Side FET Drivers | Gate(L)1-3 | 16 V | $\begin{gathered} -0.3 \mathrm{~V} \\ -2 \mathrm{~V} \text { for } 100 \mathrm{nS} \end{gathered}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Return for \#1 Driver | Gnd1 | 0.3 V | -0.3 V | $2 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Return for logic and \#2 Driver | GndL2 | N/A | N/A | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Return for \#3 Driver | Gnd3 | 0.3 V | -0.3 V | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Current Sense for phases 1-3 | CS1-CS3 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Limit Set Point | ILIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Sense Reference | $\mathrm{CS}_{\text {REF }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage ID DAC Inputs | VID0-4 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\quad\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $\mathbf{0}=$ Connected to $\mathrm{V}_{\mathrm{SS}} ; 1=$ Open or Pull-up to 3.3 V )

| Accuracy (all codes) |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {ID4 }}$ | $\mathrm{V}_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $\mathrm{V}_{\text {IDO }}$ | Measure $\mathrm{V}_{\mathrm{FB}}=$ COMP |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | - | 1.064 | 1.075 | 1.086 | V |
| 1 | 1 | 1 | 1 | 0 | - | 1.089 | 1.100 | 1.111 | V |
| 1 | 1 | 1 | 0 | 1 | - | 1.114 | 1.125 | 1.136 | V |
| 1 | 1 | 1 | 0 | 0 | - | 1.139 | 1.150 | 1.162 | V |
| 1 | 1 | 0 | 1 | 1 | - | 1.163 | 1.175 | 1.187 | V |
| 1 | 1 | 0 | 1 | 0 | - | 1.188 | 1.200 | 1.212 | V |
| 1 | 1 | 0 | 0 | 1 | - | 1.213 | 1.225 | 1.237 | V |
| 1 | 1 | 0 | 0 | 0 | - | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 1 | 1 | 1 | - | 1.262 | 1.275 | 1.288 | V |
| 1 | 0 | 1 | 1 | 0 | - | 1.287 | 1.300 | 1.313 | V |
| 1 | 0 | 1 | 0 | 1 | - | 1.312 | 1.325 | 1.338 | V |
| 1 | 0 | 1 | 0 | 0 | - | 1.350 | 1.364 | V |  |
| 1 | 0 | 0 | 1 | 1 | - | 1.361 | 1.375 | 1.389 | V |
| 1 | 0 | 0 | 1 | 0 | - | 1.386 | 1.400 | 1.414 | V |
| 1 | 0 | 0 | 0 | 1 |  | 1.436 | 1.450 | 1.465 | V |
| 1 | 0 | 0 | 0 | 0 |  | 1.425 | 1.439 | V |  |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}\right.$; $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $\mathbf{0}=$ Connected to $\mathrm{V}_{\mathrm{SS}} ; 1=$ Open or Pull-up to 3.3 V )

| 0 | 1 | 1 | 1 | 1 | - | 1.460 | 1.475 | 1.490 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 1 | 1 | 1 | 0 | - | 1.485 | 1.500 | 1.515 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.510 | 1.525 | 1.540 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.535 | 1.550 | 1.566 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.559 | 1.575 | 1.591 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.584 | 1.600 | 1.616 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.609 | 1.625 | 1.641 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.634 | 1.650 | 1.667 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.683 | 1.700 | 1.717 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.708 | 1.725 | 1.742 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.733 | 1.750 | 1.768 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.757 | 1.775 | 1.793 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.782 | 1.800 | 1.818 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.807 | 1.825 | 1.843 | V |
| 0 | 0 | 0 | 0 | 0 | - | 1.832 | 1.850 | 1.869 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID } 4}, \mathrm{~V}_{\text {ID } 3}, \mathrm{~V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 1.00 | 1.25 | 1.50 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{I D 4}, \mathrm{~V}_{\text {ID }}, \mathrm{V}_{\text {ID } 2}, \mathrm{~V}_{\text {ID }}, \mathrm{V}_{\text {ID }}$ | 25 | 50 | 100 | k $\Omega$ |
| Pull-up Voltage |  |  |  |  | - | 3.15 | 3.30 | 3.45 | V |

## Voltage Feedback Error Amplifier

| $\mathrm{V}_{\text {FB }}$ Bias Current (Note 2) | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.9 \mathrm{~V}$ | 16.8 | 19.0 | 21.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.8 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.9 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Discharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}$ COMP $<+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3 | 60 | 90 | - | - |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ COMP Capacitor | - | 400 | - | kHz |
| PSRR @ 1 kHz | - | - | 70 | - | dB |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V}$; COMP Open; DAC $=00000$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V}$; COMP Open; DAC $=00000$ | - | 0.1 | 0.2 | V |
| Hiccup Latch Discharge Current | - | 2.0 | 5.0 | 10 | $\mu \mathrm{A}$ |
| COMP Discharge Ratio | - | 4.0 | 6.0 | 10 | - |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of Rosc per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{~L}_{\mathrm{LIM}} \geq 1 \mathrm{~V}$;unless otherwise specified)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PWM Comparators |  |  |  |  |  |
| Minimum Pulse Width | Measured from CSx to GATE(H) $\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS}_{\mathrm{REF}}\right)=1.0 \mathrm{~V}, \mathrm{~V}(\mathrm{COMP})=1.5 \mathrm{~V}$ <br> 60 mV step applied between $\mathrm{V}_{\text {CSX }}$ and $\mathrm{V}_{\text {CREF }}$ | - | 350 | 515 | ns |
| Channel Start Up Offset | $\begin{aligned} & \mathrm{V}(\mathrm{CS} 1)=\mathrm{V}(\mathrm{CS} 2)=\mathrm{V}(\mathrm{CS} 3)=\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)=0.3 \\ & \mathrm{~V}(\mathrm{CS} \text { REF })=0 \mathrm{~V} \text {; Measure } \mathrm{V}(\mathrm{COMP}) \text { when } \\ & \text { GATE1 }(\mathrm{H}), 2(\mathrm{H}), 3(\mathrm{H}) \text { switch high } \end{aligned}$ | 0.4 | 0.5 | - | V |

Gate(H) and Gate(L)

| High Voltage (AC) | Note 4 Measure $\mathrm{V}_{\mathrm{CCLX}}$ - Gate(L) or $V_{\mathrm{CCHX}} \text { - Gate }(\mathrm{H})$ | - | 0 | 1.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Note 4, Measure Gate(L) or Gate(H) | - | 0 | 0.5 | V |
| Rise Time Gate(H)x | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Rise Time Gate(L) x | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time Gate(H)x | $8.0 \mathrm{~V}>\mathrm{GATE}>1.0 \mathrm{~V}$; $\mathrm{V}_{\mathrm{CCHX}}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time Gate(L) | 8.0 V > GATE > 1.0 V ; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Gate(H) to Gate(L) Delay | Gate(H) < 2.0 V , Gate(L) $>2 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| Gate(L) to Gate(H) Delay | Gate(L) < 2.0 V , Gate(H) $>2 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-down | Force $100 \mu \mathrm{~A}$ into Gate Driver with no power applied to $\mathrm{V}_{\mathrm{CCHX}}$ and $\mathrm{V}_{\mathrm{CCLX}}=2 \mathrm{~V}$. | - | 1.2 | 1.6 | V |

## Oscillator

| Switching Frequency | Measure any phase (ROSC $=53.6 \mathrm{k}$ ) | 220 | 250 | 280 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | Note 4 Measure any phase (ROSC $=32.4 \mathrm{k}$ ) | 300 | 400 | 500 | kHz |
| Switching Frequency | Note 4 Measure any phase (ROSC $=16.2 \mathrm{k})$ | 600 | 800 | 1000 | kHz |
| $\mathrm{R}_{\text {OSC }}$ Voltage | - | - | 1.00 | - | V |
| Phase Delay | - | 105 | 120 | 135 | deg |

Adaptive Voltage Positioning

| $V_{\text {DRP }}$ Output Voltage to DAC ${ }_{\text {OUT }}$ Offset | $\begin{aligned} & \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS} 3=\mathrm{CS} \text { REF }, \mathrm{V}_{\mathrm{FB}}=\mathrm{COMP} \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | -20 | - | 20 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum $\mathrm{V}_{\text {DRP }}$ Voltage | $\begin{gathered} \left\|(C S 1=C S 2=C S 3)-C_{\text {REF }}\right\|=50 \mathrm{mV}, \\ V_{F B}=C O M P, \text { Measure } V_{D R P}-C O M P \end{gathered}$ | 360 | 465 | 570 | mV |
| Current Sense Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.4 | 3.0 | 3.8 | V/V |

Current Sensing and Sharing

| CS1-CS3 Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS ${ }_{\text {REF }}$ Input Bias Current | - | - | 0.6 | 6.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifiers Gain | - | 3.8 | 4.3 | 4.8 | V/V |
| Current Sense Amp Mismatch (The sum of offset and gain errors) | Note $40 \leq\left(C S x-S_{\text {REF }}\right) \leq 50 \mathrm{mV}$ | -5.0 | - | 5.0 | mV |
| Current Sense Amplifiers Input Common Mode Range Limit | Note 47 V < $\mathrm{V}_{\text {CCLL }}<12 \mathrm{~V}$ | 0 | - | $\mathrm{V}_{\text {CCLL } 1}-2$ | V |
| Current Sense Input to ILIM Gain | 0.25 V < $\mathrm{I}_{\text {LIM }}<1.20 \mathrm{~V}$ | 5.0 | 6.5 | 8.0 | V/V |
| Current Limit Filter Slew Rate | Note 4 | 7.5 | 15.0 | 40.0 | $\mathrm{mV} / \mu \mathrm{s}$ |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code 10000, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1 \mathrm{~V}$;unless otherwise specified)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Sensing and Sharing |  |  |  |  |  |
| ILIM Bias Current | $0<\mathrm{I}_{\text {LIM }}<1.0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse by Pulse Current Limit: V(CSx) - V(CS REF) | - | 60 | 70 | 90 | mV |
| Current Share Amplifier Bandwidth | Note 5 | 1.0 | - | - | mHz |

## Reference Output

| $V_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{I}\left(\mathrm{V}_{\mathrm{REF}}\right)<1.0 \mathrm{~mA}$ | 3.15 | 3.25 | 3.35 | V |
| :--- | :--- | :--- | :--- | :--- | :---: |

General Electrical Specifications

| $\mathrm{V}_{\text {CCLL } 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 23 | 28 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CCL23 }}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 8.0 | 11 | mA |
| $\mathrm{V}_{\mathrm{CCH} 12}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 5.5 | 7.0 | mA |
| $\mathrm{V}_{\mathrm{CCH} 3}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 2.5 | 3.5 | mA |
| $\mathrm{V}_{\text {CCLL } 1}$ Start Threshold | GATEs switching, COMP charging | 4.05 | 4.40 | 4.70 | V |
| $\mathrm{V}_{\text {CCLL } 1}$ Stop Threshold | GATEs stop switching, COMP discharging | 3.75 | 4.20 | 4.60 | V |
| $V_{\text {CCLL1 }}$ Hysteresis | GATEs not switching, COMP not charging | 100 | 200 | 300 | mV |
| $\mathrm{V}_{\text {CCH12 }}$ Start Threshold | GATEs switching, COMP charging | 1.7 | 1.9 | 2.1 | V |
| $\mathrm{V}_{\mathrm{CCH12}}$ Stop Threshold | GATEs stop switching, COMP discharging | 1.55 | 1.75 | 1.90 | V |
| $\mathrm{V}_{\mathrm{CCH} 12}$ Hysteresis | GATEs not switching, COMP not charging | 100 | 200 | 300 | mV |

5. Guaranteed by design. Not tested in production.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 28 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 1 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 2 | $V_{\text {FB }}$ | Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between $V_{F B}$ and $V_{\text {OUT }}$. The input bias current of the $\mathrm{V}_{\mathrm{FB}}$ pin and the resistor value determine output voltage offset for zero output current. Short $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\text {OUT }}$ for no AVP. |
| 3 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to set amount AVP or leave this pin open for no AVP. |
| 4-6 | CS1-CS3 | Current sense amplifier inputs. Connect current sense network for the corresponding phase to each input. |
| 7 | $\mathrm{CS}_{\text {REF }}$ | Reference for current sense amplifiers. To balance input offset voltages between the inverting and noninverting inputs of the current sense amplifiers, connect a resistor between CS REF and the output voltage. The value should be $1 / 3$ of the value of the resistors connected to the CSx pins. |
| 8-12 | VID4-VID0 | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |
| 13 | ILIM | Sets threshold for current limit. Connect to reference through a resistive divider. |

PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 28 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 14 | REF | Reference output. Decouple with $0.1 \mu \mathrm{~F}$ to GndL2 |
| 15 | $\mathrm{V}_{\mathrm{CCH} 3}$ | Power for Gate(H)3. |
| 16 | Gate(H)3 | High side driver \#3. |
| 17 | Gnd3 | Return for \#3 drivers. |
| 18 | Gate(L)3 | Low side driver \#3. |
| 19 | $\mathrm{V}_{\text {CCL23 }}$ | Power for Gate(L)2 and Gate(L)3. |
| 20 | Gate(L)2 | Low side driver \#2. |
| 21 | GndL2 | Return for \#2 driver, internal control circuits and IC substrate connection. |
| 22 | Gate(H)2 | High side driver \#2. |
| 23 | $\mathrm{V}_{\mathrm{CCH} 12}$ | Power for Gate(H)1 and Gate(H)2. UVLO Sense for High Side Driver supply connects to this pin. |
| 24 | Gate(H)1 | High side driver \#1. |
| 25 | Gnd1 | Return for \#1 drivers. |
| 26 | Gate(L)1 | Low side driver \#1. |
| 27 | $\mathrm{V}_{\text {CCLL } 1}$ | Power for internal control circuits and Gate(L)1. UVLO Sense for Logic and Low Side Driver supply connects to this pin. |
| 28 | Rosc | A resistor from this pin to ground sets operating frequency and $\mathrm{V}_{\mathrm{FB}}$ bias current. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Oscillator Frequency


Figure 5. Gate(H) Rise-time vs. Load Capacitance measured from 1 V to 4 V with $\mathrm{V}_{\mathrm{cc}}$ at 5 V .


Figure 7. Gate(H) Fall-time vs. Load Capacitance measured from 4 V to 1 V with $\mathrm{V}_{\mathrm{CC}}$ at 5 V .


Figure 4. VFB Bias Current vs. Rosc Value


Figure 6. Gate(L) Rise-time vs. Load Capacitance measured from 4 V to 1 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5 V .


Figure 8. Gate(L) Fall-time vs. Load Capacitance measured from 4 V to 1 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5 V .

## APPLICATIONS INFORMATION

## FIXED FREQUENCY MULTI-PHASE CONTROL

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5303 uses a three-phase, fixed frequency, enhanced $\mathrm{V}^{2}$ architecture. Each phase is delayed $120^{\circ}$ from the previous phase. Normally GATE(H) transitions high at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator and bring GATE(H) low. Once GATE(H) goes low, it will remain low until the beginning of the next oscillator cycle. While $\operatorname{GATE}(\mathrm{H})$ is high, the enhanced $\mathrm{V}^{2}$ loop will respond to line and load transients. Once GATE $(\mathrm{H})$ is low, the loop will not respond again until the beginning of the next cycle. Therefore, constant frequency enhanced $\mathrm{V}^{2}$ will typically respond within the off-time of the converter.

The enhanced $\mathrm{V}^{2}$ architecture measures and adjusts current in each phase. An additional input ( $\mathrm{C}_{\mathrm{X}}$ ) for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 9.


Figure 9. Enhanced V ${ }^{2}$ Feedback and Current Sense Scheme

The inductor current is measured across $\mathrm{R}_{\mathrm{S}}$, amplified by CSA and summed with the OFFSET and Output Voltage at the non-inverting input of the PWM comparator. The inductor current provides the PWM ramp and as inductor current increases the voltage on the positive pin of the pwm
comparator rises and terminates the pwm cycle. If the inductor starts the cycle with a higher current the PWM cycle will terminate earlier providing negative feedback. The CS5303 provides a $\mathrm{C}_{\mathrm{X}}$ input for each phase, but the $\mathrm{CS}_{\mathrm{REF}}, \mathrm{V}_{\mathrm{FB}}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{V}_{\mathrm{FB}}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than phases with a smaller current signal.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. If the COMP pin is held steady and the inductor current changes there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$
\Delta \mathrm{V}=\mathrm{RS} \times \mathrm{CSA} \text { Gain } \times \Delta \mathrm{I}
$$

The single-phase power stage output impedance is;
Single Stage Impedance $=\Delta \mathrm{V} / \Delta \mathrm{I}=\mathrm{RS} \times$ CSA Gain.
The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few $\mu$ s of a transient before the feedback loop has repositioned the COMP pin.

The peak output current of each phase can also be calculated from;

$$
\text { Ipkout }(\text { per phase })=\frac{V_{C O M P}-V_{F B}-V_{O F F S E T}}{R_{S} \times C S A} \text { Gain }
$$

Figure 10 shows the step response of a single phase with the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides the pwm ramp through the Current Share Amplifier. The pwm cycle ends when the sum of the current signal, voltage signal and OFFSET exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next pwm cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the current signal level is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 10. Open Loop Operation

## Inductive Current Sensing

For lossless sensing current can be sensed across the inductor as shown below in Figure 11. In the diagram L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal the values of R1 and C 1 are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} 1 \times \mathrm{C} 1$. If this criteria is met the current sense signal will be the same shape as the inductor current, the voltage signal at Cx will represent the instantaneous value of inductor current and the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$.


Figure 11. Lossless Inductive Current Sensing with Enhanced V ${ }^{2}$
When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be
considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 9.

## Current Sharing Accuracy

PCB traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at the same point for each phase and the connection to the $\mathrm{CS}_{\text {REF }}$ should be made so that no phase is favored. (In some cases, especially with inductive sensing, resistance of the pcb can be useful for increasing the current sense resistance.) The total current sense resistance used for calculations must include any pcb trace between the CS inputs and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier Input Mismatch and the value of the current sense element will determine the accuracy of current sharing between phases. The worst case Current Sense Amplifier Input Mismatch is 5 mV and will typically be within 3 mV . The difference in peak currents between phases will be the CSA Input Mismatch divided by the current sense resistance. If all current sense elements are of equal resistance a 3 mV mismatch with a $2 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## Operation at > 50\% Duty Cycle

For operation at duty cycles above $50 \%$ Enhanced V ${ }^{2}$ will exhibit subharmonic oscillation unless a compensation ramp is added to each phase. A circuit like the one on the left side of Figure 12 can be added to each current sense network to implement slope compensation. The value of R1 can be varied to adjust the ramp size.


Figure 12. External Slope Compensation Circuit

## Ramp Size and Current Sensing

Because the current ramp is used for both the PWM ramp and to sense current, the inductor and sense resistor values will be constrained. A small ramp will provide a quick transient response by minimizing the difference over which the COMP pin must travel between light and heavy loads, but a steady state ramp of $25 \mathrm{mV}_{\mathrm{P}-\mathrm{P}}$ or greater is typically required to prevent pulse skipping and minimize pulse width jitter. For resistive current sensing the combination of the inductor and sense resistor values must be chosen to provide a large enough steady state ramp. For large inductor values the sense resistor value must also be increased.

For inductive current sensing the RC network must meet the requirement of $L / R_{L}=R \times C$ to accurately sense the $A C$ and DC components of the current the signal. Again the values for L and $\mathrm{R}_{\mathrm{L}}$ will be constrained in order to provide a large enough steady state ramp with a compensated current sense signal. A smaller $L$, or a larger $R_{L}$ than optimum might be required. But unlike resistive sensing, with inductive sensing small adjustments can be made easily with the values of R and C to increase the ramp size if needed.

If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R} \times \mathrm{C}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R} \times \mathrm{C}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During transients the COMP pin will be required to overshoot along with the current signal in order to maintain the output voltage. The $\mathrm{V}_{\mathrm{DRP}}$ pin will also overshoot during transients and possibly slow the response. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}$, $\mathrm{R}_{\mathrm{L}}=1.6 \mathrm{~m} \Omega, \mathrm{R} 1=20 \mathrm{k}$ and $\mathrm{C} 1=.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of R1 should be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu \mathrm{~s}$ time constant. With this compensation the $\mathrm{I}_{\text {LIM }}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 13. Inductive Sensing waveform during a Step with Fast RC Time Constant ( $50 \mathrm{\mu s} / \mathrm{div}$ )

## Current Limit

Two levels of overcurrent protection are provided. Any time the voltage on a Current Sense pin exceeds CS REF by more than the Single Phase Pulse by Pulse Current Limit, the pwm comparator for that phase is turned off. This provides fast peak current protection for individual phases. The outputs of all the currents are also summed and filtered to compare an averaged current signal to the voltage on the I $_{\text {LIM }}$ pin. If this voltage is exceeded, the fault latch trips and the SS capacitor is discharged by a $5 \mu \mathrm{~A}$ source until the COMP pin reaches 0.2 V . Then soft-start begins. The converter will continue to operate in this mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the enhanced $\mathrm{V}^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET's to shut off, and the synchronous MOSFET's to turn on. This results in a "crowbar" action to clamp the output voltage and prevents damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in
order to reduce voltage excursions during transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher at light loads to reduce output voltage sag when the load current is stepped up and set lower during heavy loads to reduce overshoot when the load current is stepped up. For low current applications a droop resistor can provide fast accurate adaptive positioning. However at high currents, the loss in a droop resistor becomes excessive. For example; in a 50 A converter a $1 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond quickly to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 14. Adaptive Positioning
The CS5303 uses two methods to provide fast and accurate adaptive positioning. For low frequency positioning the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{DRP}}$ pins are used to adjust the output voltage with varying load currents. For high frequency positioning, the current sense input pins can be used to control the power stage output impedance. The transition between fast and slow positioning is adjusted by the error amp compensation.

The CS5303 can be configured to adjust the output voltage based on the output current of the converter. The adaptive positioning circuit is designed to select the DAC setting as the maximum output voltage. (Refer to Application Diagram on page 2294.)

To set the no-load positioning a resistor (R9) is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to decrease the output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of ROSC. See Figure 4 on the datasheet.

During no load conditions the $\mathrm{V}_{\text {DRP }}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor (R8). When output current
increases the $\mathrm{V}_{\mathrm{DRP}}$ pin increases proportionally and the $\mathrm{V}_{\text {DRP }}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to further decrease.

The $V_{\text {FB }}$ and $V_{\text {DRP }}$ pins take care of the slower and DC voltage positioning. The first few $\mu \mathrm{s}$ are controlled primarily by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

Note: Large levels of adaptive positioning can cause pulse width jitter.

## Error Amp Compensation

The transconductance error amplifier can be configured to provide both a slow soft-start and a fast transient response. C4 in the main applications diagram controls soft-start. A $0.1 \mu \mathrm{~F}$ capacitor with the $30 \mu \mathrm{~A}$ error amplifier output capability will allow the output to ramp up at $0.3 \mathrm{~V} / \mathrm{ms}$ or 1.5 V in 5 ms .

R10 is connected in series with C 4 to allow the error amplifier to slew quickly over a narrow range during load transients. Here the $30 \mu \mathrm{~A}$ error amplifier output capability works against $10 \mathrm{k} \Omega$ (R10) to limit the window of fast slewing too 300 mV - enough to allow for fast transients, but not enough to interfere with soft-start. This window will be noticeable as a step in the COMP pin voltage at start-up. The size of this step must be kept smaller than the Channel Start-Up Offset (nominally 0.4 V ) for proper soft-start operation. If adaptive positioning is used the R9 and R8 form a divider with the $\mathrm{V}_{\mathrm{DRP}}$ end held at the DAC voltage during start-up, which effectively makes the Channel Start-Up Offset larger.
C12 is included for error amp stability. A capacitive load is required on the error amp output. Use of values less than 1 nF may result in error amp oscillation of several MHz .
C 11 and the parallel resistance of the $\mathrm{V}_{\mathrm{FB}}$ resistor (R9) and the $\mathrm{V}_{\mathrm{DRP}}$ resistor (R8) are used to roll off the error amp gain. The gain is rolled off at a high enough frequency to give a quick transient response, but low enough to cross zero dB well below the switching frequency to minimize ripple and noise on the COMP pin.

## UVLO

The CS5303 has undervoltage lockout functions connected to two pins. One intended for the logic and low-side drivers with a 4.4 V turn-on threshold is connected to the $\mathrm{V}_{\text {CCLL1 }}$ pin. A second for the high side drivers has a 2 V threshold and is connected to the $\mathrm{V}_{\mathrm{CCH} 12}$ pin.

The UVLO threshold for the high side drivers was chosen at a low value to allow for flexibility in the part and an input voltage as low as 3.3 V. In many applications this will be disabled or will only check that the applicable supply is on - not that it is at a high enough voltage to run the converter.

For the $12 \mathrm{~V}_{\text {IN }}$ converter in the application diagram on page 2294 the UVLO pin for the high side driver is pulled up by the 5 V supply (through two diode drops) and the function is not used. The diode between the COMP pin and the 12 V supply holds the COMP pin near Gnd and prevents start-up while the 12 V supply is off. In an application where a higher UVLO threshold is necessary a circuit like the one in Figure 15 will lock out the converter until the 12 V supply exceeds 9 V .


Figure 15. External UVLO Circuit

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to reroute the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

Voltage feedback should be taken from a point of the output or the output filter that doesn't favor any one phase. If the feedback connection is closer to one inductor than the others the ripple associated with that phase may appear larger than the ripple associated with the other phases and poor current sharing can result.

The current sense signal is typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as switch nodes and gate drive signals. The paths should be matched as well as possible. It is especially important that all current sense signals be picked off at similar points for accurate current sharing. If the current signal is taken from a place other than directly at the inductor
any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistance and should be considered in design calculations. Capacitors for the current feedback networks should be placed as close to the current sense pins as practical.

## DESIGN PROCEDURE

## Current Sensing, Power Stage and Output Filter Components

1. Choose the output filter components to meet peak transient requirements. The formula below can be used to provide an approximate starting point for capacitor choice, but will be inadequate to calculate actual values.

$$
\Delta \mathrm{V}_{\mathrm{PEAK}}=(\Delta \mathrm{I} / \Delta \mathrm{T}) \times \mathrm{ESL}+\Delta \mathrm{I} \times \mathrm{ESR}
$$

Ideally the output filter should be simulated with models including ESR, ESL, circuit board parasitics and delays due to switching frequency and converter response. Typically both bulk capacitance (electrolytic, Oscon, etc,) and low impedance capacitance (ceramic chip) will be required. The bulk capacitance provides "hold up" during the converter response. The low impedance capacitance reduces steady state ripple and bypasses the bulk capacitance during slewing of output current.
2. For inductive current sensing (only) choose the current sense network RC to provide a 25 mV minimum ramp during steady state operation.

$$
\mathrm{R}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}}}{\mathrm{~F} \times \mathrm{C} \times 25 \mathrm{mV}}
$$

Then choose the inductor value and inherent resistance to satisfy $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} \times \mathrm{C}$.
For ideal current sense compensation the ratio of L and $R_{L}$ is fixed, so the values of $L$ and $R_{L}$ will be a compromise typically with the maximum value $R_{L}$ limited by conduction losses or inductor temperature rise and the minimum value of $L$ limited by ripple current.
3. For resistive current sensing choose $L$ and $R_{S}$ to provide a steady state ramp greater than 25 mV .

$$
\mathrm{L} / \mathrm{RS}_{\mathrm{S}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{T} \mathrm{ON} / 25 \mathrm{mV}
$$

Again the ratio of L and $\mathrm{R}_{\mathrm{L}}$ is fixed and the values of L and $\mathrm{R}_{\mathrm{S}}$ will be a compromise.
4. Calculate the high frequency output impedance (ConverterZ) of the converter during transients. This is the impedance of the Output filter ESR in parallel with the power stage output impedance (PwrstgZ) and will indicate how far from the original level ( $\Delta \mathrm{VR}$ ) the output voltage will typically recover to within one switching cycle. For a good transient response $\Delta \mathrm{VR}$ should be less than the peak output voltage overshoot or undershoot.

$$
\begin{array}{r}
\Delta V R=\text { ConverterZ } \times \text { ESR } \\
\text { ConverterZ }=\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+ \text { ESR }}
\end{array}
$$

where:

$$
\text { PwrstgZ }=\text { RS } \times \text { CSA Gain } / 3
$$

Multiply the converterZ by the output current step size to calculate where the output voltage should recover to within the first switching cycle after a transient. If the ConverterZ is higher than the value required to recover to where the adaptive positioning is set the remainder of the recovery will be controlled by the error amp compensation and will typically recover in $10-20 \mu \mathrm{~s}$.

$$
\Delta \mathrm{VR}=\Delta \mathrm{I} \mathrm{OUT} \times \text { ConverterZ }
$$

Make sure that $\Delta \mathrm{VR}$ is less than the expected peak transient for a good transient response.
5. Adjust L and $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ as required to meet the best combination of transient response, steady state output voltage ripple and pulse width jitter.

## Current Limit

When the sum of the Current Sense amplifiers ( $\mathrm{V}_{\text {ITOTAL }}$ ) exceeds the voltage on the $\mathrm{I}_{\text {LIM }}$ pin the part will enter hiccup mode. For inductive sensing the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor resistance (or current sense resistor) at max temperature and max current. To set the level of the $I_{\text {LIM }}$ pin:
6. $\mathrm{V}_{\mathrm{I}(\mathrm{LIM})}=\mathrm{R} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS}$ to ILIM Gain
where:
R is $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$;
$\mathrm{I}_{\mathrm{OUT}(\mathrm{LIM})}$ is the current limit threshold.
For the overcurrent to work properly the inductor time constant (L/R) should be $\leq$ the Current sense RC. If the RC is too fast, during step loads the current waveform will appear larger than it is (typically for a few hundred $\mu \mathrm{s}$ ) and may trip the current limit at a level lower than the DC limit.

## Adaptive Positioning

7. To set the amount of voltage positioning below the DAC setting at no load connect a resistor $\left(\mathrm{R}_{\mathrm{V}}(\mathrm{FB})\right)$ between the output voltage and the $\mathrm{V}_{\mathrm{FB}}$ pin. Choose $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ as:

$$
R \mathrm{~V}(\mathrm{FB})=\mathrm{NL} \text { Position/VFB Bias Current }
$$

See Figure 4 for $\mathrm{V}_{\mathrm{FB}}$ Bias Current.
8. To set the difference in output voltage between no load and full load, connect a resistor ( $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ ) between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pins. $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ can be calculated in two steps. First calculate the difference between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pin at full load. (The $\mathrm{V}_{\mathrm{FB}}$ voltage should be the same as the DAC voltage during closed loop operation.) Then choose the $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ to source enough current across $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ for the desired change in output voltage.

$$
\Delta \mathrm{V}_{\mathrm{V}(\mathrm{DRP})}=\mathrm{I}_{\mathrm{OUTFL}} \times \mathrm{R} \times \mathrm{CS} \text { to } \mathrm{V}_{\mathrm{DRP}} \text { Gain }
$$

where:
$R=R_{L}$ or $R_{S}$ for one phase;
$\mathrm{I}_{\text {OUTFL }}$ is the full load output current.

$$
\mathrm{RV}(\mathrm{DRP})=\Delta \mathrm{V}_{\mathrm{DRP}} \times \mathrm{RV}(\mathrm{FB}) / \Delta \mathrm{V}_{\mathrm{OUT}}
$$

## DESIGN EXAMPLE

Choose the component values for lossless current sensing, adaptive positioning and current limit for a 60 A converter. The adaptive positioning is chosen 50 mV below the maximum V position with 60 A out. The peak output voltage transient is 100 mV max during a 60 A step current. The overcurrent limit is nominally 75 A .

## Current Sensing, Power Stage and Output Filter Components

1. Assume $1.5 \mathrm{~m} \Omega$ of output filter ESR.

$$
\begin{aligned}
& \text { 2. } \mathrm{R}=\left(\mathrm{V} \text { IN }-\mathrm{V}_{\text {OUT }}\right) \times\left(\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}}\right) /(\mathrm{F} \times \mathrm{C} \times 25 \mathrm{mV}) \\
& =(12-1.5) \times(1.5 / 12) /(250 \mathrm{k} \times .01 \mu \mathrm{~F} \times 25 \mathrm{mV}) \\
& =21 \mathrm{k} \Omega \Rightarrow \text { Choose } 20 \mathrm{k} \Omega \\
& \mathrm{~L} / \mathrm{R}_{\mathrm{L}}=.01 \mu \mathrm{~F} \times 20 \mathrm{k} \Omega=200 \mu \mathrm{~s} \\
& \text { Choose } R_{L}=2 \mathrm{~m} \Omega \\
& \mathrm{~L}=2 \mathrm{~m} \Omega \times 200 \mu \mathrm{~s}=400 \mathrm{nH} \\
& \text { 3. } \mathrm{n} / \mathrm{a} \\
& \text { 4. PwrstgZ }=R_{L} \times \text { CSA Gain } / 3 \\
& =1.5 \mathrm{~m} \Omega \times 4.2 / 3=2.1 \mathrm{~m} \Omega \\
& \text { ConverterZ }=\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+ \text { ESR }} \\
& =\frac{2.8 \mathrm{~m} \Omega \times 1.5 \mathrm{~m} \Omega}{2.8 \mathrm{~m} \Omega+1.5 \mathrm{~m} \Omega} \cong 1 \mathrm{~m} \Omega \\
& \Delta \mathrm{VR}=1.2 \mathrm{~m} \Omega \times 60 \mathrm{~A}=60 \mathrm{mV}
\end{aligned}
$$

5. n/a

## Current Limit

6. $\begin{aligned} \mathrm{V}_{\mathrm{I}(\mathrm{LIM})} & =\mathrm{R}_{\mathrm{L}} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS} \text { to ILIM Gain } \\ & =1.5 \mathrm{~m} \Omega \times 75 \mathrm{~A} \times 6.5=731 \mathrm{mV}\end{aligned}$

## Adaptive Positioning

7. $\mathrm{RV}(\mathrm{FB})=$ NL Position $/ \mathrm{V}$ FB Bias Current

$$
=50 \mathrm{mV} / 19 \mu \mathrm{~A}=2.63 \mathrm{k} \Omega
$$

8. $\Delta \mathrm{V}_{\mathrm{DRP}}=\mathrm{R}_{\mathrm{L}} \times$ IOUT $\times$ Current Sense to VDRP Gain

$$
=2 \mathrm{~m} \Omega \times 60 \mathrm{~A} \times 3=360 \mathrm{mV}
$$

$$
\mathrm{RV}_{\mathrm{V}(\mathrm{DRP})}=\Delta \mathrm{V}_{\mathrm{DRP}} \times \mathrm{RV}_{\mathrm{V}}(\mathrm{FB}) / \Delta \mathrm{V}_{\mathrm{OUT}}
$$

$$
=360 \mathrm{mV} \times 2.63 \mathrm{k} \Omega / 50 \mathrm{mV}=18.9 \mathrm{k} \Omega
$$

## ADDITIONAL APPLICATION DIAGRAMS



Figure 16. 5 V only to 1.2 V


Figure 17. 5 V to 1.2 V with 12 V Bias

## ADDITIONAL APPLICATION DIAGRAMS



Figure 18.5 V only to 2.5 V
PACKAGE THERMAL DATA

| Parameter |  | 28 Lead SO Wide | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 75 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5305

## Three-Phase Synchronous Switching Step-Down Controller with Single Wire Current Sharing

The CS5305 provides a low-cost, single-controller solution for the low-voltage, high-current power needs of next-generation workstation and server processors. This IC provides high accuracy and the industry's fastest transient response, reducing the need for large banks of output capacitors and providing the most compact, reliable, and economical power supply.

Since each phase's output voltage and current feed back to develop the PWM ramp signal (enhanced $\mathrm{V}^{2 \mathrm{TM}}$ control), the CS5305 shares output current accurately between phases. Accurate current sharing means that the power supply design does not need to use power components rated to handle mismatched current per phase. The enhanced $\mathrm{V}^{2}$ control compensates for variations in both line and load.

The IC's built-in single wire current sharing capability allows easy paralleling of multiple Voltage Regulator Modules (VRMs) based on the CS5305. The paralleled VRMs use a shared bus to provide high current and high reliability to multiple microprocessor workstations or servers.

The CS5305 meets VRM 9.x specifications with its Power Good, Enable, Differential Remote Sense, and single-wire Current Share features. The product fits server and workstation VRMs, and can be used to power Embedded Processors. The IC provides the simplest, lowest-cost solution for any low voltage, high current power supply.

## Features

- Enhanced $V^{2}$ Control Method
- VRM 9.x Compatible VID Codes
- Lossless Inductor Current Sensing
- Single Wire Active Current Sharing Between Converters
- Auto Master-Slave Current Share Control Method
- Programmable 200 to 800 kHz Switching Frequency
- Programmable Adaptive Voltage Positioning
- Differential Remote Sense
- Pulse-by-Pulse Current Limit
- Master Hiccup Overcurrent Protection through Single

Wire Share Bus

- 5-Bit DAC with $1 \%$ Tolerance
- ENABL Input
- VRM 9.x-Compliant Power Good Output
- Active Current Sharing During Soft Start



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PIN CONNECTIONS


## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5305GDW28 | SO-28L | 27 Units/Rail |
| CS5305GDWR28 | SO-28L | 1000 Tape \& Reel |

## APPLICATION DIAGRAMS



Figure 1. VRM 9.0, 60 A Converter


Figure 2. Two-Converter System with Sharing

MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Operating Junction Temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 |  |
| Thermal Resistance, Junction-to-Case, R ${ }_{\theta J C}$ | kV |  |
| Thermal Resistance, Junction-to-Ambient, R ${ }_{\theta J J A}$ | Reflow: (SMD styles only) Note 1. | 230 peak |
| JEDEC Moisture Sensitivity | ${ }^{\circ} \mathrm{C}$ |  |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Number | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\boldsymbol{I}_{\text {SOURCE }}$ | $\boldsymbol{I}_{\text {SiNK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | OCSET | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 2 | R $_{\text {OSC }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 3 | ENABL | 16 V | -0.3 V | 1.0 mA | 1.0 mA |
| $4-6$ | CS1-3 $^{2}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 7 | CS $_{\text {REF }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 8 | $\mathrm{I}_{\text {FB }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 9 | IOUT | 7.0 V | -0.3 V | 10 mA | 10 mA |
| 10 | SHARE | 16 V | -0.3 V | 50 mA | 1.0 mA |
| 11 | SCOMP | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 12 | $V_{\text {DRP }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 13 | $\mathrm{~V}_{\text {FB }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 14 | COMP | 7.0 V | -0.3 V | 10 mA | 1.0 mA |
| 15 | PWRGD | 16 V | -0.3 V | 1.0 mA | 20 mA |

MAXIMUM RATINGS (continued)

| Pin Number | Pin Symbol | $\mathbf{V}_{\text {MAX }}$ | $\mathbf{V}_{\text {MIN }}$ | $\mathbf{I}_{\text {SOURCE }}$ | $\mathbf{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $16-20$ | $\mathrm{~V}_{\text {ID4 }}-\mathrm{V}_{\text {IDO }}$ | 16 V | -0.3 V | 1.0 mA | 1.0 mA |
| 21 | PWRGDS | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 22 | SGND | 0.3 V | -0.3 V | 1.0 mA | 1.0 mA |
| 23 | $\mathrm{~V}_{\text {CC }}$ | 16 V | -0.3 V | $\mathrm{~N} / \mathrm{A}$ | $0.4 \mathrm{~A}, 1.0 \mu \mathrm{~s} 100 \mathrm{~mA} \mathrm{DC}$ |
| 24 | DRVON | 7.0 V | -0.3 V | 10 mA | 1.0 mA |
| $25-27$ | GATE $3-1$ | 16 V | -0.3 V | $0.1 \mathrm{~A}, 1.0 \mu \mathrm{~s} ; 25 \mathrm{~mA} \mathrm{DC}$ | $0.1 \mathrm{~A}, 1.0 \mu \mathrm{~s} 25 \mathrm{~mA} \mathrm{DC}$ |
| 28 | GND | $\mathrm{N} / \mathrm{A}$ | $\mathrm{N} / \mathrm{A}$ | $0.4 \mathrm{~A}, 1.0 \mu \mathrm{~s} ; 100 \mathrm{mADC}$ | $\mathrm{N} / \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\text {GATEX }}=100 \mathrm{pF}\right.$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SCOMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\text {ROSC }}=32.4 \mathrm{k} \Omega, \mathrm{R}_{\text {SHARE }}=60.4 \mathrm{k} \Omega, \mathrm{V}(\mathrm{OCSET})=0.54 \mathrm{~V}$, DAC Code 01110; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $0=$ Connected to GND, $1=$ Open (Pulled-up to internal 3.3 V ) or Pulled-up to external voltage $\leq 13 \mathrm{~V}$ )

| Accuracy (all codes) VID code - 125 mV |  |  |  |  | Connect VFB to COMP, SGND < 55 mV , <br> Measure COMP - SGND |  |  | $\pm 1.0$ | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {ID4 }}$ | VID3 | $V_{\text {ID2 }}$ | $V_{\text {ID1 }}$ | VIDO | $\mathrm{V}_{\text {ID }}$ Maximum Voltage |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | DRVON < 1.0 V, GATE ${ }_{\text {x }}<1.0 \mathrm{~V}$ |  | FAULT Mode |  | V |
| 1 | 1 | 1 | 1 | 0 | 1.100 | 0.965 | 0.975 | 0.985 | V |
| 1 | 1 | 1 | 0 | 1 | 1.125 | 0.990 | 1.000 | 1.010 | V |
| 1 | 1 | 1 | 0 | 0 | 1.150 | 1.015 | 1.025 | 1.035 | V |
| 1 | 1 | 0 | 1 | 1 | 1.175 | 1.040 | 1.050 | 1.061 | V |
| 1 | 1 | 0 | 1 | 0 | 1.200 | 1.064 | 1.075 | 1.086 | V |
| 1 | 1 | 0 | 0 | 1 | 1.225 | 1.089 | 1.100 | 1.111 | V |
| 1 | 1 | 0 | 0 | 0 | 1.250 | 1.114 | 1.125 | 1.136 | V |
| 1 | 0 | 1 | 1 | 1 | 1.275 | 1.139 | 1.150 | 1.162 | V |
| 1 | 0 | 1 | 1 | 0 | 1.300 | 1.163 | 1.175 | 1.187 | V |
| 1 | 0 | 1 | 0 | 1 | 1.325 | 1.188 | 1.200 | 1.212 | V |
| 1 | 0 | 1 | 0 | 0 | 1.350 | 1.213 | 1.225 | 1.237 | V |
| 1 | 0 | 0 | 1 | 1 | 1.375 | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 0 | 1 | 0 | 1.400 | 1.263 | 1.275 | 1.288 | V |
| 1 | 0 | 0 | 0 | 1 | 1.425 | 1.287 | 1.300 | 1.313 | V |
| 1 | 0 | 0 | 0 | 0 | 1.450 | 1.312 | 1.325 | 1.338 | V |
| 0 | 1 | 1 | 1 | 1 | 1.475 | 1.337 | 1.350 | 1.364 | V |
| 0 | 1 | 1 | 1 | 0 | 1.500 | 1.361 | 1.375 | 1.389 | V |
| 0 | 1 | 1 | 0 | 1 | 1.525 | 1.386 | 1.400 | 1.414 | V |
| 0 | 1 | 1 | 0 | 0 | 1.550 | 1.411 | 1.425 | 1.439 | V |
| 0 | 1 | 0 | 1 | 1 | 1.575 | 1.436 | 1.450 | 1.465 | V |
| 0 | 1 | 0 | 1 | 0 | 1.600 | 1.460 | 1.475 | 1.490 | V |
| 0 | 1 | 0 | 0 | 1 | 1.625 | 1.485 | 1.500 | 1.515 | V |
| 0 | 1 | 0 | 0 | 0 | 1.650 | 1.510 | 1.525 | 1.540 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$; $\mathrm{C}_{\text {GATEX }}=100 \mathrm{pF}$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SCOMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{R}_{\text {SHARE }}=60.4 \mathrm{k} \Omega, \mathrm{V}(\mathrm{OCSET})=0.54 \mathrm{~V}$, DAC Code 01110; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $\mathbf{0}=$ Connected to GND, $1=$ Open (Pulled-up to internal 3.3 V ) or Pulled-up to external voltage $\leq 13 \mathrm{~V}$ )

| 0 | 0 | 1 | 1 | 1 | 1.675 | 1.535 | 1.550 | 1.566 | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 | 0 | 1.700 | 1.560 | 1.575 | 1.591 | V |
| 0 | 0 | 1 | 0 | 1 | 1.725 | 1.584 | 1.600 | 1.616 | V |
| 0 | 0 | 1 | 0 | 0 | 1.750 | 1.609 | 1.625 | 1.641 | V |
| 0 | 0 | 0 | 1 | 1 | 1.775 | 1.634 | 1.650 | 1.667 | V |
| 0 | 0 | 0 | 1 | 0 | 1.800 | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 0 | 0 | 1 | 1.825 | 1.683 | 1.700 | 1.717 | V |
| 0 | 0 | 0 | 0 | 0 | 1.850 | 1.708 | 1.725 | 1.742 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID } 4}, \mathrm{~V}_{\text {ID }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID }}$ | 1.00 | 1.25 | 1.5 | V |
| Input Pull-up Resistance |  |  |  |  | $\begin{aligned} 0 & V^{<}<V_{I D 4}, V_{I D 3}, V_{I D 2}, V_{I D 1}, \\ V_{I D O} & <3.3 \mathrm{~V} \end{aligned}$ | 25 | 50 | 100 | k $\Omega$ |
| Pull-up Voltage |  |  |  |  | 1.0 M $\Omega$ to GND | 2.5 | 2.7 | 3.0 | V |
| SGND Bias Current |  |  |  |  | SGND < 55 mV , All DAC Codes | 10 | 20 | 40 | $\mu \mathrm{A}$ |

Power Good Output

| Upper Threshold |  |  |  |  | Force PWRGDS-SGND | 1.876 (-5\%) | 1.975 | 2.074 (+5\%) | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Lower Threshold |  |  |  |  | Force PWRGDS-SGND | $0.95$ | $0.975 \times$ | $V_{I D}-125 \mathrm{mV}$ | V |
| $V_{\text {ID4 }}$ | $V_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID } 2}$ | $\mathrm{V}_{\text {ID } 1}$ | VIDO |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 0 |  | 0.926 | 0.951 | 0.975 | V |
| 1 | 1 | 1 | 0 | 1 |  | 0.950 | 0.975 | 1.000 | V |
| 1 | 1 | 1 | 0 | 0 |  | 0.974 | 1.000 | 1.025 | V |
| 1 | 1 | 0 | 1 | 1 |  | 0.998 | 1.024 | 1.050 | V |
| 1 | 1 | 0 | 1 | 0 |  | 1.021 | 1.048 | 1.075 | V |
| 1 | 1 | 0 | 0 | 1 |  | 1.045 | 1.073 | 1.100 | V |
| 1 | 1 | 0 | 0 | 0 |  | 1.069 | 1.097 | 1.125 | V |
| 1 | 0 | 1 | 1 | 1 |  | 1.093 | 1.122 | 1.150 | V |
| 1 | 0 | 1 | 1 | 0 |  | 1.116 | 1.146 | 1.175 | V |
| 1 | 0 | 1 | 0 | 1 |  | 1.140 | 1.170 | 1.200 | V |
| 1 | 0 | 1 | 0 | 0 |  | 1.164 | 1.195 | 1.225 | V |
| 1 | 0 | 0 | 1 | 1 |  | 1.188 | 1.219 | 1.250 | V |
| 1 | 0 | 0 | 1 | 0 |  | 1.211 | 1.243 | 1.275 | V |
| 1 | 0 | 0 | 0 | 1 |  | 1.235 | 1.268 | 1.300 | V |
| 1 | 0 | 0 | 0 | 0 |  | 1.259 | 1.292 | 1.325 | V |
| 0 | 1 | 1 | 1 | 1 |  | 1.283 | 1.316 | 1.350 | V |
| 0 | 1 | 1 | 1 | 0 |  | 1.306 | 1.341 | 1.375 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$; $\mathrm{C}_{\text {GATEX }}=100 \mathrm{pF}$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SCOMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{R}_{\text {SHARE }}=60.4 \mathrm{k} \Omega$, $\mathrm{V}(\mathrm{OCSET})=0.54 \mathrm{~V}$, DAC Code 01110; unless otherwise stated.)

| Parameter |  |  |  |  | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 1 | 0 | 1 |  | 1.330 | 1.365 | 1.400 | V |
| 0 | 1 | 1 | 0 | 0 |  | 1.354 | 1.389 | 1.425 | V |
| 0 | 1 | 0 | 1 | 1 |  | 1.378 | 1.414 | 1.450 | V |
| 0 | 1 | 0 | 1 | 0 |  | 1.401 | 1.438 | 1.475 | V |
| 0 | 1 | 0 | 0 | 1 |  | 1.425 | 1.463 | 1.500 | V |
| 0 | 1 | 0 | 0 | 0 |  | 1.449 | 1.487 | 1.525 | V |
| 0 | 0 | 1 | 1 | 1 |  | 1.473 | 1.511 | 1.550 | V |
| 0 | 0 | 1 | 1 | 0 |  | 1.496 | 1.536 | 1.575 | V |
| 0 | 0 | 1 | 0 | 1 |  | 1.520 | 1.560 | 1.600 | V |
| 0 | 0 | 1 | 0 | 0 |  | 1.544 | 1.584 | 1.625 | V |
| 0 | 0 | 0 | 1 | 1 |  | 1.568 | 1.609 | 1.650 | V |
| 0 | 0 | 0 | 1 | 0 |  | 1.591 | 1.633 | 1.675 | V |
| 0 | 0 | 0 | 0 | 1 |  | 1.615 | 1.658 | 1.700 | V |
| 0 | 0 | 0 | 0 | 0 |  | 1.639 | 1.682 | 1.725 | V |
| Switch Leakage Current |  |  |  |  | $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}$, PWRGDS $=1.4 \mathrm{~V}$ | - | - | 1.0 | $\mu \mathrm{A}$ |
| Delay |  |  |  |  | PWRGDS low to PWRGD low | 50 | 250 | 600 | $\mu \mathrm{s}$ |
| Output Low Voltage |  |  |  |  | $\begin{aligned} & \text { PWRGDS }=1.0 \mathrm{~V}, \\ & \mathrm{I}_{\text {PWRGOOD }}=4.0 \mathrm{~mA} \end{aligned}$ | - | 0.15 | 0.4 | V |

Voltage Feedback Error Amplifier

| $V_{\text {FB }}$ Bias Current | Note 2. | 9.5 | 10.3 | 11.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Comp Source Current | $\begin{gathered} \mathrm{COMP}=0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V}, \\ \mathrm{~V}_{\mathrm{FB}}=1.6 \mathrm{~V} \end{gathered}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Comp Sink Current | $\begin{gathered} \mathrm{COMP}=0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V}, \\ \mathrm{~V}_{\mathrm{FB}}=1.0 \mathrm{~V} \end{gathered}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$, Note 3. | - | 32.0 | - | mmho |
| Output Impedance | Note 3. | - | 2.5 | - | $\mathrm{m} \Omega$ |
| Open Loop DC Gain | Note 3. | 60 | 95 | - | dB |
| Unity Gain Bandwidth | COMP $=0.01 \mu \mathrm{~F}$, Note 3. | - | 50 | - | kHZ |
| PSRR @ 1.0 kHz | Note 3. | - | 70 | - | dB |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.6 \mathrm{~V}$ | - | 0.1 | 0.2 | V |
| COMP Discharge Threshold | - | 0.15 | 0.2 | 0.25 | V |
| Hiccup Latch Discharge Current | $\begin{gathered} C S x-\text { CS }_{\text {REF }}=.05 \mathrm{~V}, \\ O C S E T=0.1 \mathrm{~V}, \\ C O M P=0.5 \mathrm{~V} \end{gathered}$ | 2.0 | 5.0 | 10 | $\mu \mathrm{A}$ |
| Hiccup Charge / Discharge Ratio | - | 4.5 | 6.0 | 7.5 | - |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of ROSC per Figure 5.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATEX}}=100 \mathrm{pF}$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SCOMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{R}_{\text {SHARE }}=60.4 \mathrm{k} \Omega$, $\mathrm{V}(\mathrm{OCSET})=0.54 \mathrm{~V}$, DAC Code 01110; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | | Voltage Feedback Error Amplifier | 0.3 | 2.5 | 5.0 | mA |
| :---: | :---: | :---: | :---: | :---: |
| SHARE Fault Discharge Current | SHARE $=3.5 \mathrm{~V}$, <br> COMP $=0.5 \mathrm{~V}$, <br> CSx $=$ CS <br> OCF $=0 \mathrm{~V}$, |  |  |  |

Enable Input

| Threshold Voltage | Monitor DRVON | 1.12 | 1.25 | 1.38 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Pull-up Voltage | $1 \mathrm{M} \Omega$ to GND | 2.5 | 2.7 | 3.0 | V |
| Input Pull-up Resistance | - | 25 | 50 | 100 | $\mathrm{k} \Omega$ |

## PWM Comparators

| Minimum Pulse Width | Measured from CSx to GATEx, $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{CS} S_{\mathrm{REF}}=0.5 \mathrm{~V}, \\ & \mathrm{COMP}=0.5 \mathrm{~V}, \end{aligned}$ $60 \mathrm{mV} \text { step on CSx; }$ $\text { measure at GATEx }=1.0 \mathrm{~V}$ | - | 75 | 220 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Transient Response Time | Measured from $\mathrm{CS}_{\text {REF }}$ to GATEx, $\begin{aligned} & \mathrm{COMP}=2.1 \mathrm{~V}, \\ & \mathrm{CSX}=\mathrm{CS} \text { REF }=0.5 \mathrm{~V}, \end{aligned}$ <br> CS ReF stepped from $1.2 \mathrm{~V}-2.0 \mathrm{~V}$ | - | 100 | 150 | ns |
| Channel Start-up Offset | $\mathrm{CSx}=\mathrm{CS}_{\mathrm{REF}}=\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$, measure V (COMP) when GATEx switch high | 0.34 | 0.6 | 0.75 | V |
| Channel Start-up Offset Mismatch | $C S x=C S_{\text {REF }}=V_{F B}=0 \mathrm{~V},$ measure V (COMP) when GATEx switch high, Note 4. | -5.0 | - | 5.0 | mV |

## Gates

| High Voltage | $\mathrm{I}_{\text {GATEx }}=1.0 \mathrm{~mA}$ | 2.25 | 2.5 | 3.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Low Voltage | $\mathrm{I}_{\text {GATEx }}=1.0 \mathrm{~mA}$ | - | 0.2 | 0.4 | V |
| Rise Time GATE | $0.8 \mathrm{~V}<\mathrm{GATE}<2.0 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | - | 15 | 30 | ns |
| Fall Time GATE | $2.0 \mathrm{~V}>\mathrm{GATE}>0.8 \mathrm{~V}$, <br> $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | - | 15 | 30 | ns |

## Oscillator

| Switching Frequency | $\mathrm{R}_{\text {OSC }}=32.4 \mathrm{k} \Omega$ | 300 | 400 | 500 | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Switching Frequency | ROSC $=63.4 \mathrm{k} \Omega$, Note 4. | 150 | 200 | 250 | kHz |
| Switching Frequency | ROSC $=16.2 \mathrm{k} \Omega$, Note 4. | 600 | 800 | 1000 | kHz |
| Rosc Voltage | Note 4. | 0.90 | 1.00 | 1.10 | V |
| Phase Delay | - | 90 | 120 | 150 | deg |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATEX}}=100 \mathrm{pF}$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SCOMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{R}_{\text {SHARE }}=60.4 \mathrm{k} \Omega$, $\mathrm{V}(\mathrm{OCSET})=0.54 \mathrm{~V}$, DAC Code 01110; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Sense Amplifiers |  |  |  |  |  |
| CS ${ }_{\text {REF }}$ Input Bias Current | CS ${ }_{\text {REF }}=\mathrm{CSx}=0 \mathrm{~V}$ | - | 0.3 | 3.0 | $\mu \mathrm{A}$ |
| CSx Input Bias Current | CS REF $=\mathrm{CSx}=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Sense Amp Gain | $\mathrm{CS}_{\text {REF }}=0 \mathrm{~V}, \mathrm{CSX}=0.05 \mathrm{~V}$, Measure V(COMP) when GATEx switches high | . 95 | 1.06 | 1.17 | V / V |
| Mismatch | $\begin{aligned} & 0 \leq\left(\text { CSx }- \text { CS }_{\text {REF }}\right) \leq 50 \mathrm{mV}, \\ & \text { Note } 5 . \end{aligned}$ | -3.0 | - | 3.0 | mV |
| Common Mode Input Range | Note 5. | 0 | - | 2.0 | V |
| Bandwidth | Note 5. | - | 7.0 | - | MHz |
| Single Phase Pulse by Pulse Current Limit | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{CS}_{\mathrm{REF}}=0.5 \mathrm{~V}, \\ & \mathrm{COMP}=2.0 \mathrm{~V}, \text { Measure } \\ & \mathrm{CSx}-\mathrm{CS}_{\text {REF }} \text { when GATEx } \\ & \text { goes low } \end{aligned}$ | 80 | 90 | 100 | mV |
| OCSET Input Bias Current | OCSET $=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Current Sense Input to OCSET Gain | $\begin{aligned} & \text { OCSET / R (CSx } \left.- \text { CS }_{\text {REF }}\right) \text {, } \\ & \text { OCSET }=0.6 \mathrm{~V}, \\ & \text { Monitor DRVON }<1.0 \mathrm{~V} \end{aligned}$ | 3.4 | 3.7 | 4.0 | $\mathrm{V} / \mathrm{V}$ |
| Current Limit Filter Slew Rate | $\begin{aligned} & \mathrm{CS}_{\text {REF }}=1.1 \mathrm{~V}, \mathrm{CSx}=1.0 \mathrm{~V}, \\ & \text { pulse CSx to } 1.16 \mathrm{~V}, \text { Note } 5 . \end{aligned}$ | 2.0 | 5.0 | 13 | $\mathrm{mV} / \mu \mathrm{s}$ |

Adaptive Voltage Positioning

| $V_{\text {DRP }}$ Output Voltage to DACout Offset | $\begin{gathered} \mathrm{CSx}=\mathrm{CS}_{\mathrm{REF}}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \\ \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{gathered}$ | -30 | 2.0 | 60 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum $\mathrm{V}_{\text {DRP }}$ Voltage | $\begin{aligned} & \mathrm{CSx}-\mathrm{CS}_{\mathrm{REF}}=50 \mathrm{mV} \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | 500 | 560 | 620 | mV |
| Current Sense Amp to V ${ }_{\text {DRP }}$ Gain | $\begin{aligned} & \mathrm{CSx}-\mathrm{CS}_{\mathrm{REF}}=50 \mathrm{mV} \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | 3.4 | 3.7 | 4.0 | V / V |
| V ${ }_{\text {DRP }}$ Source Current | $\begin{gathered} \mathrm{CSx}-\mathrm{CS}_{\mathrm{REF}}=50 \mathrm{mV}, \\ \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \\ \mathrm{~V}_{\mathrm{DRP}}=1.5 \mathrm{~V} \end{gathered}$ | 1.0 | 7.0 | 14 | mA |

SHARE Current Sense Amplifier

| $\mathrm{I}_{\mathrm{FB}}$ Input Bias Current | $\mathrm{I}_{\mathrm{FB}}=0 \mathrm{~V}$ | - | 0.2 | 1.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Offset Voltage | Note 5. | -5.0 | 0 | 5.0 | mV |
| Common Mode Input Range | Note 5. | 0 | - | 2.0 | V |
| Output Current | IOUT $=0 \mathrm{~V}, \mathrm{CSx}=0.667 \mathrm{~V}$, <br> CS <br> REF $=0.5 \mathrm{~V}$ | 1.0 | 10 | 22 | mA |
| Gain | Note 5. | - | 120 | - | dB |
| Output Unity Gain BW | Note 5. | - | 5.0 | - | MHz |

5. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATEX}}=100 \mathrm{pF}\right.$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SCOMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\text {ROSC }}=32.4 \mathrm{k} \Omega, \mathrm{R}_{\text {SHARE }}=60.4 \mathrm{k} \Omega, \mathrm{V}($ OCSET $)=0.54 \mathrm{~V}$, DAC Code 01110; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

SHARE Bus

| SHARE Amplifier Offset Voltage | $\begin{aligned} & \text { Measure V(SHARE) - V(Iout), } \\ & 0<\text { lout }_{\text {< }} \text { 2.0 V } \end{aligned}$ | 20 | 40 | 60 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SHARE Amplifier Source Current | $\mathrm{l}_{\text {OUT }}=2.1 \mathrm{~V}$, SHARE $=2.0 \mathrm{~V}$ | 1.0 | 7.5 | 24 | mA |
| SHARE Amplifier Max Voltage | $\mathrm{I}_{\text {OUT }}=3.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 2.65 | 2.80 | 3.20 | V |
| SHARE Fault Threshold | DRVON $<1.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 3.2 | 3.4 | 3.7 | V |
| SHARE OK Threshold | DRVON $>1.0 \mathrm{~V}$ | 2.0 | 2.3 | 2.5 | V |
| SHARE Fault Hysteresis | - | 1.0 | 1.15 | 1.3 | V |
| SHARE Fault Output Voltage | - | 3.8 | 4.25 | 4.7 | V |
| SHARE Fault Output Current | SHARE $=3.8 \mathrm{~V}$ | 1.2 | 2.0 | 2.5 | mA |
| SHARE Full Load Accuracy | $\begin{aligned} & \mathrm{CS}_{\text {REF }}=0.5 \mathrm{~V}, \mathrm{CSX}=0.52 \mathrm{~V}, \\ & \text { lout } / \mathrm{FB} \text { Divider }=22 \mathrm{k} \Omega / 3.0 \mathrm{k} \Omega \end{aligned}$ | 1.7 | 1.95 | 2.2 | V |
| SHARE Short Circuit Current | $\mathrm{V}\left(\mathrm{l}_{\text {OUT }}\right)=2.0 \mathrm{~V}$, SHARE $=$ GND | 1.0 | 17 | 28 | mA |
| SHARE Fault Short Circuit Current | $\mathrm{CS}_{\text {REF }}=0.5 \mathrm{~V}, \mathrm{CSx}=0.6 \mathrm{~V}$ | 2.0 | 19 | 30 | mA |

Current SHARE Adjust Amplifier

| Transconductance from lout to SCOMP | $\begin{aligned} & 0<\text { louT }<2.0 \mathrm{~V}, \\ & 0<\text { SCOMP }<2.0 \mathrm{~V} \end{aligned}$ | 23 | 40 | 53 | $\mu \mathrm{A} / \mathrm{V}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gain from lout to COMP | Note 6. | 30 | 50 | 140 | mA / V |
| Maximum SCOMP source current | SCOMP $=1.5 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Maximum SCOMP sink current | SCOMP $=1.5 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Unity Gain BW | $C(S C O M P)=$ TBD, Note 6. | 30 | 56 | 100 | Hz |

MOSFET Driver Enable

| Pull-Up Voltage | DRVON Floating | 4.5 | 5.5 | 6.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| DRVON Source Current | DRVON $=1.5 \mathrm{~V}$ | .5 | 3.0 | 6.5 | mA |
| DRVON Pull Down Resistor | DRVON $=1.5 \mathrm{~V}, \mathrm{ENABL}=0 \mathrm{~V}$, <br> $\mathrm{R}=1.5 \mathrm{~V} / \mathrm{l}(1.5 \mathrm{~V})$ | 35 | 70 | 140 | $\mathrm{k} \Omega$ |

General Electrical Specifications

| $V_{\text {CC }}$ Disable Current | ENABLE $=0$ V (no switching) | - | 30 | 60 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| UVLO Start Threshold | COMP charging, DRVON $>1.0 \mathrm{~V}$ | 8.5 | 9.0 | 9.5 | V |
| UVLO Stop Threshold | Gates not switching, COMP <br> discharging, DRVON $<1.0 ~ V$ | 7.5 | 8.0 | 8.5 | V |
| UVLO Hysteresis | Start - Stop | 0.8 | 1.0 | 1.2 | V |
| $V_{\text {CC }}$ Operating Current | ENABLE Open | - | 22 | 30 | mA |

6. Guaranteed by design. Not tested in production.

## PACKAGE PIN DESCRIPTION

| Package Pin Number |  |  |  |
| :---: | :---: | :---: | :---: |
| SO-28L | Pin Symbol | Pin Name | Function |
| 1 | OCSET | Over-Current Set | Resistor divider from R RSC to GND programs the threshold of the hiccup over-current protection. |
| 2 | Rosc | Oscillator Frequency Adjust | Resistance to GND programs the oscillator frequency. It also programs the $\mathrm{V}_{\mathrm{FB}}$ bias current shown in Figure 5. |
| 3 | ENABL | Enable Input | TTL-Compatible logic input with $50 \mathrm{k} \Omega$ internal pull-up resistor to 3.3 V . A logic low puts the IC in FAULT mode. |
| 4-6 | CS1-3 | Current Sense Inputs | Non-inverting inputs to the current sense amplifiers. |
| 7 | $\mathrm{CS}_{\text {REF }}$ | Current Sense Reference | Inverting input to the current sense amplifiers, and fast feedback input to the PWM comparator. |
| 8 | $\mathrm{I}_{\text {FB }}$ | Share Current Amp Inverting Input | Inverting input to share current amp. Connect resistor divider between $\mathrm{I}_{\mathrm{OUT}}, \mathrm{I}_{\mathrm{FB}}$, and IC GND pin 28 to program Share Current Amp gain. |
| 9 | IOUT | Share Current Amp Output | Share current amplifier output and input to share adjust amplifier. |
| 10 | SHARE | Share Bus | Connect with other modules for single-wire current sharing. |
| 11 | SCOMP | Share Compensation | Connect compensation network to stabilize share loop. |
| 12 | $\mathrm{V}_{\text {DRP }}$ | Current Sense Output for AVP | The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to program the AVP voltage or leave this pin open for no AVP. |
| 13 | $V_{\text {FB }}$ | Voltage Feedback | Error Amp inverting input. Input bias current used to program AVP light load offset via resistor connected to converter output voltage. Short $\mathrm{V}_{\mathrm{FB}}$ to the converter output voltage for no AVP. |
| 14 | COMP | Error Amp Output and PWM Comparator Input | Provides loop compensation. Also used to control Softstart and Fault timing. |
| 15 | PWRGD | Power Good Output | Open collector output goes low when $\mathrm{V}_{\mathrm{FB}}$ is out of regulation. User must externally limit current into this pin to less than 20 mA . |
| 16-20 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID }}$ | Voltage ID DAC Inputs | Programs Output Voltage. $50 \mathrm{k} \Omega$ internal pull-up resistors to 3.3 V . |
| 21 | PWRGDS | Power Good Sense | Provides remote output voltage sensing. |
| 22 | SGND | Reference Ground | Ground connection for the DAC. Provides remote sensing of ground at the load. |
| 23 | $\mathrm{V}_{\mathrm{Cc}}$ | Supply Input | IC Power Supply Input. |
| 24 | DRVON | Driver Enable | Logic High enables outputs of compatible MOSFET Driver ICs. Low turns all MOSFETs OFF. Pin driven from internal $5.5 \mathrm{~V} ; 70 \mathrm{k} \Omega$ internal resistor to GND. |
| 25-27 | GATE 3-1 | FET Driver Outputs | PWM Signal Input to external MOSFET Gate Driver ICs. |
| 28 | GND | Ground | IC Power Supply Return; connected to IC substrate. |



CS5305

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 4. Oscillator Frequency


Figure 6. Icc vs. Temperature


Figure 8. Oscillator Frequency vs. Temperature for $\mathrm{R}_{\mathrm{OSC}}=32.4 \mathrm{k} \Omega$


Figure 5. V FB Bias Current vs. Rosc Value


Figure 7. UVLO Start and Stop Thresholds vs. Temperature


Figure 9. DAC Output for VID = 01111 (1.475 V)

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 10. DAC Output for VID = 00110 (1.700 V)


Figure 11. GATE Phase Delay vs. Temperature


Figure 12. GATE Rise and Fall Time vs. Temperature


Figure 13. PWM Comparator Minimum Pulse Width vs. Temperature


Figure 14. PWM Transient Response Time vs. Temperature


Figure 15. Current Sense Amp Channel Start-Up Offset Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 16. Current Sense Amplifier Gain vs. Temperature


Figure 18. V ${ }_{\text {DRP }}$ Source Current vs. Temperature


Figure 17. $\mathrm{V}_{\mathrm{FB}}$ Bias Current vs. Temperature for $R_{\text {OSC }}=32.4 \mathrm{k} \Omega$


Figure 19. V ${ }_{\text {DRP }}$ to DAC Output Offset Voltage vs. Temperature


Figure 20. SHARE Bus Voltages vs. Temperature


Figure 21. IOUT Output Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 22. SHARE Offset Voltage vs. Temperature


Figure 24. Power Good Lower Threshold Voltage vs. Temperature


Figure 23. I IOUT to $\mathrm{S}_{\text {COMP }}$ Transconductance vs. Temperature


Figure 25. Power Good Upper Threshold Voltage vs. Temperature


Figure 26. Power Good Delay vs. Temperature

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## Fixed Frequency Multi-phase Control

Multi-phase CPU controllers include the necessary control circuitry to implement several buck converters in parallel. These converters are configured to turn on at different times. This allows much higher output current than could be provided by a single converter. The apparent ripple frequency is increased and so output current can ramp up or down faster than a single converter with the same value of output inductor. Heat is also spread among multiple components.

The CS5305 uses a fixed frequency, Enhanced V ${ }^{2}$ architecture. Each phase is delayed by approximately $120^{\circ}$ from the previous phase. The GATE output for each channel changes to a logic high at the beginning of its oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator, at which time the GATE output changes to a logic low. Once low, the GATE output remains low until the next oscillator cycle begins, and the control loop will not respond until that time. The Enhanced $V^{2}$ control loop will respond to line and load transients while the GATE output is high. Enhanced V ${ }^{2}$ control will respond within the off time of the converter.


Figure 27.
The Enhanced $\mathrm{V}^{2}$ architecture measures and adjusts current in each phase. An additional input (CSx pin) provides current information for each output phase to the control loop as shown in Figure 27. Inductor current is measured across capacitor Ccsx. The voltage across this capacitor is equal to the product of the output current and the inductor ESR if these components are chosen such that $(\operatorname{Ccsx})(\operatorname{Rcsx})=(\mathrm{L}) / \mathrm{ESR}_{\mathrm{L}}$. This signal is buffered by the current sense amplifier (unity gain in the CS5305) and summed with an offset voltage before it is presented as input to non-inverting input of the PWM comparator. Inductor current provides the PWM ramp. As inductor current
increases, the voltage at the positive input to the PWM comparator rises and terminates the PWM cycle. If the inductor starts the next cycle with higher current, the PWM cycle terminates earlier, thus providing negative feedback. A CSx input is provided for each channel, but the $\mathrm{CS}_{\text {REF }}$, $\mathrm{V}_{\mathrm{FB}}$ and COMP inputs are common to all phases. Current sharing between phases is accomplished by referencing all phases to the same error amplifier. Any phase with a larger current signal will turn off earlier than the channels with a lower current signal.
Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. In the absence of any load current, the COMP pin voltage will be equal to the sum of the output voltage, the offset voltage and half of the steady-state ramp voltage. (At no load, the output ripple current's positive and negative contributions are equal, and the DC averaged voltage is equal to half the ripple voltage.) If the COMP pin is held steady and the inductor current is forced to change, the output voltage will also change. In a closed-loop situation, changing the inductor current will force the COMP voltage to change so the output voltage can remain the same. The change in COMP voltage depends on the scaling of the current feedback signal, and can be defined as:

## $\Delta \mathrm{V}_{\mathrm{COMP}}=(\mathrm{ESRL})($ Current Sense Gain $)(\Delta \mathrm{I}$ PHASE $)$

Since the current sense gain for this loop is unity, this equation reduces to:

$$
\Delta \mathrm{V}_{\mathrm{COMP}}=\left(\mathrm{ESR}_{\mathrm{L}}\right)(\Delta \mathrm{IPHASE})
$$

and so the single-phase power stage output impedance is:

$$
\Delta \mathrm{V}_{\mathrm{COMP}} / \Delta \mathrm{IPHASE}=\mathrm{ESR} \mathrm{~L}
$$

The CS5305 has three phases, so the total power stage output impedance is then $\mathrm{ESR}_{\mathrm{L}} / 3$.

## Lossless Inductive Current Sensing

Current can be sensed across the inductor as shown in Figure 27. The output inductor is designated L and the inductor's equivalent series resistance is designated $\mathrm{ESR}_{\mathrm{L}}$. In the ideal case, the values of Rcsx and Ccsx are chosen such that $\left(\mathrm{L} / \mathrm{ESR}_{\mathrm{L}}\right)=(\operatorname{Rcsx})(\mathrm{Ccsx})$. If this criterion is met, the current sense signal will have the same shape as the inductor current, and the circuit can be analyzed as if a sense resistor with value equal to $\mathrm{ESR}_{\mathrm{L}}$ was placed in series with the inductor. However, these components also determine the ramp signal that is used to prevent pulse skipping and duty cycle jitter. Choosing (Rcsx)(Ccsx) < (L/ESR ${ }_{L}$ ) will result in the AC portion of the current sense signal being scaled more than the DC portion. This results in a larger ramp signal, but the current signal will overshoot during transients. This will affect transient response, adaptive voltage positioning and current limit. The COMP pin voltage will overshoot along with the current signal in order to maintain the output voltage. The COMP voltage will
eventually find the correct level for regulation, but the error will decay with the time constant $(\operatorname{Rcsx})(\mathrm{Ccsx})$. The $\mathrm{V}_{\mathrm{DRP}}$ voltage will also overshoot and response will be slowed, since the current signal is a component of that voltage. The single phase current limit will trip earlier since the current signal appears larger than it should be, and the module current limit will have a lower threshold for fast transients than it will for slow transients. Additional external components in the droop circuit and in the error amp compensation will correct this condition. Details are provided in the data sheet section on choosing external components.

## Adaptive Voltage Positioning

Adaptive voltage positioning is a technique used to reduce peak-to-peak output deviations during output current transients. The output voltage is set higher than nominal at light loads to reduce output voltage sag when load current is suddenly increased. Similarly, output voltage is set lower than nominal at heavy loads to reduce overshoot when load current suddenly decreases. The CS5305 implements adaptive voltage positioning by placing a resistor divider between $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\text {OUT }}$. The center tap of the divider connects to $\mathrm{V}_{\mathrm{FB}}$. These resistors, along with two or three other external components, implement a lossless droop voltage function.

Past implementations of adaptive voltage positioning used a droop resistor. This resistor was placed in series between the regulation point of the output voltage and the load. Increasing the current to the load caused the voltage at the load to droop below the regulation point. The amount of droop was equal to the change in current multiplied by the droop resistor value. This method was acceptable for low values of output current, where the droop resistor provided a minimal change in voltage without dissipating a great deal of power. Higher output current levels and tighter droop voltage requirements in today's microprocessors have rendered this droop resistor technique unusable. The lossless technique solves these problems.

The AVP function addresses DC and slow transient output voltage positioning. Response during the first few hundreds of nanoseconds of a transient are addressed primarily by the power stage output impedance, and the ESR and ESL of the output filter. The ramp size and the error amplifier compensation control the transition between these two regions. If ramp size is too large or the error amp is too slow, there will be a long transition to the final voltage after a transient. This will be most apparent if the output capacitance is low.

Figure 28 shows how adaptive positioning works. The waveform labeled "normal" shows output voltage for a converter without adaptive voltage positioning. The voltage sags when current steps up, returns to its nominal value and then overshoots when the current load is decreased. Using a slow adaptive positioning circuit can actually worsen performance. The slow adaptive positioning waveform above shows the output voltage sag, but the voltage recovers to its initial value before the adaptive positioning circuit
becomes active. When the load decreases, the overshoot causes the output voltage to exceed the upper limit. The fast adaptive positioning waveform shows how AVP can reduce transient voltage requirements by about one half compared to a "normal" converter.


Figure 28. Adaptive Positioning

## Current Limit

The CS5305 features two separate current limit circuits. First, the per-phase current limit terminates topside switch conduction in a phase if the voltage between any CSx pin and $\mathrm{CS}_{\text {REF }}$ exceeds a typical value of 90 mV . This provides fast peak current protection for individual phases. In addition, the output current signals for all three phases are summed and filtered to provide an average module current signal. This signal is compared to a voltage that is user-programmable. If this voltage is exceeded, the fault latch is set and the COMP capacitor is discharged by a $5 \mu \mathrm{~A}$ current sink until the COMP voltage falls below 0.2 V . The soft-start cycle begins when this threshold is reached, and the converter will operate in hiccup-mode until the overcurrent condition is cleared.

## Error Amplifier

The CS5305 uses the Enhanced $\mathrm{V}^{2}$ control method to offer the fastest and most accurate regulation available. One of the features of this control method is ease of error amplifier compensation. A single capacitor placed from the COMP pin to ground is sufficient to adequately stabilize the error amplifier.


Figure 29. Error Amplifier Frequency Response with No Compensation


Figure 30. Error Amplifier Frequency Response with $0.1 \mu \mathrm{~F}$ Capacitor

## Soft Start/Hiccup Mode

At initial power-up, the COMP voltage is zero. The total COMP capacitance will begin to charge with a typical current of $30 \mu \mathrm{~A}$. (There may be more than one capacitor connected between COMP and ground depending on the adaptive voltage positioning compensation.) All GATE outputs are held low until the COMP voltage reaches 0.6 V . Once this threshold is reached, the GATE outputs are released to operate normally. In hiccup-mode, this will result in GATE pulses being generated until the module overcurrent condition reoccurs, and the discharge/Soft Start cycle begins anew.

## Undervoltage Lockout

The CS5305 includes an under-voltage lockout circuit. This circuit disables the output drivers until $\mathrm{V}_{\mathrm{CC}}$ applied to the IC reaches a typical value of 9 V . The GATE outputs are disabled when $\mathrm{V}_{\mathrm{CC}}$ drops below 8 V typical.

## Enable

The CS5305 has a dedicated enable pin, in accordance with the latest VRM specifications. This pin is internally pulled up to a 3.3 V rail through a blocking diode and a $50 \mathrm{k} \Omega$ resistor. The blocking diode allows external pull up to a bias voltage greater than 3.3 V but below 13 V .

## Fault Protection Logic

The CS5305 is equipped with sophisticated fault-detection and protection circuitry to ensure proper operation in a paralleled VRM environment. In such an environment, any one of several distinct failures could not only destroy the VRM that sees the fault, but also those VRMs that are connected in parallel with the faulted VRM.
Table 1 describes the fault logic circuitry, shown below in Figure 31.


Figure 31. Fault Logic Circuitry

Table 1. Description of Fault Logic

| Fault Modes | Stop Switching | DRVON Level | PWRGD <br> Level | SHARE | Controller Off | COMP Pin Characteristics | Reset Method |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Under Voltage Lockout | yes | low | low via Power Good window comparator | n/a | no | $-5.0 \mu \mathrm{~A}$ | Comp < 0.2 V |
| VID $=11111$ | yes | low | low via Power Good window comparator | n/a | no | $-5.0 \mu \mathrm{~A}$ | Comp < 0.2 V |
| Enable Low | yes | Iow | low | n/a | no | $-5.0 \mu \mathrm{~A}$ | Comp<0.2 V |
| Module Over Current (set by OCSET) | yes | low | Iow via Power Good window comparator | > 3.8 V | no | $-5.0 \mu \mathrm{~A}$ | Comp < 0.2 V |
| Phase Over Current (0.33 V limit) | terminate pulse | high | n/a | n/a | no | not affected | not affected |
| External Share Fault (SHARE > 3.8 V ) | yes | low | Iow via Power Good window comparator | $\mathrm{n} / \mathrm{a}$ | no | -2.5 mA | remove external 3.8 V from SHARE |
| PWRGDS out of window range | no | high | low | n/a | no | not affected | not affected |

## Gate Outputs

The CS5305 is designed to operate with external gate drivers. Accordingly, the gate outputs are capable of driving a 100 pF load with typical rise and fall time of 15 ns .

## DRVON

When the CS5305 is used with DRVON-compatible gate drivers, the ability of the system to survive a fault in a paralleled environment is greatly increased. The DRVON signal tells the gate drivers to shut off both FETs while entering a fault condition. This action takes the faulted VRM "out of the picture," allowing the system to operate until the bad module can be replaced.

## Digital to Analog Converter (DAC)

The output voltage of the CS5305 module is set by means of a $5-\mathrm{bit}, 1 \% \mathrm{DAC}$. The DAC pins are internally pulled up to a 3.3 V rail through a blocking diode and a set of $50 \mathrm{k} \Omega$ resistors. The blocking diode allows external pull up to a bias voltage greater than 3.3 V and less than 13 V .

The output of the DAC is described in the Electrical Characteristics section of the datasheet. These outputs are consistent with the latest VRM specifications. The DAC produces an output voltage 125 mV lower than the VID code would indicate in order to produce an accurate PWRGD output. The relationship between the VID code and the DAC code is described by Figure 32 shown below. The shaded area shows the acceptable range of output voltages.

In order to produce a workable VRM using the CS5305, the designer is expected to use AVP as described earlier to position the output voltage above the DAC output, resulting in an output voltage somewhere in the middle of the acceptable range.


Figure 32. VRM 9.0 Output Voltage Accuracy Requirements

The latest VRM specifications require a module to turn its output off in the event of a 11111 VID code. When the DAC
sees such a code, the GATE pins stop switching and go low. The DRVON signal also goes low, which turns off all FETs on the module if the FET driver has an enable input. This condition is described in Table 1.

## PWRGD

According to the latest VRM specifications, the PWRGD signal is to be asserted when the output voltage is within a window defined by the VID code, as shown in Figure 33.


Figure 33. PWRGD Assertion Window
In addition, certain fault modes must cause PWRGD to go low to signal the system board that a VRM fault has occurred. In that sense, the PWRGD signal operates as a "VRM BAD" signal. These fault modes, as shown in Table 1 above, are ENABL low and CSx out of window.

When the ENABL pin is pulled low, PWRGD is pulled low to indicate that the VRM is off. DRVON is pulled low to turn both FETs off if the FET driver has an enable input.
The logic circuitry inside the chip sets PWRGD low only after a delay period has been passed. A "power bad" event does not cause PWRGD to go low unless it is sustained through the delay time, typically $200 \mu \mathrm{~s}$. If the anomaly disappears before the end of the delay, the PWRGD output will never be set low.
In order to use the PWRGD pin as specified, the user is advised to connect external resistors as necessary to limit the current into this pin to 4 mA or less.

## Share Bus

VRM 9.x specifications require that a single-wire share bus be provided from each module. This bus allows output current information to be communicated between modules such that the total load current is shared equally by each module. The CS5305 employs a proprietary share algorithm called direct duty cycle control. A block diagram is provided in Figure 34.


Figure 34.

Direct duty cycle control utilizes a master-slave approach to current sharing. At any given current load, one module will have a higher share bus voltage than the other modules. This module acts as the master. It conveys output current information to the other modules via the share bus. This information is buffered and provided to the PWM comparators, thus directly controlling duty cycle for the slave modules.

The share current sense amplifier allows the user to customize the share bus transconductance. Current sense information is provided to the non-inverting input from the $3.7 \times$ current sense amplifier from each phase. This provides a representation of the total module current. An external resistor divider between IOUT and ground, center-tapped at $\mathrm{I}_{\mathrm{FB}}$ programs the share bus voltage for a particular current level.

The share bus amplifier serves as a buffer and places the IOUT voltage on the SHARE pin. Note there is a diode in the schematic between the share bus amplifier and the SHARE pin. This is an "ideal" diode, and indicates that the share bus amplifier does not have current sink capability. This allows the share bus to be driven by the module with the highest share bus voltage. A 30 mV offset voltage provides noise immunity to ensure that any given module does not cycle between master and slave in a random fashion. It also guarantees that the master module is not driving duty cycle from the share bus. For the master module, the IOUT and SHARE voltages will be equal. In this case, the 30 mV offset holds the share adjust amplifier inactive, and the PWM channel is controlled in the normal manner. The offset voltage results in a current error between the master and slave modules, but this error is small compared to the current share tolerance found in the VRM 9.x specifications.

The share adjust amplifier takes the share bus voltage and directly drives the PWM comparators of all slave modules as previously described. The SCOMP pin provides a connection point for a compensation capacitor for the share adjust amplifier.

## CHOOSING EXTERNAL COMPONENTS FOR THE CS5305

## $R_{\text {OCSET }}$ and $R_{\text {OSC }}$

The $\mathrm{R}_{\text {OSC }}$ lead of the CS5305 provides a fixed 1 V reference to the user. A resistive divider is connected from $\mathrm{R}_{\mathrm{OSC}}$ to ground as shown in Figure 35. The center tap of the divider is connected to the OCSET lead. The total resistance from the $\mathrm{R}_{\text {OSC }}$ lead to ground programs the oscillator frequency for the converter according to the chart in Figure 36.
The resistive divider also sets a voltage on the OCSET lead. This voltage programs the module overcurrent trip point. The module overcurrent comparator, or OC Comparator, uses the OCSET lead voltage as the reference against which the module output current signal is compared. The output current of each phase is given as $\left(\mathrm{V}_{\mathrm{CSx}}-\mathrm{V}_{\text {CSREF }}\right)$ divided by the equivalent series resistance of the inductor. The voltage information $\left(\mathrm{V}_{\mathrm{CSx}}-\mathrm{V}_{\mathrm{CSREF}}\right)$ is gained up by a factor of 3.7 and summed for all three phases at the non-inverting input of the OC Comparator. The fault latch is set if the module overcurrent limit is exceeded. This results in "hiccup-mode" operation until the overcurrent condition is cleared.


Figure 35.


Figure 36. Fosc vs. R1 + ROCSET
Additionally, the total value of resistance between R $\mathrm{R}_{\mathrm{OSC}}$ and ground also programs the $\mathrm{V}_{\mathrm{FB}}$ pin bias current. $\mathrm{V}_{\mathrm{FB}}$ bias current is equal to 0.333 V divided by the total resistance from Rosc to ground. This current is used to generate the droop function in the adaptive voltage positioning circuitry and is discussed further in that section.

## Current Sense Components

Current sense components are chosen for two reasons. First, the value of $\mathrm{R}_{\mathrm{CSx}}$ and $\mathrm{C}_{\mathrm{CSx}}$ should be chosen to meet the criterion:

$$
\left(\mathrm{R}_{\mathrm{CSx}}\right)\left(\mathrm{C}_{\mathrm{CSx}}\right) \geq(\mathrm{L}) /\left(\mathrm{ESRL}_{\mathrm{L}}\right)
$$

where L is the inductor value and $\mathrm{ESR}_{\mathrm{L}}$ is the inductor equivalent series resistance. Meeting this criterion will ensure that the module overcurrent limit is not exceeded during current transients. Second, $\mathrm{R}_{\mathrm{CSx}}$ and $\mathrm{C}_{\mathrm{CSx}}$ should be chosen to add a small amount of ramp to the system. This will provide stable, jitter-free operation. The amount of ramp voltage required depends on several factors: supply voltage, output voltage (DAC code), switching frequency and board layout all affect the amount of artificial ramp required to some degree. The power supply designer should be aware that choosing the value of artificial ramp is a trade-off. As artificial ramp amplitude increases, the system becomes less prone to duty cycle jitter, but transient response will suffer. Adding 20 mV of artificial ramp is a good compromise and can be used to start design.

The current sense ramp is generated from the square wave obtained at the switching node of each phase by using an RC filter. The RC filter components for the CSx leads should be chosen to satisfy the following formula:

$$
R_{\mathrm{CSx}} \mathrm{CcSx}_{\mathrm{C}} \leq \frac{\left(\mathrm{V}_{\text {OUT }}\right)\left(1-\left(\mathrm{V}_{\text {OUT }} / \mathrm{V}_{\mathrm{CC}}\right)\right)}{(\mathrm{fOSC})\left(\mathrm{V}_{\text {RAMP }}\right)}
$$

Choose a convenient standard value for $\mathrm{C}_{\mathrm{CSx}}$ and solve for the value of $\mathrm{R}_{\mathrm{CSx}}$. Each of the three output phases requires its own RC combination.
An RC filter is also required for the $\mathrm{CS}_{\text {REF }}$ connection. This filter may use the same value of capacitance identified
for the CS1, CS2 and CS3 leads, but the value of resistance should be one third that of $\mathrm{R}_{\mathrm{CSx}}$ :

```
RCSREF = RCSx/3
```

This change is necessary to compensate for the difference in bias current between the $\mathrm{CS}_{\text {REF }}$ lead and each CSx lead. The schematic in Figure 37 shows the connection of these components.


Figure 37.

## Share Bus Components

Five external components are required to implement the module-to-module current share function. These components set the current sense load line, provide the share bus pull-down and compensate the share adjust amplifier.
The share current sense amplifier monitors the total module current and provides a DC voltage output proportional to that current. The share sense amplifier gain is programmable and allows the user to set the share bus transconductance. It is important that all modules in a system have a share current load line that approximates that of all the other modules to ensure accurate module-to-module current sharing. Let us arbitrarily set the share bus maximum voltage for full load at 2 V . If a module is designed to provide 81 A at full load, the module share transconductance should be $81 \mathrm{~A} / 2 \mathrm{~V}$ or $40.5 \mathrm{~A} / \mathrm{V}$. Two resistors and a capacitor set the share current sense amplifier gain. The resistors set the DC gain while the capacitor provides a zero to minimize errors due to noise.
The total module current is measured as described in the section dealing with the OCSET current limit function. That is, each phase within a module generates a voltage between the CSx and $\mathrm{CS}_{\mathrm{REF}}$ leads that is proportional to the current flow in the output inductor and the inductor's ESR:

$$
V_{C S x}-V_{C S R E F}=\left(I_{L}\right)\left(E S R_{L}\right)
$$

This signal is amplified by a factor of 3.7 for each phase and then summed for all three phases. This signal is provided as input to the share current sense amplifier. If we assume that all three phases are sharing current equally within a single module, the input to the share current sense amplifier can be expressed as:

$$
\begin{aligned}
\mathrm{V}_{\mathrm{IN}}(\mathrm{SENSE}) & =11.1\left(\mathrm{~V}_{\mathrm{CS}}-\mathrm{V}_{\mathrm{CSREF}}\right) \\
& =11.1\left(\mathrm{I}_{\mathrm{L}}\right)\left(\mathrm{ESR}_{\mathrm{L}}\right)=3.7\left(\mathrm{IOUT}^{(\mathrm{ESR}} \mathrm{L}\right)
\end{aligned}
$$

If we set $\mathrm{I}_{\mathrm{L}}$ equal to the maximum per phase current at full load, and if we know the value of ESR for our inductors, we
can calculate the required share current sense amplifier gain as:

$$
\operatorname{AV}(\text { SHARESENSE })=\frac{\text { share maximimum voltage }}{\operatorname{VIN}^{(S E N S E)}}
$$

As an example, let us again consider the case for a module providing full load current of 81 A . Each output phase is conducting 27 A . If we assume $\mathrm{ESR}=1.5 \mathrm{~m} \Omega$ then input to the share current sense amplifier is $(11.1)(27 \mathrm{~A})(1.5 \mathrm{~m} \Omega)=$ 0.45 V . The required share current sense amplifier gain is then $2 \mathrm{~V} / 0.45 \mathrm{~V}=4.44$.


Figure 38.
From the schematic in Figure 38, we derive the DC gain as:

$$
\operatorname{AV}(\text { SHARESENSE })=4.44=\left(\mathrm{RIOUT}^{2} / \mathrm{RIFB}\right)+1
$$

This specifies that $\mathrm{R}_{\text {IOUT }}$ should be 3.44 times greater than $\mathrm{R}_{\text {IFB }}$.

Another important consideration is the type of resistor selected for $\mathrm{R}_{\mathrm{IFB}}$. The thermal performance of $\mathrm{R}_{\mathrm{IFB}}$ must match that of whatever sense element is being used to monitor module current. Inductive sensing has been shown to be reasonably accurate, but copper's thermal coefficient of resistivity is approximately +4000 parts per million per ${ }^{\circ} \mathrm{C}$ ( $0.4 \%$ per ${ }^{\circ} \mathrm{C}$ ). In order to maintain accurate control of the share bus over temperature, $\mathrm{R}_{\mathrm{IFB}}$ must have a similar thermal coefficient. This requires a positive temperature coefficient element such as the KOA-Speer LT73. If a standard sense resistor is used in series between the inductor and the load, there is no need to use special resistors for sensing, but efficiency will suffer due to power dissipation in the sense resistor.

As regards the value of $\mathrm{C}_{\text {IOUT }}$, it should be noted that the complete transfer function for the share current sense amplifier in Figure 38 is:

$$
A V(S H A R E S E N S E)=\frac{R_{I O U T}}{R_{\operatorname{IFB}}\left(1+s C_{I O U T} R_{I O U T}\right)}+1
$$

$\mathrm{C}_{\text {IOUT }}$ causes the gain for high frequency noise to decrease, thus quieting the share bus.

The share resistor provides a passive pull-down on the SHARE lead. This allows the share bus voltage to be pulled all the way down to ground. The share resistor is selected to satisfy a number of criteria. First, the resistor cannot be made too small. The SHARE lead source current is guaranteed to be above 1 mA and must be capable of driving the SHARE
lead voltage to 3 V . The share bus of one module serves as master to all and drives the total resistance of all SHARE leads. Thus, the total impedance of all share resistors should be made greater than or equal to $3 \mathrm{k} \Omega$. That is,

$$
3 \mathrm{k} \Omega \geq \text { RSHARE } / \mathrm{N}
$$

where N is the maximum number of modules that can be placed in parallel as defined by the designer. As an example, if ten is the maximum number of modules that may be paralleled, then the minimum value of $\mathrm{R}_{\text {SHARE }}$ should be $30 \mathrm{k} \Omega$.

The share resistor should also not be made too large, since this is the only pull-down on the SHARE lead. Transient response of the share bus is limited by the RC time constant of the share resistance and any parasitic capacitance found on the SHARE line between modules.

## Droop Components

The CS5305 offers adaptive voltage positioning. This feature allows the output voltage to be set at different levels according to the amount of current being provided by the module. The output voltage is somewhat higher than nominal under no load or light load conditions and somewhat lower than nominal under heavy load conditions. Both set points must fall within the Power Good window. The adaptive positioning allows for overshoot and undershoot conditions that occur during load current transients and results in a reduction in the peak-to-peak $\mathrm{V}_{\text {OUT }}$ voltage excursion during load current transients.

Three components are required to implement DC adaptive voltage positioning. Resistor $\mathrm{R}_{\mathrm{FB}}$ is connected between the module $\mathrm{V}_{\mathrm{OUT}}$ (SENSE)+ lead and the $\mathrm{V}_{\mathrm{FB}}$ lead. Resistor $\mathrm{R}_{\mathrm{DRP}}$ is connected between the $\mathrm{V}_{\text {DRP }}$ lead and $\mathrm{V}_{\mathrm{FB}}$ lead. Resistor $\mathrm{R}_{\text {VSENSE }}$ is connected between the $\mathrm{V}_{\text {OUT(SENSE)+ }}$ lead and the module $\mathrm{V}_{\text {OUt }}$ lead. These connections are shown in Figure 39.


Figure 39.
The first step in choosing these components is to select the appropriate no-load and full-load output voltage set points for the particular DAC code being used. Additionally, the values of $\mathrm{R}_{\text {OSC }}$ and $\mathrm{R}_{\text {OCSET }}$ should be known, as should ESR of the output inductors and the full-load output current.


Figure 40.
As was previously noted, the total value of resistance between the $\mathrm{R}_{\text {OSC }}$ pin and ground sets the $\mathrm{V}_{\mathrm{FB}}$ lead bias current according to:

$$
\mathrm{I}\left(\mathrm{~V}_{\mathrm{FB}}\right)=0.333 \mathrm{~V} /(\mathrm{ROSC}+\mathrm{ROCSET})
$$

Referring to Figure 40, the $\mathrm{V}_{\text {DRP }}$ lead voltage is equal to the DAC voltage plus the current sense information. Under no load conditions, the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pin voltages are equal, and the entire $\mathrm{V}_{\mathrm{FB}}$ bias current flows between $\mathrm{V}_{\text {OUT(SENSE)+ }}$ and $\mathrm{V}_{\mathrm{FB}}$ through $\mathrm{R}_{\mathrm{FB}}$. Because the $\mathrm{V}_{\mathrm{FB}}$ bias current sinks into $\mathrm{V}_{\mathrm{FB}}$, the output voltage is forced to be higher than the DAC voltage, and so the value of $\mathrm{R}_{\mathrm{FB}}$ can be calculated as:

$$
\mathrm{R}_{\mathrm{FB}}=\left(\mathrm{V}_{\text {OUT }} \text { no load set point }-\mathrm{V}_{\mathrm{DAC}}\right) / \mathrm{I}\left(\mathrm{~V}_{\mathrm{FB}}\right)
$$

With $R_{F B}$ chosen, we can now select the value of $R_{\text {DRP }}$. If we again refer to Figure 40, we can use Kirchoff's Current Law at the $\mathrm{V}_{\mathrm{FB}}$ node to find that the value of $\mathrm{R}_{\mathrm{DRP}}$ is defined as:

$$
R_{D R P}=\frac{(\text { full load current })(3.7)\left(\mathrm{ESR}_{\mathrm{L}}\right)\left(\mathrm{R}_{\mathrm{FB}}\right)}{\left(\mathrm{R}_{\mathrm{FB}}\right)\left(\mathrm{I}\left(\mathrm{~V}_{\mathrm{FB}}\right)\right)+\left(\mathrm{V}(\mathrm{DAC})-\mathrm{V}_{\mathrm{OUT}} \text { full load set point }\right)}
$$

$\mathrm{R}_{\text {VSENSE }}$ is used to ensure that a connection between $\mathrm{V}_{\text {OUT }}$ and $\mathrm{V}_{\text {OUT(SENSE) }}$ always exists. This ensures that the module will operate correctly in the event that the $\mathrm{V}_{\text {OUT(SENSE) }}$ connection is broken. The module-to-load interface and the number of modules placed in parallel determine the value of RVSENSE. The CS5305 is specified to operate correctly with up to 55 mV dropped across the module connector. It is assumed that the maximum current allowed to flow in this connection to the load is 1 mA .

$$
\text { RVSENSE }=55 \mathrm{mV} /(1 \mathrm{~mA} / \mathrm{N})
$$

where:
$\mathrm{N}=$ the number of modules to be paralleled.
If four modules are to be paralleled, each contributes a maximum of $250 \mu \mathrm{~A}$ to this connection, and so $\mathrm{R}_{\text {VSENSE }}=$ $55 \mathrm{mV} / 250 \mu \mathrm{~A}=220 \Omega$. This component is placed to ensure the VRM module will regulate correctly if the module $\mathrm{V}_{\text {OUT(SENSE)+ }}$ connection to the load is opened.

The transient droop performance should be checked next. Performance should be verified using the transient test tool typically provided in a microprocessor development kit. True transient performance can be masked even at test frequencies as low as 2 kHz . It should be possible to modify
the test tool so a function generator can drive it. Using lower frequency (approximately 100 Hz ) and lower duty cycle $(10 \%)$ allow the designer to better observe the true settling behavior of the VRM module.

It may be necessary to add some filtering components to the droop voltage divider. These components cause the AC and DC gain from the current sense circuitry to match and allow the user to tailor the droop output voltage performance.
There are two methods for tuning droop performance. The first is illustrated in Figure 41. In this case, capacitors CDRP and $C_{F B}$ are placed in parallel with $R_{D R P}$ and $R_{F B}$. A third capacitor $\mathrm{C}_{\mathrm{DRCMP}}$ is connected between the COMP and $\mathrm{V}_{\text {DRP }}$ leads. The first two capacitors correct any gain errors introduced in the selection of current sense components Rcsx and Ccsx. Values for these components are defined as:

$$
C_{F B}=L /\left(\left(R_{F B}\right)\left(E S R_{L}\right)\right)
$$

and

$$
C_{D R P}=\left(\left(C_{C S x}\right)\left(R_{C S x}\right)\right) / R_{D R P}
$$

The capacitor between $V_{\text {DRP }}$ and COMP allows the user to fine-tune the transition between "fast" AVP and the slower positioning set by resistors $\mathrm{R}_{\mathrm{DRP}}$ and $\mathrm{R}_{\mathrm{FB}}$. This capacitor may or may not be required and is empirically chosen based on the fine-tuning procedure described below. A value of 1 nF is recommended as an initial value.


Figure 41.
Set up the circuit to be tested with a DVM and oscilloscope to the output. Have the scope set to DC input and set its offset so a resolution of at least $100 \mathrm{mV} / \mathrm{div}$ is used and the output is visible on the screen.
Using a DVM, measure the output voltage with no load. If this value differs from the expected value, adjust $\mathrm{R}_{\mathrm{FB}}$ until the nominal value is reached. Once this is set, mark this DC level on the scope with a cursor.
Next, measure the output voltage with full DC load. If this value deviates from the expected value, adjust $R_{\text {DRP }}$ until the nominal value is reached. Once this is set, mark this DC level on the scope with another cursor.


Figure 42.

Using the transient test tool, set up a current load step from low current ( 1 A ) to maximum load at the slew rate being designed for. Set the current step at about 100 Hz with a duty cycle of $10 \%$. Converter response should be similar to that shown in Figure 42.

Next, determine if there is a "bump" (trace 4 or trace 5) in the output. Adjust $\mathrm{C}_{\text {COMP }}$ and $\mathrm{C}_{\text {DRCMP }}$ to flatten out this bump. If the "bump" is negative (trace 5), make C ${ }_{\text {DRCMP }}$ slightly larger and $\mathrm{C}_{\text {COMP }}$ slightly smaller. If you see a positive "bump" (trace 4), make CDRCMP slightly smaller and $\mathrm{C}_{\text {COMP }}$ slightly larger. If performance is better without $\mathrm{C}_{\text {DRCMP }}$, just make C1 larger.

Once the bump is removed, look to see if the "pulse step" magnitude is larger or smaller than the DC level (trace 2 or trace 3). Make $\mathrm{C}_{\mathrm{FB}}$ slightly larger if the AC gain (trace 3 ) is too large or slightly smaller if the AC gain (trace 2) is too small. Once the output response resembles the "optimal" trace (trace 1), the controller has been optimized for the design from a static and dynamic response.

If the output appears to be jittering slightly prior to optimizing transient response, make the previous adjustments first, since they may solve the problem. If the problem persists, decreasing the value of Rcsx across the inductor will increase ramp amplitude, and jitter performance should improve with increased ramp.

The second method uses a capacitor to "square up" the COMP waveform and a series resistor and capacitor to tune the $\mathrm{V}_{\mathrm{DRP}}$ waveform. These components are chosen empirically based on observations of COMP and $V_{\text {DRP }}$ performance.

First, set the test tool for a load current transient from no load (1 A) to full load and observe the COMP waveform.

The COMP waveform should ideally be flat, or at worst decrease slightly during a current increase transient. The principle at work here is that the increase in current sense information will generate a voltage that should exactly cancel the droop voltage, and thus the COMP capacitor voltage should not change. In reality, it is unlikely that every manufactured module can be built to perfectly compensate the droop voltage, and so the COMP voltage should exhibit a small amplitude square wave during transient conditions. If the COMP voltage is decreasing gradually, the current sense information is too small to fully compensate for the droop voltage, and the designer should add a capacitor between $\mathrm{V}_{\text {OUT }}$ and COMP. This capacitor is chosen empirically, with 1 nF a good starting point. This capacitor will pull the COMP pin down initially and "square up" the COMP waveform as shown in Figure 43.


Figure 43.

In a similar manner, if the current information is too large, the COMP voltage will rise to compensate. Again, a square wave is preferable to a slow change in the COMP voltage, and placing a capacitor between $\mathrm{V}_{\mathrm{DRP}}$ and COMP will "square up" the COMP waveform as shown in Figure 44.


Figure 44.
Once the COMP waveform has been squared up, it is necessary to check the $\mathrm{V}_{\mathrm{DRP}}$ waveform. The $\mathrm{V}_{\mathrm{DRP}}$ waveform is dependent on the choice of ramp components. If these components have been chosen such that $\left(\mathrm{R}_{\mathrm{CSx}}\right)\left(\mathrm{C}_{\mathrm{CSx}}\right)=\mathrm{L} / \mathrm{ESR}_{\mathrm{L}}$, the $\mathrm{V}_{\text {DRP }}$ waveform should be a square wave that matches the current step. At this point, the V VUT waveform should also be a square wave and transient performance should be optimized.

If $\left(\mathrm{R}_{\mathrm{CSx}}\right)\left(\mathrm{C}_{\mathrm{CSx}}\right)<\mathrm{L} / \mathrm{ESR}_{\mathrm{L}}$, the $\mathrm{V}_{\mathrm{DRP}}$ waveform will be faster than current step. The $V_{\text {DRP }}$ voltage will exhibit a fast rise followed by an exponential droop down to a DC level, as shown in Figure 45. This waveform has the effect of telling the system that transient current signals are larger than the true current. Response will be slowed, and $\mathrm{V}_{\text {OUT }}$ will overshoot until the error amplifier "catches up". In this case, it is desirable to push the $\mathrm{V}_{\mathrm{FB}}$ pin down, so that COMP voltage is forced up and duty cycle is reduced slightly. This is done by placing a series RC filter across resistor $\mathrm{R}_{\mathrm{FB}}$.


Figure 45.
If $\left(\mathrm{R}_{\mathrm{CSx}}\right)\left(\mathrm{C}_{\mathrm{CSx}}\right)>\mathrm{L} / \mathrm{ESR}_{\mathrm{L}}$, the $\mathrm{V}_{\mathrm{DRP}}$ waveform will be slower than the current step. $\mathrm{V}_{\text {DRP }}$ will exhibit an initial spike, but the voltage will then exponentially rise toward its correct DC level, as shown in Figure 46. This waveform effectively tells the system that the current signal is smaller than the true current, and response will be faster than optimal. $V_{\text {OUT }}$ will then undershoot. In this case, forcing
$\mathrm{V}_{\mathrm{FB}}$ up so COMP voltage decreases results in increasing output duty cycle. The series RC filter is now located in parallel with $\mathrm{R}_{\mathrm{DRP}}$.


Figure 46.
These components are chosen empirically. The fastest way to optimize the design is to start with a 1 nF capacitor and a $500 \mathrm{k} \Omega$ potentiometer and "dial in" performance.

## Error Amplifier Compensation

Error amplifier compensation is very simple using the enhanced $\mathrm{V}^{2}$ control architecture. A single $0.1 \mu \mathrm{~F}$ capacitor from the COMP lead to ground is usually sufficient. As an alternative, a resistor and capacitor in series between COMP and ground may improve output voltage positioning during current transients. The resistance will speed up the effective slew rate of the error amplifier output.
The COMP capacitor also provides soft start and hiccup-mode timing. At start-up, the COMP capacitance must charge from ground through a typical channel start-up offset of 0.6 V before the GATE outputs are allowed to begin switching. The COMP capacitance includes both the COMP capacitor and any droop compensation capacitance that may be connected to the COMP pin. The typical soft start time can then be approximated as:

$$
\text { TSOFT-START(ms) = } 20 \text { CCOMP(TOTAL) }(\mu \mathrm{F})
$$

Hiccup timing has a similar equation. During hiccup-mode, the COMP voltage traverses between the fault reset threshold (approximately 0.2 V ) and the channel start-up offset voltage. When the fault circuitry becomes active, the COMP capacitor is discharged with a $5 \mu \mathrm{~A}$ current until the fault reset threshold is reached. The time this initial discharge takes is variable depending on the COMP voltage when the fault occurred. Once the reset threshold is reached, the COMP capacitor is charged with the $30 \mu \mathrm{~A}$ current until the start-up offset voltage is reached. The GATE outputs will begin to pulse, quickly ramping the inductor current. The fault circuitry can then re-detect the fault condition some number of GATE pulses later if it is still present. Thus, the period of the fault hiccup mode is approximately defined as:

$$
\mathrm{THICCUP}(\mathrm{~ms})=93.3 \mathrm{C} \operatorname{COMP}(\mathrm{TOTAL})(\mu \mathrm{F})
$$

Period is only approximately defined since the number of GATE pulses between restart and redetection of a fault condition is unpredictable.

## Inductors

There are many factors to consider when choosing the output inductors. Maximum load current, core and winding losses, ripple current, short circuit current, saturation characteristics, component height and cost are all variables that the designer should consider. However, the most important consideration in designing for the VRM 9.x specifications may be the effect inductor value has on transient response.

The amount of overshoot or undershoot exhibited during a current transient is defined as the product of the current step and the output filter capacitor ESR. To some degree, adaptive voltage positioning is used to "pre-position" the output voltage so the voltage step during a current transient will not cause the output voltage to exceed the Power Good window. However, adaptive positioning will not completely eliminate the overshoot or undershoot conditions, and choosing the inductor value appropriately can minimize the amount of energy that must be transferred from the inductor to the capacitor or vice-versa. In the subsequent paragraphs, we will determine the minimum value of inductance required for our system and consider the trade-off of ripple current vs. transient response.

In order to choose the minimum value of inductance, input voltage, output voltage and output current must be known. Most computer applications use reasonably well regulated bulk power supplies so that, while the equations below specify $\mathrm{V}_{\text {IN(MAX) }}$ or $\mathrm{V}_{\text {IN(MIN) }}$, it is possible to use the nominal value of $\mathrm{V}_{\mathrm{IN}}$ in these calculations with little error.

Current in the inductor while operating in the continuous current mode is defined as the load current plus ripple current.

$$
\mathrm{I}_{\mathrm{L}}=\mathrm{I}_{\mathrm{LOAD}}+\mathrm{I}_{\text {RIPPLE }}
$$

The ripple current waveform is triangular, and the current is a function of voltage across the inductor, switch FET on-time and the inductor value. FET on-time can be defined as the product of duty cycle and switch frequency, and duty cycle can be defined as a ratio of $\mathrm{V}_{\text {OUT }}$ to $\mathrm{V}_{\text {IN }}$. Thus,

$$
\text { IRIPPLE }=\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}\right)}
$$

Peak inductor current is defined as the load current plus half of the peak current. Peak current must be less than the maximum rated FET switch current, and must also be less than the inductor saturation current. Thus, the maximum output current for a single phase can be defined as:
$\operatorname{IOUT}(\mathrm{MAX})=\operatorname{ISWITCH}(\mathrm{MAX})-\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MAX})-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{(2)(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}(\mathrm{MAX})\right)}$

Since the maximum output current must be less than the maximum switch current, the minimum inductance required for a single phase can be determined.

$$
\mathrm{L}_{(\mathrm{MIN})}=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\mathrm{OUT}}\right) \mathrm{V}_{\mathrm{OUT}}}{(\mathrm{fOSC})(\mathrm{ISWITCH}(\mathrm{MAX}))\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})\right)}
$$

This equation identifies the value of inductor that will provide the full rated switch current as inductor ripple current, and will usually result in inefficient system operation. The system will sink current away from the load during some portion of the duty cycle unless load current is greater than half of the rated switch current. Some value larger than the minimum inductance must be used to ensure the converter does not sink current. Choosing larger values of inductor will reduce the ripple current, and inductor value can be designed to accommodate a particular value of ripple current by replacing $\mathrm{I}_{\text {SWITCH(MAX) }}$ with a desired value of I RIPPLE:

$$
\mathrm{L}_{(\mathrm{RIPPLE})}=\frac{\left(\mathrm{V}_{\text {IN }}(\mathrm{MIN})-\mathrm{V}_{\mathrm{OUT}}\right) \mathrm{V}_{\mathrm{OUT}}}{(\mathrm{fOSC})(\mathrm{IRIPPLE})\left(\mathrm{V}_{\mathrm{IN}(\mathrm{MIN})}\right)}
$$

However, reducing the ripple current will cause transient response times to increase. The response times for both increasing and decreasing current steps are shown below.

$$
\begin{aligned}
& \text { TRESPONSE(INCREASING) }=\frac{(\mathrm{L})\left(\Delta \mathrm{I}_{\mathrm{OUT}}\right)}{\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right)} \\
& \text { TRESPONSE }^{\text {DECREASING })}=\frac{(\mathrm{L})\left(\Delta \mathrm{I}_{\mathrm{OUT}}\right)}{\left(\mathrm{V}_{\mathrm{OUT}}\right)}
\end{aligned}
$$

Inductor value selection also depends on how much output ripple voltage the system can tolerate. Output ripple voltage is defined as the product of the output ripple current and the output filter capacitor ESR. However, since the CS5305 has three paralleled phases, the net effect is that the switching frequency as seen by the output capacitance is tripled relative to the CS5305 operating frequency. This is because each phase switches in sequence and the ripple currents in each phase are superimposed on the output capacitance. This is illustrated graphically in Figures 45 and 46.

Thus, output ripple voltage can be calculated as:
$\mathrm{V}_{\text {RIPPLE }}=\left(\mathrm{ESR}_{\mathrm{C}}\right)(\operatorname{IRIPPLE})=\frac{\left(\mathrm{ESRC}_{\mathrm{C}}\right)\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \mathrm{V}_{\text {OUT }}}{3(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}\right)}$
It is also important to note that the maximum value of inductor ESR is limited by the single-phase pulse-by-pulse current limit. The specified minimum value for this parameter is 80 mV , so the maximum inductor ESR is:
$E S R_{L(M A X)}$ (in ohms) $=\frac{(0.08 \mathrm{~V})}{(\text { single phase current limit value in Amps) }}$


Figure 47.
Finally, we should consider power dissipation in the output inductors. Power dissipation is proportional to the square of inductor current:

$$
P \mathrm{D}=\left(\mathrm{I}_{\mathrm{PHASE}}^{2}\right)\left(E S R_{\mathrm{L}}\right)
$$

The temperature rise of the inductor relative to the air surrounding it is defined as the product of power dissipation and thermal resistance to ambient:

$$
\Delta \mathrm{T}(\text { inductor })=(\mathrm{Ra})(\mathrm{PD})
$$

Ra for an inductor designed to conduct 20 A to 30 A is approximately $45^{\circ} \mathrm{C} / \mathrm{W}$. The inductor temperature is given as:

$$
\mathrm{T} \text { (inductor) }=\Delta \mathrm{T} \text { (inductor) }+ \text { Tambient }
$$

## Output Filter Capacitors

Each microprocessor manufacturer specifies output filter capacitors for the motherboards. In addition, the designer may need to add some output capacitance on the VRM module. These added output capacitors would serve to reduce the noise floor and help ensure jitter-free operation. If needed, one or two ceramic capacitors should be sufficient. They should have a 4 WVDC rating. Large amounts of bulk capacitance placed on the VRM module are not useful, since the impedance of the VRM connector exists between the module and the load. Low equivalent series resistance is important since output ripple voltage and response to output current transients are largely dependent on this parasitic parameter.

## $\mathrm{V}_{\mathrm{Cc}}$ Bypass Filtering

A small RC filter should be added between module $\mathrm{V}_{\mathrm{CC}}$ and the $\mathrm{V}_{\mathrm{CC}}$ input to the CS5305. A $10 \Omega$ resistor and a $0.1 \mu \mathrm{~F}$ capacitor should be sufficient to ensure the controller IC does not operate erratically due to injected noise.

## Module Input Filter Capacitors

The input filter capacitors for the VRM module provide a charge reservoir that minimizes supply voltage variations due to changes in current flowing through the switch FETs. These capacitors must be chosen primarily for ripple current rating.


Figure 48.
Consider the schematic shown in Figure 48. The average current flowing in the input inductor $\mathrm{L}_{\mathrm{IN}}$ for any given output current is:

$$
\begin{aligned}
\mathrm{I} \mathrm{~N}(\mathrm{AVE}) & =(\mathrm{I} \mathrm{OUT})(\mathrm{V} \text { OUT } / \mathrm{V} \text { IN }) \\
& =(\mathrm{IOUT} \text { per phase })(\mathrm{n})(\mathrm{D})
\end{aligned}
$$

where:
$\mathrm{D}=$ duty cycle,
$\mathrm{n}=$ number of phases.
Input capacitor current is positive into the capacitor when the switch FETs are off, and negative out of the capacitor when the switch FETs are on. When the switches are off, $\mathrm{I}_{\text {IN(AVE) }}$ flows into the capacitor. When the switches are on, capacitor current is equal to the per-phase output current minus $\mathrm{I}_{\mathrm{IN}(\mathrm{AVE})}$. If we ignore the small current variation due to the output ripple current, we can approximate the input capacitor current waveform as a square wave. We can then calculate the RMS input capacitor ripple current:


The input capacitance must be designed to conduct the worst case input ripple current. This will require several capacitors in parallel. In addition to the worst case current, attention must be paid to the capacitor manufacturer's derating for operation over temperature.

As an example, let us define the input capacitance for a 12 V to 1.7 V conversion at 81 A , or 27 A per phase at an ambient temperature of $60^{\circ} \mathrm{C}$. A droop voltage of 90 mV to 1.61 V and efficiency of $80 \%$ is assumed. Average input current in the input filter inductor is:

$$
\mathrm{I}_{\mathrm{I}} \mathrm{~N}(\mathrm{AVE})=\frac{(27 \mathrm{~A})(3 \text { phases })(1.61 \mathrm{~V} / 12 \mathrm{~V})}{80 \%}=10.868 \mathrm{~A}
$$

Input capacitor RMS ripple current is then

$$
\begin{aligned}
\operatorname{IIN}(\mathrm{RMS}) & =\sqrt{\begin{array}{l}
10.868^{2}+\frac{1.61 \mathrm{~V}}{12 \mathrm{~V}} \times 3 \\
\times\left[(27 \mathrm{~A}-10.868 \mathrm{~A})^{2}-10.868 \mathrm{~A}^{2}\right]
\end{array}} \\
& =13.347 \mathrm{~A}
\end{aligned}
$$

If we consider a Sanyo SP series capacitor, the ripple current rating for a 16 SPS 100 M capacitor is 2820 mA at 100 kHz and $45^{\circ} \mathrm{C}$. The derating factor is 0.85 for operation up to $65^{\circ} \mathrm{C}$, resulting in an effective ripple current rating of 2397 mA . We determine the number of input capacitors by dividing the ripple current by the per-capacitor current rating:

Number of capacitors $=13.347 \mathrm{~A} / 2.397 \mathrm{~A}=5.52$
A total of at least 6 capacitors in parallel must be used to meet the input capacitor ripple current requirements.

## Output Switch FETs

Output switch FETs must be chosen carefully, since their properties vary widely from manufacturer to manufacturer. The CS5305 system is designed assuming that a FET driver IC and $n$-channel FETs will be used. The FET characteristics of most concern are the gate charge/gate-source threshold voltage, gate capacitance, on-resistance, current rating and the thermal capability of the package.

FET driver ICs have a limited drive capability. If the switch FET has a high gate charge, the amount of time the FET stays in its ohmic region during the turn-on and turn-off transitions is larger than that of a low gate charge FET, with the result that the high gate charge FET will consume more power. Similarly, a low on-resistance FET will dissipate less power than will a higher on-resistance FET at a given current. Thus, low gate charge and low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ will result in higher module efficiency and will reduce heat being generated by the VRM module.

It can be advantageous to use multiple switch FETs to reduce power consumption. By placing a number of FETs in
parallel, the effective $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ is reduced, thus reducing the ohmic power loss. However, placing FETs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel FET reduces the ohmic power loss more than the switching losses increase, there is some advantage to doing so. However, at some point the law of diminishing returns will take hold, and a marginal increase in efficiency may not be worth the board area required to add the extra FET. Additionally, as more FETs are used, the limited drive capability of the FET driver will have to charge a larger gate capacitance, resulting in increased gate voltage rise and fall times. This will affect the amount of time the FET operates in its ohmic region and will increase power dissipation.

The following equations can be used to calculate power dissipation in the switch FETs.

For ohmic power losses due to $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ :

$$
\begin{aligned}
\mathrm{PON}(\mathrm{TOP}) & =\frac{(\mathrm{RDS}(\mathrm{ON})(\mathrm{TOP}))(\mathrm{I} M \mathrm{RM}(\mathrm{TOP}))^{2}(\mathrm{n})}{(\text { number of topside FETs per phase })} \\
\mathrm{PON}(\mathrm{BOTTOM}) & =\frac{\left(\mathrm{RDS}(\mathrm{ON})(\mathrm{BOTTOM})(\mathrm{IRMS}(\mathrm{BOTTOM}))^{2}(\mathrm{n})\right.}{(\text { number of bottom-side FETs per phase })}
\end{aligned}
$$

where:
$\mathrm{n}=$ number of phases.
Note that $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ increases with temperature. It is good practice to use the value of $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ at the FET's maximum junction temperature in the calculations shown above.

$$
\begin{aligned}
& I_{R M S}(T O P)=\sqrt{I_{\text {PK }}^{2}-(I P K)\left(I_{R I P P L E}\right)+\frac{D}{3} I_{\text {RIPPLE }}^{2}} \\
& \operatorname{IRMS}(\text { BOTTOM })=I_{\text {PK }}^{2}-(\text { IPKIRIPPLE })+\frac{(1-\mathrm{D})}{3} I_{\text {RIPPLE }}^{2} \\
& \mathrm{I}_{\text {RIPPLE }}=\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right)\left(\mathrm{V}_{\text {OUT }}\right)}{(\mathrm{fOSC})(\mathrm{L})\left(\mathrm{V}_{\text {IN }}\right)} \\
& \text { IPEAK }=I_{\text {LOAD }}+\frac{\text { IRIPPLE }^{2}}{2}=\frac{\text { IOUT }}{3}+\frac{\text { IRIPPLE }}{2}
\end{aligned}
$$

where:
D = Duty cycle.
For switching power losses:

$$
\mathrm{PD}=\mathrm{nCV} 2(\mathrm{fOSC})
$$

where:
$\mathrm{n}=$ number of switch FETs (either top or bottom) per phase,
$\mathrm{C}=\mathrm{FET}$ gate capacitance,
$\mathrm{V}=$ maximum gate drive voltage (usually $\mathrm{V}_{\mathrm{CC}}$ ),
$\mathrm{f}_{\mathrm{OSC}}=$ switching frequency.

## External FET Driver

The CS5305 is designed such that an external FET driver IC is required. The GATE pin outputs are designed to drive a 100 pF load, and do not have sufficient drive capability to directly drive the gates of switch FETs. The GATE outputs have a typical output high voltage of 2.5 V , so the turn-on threshold of the FET driver should be approximately 2 V . The GATE outputs are also phased such that the FET driver IC should turn on the topside $n$-channel FET when the GATE output goes high. The bottom-side n-channel FET should be on when the GATE output is below the FET driver IC turn-on threshold.

Additionally, the CS5305 provides a signal called DRVON that can be connected to the ENABLE pin of FET drivers that offer an enable feature. If the FET driver's ENABLE input is high, the FET driver output is determined by the GATE input, and the switch FETs are driven according to the conditions described above. If the FET driver's ENABLE input is low, all switch FETs are turned off and no current is conducted to the load. This DRVON signal is a logic output from the CS5305. DRVON goes high when all internal functions of the CS5305 are operating correctly and the IC is not in fault mode. A table of the DRVON logic may be found in the Theory of Operation section.

Choosing a FET driver IC with an enable feature significantly improves system reliability, since a faulty module is essentially disconnected from the load.

## SGND Resistor

The module-to-load interface and the number of modules placed in parallel determine the value of $\mathrm{R}_{\text {SGND }}$. The CS5305 is specified to operate correctly with up to 55 mV dropped across the module connector. It is assumed that the maximum current allowed to flow in this connection to the load is 1 mA .

$$
\mathrm{RSGND}=55 \mathrm{mV} /(1 \mathrm{~mA} / \mathrm{N})
$$

where:
$\mathrm{N}=$ the number of VRM modules to be paralleled.
If four modules are to be paralleled, each contributes a maximum of $250 \mu \mathrm{~A}$ to this connection, and so,

$$
\text { RSGND }=55 \mathrm{mV} / 250 \mu \mathrm{~A}=220 \Omega
$$

This component is placed to ensure the VRM module will regulate correctly if the module $\mathrm{V}_{\text {OUT(SENSE)- }}$ connection to the load is opened.

## Layout Considerations

Enhanced $V^{2}$ performs best under dynamic load conditions if current ramp is kept small. However, this may lead to pulse-width jitter or pulse skipping, particularly as the ambient noise level at the control circuit increases. This is a complicated design trade-off that can not be mathematically characterized, and it is crucial to have a "quiet" layout. Following the design/layout guidelines below will provide the best system performance. Refer to Figure 50 for a layout example and to page 2312 for the associated schematic. Numbers in parentheses refer to IC pin numbers. Component names refer to the reference designators for the application schematic.
1.Noise across the PWM comparator inputs needs to be low or pulse width jitter will occur. Referring to the block diagram, the $\mathrm{CS}_{\text {REF }}$ pin (7) and the COMP pin (14) present external information to the PWM comparator. Any differential signal across these pins is expressed directly across the PWM comparator, which may cause pulse-width jitter or pulse skipping. The solution is to provide a dedicated Kelvin connection for sensing the VRM's V ${ }_{\text {OUT-. }}$ The IC's GND pin (28) and COMP capacitance need a dedicated sense line to $\mathrm{V}_{\text {OUT }}$, in effect making the IC and COMP capacitance $V_{\text {OUT-ground-referenced. }}$ This is desirable since the fast feedback path through $\mathrm{CS}_{\text {REF }}$ is connected to $\mathrm{V}_{\text {OUT+ }}$ and is therefore also Vout-ground-referenced. Furthermore, a ground strip under the IC is desirable since the COMP pin is located at the opposite corner of the IC from the GND pin. This ground strip further reduces the ambient noise level of the CS5305 along with providing a good connection from COMP return to GND and VOUT-. Following this guideline will provide the most system improvement from a layout standpoint.


Figure 49.
2.Differential noise across the PWM comparator can be further reduced if the $\mathrm{V}_{\text {OUT+ }}$ and $\mathrm{V}_{\text {OUT- }}$ sense lines going to $\mathrm{CS}_{\text {REF }}$ and GND are paralleled to minimize loop area. $V_{\text {OUT+ }}$ ripple information provided to the PWM comparator via the CS $_{\text {REF }}$ pin needs to be symmetric for all three phases or poor current sharing between phases will occur. This can be accomplished by placing the $V_{\text {OUT+ }}$ and $V_{\text {OUT- }}$ sense locations symmetrically with respect to the three output inductors. See Figure 49.
3.Frequency jitter could occur if the $\mathrm{R}_{\mathrm{OSC}}$ pin (2) and OCSET pin (1) components are not properly located. Most layouts will have two resistors in series from $\mathrm{R}_{\text {OSC }}$ to GND. Keep these two components as close as possible to the IC and ensure a short ground connection to the IC GND. Provision for a small cap ( 1000 pF or less) from $\mathrm{R}_{\mathrm{OSC}}$ to GND can be placed although this is rarely needed. If the $\mathrm{R}_{\text {OSC }}$ capacitor value is too large, the $\mathrm{R}_{\mathrm{OSC}}$ voltage reference will oscillate.
4.The $\mathrm{V}_{\mathrm{CC}}$ (23) bypass capacitor ( $0.1 \mu \mathrm{~F}$ or greater) should be located as close as possible to the IC. This capacitor's connection to GND must be as short as possible. The most effective way to implement this tight component placement is to via the GATE1, 2,3 and DRVON runs to internal layers right at the IC pins.
5.The switch nodes of all three phases must be sensed for inductive current sensing. Care should be given to how this information is brought to the CS5305. Switch node voltages should not be routed underneath or near the IC; however, the resistors in the RC filter of CS1, 2, 3 must be reasonably close to their associated capacitors so noise pick-up on the CS1, 2, 3 pins is minimized. The best solution is to locate the RC filter capacitors close to the CS1, 2, 3 pins and to place the respective resistors off to the side of the IC.
6.A positive temperature coefficient thermistor can be used for R11 (see Share Bus section) to compensate for thermal variation in the inductor ESR. This
component should be placed near the one of the inductors to achieve the best thermal coupling, and so the best current sharing performance. Remote placement with respect to the IC requires dedicated parallel runs of GND and $\mathrm{I}_{\mathrm{FB}}$ to reduce share bus noise sensitivity.

## Thermal Considerations

Typically, the controller IC and the FET gate drivers do not dissipate significant amounts of power, and do not contribute greatly to module power dissipation. The main components of concern are the switch FETs and the inductors.

We have already reviewed the power calculations for these components, but we haven't related them to a thermal solution. Standards exist limiting the maximum VRM printed circuit board temperature $\left(105^{\circ} \mathrm{C}\right.$ is common), and thus power dissipation becomes a thermal consideration in addition to playing a part in overall module efficiency.

Power dissipation on the VRM results in heat radiation to the surrounding air. Power dissipated by the components is conducted to the PCB. The PCB acts as a heat sink and provides a larger surface area for heat exchange to the surrounding air. The PCB temperature is dependent on total PCB power dissipation, the surface area of the PCB available to act as a heat sink, the ambient temperature of the surrounding air and the thermal resistance to ambient of the PCB.

While it is possible to model power dissipation on the PCB for efficiency purposes, it is very difficult to accurately model thermal performance. In particular, thermal resistance to ambient of the PCB varies widely. This parameter depends on many factors: board shape, size and material; copper weight; amount of exposed copper; insulating characteristics of the solder mask layers; air flow properties (amount, direction, PCB orientation to the airflow); and even whether a particular component is "hidden" behind others. In reality, modeling PCB resistance to ambient is highly complex and the best way to guarantee thermal performance is to actually build prototypes and measure it directly.


Figure 50. Sample Layout

## Additional Information

Several additional resources are available to make system design with the CS5305 a simpler task. The power supply designer is invited to obtain the following documents and files from ON Semiconductor.
1.AND8045/D, "Enhanced $V^{2}$ Multiphase SMPS for Microprocessor." This application note provides details on the theory of operation, selection of components, layout practices and thermal management strategies necessary to design power supplies with the CS5305 controller.
2."Excel Spreadsheet Method for Choosing CS5305 External Components". This Excel spreadsheet that can be used to generate a first-pass schematic design for VRM 9.x designs based on user input, and is available from the factory.
3."Excel Spreadsheet Method for CS5305 Power Budget Optimization". This Excel spreadsheet that can be used to calculate power dissipation in all the high-power dissipation components (including metal traces). This allows the design to be optimized for power/thermal management, and is available from the factory.

## CS5307

## Advance Information <br> Four-Phase <br> Buck CPU Controller

Multiphase controllers provide fast, accurate regulation with the control features required to power the next generation of processors in workstation and server applications. Combined with external gate drivers and power components, such controllers implement a compact, highly integrated buck converter. Enhanced $\mathrm{V}^{2 \mathrm{TM}}$ control inherently compensates for variations in both line and load. Current sharing between phases is achieved by Peak Current Sharing.

The CS5307 includes Power Good with a programmable lower threshold.

Applications include Embedded Processor Power and low voltage/high current power supplies.

## Features

- Switching Regulator Controller
- Four-Phase Operation
- Loss-Less Current Sensing
- Enhanced V ${ }^{2}$ Control Method Provides Excellent Regulation and Fast Transient Response
- Programmable 200 to 800 kHz Switching Frequency (Per Phase)
- Pulse-by-Pulse 0 to 100\% Adjustment of Duty Cycle as Required to Maintain Regulation
- Programmable Adaptive Voltage Positioning Reduces Output Capacitor Requirements
- Implements Converters Capable of Supplying Up to 25 A Per Phase of Low Voltage Output Current
- Programmable Soft Start
- Current Sharing
- Current Sharing Within 10\% Between Phases
- Protection Features
- Pulse-by-Pulse Current Limit for Each Phase
- Programmable Hiccup Overcurrent Protection
- All "1" DAC Code Fault
- Processor Overvoltage Protection through Bottom MOSFETs
- Undervoltage Lockout
- System Power Management
- 5-Bit DAC With 1.0\% Tolerance Compatible with Latest VRM Specifications
- Power Good Output
- Programmable Power Good Lower Threshold

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SO-24L DW SUFFIX CASE 751E

MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5307GDW24 | SO-24L | 27 Units/Rail |
| CS5307GDWR24 | SO-24L | 1000 Tape \& Reel |



Figure 1. Application Diagram, 12 V to $1.5 \mathrm{~V} / 80 \mathrm{~A}$ Four-Phase Converter

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Package Thermal Resistance Junction-to-Case, R ®Jc Junction-to-Ambient, R $\mathrm{R}_{\text {JA }}$ |  | $\begin{aligned} & 16 \\ & 80 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1.) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Number | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | $\mathrm{I}_{\text {SINK }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | GND | N/A | N/A | $0.4 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 100 \mathrm{~mA} \mathrm{DC}$ | N/A |
| 2 | OCSET | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 3 | Rosc | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 4-7 | CS1-CS4 | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 8 | $\mathrm{CS}_{\text {REF }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 9 | $V_{\text {DRP }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 10 | $V_{\text {FB }}$ | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 11 | COMP | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 12 | SS | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 13 | PWRGD | 18 V | -0.3 V | 1.0 mA | 10 mA |
| 14 | PWRGDS | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 15-19 | $\mathrm{V}_{\text {ID } 4}-\mathrm{V}_{\text {IDO }}$ | 18 V | -0.3 V | 1.0 mA | 1.0 mA |
| 20-23 | GATE4-GATE1 | 7.0 V | -0.3 V | $0.1 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 25 \mathrm{~mA} \mathrm{DC}$ | $0.1 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 25 \mathrm{~mA} \mathrm{DC}$ |
| 24 | $\mathrm{V}_{\mathrm{CC}}$ | 18 V | -0.3 V | 100 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATEx}}=100 \mathrm{pF}\right.$,
$\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{V}_{\text {OCSET }}=0.54 \mathrm{~V}$, DAC Code 01110 ; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $\mathbf{0}=$ Connected to GND, $1=$ Open or Pull-Up to Internal 3.3 V or External Voltage 12 V )

| Accuracy (all codes) $V_{\text {ID }}$ code |  |  |  |  | Connect $\mathrm{V}_{\mathrm{FB}}$ to COMP, Measure COMP | -1.0 | - | +1.0 | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {ID4 }}$ | VID3 | VID2 | $V_{\text {ID } 1}$ | $V_{\text {IDO }}$ |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 |  |  | Fault |  |  |
| 1 | 1 | 1 | 1 | 0 |  | 1.089 | 1.100 | 1.111 | V |
| 1 | 1 | 1 | 0 | 1 |  | 1.114 | 1.125 | 1.136 | V |
| 1 | 1 | 1 | 0 | 0 |  | 1.139 | 1.150 | 1.162 | V |
| 1 | 1 | 0 | 1 | 1 |  | 1.163 | 1.175 | 1.187 | V |
| 1 | 1 | 0 | 1 | 0 |  | 1.188 | 1.200 | 1.212 | V |
| 1 | 1 | 0 | 0 | 1 |  | 1.213 | 1.225 | 1.237 | V |
| 1 | 1 | 0 | 0 | 0 |  | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 1 | 1 | 1 |  | 1.263 | 1.275 | 1.288 | V |
| 1 | 0 | 1 | 1 | 0 |  | 1.287 | 1.300 | 1.313 | V |
| 1 | 0 | 1 | 0 | 1 |  | 1.312 | 1.325 | 1.338 | V |
| 1 | 0 | 1 | 0 | 0 |  | 1.337 | 1.350 | 1.364 | V |
| 1 | 0 | 0 | 1 | 1 |  | 1.361 | 1.375 | 1.389 | V |
| 1 | 0 | 0 | 1 | 0 |  | 1.386 | 1.400 | 1.414 | V |
| 1 | 0 | 0 | 0 | 1 |  | 1.411 | 1.425 | 1.439 | V |
| 1 | 0 | 0 | 0 | 0 |  | 1.436 | 1.450 | 1.465 | V |
| 0 | 1 | 1 | 1 | 1 |  | 1.460 | 1.475 | 1.490 | V |
| 0 | 1 | 1 | 1 | 0 |  | 1.485 | 1.500 | 1.515 | V |
| 0 | 1 | 1 | 0 | 1 |  | 1.510 | 1.525 | 1.540 | V |
| 0 | 1 | 1 | 0 | 0 |  | 1.535 | 1.500 | 1.566 | V |
| 0 | 1 | 0 | 1 | 1 |  | 1.560 | 1.575 | 1.591 | V |
| 0 | 1 | 0 | 1 | 0 |  | 1.584 | 1.600 | 1.616 | V |
| 0 | 1 | 0 | 0 | 1 |  | 1.609 | 1.625 | 1.641 | V |
| 0 | 1 | 0 | 0 | 0 |  | 1.634 | 1.650 | 1.667 | V |
| 0 | 0 | 1 | 1 | 1 |  | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 1 | 1 | 0 |  | 1.683 | 1.700 | 1.717 | V |
| 0 | 0 | 1 | 0 | 1 |  | 1.708 | 1.725 | 1.742 | V |
| 0 | 0 | 1 | 0 | 0 |  | 1.733 | 1.750 | 1.768 | V |
| 0 | 0 | 0 | 1 | 1 |  | 1.757 | 1.775 | 1.793 | V |
| 0 | 0 | 0 | 1 | 0 |  | 1.782 | 1.800 | 1.818 | V |
| 0 | 0 | 0 | 0 | 1 |  | 1.807 | 1.825 | 1.843 | V |
| 0 | 0 | 0 | 0 | 0 |  | 1.832 | 1.850 | 1.869 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID }}$ | 1.00 | 1.25 | 1.5 | V |
| Input Pull-Up Resistance |  |  |  |  | $\begin{aligned} & 0 V<V_{I D 4}, V_{I D 3}, V_{I D 2}, V_{I D 1}, \\ & V_{I D O}<3.3 \mathrm{~V} \end{aligned}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATEx}}=100 \mathrm{pF}\right.$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SS }}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{V}_{\text {OCSET }}=0.54 \mathrm{~V}$, DAC Code 01110 ; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $0=$ Connected to GND, $1=$ Open or Pull-Up to Internal 3.3 V or External Voltage 12 V ) (continued)

| Pull-Up Voltage | $1.0 \mathrm{M} \Omega$ to GND | 2.5 | 2.7 | 3.0 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

Power Good Output

| Upper Threshold |  |  |  |  | Force PWRGDS | 1.876 (-5\%) | 1.975 | 2.074 (+5\%) | V |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Lower Threshold |  |  |  |  | Force PWRGDS | -2.6\% | $\mathrm{V}_{\text {ID }} / 2$ | +2.6\% | V |
| VID4 | $V_{\text {ID3 }}$ | VID2 | $V_{\text {ID } 1}$ | $V_{\text {IDO }}$ |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | FAULT |  |  |  | V |
| 1 | 1 | 1 | 1 | 0 |  | 0.536 | 0.550 | 0.564 | V |
| 1 | 1 | 1 | 0 | 1 |  | 0.548 | 0.563 | 0.577 | V |
| 1 | 1 | 1 | 0 | 0 |  | 0.560 | 0.575 | 0.590 | V |
| 1 | 1 | 0 | 1 | 1 |  | 0.572 | 0.588 | 0.603 | V |
| 1 | 1 | 0 | 1 | 0 |  | 0.584 | 0.600 | 0.616 | V |
| 1 | 1 | 0 | 0 | 1 |  | 0.597 | 0.613 | 0.628 | V |
| 1 | 1 | 0 | 0 | 0 |  | 0.609 | 0.625 | 0.641 | V |
| 1 | 0 | 1 | 1 | 1 |  | 0.621 | 0.638 | 0.654 | V |
| 1 | 0 | 1 | 1 | 0 |  | 0.633 | 0.650 | 0.667 | V |
| 1 | 0 | 1 | 0 | 1 |  | 0.645 | 0.663 | 0.680 | V |
| 1 | 0 | 1 | 0 | 0 |  | 0.657 | 0.675 | 0.693 | V |
| 1 | 0 | 0 | 1 | 1 |  | 0.670 | 0.688 | 0.705 | V |
| 1 | 0 | 0 | 1 | 0 |  | 0.682 | 0.700 | 0.718 | V |
| 1 | 0 | 0 | 0 | 1 |  | 0.694 | 0.713 | 0.731 | V |
| 1 | 0 | 0 | 0 | 0 |  | 0.706 | 0.725 | 0.744 | V |
| 0 | 1 | 1 | 1 | 1 |  | 0.718 | 0.738 | 0.757 | V |
| 0 | 1 | 1 | 1 | 0 |  | 0.731 | 0.750 | 0.770 | V |
| 0 | 1 | 1 | 0 | 1 |  | 0.743 | 0.763 | 0.782 | V |
| 0 | 1 | 1 | 0 | 0 |  | 0.755 | 0.775 | 0.795 | V |
| 0 | 1 | 0 | 1 | 1 |  | 0.767 | 0.788 | 0.808 | V |
| 0 | 1 | 0 | 1 | 0 |  | 0.779 | 0.800 | 0.821 | V |
| 0 | 1 | 0 | 0 | 1 |  | 0.791 | 0.813 | 0.834 | V |
| 0 | 1 | 0 | 0 | 0 |  | 0.804 | 0.825 | 0.846 | V |
| 0 | 0 | 1 | 1 | 1 |  | 0.816 | 0.838 | 0.859 | V |
| 0 | 0 | 1 | 1 | 0 |  | 0.828 | 0.850 | 0.872 | V |
| 0 | 0 | 1 | 0 | 1 |  | 0.840 | 0.863 | 0.885 | V |
| 0 | 0 | 1 | 0 | 0 |  | 0.852 | 0.875 | 0.898 | V |
| 0 | 0 | 0 | 1 | 1 |  | 0.864 | 0.888 | 0.911 | V |
| 0 | 0 | 0 | 1 | 0 |  | 0.877 | 0.900 | 0.923 | V |
| 0 | 0 | 0 | 0 | 1 |  | 0.889 | 0.913 | 0.936 | V |
| 0 | 0 | 0 | 0 | 0 |  | 0.901 | 0.925 | 0.949 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATEx}}=100 \mathrm{pF}\right.$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SS }}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{V}_{\text {OCSET }}=0.54 \mathrm{~V}$, DAC Code 01110 ; unless otherwise stated. )

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | | Power Good Output | $V_{C C}=14 \mathrm{~V}$, PWRGDS $=1.4 \mathrm{~V}$ | - | 0.1 | 1.0 |
| :--- | :--- | :---: | :---: | :---: |
| Switch Leakage Current | PWRGDS low to PWRGD low | 100 | 500 | 1000 |
| Delay | PWRGDS $=1.0 \mathrm{~V}$, <br> IPWRGD $=4.0 \mathrm{~mA}$ | - | 0.15 | 0.4 |
| Output Low Voltage |  |  |  | V |

## Voltage Feedback Error Amplifier

| $V_{\text {FB }}$ Bias Current | Note 2 | 9.5 | 10 | 10.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Comp Source Current | $\begin{aligned} & \mathrm{COMP}=0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{FB}}=1.8 \mathrm{~V}, \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Comp Sink Current | $\begin{aligned} & \mathrm{COMP}=0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{FB}}=1.15 \mathrm{~V}, \mathrm{DAC}=11110 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$, Note 3 | 200 | 500 | 750 | $\mu \mathrm{mho}$ |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3 | 45 | 95 | - | dB |
| Unity Gain Bandwidth | - | - | 50 | - | kHZ |
| PSRR @ 1.0 kHz | - | - | 60 | - | dB |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=0 \mathrm{~V}$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.6 \mathrm{~V}$ | - | 50 | 150 | mV |

PWM Comparators

| Minimum Pulse Width | Measured from CSx to GATEx, $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=\mathrm{CS} \mathrm{~S}_{\mathrm{REF}}=0.5 \mathrm{~V}, \\ & \mathrm{COMP}=0.5 \mathrm{~V}, \\ & 60 \mathrm{mV} \text { step on } \mathrm{CSx} \end{aligned}$ $\text { measure at GATEx }=1.0 \mathrm{~V}$ | - | 75 | 120 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Transient Response Time | Measured from CS $_{\text {REF }}$ to GATEx, $\begin{aligned} & \mathrm{COMP}=2.1 \mathrm{~V} \\ & \mathrm{CSx}=\mathrm{CS}_{\mathrm{REF}}=0.5 \mathrm{~V} \end{aligned}$ <br> $\mathrm{CS}_{\text {REF }}$ stepped from $1.2 \mathrm{~V}-2.0 \mathrm{~V}$ | - | 40 | 60 | ns |
| Channel Start-Up Offset | $C S x=C S_{R E F}=V_{F B}=0 \mathrm{~V},$ <br> measure $\mathrm{V}_{\mathrm{COMP}}$ when GATEx switch high | 0.4 | 0.6 | 0.8 | V |
| Channel Start-Up Offset Mismatch | $C S x=C S_{R E F}=V_{F B}=0 V,$ <br> measure V (COMP) when GATEx switch high, Note 3 | -5.0 | - | 5.0 | mV |
| Artificial Ramp Amplitude | 50\% Duty Cycle, Note 3 | 120 | 140 | 160 | mV |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of $\mathrm{R}_{\mathrm{OSC}}$ per Figure X .
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATEx}}=100 \mathrm{pF}\right.$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{\text {SS }}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{V}_{\text {OCSET }}=0.54 \mathrm{~V}$, DAC Code 01110 ; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Gates |  |  |  |  |  |
| High Voltage | Measure GATEx <br> $I_{\text {GATEx }}=1.0 \mathrm{~mA}$ | 2.0 | 2.6 | 3.0 | V |
| Low Voltage | Measure GATEx, I IATEx $=1.0 \mathrm{~mA}$ | - | 0.5 | 0.7 | V |
| Rise Time Gate | $0.8 \mathrm{~V}<$ GATEx $<2.0 \mathrm{~V}$, <br> $\mathrm{V}_{\text {CC }}=10 \mathrm{~V}$ | - | 5.0 | 20 | ns |
| Fall Time Gate | $2.0 \mathrm{~V}>$ GATEx $>0.8 \mathrm{~V}$, <br> $\mathrm{V}_{\text {CC }}=10 \mathrm{~V}$ | - | 5.0 | 20 | ns |

## Oscillator

| Switching Frequency | $\mathrm{R}_{\text {OSC }}=32.4 \mathrm{k} \Omega$ | 300 | 400 | 500 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | $\mathrm{R}_{\text {OSC }}=63.4 \mathrm{k} \Omega$, Note 4 | 150 | 200 | 250 | kHz |
| Switching Frequency | $\mathrm{R}_{\text {OSC }}=16.2 \mathrm{k} \Omega$, Note 4 | 600 | 800 | 1000 | kHz |
| Rosc Voltage |  | 0.90 | 1.00 | 1.10 | V |
| Phase Delay | - | 75 | 90 | 105 | deg |

Adaptive Voltage Positioning

| $V_{\text {DRP }}$ Output Voltage to DAC | $\begin{gathered} \mathrm{CSx}=\mathrm{CS}_{\mathrm{REF}}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \\ \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{gathered}$ | -30 | 10 | 60 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum $\mathrm{V}_{\text {DRP }}$ Voltage | $\begin{aligned} & \mathrm{CSx}-\mathrm{CS}_{\mathrm{REF}}=50 \mathrm{mV}, \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | 450 | 600 | 750 | mV |
| Current Sense Input to $V_{\text {DRP }}$ Gain | $\begin{aligned} & C S x-C_{\text {REF }}=50 \mathrm{mV}, \\ & V_{\text {FB }}=C O M P, \\ & \text { Measure } V_{D R P}-C O M P \end{aligned}$ | 2.85 | 3.10 | 3.35 | V/V |
| $\mathrm{V}_{\text {DRP }}$ Source Current Limit | $\begin{aligned} & \text { CSx }- \text { CS }_{\text {REF }}=50 \mathrm{mV} \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \text { Measure } \mathrm{V}_{\mathrm{DRP}}- \\ & \mathrm{COMP} \mathrm{~V}_{\mathrm{DRP}}=1.5 \mathrm{~V} \end{aligned}$ | 1.0 | 7.0 | 14 | mA |

## Soft Start

| SS Source Current | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$, Note 5 | 130 | 160 | 200 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| SS Sink Current | $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$, Note 5 | 4.0 | 5.0 | 6.25 | $\mu \mathrm{~A}$ |
| SS Min Threshold | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | 0.25 | 0.3 | 0.35 | V |
| SS Max Threshold | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | 2.4 | 2.7 | - | V |
| SS Source/Sink Ratio |  | 20 | 32 | 48 | - |
| SS COMP Pull Down Current | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | 200 | 900 | 2100 | $\mu \mathrm{~A}$ |

Current Sense Amplifiers

| CS $_{\text {REF }}$ Input Bias Current | CS $_{\text {REF }}=$ CSX = 0 V | - | 3.4 | 4.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| CSx Input Bias Current | CS $_{\text {REF }}=\mathrm{CSx}=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| Sense Amp Gain | $\mathrm{CS}_{\text {REF }}=0 \mathrm{~V}, \mathrm{CSx}=0.05 \mathrm{~V}$, <br> Measure V(COMP) when GATEx <br> switches high | 2.85 | 3.10 | 3.35 | $\mathrm{~V} / \mathrm{V}$ |
| Mismatch | - | -3.0 | - | 3.0 | mV |
| Common Mode Input Range | Note 4 | 0 | - | 2.0 | V |
| Bandwidth | - | - | 7.0 | - | MHz |

4. Guaranteed by design. Not tested in production.
5. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of $\mathrm{R}_{\mathrm{OSC}}$ per Figure X .

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V}\right.$; $\mathrm{C}_{\text {GATEx }}=100 \mathrm{pF}$, $\mathrm{C}_{\text {COMP }}=0.01 \mu \mathrm{~F}, \mathrm{C}_{S S}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k} \Omega, \mathrm{V}_{\text {OCSET }}=0.54 \mathrm{~V}$, DAC Code 01110 ; unless otherwise stated. )

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Current Sense Amplifiers |  |  |  |  |  |
| Single Phase Pulse by Pulse Current Limit | $\begin{aligned} & \mathrm{V}_{\mathrm{FB}}=C S_{\text {REF }}=0.5 \mathrm{~V}, C O M P=2.0 \\ & \mathrm{~V}, \text { Measure } \mathrm{CSx}-\mathrm{CS} \text { REF when } \\ & \text { GATEx goes low } \end{aligned}$ | 75 | 83 | 91 | mV |
| OCSET Input Bias Current | OCSET $=0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Current Sense Input to OCSET Gain | OCSET/(CSx-CS REF , 0.25 V < OCSET < 0.6 V, GATEx not switching | 2.85 | 3.10 | 3.35 | V/V |
| Current Limit Filter Slew Rate | $C_{\text {REF }}=1.1 \mathrm{~V}, \mathrm{CSx}=1.0 \mathrm{~V}$, pulse CSx to 1.16 V | 2.0 | 5.0 | 13 | $\mathrm{mV} / \mu \mathrm{s}$ |

## General Electrical Specification

| $\mathrm{V}_{\text {CC }}$ Operating Current | COMP $=0.3 \mathrm{~V}$ (no switching) | - | 20 | 30 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| UVLO Start Threshold | SS Charging Gates Switching | 8.5 | 9.0 | 9.5 | V |
| UVLO Stop Threshold | Gates not switching, SS \& COMP <br> discharging | 7.5 | 8.0 | 8.5 | V |
| UVLO Hysteresis | Start-Stop | 0.8 | 1.0 | 1.2 | V |

## PACKAGE PIN DESCRIPTION

| Pin Number |  |  |  |
| :---: | :---: | :---: | :---: |
| SO-24L | Pin Symbol | Pin Name | Function |
| 1 | GND | Ground | IC power supply return. Connected to IC substrate. |
| 2 | OCSET | Overcurrent Set | Resistor divider from Rosc to GND. Programs the threshold of the hiccup overcurrent protection. |
| 3 | Rosc | Oscillator Frequency Adjust | Rosc is a regulated 1.0 V output and programs the oscillator frequency with a resistor to GND. |
| 4-7 | CS1-CS4 | Current Sense Inputs | Non-inverting inputs to the current sense amplifiers. |
| 8 | $\mathrm{CS}_{\text {REF }}$ | Current Sense Reference | Inverting input to the current sense amplifiers and reference for Power Good. |
| 9 | $V_{\text {DRP }}$ | Current Sense Amp Output | Compensates for IR droop. A resistor from $V_{\text {DRP }}$ to FB programs the amount of Adaptive Voltage Positioning. Omitting this resistor defeats the AVP function. |
| 10 | $V_{F B}$ | Voltage Feedback | Error Amplitude inverting input. Input bias current is used to program AVP light load offset via a resistor connected to the converter output voltage. |
| 11 | COMP | Error Amp Output and PWM Comparator Input | Provides loop compensation and is clamped by SS. |
| 12 | SS | Soft Start | Controls fault timing and startup. |
| 13 | PWRGD | Power Good Output | Open collector output, which is "low" when the converter output is out of regulation. |
| 14 | PWRGDS | Power Good Sense | A resistor divider from VOUT to GND programs the Power Good lower threshold. |
| 15-19 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID }}$ | DAC $V_{\text {ID }}$ Inputs | TTL compatible logic input used to program the converter output voltage. Internal 50 k pull-up resistors are provided to 3.3 V . All high generates fault. |
| 20-23 | GATE4-1 | Channel Outputs | PWM outputs to drive FET driver IC. |
| 24 | $\mathrm{V}_{\mathrm{CC}}$ | Supply Input | IC bias input. |



## APPLICATIONS INFORMATION

## Overview

The CS5307 DC/DC controller from ON Semiconductor was developed using the Enhanced $\mathrm{V}^{2}$ topology to meet requirements of low voltage, high current loads with fast transient requirements. Enhanced $V^{2}$ combines the original $\mathrm{V}^{2}$ topology with peak current-mode control for fast transient response and current sensing capability. The addition of an internal PWM ramp and implementation of fast-feedback directly from Vcore has improved transient response and simplified design. The CS5307 includes Power Good (PWRGD), providing a highly integrated solution to simplify design, minimize circuit board area, and reduce overall system cost.

Two advantages of a multi-phase converter over a single-phase converter are current sharing and increased apparent output frequency. Current sharing allows the designer to use less inductance in each phase than would be required in a single-phase converter. The smaller inductor will produce larger ripple currents but the total per phase power dissipation is reduced because the RMS current is lower. Transient response is improved because the control loop will measure and adjust the current faster in a smaller output inductor. Increased apparent output frequency is desirable because the off- time and the ripple voltage of the two-phase converter will be less than that of a single-phase converter.

## Fixed Frequency Multi-Phase Control

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5307 controller uses four-phase, fixed-frequency, Enhanced $\mathrm{V}^{2}$ architecture to measure and control currents in
individual phases. Each phase is delayed $90^{\circ}$ from the previous phase. Normally, GATEx transitions to a high voltage at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring GATEx low. Once GATEx goes low, it will remain low until the beginning of the next oscillator cycle. While GATEx is high, the Enhanced V ${ }^{2}$ loop will respond to line and load variations. On the other hand, once GATEx is low, the loop can not respond until the beginning of the next PWM cycle. Therefore, constant frequency Enhanced $V^{2}$ will typically respond to disturbances within the off-time of the converter.
The Enhanced $V^{2}$ architecture measures and adjusts the output current in each phase. An additional input (CSx) for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 3. The triangular inductor current is measured differentially across RS, amplified by CSA and summed with the Channel Startup Offset, the Internal Ramp, and the Output Voltage at the non-inverting input of the PWM comparator. The purpose of the Internal Ramp is to compensate for propagation delays in the CS5307. This provides greater design flexibility by allowing smaller external ramps, lower minimum pulse widths, higher frequency operation, and PWM duty cycles above $50 \%$ without external slope compensation. As the sum of the inductor current and the internal ramp increase, the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts a cycle with higher current, the PWM cycle will terminate earlier providing negative feedback. The CS5307 provides a CSx input for each phase, but the $\mathrm{CS}_{\text {REF }}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same CS $_{\text {REF }}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than a phase with a smaller current signal.


Figure 3. Enhanced V ${ }^{2}$ Control Employing Resistive Current Sensing and Additional Internal Ramp

Enhanced $\mathrm{V}^{2}$ responds to disturbances in $\mathrm{V}_{\text {CORE }}$ by employing both "slow" and "fast" voltage regulation. The internal error amplifier performs the slow regulation. Depending on the gain and frequency compensation set by the amplifier's external components, the error amplifier will typically begin to ramp its output to react to changes in the output voltage in 1-2 PWM cycles. Fast voltage feedback is implemented by a direct connection from Vcore to the non-inverting pin of the PWM comparator via the summation with the inductor current, internal ramp, and Offset. A rapid increase in output current will produce a negative offset at Vcore and at the output of the summer. This will cause the PWM duty cycle to increase almost instantly. Fast feedback will typically adjust the PWM duty-cycle in 1 PWM cycle.
As shown in Figure 3, an internal ramp (nominally 90 mV at a $50 \%$ duty cycle) is added to the inductor current ramp at the positive terminal of the PWM comparator. This additional ramp compensates for propagation time delays from the current sense amplifier (CSA), the PWM comparator, and the MOSFET gate drivers. As a result, the minimum ON time of the controller is reduced and lower duty-cycles may be achieved at higher frequencies. Also, the additional ramp reduces the reliance on the inductor current ramp and allows greater flexibility when choosing the output inductor and the $\mathrm{R}_{\mathrm{CSx}} \mathrm{C}_{\mathrm{CSx}}$ time constant of the feedback components from $\mathrm{V}_{\text {CORE }}$ to the CSn pin.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be:

$$
\begin{aligned}
\text { VCOMP }= & \text { VOUT @ } 0 \text { A + Channel_Startup_Offset } \\
& + \text { Int_Ramp }+ \text { GCSA } \cdot \text { Ext_Ramp } / 2
\end{aligned}
$$

Int_Ramp is the "partial" internal ramp value at the corresponding duty cycle, Ext_Ramp is the peak-to-peak external steady-state ramp at 0 A, $\mathrm{G}_{\mathrm{CSA}}$ is the Current Sense Amplifier Gain (nominally 3 V/V), and the Channel Startup Offset is typically 0.60 V . The magnitude of the Ext_Ramp can be calculated from:

$$
\text { Ext_Ramp }=\mathrm{D} \cdot\left(\mathrm{~V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) /\left(\mathrm{RCSn}^{2} \cdot \mathrm{CCSn} \cdot \mathrm{fSW}\right)
$$

For example, if $\mathrm{V}_{\text {Out }}$ at 0 A is set to 1.700 V with AVP and the input voltage is 12.0 V , the duty cycle ( D ) will be $1.700 / 12.0$ or $14.2 \%$. Int_Ramp will be $90 \mathrm{mV} / 50 \bullet 14.2 \%$ $=26 \mathrm{mV}$. Realistic values for $\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}$ and $\mathrm{f}_{\mathrm{Sw}}$ are $10 \mathrm{k} \Omega$, $0.015 \mu \mathrm{~F}$, and 650 kHz - using these and the previously mentioned formula, Ext_Ramp will be 15.0 mV .

$$
\begin{aligned}
\mathrm{V} \text { COMP }= & 1.700 \mathrm{~V}+0.60 \mathrm{~V}+26 \mathrm{mV} \\
& +3 \mathrm{~V} / \mathrm{V} \cdot 15.0 \mathrm{mV} / 2 \\
= & 2.348 \mathrm{Vdc}
\end{aligned}
$$

If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current
changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as:

$$
\Delta \mathrm{V}=\mathrm{RS} \cdot \mathrm{GCSA} \cdot \Delta \mathrm{I} \mathrm{OUT}
$$

The single-phase power stage output impedance is:

$$
\text { Single Stage Impedance }=\Delta \mathrm{V}_{\mathrm{OUT}} / \Delta \mathrm{I} \mathrm{OUT}=\mathrm{RS} \cdot \mathrm{GCSA}
$$

The total output impedance will be the single stage impedance divided by 4 .

The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few microseconds of a transient before the feedback loop has repositioned the COMP pin.

The peak output current can be calculated from:


Figure 4. Open Loop Operation
Figure 4 shows the step response of the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides a portion of the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current ramp, the "partial" internal ramp voltage signal and Offset exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T 2 . After T 2 the output voltage remains lower than at light load and the average current signal level (CSx output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 5. Enhanced ${ }^{2}$ Control Employing Lossless Inductive Current Sensing and Internal Ramp

## Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 5. In the diagram, L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal, the values of $\mathrm{R}_{\mathrm{CSx}}$ and $\mathrm{C}_{\mathrm{CSx}}$ are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$. If this criteria is met, the current sense signal will be the same shape as the inductor current and the voltage signal at CSx will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value $\mathrm{R}_{\mathrm{L}}$ was used as a sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$.

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be considered when setting the OCSET threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 3.

## Current Sharing Accuracy

Printed circuit board (PCB) traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at relatively the same point for each phase and the connection to the $\mathrm{CS}_{\mathrm{REF}}$ pin should be made so that no phase is favored. In some cases, especially with inductive sensing, resistance of the PCB can be useful for increasing the current sense resistance. The total current sense resistance used for calculations must include any PCB trace resistance between the CSx input and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case Current Sense Amplifier input mismatch is $\pm 5.0 \mathrm{mV}$ and will typically be within 3.0 mV . The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance a 3.0 mV mismatch with a $2.0 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## External Ramp Size and Current Sensing

The internal ramp allows flexibility of current sense time constant. Typically, the current sense $\mathrm{R}_{\mathrm{CSx}} \mathrm{C}_{\mathrm{CSx}}$ time constant should be equal to or slightly slower than the inductor's time constant. If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC or transient portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R}_{\mathrm{CSx}} \bullet \mathrm{C}_{\mathrm{CSx}}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R}_{\mathrm{CSx}} \bullet \mathrm{C}_{\mathrm{CSx}}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During a positive current transient, the COMP pin will be required to undershoot in response to the current signal in order to maintain the output voltage. Similarly, the $\mathrm{V}_{\text {DRP }}$ signal will overshoot which will produce too much transient droop in the output voltage. The single phase pulse-by-pulse overcurrent protection will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rising step loads than for slowly rising output currents.
The waveforms in Figure 6 show a simulation of the current sense signal and the actual inductor current during a
positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}, \mathrm{R}_{\mathrm{L}}$ $=1.6 \mathrm{~m} \Omega, \mathrm{R}_{\mathrm{CSx}}=20 \mathrm{k}$ and $\mathrm{C}_{\mathrm{CSx}}=.01 \mu \mathrm{~F}$. In this case, ideal current signal compensation would require $\mathrm{R}_{\mathrm{CSx}}$ to be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu \mathrm{~s}$ time constant. With this compensation the OCSET pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 6. Inductive Sensing Waveform During a Load Step with Fast RC Time Constant ( $50 \mu \mathrm{~s} / \mathrm{div}$ )

## Transient Response and Adaptive Voltage Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is applied. Similarly, the output voltage can be set lower than nominal during heavy loads to reduce overshoot when the load current is removed. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example, in a 50 A converter a $1 \mathrm{~m} \Omega$ resistor would provide a 50 mV change in output voltage between no load and full load and would dissipate 2.5 W .
Lossless adaptive voltage positioning (AVP) is an alternative to using a droop resistor, but it must respond to changes in load current. Figure 7 shows how AVP works. The waveform labeled normal shows a converter without AVP. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) AVP the peak to peak
excursions are cut in half. In the slow AVP waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 7. Adaptive Voltage Positioning
The controller can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram in Figure 1). To set the no-load positioning, a resistor is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to adjust the no-load output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of $\mathrm{R}_{\mathrm{OSC}}$ as shown in the datasheets.

During no load conditions the $\mathrm{V}_{\mathrm{DRP}}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor. When output current increases the $V_{\text {DRP }}$ pin increases proportionally and the $V_{\text {DRP }}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to decrease.

The response during the first few microseconds of a load transient are controlled primarily by power stage output impedance and the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced $\mathrm{V}^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 40 ns , causing the GATEx output to shut OFF. The (external) MOSFET driver should react normally to turn off the top MOSFET and turn on the bottom MOSFET. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Power Good

According to the latest specifications, the Power Good (PWRGD) signal must be asserted when the output voltage is within a window defined by the VID code, as shown in Figure 8.


Figure 8. PWRGD Assertion Window
The PWRGDS pin is provided to allow the PWRGD comparators to accurately sense the output voltage. The effect of the PWRGD lower threshold can be modified using a resistor divider from the output to PWRGDS to ground, as shown in Figure 9, below.


Figure 9. Adjusting the PWRGD Threshold
Since the internally set thresholds for PWRGDS are VID/2 for the lower threshold and a fixed 1.975V for the upper threshold, a simple equation can be provided to assist the designer in selecting a resistor divider to provide the desired PWRGD performance.

$$
\begin{aligned}
& V_{\text {LOWER }}=\frac{V_{V I D}}{2} \cdot \frac{R_{1}+R_{2}}{R_{1}} \\
& V_{\text {UPPER }}=1.975 \mathrm{~V}
\end{aligned}
$$

The logic circuitry inside the chip sets PWRGD low only after a delay period has been passed. A "power bad" event does not cause PWRGD to go low unless it is sustained through the delay time of $500 \mu \mathrm{~s}$. If the anomaly disappears before the end of the delay, the PWRGD output will never be set low.

In order to use the PWRGD pin as specified, the user is advised to connect external resistors as necessary to limit the current into this pin to 4 mA or less.

## Undervoltage Lockout

The CS5307 includes an undervoltage lockout circuit. This circuit keeps the IC's output drivers low until $\mathrm{V}_{\mathrm{CC}}$ applied to the IC reaches 9 V . The GATE outputs are disabled when $\mathrm{V}_{\mathrm{CC}}$ drops below 8 V .

## Soft Start and Hiccup Mode

At initial power-up, both SS and COMP voltages are zero. The total SS capacitance will begin to charge with a current of $160 \mu \mathrm{~A}$. The error amplifier directly charges the COMP capacitance. An internal clamp ensures that the COMP pin voltage will always be less than the voltage at the SS pin, ensuring proper start-up behavior. All GATE outputs are held low until the COMP voltage reaches 0.6 V . Once this threshold is reached, the GATE outputs are released to operate normally. In hiccup-mode, the internal fault latch will initiate a $5 \mu \mathrm{~A}$ discharge current on the SS pin, and the internal clamp will discharge the capacitor connected to the COMP pin at a similar rate. This performance will result in GATE pulses being generated until the overcurrent condition reoccurs, and the discharge/soft start cycle begins anew.

## Current Limit

Two levels of over-current protection are provided. First, if the voltage on the Current Sense pins (either CS1 or CS2) exceeds $\mathrm{CS}_{\text {REF }}$ by more than a fixed threshold (Single Pulse Current Limit), the PWM comparator is turned off. This provides fast peak current protection for individual phases. Second, the individual phase currents are summed and low-pass filtered to compare an averaged current signal to a user adjustable voltage on the OCSET pin. If the OCSET voltage is exceeded, the fault latch trips and the Soft Start capacitor discharges until the Soft Start pin reaches 0.3 V . Then Soft Start begins. The converter will continue to operate in a low current hiccup mode until the fault condition is corrected.

## Fault Protection Logic

The CS5307 includes fault protection circuitry to prevent harmful modes of operation from occurring. The fault logic is described in Table 1.

Table 1. Fault Protection Logic

| Fault Modes | Stop Switching | SS Pin Characteristics | Reset Method |
| :--- | :---: | :---: | :---: |
| Undervoltage Lockout | Yes | $-5.0 \mu \mathrm{~A}$ | SS $<0.3 \mathrm{~V}$ |
| VID-11111 | Yes | $-5.0 \mu \mathrm{~A}$ | Change VID Code |
| Phase Over Current <br> $(0.33 ~ V ~ L i m i t) ~$ | No | Not Affected | Automatic |

## Gate Outputs

The CS5307 is designed to operate with external gate drivers. Accordingly, the gate outputs are capable of driving a 100 pF load with typical rise and fall times of 15 ns .

## Digital to Analog Converter (DAC)

The output voltage of the CS5307 is set by means of a 5 -bit, $1 \%$ DAC. The DAC pins are internally pulled up to a 3.3 V rail through a blocking diode and a set of $50 \mathrm{k} \Omega$ resistors. The blocking diode allows external pull up to a bias voltage greater than 3.3 V and less than 13 V .

The output of the DAC is described in the Electrical Characteristics section of the data sheet. These outputs are
consistent with the latest VRM and processor specifications. The DAC output is equal to the VID code specification.

In order to produce a workable power supply using the CS5307, the designer is expected to use AVP as described earlier to position the output voltage above the DAC output, resulting in an output voltage somewhere in the middle of the acceptable range.

The latest VRM and processor specifications require a power supply to turn its output off in the event of a 11111 VID code. When the DAC sees such a code, the GATE pins stop switching and go low. This condition is described in Table 1.

## CS5308

## Two－Phase PWM Controller with Integrated Gate Drivers for VRM 8.5

The CS5308 is a second－generation，two－phase step down controller that incorporates all control functions required to power next generation processors．Proprietary multi－phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications．Enhanced V ${ }^{2 \mathrm{TM}}$ control architecture provides the fastest possible transient response，excellent overall regulation，and ease of use．The CS5308 is a second generation PWM controller because it optimizes transient response by combining traditional Enhanced $\mathrm{V}^{2}$ with an internal PWM ramp and fast－feedback directly from $\mathrm{V}_{\text {CORE }}$ to the internal PWM comparator． These enhancements provide greater design flexibility，facilitate use and reduce output voltage jitter．

The multi－phase architecture reduces input and output filter ripple， allowing for a significant reduction in filter size and inductor values with a corresponding increase in the output inductor current slew rate． This approach allows a considerable reduction in input and output capacitor requirements，as well as reducing overall solution size and cost．

The CS5308 includes VTT monitoring and timing，VTT Power Good（VTT ${ }_{\text {PGD }}$ ），Power Good（PWRGD），and internal MOSFET gate drivers to provide a＂fully integrated solution＂to simplify design， minimize circuit board area，and reduce overall system cost．

## Features

－Enhanced $V^{2}$ Control Method
－Internal PWM Ramp
－Fast－Feedback Directly from $V_{\text {CORE }}$
－5－Bit DAC with $1 \%$ Tolerance
－Adjustable Output Voltage Positioning
－ 200 kHz to 800 kHz Operation Set by Resistor
－Current Sensed through Sense Resistors or Output Inductors
－Adjustable Hiccup Mode Current Limit
－Overvoltage Protection through Synchronous MOSFETs
－Individual Current Limits for Each Phase
－On－Board Current Share Amplifiers
－ $3.3 \mathrm{~V}, 1.0 \mathrm{~mA}$ Reference Output
－VTT Monitoring and VTT Power Good（VTT ${ }_{\text {PGD }}$ ）
－V CORE Power Good
－On／Off Control（through COMP Pin）
－Improved Noise Immunity

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PIN CONNECTIONS

| － 1 |  | 28 |
| :---: | :---: | :---: |
| COMP | O | ${ }^{28} \mathrm{R}_{\text {OSC }}$ |
| $\mathrm{V}_{\text {FB }}$ 罒 |  | $\square$ LGND |
| $V_{\text {DRP }}$ 吅 |  | $\boxplus \mathrm{V}_{\text {CCL }}$ |
| REF $\square^{-1}$ |  | $\square \mathrm{V}_{\mathrm{CCH} 1}$ |
| $\mathrm{l}_{\text {LIM }}$ 피 |  | $\square$ GATE（H）1 |
|  |  | $\square$ GATE（L）1 |
| VID0 ${ }^{\text {d }}$ |  | $\square$ PGND |
| $V_{\text {ID1 }}$［1］ |  | $\square \mathrm{V}_{\text {CCL12 }}$ |
| $V_{\text {ID2 }}$－ |  | $\square$ GATE（L）2 |
| $V_{\text {ID3 }}$ ■ |  | $\multimap$ GATE（H）2 |
| PWRGD ${ }^{\text {－}}$ |  | $\square \mathrm{V}_{\mathrm{CCH} 2}$ |
| $C S_{\text {REF }}$ 回 |  | $\square \mathrm{VTT}_{\mathrm{PGD}}$ |
| CS1 $\square^{-1}$ |  | $\sim_{\text {VTT }}^{\text {CT }}$ |
| CS2 |  | $\square$ VTT |

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5308GDW28 | SO－28L | 27 Units／Rail |
| CS5308GDWR28 | SO－28L | 1000 Tape \＆Reel |
| XC5308GDW28 | SO－28L | 27 Units／Rail |
| XC5308GDWR28 | SO－28L | 1000 Tape \＆Reel |



Recommended Components:
L1: Coiltronics CTX15-14771 or T30-26 core with 3T of \#16 AWG
L2: Coiltronics CTX22-15401 X1 or T50-52 with 5T of \#16 AWG Bifilar
$\mathrm{C}_{\text {INPUT: }} 2 \times$ Sanyo Oscon 6SP680M ( $680 \mu \mathrm{~F}, 6.3 \mathrm{~V}$ )
Cout: $7 \times$ Rubycon 6.3ZA1000M10x16 ( $1000 \mu \mathrm{~F}, 6.3 \mathrm{~V}$ )
$\mathrm{C}_{\text {CERAMICs: }} 12 \times$ Panasonic ECJ-3YBOJ106K ( $10 \mu \mathrm{~F}, 6.3 \mathrm{~V}$ )
Q1-Q4: ON Semiconductor NTB85N03 (28 V, 85 A)
Figure 1. Application Diagram. 5.0 V to 1.7 V at $28 \mathrm{~A}, 335 \mathrm{kHz}$ with 12 V Bias for Pentium ${ }^{\circledR}$ III Applications

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance Junction-to-Case, R RJC Junction-to-Ambient, R $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{aligned} & 15 \\ & 75 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| JEDEC Moisture Sensitivity |  | Level 2 | - |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Name | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | Isink |
| :---: | :---: | :---: | :---: | :---: |
| COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $V_{\text {FB }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $V_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| CS1-CS2 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $\mathrm{CS}_{\text {REF }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| PWRGD | 6.0 V | -0.3 V | 1.0 mA | 8.0 mA |
| VID Pins | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| ILIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| REF | 6.0 V | -0.3 V | 1.0 mA | 20 mA |
| VTT | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $\mathrm{VTT}_{C T}$ | 6.0 V | -0.3 V | 1.0 mA | 40 mA |
| $\mathrm{VTT}_{\text {PGD }}$ | 6.0 V | -0.3 V | 1.0 mA | 8.0 mA |
| $\mathrm{V}_{\text {CCHx }}$ | 20 V | -0.3 V | N/A | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC |
| GATE(H)x | 20 V | -0.3 V DC <br> -2.0 V for 100 ns | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mADC |
| GATE(L)x | 16 V | $\begin{aligned} & -0.3 \mathrm{~V} \mathrm{DC} \\ & -2.0 \mathrm{~V} \text { for } 100 \mathrm{~ns} \end{aligned}$ | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC | $1.5 \mathrm{~A} \text { for } 1.0 \mu \mathrm{~s} \text {, }$ 200 mADC |
| $\mathrm{V}_{\text {CCL12 }}$ | 16 V | -0.3 V | N/A | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC |
| PGND | 0.3 V | -0.3 V | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| LGND | 0 V | 0 V | 50 mA | N/A |
| $\mathrm{V}_{\text {CCL }}$ | 16 V | -0.3 V | N/A | 50 mA |
| Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH} 1}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V}\right.$;
$4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CCL} 12}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code 01000 ( 1.65 V ),
$\mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC

| Accuracy (all codes) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ | - | - | $\pm 1.0$ | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {ID25 }}$ | VID3 | $V_{\text {ID } 2}$ | $\mathrm{V}_{\text {ID } 1}$ | VIDO | - | - | - | - | - |
| 0 | 0 | 1 | 0 | 0 | - | 1.039 | 1.050 | 1.061 | V |
| 1 | 0 | 1 | 0 | 0 | - | 1.064 | 1.075 | 1.086 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.089 | 1.100 | 1.111 | V |
| 1 | 0 | 0 | 1 | 1 | - | 1.114 | 1.125 | 1.136 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.139 | 1.150 | 1.162 | V |
| 1 | 0 | 0 | 1 | 0 | - | 1.163 | 1.175 | 1.187 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.188 | 1.200 | 1.212 | V |
| 1 | 0 | 0 | 0 | 1 | - | 1.213 | 1.225 | 1.237 | V |
| 0 | 0 | 0 | 0 | 0 | - | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 0 | 0 | 0 | - | 1.262 | 1.275 | 1.288 | V |
| 0 | 1 | 1 | 1 | 1 | - | 1.287 | 1.300 | 1.313 | V |
| 1 | 1 | 1 | 1 | 1 | - | 1.312 | 1.325 | 1.338 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.337 | 1.350 | 1.364 | V |
| 1 | 1 | 1 | 1 | 0 | - | 1.361 | 1.375 | 1.389 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.386 | 1.400 | 1.414 | V |
| 1 | 1 | 1 | 0 | 1 | - | 1.411 | 1.425 | 1.439 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.436 | 1.450 | 1.465 | V |
| 1 | 1 | 1 | 0 | 0 | - | 1.460 | 1.475 | 1.490 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.485 | 1.500 | 1.515 | V |
| 1 | 1 | 0 | 1 | 1 | - | 1.510 | 1.525 | 1.540 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.535 | 1.550 | 1.566 | V |
| 1 | 1 | 0 | 1 | 0 | - | 1.559 | 1.575 | 1.591 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.584 | 1.600 | 1.616 | V |
| 1 | 1 | 0 | 0 | 1 | - | 1.609 | 1.625 | 1.641 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.634 | 1.650 | 1.667 | V |
| 1 | 1 | 0 | 0 | 0 | - | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.683 | 1.700 | 1.717 | V |
| 1 | 0 | 1 | 1 | 1 | - | 1.708 | 1.725 | 1.742 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.733 | 1.750 | 1.768 | V |
| 1 | 0 | 1 | 1 | 0 | - | 1.757 | 1.775 | 1.793 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.782 | 1.800 | 1.818 | V |
| 1 | 0 | 1 | 0 | 1 | - | 1.807 | 1.825 | 1.843 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID25 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 1.00 | 1.25 | 1.5 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID25 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 25 | 50 | 100 | k $\Omega$ |
| Pull-up Voltage |  |  |  |  | - | 3.15 | 3.3 | 3.45 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH} 1}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V}\right.$; $4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CCL} 12}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code 01000 ( 1.65 V ), $\mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output |  |  |  |  |  |
| Power Good Fault Delay | $C S_{\text {REF }}=$ DAC to DAC $\pm 15 \%$ | 25 | 50 | 100 | $\mu \mathrm{s}$ |
| PWRGD Low Voltage | $\mathrm{I}_{\text {PWRGD }}=4.0 \mathrm{~mA}$ | - | 250 | 400 | mV |
| Output Leakage Current | $\mathrm{V}_{\text {PWRGD }}=5.5 \mathrm{~V}$ | - | 0.1 | 10 | $\mu \mathrm{A}$ |
| Lower Threshold | - | -15 | -12 | -9.0 | \% |
| Upper Threshold | - | 9.0 | 12 | 15 | \% |

## Voltage Feedback Error Amplifier

| $V_{\text {FB }}$ Bias Current, (Note 2.) | $0.9 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.9 \mathrm{~V}$ | 9.4 | 10.3 | 11.1 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | COMP $=0.5 \mathrm{~V}$ to 2.0 V ; $\mathrm{V}_{\mathrm{FB}}=1.6 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | COMP $=0.5 \mathrm{~V}$ to 2.0 V ; $\mathrm{V}_{\text {FB }}=1.7 \mathrm{~V}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Discharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3. | 60 | 90 | - | dB |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ | - | 400 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=1.6 \mathrm{~V}$ COMP Open | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.7 \mathrm{~V}$ COMP Open | - | 0.1 | 0.2 | V |
| Hiccup Latch Discharge Current | - | 2.0 | 5.0 | 10 | $\mu \mathrm{A}$ |
| COMP Discharge Ratio | - | 4.0 | 6.0 | 10 | - |

PWM Comparators

| Minimum Pulse Width | $\mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}$ REF | - | 350 | 475 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Channel Startup Offset | $\mathrm{V}(\mathrm{CS} 1)=\mathrm{V}(\mathrm{CS} 2)=\mathrm{V}\left(\mathrm{V}_{\mathrm{FB}}\right)=$ <br> $\mathrm{V}(\mathrm{CS}(\mathrm{REF})=0 \mathrm{~V} ;$ <br> Measure $\mathrm{V}(\mathrm{COMP})$ when <br> GATE $(\mathrm{H}) 1,2$ switch high | 0.3 | 0.4 | 0.5 | V |
|  |  |  |  |  |  |

## VTT Power Good

| VTT Threshold | - | 1.03 | 1.05 | 1.07 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VTT PGD Low Voltage | $\mathrm{I}_{\mathrm{VTTPGD}}=4.0 \mathrm{~mA}$ | - | 0.25 | 0.4 | V |
| VTT ${ }_{\text {PGD }}$ Leakage Current | $\mathrm{VTT}_{\mathrm{PGD}}=5.5 \mathrm{~V}$ | - | 0.1 | 10 | $\mu \mathrm{A}$ |
| $V_{T T}{ }_{\text {CT }}$ Threshold Voltage | - | 1.0 | 1.05 | 1.10 | V |
| VTT $_{\text {CT }}$ Charge Current | Note 2. | 15 | 30 | 45 | $\mu \mathrm{A}$ |
| $\mathrm{VTT}_{\text {CT }}$ Discharge Threshold | - | 0.24 | 0.32 | 0.38 | V |

## GATES

| High Voltage (AC) | Measure VCCx - GATEx, Note 3. | - | 0 | 1.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Measure GATEx, Note 3. | - | 0 | 0.5 | V |
| Rise Time GATEx | $1.0 \mathrm{~V}<\mathrm{GATE}<8.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CCx}}=10 \mathrm{~V}$ | - | 35 | 80 | ns |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current and VTT ${ }_{\text {CT }}$ Charge Currents change with the value of Rosc per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH} 1}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V}\right.$; $4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CCL} 12}<14 \mathrm{~V}$; $\mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $01000(1.65 \mathrm{~V})$, $\mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATES |  |  |  |  |  |
| Fall Time GATEx | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V} ; \mathrm{V}_{C C x}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| GATE(H)x to GATE(L)x Delay | $\begin{aligned} & \operatorname{GATE}(H) x<2.0 \mathrm{~V}, \\ & \operatorname{GATE}(\mathrm{~L}) \mathrm{x} \end{aligned}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE(L)x to GATE(H)x Delay | $\begin{aligned} & \text { GATE(L)x }<2.0 \mathrm{~V}, \\ & \text { GATE(H)x }>2.0 \mathrm{~V} \end{aligned}$ | 30 | 65 | 110 | ns |
| GATE Pull-down | Force $100 \mu \mathrm{~A}$ into Gate with no power applied to $\mathrm{V}_{\mathrm{CCHx}}$ and $\mathrm{V}_{\mathrm{CCLx}}=2.0 \mathrm{~V}$ | - | 1.2 | 1.6 | V |

## Oscillator

| Switching Frequency | $R_{\text {OSC }}=32.4 \mathrm{k}$ | 340 | 400 | 460 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | $\mathrm{R}_{\text {OSC }}=63.4 \mathrm{k}$, Note 4. | 150 | 200 | 250 | kHz |
| Switching Frequency | R OSC $=16.2 \mathrm{k}$, Note 4. | 600 | 800 | 1000 | kHz |
| R OSC Voltage | - | - | 1.0 | - | V |
| Phase Delay | Rising edge only | 165 | 180 | 195 | deg |

Adaptive Voltage Positioning

| V ${ }_{\text {DRP }}$ Offset | $\begin{aligned} & \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\mathrm{REF}}, \mathrm{~V}_{\mathrm{FB}}= \\ & \mathrm{COMP}, \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | -15 | - | 15 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DRP }}$ Operating Voltage Range | Measure V ${ }_{\text {DRP }}$ - GND, Note 4. | 0.1 | - | 2.3 | V |
| Maximum V ${ }_{\text {DRP }}$ Voltage | $\begin{aligned} & (\mathrm{CS1}=\mathrm{CS} 2)-\mathrm{CS}_{\mathrm{REF}}=50 \mathrm{mV} \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP} \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | 260 | 320 | 400 | mV |
| Current Share Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.6 | 3.2 | 4.0 | V/V |

Current Sensing and Sharing

| CS1 - CS2 Input Bias Current | $\mathrm{V}(\mathrm{Cx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.1 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS ${ }_{\text {REF }}$ Input Bias Current | - | - | 0.5 | 2.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifier Gain | - | 3.05 | 3.50 | 3.95 | V/v |
| Current Sense Amp Mismatch (The sum of gain and offset errors.) | $\begin{aligned} & 0<\text { CSx }- \text { CS }_{\text {REF }}<50 \mathrm{mV} \text {. } \\ & \text { Note } 4 . \end{aligned}$ | -5.0 | - | 5.0 | mV |
| Current Sense Input to LIIM Gain | $\mathrm{LIIM}=1.0 \mathrm{~V}$ | 5.5 | 6.5 | 7.5 | $\mathrm{V} / \mathrm{V}$ |
| Current Limit Filter Slew Rate | Note 4. | 7.5 | 15 | 40 | $\mathrm{mV} / \mu \mathrm{s}$ |
| $\mathrm{I}_{\text {LIM }}$ Operating Voltage Range | Note 4. | 0.1 | - | 1.3 | V |
| ILIM Bias Current | $0 \mathrm{~V}<\mathrm{I}_{\text {LIM }}<1.0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse by Pulse Current Limit: $\mathrm{V}(\mathrm{Cx})-\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)$ | - | 90 | 105 | 135 | mV |
| Current Sense Amplifier Bandwidth | Note 4. | 1.0 | - | - | MHz |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH} 1}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V}\right.$; $4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CCL} 12}<14 \mathrm{~V}$; $\mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{ROSC}}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $01000(1.65 \mathrm{~V})$, $\mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| General Electrical Specifications |  |  |  |  |  |
| $\mathrm{V}_{\text {CCL }}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 20.5 | 26.0 | mA |
| $\mathrm{V}_{\text {CCL12 }}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 8.0 | 11 | mA |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 2.8 | 4.0 | mA |
| $\mathrm{V}_{\mathrm{CCH} 2}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 2.5 | 3.5 | mA |
| $\mathrm{V}_{\text {CCL }}$ Start Threshold | GATEs switching, COMP charging | 4.05 | 4.3 | 4.5 | V |
| $\mathrm{V}_{\text {CCL }}$ Stop Threshold | GATEs stop switching, COMP discharging | 3.75 | 4.1 | 4.35 | V |
| $\mathrm{V}_{\text {CCL }}$ Hysteresis | GATEs not switching, COMP not charging | 100 | 200 | 300 | mV |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Start Threshold | GATEs switching, COMP charging | 8.0 | 8.5 | 9.0 | V |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Stop Threshold | GATEs stop switching, COMP discharging | 7.5 | 8.0 | 8.5 | V |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Hysteresis | GATEs not switching, COMP not charging | 300 | 500 | 700 | mV |

Reference Output

| $V_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{I}\left(\mathrm{V}_{\text {REF }}\right)<1.0 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Internal Ramp |  |  |  |  |  |
| Ramp Height @ $50 \%$ DTC | $\mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\text {REF }}$ | - | 125 | - | mV |

5. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 28 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 1 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 2 | $\mathrm{V}_{\mathrm{FB}}$ | Voltage Feedback Pin. To use Adaptive Voltage Positioning, set the light load offset voltage by connecting a resistor between $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {OUT }}$. The resistor and the $\mathrm{V}_{\text {FB }}$ bias current determine the offset. For no adaptive positioning connect $\mathrm{V}_{\mathrm{FB}}$ directly to $\mathrm{V}_{\mathrm{OUT}}$. |
| 3 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for Adaptive Voltage Positioning (AVP). The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to set the amount of AVP or leave this pin open for no AVP. This pin's maximum working voltage is 2.3 Vdc . |
| 4 | REF | Reference output. Decouple to LGND with $0.1 \mu \mathrm{~F}$. |
| 5 | ILIM | Sets threshold for current limit. Connect to reference through a resistive divider. This pin's maximum working voltage is 1.3 Vdc . |
| 6-10 | VID Pins | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |
| 11 | PWRGD | Power Good Output. Open collector output goes low when $\mathrm{CS}_{\text {REF }}$ is out of regulation. |
| 12 | CS ${ }_{\text {REF }}$ | Reference for current sense amplifiers, input to the Power Good comparators, and fast feedback connection to the PWM comparator. Connect this pin to the output voltage through a resistor equal to $1 / 5$ th the value of the current sense resistors. The input voltage to this pin must not exceed the maximum VID (DAC) setting by more than 100 mV . |
| 13, 14 | CS1-CS2 | Current Sense inputs. Connect Current Sense network for the corresponding phase to each input. The input voltages to these pins must be kept within 105 mV of $\mathrm{CS}_{\text {REF }}$ or pulse-by-pulse current limit will be triggered. |
| 15 | VTT | VTT sense input. The voltage on this pin must be higher than the VTT threshold (nominally 1.05 V ) or switching will not occur. |
| 16 | $\mathrm{VTT}_{\text {CT }}$ | 1.0 ms timer for VTT Power Good. |
| 17 | VTTP $_{\text {GD }}$ | VTT Power Good output. Open collector, pulls down when VTT < 1.03 V . |
| 18 | $\mathrm{V}_{\mathrm{CCH} 2}$ | Power for channel 2 high side gate driver. |
| 19, 20 | GATE(H)2, GATE(L)2 | High and low side gate drivers for channels 1 and 2. |
| 21 | $\mathrm{V}_{\text {CCL12 }}$ | Power for both low side gate drivers. |
| 22 | PGND | Return for all gate drivers. |
| 23, 24 | GATE(L)1, GATE(H)1 | Low and high side gate drivers for channels 1 and 2. |
| 25 | $\mathrm{V}_{\mathrm{CCH} 1}$ | Power for channel 1 high side gate driver. |
| 26 | $\mathrm{V}_{\mathrm{CCL}}$ | Power for logic. UVLO Sense for supply connects to this pin. |
| 27 | LGND | Ground for internal control circuits and the IC substrate connection. |
| 28 | Rosc | A resistor from this pin to ground sets operating frequency. |



CS5308

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Oscillator Frequency vs. Rosc


Figure 5. GATE(H) Rise Time vs. Load Capacitance Measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{cc}}$ at 5.0 V


Figure 7. GATE(L) Rise Time vs. Load Capacitance Measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V


Figure 4. V $_{\text {FB }} \&$ VTT $_{\text {CT }}$ Currents vs. Rosc Value


Figure 6. GATE(H) Fall Time vs. Load Capacitance Measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{cc}}$ at 5.0 V


Figure 8. GATE(L) Fall Time vs. Load Capacitance Measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{cc}}$ at 5.0 V

## APPLICATIONS INFORMATION

## Overview

The CS5308 DC/DC controller from ON Semiconductor was developed using the Enhanced $\mathrm{V}^{2}$ topology to meet requirements of low voltage, high current loads with fast transient requirements. Enhanced $\mathrm{V}^{2}$ combines the original $\mathrm{V}^{2}$ topology with peak current-mode control for fast transient response and current sensing capability. The addition of an internal PWM ramp and implementation of fast-feedback directly from $V_{\text {CORE }}$ has improved transient response and simplified design. The CS5308 includes VTT monitoring, $\mathrm{VTT}_{\mathrm{PGD}}$, PWRGD, and MOSFET gate drivers to provide a "fully integrated solution" to simplify design, minimize circuit board area, and reduce overall system cost.

Two advantages of a multi-phase converter over a single-phase converter are current sharing and increased apparent output frequency. Current sharing allows the designer to use less inductance in each phase than would be required in a single-phase converter. The smaller inductor will produce larger ripple currents but the total per phase power dissipation is reduced because the RMS current is lower. Transient response is improved because the control loop will measure and adjust the current faster in a smaller output inductor. Increased apparent output frequency is desirable because the off-time and the ripple voltage of the two-phase converter will be less than that of a single-phase converter.

## Fixed Frequency Multi-Phase Control

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5308 controller uses two-phase, fixed frequency, Enhanced $\mathrm{V}^{2}$ architecture to measure and control currents in
individual phases. Each phase is delayed $180^{\circ}$ from the previous phase. Normally, GATE(H) transitions to a high voltage at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring GATE(H) low. Once GATE(H) goes low, it will remain low until the beginning of the next oscillator cycle. While $\operatorname{GATE}(\mathrm{H})$ is high, the Enhanced $\mathrm{V}^{2}$ loop will respond to line and load variations. On the other hand, once $\operatorname{GATE}(\mathrm{H})$ is low, the loop can not respond until the beginning of the next PWM cycle. Therefore, constant frequency Enhanced $\mathrm{V}^{2}$ will typically respond to disturbances within the off-time of the converter.
The Enhanced $V^{2}$ architecture measures and adjusts the output current in each phase. An additional input ( CSn ) for inductor current information has been added to the $\mathrm{V}^{2 \mathrm{TM}}$ loop for each phase as shown in Figure 9. The triangular inductor current is measured differentially across $\mathrm{R}_{\mathrm{S}}$, amplified by CSA and summed with the Channel Startup Offset, the Internal Ramp, and the Output Voltage at the non-inverting input of the PWM comparator. The purpose of the Internal Ramp is to compensate for propagation delays in the CS5308. This provides greater design flexibility by allowing smaller external ramps, lower minimum pulse widths, higher frequency operation, and PWM duty cycles above $50 \%$ without external slope compensation. As the sum of the inductor current and the internal ramp increase, the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts a cycle with higher current, the PWM cycle will terminate earlier providing negative feedback. The CS5308 provides a CSn input for each phase, but the $\mathrm{CS}_{\text {REF }}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{CS}_{\text {REF }}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than a phase with a smaller current signal.


Figure 9. Enhanced V ${ }^{2}$ Control Employing Resistive Current Sensing and Additional Internal Ramp

Enhanced $\mathrm{V}^{2}$ responds to disturbances in $\mathrm{V}_{\text {CORE }}$ by employing both "slow" and "fast" voltage regulation. The internal error amplifier performs the slow regulation. Depending on the gain and frequency compensation set by the amplifier's external components, the error amplifier will typically begin to ramp its output to react to changes in the output voltage in 1-2 PWM cycles. Fast voltage feedback is implemented by a direct connection from $\mathrm{V}_{\text {CORE }}$ to the non-inverting pin of the PWM comparator via the summation with the inductor current, internal ramp, and OFFSET. A rapid increase in load current will produce a negative offset at $\mathrm{V}_{\text {CORE }}$ and at the output of the summer. This will cause the PWM duty cycle to increase almost instantly. Fast feedback will typically adjust the PWM duty-cycle in one PWM cycle.
As shown in Figure 9, a "partial" internal ramp (nominally 125 mV at a $50 \%$ duty cycle) is added to the inductor current ramp at the positive terminal of the PWM comparator. This additional ramp compensates for propagation time delays from the current sense amplifier (CSA), the PWM comparator, and the MOSFET gate drivers. As a result, the minimum ON time of the controller is reduced and lower duty cycles may be achieved at higher frequencies. Also, the additional ramp reduces the reliance on the inductor current ramp and allows greater flexibility when choosing the output inductor and the $\mathrm{R}_{\mathrm{CSn}} \mathrm{C}_{\mathrm{CSn}}(\mathrm{n}=1$ or 2 ) time constant of the feedback components from $\mathrm{V}_{\text {CORE }}$ to the CSn pin.
Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be:

$$
\begin{aligned}
\text { VCOMP }= & \text { VOUT @ } 0 \text { A }+ \text { Channel_Startup_Offset } \\
& + \text { Int_Ramp }+ \text { GCSA } \cdot \text { Ext_Ramp } / 2
\end{aligned}
$$

Int_Ramp is the "partial" internal ramp value at the corresponding duty cycle, Ext_Ramp is the peak-to-peak external steady-state ramp at 0 A, $\mathrm{G}_{\mathrm{CSA}}$ is the Current Sense Amplifier Gain (nominally $3.5 \mathrm{~V} / \mathrm{V}$ ), and the Channel Startup Offset is typically 0.40 V . The magnitude of the Ext_Ramp can be calculated from:

$$
\text { Ext_Ramp }=\mathrm{D} \cdot\left(\mathrm{~V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) /\left(\mathrm{R}_{\mathrm{CSn}} \cdot \mathrm{C}_{\mathrm{CSn}} \cdot \mathrm{fSW}\right)
$$

For example, if $\mathrm{V}_{\text {Out }}$ at 0 A is set to 1.745 V with AVP and the input voltage is 5.0 V , the duty cycle (D) will be $1.745 / 5.0$ or $35 \%$. Int_Ramp will be $125 \mathrm{mV} \bullet 35 / 50=87.5 \mathrm{mV}$. Realistic values for $\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}$ and $\mathrm{f}_{\text {Sw }}$ are $60 \mathrm{k} \Omega, 0.01 \mu \mathrm{~F}$, and 300 kHz - using these Ext_Ramp will be 6.3 mV .

$$
\begin{aligned}
\mathrm{V}_{\mathrm{COMP}}= & 1.745 \mathrm{~V}+0.40 \mathrm{~V}+87.5 \mathrm{mV} \\
& +3.5 \mathrm{~V} / \mathrm{V} \cdot 6.3 \mathrm{mV} / 2 \\
= & 2.244 \mathrm{Vdc}
\end{aligned}
$$

If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage.

Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as:

$$
\Delta \mathrm{V}=\mathrm{R} \cdot \mathrm{G} \cdot \mathrm{CSA} \cdot \Delta \mathrm{I} \text { OUT }
$$

The single-phase power stage output impedance is:

$$
\text { Single Stage Impedance }=\Delta \mathrm{V}_{\mathrm{OUT}} / \Delta \mathrm{I} \mathrm{OUT}=\mathrm{RS} \cdot \mathrm{GCSA}
$$

The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few microseconds of a transient before the feedback loop has repositioned the COMP pin.

The peak output current can be calculated from:
IOUT,PEAK $=\left(V_{\text {COMP }}-\right.$ VOUT - Offset $) /\left(\mathrm{RS}_{\text {S }} \cdot \mathrm{GCSA}\right)$
Figure 10 shows the step response of the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides a portion of the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current ramp, the "partial" internal ramp voltage signal and Offset exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the average current signal level (CSn output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 10. Open Loop Operation


Figure 11. Enhanced V² Control Employing Lossless Inductive Current Sensing and Internal Ramp

## Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 11. In the diagram, L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal, the values of $\mathrm{R}_{\mathrm{CSn}}$ and $\mathrm{C}_{\mathrm{CSn}}$ are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$. If this criteria is met, the current sense signal will be the same shape as the inductor current and the voltage signal at CSn will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor ( $\mathrm{R}_{\mathrm{S}}$ ).

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 9.

## Current Sharing Accuracy

Printed circuit board (PCB) traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at relatively the same point for each phase and the connection to the $\mathrm{CS}_{\mathrm{REF}}$ pin should be made so that no phase is favored. In some cases, especially with inductive sensing, resistance of the PCB can be useful for increasing the current sense resistance. The total current sense resistance used for calculations must include any PCB trace resistance between the CSn input and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case Current Sense Amplifier input mismatch is $\pm 5.0 \mathrm{mV}$ and will typically be within 3.0 mV . The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance a 3.0 mV mismatch with a $2.0 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## External Ramp Size and Current Sensing

The internal ramp allows flexibility of current sense time constant. Typically, the current sense $\mathrm{R}_{\mathrm{CSn}} \mathrm{C}_{\mathrm{CSn}}$ time constant ( $\mathrm{n}=1$ or 2 ) should be equal to or slower than the inductor's time constant. If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC or transient portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During a positive current transient, the COMP pin will be required to overshoot in response to the current signal in order to maintain the output voltage. Similarly, the $\mathrm{V}_{\text {DRP }}$ signal will overshoot which will produce too much transient droop in the output voltage. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.
The waveforms in Figure 12 show a simulation of the current sense signal and the actual inductor current during
a positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}$, $\mathrm{R}_{\mathrm{L}}=1.6 \mathrm{~m} \Omega, \mathrm{R}_{\mathrm{CSn}}=20 \mathrm{k}$ and $\mathrm{C}_{\mathrm{CSn}}=0.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of $\mathrm{R}_{\mathrm{CSn}}$ should be 31 $\mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu$ s time constant. With this compensation the $\mathrm{I}_{\text {LIM }}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 12. Inductive Sensing Waveform During a Load Step with Fast RC Time Constant ( $50 \mu \mathrm{~s} / \mathrm{div}$ )

## Current Limit

Two levels of over-current protection are provided. First, if the voltage on the Current Sense pins (either CS1 or CS2) exceeds CS $_{\text {REF }}$ by more than a fixed threshold (Single Pulse Current Limit), the PWM comparator is turned off. This provides fast peak current protection for individual phases. Second, the individual phase currents are summed and low-pass filtered to compare an averaged current signal to a user adjustable voltage on the $\mathrm{I}_{\text {LIM }}$ pin. If the $\mathrm{I}_{\text {LIM }}$ voltage is exceeded, the fault latch trips and the Soft Start capacitor is discharged until the COMP pin reaches 0.27 V . Then Soft Start begins. The converter will continue to operate in a low current hiccup mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced $\mathrm{V}^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET to shut OFF and the synchronous (lower) MOSFET to turn ON. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is applied. Similarly, the output voltage can be set lower than nominal during heavy loads to reduce overshoot when the load current is removed. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example; in a 50 A converter a $1 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond to changes in load current. Figure 13 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 13. Adaptive Positioning
The controller can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram in Figure 1.) To set the no-load positioning, a resistor is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to adjust the no-load output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of $\mathrm{R}_{\mathrm{OSC}}$ as shown in the data sheets.

During no-load conditions the $\mathrm{V}_{\mathrm{DRP}}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor. When output current increases the $\mathrm{V}_{\text {DRP }}$ pin increases proportionally and the $\mathrm{V}_{\text {DRP }}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to decrease.

The response during the first few microseconds of a load transient are controlled primarily by power stage output impedance and the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the current signal is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

## Error Amp Compensation \& Tuning

The transconductance error amplifier requires a capacitor ( $\mathrm{C}_{\mathrm{CMP} 2}$ in the Applications Diagram) between the COMP pin and GND for two reasons. First, this capacitor stabilizes the transconductance error amplifier. Values less than a few nF may cause oscillations of the COMP voltage. These oscillations will increase the output voltage jitter. Second, this capacitor sets the Soft Start time when power is applied to the converter or the converter is enabled. The internal error amplifier will source approximately $30 \mu \mathrm{~A}$ during Soft Start and no switching will occur until the COMP voltage exceeds the Channel Startup Offset (nominally 0.4 V ). The COMP voltage will ramp up to the value shown previously (repeated here for convenience):

$$
\begin{aligned}
\text { VCOMP }= & \text { VOUT @ } 0 \text { A }+ \text { Channel_Startup_Offset } \\
& + \text { Int_Ramp }+ \text { GCSA } \cdot \text { Ext_Ramp } / 2
\end{aligned}
$$

The RC network between the COMP pin and the Soft Start capacitor ( $\mathrm{R}_{\mathrm{CMP1}}$ and $\mathrm{C}_{\mathrm{CMP1}}$ ) allows the COMP voltage to slew quickly during transient loading of the converter. Without this network the error amplifier would have to drive the large Soft Start/Stability capacitor directly, which would drastically limit the slew rate of the COMP voltage. The $\mathrm{R}_{\mathrm{CMP1}} / \mathrm{C}_{\mathrm{CMP} 1}$ network allows the COMP voltage to undergo a step change in voltage of approximately $\mathrm{R}_{\mathrm{CMP} 1} \bullet \mathrm{I}_{\mathrm{COMP}}$.

The capacitor ( $\mathrm{C}_{\mathrm{AMP}}$ ) between the COMP pin and the inverting error amplifier input (the $\mathrm{V}_{\mathrm{FB}} \mathrm{pin}$ ) and the parallel combination of the resistors $\mathrm{R}_{\mathrm{FBK} 1}$ and $\mathrm{R}_{\mathrm{DRP} 1}$ determine the bandwidth of the error amplifier. The gain of the error amplifier crosses 0 dB at a high enough frequency to give a quick transient response, but well below the switching frequency to minimize ripple and noise on the COMP pin. A capacitor in parallel with the $\mathrm{V}_{\mathrm{FB}}$ resistor $\left(\mathrm{C}_{\mathrm{FBK} 2}\right)$ adds a zero to boost phase near the crossover frequency to improve loop stability.

Setting-up and tuning the error amplifier is a three step process. First, the no-load and full-load adaptive voltage positioning (AVP) are set using $\mathrm{R}_{\mathrm{FBK} 1}$ and $\mathrm{R}_{\mathrm{DRP} 1}$, respectively. Second, the current sense time constant and error amplifier gain are adjusted with $\mathrm{R}_{\mathrm{CSn}}$ and $\mathrm{C}_{\mathrm{AMP}}$ while monitoring $V_{\text {OUT }}$ during transient loading. Lastly, the peak-to-peak voltage ripple on the COMP pin is examined when the converter is fully loaded to insure low output voltage jitter. The details of this process are covered in the Design Procedure section.

## Undervoltage Lockout (UVLO)

The controller has undervoltage lockout functions connected to two pins. One, intended for the logic and low-side drivers, with approximately a 4.2 V turn-on threshold is connected to the $\mathrm{V}_{\mathrm{CC}}$ pin. A second, for the high side drivers, with approximately an 8.25 V threshold, is connected to the $\mathrm{V}_{\mathrm{CCH}}$ pin.

The UVLO threshold for the high side drivers varies with the part type. In many applications this function will be disabled or will only check that the applicable supply is on - not that is at a high enough voltage to run the converter. See individual data sheets for more information on UVLO.

## Soft Start Enable, and Hiccup Mode

A capacitor between the COMP pin and GND controls Soft Start and hiccup mode slopes. A $0.1 \mu \mathrm{~F}$ capacitor with the $30 \mu \mathrm{~A}$ charge current will allow the output to ramp up at $0.3 \mathrm{~V} / \mathrm{ms}$ or 1.5 V in 5 ms at start-up.

When a fault is detected due to an overcurrent condition the converter will enter a low duty cycle hiccup mode. During hiccup mode the converter will not switch from the time a fault is detected until the Soft Start capacitor has discharged below the Soft Start Discharge Threshold and then charged back up above the Channel Start Up Offset.

The COMP pin will disable the converter when pulled below 0.27 V

## VTT Monitoring \& VTT Power Good (VTT ${ }_{\text {PGD }}$ )

The CS5308 includes VTT monitoring, delay timing and an open-collector VTT Power Good ( $\mathrm{VTT}_{\mathrm{PGD}}$ ) output. A comparator with a threshold of approximately 1.05 V monitors VTT. At power-up, VTT PGD is held low and is released a short time after VTT crosses the 1.05 V threshold. The time between VTT stabilizing and the release of $\mathrm{VTT}_{\mathrm{PGD}}$ is set by a capacitor ( $\mathrm{C}_{\mathrm{VTT}}$ ) at the open-collector $\mathrm{VTT}_{\mathrm{CT}}$ pin. The voltage at the $\mathrm{VTT}_{\mathrm{CT}}$ pin will ramp from its $\mathrm{V}_{\mathrm{CE}(\mathrm{sat})}$ voltage, approximately 0.25 V , to 1 V before $\mathrm{VTT}_{\mathrm{PGD}}$ is pulled HIGH. The $\mathrm{VTT}_{\mathrm{CT}}$ charging current and $\mathrm{C}_{\text {VTT }}$ set the $\mathrm{VTT}_{\text {PGD }}$ delay time. The delay time can be calculated using:

$$
\text { TD,VTT = (1 V - } 0.25 \mathrm{~V}) \cdot \mathrm{CVTT} / \mathrm{VTT} \mathrm{CT} \text { _Current. }
$$

The $\mathrm{VTT}_{\mathrm{CT}}$ charging current is dependent on the selection of the oscillator frequency. See Figure 3 for a representation of oscillator frequency and charging current versus $\mathrm{R}_{\text {OSC }}$ value.

If either VTT or VTT $_{\text {PGD }}$ are held LOW, the internal Fault latch will be SET, the controller will stop switching, and $V_{\text {CORE }}$ will be zero.

## Power Good (PWRGD)

The open-collector Power Good (PWRGD) pin is driven by a "window-comparator" monitoring VCORE. This comparator will transition HIGH if $\mathrm{V}_{\text {CORE }}$ is within $\pm 12 \%$ of the nominal VID setting. After a $50 \mu \mathrm{~s}$ delay, the comparators output will saturate the open-collector output transistor and the PWRGD pin will be pulled LOW.

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically, a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to route the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

The current sense signals are typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as the switch node and gate drive signals. If the current signals are taken from a location other than directly at the inductor any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistances and should be considered in design calculations. The capacitors for the current feedback networks should be placed as close to the current sense pins as practical. After placing the CS5308 control IC, follow these guidelines to optimize the layout and routing:

1. Place the $1 \mu \mathrm{~F}$ power-supply bypass (ceramic) capacitors close to their associated pins: $\mathrm{V}_{\mathrm{CCL}}$, $\mathrm{V}_{\mathrm{CCH} 1}, \mathrm{~V}_{\mathrm{CCH} 2}, \mathrm{~V}_{\mathrm{CCL} 12}$.
2. Place the MOSFETs to minimize the length of the Gate traces. Orient the MOSFETs such that the Drain connections are away from the controller and the Gate connections are closest to the controller.
3. Place the components associated with the internal error amplifier ( $\mathrm{R}_{\mathrm{FBK} 1}, \mathrm{C}_{\mathrm{FBK} 2}, \mathrm{C}_{\mathrm{AMP}}, \mathrm{R}_{\mathrm{CMP} 1}$, $\mathrm{C}_{\mathrm{CMP} 1}, \mathrm{C}_{\mathrm{CMP} 2}, \mathrm{R}_{\mathrm{DRP} 1}$ ) to minimize the trace lengths to the pins $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{DRP}}$ and COMP.
4. Place the current sense components ( $\mathrm{R}_{\mathrm{CS} 1}, \mathrm{R}_{\mathrm{CS} 2}$, $\mathrm{C}_{\mathrm{CS} 1}, \mathrm{C}_{\mathrm{CS} 2}, \mathrm{R}_{\mathrm{CSREF}}, \mathrm{C}_{\mathrm{CSREF}}$ ) near the CS1, CS2, and $C_{\text {REF }}$ pins.
5. Place the frequency setting resistor ( $\mathrm{R}_{\mathrm{OSC}}$ ) close to the $\mathrm{R}_{\text {OSC }}$ pin. The $\mathrm{R}_{\text {OSC }}$ pin is very sensitive to noise. Route noisy traces, such as the SWNODEs and GATE traces, away from the $\mathrm{R}_{\mathrm{OSC}}$ pin and resistor.
6. Place the VTT timing capacitor ( $\mathrm{C}_{\mathrm{VTT}}$ ) and pull-up resistor $\left(\mathrm{R}_{\mathrm{VTT}}\right)$ near the $\mathrm{VTT}_{\mathrm{CT}}$ and $\mathrm{VTT}_{\mathrm{PGD}}$ pins.
7. Place the MOSFETs and output inductors to reduce the size of the noisy SWNODEs. There is a trade-off between reducing the size of the SWNODEs for noise reduction and providing adequate heat-sinking for the synchronous MOSFETs.
8. Place the input inductor and input capacitor(s) near the Drain of the control (upper) MOSFETs. There is a trade-off between reducing the size of this node to save board area and providing adequate heat-sinking for the control MOSFETs.
9. Place the output capacitors (electrolytic and ceramic) close to the processor socket or output connector.
10. The trace from the SWNODEs to the current sense components will be very noisy. Route this away from more sensitive, low-level traces. The Ground layer can be used to help isolate this trace.
11. The Gate traces are very noisy. Route these away from more sensitive, low-level traces. Keep each Gate signal on one layer and insure that there is an uninterrupted return path directly below the Gate trace. The Ground layer can be used to help isolate these traces.
12. Don't "daisy chain" connections to Ground from one via. Allow each connection to Ground to have its own via as close to the component as possible.
13. Use a slot in the ground plane from the bulk output capacitors back to the input power connector to prevent high currents from flowing beneath the control IC. This slot should extend length-wise under the control IC and separate the connections to "signal ground" and "power ground." Examples of signal ground include the capacitors at COMP, $\mathrm{CS}_{\mathrm{REF}}, \mathrm{REF}$, and $\mathrm{VTT}_{\mathrm{CT}}$, the resistors at $\mathrm{R}_{\mathrm{OSC}}$ and $\mathrm{I}_{\mathrm{LIM}}$, and the LGND pin to the controller. Examples of power ground include the capacitors to $\mathrm{V}_{\mathrm{CCH} 1}$, $\mathrm{V}_{\mathrm{CCH} 2}$ and $\mathrm{V}_{\mathrm{CCL} 12}$, the Source of the synchronous MOSFETs, and the PGND pin to the controller.
14. The $\mathrm{CS}_{\text {REF }}$ sense point should be equidistant between the output inductors to equalize the PCB resistance added to the current sense paths. This will insure acceptable current sharing. Also, route the $\mathrm{CS}_{\text {REF }}$ connection away from noisy traces such as the SWNODEs and GATE traces. If noise from the SWNODEs or GATE signals capacitively couples to the $\mathrm{CS}_{\text {REF }}$ trace the external ramps will be very noise and voltage jitter will result.
15. Ideally, the SWNODEs are exactly the same shape and the current sense points (connections to $\mathrm{R}_{\mathrm{CS} 1}$ and $\mathrm{R}_{\mathrm{CS} 2}$ ) are made at identical locations to equalize the PCB resistance added to the current sense paths. This will help to insure acceptable current sharing.
16. Place the $0.1 \mu \mathrm{~F}$ ceramic capacitors, $\mathrm{C}_{\mathrm{Q} 1}$ and $\mathrm{C}_{\mathrm{Q} 2}$, close to the drains of the MOSFETs Q1 and Q2, respectively.

## Design Procedure

## 1. Output Capacitor Selection

The output capacitors filter the current from the output inductor and provide a low impedance for transient load current changes. Typically, microprocessor applications will require both bulk (electrolytic, tantalum) and low impedance, high frequency (ceramic) types of capacitors. The bulk capacitors provide "hold up" during transient loading. The low impedance capacitors reduce steady-state ripple and bypass the bulk capacitance when the output current changes very quickly. The microprocessor manufacturers usually specify a minimum number of ceramic capacitors. The designer must determine the number of bulk capacitors.

Choose the number of bulk output capacitors to meet the peak transient requirements. The formula below can be used to provide a starting point for the minimum number of bulk capacitors ( $\mathrm{N}_{\text {OUT,MIN }}$ ):

$$
\begin{equation*}
\text { NOUT,MIN }=\text { ESR per capacitor } \cdot \frac{\Delta \mathrm{I}, \mathrm{MAX}}{\Delta \mathrm{~V}_{\mathrm{O}, \mathrm{MAX}}} \tag{1}
\end{equation*}
$$

In reality, both the ESR and ESL of the bulk capacitors determine the voltage change during a load transient according to:
$\Delta \mathrm{V}_{\mathrm{O}, \mathrm{MAX}}=\left(\Delta \mathrm{I}_{\mathrm{O}, \mathrm{MAX}} / \Delta \mathrm{t}\right) \cdot \mathrm{ESL}+\Delta \mathrm{I}_{\mathrm{O}, \mathrm{MAX}} \cdot \mathrm{ESR}$
Unfortunately, capacitor manufacturers do not specify the ESL of their components and the inductance added by the PCB traces is highly dependent on the layout and routing. Therefore, it is necessary to start a design with slightly more than the minimum number of bulk capacitors and perform transient testing or careful modeling/simulation to determine the final number of bulk capacitors.

## 2. Output Inductor Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady-state and transient performance of the converter. When selecting an inductor the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size, and cost (usually the primary concern).

In general, the output inductance value should be as low and physically small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc.) resulting in increased dissipation and lower converter efficiency. Also, increased ripple currents will force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors - the converter cost will be adversely effected.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. Equation 3 may be used to calculate the minimum inductor value to produce a given maximum ripple current ( $\alpha$ ) per phase. The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the maximum ripple current.

$$
\begin{equation*}
\text { LOMIN }=\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}\right) \cdot \mathrm{V}_{\text {OUT }}}{\left(\alpha \cdot \mathrm{I}_{\mathrm{O}, \mathrm{MAX}} \cdot \mathrm{~V}_{\mathrm{IN}} \cdot \mathrm{fSW}\right)} \tag{3}
\end{equation*}
$$

$\alpha$ is the ripple current as a percentage of the maximum output current per phase ( $\alpha=0.15$ for $\pm 15 \%, \alpha=0.25$ for $\pm 25 \%$, etc.). If the minimum inductor value is used, the inductor current will swing $\pm \alpha \%$ about its value at the center ( $1 / 2$ the DC output current for a two-phase converter). Therefore, for a two-phase converter, the inductor must be designed or selected such that it will not saturate with a peak current of $(1+\alpha) \bullet \mathrm{I}_{\mathrm{O}, \mathrm{MAX}} / 2$.
The maximum inductor value is limited by the transient response of the converter. If the converter is to have a fast transient response then the inductor should be made as small as possible. If the inductor is too large its current will change too slowly, the output voltage will droop excessively, more bulk capacitors will be required, and the converter cost will be increased. For a given inductor value, its interesting to determine the times required to increase or decrease the current.

For increasing current:

$$
\begin{equation*}
\Delta \mathrm{t} \mathrm{INC}=\mathrm{Lo} \cdot \Delta \mathrm{I}_{\mathrm{O}} /\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \tag{3.1}
\end{equation*}
$$

For decreasing current:

$$
\begin{equation*}
\Delta \mathrm{tDEC}=\mathrm{Lo} \cdot \Delta \mathrm{IO} /(\mathrm{VOUT}) \tag{3.2}
\end{equation*}
$$

For typical processor applications with output voltages less than half the input voltage, the current will be increased much more quickly than it can be decreased. It may be more difficult for the converter to stay within the regulation limits when the load is removed than when it is applied - excessive overshoot may result.

The output voltage ripple can be calculated using the output inductor value derived in this Section (Lomin), the number of output capacitors ( $\mathrm{N}_{\text {OUT,MIN }}$ ) and the per capacitor ESR determined in the previous Section:

$$
\begin{align*}
& \text { VOUT,P-P }=(\text { ESR per cap } / \text { NOUT,MIN }) \cdot  \tag{4}\\
& \quad\{(\text { VIN }- \text { \#Phases } \cdot \text { VOUT }) \cdot \mathrm{D} /(\text { LoMIN } \cdot \text { fSW })\}
\end{align*}
$$

This formula assumes steady-state conditions with no more than one phase on at any time. The second term in Equation 4 is the total ripple current seen by the output capacitors. The total output ripple current is the "time
summation" of the two individual phase currents that are 180 degrees out-of-phase. As the inductor current in one phase ramps upward, current in the other phase ramps downward and provides a canceling of currents during part of the switching cycle. Therefore, the total output ripple current and voltage are reduced in a multi-phase converter.

## 3. Input Capacitor Selection

The choice and number of input capacitors is primarily determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with adequate margin. To calculate the number of input capacitors one must first determine the total RMS input ripple current. To this end, begin by calculating the average input current to the converter:

$$
\begin{equation*}
\mathrm{I} \mathrm{IN}, \mathrm{AVG}=\mathrm{IO}, \mathrm{MAX} \cdot \mathrm{D} / \eta \tag{5}
\end{equation*}
$$

where:
D is the duty cycle of the converter, $\mathrm{D}=\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}}$; $\eta$ is the specified minimum efficiency;
$\mathrm{I}_{\mathrm{O}, \text { MAX }}$ is the maximum converter output current.
The input capacitors will discharge when the control FET is ON and charge when the control FET is OFF as shown in Figure 14.


Figure 14. Input Capacitor Current for a Two-Phase Converter

The following equations will determine the maximum and minimum currents delivered by the input capacitors:

$$
\begin{align*}
\mathrm{IC}, \mathrm{MAX} & =\mathrm{I} \mathrm{LO}, \mathrm{MAX} / \eta-\mathrm{I} \mathrm{IN}, \mathrm{AVG}  \tag{6}\\
\mathrm{IC}, \mathrm{MIN} & =\mathrm{I} \mathrm{LO}, \mathrm{MIN} / \eta-\mathrm{I} \mathrm{IN}, \mathrm{AVG} \tag{7}
\end{align*}
$$

$\mathrm{I}_{\text {Lo,MAX }}$ is the maximum output inductor current:

$$
\begin{equation*}
\mathrm{I}_{\mathrm{Lo}, \mathrm{MAX}}=\mathrm{I} \mathrm{O}, \mathrm{MAX} / 2+\Delta \mathrm{I}_{\mathrm{Lo}} / 2 \tag{8}
\end{equation*}
$$

$\mathrm{I}_{\mathrm{Lo}, \mathrm{MIN}}$ is the minimum output inductor current:

$$
\begin{equation*}
\mathrm{I} \mathrm{Lo}, \mathrm{MIN}=\mathrm{I}, \mathrm{MAX} / 2-\Delta \mathrm{I} \mathrm{Lo} / 2 \tag{9}
\end{equation*}
$$

$\Delta \mathrm{I}_{\mathrm{Lo}}$ is the peak-to-peak ripple current in the output inductor of value Lo:

$$
\begin{equation*}
\Delta \mathrm{I}_{\mathrm{Lo}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \cdot \mathrm{D} /(\mathrm{Lo} \cdot \mathrm{fSW}) \tag{10}
\end{equation*}
$$

For the two-phase converter, the input capacitor(s) RMS current is then:

$$
\begin{align*}
& \mathrm{I}_{\mathrm{CIN}} \mathrm{RMS}=\left[2 \mathrm { D } \cdot \left(\mathrm{IC}, \mathrm{MIN}^{2}+\mathrm{I}_{\mathrm{C}, \mathrm{MIN} \cdot \Delta \mathrm{I}} \mathrm{I}, \mathrm{IN}\right.\right.  \tag{11}\\
& \left.\left.+\Delta_{C}, I^{2} / 3\right)+I_{I N}, A V G^{2} \cdot(1-2 D)\right]^{1 / 2}
\end{align*}
$$

Select the number of input capacitors $\left(\mathrm{N}_{\mathrm{IN}}\right)$ to provide the RMS input current ( $\mathrm{I}_{\mathrm{CIN}, \mathrm{RMS}}$ ) based on the RMS ripple current rating per capacitor ( $\mathrm{I}_{\text {RMS,RATED }}$ ):
NIN = ICIN,RMS/IRMS,RATED

For a two-phase converter with perfect efficiency ( $\eta=1$ ), the worst case input ripple-current will occur when the converter is operating at a $25 \%$ duty cycle. At this operating point, the parallel combination of input capacitors must support an RMS ripple current equal to $25 \%$ of the converter's DC output current. At other duty cycles, the ripple-current will be less. For example, at a duty cycle of either $10 \%$ or $40 \%$, the two-phase input ripple-current will be approximately $20 \%$ of the converter's DC output current.
In general, capacitor manufacturers require derating to the specified ripple-current based on the ambient temperature. More capacitors will be required because of the current derating. The designer should be cognizant of the ESR of the input capacitors. The input capacitor power loss can be calculated from:

$$
\begin{equation*}
\text { PCIN }=\text { ICIN,RMS }{ }^{2} \cdot \text { ESR_per_capacitor/NIN } \tag{13}
\end{equation*}
$$

Low ESR capacitors are recommended to minimize losses and reduce capacitor heating. The life of an electrolytic capacitor is reduced $50 \%$ for every $10^{\circ} \mathrm{C}$ rise in the capacitor's temperature.

## 4. Input Inductor Selection

The use of an inductor between the input capacitors and the power source will accomplish two objectives. First, it will isolate the voltage source and the system from the noise generated in the switching supply. Second, it will limit the inrush current into the input capacitors at power up. Large inrush currents will reduce the expected life of the input capacitors. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients.


Figure 15. Calculating the Input Inductance

The worst case input current slew rate will occur during the first few PWM cycles immediately after a step-load change is applied as shown in Figure 15. When the load is applied, the output voltage is pulled down very quickly. Current through the output inductors will not change instantaneously so the initial transient load current must be conducted by the output capacitors. The output voltage will step downward depending on the magnitude of the output current ( $\mathrm{I}_{\mathrm{O}, \mathrm{MAX}}$ ), the per capacitor ESR of the output capacitors ( $\mathrm{ESR}_{\mathrm{OUT}}$ ), and the number of the output capacitors $\left(\mathrm{N}_{\text {OUT }}\right)$ as shown in Figure . Assuming the load current is shared equally between the two phases, the output voltage at full, transient load will be:

$$
\begin{aligned}
& \text { VOUT,FULL-LOAD }= \\
& \text { VOUT,NO-LOAD }-(\mathrm{IO}, \mathrm{MAX} / 2) \cdot \text { ESROUT/NOUT }
\end{aligned}
$$

When the control MOSFET (Q1 in Figure 15) turns ON, the input voltage will be applied to the opposite terminal of the output inductor (the SWNODE). At that instant, the voltage across the output inductor can be calculated as:

$$
\begin{align*}
\Delta \mathrm{V}_{\text {Lo }}= & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }, \text { FULL-LOAD }}  \tag{15}\\
= & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT,NO-LOAD }} \\
& +(\mathrm{IO}, \mathrm{MAX} / 2) \cdot \text { ESROUT }^{2} \text { NOUT }
\end{align*}
$$

The differential voltage across the output inductor will cause its current to increase linearly with time. The slew rate of this current can be calculated from:

$$
\begin{equation*}
\mathrm{dl} \mathrm{Lo} / \mathrm{dt}=\Delta \mathrm{V}_{\mathrm{Lo}} / \mathrm{Lo} \tag{16}
\end{equation*}
$$

Current changes slowly in the input inductor so the input capacitors must initially deliver the vast majority of the input current. The amount of voltage drop across the input capacitors $\left(\Delta \mathrm{V}_{\mathrm{Ci}}\right)$ is determined by the number of input capacitors $\left(\mathrm{N}_{\mathrm{IN}}\right)$, their per capacitor ESR $\left(\mathrm{ESR}_{\mathrm{IN}}\right)$, and the current in the output inductor according to:

$$
\begin{align*}
\Delta \mathrm{V}_{\mathrm{Ci}} & =\mathrm{ESR}_{\mathrm{IN}} / \mathrm{N}_{\mathrm{IN}} \cdot \mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt} \cdot \mathrm{tON}  \tag{17}\\
& =\mathrm{ESR} \mathrm{IN}_{\mathrm{N}} / \mathrm{N}_{\mathrm{IN}} \cdot \mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt} \cdot \mathrm{D} / \mathrm{fSW}
\end{align*}
$$

Before the load is applied, the voltage across the input inductor $\left(\mathrm{V}_{\mathrm{Li}}\right)$ is very small - the input capacitors charge to the input voltage, $\mathrm{V}_{\mathrm{IN}}$. After the load is applied the voltage drop across the input capacitors, $\Delta \mathrm{V}_{\mathrm{Ci}}$, appears across the input inductor as well. Knowing this, the minimum value of the input inductor can be calculated from:

$$
\begin{align*}
\mathrm{Li}_{\mathrm{MIN}} & =\mathrm{V}_{\mathrm{Li}} / \mathrm{dl}_{\mathrm{IN}} / \mathrm{dt}_{\mathrm{MAX}}  \tag{18}\\
& =\Delta \mathrm{V}_{\mathrm{Ci}} / \mathrm{dl}_{\mathrm{IN}} / \mathrm{dt}_{\mathrm{MAX}}
\end{align*}
$$

$\mathrm{dI}_{\mathrm{IN}} / \mathrm{dt}_{\text {MAX }}$ is the maximum allowable input current slew rate (specified as $0.1 \mathrm{~A} / \mu$ s or $0.1 \times 10^{6} \mathrm{~A} / \mathrm{s}$ for VRM 8.5).

The input inductance value calculated from Equation 18 is relatively conservative. It assumes the supply voltage is very "stiff" and does not account for any parasitic elements that will limit $\mathrm{dI} / \mathrm{dt}$ such as stray inductance. Also, the ESR values of the capacitors specified by the manufacturer's data sheets are worst case high limits. In reality input voltage "sag," lower capacitor ESRs, and stray inductance will help reduce the slew rate of the input current.

As with the output inductor, the input inductor must support the maximum current without saturating the magnetic. Also, for an inexpensive iron powder core, such as the -26 or -52 from Micrometals, the inductance "swing" with DC bias must be taken into account - inductance will decrease as the DC input current increases. At the maximum input current, the inductance must not decrease below the minimum value or the $\mathrm{dI} / \mathrm{dt}$ will be higher than expected.

## 5. MOSFET \& Heatsink Selection

Power dissipation, package size, and thermal solution drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation. Once the dissipation is known, the heat sink
thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non-overlap time of the gate drivers.

For the upper or control MOSFET, the power dissipation can be approximated from:

$$
\begin{align*}
& P_{D, C O N T R O L}=\left(\operatorname{IRMS}, C N T L{ }^{2} \cdot R_{D S}(o n)\right)  \tag{19}\\
& +\left(\mathrm{L}_{\mathrm{Lo}, \mathrm{MAX}} \cdot \mathrm{Q}_{\text {switch }} / \mathrm{I}_{\mathrm{g}} \cdot \mathrm{~V}_{\text {IN }} \cdot \mathrm{f}_{\mathrm{SW}}\right) \\
& +\left(Q_{\mathrm{Oss}} / 2 \cdot \mathrm{~V}_{\mathrm{IN}} \cdot \mathrm{fs}_{\mathrm{S}}\right)+\left(\mathrm{V}_{\mathrm{IN}} \cdot \mathrm{Q}_{\mathrm{RR}} \cdot \mathrm{f}_{\mathrm{SW}}\right)
\end{align*}
$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the losses associated with the control and synchronous MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the synchronous MOSFET. The first two terms are usually adequate to predict the majority of the losses.

Where $\mathrm{I}_{\mathrm{RMS}, \mathrm{CNTL}}$ is the RMS value of the trapezoidal current in the control MOSFET:

IRMS,CNTL $=\sqrt{D}$

$\mathrm{I}_{\text {Lo,MAX }}$ is the maximum output inductor current:

$$
\begin{equation*}
\mathrm{ILo}_{\mathrm{Lo}, \mathrm{MAX}}=\mathrm{IO}, \mathrm{MAX} / 2+\Delta \mathrm{I}_{\mathrm{Lo}} / 2 \tag{21}
\end{equation*}
$$

$\mathrm{I}_{\mathrm{Lo}, \mathrm{MIN}}$ is the minimum output inductor current:

$$
\begin{equation*}
\mathrm{I} \mathrm{Lo}, \mathrm{MIN}=\mathrm{I} \mathrm{O}, \mathrm{MAX} / 2-\Delta \mathrm{I} \mathrm{Lo} / 2 \tag{22}
\end{equation*}
$$

$\mathrm{I}_{\mathrm{O}, \text { MAX }}$ is the maximum converter output current.
D is the duty cycle of the converter:

$$
\begin{equation*}
\mathrm{D}=\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}} \tag{23}
\end{equation*}
$$

$\Delta \mathrm{I}_{\mathrm{Lo}}$ is the peak-to-peak ripple current in the output inductor of value $L_{0}$ :

$$
\begin{equation*}
\Delta \mathrm{I}_{\mathrm{Lo}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \cdot \mathrm{D} /(\mathrm{Lo} \cdot \mathrm{fSW}) \tag{24}
\end{equation*}
$$

$\mathrm{R}_{\mathrm{DS}(\text { on) }}$ is the ON resistance of the MOSFET at the applied gate drive voltage.
$Q_{\text {switch }}$ is the post gate threshold portion of the gate-to-source charge plus the gate-to-drain charge. This
may be specified in the data sheet or approximated from the gate-charge curve as shown in the Figure 16.

$$
\begin{equation*}
Q_{s w i t c h}=Q_{g s 2}+Q_{g d} \tag{25}
\end{equation*}
$$



Figure 16. MOSFET Switching Characteristics
$\mathrm{I}_{\mathrm{g}}$ is the output current from the gate driver IC.
$\mathrm{V}_{\mathrm{IN}}$ is the input voltage to the converter.
$\mathrm{f}_{\text {sw }}$ is the switching frequency of the converter.
$\mathrm{Q}_{\mathrm{G}}$ is the MOSFET total gate charge to obtain $\mathrm{R}_{\mathrm{DS}(\text { on })}$. Commonly specified in the data sheet.
$\mathrm{V}_{\mathrm{g}}$ is the gate drive voltage.
$\mathrm{Q}_{\mathrm{RR}}$ is the reverse recovery charge of the lower MOSFET.
$\mathrm{Q}_{\text {oss }}$ is the MOSFET output charge specified in the data sheet.
For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$
\begin{align*}
& \text { PD,SYNCH }=\left(I_{R M S}, S Y N C H^{2} \cdot \operatorname{RDS}(o n)\right) \\
& \quad+\left(\text { Vf }_{\text {diode }} \cdot \mathrm{IO}_{\mathrm{O}}, \mathrm{MAX} / 2 \cdot \mathrm{t} \text { _nonoverlap } \cdot \mathrm{fSW}\right) \tag{26}
\end{align*}
$$

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non-overlap time.
All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$
\begin{align*}
& \text { IRMS,SYNCH }=\sqrt{1-\mathrm{D}}  \tag{27}\\
& \cdot\left[\left(\text { ILo }_{\text {Lo }}\right.\right. \text { MAX }
\end{align*}
$$

where:
$\mathrm{Vf}_{\text {diode }}$ is the forward voltage of the MOSFET's intrinsic diode at the converter output current.
t _nonoverlap is the non-overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.


Figure 17. AVP Circuitry at No-Load

When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature

$$
\begin{equation*}
\theta \mathrm{T}<(\mathrm{T} \mathrm{~J}-\mathrm{T} \mathrm{~A}) / \mathrm{PD}_{\mathrm{D}} \tag{28}
\end{equation*}
$$

where:
$\theta_{\mathrm{T}}$ is the total thermal impedance $\left(\theta_{\mathrm{JC}}+\theta_{\mathrm{SA}}\right)$;
$\theta_{\mathrm{JC}}$ is the junction-to-case thermal impedance of the MOSFET;
$\theta_{\mathrm{SA}}$ is the sink-to-ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal "pad" is used);
$\mathrm{T}_{\mathrm{J}}$ is the specified maximum allowed junction temperature;
$\mathrm{T}_{\mathrm{A}}$ is the worst case ambient operating temperature.
For TO-220 and TO-263 packages, standard FR-4 copper clad circuit boards will have approximate thermal resistances $\left(\theta_{\mathrm{SA}}\right)$ as shown below:

| Pad Size <br> $\left(\right.$ in $^{2} / \mathrm{mm}^{2}$ ) | Single-Sided <br> 1 oz. Copper |
| :---: | :---: |
| $0.50 / 323$ | $60-65^{\circ} \mathrm{C} / \mathrm{W}$ |
| $0.75 / 484$ | $55-60^{\circ} \mathrm{C} / \mathrm{W}$ |
| $1.00 / 645$ | $50-55^{\circ} \mathrm{C} / \mathrm{W}$ |
| $1.50 / 968$ | $45-50^{\circ} \mathrm{C} / \mathrm{W}$ |

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e., worst case MOSFET $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ ). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board
and MOSFET. For any new design, its advisable to have as much heatsink area as possible - all too often new designs are found to be too hot and require re-design to add heatsinking.

## 6. Adaptive Voltage Positioning

There are two resistors that determine the Adaptive Voltage Positioning: $\mathrm{R}_{\text {VFBK }}$ and $\mathrm{R}_{\text {DRP }}$. R RFBK establishes the no-load "high" voltage position and $\mathrm{R}_{\mathrm{DRP}}$ determines the full-load "droop" voltage.
Resistor $\mathrm{R}_{\mathrm{VFBK}}$ is connected between $\mathrm{V}_{\text {CORE }}$ and the $\mathrm{V}_{\mathrm{FB}}$ pin of the controller. At no load, this resistor will conduct the internal bias current of the $\mathrm{V}_{\mathrm{FB}}$ pin and develop a voltage drop from $V_{\text {CORE }}$ to the $V_{\text {FB }}$ pin. Because the error amplifier regulates $\mathrm{V}_{\mathrm{FB}}$ to the DAC setting, the output voltage, $\mathrm{V}_{\mathrm{CORE}}$, will be higher by the amount IBIAS $\mathrm{VFB} \bullet \mathrm{R}_{\mathrm{VFBK}}$. This condition is shown in Figure 17.

To calculate $\mathrm{R}_{\mathrm{VFBK}}$ the designer must specify the no-load voltage increase above the VID setting ( $\Delta \mathrm{V}_{\text {NO-LOAD }}$ ) and determine the $\mathrm{V}_{\mathrm{FB}}$ bias current. Usually, the no-load voltage increase is specified in the design guide for the processor that is available from the manufacturer. The $\mathrm{V}_{\mathrm{FB}}$ bias current is determined by the value of the resistor from $\mathrm{R}_{\text {OSC }}$ to ground (see Figure in the data sheet for a graph of IBIAS ${ }_{V F B}$ versus R_OSC). The value of $\mathrm{R}_{\mathrm{VFBK}}$ can then be calculated:

$$
\begin{equation*}
\text { RVFBK }=\Delta \mathrm{V}_{\text {NO-LOAD }} / \mathrm{IBIASVFB} \tag{29}
\end{equation*}
$$

Resistor $\mathrm{R}_{\mathrm{DRP}}$ is connected between the $\mathrm{V}_{\mathrm{DRP}}$ and the $\mathrm{V}_{\mathrm{FB}}$ pins. At no-load, the $\mathrm{V}_{\mathrm{DRP}}$ and the $\mathrm{V}_{\mathrm{FB}}$ pins will both be at the DAC voltage so this resistor will conduct zero current. However, at full-load, the voltage at the $\mathrm{V}_{\mathrm{DRP}}$ pin will increase proportional to the output inductor's current while $\mathrm{V}_{\mathrm{FB}}$ will still be regulated to the DAC voltage. Current will be conducted from $\mathrm{V}_{\mathrm{DRP}}$ to $\mathrm{V}_{\mathrm{FB}}$ by $\mathrm{R}_{\mathrm{DRP}}$. This current will be large enough to supply the $\mathrm{V}_{\mathrm{FB}}$ bias current and cause a voltage drop from $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\text {CORE }}$ across $\mathrm{R}_{\mathrm{FBK}}$ - the converter's output voltage will be reduced. This condition is shown in Figure 18.


Figure 18. AVP Circuitry at Full-Load

To determine the value of $R_{D R P}$ the designer must specify the full-load voltage reduction from the VID (DAC) setting ( $\Delta \mathrm{V}_{\text {OUT,FULL-LOAD }}$ ) and predict the voltage increase at the $V_{\text {DRP }}$ pin at full-load. Usually, the full-load voltage reduction is specified in the design guide for the processor that is available from the manufacturer. To predict the voltage increase at the $\mathrm{V}_{\text {DRP }}$ pin at full-load ( $\Delta \mathrm{V}_{\mathrm{DRP}}$ ), the designer must consider the output inductor's resistance $\left(\mathrm{R}_{\mathrm{L}}\right)$, the PCB trace resistance between the current sense points ( $\mathrm{R}_{\mathrm{PCB}}$ ), and the controller IC's gain from the current sense to the $\mathrm{V}_{\text {DRP }}$ pin $\left(\mathrm{G}_{\mathrm{VDRP}}\right)$ :

$$
\begin{equation*}
\Delta V_{D R P}=I O, M A X \cdot\left(R_{L}+R P C B\right) \cdot G V D R P \tag{30}
\end{equation*}
$$

The value of $\mathrm{R}_{\mathrm{DRP}}$ can then be calculated:
RDRP $=\frac{\Delta V_{\text {DRP }}}{\left(\mathrm{IBIASVFB}+\Delta \mathrm{V}_{\text {OUT }}, F U L L-L O A D / R V F B K\right)}$
$\Delta \mathrm{V}_{\text {OUT,FULL-LOAD }}$ is the full-load voltage reduction from the VID (DAC) setting. $\Delta$ VOUT,FULL-LOAD is not the voltage change from the no-load AVP setting.

## 7. Current Sensing

For inductive current sensing, choose the current sense network ( $\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}, \mathrm{n}=1$ or 2 ) to satisfy

$$
\begin{equation*}
\mathrm{RCSn}_{\mathrm{CS}} \cdot \mathrm{CCSn}_{\mathrm{CS}}=\mathrm{Lo} /\left(\mathrm{R}_{\mathrm{L}}+\mathrm{RPCB}\right) \tag{32}
\end{equation*}
$$

For resistive current sensing, choose the current sense network ( $\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}, \mathrm{n}=1$ or 2 ) to satisfy

$$
\begin{equation*}
\mathrm{R}_{\mathrm{CSn}} \cdot \mathrm{C}_{\mathrm{CSn}}=\mathrm{Lo} /\left(\mathrm{R}_{\text {Sense }}\right) \tag{33}
\end{equation*}
$$

This will provide an adequate starting point for $\mathrm{R}_{\mathrm{CSn}}$ and $\mathrm{C}_{\mathrm{CSn}}$. After the converter is constructed, the value of $\mathrm{R}_{\mathrm{CSn}}$ (and/or $\mathrm{C}_{\mathrm{CSn}}$ ) should be fine-tuned in the lab by observing the $\mathrm{V}_{\text {DRP }}$ signal during a step change in load current. Tune
the $\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$ network to provide a "square-wave" at the $\mathrm{V}_{\text {DRP }}$ output pin with maximum rise time and minimal overshoot as shown in Figure 21.


Figure 19. V DRP Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Long (Slow): $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\text {OUT }}$ Respond Too Slowly.


Figure 20. V ${ }_{\text {DRP }}$ Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Too Short (Fast): V


Figure 21. V ${ }_{\text {DRP }}$ Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Optimal: $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\text {OUT }}$ Respond to the Load Current Quickly Without Overshooting.

## 8. Error Amplifier Tuning

After the steady-state (static) AVP has been set and the current sense network has been optimized the Error Amplifier must be tuned. Basically, the gain of the Error Amplifier should be adjusted to provide an acceptable transient response by increasing or decreasing the Error Amplifier's feedback capacitor ( $\mathrm{C}_{\text {AMP }}$ in the Applications Diagram). The bandwidth of the control loop will vary directly with the gain of the error amplifier.


Figure 22. The Value of $\mathrm{C}_{\text {AMP }}$ Is Too High and the Loop Gain/Bandwidth Too Low. COMP Slews Too Slowly Which Results in Overshoot in Vout.

If $\mathrm{C}_{\mathrm{AMP}}$ is too large the loop gain/bandwidth will be low, the COMP pin will slew too slowly, and the output voltage will overshoot as shown in Figure 22. On the other hand, if $\mathrm{C}_{\text {AMP }}$ is too small the loop gain/bandwidth will be high, the COMP pin will slew very quickly and overshoot. Integrator "wind up" is the cause of the overshoot. In this case the output voltage will transition more slowly because COMP
spikes upward as shown in Figure 23. Too much loop gain/bandwidth increase the risk of instability. In general, one should use the lowest loop gain/bandwidth as possible to achieve acceptable transient response - this will insure good stability. If $\mathrm{C}_{\mathrm{AMP}}$ is optimal the COMP pin will slew quickly but not overshoot and the output voltage will monotonically settle as shown in Figure 24.


Figure 23. The Value of $\mathrm{C}_{\mathrm{AMP}}$ Is Too Low and the Loop Gain/Bandwidth Too High. COMP Moves Too Quickly, Which Is Evident from the Small Spike in Its Voltage When the Load Is Applied or Removed. The Output Voltage Transitions More Slowly Because of the COMP Spike.


Figure 24. The Value of $\mathrm{C}_{\text {AMP }}$ Is Optimal. COMP Slews Quickly Without Spiking or Ringing. V Overshoot and Monotonically Settles to Its Final Value.

After the control loop is tuned to provide an acceptable transient response the steady-state voltage ripple on the COMP pin should be examined. When the converter is operating at full, steady-state load, the peak-to-peak voltage ripple on the COMP pin should be less than $20 \mathrm{mV}_{\mathrm{PP}}$ as shown in Figure 25. Less than 10 mV PP is ideal. Excessive ripple on the COMP pin will contribute to output voltage jitter.


Figure 25. At Full-Load (28 A) the Peak-to-Peak Voltage Ripple on the COMP Pin Should Be Less than $\mathbf{2 0} \mathbf{~ m V}$ for a Well-Tuned/Stable Controller. Higher COMP Voltage Ripple Will Contribute to Output Voltage Jitter.

## 9. Current Limit Setting

When the output of the current sense amplifier (CO1 or CO 2 in the block diagram) exceeds the voltage on the $\mathrm{I}_{\mathrm{LIM}}$ pin the part will enter hiccup mode. For inductive sensing, the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor's maximum resistance ( $\mathrm{R}_{\mathrm{LMAX}}$ ). The design must consider the inductor's resistance increase due to current heating and ambient temperature rise. Also, depending on the current sense points, the circuit board may add additional resistance. In general, the temperature coefficient of copper is $+0.39 \%$ per ${ }^{\circ} \mathrm{C}$. If using a current sense resistor ( $\mathrm{R}_{\text {SENSE }}$ ), the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the maximum value of the sense resistor. To set the level of the $\mathrm{I}_{\text {LIM }}$ pin:

$$
\begin{equation*}
\text { VILIM }=(\mathrm{IOUT}, \mathrm{LIM}+\Delta \mathrm{I} \mathrm{Lo} / 2) \cdot \mathrm{R} \cdot \mathrm{GILIM} \tag{34}
\end{equation*}
$$

where:
IOUT,LIM is the current limit threshold of the converter;
$\Delta \mathrm{I}_{\mathrm{Lo}} / 2$ is half the inductor ripple current;
$R$ is either ( $\mathrm{R}_{\text {LMAX }}+\mathrm{R}_{\mathrm{PCB}}$ ) or $\mathrm{R}_{\text {SENSE; }}$
$\mathrm{G}_{\text {ILIM }}$ is the current sense to $\mathrm{I}_{\text {LIM }}$ gain.
For the overcurrent protection to work properly, the current sense time constant (RC) should be slightly larger than the $\mathrm{R}_{\mathrm{L}}$ time constant. If the RC time constant is too fast, during step load changes the sensed current waveform will appear larger than the actual inductor current and will probably trip the current limit at a lower level than expected.

## 10. PWM Comparator Input Voltage

The voltage at the positive input terminal of the PWM comparator (see Figure 9 or 11) is limited by the internal voltage supply of the controller ( 3.3 V ), the size of the internal ramp, and the magnitude of the channel startup offset voltage. To prevent the PWM comparator from saturating, the differential input voltage from $\mathrm{CS}_{\text {REF }}$ to CSn ( $\mathrm{n}=1$ or 2 ) must satisfy the following equation:
VCSREF,MAX $+\mathrm{V}_{\text {COn }}, \mathrm{MAX}+310 \mathrm{mV} \cdot \mathrm{D} \leq 2.45 \mathrm{~V}$
where:

> VCSREF,MAX = Max VID Setting w/ AVP @ Full Load
$\mathrm{V}_{\text {COn }}$ MAX $=\left[\mathrm{V}_{\text {CSn }}-\mathrm{V}_{\text {CSREF }}\right] \cdot$ GCSA,MAX $=(\mathrm{IO}, \mathrm{MAX} / 2+\Delta \mathrm{I} \mathrm{Lo} / 2) \cdot \mathrm{R}_{\text {MAX }}$

- GcsA,MAX
RMAX = RSENSE or (RL,MAX + RPCB,MAX)


## 11. $\mathrm{VTT}_{\mathrm{PGD}}$ Delay Time Setting

The $\mathrm{VTT}_{\mathrm{PGD}}$ signal is pulled LOW a predetermined delay time ( $\mathrm{T}_{\mathrm{D}, \mathrm{VTT}}$ ) after the VTT voltage crosses the VTT Threshold. The $\mathrm{VTT}_{\mathrm{CT}}$ charge current and the capacitor value from the $\mathrm{VTT}_{\mathrm{CT}}$ pin to ground $\left(\mathrm{C}_{\mathrm{VTT}}\right)$ determine the $\mathrm{T}_{\mathrm{D}, \mathrm{VTT}}$ delay time. However, the choice of oscillator frequency and the value of $\mathrm{R}_{\mathrm{OSC}}$ set the $\mathrm{VTT}_{\mathrm{CT}}$ charge current as shown in Figure 4. Therefore, delay time is simply set by the value of $\mathrm{C}_{\mathrm{VTT}}$ according to the following equation:

$$
\begin{equation*}
\text { TD,VTT }=(1 \mathrm{~V}-0.25 \mathrm{~V}) \cdot \mathrm{CVTT} / \mathrm{VTT} \mathrm{CT} \_ \text {Current } \tag{36}
\end{equation*}
$$

## 12. Soft Start Time

The Soft Start time ( $\mathrm{T}_{\mathrm{SS}}$ ) can be calculated from:
TSS $=\left(\right.$ VCOMP $\left.-R_{C M P 1} \cdot I_{C O M P}\right) \cdot$ CCMP2/ICOMP
where:

$$
\begin{aligned}
\text { VCOMP }= & \text { VOUT @ } 0 \text { A }+ \text { Channel_Startup_Offset } \\
& + \text { Int_Ramp }+ \text { GCSA } \cdot \text { Ext_Ramp } / 2
\end{aligned}
$$

$\mathrm{I}_{\text {COMP }}$ is the COMP source current from the data sheet.

## Design Example

## Typical Design Requirements:

$\mathrm{V}_{\mathrm{IN}}=5.0 \mathrm{Vdc}$
$\mathrm{V}_{\text {OUT }}=1.70 \mathrm{Vdc}$ (nominal)
$V_{\text {OUT,RIPPLE }}=10 \mathrm{~m}_{\text {PP }} \max$
VID Range: $1.050 \mathrm{Vdc}-1.825 \mathrm{Vdc}$
$\mathrm{I}_{\mathrm{O}, \mathrm{MAX}}=28 \mathrm{~A}$ at full-load
$\mathrm{I}_{\text {OUT,LIM }}=33 \mathrm{~A}$ min at $50^{\circ} \mathrm{C}$ (shutdown threshold)
$\mathrm{dI}_{\text {IN }} / \mathrm{dt}=0.1 \mathrm{~A} / \mathrm{Hs}^{\max }$
$\mathrm{f}_{\mathrm{SW}}=335 \mathrm{kHz}$
$\eta=81 \%$ minimum
$\mathrm{T}_{\mathrm{A}, \mathrm{MAX}}=60^{\circ} \mathrm{C}$
$\mathrm{T}_{\mathrm{J}, \mathrm{MAX}}=115^{\circ} \mathrm{C}$
$\mathrm{T}_{\mathrm{D}, \mathrm{VTT}}=2.5 \mathrm{~ms}$ (VTT $\mathrm{VGGD}_{\mathrm{PG}}$ delay time)
$\mathrm{T}_{\mathrm{SS}}=6.5 \mathrm{~ms}$ (Soft Start time)
$\Delta \mathrm{V}_{\text {OUT }}$ at no-load (static) $=$
+45 mV from VID setting $=1.745 \mathrm{Vdc}$
$\Delta \mathrm{V}_{\text {OUT }}$ at full-load (static) $=$
-45 mV from VID setting $=1.655 \mathrm{Vdc}$
$\Delta \mathrm{V}_{\text {OUT }}$ at full-load (transient) $=$
-90 mV from VID setting $=1.610 \mathrm{Vdc}$

## 1. Output Capacitor Selection

First, choose a low-cost, low-ESR output capacitor such as the Rubycon 6.3ZA1000M10X16: $6.3 \mathrm{~V}, 1000 \mu \mathrm{~F}, 1.65$ ARMS , $24 \mathrm{~m} \Omega, 10 \times 16 \mathrm{~mm}$. Calculate the minimum number of output capacitors:

$$
\begin{align*}
\text { NOUT,MIN } & =\text { ESR per capacitor } \cdot \frac{\Delta \mathrm{I}_{\mathrm{O}, \mathrm{MAX}}}{\Delta \mathrm{~V}, \mathrm{MAX}}  \tag{1}\\
& =24 \mathrm{~m} \Omega \cdot 28 \mathrm{~A} /(1.745 \mathrm{~V}-1.610 \mathrm{~V}) \\
& =4.987 \text { or } 5 \text { capacitors minimum }(5000 \mu \mathrm{~F})
\end{align*}
$$

## 2. Output Inductor Selection

Calculate the minimum output inductance at $\mathrm{I}_{\mathrm{O}, \mathrm{MAX}}$ according to Equation 3 with $\pm 20 \%$ inductor ripple current ( $\alpha=0.20$ ):

$$
\begin{align*}
\text { LOMIN } & =\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \cdot \mathrm{VOUT}^{\left(\alpha \cdot \mathrm{IO}_{\mathrm{OAX}} \cdot \mathrm{~V}_{\text {IN }} \cdot \mathrm{fSW}\right)}}{}  \tag{3}\\
& =\frac{(5 \mathrm{~V}-1.655 \mathrm{~V}) \cdot 1.655 \mathrm{~V}}{(0.2 \cdot 28 \mathrm{~A} \cdot 5 \mathrm{~V} \cdot 335 \mathrm{kHz})} \\
& =590 \mathrm{nH}
\end{align*}
$$

To save cost, we choose the inexpensive T50-52 core from Micrometals: $33 \mathrm{nH} / \mathrm{N}^{2}, 3.19 \mathrm{~cm} . / t \mathrm{urn}$. At 14 A per phase the permeability of this core will be approximately $80 \%$ of the permeability at 0 A . Therefore, at 0 A we must achieve at least $590 \mathrm{nH} / 0.8$ or 738 nH . Using four turns results in only 528 nH , so we must use five turns of \#16AWG bifilar ( $2 \mathrm{~m} \Omega / \mathrm{ft}$.) to produce 825 nH . This inductor is available as part number CTX22-15401 from Coiltronics.

Use Equation 4 to insure the output voltage ripple will satisfy the design goal with the minimum number of capacitors and the nominal output inductance:

```
VOUT,P-P \(=(\) ESR per cap / NOUT,MIN) .
    \(\left\{\left(\mathrm{VIN}_{\mathrm{IN}}\right.\right.\) - \#Phases \(\left.\cdot \mathrm{V}_{\text {OUT }}\right) \cdot \mathrm{D} /(\) Lomin \(\cdot\) fsw \(\left.)\right\}\)
\(=(24 \mathrm{~m} \Omega / 5)\).
    \(\{(5.0 \mathrm{~V}-2 \cdot 1.7 \mathrm{~V}) \cdot(1.7 \mathrm{~V} / 5.0 \mathrm{~V}) /(825 \mathrm{nH} \cdot 335 \mathrm{kHz})\}\)
\(=(4.8 \mathrm{mQ}) \cdot\{1.97 \mathrm{~A}\}\)
\(=9.45 \mathrm{mV}\)
```

The output voltage ripple will be decreased when output capacitors are added to satisfy transient loading requirements.
We will need the nominal and worst case inductor resistances for subsequent calculations:

$$
\begin{aligned}
R_{\mathrm{L}} & =5 \text { turns } \cdot 3.19 \mathrm{~cm} / \text { turn } \cdot 0.03218 \mathrm{ft} / \mathrm{cm} \cdot 2 \mathrm{~m} \Omega / \mathrm{ft} \\
& =1.03 \mathrm{~m} \Omega
\end{aligned}
$$

The inductor resistance will be maximized when the inductor is "hot" due to the load current and the ambient temperature is high. Assuming a $40^{\circ} \mathrm{C}$ temperature rise of the inductor at full-load and a $25^{\circ} \mathrm{C}$ ambient temperature rise we can calculate:

$$
\begin{aligned}
\mathrm{R}_{\mathrm{L}, \mathrm{MAX}} & =1.03 \mathrm{~m} \Omega \cdot\left[1+0.39 \% /{ }^{\circ} \mathrm{C} \cdot\left(40^{\circ} \mathrm{C}+25^{\circ} \mathrm{C}\right)\right] \\
& =1.29 \mathrm{~m} \Omega
\end{aligned}
$$

## 3. Input Capacitor Selection

Use Equation 5 to determine the average input current to the converter:

$$
\begin{align*}
\mathrm{I}_{\mathrm{I}, \mathrm{AVG}} & =\mathrm{I}_{\mathrm{O}, \mathrm{MAX} \cdot \mathrm{D} / \eta}  \tag{5}\\
& =28 \mathrm{~A} \cdot(1.655 \mathrm{~V} / 5.0 \mathrm{~V}) / 0.81=11.44 \mathrm{~A}
\end{align*}
$$

Next, use Equations 6 to 10:

$$
\begin{align*}
\Delta \mathrm{L}_{\mathrm{Lo}} & =\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V} \text { OUT }\right) \cdot \mathrm{D} /(\mathrm{Lo} \cdot \mathrm{fSW}) \\
& =(5 \mathrm{~V}-1.655 \mathrm{~V}) \cdot \frac{(1.655 \mathrm{~V} / 5.0 \mathrm{~V})}{(825 \mathrm{nH} \cdot 335 \mathrm{kHz})}  \tag{10}\\
& =4.00 \mathrm{App}
\end{align*}
$$

$$
\begin{equation*}
\mathrm{I} \text { Lo,MAX }=\mathrm{I} \mathrm{O}, \mathrm{MAX} / 2+\Delta \mathrm{I} \mathrm{Lo} / 2 \tag{8}
\end{equation*}
$$

$$
=28 \mathrm{~A} / 2+4 \mathrm{App} / 2=16 \mathrm{~A}
$$

$$
\mathrm{ILo}, \mathrm{MIN}=\mathrm{I}, \mathrm{MAX} / 2-\Delta \mathrm{I}_{\mathrm{Lo}} / 2
$$

$$
\begin{equation*}
=28 \mathrm{~A} / 2-4 \mathrm{App} / 2=12 \mathrm{~A} \tag{9}
\end{equation*}
$$

$$
\begin{equation*}
\mathrm{IC}, \mathrm{MAX}=\mathrm{I} \mathrm{Lo}, \mathrm{MAX} / \eta-\mathrm{I} \mathrm{IN}, \mathrm{AVG} \tag{6}
\end{equation*}
$$

$$
=16 \mathrm{~A} / 0.81-11.44 \mathrm{~A}=8.3 \mathrm{~A}
$$

$$
\begin{equation*}
\mathrm{I}_{\mathrm{C}, \mathrm{MIN}}=\mathrm{I} \mathrm{Lo}, \mathrm{MIN} / \eta-\mathrm{I} \mathrm{IN}, \mathrm{AVG} \tag{7}
\end{equation*}
$$

$$
=12 \mathrm{~A} / 0.81-11.44 \mathrm{~A}=3.3 \mathrm{~A}
$$

For the two-phase converter, the input capacitor(s) RMS current is then (Note: $\mathrm{D}=1.655 \mathrm{~V} / 5 \mathrm{~V}=0.331$ ):

$$
\begin{aligned}
\mathrm{I}_{\mathrm{IIN}, \mathrm{RMS}}= & {\left[2 \mathrm { D } \cdot \left(\mathrm{I}_{\mathrm{C}, \mathrm{MIN}^{2}+\mathrm{I}_{\mathrm{C}, \mathrm{MIN} \cdot \Delta \mathrm{I}, \mathrm{IN}}}\right.\right.} \\
& +\Delta \mathrm{I}_{\left.\mathrm{C}, \mathrm{IN}^{2} / 3\right)+\mathrm{I}_{\left.\mathrm{IN}, \mathrm{AVG}^{2} \cdot(1-2 \mathrm{D})\right]^{1 / 2}}^{=}}\left[0.662 \cdot\left(3.3^{2}+3.3 \cdot 5+5^{2} / 3\right)+11.44^{2}\right. \\
& \cdot(1-0.662)]^{1 / 2} \\
= & 8.94 \text { ARMS }
\end{aligned}
$$

At this point, the designer must decide between saving board space by using higher-rated/more costly capacitors or saving cost by using more lower-rated/less costly capacitors. To save board space, we choose the SP (Oscon) series capacitors by Sanyo: $680 \mu \mathrm{~F}, 6.3 \mathrm{~V}, 4.84 \mathrm{~A}_{\text {RMS }}, 13 \mathrm{~m} \Omega$ $10 \times 10.5 \mathrm{~mm}$. We need approximately $8.94 \mathrm{~A} / 4.84 \mathrm{~A}=1.84$ or $\mathrm{N}_{\mathrm{IN}}=2$ capacitors on the input for a conservative design.

## 4. Input Inductor Selection

The input inductor must limit the input current slew rate to less than $0.1 \mathrm{~A} / \mu \mathrm{s}$ during a load transient from 0 to 28 A . A conservative value will be calculated assuming the minimum number of output capacitors ( $\mathrm{N}_{\text {OUT }}=5$ ), two input capacitors ( $\mathrm{N}_{\mathrm{IN}}=2$ ), worst case ESR values for both the input and output capacitors, and a maximum duty cycle $\left(\mathrm{D}=\left(1.825 \mathrm{~V}+45 \mathrm{mV}_{\mathrm{AVP}}\right) / 5.0 \mathrm{~V}_{\mathrm{IN}}=0.374\right)$.

First, use Equation 15 to calculate the voltage across the output inductor due to the 28 A load current being shared equally between the two phases:

$$
\begin{align*}
\Delta \mathrm{V}_{\mathrm{Lo}}= & \mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}, \mathrm{NO}-\mathrm{LOAD}}  \tag{15}\\
& +(\mathrm{IO}, \mathrm{MAX} / 2) \cdot \mathrm{ESROUT} / \mathrm{NOUT} \\
= & 5.0 \mathrm{~V}-1.87 \mathrm{~V}+14 \mathrm{~A} \cdot 23 \mathrm{~m} \Omega / 5 \\
= & 3.194 \mathrm{~V}
\end{align*}
$$

Second, use Equation 16 to determine the rate of current increase in the output inductor:

$$
\begin{align*}
\mathrm{dl} \text { Lo } / \mathrm{dt} & =\Delta \mathrm{V}_{\mathrm{Lo}} / \mathrm{Lo}  \tag{16}\\
& =3.194 \mathrm{~V} / 825 \mathrm{nH}=3.872 \mathrm{~V} / \mu \mathrm{s}
\end{align*}
$$

Finally, use Equations 17 and 18 to calculate the minimum input inductance value:

$$
\begin{align*}
\Delta \mathrm{V}_{\mathrm{Ci}} & =\mathrm{ESR} \mathrm{IN} / \mathrm{N} \text { IN } \cdot \mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt} \cdot \mathrm{D} / \mathrm{fSW}  \tag{17}\\
& =13 \mathrm{~m} \Omega / 2 \cdot 3.872 \mu \mathrm{~s} \cdot 0.374 / 335 \mathrm{kHz} \\
& =28.1 \mathrm{mV} \\
& \begin{aligned}
\mathrm{Li} \mathrm{MIN} & =\Delta \mathrm{V}_{\mathrm{Ci}} / \mathrm{dl}_{\mathrm{IN}} / \mathrm{dt}_{\mathrm{MAX}} \\
& =28.1 \mathrm{mV} / 0.1 \mathrm{~A} / \mu \mathrm{s}=281 \mathrm{nH}
\end{aligned} \tag{18}
\end{align*}
$$

We choose the small, cost effective T30-26 core from Micrometals ( $33.5 \mathrm{nH} / \mathrm{N}^{2}$ ) with \#16 AWG. We need at least
2.89 or 3 turns to achieve the minimum inductance value. With three turns the input inductor will be:

$$
\mathrm{Li}_{\mathrm{i}}=3^{2} \cdot 33.5 \mathrm{nH} / \mathrm{N}^{2}=301 \mathrm{nH}
$$

This inductor is available as part number CTX15-14771 from Coiltronics.


Figure 26. CS5308 Circuitry With Only 5 Rubycon Output Capacitors, 2 Oscon Input Capacitors and a 300 nH Input Inductor. The $\mathrm{dl}_{\mathrm{IN}} / \mathrm{dt}$ of the Input Current ( $0.064 \mathrm{~A} / \mathrm{us}$ ) Is Much Lower Than
Expected (0.1 A/us) Because of Input Voltage Drop and Lower Real ESRs Than Specified in the Capacitors' Data Sheets.

## 5. MOSFET \& Heatsink Selection

The NTB75N03-06 from ON Semiconductor is chosen for both the control and synchronous MOSFET due to its low $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ and low gate-charge requirements. The following parameters are derived from the NTB75N03-06 data sheet:

$$
\begin{aligned}
& \mathrm{R}_{\mathrm{DS}(\mathrm{on})}=5.3 \mathrm{~m} \Omega \\
& \mathrm{Q}_{\mathrm{SW} \text { sitch }}=29 \mathrm{nC} \\
& \mathrm{Q}_{\mathrm{G}}=52 \mathrm{nC} \\
& \mathrm{Q}_{\mathrm{RR}}=23 \mathrm{nC} \\
& \mathrm{Q}_{\mathrm{OS}}=35 \mathrm{nC} \text { (approx.) } \\
& \mathrm{Vf}_{\text {diode }}=0.76 \mathrm{~V} @ 15 \mathrm{~A} \\
& \theta_{\mathrm{JC}}=1.0^{\circ} \mathrm{C} / \mathrm{W} \\
& \mathrm{CS} 5308 \text { Parameters: } \\
& \mathrm{i}_{\mathrm{G}}=1 \mathrm{~A} \\
& \mathrm{~V}_{\mathrm{G}}=10 \mathrm{~V} \\
& \text { t_nonoverlap }=65 \mathrm{~ns}
\end{aligned}
$$

The RMS value of the current in the control MOSFET is calculated from Equation 20 and the previously derived values for $\mathrm{D}, \mathrm{I}_{\text {LMAX }}$, and $\mathrm{I}_{\text {LMIN }}$ at the converter's maximum output current:

$$
\begin{align*}
& \mathrm{IRMS}_{\mathrm{CNTL}}= \sqrt{\mathrm{D}} \cdot\left[\left(\mathrm{ILO}_{\mathrm{LO}} \mathrm{MAX}^{2}+\mathrm{ILO}_{\mathrm{LO}} \mathrm{MAX} \cdot \mathrm{ILo}_{\mathrm{LO}, \mathrm{MIN}}{ }^{(20)}\right.\right.  \tag{20}\\
&+{\left.\left.\mathrm{ILO}, \mathrm{MIN}^{2}\right) / 3\right]^{1 / 2}}^{=} \\
& 0.575 \cdot\left[\left(16^{2}+16 \cdot 12+12^{2}\right) / 3\right]^{1 / 2} \\
&= 8.08 \text { ARMS }
\end{align*}
$$

control MOSFET:

$$
\begin{align*}
& \text { PD,CONTROL }=(\text { IRMS,CNTL } 2 \cdot R \text { DS(on) })  \tag{19}\\
& +\left(\text { Lo,MAX } \cdot \mathrm{Q}_{\text {switch }} / \mathrm{I}_{\mathrm{g}} \cdot \mathrm{~V}_{\text {IN }} \cdot \mathrm{f}_{\mathrm{SW}}\right) \\
& +\left(Q_{\text {Oss }} / 2 \cdot V_{I N} \cdot f_{S W}\right)+\left(V_{\text {IN }} \cdot Q_{R R} \cdot f_{S W}\right) \\
& =\left(8.08^{2} \text { ARMS } \cdot 5.3 \mathrm{~m} \Omega\right) \\
& +(16 \mathrm{~A} \cdot 29 \mathrm{nC} / 1 \mathrm{~A} \cdot 5 \mathrm{~V} \cdot 335 \mathrm{kHz}) \\
& +(35 \mathrm{nC} / 2 \cdot 5 \mathrm{~V} \cdot 335 \mathrm{kHz}) \\
& +(5 \mathrm{~V} \cdot 23 \mathrm{nC} \cdot 335 \mathrm{kHz}) \\
& =0.346 \mathrm{~W}+0.78 \mathrm{~W}+0.03 \mathrm{~W}+0.04 \mathrm{~W} \\
& =1.2 \mathrm{~W}
\end{align*}
$$

The RMS value of the current in the synchronous MOSFET is calculated from Equation 27 and the previously derived values for D , $\mathrm{I}_{\mathrm{Lo}, \mathrm{MAX}}$, and $\mathrm{I}_{\mathrm{Lo}, \mathrm{MIN}}$ at the converter's maximum output current:

$$
\begin{aligned}
& \text { IRMS,SYNCH }=\sqrt{1-\mathrm{D}}
\end{aligned}
$$

$$
\begin{aligned}
& =\sqrt{0.669} \cdot\left[\left(16^{2}+16 \cdot 12+12^{2}\right) / 3\right]^{1 / 2} \\
& =11.5 \text { ARMS }
\end{aligned}
$$

Equation 26 is used to calculate the power dissipation of the synchronous MOSFET:

$$
\begin{align*}
& \mathrm{P}_{\mathrm{D}, \mathrm{SYNCH}}=\left(\mathrm{IRMS}, \mathrm{SYNCH}{ }^{2} \cdot \mathrm{RDS}_{\text {(on) }}\right)  \tag{26}\\
& +\left(\mathrm{Vf}_{\text {diode }} \cdot \mathrm{IO}_{\mathrm{O}} \mathrm{MAX} / 2 \cdot \mathrm{t} \text { nonoverlap } \cdot \mathrm{f} \mathrm{SW}\right) \\
& =\left(11.5^{2} \text { ARMS } \cdot 5.3 \mathrm{~m} \Omega\right) \\
& +(0.76 \mathrm{~V} \cdot 28 \mathrm{~A} / 2 \cdot 65 \mathrm{~ns} \cdot 335 \mathrm{kHz}) \\
& =0.70 \mathrm{~W}+0.23 \mathrm{~W}=0.93 \mathrm{~W}
\end{align*}
$$

Equation 28 is used to calculate the heat sink thermal impedances necessary to maintain less than the specified maximum junction temperatures at $60^{\circ} \mathrm{C}$ ambient:
${ }^{\theta} \mathrm{CNTL}<\left(115-60^{\circ} \mathrm{C}\right) / 1.2 \mathrm{~W}-1.0^{\circ} \mathrm{C} / \mathrm{W}=46^{\circ} \mathrm{C} / \mathrm{W}$
${ }^{\theta}$ SYNCH $<\left(115-60^{\circ} \mathrm{C}\right) / 0.93 \mathrm{~W}-1.0^{\circ} \mathrm{C} / \mathrm{W}=59^{\circ} \mathrm{C} / \mathrm{W}$
If board area permits, a cost effective heatsink could be formed by using a TO-263 mounting pad of at least 1.0$1.5 \mathrm{in}^{2}$ per MOSFET on a single-sided, 1 oz . copper PCB (or 0.5 to $0.75 \mathrm{in}^{2}$ on each side of a two-sided board). If board space must be conserved, AAVID offers clip-on heatsinks for TO-220 thru-hole packages. Examples of these
heatsinks include \#577002 $\left(1^{\prime \prime} \times 0.75^{\prime \prime} \times 0.25^{\prime \prime}, 39^{\circ} \mathrm{C} / \mathrm{W}\right.$ at $1 \mathrm{~W})$ and \#591302 ( $0.75^{\prime \prime} \times 0.5^{\prime \prime} \times 0.5^{\prime \prime}, 34^{\circ} \mathrm{C} / \mathrm{W}$ at 1 W )

## 6. Adaptive Voltage Positioning

First, to achieve the 335 kHz switching frequency, use Figure 3 to determine that a $39 \mathrm{k} \Omega$ resistor is needed for $\mathrm{R}_{\mathrm{OSC}}$. Then, use Figure 4 to find the $\mathrm{V}_{\mathrm{FB}}$ bias current at the corresponding value of R RSC. In this example, the $39 \mathrm{k} \Omega$ $\mathrm{R}_{\mathrm{OSC}}$ resistor results in a $\mathrm{V}_{\mathrm{FB}}$ bias current of approximately $7.0 \mu \mathrm{~A}$. Knowing the $\mathrm{V}_{\mathrm{FB}}$ bias current, one can calculate the required values for $\mathrm{R}_{\mathrm{VFBK}}$ and $\mathrm{R}_{\mathrm{DRP}}$ using Equations 29 through 31.
The no-load position is easily set using Equation 29:

$$
\begin{align*}
\text { RVFBK } & =\Delta \mathrm{V}_{\mathrm{NO}}-\text { LOAD/IBIASVFB }  \tag{29}\\
& =+45 \mathrm{mV} / 7.0 \mu \mathrm{~A} \\
& =6.49 \mathrm{k} \Omega
\end{align*}
$$

For inductive current sensing, the designer must calculate the inductor's resistance ( $\mathrm{R}_{\mathrm{L}}$ ) and approximate any resistance added by the circuit board ( $\mathrm{R}_{\mathrm{PCB}}$ ). We found the inductor's nominal resistance in Section $2(1.03 \mathrm{~m} \Omega)$. In this example, we approximate $0.75 \mathrm{~m} \Omega$ for the circuit board resistance ( $\mathrm{R}_{\mathrm{PCB}}$ ). With this information, Equation 30 can be used to calculate the increase at the $V_{\text {DRP }}$ pin at full load;

$$
\begin{aligned}
\Delta \mathrm{V}_{\mathrm{DRP}} & =\mathrm{I} 0, \mathrm{MAX} \cdot\left(\mathrm{RL}_{\mathrm{L}}+\mathrm{RPCB}^{2}\right) \cdot \operatorname{GVDRP} \\
& =28 \mathrm{~A} \cdot(1.03 \mathrm{~m} \Omega+0.75 \mathrm{~m} \Omega) \cdot 3.2 \mathrm{~V} / \mathrm{V} \\
& =159 \mathrm{mV}
\end{aligned}
$$

$\mathrm{R}_{\mathrm{DRP}}$ can then be calculated from Equation 31:

$$
\begin{align*}
\mathrm{RDRP} & =\frac{\Delta \mathrm{V}_{\mathrm{DRP}}}{(\mathrm{IBIASVFB}+\Delta \mathrm{VOUT}, \mathrm{FULL-LOAD} / \mathrm{RVFBK})}  \tag{31}\\
& =159 \mathrm{mV} /(7.0 \mu \mathrm{~A}+45 \mathrm{mV} / 6.49 \mathrm{k} \Omega) \\
& =11.5 \mathrm{k} \Omega
\end{align*}
$$

## 7. Current Sensing

Choose the current sense network $\left(\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}, \mathrm{n}=1\right.$ or 2$)$ to satisfy

$$
\begin{equation*}
\mathrm{RCSn}_{\mathrm{CS}} \cdot \mathrm{C}_{\mathrm{CSn}}=\mathrm{Lo} /\left(\mathrm{R}_{\mathrm{L}}+\mathrm{RPCB}^{2}\right) \tag{30}
\end{equation*}
$$

The component values determined thus far are $\mathrm{L}_{\mathrm{o}}=825 \mathrm{nH}$, $R_{L}=1.03 \mathrm{~m} \Omega$ and $R_{P C B}=0.75 \mathrm{~m} \Omega$. We choose a convenient value for $\mathrm{C}_{\mathrm{CS} 1}(0.01 \mu \mathrm{~F})$ and solve for $\mathrm{R}_{\mathrm{CS} 1}$ :

$$
\begin{aligned}
\mathrm{RCSn} & =825 \mathrm{nH} /(1.03 \mathrm{~m} \Omega+0.75 \mathrm{~m} \Omega) / 0.01 \mu \mathrm{~F} \\
& =46 \mathrm{k} \Omega \text { or } 50 \mathrm{k} \Omega \text { when rounded up. }
\end{aligned}
$$

After the circuit is constructed, the values of $\mathrm{R}_{\mathrm{CSn}}$ and/or $\mathrm{C}_{\mathrm{CSn}}$ should be tuned to provide a "square-wave" at $\mathrm{V}_{\mathrm{DRP}}$ with minimal overshoot and fast rise time due to a step change in load current as shown in Figures 19-21. Based on experience, the starting value for $\mathrm{R}_{\mathrm{CSn}}$ is probably too low
and will need to be increased to provide a current sense signal similar to those in Figure 21.

Equation 30 will be most accurate for higher quality iron powder core materials such as the -2 or -8 from Micrometals. The permeability of these more expensive cores is relatively constant versus DC current, AC flux density and frequency. Less expensive core materials (such as the -52 from Micrometals) change their characteristics versus DC current, AC flux density, and frequency. The less expensive materials may yield acceptable converter performance if the current sense time constant is set approximatley $2 \times$ longer than anticipated. For example, use approximately twice the resistance $\left(\mathrm{R}_{\mathrm{CSn}}\right)$ or twice the capacitance $\left(\mathrm{C}_{\mathrm{CSn}}\right)$ when using the less expensive core material. If we use -52 material for this design, the value of $\mathrm{R}_{\mathrm{CSn}}$ should be increased to $2 \times 50 \mathrm{k} \Omega$ or $100 \mathrm{k} \Omega$.

## 8. Error Amplifier Tuning

The error amplifier is tuned by adjusting $\mathrm{C}_{\mathrm{AMP}}$ to provide an acceptable full-load transient response as shown in Figures $22-24$. After a value for $\mathrm{C}_{\mathrm{AMP}}$ is chosen, the peak-to-peak voltage ripple on the COMP pin is examined under full-load to insure less than $20 \mathrm{mV}_{\mathrm{PP}}$ as shown in Figure 25.

## 9. Current Limit Setting

The maximum inductor resistance, the maximum PCB resistance, and the maximum current-sense gain as shown in Equation 34 determine the current limit. The maximum current, $\mathrm{I}_{\text {OUT,LIM, }}$ was specified in the design requirements. The maximum inductor resistance occurs at full-load and the highest ambient temperature. This value was found in the "Output Inductor Section" ( $1.58 \mathrm{~m} \Omega$ ). The PCB resistance increases due to the change in ambient temperature:

$$
\begin{aligned}
\mathrm{RPCB}_{\mathrm{MAX}}= & 0.75 \mathrm{~m} \Omega \cdot\left(1+0.39 \% /{ }^{\circ} \mathrm{C} \cdot(60-25)^{\circ} \mathrm{C}\right) \\
= & 0.85 \mathrm{~m} \Omega \\
\mathrm{~V}_{\text {ILIM }}= & \left(\mathrm{I}_{\mathrm{OUT}, \mathrm{LIM}}+\Delta_{\mathrm{L}} / 2\right) \cdot\left(\mathrm{R}_{\mathrm{LMAX}}+\mathrm{RPCB}^{2}, \mathrm{MAX}\right) \\
& \cdot \mathrm{GILIM}^{=} \\
= & (33 \mathrm{~A}+4.0 \mathrm{~A} / 2) \cdot(1.29 \mathrm{~m} \Omega+0.85 \mathrm{~m} \Omega) \\
& \cdot 6.5 \mathrm{~V} / \mathrm{V} \\
= & 0.486 \mathrm{Vdc}
\end{aligned}
$$

Set the voltage at the $\mathrm{I}_{\text {LIM }}$ pin using a resistor divider from the 3.3 V reference output as shown in Figure 27. If the resistor from $\mathrm{I}_{\text {LIM }}$ to GND is chosen as $1 \mathrm{k}\left(\mathrm{R}_{\mathrm{LIM} 2}\right)$, the resistor from $\mathrm{I}_{\mathrm{LIM}}$ to 3.3 V can be calculated from:

$$
\begin{aligned}
\mathrm{R}_{\text {LIM } 1} & =\left(\mathrm{V}_{\text {REF }}-\mathrm{V}_{\text {ILIM }}\right) /\left(\mathrm{V}_{\text {ILIM }} / \mathrm{R}_{\text {LIM } 2}\right) \\
& =(3.3 \mathrm{~V}-0.486 \mathrm{~V}) /(0.486 \mathrm{~V} / 1 \mathrm{k} \Omega) \\
& =5790 \Omega \text { or } 5.76 \mathrm{k} \Omega
\end{aligned}
$$



Figure 27. Setting the Current Limit

## 10. PWM Comparator Input Voltage

Use Equation 35 to check the voltage level to the positive pin of the internal PWM comparators to insure the design will not saturate the comparator at maximum DAC output voltage with $1 \%$ error, AVP at full-load, $100 \%$ duty cycle (D $=1)$, and maximum internal ramp ( 310 mV at $100 \%$ duty-cycle):

$$
\begin{align*}
& \text { VCSREF,MAX = Max VID Setting w/ AVP @ Full-Load } \\
& =1.01 \cdot 1.825 \mathrm{~V}-45 \mathrm{mV}=1.80 \mathrm{~V} \\
& \text { VCOn,MAX } \\
& =(\mathrm{IO}, \mathrm{MAX} / 2+\Delta \mathrm{L} \text { Lo/2 }) \cdot \mathrm{R}_{\mathrm{MAX}} \cdot \operatorname{GCSA}, \mathrm{MAX} \\
& =(28 \mathrm{~A} / 2+4.0 \mathrm{~A} / 2) \cdot(1.29 \mathrm{~m} \Omega+0.82 \mathrm{~m} \Omega) \\
& \text {-3.95 V/V } \\
& =0.133 \mathrm{~V} \\
& \mathrm{~V}_{\text {CSREF, }} \text { MAX }+\mathrm{V}_{\text {COn,MAX }}+310 \mathrm{mV} \cdot \mathrm{D}  \tag{35}\\
& =1.80 \mathrm{~V}+0.133 \mathrm{~V}+310 \mathrm{mV} \\
& =2.243 \mathrm{~V}
\end{align*}
$$

This value is acceptable because it is below the specified maximum of 2.45 V .

## 11. $\mathrm{VTT}_{\mathrm{PGD}}$ Delay Time Setting

To obtain the 335 kHz switching frequency the value of $\mathrm{R}_{\text {OSC }}$ was set to $39 \mathrm{k} \Omega$ in Section 6 . Figure 4 must be used to determine the value of the $\mathrm{VTT}_{\mathrm{CT}}$ Charge Current at this $\mathrm{R}_{\mathrm{OSC}}$ value. In this example, the $39 \mathrm{k} \Omega \mathrm{R}_{\mathrm{OSC}}$ resistor results in a $\mathrm{VTT}_{\mathrm{CT}}$ Charge Current of approximately $26 \mu \mathrm{~A}$. Using Equation 34 and solving for $\mathrm{C}_{\mathrm{VtT}}$ :

$$
\begin{align*}
& \mathrm{T}_{\mathrm{D}, \mathrm{VTT}}=(1 \mathrm{~V}-0.25 \mathrm{~V}) \cdot \mathrm{CVTT}_{\mathrm{V}} / \mathrm{VTT} \mathrm{CT} \text { _Current }  \tag{34}\\
& \mathrm{CVTT}=\mathrm{T}_{\mathrm{D}, \mathrm{VTT}} \cdot \mathrm{VTT} \mathrm{CT} \_ \text {Current } / 0.75 \mathrm{~V} \\
&=2.5 \mathrm{~ms} \cdot 26 \mu \mathrm{~A} / 0.75 \mathrm{~V} \\
&=0.086 \mu \mathrm{~F} \text { or } 0.1 \mu \mathrm{~F}
\end{align*}
$$

## 12. Soft Start Time

To set the Soft Start time we first approximate the COMP voltage at a duty-cycle of $\mathrm{D}=1.745 \mathrm{~V} / 5 \mathrm{~V}=0.349$ :

$$
\begin{aligned}
\mathrm{V}_{\text {COMP }}= & \text { VOUT @ } 0 \mathrm{~A}+\text { Channel_Startup_Offset } \\
& + \text { Int_Ramp } \\
= & 1.745 \mathrm{~V}+0.40 \mathrm{~V}+250 \mathrm{mV} \cdot 0.349 \\
= & 2.232 \mathrm{~V}
\end{aligned}
$$

We then choose a convenient value for $\mathrm{R}_{\mathrm{CMP1}}(5.62 \mathrm{k} \Omega$ ) and solve Equation 37 for $\mathrm{C}_{\mathrm{CMP}}$ :

$$
\begin{aligned}
\mathrm{C} C M P 2 & =\mathrm{TSS} \cdot \frac{\mathrm{ICOMP}}{\left(\mathrm{VCOMP}-\mathrm{RCMP}_{\mathrm{CM}} \cdot \mathrm{ICOMP}\right)} \\
& =6.5 \mathrm{~ms} \cdot \frac{30 \mu \mathrm{~A}}{(2.232 \mathrm{~V}-5.62 \mathrm{k} \Omega \cdot 30 \mu \mathrm{~A})} \\
& =0.0945 \mu \mathrm{~F} \text { or } 0.1 \mu \mathrm{~F}
\end{aligned}
$$



Figure 28. Timing Diagram, VTT Power Good

## CS5322

## Two-Phase Buck Controller with Integrated Gate Drivers and 5-Bit DAC

The CS5322 is a two-phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi-phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced V ${ }^{2 T M}$ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use.

The CS5322 multi-phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in inductor values and a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

## Features

- Enhanced $\mathrm{V}^{2}$ Control Method
- 5-Bit DAC with $1.0 \%$ Accuracy
- Adjustable Output Voltage Positioning
- 4 On-Board Gate Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors, Sense Resistors, or V-S Control
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On-Board Current Sense Amplifiers
- $3.3 \mathrm{~V}, 1.0 \mathrm{~mA}$ Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through Soft Start Pin)
- Power Good Output with Internal Delay


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


SO-28L DW SUFFIX CASE 751F

PIN CONNECTIONS AND MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week
ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS5322GDW28 | SO-28L | 27 Units/Rail |
| CS5322GDWR28 | SO-28L | 1000 Tape \& Reel |



Figure 1. Application Diagram, 12 V to 1.6 V, 35 A Converter

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Operating Junction Temperature | Reflow: (SMD styles only) (Note 1 ) | 230 peak |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature Range | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power for Logic | $\mathrm{V}_{\text {CCL }}$ | 16 V | -0.3 V | N/A | 50 mA |
| Power for GATE(L)1 | $\mathrm{V}_{\text {CCL1 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for GATE(L)2 | $\mathrm{V}_{\text {CCL2 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power GATE(H)1 | $\mathrm{V}_{\mathrm{CCH} 1}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for GATE(H)2 | $\mathrm{V}_{\mathrm{CCH} 2}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | 1.0 mA | 20 mA |
| Soft Start Capacitor | SS | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Compensation Network | COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Input | $V_{F B}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Output for Adjusting Adaptive Voltage Position | $\mathrm{V}_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Frequency Resistor | Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Reference Output | REF | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| High-Side FET Drivers | GATE(H)1-2 | 20 V | $\begin{gathered} -0.3 \vee \mathrm{DC} \\ -2.0 \mathrm{~V} \text { for } 100 \\ \mathrm{~ns} \end{gathered}$ | $\begin{aligned} & 1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} \\ & 200 \mathrm{~mA} \mathrm{DC} \end{aligned}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s}$ 200 mA DC |
| Low-Side FET Drivers | GATE(L)1-2 | 16 V | $\begin{gathered} -0.3 \vee \mathrm{DC} \\ -2.0 \mathrm{~V} \text { for } 100 \\ \mathrm{~ns} \end{gathered}$ | $\begin{aligned} & 1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} \\ & 200 \mathrm{~mA} \mathrm{DC} \end{aligned}$ | $\begin{aligned} & 1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} \\ & 200 \mathrm{~mA} \mathrm{DC} \end{aligned}$ |
| Return for Logic | LGND | N/A | N/A | 50 mA | N/A |
| Return for \#1 Driver | GND1 | 0.3 V | -0.3 V | 2.0 A, $1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Return for \#2 Driver | GND2 | 0.3 V | -0.3 V | 2.0 A, $1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Current Sense for Phases 1-2 | CS1-CS2 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Limit Set Point | ILIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Sense Reference | $\mathrm{CS}_{\text {REF }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage ID DAC Inputs | $\mathrm{V}_{\text {IDO-4 }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$;
$\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{l}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $0=$ Connected to $\mathrm{V}_{\mathrm{SS}} ; 1=$ Open or Pull-up to 3.3 V )


ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, LIIM $\geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output |  |  |  |  |  |
| Power Good Fault Delay | $C S_{\text {REF }}=V_{\text {DAC }}$ to $\mathrm{V}_{\text {DAC }} \pm 15 \%$ | 25 | 50 | 125 | $\mu \mathrm{s}$ |
| Output Low Voltage | $\mathrm{CS}_{\text {REF }}=1.0 \mathrm{~V}, \mathrm{I}_{\text {PWRGD }}=4.0 \mathrm{~mA}$ | - | 0.25 | 0.40 | V |
| Output Leakage Current | $C S_{\text {REF }}=1.45 \mathrm{~V}, \mathrm{PWRGD}=5.5 \mathrm{~V}$ | - | 0.1 | 10 | $\mu \mathrm{A}$ |
| Lower Threshold | \% of Nominal VID Code | -14 | -11 | -8.0 | \% |
| Upper Threshold | \% of Nominal VID Code | 8 | 11 | 14 | \% |

Voltage Feedback Error Amplifier

| $V_{\text {FB }}$ Bias Current (Note 2) | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.9 \mathrm{~V}$ | 9.0 | 10.3 | 11.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.8 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.9 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V}$ COMP Open; DAC $=00000$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V}$ COMP Open; $\mathrm{DAC}=00000$ | - | 0.1 | 0.2 | V |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3 | 60 | 90 | - | dB |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ COMP Capacitor | - | 400 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |

## Soft Start

| Soft Start Charge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 15 | 30 | 50 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Soft Start Discharge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 4.0 | 7.5 | 13 | $\mu \mathrm{~A}$ |
| Hiccup Mode Charge/Discharge Ratio | - | 3.0 | 4.0 | - | - |
| Peak Soft Start Charge Voltage | - | 3.3 | 4.0 | 4.2 | V |
| Soft Start Discharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |

## PWM Comparators

| Minimum Pulse Width | Measured from CSx to GATE(H)X $\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS}_{\mathrm{REF}}\right)=1.0 \mathrm{~V}, \mathrm{~V}(\mathrm{COMP})=1.5 \mathrm{~V}$ <br> 60 mV step applied between $\mathrm{V}_{\mathrm{CSX}}$ and $\mathrm{V}_{\text {CREF }}$ | - | 350 | 515 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Channel Start Up Offset | $\mathrm{V}(\mathrm{CS} 1)=\mathrm{V}(\mathrm{CS} 2)=\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS}_{\mathrm{REF}}\right)=0 \mathrm{~V}$ Measure V(COMP) when GATE(H)1, GATE(H)2, switch high | 0.3 | 0.4 | 0.5 | V |

## GATE(H) and GATE(L)

| High Voltage (AC) | Note 3 Measure $\mathrm{V}_{\text {CCLX }}$ - GATE(L) X or $\mathrm{V}_{\mathrm{CCHX}}-\operatorname{GATE}(\mathrm{H})_{\mathrm{X}}$ | - | 0 | 1.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Note 3 Measure GATE(L) X or GATE(H)X | - | 0 | 0.5 | V |
| Rise Time GATE $(\mathrm{H})_{\mathrm{X}}$ | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Rise Time GATE(L) X | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of ROSC per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, LIIM $\geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATE(H) and GATE(L) |  |  |  |  |  |
| Fall Time GATE(H)X | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V}$; $\mathrm{V}_{\mathrm{CCHX}}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time GATE(L)X | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V}$; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| GATE(H) to GATE(L) Delay | GATE $(\mathrm{H})_{\mathrm{X}}<2.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{L})_{\mathrm{x}}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE(L) to GATE(H) Delay | GATE(L) $\mathrm{x}<2.0 \mathrm{~V}$, GATE $(\mathrm{H})_{\mathrm{x}}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-down | Force $100 \mu \mathrm{~A}$ into GATE Driver with no power applied to $\mathrm{V}_{\mathrm{CCHX}}$ and $\mathrm{V}_{\mathrm{CCLX}}=2.0 \mathrm{~V}$. | - | 1.2 | 1.6 | V |

Oscillator

| Switching Frequency | Measure any phase (RoSC $=32.4 \mathrm{k})$ | 300 | 400 | 500 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | Note 4 Measure any phase (ROSC $=63.4 \mathrm{k})$ | 150 | 200 | 250 | kHz |
| Switching Frequency | Note 4 Measure any phase (ROSC $=16.2 \mathrm{k})$ | 600 | 800 | 1000 | kHz |
| ROsc Voltage | - | - | 1.0 | - | V |
| Phase Delay | - | 165 | 180 | 195 | deg |


| Adaptive Voltage Positioning |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {DRP }}$ Output Voltage to DACOUT Offset | $\begin{gathered} \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\mathrm{REE}}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP} \\ \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{gathered}$ | -15 | - | 15 | mV |
| Maximum V ${ }_{\text {DRP }}$ Voltage | $\begin{aligned} & (C S 1=C S 2)-C_{R E F}=50 \mathrm{mV}, \\ & V_{F B}=C O M P, \text { Measure } V_{D R P}-C O M P \end{aligned}$ | 240 | 310 | 380 | mV |
| Current Sense Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.4 | 3.0 | 3.8 | V/V |


| CS ${ }_{\text {REF }}$ Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.5 | 4.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS1-CS2 Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifiers Gain | - | 2.8 | 3.15 | 3.53 | V/V |
| Current Sense Amp Mismatch | Note 4, $0 \leq\left(C S x-C S_{\text {REF }}\right) \leq 50 \mathrm{mV}$ | -5.0 | - | 5.0 | mV |
| Current Sense Amplifiers Input Common Mode Range Limit | Note 4 | 0 | - | $\mathrm{V}_{\mathrm{CCL}}-2$ | V |
| Current Sense Input to ILIM Gain | $0.25 \mathrm{~V}<\mathrm{I}_{\text {LIM }}<1.20 \mathrm{~V}$ | 5.0 | 6.25 | 8.0 | V/V |
| Current Limit Filter Slew Rate | Note 4 | 4.0 | 10 | 26 | $\mathrm{mV} / \mu \mathrm{s}$ |
| ILIM Bias Current | $0<1$ LIM $<1.0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse by Pulse Current Limit: V(CSx) - V(CS REF $)$ | - | 90 | 105 | 135 | mV |
| Current Share Amplifier Bandwidth | Note 4 | 1.0 | - | - | MHz |

Reference Output

| $V_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{I}\left(\mathrm{V}_{\mathrm{REF}}\right)<1.0 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| :--- | :--- | :--- | :--- | :--- | :---: |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, LIIM $\geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

General Electrical Specifications

| $\mathrm{V}_{\text {CCL }}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 20 | 24.5 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CCL1 }}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 4.0 | 5.5 | mA |
| $\mathrm{V}_{\text {CCL2 }}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 4.0 | 5.5 | mA |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 2.8 | 4.0 | mA |
| $\mathrm{V}_{\mathrm{CCH} 2}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ (no switching) | - | 2.5 | 3.5 | mA |
| $\mathrm{V}_{\text {CCL }}$ Start Threshold | GATEs switching, Soft Start charging | 4.05 | 4.4 | 4.7 | V |
| $\mathrm{V}_{\text {CCL }}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 3.75 | 4.2 | 4.6 | V |
| $V_{\text {CCL }}$ Hysteresis | GATEs not switching, Soft Start not charging | 100 | 200 | 300 | mV |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Start Threshold | GATEs switching, Soft Start charging | 1.8 | 2.0 | 2.2 | V |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 1.55 | 1.75 | 1.90 | V |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Hysteresis | GATEs not switching, Soft Start not charging | 100 | 200 | 300 | mV |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| SO-28L |  |  |
| 1 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 2 | $V_{\text {FB }}$ | Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{OUT}}$. The input current of the $\mathrm{V}_{\mathrm{FB}}$ pin and the resistor value determine output voltage offset for zero output current. Short $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\mathrm{OUT}}$ for no AVP. |
| 3 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to set amount AVP or leave this pin open for no AVP. |
| 4-5 | CS1-CS2 | Current sense inputs. Connect current sense network for the corresponding phase to each input. |
| 6 | CS REF | Reference for Current Sense Amplifiers. To balance input offset voltages between the inverting and noninverting inputs of the Current Sense Amplifiers, connect a resistor between CS REF and the output voltage. The value should be $1 / 3$ of the value of the resistors connected to the CSx pins. |
| 7 | PWRGD | Power Good Output. Open collector output goes low when $\mathrm{CS}_{\text {REF }}$ is out of regulation. |
| 8-12 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID }}$ | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |
| 13 | ILIM | Sets threshold for current limit. Connect to reference through a resistive divider. |
| 14 | REF | Reference output. Decouple with $0.1 \mu \mathrm{~F}$ to LGND. |
| 15 | $\mathrm{V}_{\mathrm{CCH} 2}$ | Power for GATE(H)2. |
| 16 | GATE(H)2 | High side driver \#2. |
| 17 | GND2 | Return for \#2 driver. |
| 18 | GATE(L)2 | Low side driver \#2. |

PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-28L | PIN SYMBOL | FUNCTION |
| 19 | $V_{\text {CCL2 }}$ | Power for GATE(L)2. |
| 20 | SS | Soft Start capacitor pin. The Soft Start capacitor controls both Soft Start time and hiccup mode frequency. The COMP pin is clamped below Soft Start during Start-Up and hiccup mode. |
| 21 | LGND | Return for internal control circuits and IC substrate connection. |
| 22 | $\mathrm{V}_{\mathrm{CCH} 1}$ | Power for GATE(H)1. UVLO Sense for High Side Driver supply connects to this pin. |
| 23 | GATE(H)1 | High side driver \#1. |
| 24 | GND1 | Return \#1 drivers. |
| 25 | GATE(L) 1 | Low side driver \#1. |
| 26 | $\mathrm{V}_{\text {CCL1 }}$ | Power for GATE(L)1. |
| 27 | $\mathrm{V}_{\mathrm{CCL}}$ | Power for internal control circuits. UVLO Sense for Logic connects to this pin. |
| 28 | Rosc | A resistor from this pin to ground sets operating frequency and $\mathrm{V}_{\mathrm{FB}}$ bias current. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Oscillator Frequency


Figure 5. Gate(H) Rise-time vs. Load Capacitance measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 7. Gate(L) Rise-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 4. VFB Bias Current vs. Rosc Value


Figure 6. Gate(H) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 8. Gate(L) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .

## APPLICATIONS INFORMATION

## FIXED FREQUENCY MULTI-PHASE CONTROL

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5322 uses a two-phase, fixed frequency, Enhanced V ${ }^{2}$ architecture. Each phase is delayed $180^{\circ}$ from the previous phase. Normally Gate(H) transitions high at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator and bring Gate(H) low. Once Gate $(\mathrm{H})$ goes low, it will remain low until the beginning of the next oscillator cycle. While Gate(H) is high, the enhanced $\mathrm{V}^{2}$ loop will respond to line and load transients. Once Gate $(\mathrm{H})$ is low, the loop will not respond again until the beginning of the next cycle. Therefore, constant frequency Enhanced $V^{2}$ will typically respond within the off-time of the converter.

The Enhanced $\mathrm{V}^{2}$ architecture measures and adjusts current in each phase. An additional input ( Cx ) for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 9.


Figure 9. Enhanced V ${ }^{2}$ Feedback and Current Sense Scheme

The inductor current is measured across $\mathrm{R}_{\mathrm{S}}$, amplified by CSA and summed with the OFFSET and Output Voltage at the non-inverting input of the PWM comparator. The inductor current provides the PWM ramp and as inductor current increases the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts the cycle with a higher current, the PWM
cycle will terminate earlier providing negative feedback. The CS5322 provides a Cx input for each phase, but the $\mathrm{CS}_{\mathrm{REF}}, \mathrm{V}_{\mathrm{FB}}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{V}_{\mathrm{FB}}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than phases with a smaller current signal.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be only $1 / 2$ of the steady state ramp height plus the OFFSET above the output voltage. If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$
\Delta \mathrm{V}=\mathrm{RS} \times \mathrm{CSA} \text { Gain } \times \Delta \mathrm{I}
$$

The single-phase power stage output impedance is:
Single Stage Impedance $=\Delta \mathrm{V} / \Delta \mathrm{I}=\mathrm{R}_{\mathrm{S}} \times$ CSA Gain.
The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few $\mu$ s of a transient before the feedback loop has repositioned the COMP pin.

The peak output current of each phase can also be calculated from;

$$
I_{\text {pkout }}(\text { per phase })=\frac{\mathrm{V}_{\mathrm{COMP}}-\mathrm{V}_{\mathrm{FB}}-\mathrm{V}_{\text {OFFSET }}}{\mathrm{R}_{\mathrm{S}} \times \mathrm{CSA} \text { Gain }}
$$

Figure 10 shows the step response of a single phase with the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current signal, voltage signal and OFFSET exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the current signal level is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 10. Open Loop Operation

## Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 11. In the diagram L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal the values of R 1 and C 1 are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} 1 \times \mathrm{C} 1$. If this criteria is met the current sense signal will be the same shape as the inductor current, the voltage signal at Cx will represent the instantaneous value of inductor current and the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$.


Figure 11. Lossless Inductive Current Sensing with Enhanced V ${ }^{2}$
When choosing or designing inductors for use with inductive sensing tolerances and temperature, effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be
considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 9.

## Current Sharing Accuracy

PCB traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at the same point for each phase and the connection to the $\mathrm{CS}_{\text {REF }}$ should be made so that no phase is favored. (In some cases, especially with inductive sensing, resistance of the pcb can be useful for increasing the current sense resistance.) The total current sense resistance used for calculations must include any pcb trace between the CS inputs and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier Input Mismatch and the value of the current sense element will determine the accuracy of current sharing between phases. The worst case Current Sense Amplifier Input Mismatch is 5.0 mV and will typically be within 3.0 mV . The difference in peak currents between phases will be the CSA Input Mismatch divided by the current sense resistance. If all current sense elements are of equal resistance a 3.0 mV mismatch with a $2.0 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## Operation at > 50\% Duty Cycle

For operation at duty cycles above $50 \%$ Enhanced V ${ }^{2}$ will exhibit subharmonic oscillation unless a compensation ramp is added to each phase. A circuit like the one on the left side of Figure 12 can be added to each current sense network to implement slope compensation. The value of R1 can be varied to adjust the ramp size.


Figure 12. External Slope Compensation Circuit

## Ramp Size and Current Sensing

Because the current ramp is used for both the PWM ramp and to sense current, the inductor and sense resistor values will be constrained. A small ramp will provide a quick transient response by minimizing the difference over which the COMP pin must travel between light and heavy loads, but a steady state ramp of 25 mV -p or greater is typically required to prevent pulse skipping and minimize pulse width jitter. For resistive current sensing, the combination of the inductor and sense resistor values must be chosen to provide a large enough steady state ramp. For large inductor values the sense resistor value must also be increased.

For inductive current sensing, the RC network must meet the requirement of $L / R_{L}=R \times C$ to accurately sense the $A C$ and DC components of the current the signal. Again the values for L and $\mathrm{R}_{\mathrm{L}}$ will be constrained in order to provide a large enough steady state ramp with a compensated current sense signal. A smaller $L$, or a larger $R_{L}$ than optimum might be required. But unlike resistive sensing, with inductive sensing, small adjustments can be made easily with the values of R and C to increase the ramp size if needed.

If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R} \times \mathrm{C}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R} \times \mathrm{C}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During transients the COMP pin will be required to overshoot along with the current signal in order to maintain the output voltage. The $\mathrm{V}_{\mathrm{DRP}}$ pin will also overshoot during transients and possibly slow the response. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}, \mathrm{R}_{\mathrm{L}}$ $=1.6 \mathrm{~m} \Omega, \mathrm{R} 1=20 \mathrm{k}$ and $\mathrm{C} 1=.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of R1 should be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu$ s time constant. With this compensation the $\mathrm{I}_{\text {LIM }}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 13. Inductive Sensing waveform during a Step with Fast RC Time Constant ( $50 \mu \mathrm{~s} / \mathrm{div}$ )

## Current Limit

Two levels of overcurrent protection are provided. Any time the voltage on a Current Sense pin exceeds CS $_{\text {REF }}$ by more than the Single Phase Pulse by Pulse Current Limit, the PWM comparator for that phase is turned off. This provides fast peak current protection for individual phases. The outputs of all the currents are also summed and filtered to compare an averaged current signal to the voltage on the $\mathrm{I}_{\text {LIM }}$ pin. If this voltage is exceeded, the fault latch trips and the Soft Start capacitor is discharged by a $7.5 \mu \mathrm{~A}$ source until the COMP pin reaches 0.2 V . Then Soft Start begins. The converter will continue to operate in this mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced $V^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET's to shut off and the synchronous MOSFET's to turn on. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is stepped up and set lower than nominal during heavy loads to reduce overshoot when the load current is stepped up. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example; in a 50 A converter a $1.0 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond quickly to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 14. Adaptive Positioning
The CS5322 can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram on page 2387)

To set the no-load positioning, a resistor is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to increase the output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of $\mathrm{R}_{\text {OSC }}$. See Figure 4.

During no load conditions the $\mathrm{V}_{\text {DRP }}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor. When output current increases the $\mathrm{V}_{\text {DRP }}$ pin increases proportionally and the $\mathrm{V}_{\text {DRP }}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to decrease.

The $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\text {DRP }}$ pins take care of the slower and DC voltage positioning. The first few $\mu$ s are controlled primarily by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the ramp
size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.
Note: Large levels of adaptive positioning can cause pulse width jitter.

## Error Amp Compensation

The transconductance error amplifier requires a capacitor between the COMP pin and GND. Use of values less than 1 nF may result in error amp oscillation of several MHz .
The capacitor between the COMP pin and the inverting error amplifier input and the parallel resistance of the $\mathrm{V}_{\mathrm{FB}}$ resistor and the $\mathrm{V}_{\mathrm{DRP}}$ resistor are used to roll off the error amp gain. The gain is rolled off at a high enough frequency to give a quick transient response, but low enough to cross zero dB well below the switching frequency to minimize ripple and noise on the COMP pin.

## UVLO

The CS5322 has undervoltage lockout functions connected to two pins. One, intended for the logic and low-side drivers, with a 4.4 V turn-on threshold is connected to the $\mathrm{V}_{\mathrm{CCL}}$ pin. A second, for the high side drivers, has a 2.0 V threshold and is connected to the $\mathrm{V}_{\mathrm{CCH}} 1$ pin.
The UVLO threshold for the high side drivers was chosen at a low value to allow for flexibility in the part and an input voltage as low as 3.3 V. In many applications this will be disabled or will only check that the applicable supply is on - not that is at a high enough voltage to run the converter.

For the $12 \mathrm{~V}_{\text {IN }}$ converter in the application diagram on page 2387, the UVLO pin for the high side driver is pulled up by the 5.0 V supply (through two diode drops) and the function is not used. The diode between the Soft Start pin near GND and prevents start-up while the 12 V supply is off. In an application where a higher UVLO threshold is necessary a circuit like the one in Figure 15 will lock out the converter until the 12 V supply exceeds 9 V .


Figure 15. External UVLO Circuit

## Soft Start and Hiccup Mode

A capacitor between the Soft Start pin and GND controls Soft Start and hiccup mode slopes. A $0.1 \mu \mathrm{~F}$ capacitor with
the $30 \mu \mathrm{~A}$ charge current will allow the output to ramp up at $0.3 \mathrm{~V} / \mathrm{ms}$ or 1.5 V in 5.0 ms at start-up.

When a fault is detected due to overcurrent or UVLO the converter will enter a low duty cycle hiccup mode. During hiccup mode the converter will not switch from the time a fault is detected until the Soft Start capacitor has discharged below the Soft Start Discharge Threshold and then charged back up above the Channel Start Up Offset.

The Soft Start pin will disable the converter when pulled below 0.3 V .

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically, a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to reroute the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

Voltage feedback should be taken from a point of the output or the output filter that doesn't favor any one phase. If the feedback connection is closer to one inductor than the others the ripple associated with that phase may appear larger than the ripple associated with the other phases and poor current sharing can result.

The current sense signal is typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as switch nodes and gate drive signals. The paths should be matched as well as possible. It is especially important that all current sense signals be picked off at similar points for accurate current sharing. If the current signal is taken from a place other than directly at the inductor any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistance and should be considered in design calculations. Capacitors for the current feedback networks should be placed as close to the current sense pins as practical.

## DESIGN PROCEDURE

## Current Sensing, Power Stage and Output Filter Components

1. Choose the output filter components to meet peak transient requirements. The formula below can be used to provide an approximate starting point for capacitor choice, but will be inadequate to calculate actual values.

$$
\Delta \mathrm{V}_{\mathrm{PEAK}}=(\Delta \mathrm{I} / \Delta \mathrm{T}) \times \mathrm{ESL}+\Delta \mathrm{I} \times \mathrm{ESR}
$$

Ideally the output filter should be simulated with models including ESR, ESL, circuit board parasitics and delays due to switching frequency and converter response. Typically both bulk capacitance (electrolytic, Oscon, etc.,) and low impedance capacitance (ceramic chip) will be required. The bulk capacitance provides "hold up" during the converter response. The low impedance capacitance reduces steady state ripple and bypasses the bulk capacitance during slewing of output current.
2. For inductive current sensing (only) choose the current sense network RC to provide a 25 mV minimum ramp during steady state operation.

$$
\mathrm{R}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}}}{\mathrm{~F} \times \mathrm{C} \times 25 \mathrm{mV}}
$$

Then choose the inductor value and inherent resistance to satisfy $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} \times \mathrm{C}$.
For ideal current sense compensation the ratio of $L$ and $R_{L}$ is fixed, so the values of $L$ and $R_{L}$ will be a compromise typically with the maximum value $\mathrm{R}_{\mathrm{L}}$ limited by conduction losses or inductor temperature rise and the minimum value of L limited by ripple current.
3. For resistive current sensing choose $L$ and $R_{S}$ to provide a steady state ramp greater than 25 mV .

$$
\mathrm{L} / \mathrm{RS}_{\mathrm{S}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{T} \mathrm{ON} / 25 \mathrm{mV}
$$

Again the ratio of $L$ and $R_{L}$ is fixed and the values of L and $\mathrm{R}_{\mathrm{S}}$ will be a compromise.
4. Calculate the high frequency output impedance (ConverterZ) of the converter during transients. This is the impedance of the Output filter ESR in parallel with the power stage output impedance (PwrstgZ) and will indicate how far from the original level ( $\Delta \mathrm{VR}$ ) the output voltage will typically recover to within one switching cycle. For a good transient response $\Delta \mathrm{VR}$ should be less than the peak output voltage overshoot or undershoot.

$$
\begin{array}{r}
\Delta V R=\text { ConverterZ } \times \text { ESR } \\
\text { ConverterZ }=\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+E S R}
\end{array}
$$

where:

$$
\text { PwrstgZ }=\text { RS } \times \text { CSA Gain/2.0 }
$$

Multiply the converterZ by the output current step size to calculate where the output voltage should recover to within the first switching cycle after a transient. If the ConverterZ is higher than the value required to recover to where the adaptive positioning is set the remainder of the recovery will be controlled by the error amp compensation and will typically recover in $10-20 \mu \mathrm{~s}$.

$$
\Delta \mathrm{VR}=\Delta \mathrm{l} \text { OUT } \times \text { ConverterZ }
$$

Make sure that $\Delta \mathrm{VR}$ is less than the expected peak transient for a good transient response.
5. Adjust L and $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ as required to meet the best combination of transient response, steady state output voltage ripple and pulse width jitter.

## Current Limit

When the sum of the Current Sense amplifiers ( $\mathrm{V}_{\text {ITOTAL }}$ ) exceeds the voltage on the $\mathrm{I}_{\text {LIM }}$ pin the part will enter hiccup mode. For inductive sensing the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor resistance (or current sense resistor) at max temperature and max current. To set the level of the $I_{\text {LIM }}$ pin:
6. $\mathrm{V}_{\mathrm{I}(\mathrm{LIM})}=\mathrm{R} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS}$ to ILIM Gain
where:

$$
\mathrm{R} \text { is } \mathrm{R}_{\mathrm{L}} \text { or } \mathrm{R}_{\mathrm{S}}
$$

$\mathrm{I}_{\mathrm{OUT}(\mathrm{LIM})}$ is the current limit threshold.
For the overcurrent to work properly the inductor time constant (L/R) should be $\leq$ the Current sense RC. If the RC is too fast, during step loads the current waveform will appear larger than it is (typically for a few hundred $\mu \mathrm{s}$ ) and may trip the current limit at a level lower than the DC limit.

## Adaptive Positioning

7. To set the amount of voltage positioning below the DAC setting at no load connect a resistor $\left(\mathrm{R}_{\mathrm{V}(\mathrm{FB})}\right)$ between the output voltage and the $\mathrm{V}_{\mathrm{FB}}$ pin. Choose $\mathrm{R}_{\mathrm{V}(\mathrm{FB})}$ as;

$$
R V(F B)=N L \text { Position } / V F B \text { Bias Current }
$$

See Figure 4 for $V_{F B}$ Bias Current.
8. To set the difference in output voltage between no load and full load, connect a resistor $\left(\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}\right)$ between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pins. $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ can be calculated in two steps. First calculate the difference between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pin at full load. (The $\mathrm{V}_{\mathrm{FB}}$ voltage should be the same as the DAC voltage during
closed loop operation.) Then choose the $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ to source enough current across $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ for the desired change in output voltage.

$$
\Delta \mathrm{V} V(\mathrm{DRP})=\mathrm{IOUTFL} \times \mathrm{R} \times \mathrm{CS} \text { to } \mathrm{V}_{\mathrm{DRP}} \text { Gain }
$$

where:
$\mathrm{R}=\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ for one phase;
IOUTFL is the full load output current.

$$
\mathrm{RV}(\mathrm{DRP})=\Delta \mathrm{V}_{\mathrm{DRP}} \times \operatorname{RV}(\mathrm{FB}) / \Delta \mathrm{VOUT}_{\mathrm{OU}}
$$

## Calculate Input Filter Capacitor Current Ripple

The procedure below assumes that phases do not overlap and output inductor ripple current $(\mathrm{P}-\mathrm{P})$ is less than the average output current of one phase.
9. Calculate Input Current
$\mathrm{I}_{\mathrm{IN}}=\frac{\mathrm{V}_{\text {OUT }} \times \mathrm{IOUT}}{\left(\text { Efficiency } \times \mathrm{V}_{\text {IN }}\right)}$
10. Calculate Duty Cycle (per phase).

Duty Cycle $=\frac{\mathrm{VOUT}^{\left(\text {Efficiency } \times \mathrm{V}_{\mathrm{IN}}\right)}}{\left(\begin{array}{ll}\end{array}\right)}$
11. Calculate Apparent Duty Cycle.

## Apparent Duty Cycle $=$ Duty Cycle $\times \#$ of Phases

12. Calculate Input Filter Capacitor Ripple Current. Use the chart in Figure 16 to calculate the normalized ripple current ( $\mathrm{K}_{\mathrm{RMS}}$ ) based on the reciprocal of Apparent Duty Cycle. Then multiply the input current by $K_{\text {RMS }}$ to obtain the Input Filter Capacitor Ripple Current.


Figure 16. Normalized Input Filter Capacitor Ripple Current

## DESIGN EXAMPLE

Choose the component values for a 12 V to $1.6 \mathrm{~V}, 35 \mathrm{~A}$ converter with lossless current sensing, adaptive positioning and a 45 A current limit. The adaptive positioning is chosen 30 mV above the nominal $\mathrm{V}_{\text {OUT }}$ at no load and 40 mV below the no-load position with 35 A out. The peak output voltage transient is 70 mV max during a 32 A step current.

## Current Sensing, Power Stage and

## Output Filter Components

1. Assume $1.5 \mathrm{~m} \Omega$ of output filter ESR.
2. 

$$
\begin{aligned}
& \mathrm{R}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \frac{\mathrm{V}_{\mathrm{OUT}} / \mathrm{V} \mathrm{IN}}{\mathrm{~F} \times \mathrm{C} \times 25 \mathrm{mV}} \\
&=(12-1.6) \times \frac{1.6 / 12}{250 \mathrm{k} \times 0.01 \mu \mathrm{~F} \times 25 \mathrm{mV}} \\
&=22 \mathrm{k} \Omega \\
& \mathrm{~L} / \mathrm{R}_{\mathrm{L}}=.01 \mu \mathrm{~F} \times 20 \mathrm{k} \Omega=200 \mu \mathrm{~s} \\
& \mathrm{Choose} \mathrm{R} \\
& \mathrm{~L}=2.0 \mathrm{~m} \Omega \\
& 2.0 \mathrm{~m} \Omega \times 200 \mu \mathrm{~s}=400 \mathrm{nH} \\
& \text { 4. } \mathrm{n} / \mathrm{a}
\end{aligned}
$$

$$
\begin{aligned}
\text { PwrstgZ } & =R_{L} \times \text { CSA Gain } / 2.0 \\
& =2.0 \mathrm{~m} \Omega \times 3.15 / 2.0=3.1 \mathrm{~m} \Omega
\end{aligned}
$$

ConverterZ $=\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+ \text { ESR }}$

$$
=\frac{3.1 \mathrm{~m} \Omega \times 1.5 \mathrm{~m} \Omega}{3.1 \mathrm{~m} \Omega+1.5 \mathrm{~m} \Omega} \cong 1.0 \mathrm{~m} \Omega
$$

$\Delta V R=1.0 \mathrm{~m} \Omega \times 32 \mathrm{~A}=32 \mathrm{mV}$
5. $\mathrm{n} / \mathrm{a}$

## Current Limit

6. 

$$
\begin{aligned}
\mathrm{V}_{\mathrm{I}(\mathrm{LIM})=}= & \mathrm{R}_{\mathrm{L}} \times \operatorname{IOUT}(\mathrm{LIM}) \\
& \times \mathrm{CS} \text { to ILIM Gain } \\
= & 2.0 \mathrm{~m} \times 45 \mathrm{~A} \times 6.25 \\
= & 562 \mathrm{mV}
\end{aligned}
$$

## Adaptive Positioning

7. 

$$
R V(F B)=\text { NL Position } / V_{F B} \text { Bias Current }
$$

$$
=30 \mathrm{mV} / 6.0 \mu \mathrm{~A}=5.0 \mathrm{k} \Omega
$$

8. 

$$
\begin{aligned}
\Delta V \mathrm{DRP}= & \mathrm{R}_{\mathrm{L}} \times \text { IOUT } \\
& \times \text { Current Sense to VDRP Gain } \\
= & 2.0 \mathrm{~m} \Omega \times 35 \mathrm{~A} \times 3.0 \\
= & 210 \mathrm{mV} \\
\mathrm{RV}(\mathrm{DRP}) & =\Delta \mathrm{V} \mathrm{DRP} \times \mathrm{RV}(\mathrm{FB}) / \Delta \mathrm{V} \text { OUT } \\
= & 210 \mathrm{mV} \times 5.0 \mathrm{k} \Omega / 40 \mathrm{mV} \\
= & 26 \mathrm{k} \Omega
\end{aligned}
$$

9. 

$\mathrm{I}_{\mathrm{IN}}=1.52 \mathrm{~V} \times \frac{41 \mathrm{~A}}{0.85 \times 12 \mathrm{~V} \mathrm{IN}}=6.1 \mathrm{~A}$
10.

Duty Cycle $=\frac{1.52 \mathrm{~V}}{0.85 \times 12 \mathrm{VIN}}=0.15$
11.

Apparent Duty Cycle $=0.15 \times 2.0=0.3$
12.

RMS ripple $=6.1 \mathrm{~A} \times 1.5=9.2 \mathrm{~A}$


Figure 17. 5.0 V only to $1.6 \mathrm{~V}, 35 \mathrm{~A}$

## ADDITIONAL APPLICATION DIAGRAMS



Figure 18. 5.0 V only to 2.5 V Converter

## ADDITIONAL APPLICATION DIAGRAMS



Figure 19. 5.0 V only to 1.2 V Bias to $1.6 \mathrm{~V}, 35 \mathrm{~A}$

PACKAGE THERMAL DATA

| Parameter |  | 28 Lead SO Wide | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 75 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## NCP5322A

## Two-Phase Buck Controller with Integrated Gate Drivers and 5-Bit DAC

The NCP5322A is a second-generation, two-phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi-phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced $V^{2 T M}$ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use. The NCP5322A is a second-generation PWM controller because it optimizes transient response by combining traditional Enhanced $\mathrm{V}^{2}$ with an internal PWM ramp and fast-feedback directly from $V_{\text {CORE }}$ to the internal PWM comparator. These enhancements provide greater design flexibility, facilitate use and reduce output voltage jitter.

The NCP5322A multi-phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in filter size and inductor values with a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

## Features

- Enhanced $V^{2}$ Control Method with Internal Ramp
- Internal PWM Ramp
- Fast-Feedback Directly from $V_{\text {CORE }}$
- 5-Bit DAC with $1.0 \%$ Accuracy
- Adjustable Output Voltage Positioning
- 4 On-Board Gate Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors or Sense Resistors
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On-Board Current Sense Amplifiers
- $3.3 \mathrm{~V}, 1.0 \mathrm{~mA}$ Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through Soft Start Pin)
- Power Good Output with Internal Delay

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SO-28L DW SUFFIX CASE 751F

## PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
$W W, W=$ Work Week

## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP5322ADW | SO-28L | 27 Units/Rail |
| NCP5322ADWR2 | SO-28L | 1000 Tape \& Reel |



## Recommended Components:

L1: Coiltronics P/N CTX15-14771 or T30-26 core with 3T of \#16 AWG
L2: Coiltronics P/N TBD or T50-52B with 5T of \#16 AWG Bifilar
$\mathrm{C}_{\text {Input: }} 3 \times$ Sanyo Oscon 16SP270M ( $270 \mu \mathrm{~F}, 16 \mathrm{~V}, 4.4 \mathrm{~A}_{\text {RMS }}, 18 \mathrm{~m} \Omega$ )
Cout: $10 \times$ Rubycon 16MBZ1500M10x20 ( $1500 \mu \mathrm{~F}, 16 \mathrm{~V}, 13 \mathrm{~m} \Omega$ ) or $8 \times$ Sanyo Oscon 4 SP820M ( $820 \mu \mathrm{~F}, 4 \mathrm{~V}, 12 \mathrm{~m} \Omega)$
C Ceramics: $12 \times$ Panasonic ECJ-3YB0J106K ( $10 \mu \mathrm{~F}, 6.3 \mathrm{~V}$ )
Q1-Q4: ON Semiconductor NTB85N03 ( $28 \mathrm{~V}, 85$ A)
$\mathrm{L}_{\mathrm{vcc}}$ : Murata P/N BLM21P221SG (220 $\Omega$ at 100 MHz )

Figure 1. Application Diagram, 12 V Only to 1.6 V at 45 A, 220 kHz


Recommended Components:
L1: Coiltronics P/N CTX15-14771 or T30-26 core with 3T of \#16 AWG
L2: Coiltronics P/N CTX22-15401 or T50-52 with 5T of \#16 AWG Bifilar
Lvcc: Murata P/N BLM21P221SG ( $220 \Omega$ at 100 MHz )
Q1-Q4: ON Semiconductor NTB85N03 (28 V, 85 A)

Figure 2. Alternate Application Diagram, 5.0 V (with 12 V Bias) to 1.6 V at $45 \mathrm{~A}, 335 \mathrm{kHz}$

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance: Junction-to-Case, R ®JC Junction-to-Ambient, R ®JA |  | $\begin{aligned} & 15 \\ & 75 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Storage Temperature Range |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| JEDEC Moisture Sensitivity |  | Level 2 | - |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Name | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: |
| COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $V_{F B}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $V_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| CS1, CS2 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| CS REF | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| PWRGD | 6.0 V | -0.3 V | 1.0 mA | 8.0 mA |
| VID Pins | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| lıIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| REF | 6.0 V | -0.3 V | 1.0 mA | 20 mA |
| SS | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| $\mathrm{V}_{\text {CCL }}$ | 16 V | -0.3 V | N/A | 50 mA |
| $\mathrm{V}_{\text {cCHx }}$ | 20 V | -0.3 V | N/A | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC |
| $\mathrm{V}_{\text {CCLx }}$ | 16 V | -0.3 V | N/A | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC |
| GATE(H)x | 20 V | $\begin{gathered} -2.0 \mathrm{~V} \text { for } 100 \mathrm{~ns}, \\ -0.3 \vee \mathrm{DC} \end{gathered}$ | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC | $\begin{aligned} & 1.5 \mathrm{~A} \text { for } 1.0 \mu \mathrm{~s}, \\ & 200 \mathrm{mADDC} \end{aligned}$ |
| GATE(L)x | 16 V | $\begin{gathered} -2.0 \mathrm{~V} \text { for } 100 \mathrm{~ns}, \\ -0.3 \vee \mathrm{DC} \end{gathered}$ | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC | 1.5 A for $1.0 \mu \mathrm{~s}$, 200 mA DC |
| GND1, GND2 | 0.3 V | -0.3 V | 2.0 A for $1.0 \mu \mathrm{~s}$, 200 mA DC | N/A |
| LGND | 0 V | 0 V | 50 mA | N/A |

## NCP5322A

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V} ; 4.5 \mathrm{~V}<\right.$
$\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CCL} 1}=\mathrm{V}_{\mathrm{CCL2}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, DAC Code 10000 ( 1.45 V ), $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC

| Accuracy (all codes) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ |  |  | $\pm 1.0$ | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {ID } 4}$ | $V_{\text {ID3 }}$ | $\mathrm{V}_{\text {ID2 }}$ | $\mathrm{V}_{\text {ID1 }}$ | $\mathrm{V}_{\text {ID }}$ |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | - | Fault Mode - Output Off |  |  | V |
| 1 | 1 | 1 | 1 | 0 | - | 1.089 | 1.100 | 1.111 | V |
| 1 | 1 | 1 | 0 | 1 | - | 1.114 | 1.125 | 1.136 | V |
| 1 | 1 | 1 | 0 | 0 | - | 1.139 | 1.150 | 1.162 | V |
| 1 | 1 | 0 | 1 | 1 | - | 1.163 | 1.175 | 1.187 | V |
| 1 | 1 | 0 | 1 | 0 | - | 1.188 | 1.200 | 1.212 | V |
| 1 | 1 | 0 | 0 | 1 | - | 1.213 | 1.225 | 1.237 | V |
| 1 | 1 | 0 | 0 | 0 | - | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 1 | 1 | 1 | - | 1.262 | 1.275 | 1.288 | V |
| 1 | 0 | 1 | 1 | 0 | - | 1.287 | 1.300 | 1.313 | V |
| 1 | 0 | 1 | 0 | 1 | - | 1.312 | 1.325 | 1.338 | V |
| 1 | 0 | 1 | 0 | 0 | - | 1.337 | 1.350 | 1.364 | V |
| 1 | 0 | 0 | 1 | 1 | - | 1.361 | 1.375 | 1.389 | V |
| 1 | 0 | 0 | 1 | 0 | - | 1.386 | 1.400 | 1.414 | V |
| 1 | 0 | 0 | 0 | 1 | - | 1.411 | 1.425 | 1.439 | V |
| 1 | 0 | 0 | 0 | 0 | - | 1.436 | 1.450 | 1.465 | V |
| 0 | 1 | 1 | 1 | 1 | - | 1.460 | 1.475 | 1.490 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.485 | 1.500 | 1.515 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.510 | 1.525 | 1.540 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.535 | 1.550 | 1.566 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.559 | 1.575 | 1.591 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.584 | 1.600 | 1.616 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.609 | 1.625 | 1.641 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.634 | 1.650 | 1.667 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.683 | 1.700 | 1.717 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.708 | 1.725 | 1.742 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.733 | 1.750 | 1.768 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.757 | 1.775 | 1.793 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.782 | 1.800 | 1.818 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.807 | 1.825 | 1.843 | V |
| 0 | 0 | 0 | 0 | 0 | - | 1.832 | 1.850 | 1.869 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 1.00 | 1.25 | 1.50 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID }}$ | 25 | 50 | 100 | k $\Omega$ |
| Pull-up Voltage |  |  |  |  | - | 3.15 | 3.30 | 3.45 | V |

## NCP5322A

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH} 1}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V} ; 4.5 \mathrm{~V}<\right.$ $\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CLL} 1}=\mathrm{V}_{\mathrm{CCL} 2}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, DAC Code 10000 ( 1.45 V ), $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Good Output |  |  |  |  |  |
| Power Good Fault Delay | $C S_{\text {REF }}=$ DAC to DAC $\pm 15 \%$ | 60 | 120 | 240 | $\mu \mathrm{s}$ |
| PWRGD Low Voltage | $\mathrm{CS}_{\text {REF }}=1.0 \mathrm{~V}, \mathrm{IPWRGD}=4.0 \mathrm{~mA}$ | - | 0.25 | 0.40 | V |
| Output Leakage Current | $\mathrm{CS}_{\text {REF }}=1.45 \mathrm{~V}, \mathrm{PWRGD}=5.5 \mathrm{~V}$ | - | 0.1 | 10 | $\mu \mathrm{A}$ |
| Lower Threshold | - | -15 | -12 | -9.0 | \% |
| Upper Threshold | - | 9.0 | 12 | 15 | \% |
| Voltage Feedback Error Amplifier |  |  |  |  |  |
| $V_{\text {FB }}$ Bias Current | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.9 \mathrm{~V}$. Note 2. | 9.0 | 10.3 | 11.5 | $\mu \mathrm{A}$ |
| COMP Source Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.8 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.9 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Clamp Voltage | $\begin{aligned} & \mathrm{SS}=0.25 \mathrm{~V} \text { to } 2.5 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=\mathrm{LGND} ; \\ & \text { Measure COMP } \end{aligned}$ | - | - | SS Voltage | V |
| COMP Max Voltage | COMP Open; $\mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V}$; DAC $=00000$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | COMP Open; $\mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V}$; DAC $=00000$ | - | 0.1 | 0.2 | V |
| Transconductance | $-10 \mu \mathrm{~A}$ < $\mathrm{I}_{\text {COMP }}$ < $+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | M $\Omega$ |
| Open Loop DC Gain | Note 3. | 60 | 90 | - | dB |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ COMP Capacitor | - | 400 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |

## Soft Start

| Soft Start Charge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 15 | 30 | 50 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Soft Start Discharge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 4.0 | 7.5 | 13 | $\mu \mathrm{~A}$ |
| Hiccup Mode Charge/Discharge Ratio | - | 3.0 | 4.0 | - | - |
| Soft Start Clamp Voltage | - | 3.3 | 4.0 | 4.2 | V |
| Soft Start Discharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |

## PWM Comparators

| Minimum Pulse Width | $\mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\text {REF }}$ | - | 350 | 475 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Channel Start Up Offset | $\mathrm{V}(\mathrm{CS} 1)=\mathrm{V}(\mathrm{CS} 2)=\mathrm{V}\left(\mathrm{V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS} \mathrm{S}_{\mathrm{REF}}\right)=0 \mathrm{~V} ;$ <br> Measure $\mathrm{V}(\mathrm{COMP})$ when $\mathrm{GATE}(\mathrm{H}) 1$, <br> GATE $(\mathrm{H}) 2$, switch high | 0.3 | 0.4 | 0.5 | V |

## GATE(H) and GATE(L)

| High Voltage (AC) | $\begin{gathered} \text { Measure } \mathrm{V}_{\mathrm{CCLX}}-\mathrm{GATE}(\mathrm{~L})_{\mathrm{x}} \text { or } \\ \mathrm{V}_{\mathrm{CCHX}}-\mathrm{GATE}(\mathrm{H})_{\mathrm{X}} . \text { Note } 3 . \end{gathered}$ | - | 0 | 1.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low Voltage (AC) | Measure GATE $(\mathrm{L})_{\mathrm{X}}$ or GATE $(\mathrm{H})_{\mathrm{X}}$. Note 3. | - | 0 | 0.5 | V |
| Rise Time GATE $(\mathrm{H})_{\mathrm{X}}$ | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of $\mathrm{R}_{\mathrm{OSC}}$ per Figure 5 .
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C}\right.$; $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH} 1}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V} ; 4.5 \mathrm{~V}<$ $\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CLL} 1}=\mathrm{V}_{\mathrm{CCL} 2}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, DAC Code $10000(1.45 \mathrm{~V}), C_{V C C}=1.0 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATE(H) and GATE(L) |  |  |  |  |  |
| Rise Time GATE(L) X | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time GATE(H)X | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V}$; $\mathrm{V}_{\text {CCHX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time GATE(L)X | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V}$; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| GATE(H)x to GATE(L)x Delay | GATE $(\mathrm{H})_{\mathrm{X}}<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{~L})_{\mathrm{x}}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE(L)x to GATE(H)x Delay | GATE $(\mathrm{L})_{\mathrm{x}}<2.0 \mathrm{~V}$, GATE $(\mathrm{H})_{\mathrm{x}}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-Down | Force $100 \mu \mathrm{~A}$ into GATE with no power applied to $\mathrm{V}_{\mathrm{CCHX}}$ and $\mathrm{V}_{\mathrm{CCLX}}=2.0 \mathrm{~V}$. | - | 1.2 | 1.6 | V |


| Oscillator |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Switching Frequency | Measure any phase ( $\mathrm{R}_{\mathrm{OSC}}=32.4 \mathrm{k}$ ) | 340 | 400 | 460 | kHz |
| Switching Frequency | Measure any phase ( $\mathrm{R}_{\text {OSC }}=63.4 \mathrm{k}$ ). Note 4. | 150 | 200 | 250 | kHz |
| Switching Frequency | Measure any phase ( $\mathrm{R}_{\text {OSC }}=16.2 \mathrm{k}$ ). . .te 4. | 600 | 800 | 1000 | kHz |
| Rosc Voltage | - | - | 1.0 | - | V |
| Phase Delay | - | 165 | 180 | 195 | deg |

## Adaptive Voltage Positioning

| $V_{\text {DRP }}$ Output Voltage to DAC ${ }_{\text {OUT }}$ Offset | $\begin{gathered} \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\mathrm{REF}}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP} \\ \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{gathered}$ | -15 | - | 15 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {DRP }}$ Operating Voltage Range | Measure V ${ }_{\text {DRP }}$ - GND, Note 4. | - | - | 2.3 | V |
| Maximum $\mathrm{V}_{\text {DRP }}$ Voltage | $\begin{aligned} & (\mathrm{CS} 1=\mathrm{CS} 2)-\mathrm{CS} \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COF}=50 \mathrm{mV}, \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | 260 | 330 | 400 | mV |
| Current Sense Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.6 | 3.3 | 4.0 | V/V |


| CS1-CS2 Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.1 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS REF $^{\text {Input Bias Current }}$ | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.3 | 4.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifier Gain | - | 3.15 | 3.5 | 3.9 | V/V |
| Current Sense Amp Mismatch (The Sum of Gain and Offset Errors.) | $0 \leq\left(C S x-C S_{\text {REF }}\right) \leq 50 \mathrm{mV}$. Note 4. | -5.0 | - | 5.0 | mV |
| Current Sense Input to ILIM Gain | $0.25 \mathrm{~V}<\mathrm{I}_{\text {LIM }}<1.00 \mathrm{~V}$ | 5.5 | 6.75 | 8.5 | V/V |
| Current Limit Filter Slew Rate | - | 4.0 | 10 | 26 | $\mathrm{mV} / \mathrm{\mu s}$ |
| ILIM Operating Voltage Range | Note 4. | - | - | 1.3 | V |
| ILIM Bias Current | $0<\mathrm{ILIM}^{\text {< }}$ < 1.0 V | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse-by-Pulse Current Limit | Measure $\mathrm{V}(\mathrm{CSx})-\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)$ that Trips Pulse-by-Pulse Limit | 90 | 105 | 135 | mV |
| Current Share Amplifier Bandwidth | Note 4. | 1.0 | - | - | MHz |

## General Electrical Specifications

| $V_{C C L}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 22 | 26 | mA |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~V}_{\mathrm{CCL} 1}$ or $\mathrm{V}_{\mathrm{CCL2}}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=\operatorname{COMP}$ (no switching) | - | 4.5 | 5.5 | mA |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH} 1}=\mathrm{V}_{\mathrm{CCH} 2}<20 \mathrm{~V} ; 4.5 \mathrm{~V}<\right.$ $\mathrm{V}_{\mathrm{CCL}}=\mathrm{V}_{\mathrm{CLL} 1}=\mathrm{V}_{\mathrm{CCL} 2}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}$, DAC Code $10000(1.45 \mathrm{~V}), C_{V C C}=1.0 \mu \mathrm{~F}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| General Electrical Specifications |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{CCH} 1}$ or $\mathrm{V}_{\mathrm{CCH} 2}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 3.2 | 4.5 | mA |
| $\mathrm{V}_{\text {CCL }}$ Start Threshold | GATEs switching, Soft Start charging | 4.05 | 4.3 | 4.5 | V |
| $\mathrm{V}_{\text {CCL }}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 3.75 | 4.1 | 4.35 | V |
| $\mathrm{V}_{\text {CCL }}$ Hysteresis | GATEs not switching, Soft Start not charging | 100 | 200 | 300 | mV |
| $\mathrm{V}_{\text {CCH } 1}$ Start Threshold | GATEs switching, Soft Start charging | 1.8 | 2.0 | 2.2 | V |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 1.55 | 1.75 | 1.90 | V |
| $V_{\text {CCH1 }}$ Hysteresis | GATEs not switching, Soft Start not charging | 100 | 200 | 300 | mV |


| Reference Output |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{l}\left(\mathrm{V}_{\text {REF }}\right)<1.0 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| Internal Ramp |  |  |  |  |  |
| Ramp Height @ 50\% PWM Duty-Cycle | $\mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\text {REF }}$. | - | 125 | - | mV |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| SO-28L |  |  |
| 1 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 2 | $V_{\text {FB }}$ | Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{OUT}}$. The input current of the $\mathrm{V}_{\mathrm{FB}}$ pin and the resistor value determine output voltage offset for zero output current. Short $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\mathrm{OUT}}$ for no AVP. |
| 3 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to set amount AVP or leave this pin open for no AVP. This pin's maximum working voltage is 2.3 Vdc. |
| 4-5 | CS1-CS2 | Current sense inputs. Connect current sense network for the corresponding phase to each input. The input voltages to these pins must be kept within 105 mV of $\mathrm{CS}_{\text {REF }}$ or pulse-by-pulse current limit will be tripped. |
| 6 | $\mathrm{CS}_{\text {REF }}$ | Reference for Current Sense Amplifiers, input to the Power Good comparators, and fast feedback connection to the PWM comparator. To balance input offset voltages between the inverting and noninverting inputs of the Current Sense Amplifiers, connect a resistor between CS $_{\text {REF }}$ and the output voltage. The value should be $1 / 3$ of the value of the resistors connected to the CSx pins. The input voltage to this pin must not exceed the maximum DAC (VID) setting by more than 100 mV or the internal PWM comparator may saturate. |
| 7 | PWRGD | Power Good Output. Open collector output goes low when $\mathrm{CS}_{\text {REF }}\left(\mathrm{V}_{\text {OUT }}\right)$ is out of regulation. |
| 8-12 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {ID }}$ | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |

## PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| SO-28L | PIN SYMBOL | FUNCTION |
| 13 | ILIM | Sets threshold for current limit. Connect to reference through a resistive divider. This pin's maximum working voltage is 1.3 Vdc . |
| 14 | REF | Reference output. Decouple with $0.1 \mu \mathrm{~F}$ to LGND. |
| 15 | $\mathrm{V}_{\mathrm{CCH} 2}$ | Power for GATE(H)2. |
| 16 | GATE(H)2 | High side driver \#2. |
| 17 | GND2 | Return for \#2 drivers. |
| 18 | GATE(L)2 | Low side driver \#2. |
| 19 | $\mathrm{V}_{\text {CCL2 }}$ | Power for GATE(L)2. |
| 20 | SS | Soft Start capacitor pin. The Soft Start capacitor controls both Soft Start time and hiccup mode frequency. The COMP pin is clamped below Soft Start during Start-Up and hiccup mode. |
| 21 | LGND | Return for internal control circuits and IC substrate connection. |
| 22 | $\mathrm{V}_{\mathrm{CCH} 1}$ | Power for GATE(H)1. UVLO Sense for High Side Driver supply connects to this pin. |
| 23 | GATE(H)1 | High side driver \#1. |
| 24 | GND1 | Return \#1 drivers. |
| 25 | GATE(L) 1 | Low side driver \#1. |
| 26 | $\mathrm{V}_{\text {CCL1 }}$ | Power for GATE(L)1. |
| 27 | $\mathrm{V}_{\text {CCL }}$ | Power for internal control circuits. UVLO Sense for Logic connects to this pin. |
| 28 | Rosc | A resistor from this pin to ground sets operating frequency and $\mathrm{V}_{\mathrm{FB}}$ bias current. |



TYPICAL PERFORMANCE CHARACTERISTICS


Figure 4. Oscillator Frequency vs. Rosc Value


Figure 6. GATE(H) Rise Time vs. Load Capacitance Measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V


Figure 8. GATE(L) Rise Time vs. Load Capacitance Measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V


Figure 5. VFB Bias Current vs. Rosc Value


Figure 7. GATE(H) Fall Time vs. Load Capacitance Measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V


Figure 9. GATE(L) Fall Time vs. Load Capacitance Measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V

## APPLICATIONS INFORMATION

## Overview

The NCP5322A DC/DC controller from ON Semiconductor was developed using the Enhanced $V^{2}$ topology to meet requirements of low voltage, high current loads with fast transient requirements. Enhanced $V^{2}$ combines the original $\mathrm{V}^{2}$ topology with peak current-mode control for fast transient response and current sensing capability. The addition of an internal PWM ramp and implementation of fast-feedback directly from $V_{\text {CORE }}$ has improved transient response and simplified design. The NCP5322A includes Power Good (PWRGD) and MOSFET gate drivers to provide a "fully integrated solution" to simplify design, minimize circuit board area, and reduce overall system cost.

Two advantages of a multi-phase converter over a single-phase converter are current sharing and increased apparent output frequency. Current sharing allows the designer to use less inductance in each phase than would be required in a single-phase converter. The smaller inductor will produce larger ripple currents but the total per phase power dissipation is reduced because the RMS current is lower. Transient response is improved because the control loop will measure and adjust the current faster in a smaller output inductor. Increased apparent output frequency is desirable because the off time and the ripple voltage of the two-phase converter will be less than that of a single-phase converter.

## Fixed Frequency Multi-Phase Control

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The NCP5322A controller uses two-phase, fixed frequency, Enhanced $\mathrm{V}^{2}$ architecture to measure and control
currents in individual phases. Each phase is delayed $180^{\circ}$ from the previous phase. Normally, GATE(H) transitions to a high voltage at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal, the internal ramp and the output voltage ripple trip the PWM comparator and bring $\operatorname{GATE}(\mathrm{H})$ low. Once GATE(H) goes low, it will remain low until the beginning of the next oscillator cycle. While GATE(H) is high, the Enhanced $\mathrm{V}^{2}$ loop will respond to line and load variations. On the other hand, once $\operatorname{GATE}(\mathrm{H})$ is low, the loop can not respond until the beginning of the next PWM cycle. Therefore, constant frequency Enhanced $\mathrm{V}^{2}$ will typically respond to disturbances within the off-time of the converter.
The Enhanced $V^{2}$ architecture measures and adjusts the output current in each phase. An additional input (CSn) for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 10. The triangular inductor current is measured differentially across RS, amplified by CSA and summed with the Channel Startup Offset, the Internal Ramp, and the Output Voltage at the non-inverting input of the PWM comparator. The purpose of the Internal Ramp is to compensate for propagation delays in the NCP5322A. This provides greater design flexibility by allowing smaller external ramps, lower minimum pulse widths, higher frequency operation, and PWM duty cycles above $50 \%$ without external slope compensation. As the sum of the inductor current and the internal ramp increase, the voltage on the positive pin of the PWM comparator rises and terminates the PWM cycle. If the inductor starts a cycle with higher current, the PWM cycle will terminate earlier providing negative feedback. The NCP5322A provides a CSn input for each phase, but the $\mathrm{CS}_{\text {REF }}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{CS}_{\text {REF }}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than a phase with a smaller current signal.


Figure 10. Enhanced $V^{2}$ Control Employing Resistive Current Sensing and Additional Internal Ramp

Enhanced $\mathrm{V}^{2}$ responds to disturbances in $\mathrm{V}_{\text {CORE }}$ by employing both "slow" and "fast" voltage regulation. The internal error amplifier performs the slow regulation. Depending on the gain and frequency compensation set by the amplifier's external components, the error amplifier will typically begin to ramp its output to react to changes in the output voltage in 1-2 PWM cycles. Fast voltage feedback is implemented by a direct connection from $\mathrm{V}_{\text {CORE }}$ to the non-inverting pin of the PWM comparator via the summation with the inductor current, internal ramp, and Offset. A rapid increase in load current will produce a negative offset at $\mathrm{V}_{\text {CORE }}$ and at the output of the summer. This will cause the PWM duty cycle to increase almost instantly. Fast feedback will typically adjust the PWM duty cycle in 1 PWM cycle.

As shown in Figure 10, an internal ramp (nominally 125 mV at a $50 \%$ duty cycle) is added to the inductor current ramp at the positive terminal of the PWM comparator. This additional ramp compensates for propagation time delays from the current sense amplifier (CSA), the PWM comparator, and the MOSFET gate drivers. As a result, the minimum ON time of the controller is reduced and lower duty cycles may be achieved at higher frequencies. Also, the additional ramp reduces the reliance on the inductor current ramp and allows greater flexibility when choosing the output inductor and the $\mathrm{R}_{\mathrm{CSn}} \mathrm{C}_{\mathrm{CSn}}$ ( $\mathrm{n}=1$ or 2 ) time constant of the feedback components from $\mathrm{V}_{\text {CORE }}$ to the CSn pin.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. When the average output current is zero, the COMP pin will be:

$$
\begin{aligned}
\text { VCOMP }= & \text { VOUT @ } 0 \text { A + Channel_Startup_Offset } \\
& + \text { Int_Ramp }+ \text { GCSA } \cdot \text { Ext_Ramp } / 2
\end{aligned}
$$

Int_Ramp is the "partial" internal ramp value at the corresponding duty cycle, Ext_Ramp is the peak-to-peak external steady-state ramp at 0 A, $G_{\text {CSA }}$ is the Current Sense Amplifier Gain (nominally $3.5 \mathrm{~V} / \mathrm{V}$ ), and the Channel Startup Offset is typically 0.40 V . The magnitude of the Ext_Ramp can be calculated from:

$$
\text { Ext_Ramp }=\mathrm{D} \cdot\left(\mathrm{~V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) /\left(\mathrm{RCSn}^{2} \cdot \mathrm{C} \mathrm{CSn} \cdot \mathrm{fSW}\right)
$$

For example, if $\mathrm{V}_{\text {Out }}$ at 0 A is set to 1.630 V with AVP and the input voltage is 12.0 V , the duty cycle ( D ) will be $1.630 / 12.0$ or $13.6 \%$. Int_Ramp will be $125 \mathrm{mV} \bullet 13.6 / 50=$ 34 mV . Realistic values for $\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}$ and $\mathrm{f}_{\mathrm{SW}}$ are $60 \mathrm{k} \Omega$ $0.01 \mu \mathrm{~F}$, and 220 kHz - using these and the previously mentioned formula, Ext_Ramp will be 10.6 mV .

$$
\begin{aligned}
\mathrm{V} \text { COMP }= & 1.630 \mathrm{~V}+0.40 \mathrm{~V}+34 \mathrm{mV} \\
& +3.5 \mathrm{~V} / \mathrm{V} \cdot 10.6 \mathrm{mV} / 2 \\
= & 2.083 \mathrm{Vdc}
\end{aligned}
$$

If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage.

Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as:

$$
\Delta \mathrm{V}=\mathrm{RS} \cdot \mathrm{G} \text { CSA } \cdot \Delta \mathrm{I} \text { OUT }
$$

The single-phase power stage output impedance is:

$$
\text { Single Stage Impedance }=\Delta \mathrm{V}_{\mathrm{OUT}} / \Delta \mathrm{I} \text { OUT }=\mathrm{RS} \cdot \mathrm{GCSA}
$$

The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few microseconds of a transient before the feedback loop has repositioned the COMP pin.

The peak output current can be calculated from:
IOUT,PEAK $=\left(V_{\text {COMP }}-V_{\text {OUT }}-\right.$ Offset $) /\left(\mathrm{RS}_{\text {S }} \cdot \mathrm{GCSA}\right)$
Figure 11 shows the step response of the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides a portion of the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current ramp, the "partial" internal ramp voltage signal and Offset exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the average current signal level (CSn output) is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 11. Open Loop Operation


Figure 12. Enhanced V ${ }^{2}$ Control Employing Lossless Inductive Current Sensing and Internal Ramp

## Inductive Current Sensing

For lossless sensing, current can be sensed across the inductor as shown in Figure 12. In the diagram, L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal, the values of $\mathrm{R}_{\mathrm{CSn}}$ and $\mathrm{C}_{\mathrm{CSn}}$ are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$. If this criteria is met, the current sense signal will be the same shape as the inductor current and the voltage signal at CSn will represent the instantaneous value of inductor current. Also, the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor ( $\mathrm{R}_{\mathrm{S}}$ ).

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 10.

## Current Sharing Accuracy

Printed circuit board (PCB) traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at relatively the same point for each phase and the connection to the $\mathrm{CS}_{\text {REF }}$ pin should be made so that no phase is favored. In some cases, especially with inductive sensing, resistance of the PCB can be useful for increasing the current sense resistance. The total current sense resistance used for calculations must include any PCB trace resistance between the CSn input and the $\mathrm{CS}_{\mathrm{REF}}$ input that carries inductor current.

Current Sense Amplifier (CSA) input mismatch and the value of the current sense component will determine the accuracy of the current sharing between phases. The worst case Current Sense Amplifier input mismatch is $\pm 5.0 \mathrm{mV}$ and will typically be within 3.0 mV . The difference in peak currents between phases will be the CSA input mismatch divided by the current sense resistance. If all current sense components are of equal resistance a 3.0 mV mismatch with a $2.0 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## External Ramp Size and Current Sensing

The internal ramp allows flexibility of current sense time constant. Typically, the current sense $\mathrm{R}_{\mathrm{CSn}} \cdot \mathrm{C}_{\mathrm{CSn}}$ time constant ( $\mathrm{n}=1$ or 2 ) should be equal to or slower than the inductor's time constant. If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC or transient portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During a positive current transient, the COMP pin will be required to undershoot in response to the current signal in order to maintain the output voltage. Similarly, the $\mathrm{V}_{\text {DRP }}$ signal will overshoot which will produce too much transient droop in the output voltage. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.
The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a
positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}, \mathrm{R}_{\mathrm{L}}$ $=1.6 \mathrm{~m} \Omega, \mathrm{R}_{\mathrm{CSn}}=20 \mathrm{k}$ and $\mathrm{C}_{\mathrm{CSn}}=0.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of $\mathrm{R}_{\mathrm{CSn}}$ should be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu \mathrm{~s}$ time constant. With this compensation the $\mathrm{I}_{\text {LIM }}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 13. Inductive Sensing Waveform During a Load Step with Fast RC Time Constant ( $50 \mu \mathrm{~s} / \mathrm{div}$ )

## Current Limit

Two levels of overcurrent protection are provided. First, if the voltage on the Current Sense pins (either CS1 or CS2) exceeds CS $_{\text {REF }}$ by more than a fixed threshold (Single Pulse Current Limit), the PWM comparator is turned off. This provides fast peak current protection for individual phases. Second, the individual phase currents are summed and low-pass filtered to compare an averaged current signal to a user adjustable voltage on the $\mathrm{I}_{\text {LIM }}$ pin. If the $\mathrm{I}_{\text {LIM }}$ voltage is exceeded, the fault latch trips and the Soft Start capacitor is discharged until the Soft-Start pin reaches 0.27 V . Then Soft Start begins. The converter will continue to operate in a low current hiccup mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced $\mathrm{V}^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET to shut OFF and the synchronous (lower) MOSFET to turn ON. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in order to reduce voltage excursions during load transients. Adaptive voltage positioning can reduce peak-to-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is applied. Similarly, the output voltage can be set lower than nominal during heavy loads to reduce overshoot when the load current is removed. For low current applications a droop resistor can provide fast accurate adaptive positioning. However, at high currents the loss in a droop resistor becomes excessive. For example; in a 50 A converter a $1 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 14. Adaptive Positioning
The controller can be configured to adjust the output voltage based on the output current of the converter. (Refer to the application diagram in Figure 1). To set the no-load positioning, a resistor is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to adjust the no-load output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of $\mathrm{R}_{\mathrm{OSC}}$ as shown in the datasheet.

During no load conditions the $\mathrm{V}_{\text {DRP }}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor. When output current increases the $\mathrm{V}_{\mathrm{DRP}}$ pin increases proportionally and the $\mathrm{V}_{\mathrm{DRP}}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to decrease.

The response during the first few microseconds of a load transient are controlled primarily by power stage output impedance and the ESR and ESL of the output filter. The
transition between fast and slow positioning is controlled by the total ramp size and the error amp compensation. If the current signal size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

## Error Amp Compensation \& Tuning

The transconductance error amplifier requires a capacitor ( $\mathrm{C}_{\mathrm{CMP1}}$ in the Applications Diagram) between the COMP pin and GND. This capacitor stabilizes the transconductance error amplifier. Values less than 1 nF may cause oscillations of the COMP voltage. These oscillations will increase the output voltage jitter.

The capacitor ( $\mathrm{C}_{\mathrm{AMP}}$ ) between the COMP pin and the inverting error amplifier input (the $\mathrm{V}_{\mathrm{FB}} \mathrm{pin}$ ) and the parallel combination of the resistors $\mathrm{R}_{\mathrm{FBK} 1}$ and $\mathrm{R}_{\mathrm{DRP} 1}$ determine the bandwidth of the error amplifier. The gain of the error amplifier crosses 0 dB at a high enough frequency to give a quick transient response, but well below the switching frequency to minimize ripple and noise on the COMP pin. A capacitor in parallel with the $\mathrm{V}_{\mathrm{FB}}$ resistor $\left(\mathrm{C}_{\mathrm{FBK} 2}\right)$ adds a zero to boost phase near the crossover frequency to improve loop stability.

Setting-up and tuning the error amplifier is a three step process. First, the no-load and full-load adaptive voltage positioning (AVP) are set using $\mathrm{R}_{\mathrm{FBK} 1}$ and $\mathrm{R}_{\mathrm{DRP} 1}$, respectively. Second, the current sense time constant and error amplifier gain are adjusted with $\mathrm{R}_{\mathrm{CSn}}$ and $\mathrm{C}_{\mathrm{AMP}}$ while monitoring $V_{\text {OUT }}$ during transient loading. Lastly, the peak-to-peak voltage ripple on the COMP pin is examined when the converter is fully loaded to insure low output voltage jitter. The details of this process are covered in the Design Procedure section.

## Undervoltage Lockout (UVLO)

The controller has undervoltage lockout functions connected to two pins. One, intended for the logic and low-side drivers, with approximately a 4.2 V turn-on threshold is connected to the $\mathrm{V}_{\mathrm{CCL}}$ pin. A second, for the high side drivers, with approximately a 1.875 V threshold, is connected to the $\mathrm{V}_{\mathrm{CCH} 1}$ pin.

The UVLO threshold for the high side drivers varies with the part type. In many applications this function will be disabled or will only check that the applicable supply is on - not that is at a high enough voltage to run the converter. See individual datasheets for more information on UVLO.

## Soft Start Enable, and Hiccup Mode

A capacitor between the Soft Start pin and GND controls Soft Start and Hiccup mode slopes. A $0.1 \mu \mathrm{~F}$ capacitor with the $30 \mu \mathrm{~A}$ charge current will allow the output to ramp up at $0.3 \mathrm{~V} / \mathrm{ms}$ or 1.6 V in 5.3 ms at start-up.

When a fault is detected due to an overcurrent condition the converter will enter a low duty cycle hiccup mode. During hiccup mode the converter will not switch from the time a fault is detected until the Soft Start capacitor has
discharged below the Soft Start Discharge Threshold and then charged back up above the Channel Start Up Offset.

The Soft Start pin will disable the converter when pulled below the maximum Soft Start Discharge Threshold (nominally 0.27 V ).

## Power Good (PWRGD)

The open-collector Power Good (PWRGD) pin is driven by a "window-comparator" monitoring V CORE. This comparator will transition HIGH if $\mathrm{V}_{\text {CORE }}$ is within $\pm 12 \%$ of the nominal VID setting. After a $120 \mu \mathrm{~s}$ delay, the comparators output will saturate the open-collector output transistor and the PWRGD pin will be pulled LOW.

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically, a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to route the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.
The current sense signals are typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as the switch node and gate drive signals. If the current signals are taken from a location other than directly at the inductor any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistances and should be considered in design calculations. The capacitors for the current feedback networks should be placed as close to the current sense pins as practical. After placing the NCP5322A control IC, follow these guidelines to optimize the layout and routing:

1. Place the $1 \mu \mathrm{~F}$ power supply bypass (ceramic) capacitors close to their associated pins: $\mathrm{V}_{\mathrm{CCL}}$, $\mathrm{V}_{\mathrm{CCH} 1}$ (and/or $\mathrm{V}_{\mathrm{CCH} 2}$ ), $\mathrm{V}_{\mathrm{CCL} 1}$ (and/or $\mathrm{V}_{\mathrm{CCL} 2}$ ).
2. Place the MOSFETs to minimize the length of the Gate traces. Orient the MOSFETs such that the Drain connections are away from the controller and the Gate connections are closest to the controller.
3. Place the components associated with the internal error amplifier ( $\mathrm{R}_{\mathrm{FBK} 1}, \mathrm{C}_{\mathrm{FBK} 2}, \mathrm{C}_{\mathrm{AMP}}, \mathrm{R}_{\mathrm{CMP} 1}$, $\mathrm{C}_{\mathrm{CMP} 1}, \mathrm{R}_{\mathrm{DRP} 1}$ ) to minimize the trace lengths to the pins $\mathrm{V}_{\mathrm{FB}}, \mathrm{V}_{\mathrm{DRP}}$ and COMP.
4. Place the current sense components $\left(\mathrm{R}_{\mathrm{CS} 1}, \mathrm{R}_{\mathrm{CS} 2}\right.$, $\mathrm{C}_{\mathrm{CS} 1}, \mathrm{C}_{\mathrm{CS} 2}, \mathrm{R}_{\mathrm{CSREF}}, \mathrm{C}_{\text {CSREF }}$ near the CS1, CS2, and $\mathrm{CS}_{\text {REF }}$ pins.
5. Place the frequency setting resistor ( $\mathrm{R}_{\mathrm{OSC}}$ ) close to the $\mathrm{R}_{\text {OSC }}$ pin. The $\mathrm{R}_{\text {OSC }}$ pin is very sensitive to noise. Route noisy traces, such as the SWNODEs and GATE traces, away from the $\mathrm{R}_{\text {OSC }}$ pin and resistor.
6. Place the Soft Start capacitor $\left(\mathrm{C}_{\mathrm{SS}}\right)$ near the Soft Start pin.
7. Place the MOSFETs and output inductors to reduce the size of the noisy SWNODEs. There is a tradeoff between reducing the size of the SWNODEs for noise reduction and providing adequate heat-sinking for the synchronous MOSFETs.
8. Place the input inductor and input capacitor(s) near the Drain of the control (upper) MOSFETs. There is a trade-off between reducing the size of this node to save board area and providing adequate heat-sinking for the control MOSFETs.
9. Place the output capacitors (electrolytic and ceramic) close to the processor socket or output connector.
10. The trace from the SWNODEs to the current sense components ( $\mathrm{R}_{\mathrm{CS} 1}, \mathrm{R}_{\mathrm{CS} 2}$ ) will be very noisy. Route this away from more sensitive, low-level traces. The Ground layer can be used to help isolate this trace.
11. The Gate traces are very noisy. Route these away from more sensitive, low-level traces. Keep each Gate signal on one layer and insure that there is an uninterrupted return path directly below the Gate trace. The Ground layer can be used to help isolate these traces.
12. Don't "daisy chain" connections to Ground from one via. Allow each connection to Ground to have its own via as close to the component as possible.
13. Use a slot in the ground plane from the bulk output capacitors back to the input power connector to prevent high currents from flowing beneath the control IC. This slot should extend length-wise under the control IC and separate the connections to "signal ground" and "power ground." Examples of signal ground include the capacitors at COMP, CS $_{\text {REF }}$, Soft-Start (SS), $\mathrm{V}_{\mathrm{CCL}}$, and REF, the resistors at $\mathrm{R}_{\mathrm{OSC}}$ and $\mathrm{I}_{\mathrm{LIM}}$, and the LGND pin to the controller. Examples of power ground include the capacitors to $\mathrm{V}_{\mathrm{CCH} 1}$ (and/or $\mathrm{V}_{\mathrm{CCH} 2}$ ) and $\mathrm{V}_{\mathrm{CCL} 1}$ (and/or $\mathrm{V}_{\mathrm{CCL} 2}$ ), the Source of the synchronous MOSFET, and the GND1 and GND2 pins of the controller.
14. The $\mathrm{CS}_{\text {REF }}$ sense point should be equidistant between the output inductors to equalize the PCB
resistance added to the current sense paths. This will insure acceptable current sharing. Also, route the $\mathrm{CS}_{\text {REF }}$ connection away from noisy traces such as the SWNODEs and GATE traces. If noise from the SWNODEs or GATE signals capacitively couples to the $\mathrm{CS}_{\text {REF }}$ trace the external ramps will be very noisy and voltage jitter will result.
15. Ideally, the SWNODEs are exactly the same shape and the current sense points (connections to $\mathrm{R}_{\mathrm{CS} 1}$ and $\mathrm{R}_{\mathrm{CS} 2}$ ) are made at identical locations to equalize the PCB resistance added to the current sense paths. This will help to insure acceptable current sharing.
16. Place the $0.1 \mu \mathrm{~F}$ ceramic capacitors, $\mathrm{C}_{\mathrm{Q} 1}$ and $\mathrm{C}_{\mathrm{Q} 2}$, close to the drains of the MOSFETs Q1 and Q2, respectively.

## Design Procedure

## 1. Output Capacitor Selection

The output capacitors filter the current from the output inductor and provide a low impedance for transient load current changes. Typically, microprocessor applications will require both bulk (electrolytic, tantalum) and low impedance, high frequency (ceramic) types of capacitors. The bulk capacitors provide "hold up" during transient loading. The low impedance capacitors reduce steady-state ripple and bypass the bulk capacitance when the output current changes very quickly. The microprocessor manufacturers usually specify a minimum number of ceramic capacitors. The designer must determine the number of bulk capacitors.

Choose the number of bulk output capacitors to meet the peak transient requirements. The formula below can be used to provide a starting point for the minimum number of bulk capacitors ( $\mathrm{N}_{\text {OUT,MIN }}$ ):

$$
\begin{equation*}
\text { NOUT,MIN }=\text { ESR per capacitor } \cdot \frac{\Delta \mathrm{I}_{\mathrm{O}, \mathrm{MAX}}}{\Delta \mathrm{~V}_{\mathrm{O}, \mathrm{MAX}}} \tag{1}
\end{equation*}
$$

In reality, both the ESR and ESL of the bulk capacitors determine the voltage change during a load transient according to:
$\Delta \mathrm{V}_{\mathrm{O}, \mathrm{MAX}}=\left(\Delta \mathrm{I}_{\mathrm{O}, \mathrm{MAX}} / \Delta \mathrm{t}\right) \cdot \mathrm{ESL}+\Delta \mathrm{I}_{\mathrm{O}, \mathrm{MAX}} \cdot \mathrm{ESR}$
Unfortunately, capacitor manufacturers do not specify the ESL of their components and the inductance added by the PCB traces is highly dependent on the layout and routing. Therefore, it is necessary to start a design with slightly more than the minimum number of bulk capacitors and perform transient testing or careful modeling/simulation to determine the final number of bulk capacitors.

## 2. Output Inductor Selection

The output inductor may be the most critical component in the converter because it will directly effect the choice of other components and dictate both the steady-state and
transient performance of the converter. When selecting an inductor the designer must consider factors such as DC current, peak current, output voltage ripple, core material, magnetic saturation, temperature, physical size, and cost (usually the primary concern).

In general, the output inductance value should be as low and physically small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, too low an inductance value will result in very large ripple currents in the power components (MOSFETs, capacitors, etc) resulting in increased dissipation and lower converter efficiency. Also, increased ripple currents will force the designer to use higher rated MOSFETs, oversize the thermal solution, and use more, higher rated input and output capacitors - the converter cost will be adversely effected.

One method of calculating an output inductor value is to size the inductor to produce a specified maximum ripple current in the inductor. Lower ripple currents will result in less core and MOSFET losses and higher converter efficiency. Equation 3 may be used to calculate the minimum inductor value to produce a given maximum ripple current $(\alpha)$ per phase. The inductor value calculated by this equation is a minimum because values less than this will produce more ripple current than desired. Conversely, higher inductor values will result in less than the maximum ripple current.

$$
\begin{equation*}
\text { LOMIN }=\frac{\left(V_{\text {IN }}-V_{\text {OUT }}\right) \cdot V_{\text {OUT }}}{\left(\alpha \cdot I_{O, M A X ~} \cdot \mathrm{~V}_{\text {IN }} \cdot \mathrm{fS}^{2}\right)} \tag{3}
\end{equation*}
$$

$\alpha$ is the ripple current as a percentage of the maximum output current per phase ( $\alpha=0.15$ for $\pm 15 \%, \alpha=0.25$ for $\pm 25 \%$, etc). If the minimum inductor value is used, the inductor current will swing $\pm \alpha \%$ about its value at the center ( $1 / 2$ the DC output current for a two-phase converter). Therefore, for a two-phase converter, the inductor must be designed or selected such that it will not saturate with a peak current of $(1+\alpha) \bullet I_{O, M A X} / 2$.

The maximum inductor value is limited by the transient response of the converter. If the converter is to have a fast transient response then the inductor should be made as small as possible. If the inductor is too large its current will change too slowly, the output voltage will droop excessively, more bulk capacitors will be required, and the converter cost will be increased. For a given inductor value, its interesting to determine the times required to increase or decrease the current.

For increasing current:

$$
\begin{equation*}
\Delta \mathrm{t} \operatorname{INC}=\mathrm{Lo} \cdot \Delta \mathrm{I} \mathrm{O} /\left(\mathrm{V} \text { IN }-\mathrm{V}_{\mathrm{OUT}}\right) \tag{3.1}
\end{equation*}
$$

For decreasing current:

$$
\begin{equation*}
\Delta \mathrm{t} \mathrm{DEC}=\mathrm{Lo} \cdot \Delta \mathrm{I}_{\mathrm{O}} /\left(\mathrm{V}_{\mathrm{OUT}}\right) \tag{3.2}
\end{equation*}
$$

For typical processor applications with output voltages less than half the input voltage, the current will be increased much more quickly than it can be decreased. It may be more
difficult for the converter to stay within the regulation limits when the load is removed than when it is applied - excessive overshoot may result.

The output voltage ripple can be calculated using the output inductor value derived in this Section (Lomin), the number of output capacitors (NOUT,MIN) and the per capacitor ESR determined in the previous Section:

$$
\begin{align*}
& \text { VOUT,P-P }=(\text { ESR per cap } / \text { NOUT,MIN }) \cdot  \tag{4}\\
& \{(\text { VIN }- \text { \#Phases } \cdot \text { VOUT }) \cdot \mathrm{D} /(\text { LoMIN } \cdot \text { fSW })\}
\end{align*}
$$

This formula assumes steady-state conditions with no more than one phase on at any time. The second term in Equation 4 is the total ripple current seen by the output capacitors. The total output ripple current is the "time summation" of the two individual phase currents that are 180 degrees out-of-phase. As the inductor current in one phase ramps upward, current in the other phase ramps downward and provides a canceling of currents during part of the switching cycle. Therefore, the total output ripple current and voltage are reduced in a multi-phase converter.

## 3. Input Capacitor Selection

The choice and number of input capacitors is primarily determined by their voltage and ripple current ratings. The designer must choose capacitors that will support the worst case input voltage with adequate margin. To calculate the number of input capacitors one must first determine the total RMS input ripple current. To this end, begin by calculating the average input current to the converter:

$$
\begin{equation*}
I_{I N, A V G}=I O, M A X \cdot D / \eta \tag{5}
\end{equation*}
$$

where:
D is the duty cycle of the converter, $\mathrm{D}=\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}}$. $\eta$ is the specified minimum efficiency.
$\mathrm{I}_{\mathrm{O}, \text { MAX }}$ is the maximum converter output current.
The input capacitors will discharge when the control FET is ON and charge when the control FET is OFF as shown in Figure 15.


Figure 15. Input Capacitor Current for a Two-Phase Converter

The following equations will determine the maximum and minimum currents delivered by the input capacitors:

$$
\begin{align*}
\mathrm{I}_{\mathrm{C}, \mathrm{MAX}} & =\mathrm{I}_{\mathrm{Lo}}, \mathrm{MAX} / \eta-\mathrm{I}_{\mathrm{IN}, \mathrm{AVG}}  \tag{6}\\
\mathrm{I}_{\mathrm{C}, \mathrm{MIN}} & =\mathrm{I}_{\mathrm{Lo}, \mathrm{MIN} / \eta}-\mathrm{I}_{\mathrm{IN}, \mathrm{AVG}} \tag{7}
\end{align*}
$$

$\mathrm{I}_{\text {Lo,MAX }}$ is the maximum output inductor current:

$$
\begin{equation*}
\mathrm{I} \mathrm{Lo}, \mathrm{MAX}=\mathrm{I}, \mathrm{MAX} / 2+\Delta \mathrm{I}_{\mathrm{Lo}} / 2 \tag{8}
\end{equation*}
$$

$\mathrm{I}_{\text {Lo,MIN }}$ is the minimum output inductor current:

$$
\begin{equation*}
\mathrm{ILO}, \mathrm{MIN}=\mathrm{I}, \mathrm{MAX} / 2-\Delta \mathrm{I} \mathrm{Lo} / 2 \tag{9}
\end{equation*}
$$

$\Delta \mathrm{I}_{\text {Lo }}$ is the peak-to-peak ripple current in the output inductor of value Lo:

$$
\begin{equation*}
\Delta_{\mathrm{Lo}}=\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \cdot \mathrm{D} /\left(\mathrm{Lo} \cdot \mathrm{f}_{\mathrm{SW}}\right) \tag{10}
\end{equation*}
$$

For the two-phase converter, the input capacitor(s) RMS current is then:

$$
\begin{align*}
\mathrm{ICIN}, \mathrm{RMS}= & {\left[2 \mathrm { D } \cdot \left(\mathrm{IC}, \mathrm{MIN}^{2}+\mathrm{I}_{\mathrm{C}, \mathrm{MIN} \cdot \Delta \mathrm{IC}, \mathrm{IN}}\right.\right.}  \tag{11}\\
& +\Delta \mathrm{I}_{\left.\left.\mathrm{C}, \mathrm{IN}^{2} / 3\right)+\mathrm{IIN}_{2}, \mathrm{AVG}^{2} \cdot(1-2 \mathrm{D})\right]^{1 / 2}}
\end{align*}
$$

Select the number of input capacitors ( $\mathrm{N}_{\text {IN }}$ ) to provide the RMS input current ( $\mathrm{I}_{\mathrm{CIN}, \mathrm{RMS}}$ ) based on the RMS ripple current rating per capacitor ( $\mathrm{I}_{\text {RMS,RATED }}$ ):
NIN = ICIN,RMS/IRMS,RATED

For a two-phase converter with perfect efficiency ( $\eta=1$ ), the worst case input ripple-current will occur when the converter is operating at a $25 \%$ duty cycle. At this operating point, the parallel combination of input capacitors must support an RMS ripple current equal to $25 \%$ of the converter's DC output current. At other duty cycles, the ripple-current will be less. For example, at a duty cycle of either $10 \%$ or $40 \%$, the two-phase input ripple-current will be approximately $20 \%$ of the converter's DC output current.

In general, capacitor manufacturers require derating to the specified ripple-current based on the ambient temperature. More capacitors will be required because of the current
derating. The designer should be cognizant of the ESR of the input capacitors. The input capacitor power loss can be calculated from:

$$
\begin{equation*}
\text { PCIN }=\text { ICIN,RMS }{ }^{2} \cdot \text { ESR_per_capacitor/NIN } \tag{13}
\end{equation*}
$$

Low ESR capacitors are recommended to minimize losses and reduce capacitor heating. The life of an electrolytic capacitor is reduced $50 \%$ for every $10^{\circ} \mathrm{C}$ rise in the capacitor's temperature.

## 4. Input Inductor Selection

The use of an inductor between the input capacitors and the power source will accomplish two objectives. First, it will isolate the voltage source and the system from the noise generated in the switching supply. Second, it will limit the inrush current into the input capacitors at power up. Large inrush currents will reduce the expected life of the input capacitors. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients.
The worst case input current slew rate will occur during the first few PWM cycles immediately after a step-load change is applied as shown in Figure 16. When the load is applied, the output voltage is pulled down very quickly. Current through the output inductors will not change instantaneously so the initial transient load current must be conducted by the output capacitors. The output voltage will step downward depending on the magnitude of the output current ( $\mathrm{I}_{\mathrm{O}, \mathrm{MAX}}$ ), the per capacitor ESR of the output capacitors (ESR OUT ), and the number of the output capacitors ( $\mathrm{N}_{\text {OUT }}$ ) as shown in Figure 16. Assuming the load current is shared equally between the two phases, the output voltage at full, transient load will be:

$$
\begin{aligned}
& \text { VOUT,FULL-LOAD }= \\
& \text { VOUT,NO-LOAD - (IO,MAX/2) } \cdot \text { ESROUT/NOUT }
\end{aligned}
$$



Figure 16. Calculating the Input Inductance

When the control MOSFET (Q1 in Figure 16) turns ON, the input voltage will be applied to the opposite terminal of the output inductor (the SWNODE). At that instant, the voltage across the output inductor can be calculated as:

$$
\begin{align*}
\Delta V_{\text {Lo }}= & V_{I N}-V_{\text {OUT }, \text { FULL-LOAD }}  \tag{15}\\
= & V_{I N}-V_{O U T, N O-L O A D} \\
& +\left(I_{O, M A X / 2)}\right) \cdot \text { ESROUT/NOUT }
\end{align*}
$$

The differential voltage across the output inductor will cause its current to increase linearly with time. The slew rate of this current can be calculated from:

$$
\begin{equation*}
\mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt}=\Delta \mathrm{V}_{\mathrm{Lo}} / \mathrm{Lo} \tag{16}
\end{equation*}
$$

Current changes slowly in the input inductor so the input capacitors must initially deliver the vast majority of the input current. The amount of voltage drop across the input capacitors $\left(\Delta \mathrm{V}_{\mathrm{Ci}}\right)$ is determined by the number of input capacitors $\left(\mathrm{N}_{\mathrm{IN}}\right)$, their per capacitor ESR $\left(\mathrm{ESR}_{\mathrm{IN}}\right)$, and the current in the output inductor according to:

$$
\begin{align*}
\Delta \mathrm{V}_{\mathrm{Ci}} & =\mathrm{ESR}_{\mathrm{IN}} / \mathrm{N}_{\mathrm{IN}} \cdot \mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt} \cdot \mathrm{tON}  \tag{17}\\
& =\mathrm{ESR}_{\mathrm{IN}} / \mathrm{N}_{\mathrm{IN}} \cdot \mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt}^{2} \cdot \mathrm{D} / \mathrm{f} \mathrm{SW}
\end{align*}
$$

Before the load is applied, the voltage across the input inductor $\left(\mathrm{V}_{\mathrm{Li}}\right)$ is very small - the input capacitors charge to the input voltage, $\mathrm{V}_{\mathrm{IN}}$. After the load is applied the voltage drop across the input capacitors, $\Delta \mathrm{V}_{\mathrm{Ci}}$, appears across the input inductor as well. Knowing this, the minimum value of the input inductor can be calculated from:

$$
\begin{align*}
& \text { Limin }=\mathrm{V}_{\mathrm{Li}} / \text { dIIN/dtMAX }  \tag{18}\\
& =\Delta \mathrm{V}_{\mathrm{Ci}} / \mathrm{dlin}_{\mathrm{I}} / \mathrm{dt}_{\mathrm{MAX}}
\end{align*}
$$

$\mathrm{dI}_{\mathrm{IN}} / \mathrm{dt}_{\text {MAX }}$ is the maximum allowable input current slew rate.

The input inductance value calculated from Equation 18 is relatively conservative. It assumes the supply voltage is very "stiff" and does not account for any parasitic elements that will limit dI/dt such as stray inductance. Also, the ESR values of the capacitors specified by the manufacturer's data sheets are worst case high limits. In reality input voltage "sag," lower capacitor ESRs, and stray inductance will help reduce the slew rate of the input current.

As with the output inductor, the input inductor must support the maximum current without saturating the magnetic. Also, for an inexpensive iron powder core, such as the -26 or -52 from Micrometals, the inductance "swing" with DC bias must be taken into account - inductance will decrease as the DC input current increases. At the maximum input current, the inductance must not decrease below the minimum value or the $\mathrm{dI} / \mathrm{dt}$ will be higher than expected.

## 5. MOSFET \& Heatsink Selection

Power dissipation, package size, and thermal solution drive MOSFET selection. To adequately size the heat sink, the design must first predict the MOSFET power dissipation.

Once the dissipation is known, the heat sink thermal impedance can be calculated to prevent the specified maximum case or junction temperatures from being exceeded at the highest ambient temperature. Power dissipation has two primary contributors: conduction losses and switching losses. The control or upper MOSFET will display both switching and conduction losses. The synchronous or lower MOSFET will exhibit only conduction losses because it switches into nearly zero voltage. However, the body diode in the synchronous MOSFET will suffer diode losses during the non-overlap time of the gate drivers.
For the upper or control MOSFET, the power dissipation can be approximated from:

$$
\begin{align*}
& \text { PD, } \mathrm{CONTROL}=\left(\mathrm{I}_{\mathrm{RMS}, \mathrm{CNTL}}{ }^{2} \cdot \mathrm{R}_{\mathrm{DS}}(\mathrm{on})\right)  \tag{19}\\
& \quad+\left(\mathrm{I}_{\mathrm{Lo}, \mathrm{MAX}} \cdot \mathrm{Q}_{\mathrm{Switch}} / \mathrm{I}_{\mathrm{g}} \cdot \mathrm{~V}_{\mathrm{IN}} \cdot \mathrm{fSW}\right) \\
& \quad+\left(\mathrm{Q}_{\mathrm{OSS}} / 2 \cdot \mathrm{~V}_{\mathrm{IN}} \cdot \mathrm{f}_{\mathrm{SW}}\right)+\left(\mathrm{V}_{\mathrm{IN}} \cdot \mathrm{Q}_{\mathrm{RR}} \cdot \mathrm{fSW}\right)
\end{align*}
$$

The first term represents the conduction or IR losses when the MOSFET is ON while the second term represents the switching losses. The third term is the losses associated with the control and synchronous MOSFET output charge when the control MOSFET turns ON. The output losses are caused by both the control and synchronous MOSFET but are dissipated only in the control FET. The fourth term is the loss due to the reverse recovery time of the body diode in the synchronous MOSFET. The first two terms are usually adequate to predict the majority of the losses.

Where $\mathrm{I}_{\mathrm{RMS}, \mathrm{CNTL}}$ is the RMS value of the trapezoidal current in the control MOSFET:

$$
\begin{align*}
& \left.\left.+ \text { Lo oMIN }^{2}\right) / 3\right]^{1 / 2} \tag{20}
\end{align*}
$$

$\mathrm{I}_{\text {Lo,MAX }}$ is the maximum output inductor current:

$$
\begin{equation*}
\mathrm{I}_{\mathrm{Lo}, \mathrm{MAX}}=\mathrm{I}_{\mathrm{O}, \mathrm{MAX}} / 2+\Delta \mathrm{I}_{\mathrm{Lo}} / 2 \tag{21}
\end{equation*}
$$

$\mathrm{I}_{\text {Lo,MIN }}$ is the minimum output inductor current:

$$
\begin{equation*}
\mathrm{I} \mathrm{Lo}, \mathrm{MIN}=\mathrm{IO}, \mathrm{MAX} / 2-\Delta \mathrm{I} \mathrm{Lo} / 2 \tag{22}
\end{equation*}
$$

$\mathrm{I}_{\mathrm{O}, \text { MAX }}$ is the maximum converter output current.
D is the duty cycle of the converter:

$$
\begin{equation*}
\mathrm{D}=\mathrm{V}_{\mathrm{OUT}} / \mathrm{V}_{\mathrm{IN}} \tag{23}
\end{equation*}
$$

$\Delta \mathrm{I}_{\mathrm{Lo}}$ is the peak-to-peak ripple current in the output inductor of value Lo:

$$
\begin{equation*}
\Delta \mathrm{I}_{\mathrm{Lo}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \cdot \mathrm{D} /(\mathrm{Lo} \cdot \mathrm{fSW}) \tag{24}
\end{equation*}
$$

$\mathrm{R}_{\mathrm{DS} \text { (on) }}$ is the ON resistance of the MOSFET at the applied gate drive voltage.
$\mathrm{Q}_{\text {switch }}$ is the post gate threshold portion of the gate-to-source charge plus the gate-to-drain charge. This may be specified in the data sheet or approximated from the gate-charge curve as shown in the Figure 17.

$$
\begin{equation*}
\mathrm{Q}_{\mathrm{switch}}=\mathrm{Q}_{\mathrm{gs} 2}+\mathrm{Q}_{\mathrm{gd}} \tag{25}
\end{equation*}
$$



Figure 17. MOSFET Switching Characteristics
$\mathrm{I}_{\mathrm{g}}$ is the output current from the gate driver IC.
$\mathrm{V}_{\text {IN }}$ is the input voltage to the converter.
$f_{\text {sw }}$ is the switching frequency of the converter.
$\mathrm{Q}_{\mathrm{G}}$ is the MOSFET total gate charge to obtain $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$.
Commonly specified in the data sheet.
$\mathrm{V}_{\mathrm{g}}$ is the gate drive voltage.
$\mathrm{Q}_{\mathrm{RR}}$ is the reverse recovery charge of the lower MOSFET.
$\mathrm{Q}_{\text {oss }}$ is the MOSFET output charge specified in the data sheet.
For the lower or synchronous MOSFET, the power dissipation can be approximated from:

$$
\begin{align*}
& \text { PD,SYNCH }=\left(\mathrm{IRMS}_{\mathrm{RM}, \mathrm{SYNCH}}{ }^{2} \cdot \mathrm{RDS}_{\mathrm{DS}(\text { on })}\right. \\
& \quad+\left(\mathrm{Vf}_{\text {diode }} \cdot \mathrm{I}_{\mathrm{O}, \mathrm{MAX} / 2 \cdot \mathrm{t} \text { nonoverlap } \cdot \mathrm{fSW})}\right. \tag{26}
\end{align*}
$$

The first term represents the conduction or IR losses when the MOSFET is ON and the second term represents the diode losses that occur during the gate non-overlap time.

All terms were defined in the previous discussion for the control MOSFET with the exception of:

$$
\begin{aligned}
& \text { IRMS, SYNCH }=[(1-\mathrm{D}) \\
& \cdot\left(\mathrm{ILo}_{\mathrm{Lo}}, \mathrm{MAX}\right.
\end{aligned}
$$

where:
$\mathrm{Vf}_{\text {diode }}$ is the forward voltage of the MOSFET's intrinsic diode at the converter output current.
t _nonoverlap is the non-overlap time between the upper and lower gate drivers to prevent cross conduction. This time is usually specified in the data sheet for the control IC.
When the MOSFET power dissipations are known, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient operating temperature

$$
\begin{equation*}
\theta \mathrm{T}<(\mathrm{T} \mathrm{~J}-\mathrm{T} \mathrm{~A}) / \mathrm{PD} \tag{28}
\end{equation*}
$$

where;
$\theta_{\mathrm{T}}$ is the total thermal impedance $\left(\theta_{\mathrm{JC}}+\theta_{\mathrm{SA}}\right)$.
$\theta_{\mathrm{JC}}$ is the junction-to-case thermal impedance of the MOSFET.
$\theta_{\mathrm{SA}}$ is the sink-to-ambient thermal impedance of the heatsink assuming direct mounting of the MOSFET (no thermal "pad" is used).
$\mathrm{T}_{\mathrm{J}}$ is the specified maximum allowed junction temperature.
$\mathrm{T}_{\mathrm{A}}$ is the worst case ambient operating temperature.
For TO-220 and TO-263 packages, standard FR-4 copper clad circuit boards will have approximate thermal resistances $\left(\theta_{\mathrm{SA}}\right)$ as shown below:

| Pad Size <br> (in $^{2} / \mathrm{mm}^{2}$ ) | Single-Sided <br> $\mathbf{1 ~ o z . ~ C o p p e r ~}$ |
| :---: | :---: |
| $0.5 / 323$ | $60-65^{\circ} \mathrm{C} / \mathrm{W}$ |
| $0.75 / 484$ | $55-60^{\circ} \mathrm{C} / \mathrm{W}$ |
| $1.0 / 645$ | $50-55^{\circ} \mathrm{C} / \mathrm{W}$ |
| $1.5 / 968$ | $45-50^{\circ} \mathrm{C} / \mathrm{W}$ |
| $2.0 / 1290$ | $38-42^{\circ} \mathrm{C} / \mathrm{W}$ |
| $2.5 / 1612$ | $33-37^{\circ} \mathrm{C} / \mathrm{W}$ |

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e. worst case MOSFET $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ ). Also, the inductors and capacitors share the MOSFET's heatsinks and will add heat and raise the temperature of the circuit board and MOSFET. For any new design, its advisable to have as much heatsink area as possible - all too often new designs are found to be too hot and require re-design to add heatsinking.

## 6. Adaptive Voltage Positioning

There are two resistors that determine the Adaptive Voltage Positioning: $\mathrm{R}_{\mathrm{FBK} 1}$ and $\mathrm{R}_{\mathrm{DRP}} . \mathrm{R}_{\mathrm{FBK} 1}$ establishes the no-load "high" voltage position and $\mathrm{R}_{\mathrm{DRP}}$ determines the full-load "droop" voltage.

Resistor $\mathrm{R}_{\mathrm{FBK} 1}$ is connected between $\mathrm{V}_{\mathrm{CORE}}$ and the $\mathrm{V}_{\mathrm{FB}}$ pin of the controller. At no load, this resistor will conduct the internal bias current of the $\mathrm{V}_{\mathrm{FB}}$ pin and develop a voltage drop from $V_{\text {CORE }}$ to the $V_{\text {FB }}$ pin. Because the error amplifier regulates $\mathrm{V}_{\mathrm{FB}}$ to the DAC setting, the output voltage, $\mathrm{V}_{\mathrm{CORE}}$, will be higher by the amount IBIAS $\mathrm{VFB}^{\bullet} \mathrm{R}_{\mathrm{FBK} 1}$. This condition is shown in Figure 18.

To calculate $\mathrm{R}_{\text {FBK1 }}$ the designer must specify the no-load voltage increase above the VID setting ( $\Delta \mathrm{V}_{\text {NO-LOAD }}$ ) and determine the $\mathrm{V}_{\mathrm{FB}}$ bias current. Usually, the no-load voltage increase is specified in the design guide for the processor that is available from the manufacturer. The $\mathrm{V}_{\mathrm{FB}}$ bias current is determined by the value of the resistor from $\mathrm{R}_{\text {OSC }}$ to ground (see Figure 5 in the data sheet for a graph of IBIAS $_{\text {VFB }}$ versus $\mathrm{R}_{\mathrm{OSC}}$ ). The value of $\mathrm{R}_{\mathrm{FBK} 1}$ can then be calculated:


Figure 18. AVP Circuitry at No-Load

$$
\begin{equation*}
\mathrm{R}_{\mathrm{FBK} 1}=\Delta \mathrm{V}_{\text {NO-LOAD }} / \mathrm{IBIASVFB} \tag{29}
\end{equation*}
$$

Resistor $\mathrm{R}_{\mathrm{DRP}}$ is connected between the $\mathrm{V}_{\mathrm{DRP}}$ and the $\mathrm{V}_{\mathrm{FB}}$ pins. At no-load, the $\mathrm{V}_{\mathrm{DRP}}$ and the $\mathrm{V}_{\mathrm{FB}}$ pins will both be at the DAC voltage so this resistor will conduct zero current. However, at full-load, the voltage at the $\mathrm{V}_{\text {DRP }}$ pin will increase proportional to the output inductor's current while $\mathrm{V}_{\mathrm{FB}}$ will still be regulated to the DAC voltage. Current will be conducted from $V_{D R P}$ to $V_{F B}$ by $R_{D R P}$. This current will be large enough to supply the $\mathrm{V}_{\mathrm{FB}}$ bias current and cause a voltage drop from $\mathrm{V}_{\mathrm{FB}}$ to Vcore across $\mathrm{R}_{\mathrm{FBK}}$ - the converter's output voltage will be reduced. This condition is shown in Figure 19.

To determine the value of $\mathrm{R}_{\mathrm{DRP}}$ the designer must specify the full-load voltage reduction from the VID (DAC) setting ( $\Delta \mathrm{V}_{\text {OUT,FULL-LOAD }}$ ) and predict the voltage increase at the $\mathrm{V}_{\text {DRP }}$ pin at full-load. Usually, the full-load voltage reduction is specified in the design guide for the processor that is available from the manufacturer. To predict the voltage increase at the $\mathrm{V}_{\text {DRP }}$ pin at full-load ( $\Delta \mathrm{V}_{\text {DRP }}$ ), the designer must consider the output inductor's resistance
$\left(R_{L}\right)$, the PCB trace resistance between the current sense points ( $\mathrm{R}_{\mathrm{PCB}}$ ), and the controller IC's gain from the current sense to the $\mathrm{V}_{\text {DRP }}$ pin $\left(\mathrm{G}_{\mathrm{VDRP}}\right)$ :

$$
\begin{equation*}
\Delta V_{D R P}=I_{O, M A X} \cdot\left(R_{L}+R_{P C B}\right) \cdot G V D R P \tag{30}
\end{equation*}
$$

The value of $\mathrm{R}_{\mathrm{DRP}}$ can then be calculated:
$\operatorname{RDRP}=\frac{\Delta V_{\text {DRP }}}{\left(\text { IBIASVFB }+\Delta \mathrm{V}_{\text {OUT }}, \text { FULL-LOAD } / R_{F B K 1}\right)}$
$\Delta \mathrm{V}_{\text {OUT,FULL-LOAD }}$ is the full-load voltage reduction from the VID (DAC) setting. $\Delta \mathrm{V}_{\text {OUT,FULL-LOAD }}$ is not the voltage change from the no-load AVP setting.

## 7. Current Sensing

For inductive current sensing, choose the current sense network ( $\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}, \mathrm{n}=1$ or 2 ) to satisfy

$$
\begin{equation*}
\mathrm{R}_{\mathrm{CSn}} \cdot \mathrm{CCSn}=\mathrm{Lo} /\left(\mathrm{R}_{\mathrm{L}}+\mathrm{RPCB}\right) \tag{32}
\end{equation*}
$$



Figure 19. AVP Circuitry at Full-Load


Figure 20. V Constant of the Current Sense Network Is Too Long (Slow): $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\text {OUT }}$ Respond Too Slowly.


Figure 21. V Constant of the Current Sense Network Is Too Short (Fast): $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\text {OUT }}$ Both Overshoot.


Figure 22. V ${ }_{\text {DRP }}$ Tuning Waveforms. The RC Time Constant of the Current Sense Network Is Optimal: $\mathrm{V}_{\text {DRP }}$ and $\mathrm{V}_{\text {OUT }}$ Respond to the Load Current Quickly Without Overshooting.

For resistive current sensing, choose the current sense network ( $\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}, \mathrm{n}=1$ or 2 ) to satisfy

$$
\begin{equation*}
\mathrm{R}_{\mathrm{CSn}} \cdot \mathrm{C}_{\mathrm{CSn}}=\mathrm{Lo} /\left(\mathrm{R}_{\text {sense }}\right) \tag{33}
\end{equation*}
$$

This will provide an adequate starting point for $\mathrm{R}_{\mathrm{CSn}}$ and $\mathrm{C}_{\mathrm{CSn}}$. After the converter is constructed, the value of $\mathrm{R}_{\mathrm{CSn}}$ (and/or $\mathrm{C}_{\mathrm{CSn}}$ ) should be fine-tuned in the lab by observing the $\mathrm{V}_{\text {DRP }}$ signal during a step change in load current. The $\mathrm{R}_{\mathrm{CSn}}-\mathrm{C}_{\mathrm{CSn}}$ network should be tuned to provide a "square-wave" at the $V_{\text {DRP }}$ output pin with maximum rise time and minimal overshoot as shown in Figure 22.

Equation 32 will be most accurate for better iron powder core material (such as the -8 from Micrometals). This material is very consistent with DC current and frequency. Less expensive core materials (such as the -52 from Micrometals) change their characteristics with DC current, AC flux density, and frequency. This material will yield acceptable converter performance if the current sense time constant is set lower (longer) than anticipated. As a rule of thumb, use approximately twice the resistance $\left(\mathrm{R}_{\mathrm{CSn}}\right)$ or twice the capacitance $\left(\mathrm{C}_{\mathrm{CSn}}\right)$ when using the less expensive core material.

## 8. Error Amplifier Tuning

After the steady-state (static) AVP has been set and the current sense network has been optimized the Error Amplifier must be tuned. Basically, the gain of the Error Amplifier should be adjusted to provide an acceptable transient response by increasing or decreasing the Error Amplifier's feedback capacitor ( $\mathrm{C}_{\text {AMP }}$ in the Applications Diagram). The bandwidth of the control loop will vary directly with the gain of the error amplifier.


Figure 23. The Value of $\mathrm{C}_{\text {AMP }}$ Is Too High and the Loop Gain/Bandwidth Too Low. COMP Slews Too Slowly Which Results in Overshoot in $\mathrm{V}_{\text {OUT }}$.

If $\mathrm{C}_{\text {AMP }}$ is too large the loop gain/bandwidth will be low, the COMP pin will slew too slowly, and the output voltage will overshoot as shown in Figure 23. On the other hand, if $\mathrm{C}_{\mathrm{AMP}}$ is too small the loop gain/bandwidth will be high, the COMP pin will slew very quickly and overshoot. Integrator
"wind up" is the cause of the overshoot. In this case the output voltage will transition more slowly because COMP spikes upward as shown in Figure 24. Too much loop gain/bandwidth increase the risk of instability. In general, one should use the lowest loop gain/bandwidth as possible to achieve acceptable transient response - this will insure good stability. If $\mathrm{C}_{\mathrm{AMP}}$ is optimal the COMP pin will slew quickly but not overshoot and the output voltage will monotonically settle as shown in Figure 25.

After the control loop is tuned to provide an acceptable transient response the steady-state voltage ripple on the COMP pin should be examined. When the converter is operating at full, steady-state load, the peak-to-peak voltage ripple on the COMP pin should be less than $20 \mathrm{mV}_{\mathrm{PP}}$ as shown in Figure 26. Less than $10 \mathrm{mV}_{\mathrm{PP}}$ is ideal. Excessive ripple on the COMP pin will contribute to output voltage jitter.


Figure 24. The Value of $\mathrm{C}_{\mathrm{AMP}}$ Is Too Low and the Loop Gain/Bandwidth Too High. COMP Moves Too Quickly, Which Is Evident from the Small Spike in Its Voltage When the Load Is Applied or Removed. The Output Voltage Transitions More Slowly Because of the COMP Spike.


Figure 25. The Value of $\mathrm{C}_{\text {AMP }}$ Is Optimal. COMP Slews Quickly Without Spiking or Ringing. $\mathrm{V}_{\text {OUT }}$ Does Not Overshoot and Monotonically Settles to Its Final Value.


Figure 26. At Full-Load (28 A) the Peak-to-Peak Voltage Ripple on the COMP Pin Should Be Less than 20 mV for a Well-Tuned/Stable Controller. Higher COMP Voltage Ripple Will Contribute to Output Voltage Jitter.

## 9. Current Limit Setting

When the output of the current sense amplifier (CO1 or CO 2 in the block diagram) exceeds the voltage on the $\mathrm{I}_{\mathrm{LIM}}$ pin the part will enter hiccup mode. For inductive sensing, the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor's maximum resistance ( $\mathrm{R}_{\text {LMAX }}$ ). The design must consider the inductor's resistance increase due to current heating and ambient temperature rise. Also, depending on the current sense points, the circuit board may add additional resistance. In general, the temperature coefficient of copper is $+0.393 \%$ per ${ }^{\circ} \mathrm{C}$. If using a current sense resistor ( $\mathrm{R}_{\text {SENSE }}$ ), the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the maximum value of the sense resistor. To set the level of the $\mathrm{I}_{\text {LIM }}$ pin:

$$
\begin{equation*}
\text { VILIM }=(\mathrm{IOUT}, \mathrm{LIM}+\Delta \mathrm{I} \mathrm{Lo} / 2) \cdot \mathrm{R} \cdot \mathrm{GILIM} \tag{34}
\end{equation*}
$$

where:
IOUT,LIM is the current limit threshold of the converter;
$\Delta \mathrm{I}_{\mathrm{Lo}} / 2$ is half the inductor ripple current;
R is either ( $\mathrm{R}_{\mathrm{LMAX}}+\mathrm{R}_{\mathrm{PCB}}$ ) or $\mathrm{R}_{\text {SENSE }}$;
$\mathrm{G}_{\text {ILIM }}$ is the current sense to $\mathrm{I}_{\text {LIM }}$ gain.
For the overcurrent protection to work properly, the current sense time constant (RC) should be slightly larger than the RL time constant. If the RC time constant is too fast, during step load changes the sensed current waveform will appear larger than the actual inductor current and will probably trip the current limit at a lower level than expected.

## 10. PWM Comparator Input Voltage

The voltage at the positive input terminal of the PWM comparator (see Figure 10 or 12) is limited by the internal voltage supply of the controller ( 3.3 V ), the size of the internal ramp, and the magnitude of the channel startup offset voltage. To prevent the PWM comparator from saturating, the differential input voltage from $\mathrm{CS}_{\text {REF }}$ to CSn ( $\mathrm{n}=1$ or 2 ) must satisfy the following equation:
$V_{C S R E F}, \mathrm{MAX}+\mathrm{V}_{\text {COn }}, \mathrm{MAX}+310 \mathrm{mV} \cdot \mathrm{D} \leq 2.45 \mathrm{~V}$
where:
VCSREF,MAX = Max VID Setting w/ AVP @ Full Load
$\mathrm{V}_{\text {COn, MAX }}=\left[\mathrm{V}_{\text {CSn }}-\mathrm{V}_{\text {CSREF }}\right] \cdot \mathrm{GCSA}, \mathrm{MAX}$
$=\left(\mathrm{IO}, \mathrm{MAX} / 2+\mathrm{I}_{\mathrm{Lo}} / 2\right) \cdot \mathrm{R}_{\text {MAX }}$

- GCSA,MAX
$R_{\text {MAX }}=R_{\text {SENSE }}$ or ( $\mathrm{R}_{\mathrm{L}, \mathrm{MAX}}+\mathrm{RPCB}, \mathrm{MAX}$ )


## 11. Soft Start Time

If the Soft Start time is defined from the instant the Soft Start pin is released (i.e. the converter is enabled) to when the output reaches the VID setting with AVP then the Soft Start time ( $\mathrm{t}_{\mathrm{SS}}$ ) can be calculated from:

$$
\begin{equation*}
\text { TSS }=\text { VCOMP } \cdot \mathrm{CSS} / \mathrm{ISS} \tag{36}
\end{equation*}
$$

where:

$$
\begin{aligned}
\text { V COMP }^{=} & \text {VOUT @ } 0 \text { A + Channel_Startup_Offset } \\
& + \text { Int_Ramp }+ \text { GCSA } \cdot \text { Ext_Ramp } / 2
\end{aligned}
$$

$\mathrm{C}_{\mathrm{SS}}$ is the capacitor from the Soft-Start pin to LGND;
Ext_Ramp = D • $\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) /\left(\mathrm{R}_{\mathrm{CSn}} \bullet \mathrm{C}_{\mathrm{CSn}} \bullet \mathrm{f}_{\mathrm{SW}}\right)$;
$\mathrm{I}_{\mathrm{SS}}$ is the Soft-Start charge current from the data sheet.

## Design Example

## Typical Design Requirements:

$\mathrm{V}_{\mathrm{IN}}=12.0 \mathrm{Vdc}$
$\mathrm{V}_{\text {OUT }}=1.60 \mathrm{Vdc}$ (nominal)
$\mathrm{V}_{\text {OUT,RIPPLE }}<10 \mathrm{mV}_{\text {PP }} \max$
VID Range: 1.100 Vdc -1.850 Vdc
$\mathrm{I}_{\mathrm{O}, \mathrm{MAX}}=45 \mathrm{~A}$ at full-load
$\mathrm{I}_{\text {OUT,LIM }}=52 \mathrm{~A} \mathrm{~min}$ at $55^{\circ} \mathrm{C}$ (shutdown threshold)
$\mathrm{dI}_{\mathrm{IN}} / \mathrm{dt}=0.50 \mathrm{~A} / \mu \mathrm{s} \max$
$\mathrm{f}_{\mathrm{SW}}=220 \mathrm{kHz}$
$\eta=81 \%$ min at full-load
$\mathrm{T}_{\mathrm{A}, \mathrm{MAX}}=60^{\circ} \mathrm{C}$
$\mathrm{T}_{\mathrm{J}, \mathrm{MAX}}=125^{\circ} \mathrm{C}$
$\mathrm{t}_{\mathrm{SS}}<10.0 \mathrm{~ms}$ (Soft Start time)
$\Delta \mathrm{V}_{\text {OUT }}$ at no-load (static) $=$
+30 mV from VID setting $=1.630 \mathrm{Vdc}$
$\Delta \mathrm{V}_{\text {OUT }}$ at full-load (static) $=$
-35 mV from VID setting $=1.565 \mathrm{Vdc}$
$\Delta \mathrm{V}_{\text {OUT }}$ at full-load (transient) $=$
-65 mV from VID setting $=1.540 \mathrm{Vdc}$

## 1. Output Capacitor Selection

First, choose a low-cost, low-ESR output capacitor such as the Rubycon 16MBZ1500M10X20: $16 \mathrm{~V}, 1500 \mu \mathrm{~F}$, 2.55 A $_{\text {RMS }}, 13 \mathrm{~m} \Omega, 10 \times 20 \mathrm{~mm}$. Calculate the minimum number of output capacitors:

$$
\begin{align*}
\text { NOUT,MIN } & =\text { ESR per capacitor } \cdot \frac{\Delta \mathrm{I}_{\mathrm{O}, \mathrm{MAX}}}{\Delta \mathrm{~V}_{\mathrm{O}, \mathrm{MAX}}}  \tag{1}\\
& =13 \mathrm{~m} \Omega \cdot 45 \mathrm{~A} /(1.630 \mathrm{~V}-1.540 \mathrm{~V}) \\
& =6.5 \text { or } 7 \text { capacitors minimum }(10,500 \mu \mathrm{~F})
\end{align*}
$$

## 2. Output Inductor Selection

Calculate the minimum output inductance at $I_{O, M A X}$ according to Equation 4 with $\pm 20 \%$ inductor ripple current ( $\alpha=0.20$ ):

$$
\begin{align*}
\text { LoMIN } & =\frac{\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}\right) \cdot \mathrm{V}_{\text {OUT }}}{\left(\alpha \cdot \mathrm{I}_{\left.\mathrm{O}, \mathrm{MAX} \cdot \mathrm{VIN}^{2} \cdot \mathrm{fSW}\right)}\right.}  \tag{3}\\
& =\frac{(12 \mathrm{~V}-1.565 \mathrm{~V}) \cdot 1.565 \mathrm{~V}}{(0.2 \cdot 45 \mathrm{~A} \cdot 12 \mathrm{~V} \cdot 220 \mathrm{kHz})} \\
& =687 \mathrm{nH}
\end{align*}
$$

To save cost, we choose the inexpensive T50-52B core from Micrometals: $43.5 \mathrm{nH} / \mathrm{N}^{2}, 3.19 \mathrm{~cm} /$ turn. According to the Micrometals catalog, at 22.5 A (per phase) the permeability of this core will be approximately $70 \%$ of the permeability at 0 A . Therefore, at 0 A we must achieve at least $687 \mathrm{nH} / 0.7$ or 981 nH . Using five turns of \#16AWG bifilar ( $2 \mathrm{~m} \Omega / \mathrm{ft}$ ) will produce $1.1 \mu \mathrm{H}$.

Use Equation 4 to insure the output voltage ripple will satisfy the design goal with the minimum number of capacitors and the nominal output inductance:

```
VOUT,P-P \(=(\) ESR per cap \(/\) NOUT,MIN) \(\cdot\)
    \(\left\{\left(\mathrm{V}_{\text {IN }}-\right.\right.\) \#Phases \(\left.\cdot \mathrm{V}_{\text {OUT }}\right) \cdot \mathrm{D} /(\) LoMIN \(\cdot \mathrm{f}\) SW \(\left.)\right\}\)
\(=(13 \mathrm{~m} \Omega / 7)\).
    \(\{(5.0 \mathrm{~V}-2 \cdot 1.6 \mathrm{~V}) \cdot(1.6 \mathrm{~V} / 5.0 \mathrm{~V}) /(1.1 \mu \mathrm{H} \cdot 220 \mathrm{kHz})\}\)
\(=(1.86 \mathrm{~m} \Omega) \cdot\{2.38 \mathrm{~A}\}\)
\(=4.43 \mathrm{mV}\)
```

The output voltage ripple will be decreased when output capacitors are added to satisfy transient loading requirements.

We will need the nominal and worst case inductor resistances for subsequent calculations:

$$
\begin{aligned}
R_{\mathrm{L}} & =5 \text { turns } \cdot 3.19 \mathrm{~cm} / \text { turn } \cdot 0.03218 \mathrm{ft} / \mathrm{cm} \cdot 2 \mathrm{~m} \Omega / \mathrm{ft} \\
& =1.03 \mathrm{~m} \Omega
\end{aligned}
$$

The inductor resistance will be maximized when the inductor is "hot" due to the load current and the ambient temperature is high. Assuming a $40^{\circ} \mathrm{C}$ temperature rise of the inductor at full-load and a $35^{\circ} \mathrm{C}$ ambient temperature rise we can calculate:

$$
\begin{aligned}
\mathrm{RL}, \mathrm{MAX} & =1.03 \mathrm{~m} \Omega \cdot\left[1+0.39 \% /{ }^{\circ} \mathrm{C} \cdot\left(40^{\circ} \mathrm{C}+35^{\circ} \mathrm{C}\right)\right] \\
& =1.33 \mathrm{~m} \Omega
\end{aligned}
$$

The output inductance at full-load will be:

$$
\mathrm{Lo}=0.70 \times 1.1 \mu \mathrm{H}=770 \mathrm{nH}
$$

## 3. Input Capacitor Selection

Use Equation 5 to determine the average input current to the converter at full-load;

$$
\begin{align*}
\mathrm{I}_{\mathrm{I}, \mathrm{AVG}} & =\mathrm{I}, \mathrm{MAX} \cdot \mathrm{D} / \eta  \tag{5}\\
& =45 \mathrm{~A} \cdot(1.565 \mathrm{~V} / 12 \mathrm{~V}) / 0.81=5.87 \mathrm{~A}
\end{align*}
$$

Next, use Equations 6 to 10 with the full-load inductance value of 770 nH :

$$
\begin{align*}
& \Delta \mathrm{I}_{\mathrm{Lo}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \cdot \mathrm{D} /(\mathrm{Lo} \cdot \mathrm{fSW}) \\
& =(12 \mathrm{~V}-1.565 \mathrm{~V}) \cdot \frac{(1.565 \mathrm{~V} / 12 \mathrm{~V})}{(770 \mathrm{nH} \cdot 220 \mathrm{kHz})}  \tag{10}\\
& =8.03 \mathrm{App} \\
& \mathrm{I}_{\mathrm{Lo}}, \mathrm{MAX}=\mathrm{I}_{\mathrm{O}, \mathrm{MAX}} / 2+\Delta \mathrm{I}_{\mathrm{Lo}} / 2  \tag{8}\\
& =45 \mathrm{~A} / 2+8.03 \mathrm{App} / 2=26.5 \mathrm{~A} \\
& \mathrm{I}_{\mathrm{Lo}}, \mathrm{MIN}=\mathrm{I} \mathrm{O}, \mathrm{MAX} / 2-\Delta \mathrm{I} \mathrm{Lo} / 2 \\
& =45 \mathrm{~A} / 2-8.03 \mathrm{App} / 2=18.5 \mathrm{~A}  \tag{9}\\
& \mathrm{I}_{\mathrm{C}}, \mathrm{MAX}=\mathrm{I}_{\mathrm{Lo}}, \mathrm{MAX} / \eta-\mathrm{I}_{\mathrm{IN}, \mathrm{AVG}}  \tag{6}\\
& =26.5 \mathrm{~A} / 0.81-5.87 \mathrm{~A}=20.63 \mathrm{~A} \\
& \mathrm{I}_{\mathrm{C}} \mathrm{MIN}=\mathrm{I} \mathrm{Lo}, \mathrm{MIN} / \eta-\mathrm{IIN}, \mathrm{AVG}  \tag{7}\\
& =18.5 \mathrm{~A} / 0.81-5.87 \mathrm{~A}=12.63 \mathrm{~A}
\end{align*}
$$

For the two-phase converter, the input capacitor(s) RMS current at full-load is then (Note: $\mathrm{D}=1.565 \mathrm{~V} / 12 \mathrm{~V}=0.13$ ):

$$
\begin{align*}
\mathrm{I} \mathrm{CIN}, R \mathrm{RMS}= & {\left[2 \mathrm { D } \cdot \left(\mathrm{IC}, \mathrm{MIN}^{2}+\mathrm{I}_{\mathrm{C}, \mathrm{MIN} \cdot \Delta \mathrm{I}_{\mathrm{C}}, \mathrm{IN}}\right.\right.}  \tag{11}\\
& +\Delta \mathrm{I}_{\left.\mathrm{C}, \mathrm{IN}^{2} / 3\right)+\mathrm{I}_{\left.\mathrm{IN}, \mathrm{AVG}^{2} \cdot(1-2 \mathrm{D})\right]^{1 / 2}}}=\left[0.26 \cdot\left(12.63^{2}+12.63 \cdot 8.00+8.00^{2} / 3\right)\right. \\
& \left.+5.87^{2} \cdot(1-0.26)\right]^{1 / 2} \\
= & 9.69 \text { ARMS }
\end{align*}
$$

At this point, the designer must decide between saving board space by using higher-rated/more costly capacitors or saving cost by using more lower-rated/less costly capacitors. To save board space, we choose the SP (Oscon) series capacitors by Sanyo. Part number 16SP270: $270 \mu \mathrm{~F}$, $16 \mathrm{~V}, 4.4 \mathrm{~A}_{\mathrm{RMS}}, 18 \mathrm{~m} \Omega, 10 \times 10.5 \mathrm{~mm}$. This design will require $9.69 \mathrm{~A} / 4.4 \mathrm{~A}=2.2$ or $\mathrm{N}_{\mathrm{IN}}=3$ capacitors on the input for a conservative design.

## 4. Input Inductor Selection

The input inductor must limit the input current slew rate to less than $0.5 \mathrm{~A} / \mu \mathrm{s}$ during a load transient from 0 to 45 A . A conservative value will be calculated assuming the minimum number of output capacitors ( $\mathrm{N}_{\text {OUT }}=7$ ), three input capacitors ( $\mathrm{N}_{\mathrm{IN}}=3$ ), worst case ESR values for both the input and output capacitors, and a maximum duty cycle $\left(\mathrm{D}=\left(1.850 \mathrm{~V}+30 \mathrm{mV}_{\mathrm{AVP}}\right) / 12.0 \mathrm{~V}_{\mathrm{IN}}=0.157\right)$.


Figure 27. Actual DC/DC Converter Circuitry With the Calculated Input Inductor and Minimum Filtering Components. The Measured Slew-Rate ( $\mathrm{dl}_{\mathrm{IN}} / \mathrm{dt}$ ) of the Input Current ( $0.064 \mathrm{~A} / \mu \mathrm{s}$ ) Is Much Lower Than Expected ( $0.1 \mathrm{~A} / \mu \mathrm{s}$ ) Because of Input Voltage Drop, Parasitic Inductance, and Lower Real ESRs Than Specified in the Capacitors' Data Sheets.

First, use Equation 15 to calculate the voltage across the output inductor due to the 45 A load current being shared equally between the two phases:

$$
\begin{align*}
\Delta \mathrm{V}_{\mathrm{Lo}}= & \mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}, \mathrm{NO}-\mathrm{LOAD}}  \tag{15}\\
& +(\mathrm{IO}, \mathrm{MAX} / 2) \cdot \mathrm{ESR} \mathrm{OUT} / \mathrm{NOUT} \\
= & 12 \mathrm{~V}-1.85 \mathrm{~V}+45 \mathrm{~A} / 2 \cdot 13 \mathrm{~m} \Omega / 7 \\
= & 10.19 \mathrm{~V}
\end{align*}
$$

Second, use Equation 16 to determine the rate of current increase in the output inductor when the load is first applied (i.e. Lo has not changed much due to the DC current):

$$
\begin{align*}
\mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt} & =\Delta \mathrm{V}_{\mathrm{Lo}} / \mathrm{Lo}  \tag{16}\\
& =10.19 \mathrm{~V} / 1.1 \mu \mathrm{H}=9.26 \mathrm{~V} / \mu \mathrm{s}
\end{align*}
$$

Finally, use Equations 17 and 18 to calculate the minimum input inductance value:

$$
\begin{align*}
\Delta \mathrm{V}_{\mathrm{Ci}} & =\mathrm{ESRIN} / \mathrm{N}_{\mathrm{IN}} \cdot \mathrm{dl}_{\mathrm{Lo}} / \mathrm{dt} \cdot \mathrm{D} / \mathrm{fSW}  \tag{17}\\
& =18 \mathrm{~m} \Omega / 3 \cdot 9.26 \mathrm{~V} / \mu \mathrm{s} \cdot 0.157 / 220 \mathrm{kHz} \\
& =39.7 \mathrm{mV} \\
\mathrm{LiMIN} & =\Delta \mathrm{V}_{\mathrm{Ci}} / \mathrm{dl}_{\mathrm{IN}} / \mathrm{dtMAX}_{\mathrm{MA}}  \tag{18}\\
& =39.7 \mathrm{mV} / 0.50 \mathrm{~A} / \mu \mathrm{s}=80 \mathrm{nH}
\end{align*}
$$

Next, choose the small, cost effective T30-26 core from Micrometals ( $33.5 \mathrm{nH} / \mathrm{N}^{2}$ ) with \#16 AWG. The design requires only 1.54 turns to achieve the minimum inductance value. Allow for inductance "swing" at full-load by using three turns. The input inductor's value will be:

$$
\mathrm{L}_{\mathrm{i}}=3^{2} \cdot 33.5 \mathrm{nH} / \mathrm{N}^{2}=301 \mathrm{nH}
$$

This inductor is available as part number CTX15-14771 from Coiltronics.

## 5. MOSFET \& Heatsink Selection

The IPB05N03L from Infineon is chosen for both the control and synchronous MOSFET due to its low $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ and low gate-charge requirements. The following parameters are derived from the IPB05N03L data sheet:

$$
\begin{aligned}
& \mathrm{Rds}_{\mathrm{ON}}=3.9 \mathrm{~m} \Omega @ 10 \mathrm{~V} \\
& \mathrm{Q}_{\mathrm{SWITCH}}=25 \mathrm{nC} \\
& \mathrm{Q}_{\mathrm{RR}}=45 \mathrm{nC} \\
& \mathrm{Q}_{\mathrm{OSS}}=35 \mathrm{nC} \\
& \mathrm{Vf}_{\text {diode }}=0.86 \mathrm{~V} @ 25 \mathrm{~A} \\
& \theta_{\mathrm{JC}}=1.0^{\circ} \mathrm{C} / \mathrm{W}
\end{aligned}
$$

## NCP5322A Parameters:

$$
\mathrm{i}_{\mathrm{G}}=1.5 \mathrm{~A}
$$

$\mathrm{V}_{\mathrm{G}}=10 \mathrm{~V}$
t_nonoverlap $=65 \mathrm{~ns}$
The RMS value of the current in the control MOSFET is calculated from Equation 20 and the previously derived values for $\mathrm{D}, \mathrm{I}_{\text {LMAX }}$, and $\mathrm{I}_{\text {LMIN }}$ at the converter's maximum output current:

$$
\begin{align*}
& \mathrm{I}_{\mathrm{RMS}, \mathrm{CNTL}}= {[\mathrm{D} \cdot}  \tag{20}\\
&\left(\mathrm{ILo}_{\mathrm{Lo}, \mathrm{MAX}}{ }^{2}+\mathrm{I}_{\mathrm{Lo}}, \mathrm{MAX} \cdot \mathrm{I}_{\mathrm{Lo}, \mathrm{MIN}}\right. \\
& \quad+\mathrm{ILo}_{\left.\left.\mathrm{Lo}, \mathrm{MIN}^{2}\right) / 3\right]^{1 / 2}} \\
&=0.36 \cdot\left[\left(26.5^{2}+26.5 \cdot 18.5+18.5^{2}\right) / 3\right]^{1 / 2} \\
&= 8.15 \text { ARMS }
\end{align*}
$$

Equation 19 is used to calculate the power dissipation of the control MOSFET:

$$
\begin{aligned}
& \text { PD,CONTROL }=\left(\mathrm{I}_{\mathrm{RMS}, \mathrm{CNTL}}{ }^{2} \cdot \mathrm{R}_{\mathrm{DS}}(\mathrm{on})\right) \\
&+\left(\mathrm{ILo}_{\mathrm{M}} \mathrm{MAX} \cdot \mathrm{Q}_{\left.\mathrm{Switch} / \mathrm{I}_{\mathrm{g}} \cdot \mathrm{VIN} \cdot \mathrm{fSW}\right)}\right. \\
&+\left(\mathrm{Q}_{\mathrm{OSS}} / 2 \cdot \mathrm{~V}_{\mathrm{IN}} \cdot \mathrm{fSW}\right)+\left(\mathrm{V}_{\mathrm{IN}} \cdot \mathrm{Q}_{\mathrm{RR}} \cdot \mathrm{fSW}\right) \\
&=\left(8.15^{2} \mathrm{ARMS} \cdot 3.9 \mathrm{~m} \Omega\right) \\
&+(26.5 \mathrm{~A} \cdot 25 \mathrm{nC} / 1.5 \mathrm{~A} \cdot 12 \mathrm{~V} \cdot 220 \mathrm{kHz}) \\
&+(35 \mathrm{nC} / 2 \cdot 12 \mathrm{~V} \cdot 220 \mathrm{kHz}) \\
&+(12 \mathrm{~V} \cdot 45 \mathrm{nC} \cdot 220 \mathrm{kHz}) \\
&= 0.26 \mathrm{~W}+1.17 \mathrm{~W}+0.05 \mathrm{~W}+0.12 \mathrm{~W} \\
&= 1.60 \mathrm{~W}
\end{aligned}
$$

The RMS value of the current in the synchronous MOSFET is calculated from Equation 27 and the previously derived values for $\mathrm{D}, \mathrm{I}_{\mathrm{Lo}, \mathrm{MAX}}$, and $\mathrm{I}_{\mathrm{Lo}, \mathrm{MIN}}$ at the converter's maximum output current:

$$
\begin{aligned}
& \text { IRMS,SYNCH }=[(1-D) \cdot
\end{aligned}
$$

$$
\begin{aligned}
& =\left[(1-0.13) \cdot\left(26.5^{2}+26.5 \cdot 18.5+18.5^{2}\right) / 3\right]^{1 / 2} \\
& =21.1 \text { ARMS }
\end{aligned}
$$

Equation 26 is used to calculate the power dissipation of the synchronous MOSFET:

$$
\begin{align*}
\mathrm{PD}, \mathrm{SYNCH}= & \left(\mathrm{I}_{\mathrm{RMS}, \mathrm{SYNCH}}\right.  \tag{26}\\
& +\mathrm{RDS}(\mathrm{on})) \\
= & \left(21.1^{2} \mathrm{ARf} \text { diode } \cdot \mathrm{IO}_{\mathrm{RMS}} \cdot \mathrm{MAX} / 2 \cdot \mathrm{t} .9 \mathrm{~m} \Omega\right) \\
& +(0.86 \mathrm{~V} \cdot 45 \mathrm{~A} / 2 \cdot 65 \mathrm{~ns} \cdot 220 \mathrm{kHz}) \\
= & 1.74 \mathrm{~W}+0.28 \mathrm{~W}=2.02 \mathrm{~W}
\end{align*}
$$

Equation 28 is used to calculate the heat sink thermal impedances necessary to maintain less than the specified maximum junction temperatures at $60^{\circ} \mathrm{C}$ ambient:

$$
\begin{aligned}
& \theta \mathrm{CNTL}<\left(125-60^{\circ} \mathrm{C}\right) / 1.6 \mathrm{~W}-1.0^{\circ} \mathrm{C} / \mathrm{W}=40^{\circ} \mathrm{C} / \mathrm{W} \\
& \theta \text { SYNCH }<\left(125-60^{\circ} \mathrm{C}\right) / 2.02 \mathrm{~W}-1.0^{\circ} \mathrm{C} / \mathrm{W}=31^{\circ} \mathrm{C} / \mathrm{W}
\end{aligned}
$$

If board area permits, a cost effective heatsink could be formed by using a TO-263 mounting pad of at least $1.5 \mathrm{in}^{2}$ for the upper MOSFET and $2.5 \mathrm{in}^{2}$ for the lower MOSFET on a single-sided, 1 oz . copper PCB. The total required pad area would be slightly less if the area were divided evenly between top and bottom layers with multiple thermal vias joining the two areas. To conserve board space, AAVID offers clip-on heatsinks for TO-220 thru-hole packages. Examples of these heatsinks include \#577002 ( $1^{\prime \prime} \times 0.75^{\prime \prime} \times$ $0.25^{\prime \prime}, 33^{\circ} \mathrm{C} / \mathrm{W}$ at 2 W$)$ and \#591302 ( $0.75^{\prime \prime} \times 0.5^{\prime \prime} \times 0.5^{\prime \prime}$, $29^{\circ} \mathrm{C} / \mathrm{W}$ at 2 W ).

## 6. Adaptive Voltage Positioning

First, to achieve the 220 kHz switching frequency, use Figure 4 to determine that a $65 \mathrm{k} \Omega$ resistor is needed for $\mathrm{R}_{\mathrm{OSC}}$. Then, use Figure 5 to find the $\mathrm{V}_{\mathrm{FB}}$ bias current at the corresponding value of $\mathrm{R}_{\mathrm{OSC}}$. In this example, the $65 \mathrm{k} \Omega$ $\mathrm{R}_{\mathrm{OSC}}$ resistor results in a $\mathrm{V}_{\mathrm{FB}}$ bias current of approximately $5.0 \mu \mathrm{~A}$. Knowing the $\mathrm{V}_{\mathrm{FB}}$ bias current, one can calculate the required values for $\mathrm{R}_{\mathrm{FBK} 1}$ and $\mathrm{R}_{\mathrm{DRP}}$ using Equations 29 through 31.
The no-load position is easily set using Equation 29:

$$
\begin{align*}
\text { RFBK1 } & =\Delta \mathrm{V}_{\text {NO }}-\text { LOAD/IBIASVFB }  \tag{29}\\
& =+30 \mathrm{mV} / 5.0 \mu \mathrm{~A} \\
& =6.04 \mathrm{k} \Omega
\end{align*}
$$

For inductive current sensing, the designer must calculate the inductor's resistance $\left(\mathrm{R}_{\mathrm{L}}\right)$ and approximate any resistance added by the circuit board ( $\mathrm{R}_{\mathrm{PCB}}$ ). We found the inductor's nominal resistance in Section $2(0.82 \mathrm{~m} \Omega)$. In this example, we approximate $0.50 \mathrm{~m} \Omega$ for the circuit board resistance ( $\mathrm{R}_{\mathrm{PCB}}$ ). With this information, Equation 30 can be used to calculate the increase at the $\mathrm{V}_{\text {DRP }}$ pin at full load:

$$
\begin{aligned}
\Delta \mathrm{V}_{\mathrm{DRP}} & =\mathrm{I}_{\mathrm{O}}, \mathrm{MAX} \cdot\left(\mathrm{R}_{\mathrm{L}}+\mathrm{RPCB}\right) \cdot \mathrm{GVDRP} \\
& =45 \mathrm{~A} \cdot(1.03 \mathrm{~m} \Omega+0.50 \mathrm{~m} \Omega) \cdot 3.3 \mathrm{~V} / \mathrm{V} \\
& =227 \mathrm{mV}
\end{aligned}
$$

$\mathrm{R}_{\mathrm{DRP1}}$ can then be calculated from Equation 31:

$$
\begin{aligned}
\mathrm{R}_{\mathrm{DRP}} & =\frac{\Delta \mathrm{V} \text { DRP }}{\left(\mathrm{IBIASVFB}+\Delta \mathrm{V}_{\mathrm{OUT}, \mathrm{FULL}-\mathrm{LOAD} / \mathrm{RFBK} 1)}\right)} \\
& =227 \mathrm{mV} /(5.0 \mu \mathrm{~A}+35 \mathrm{mV} / 6.04 \mathrm{k} \Omega) \\
& =21.0 \mathrm{k} \Omega
\end{aligned}
$$

## 7. Current Sensing

Choose the current sense network $\left(\mathrm{R}_{\mathrm{CSn}}, \mathrm{C}_{\mathrm{CSn}}, \mathrm{n}=1\right.$ or 2$)$ to satisfy:

$$
\begin{equation*}
\mathrm{R}_{\mathrm{CSn}} \cdot \mathrm{C}_{\mathrm{CS}}=\mathrm{Lo} /\left(\mathrm{R}_{\mathrm{L}}+\mathrm{RPCB}\right) \tag{32}
\end{equation*}
$$

Equation 32 will be most accurate for better iron powder core material (such as the -8 from Micrometals). This material is very consistent with DC current and frequency. Less expensive core materials (such as the -52 from Micrometals) change their characteristics with DC current, AC flux density, and frequency. This material will yield acceptable converter performance if the current sense time constant is set lower (longer) than anticipated. As a rule of thumb, use approximately twice the resistance $\left(\mathrm{R}_{\mathrm{CSn}}\right)$ or twice the capacitance $\left(\mathrm{C}_{\mathrm{CSn}}\right)$ when using the less expensive core material.

The component values determined thus far are $L o=1.1 \mu \mathrm{H}$, $\mathrm{R}_{\mathrm{L}}=1.03 \mathrm{~m} \Omega$, and $\mathrm{R}_{\mathrm{PCB}}=0.50 \mathrm{~m} \Omega$. We choose a convenient value for $\mathrm{C}_{\mathrm{CS} 1}(0.01 \mu \mathrm{~F})$ and solve for $\mathrm{R}_{\mathrm{CS} 1}$;

$$
\begin{aligned}
\mathrm{R}_{\mathrm{CSn}} & =1.1 \mu \mathrm{H} /(1.03 \mathrm{~m} \Omega+0.50 \mathrm{~m} \Omega) / 0.01 \mu \mathrm{~F} \\
& =71 \mathrm{k} \Omega
\end{aligned}
$$

Equation 32 will be most accurate for higher quality iron powder core materials such as the -2 or -8 from Micrometals. The permeability of these more expensive cores is relatively constant versus DC current, AC flux density and frequency. Less expensive core materials (such as the -52 from Micrometals) change their characteristics versus DC current, AC flux density, and frequency. The less expensive materials may yield acceptable converter performance if the current sense time constant is set approximately $1 \times-2 \times$ longer than anticipated. For example, use up to twice the resistance $\left(\mathrm{R}_{\mathrm{CSn}}\right)$ or twice the capacitance $\left(\mathrm{C}_{\mathrm{CSn}}\right)$ when using the less expensive core material. If we use -52 material for this design, the value of $\mathrm{R}_{\mathrm{CSn}}$ may need to be increased to $2 \times 71 \mathrm{k} \Omega$ or $142 \mathrm{k} \Omega$.

After the circuit is constructed, the values of $\mathrm{R}_{\mathrm{CSn}}$ and/or $\mathrm{C}_{\mathrm{CSn}}$ should be tuned to provide a "square-wave" at $\mathrm{V}_{\mathrm{DRP}}$ with minimal overshoot and fast rise time due to a step change in load current as shown in Figures 20-22.

## 8. Error Amplifier Tuning

The error amplifier is tuned by adjusting $\mathrm{C}_{\mathrm{AMP}}$ to provide an acceptable full-load transient response as shown in Figures 23-25. After a value for $\mathrm{C}_{\mathrm{AMP}}$ is chosen, the peak-to-peak voltage ripple on the COMP pin is examined under full-load to insure less than $20 \mathrm{mV}_{\mathrm{PP}}$ as shown in Figure 26.

## 9. Current Limit Setting

The maximum inductor resistance, the maximum PCB resistance, and the maximum current-sense gain as shown in Equation 34 determine the current limit. The maximum current, IOUT,LIM, was specified in the design requirements. The maximum inductor resistance occurs at full-load and the highest ambient temperature. This value was found in the "Output Inductor Section" ( $1.06 \mathrm{~m} \Omega$ ). This analysis assumes the PCB resistance only increases due to the change in ambient temperature. Component heating will also increase the PCB temperature but quantifying this effect is difficult. Lab testing should be used to "fine tune" the overcurrent threshold.

$$
\begin{aligned}
\mathrm{RPCB}, \mathrm{MAX}= & 0.50 \mathrm{~m} \Omega \cdot\left(1+0.39 \% /{ }^{\circ} \mathrm{C} \cdot(60-25)^{\circ} \mathrm{C}\right) \\
= & 0.57 \mathrm{~m} \Omega \\
\mathrm{~V}_{\text {ILIM }}= & \left(\mathrm{l} \text { OUT,LIM }+\Delta \mathrm{L}_{\mathrm{Lo}} / 2\right) \cdot\left(\mathrm{R}_{\mathrm{LMAX}}+\mathrm{RPCB}^{2}, \mathrm{MAX}\right) \\
& \cdot \mathrm{GILIM} \\
= & (52 \mathrm{~A}+8.03 \mathrm{~A} / 2) \cdot(1.33 \mathrm{~m} \Omega+0.57 \mathrm{~m} \Omega) \\
& \cdot 6.75 \mathrm{~V} / \mathrm{V} \\
= & 0.718 \mathrm{Vdc}
\end{aligned}
$$

Set the voltage at the $\mathrm{I}_{\text {LIM }}$ pin using a resistor divider from the 3.3 V reference output as shown in Figure 28. If the resistor from $\mathrm{I}_{\mathrm{LIM}}$ to GND is chosen as $1 \mathrm{k}\left(\mathrm{R}_{\mathrm{LIM}}\right)$, the resistor from $\mathrm{I}_{\text {LIM }}$ to 3.3 V can be calculated from:

$$
\begin{aligned}
\mathrm{R}_{\mathrm{LIM} 1} & =\left(\mathrm{V}_{\text {REF }}-\mathrm{V} \text { ILIM }\right) /\left(\mathrm{V} \text { ILIM } / \mathrm{R}_{\text {LIM }}\right) \\
& =(3.3 \mathrm{~V}-0.718 \mathrm{~V}) /(0.718 \mathrm{~V} / 1 \mathrm{k} \Omega) \\
& =3596 \Omega \text { or } 3.57 \mathrm{k} \Omega
\end{aligned}
$$



Figure 28. Setting the Current Limit

## 10. PWM Comparator Input Voltage

Use Equation 35 to check the voltage level to the positive pin of the internal PWM comparators. The design should not saturate the PWM comparator at maximum DAC output voltage ( $+1 \%$ error), AVP at full-load, $100 \%$ duty cycle (D $=1$ ), and worst-case maximum internal ramp ( 310 mV at $100 \%$ duty cycle):

$$
\begin{aligned}
\text { VCSREF,MAX } & =\text { Max VID Setting w/AVP @ Full-Load } \\
& =1.01 \cdot 1.850 \mathrm{~V}-30 \mathrm{mV}=1.834 \mathrm{~V}
\end{aligned}
$$

$$
\begin{align*}
& \mathrm{VCOn}, \mathrm{MAX} \\
&=\left(\mathrm{IO}, \mathrm{MAX} / 2+\Delta \mathrm{I}_{\mathrm{Lo}} / 2\right) \cdot \mathrm{RMAX} \cdot \mathrm{GCSA}, \mathrm{MAX} \\
&=(52 \mathrm{~A} / 2+8.03 \mathrm{~A} / 2) \cdot(1.33 \mathrm{~m} \Omega+0.57 \mathrm{~m} \Omega) \\
& \cdot 3.90 \mathrm{~V} / \mathrm{V} \\
&= 0.222 \mathrm{~V} \\
& \mathrm{~V} \tag{35}
\end{align*}
$$

This value is acceptable because it below the specified maximum of 2.45 V .

## 11. Soft Start Time

To set the Soft Start time, first calculate the external ramp size at a duty-cycle of $\mathrm{D}=1.630 \mathrm{~V} / 12 \mathrm{~V}=0.135$ :

$$
\begin{aligned}
\text { Ext_Ramp } & =\mathrm{D} \cdot \frac{\left(\mathrm{~V}_{\text {IN }}-\mathrm{V}_{\mathrm{OUT}}\right)}{\left(\mathrm{RCSn} \cdot \mathrm{C}_{\mathrm{CSn}} \cdot \mathrm{fSW}\right)} \\
& =0.135 \cdot \frac{(12 \mathrm{~V}-1.630 \mathrm{~V})}{60 \mathrm{k} \Omega \cdot 0.01 \mathrm{~F} \cdot 220 \mathrm{kHz})} \\
& =11 \mathrm{mV}
\end{aligned}
$$

Then calculate the steady-state COMP voltage:

$$
\begin{aligned}
\text { VCOMP }= & \text { VOUT @ } 0 \mathrm{~A}+\text { Channel_Startup_Offset } \\
& + \text { Int_Ramp }+ \text { GCSA } \cdot \text { Ext_Ramp } / 2 \\
= & 1.630 \mathrm{~V}+0.40 \mathrm{~V}+0.135 \cdot 250 \mathrm{mV} \\
& +3.5 \mathrm{~V} / \mathrm{V} \cdot 11 \mathrm{mV} / 2 \\
= & 2.083 \mathrm{~V}
\end{aligned}
$$

Then choose a convenient value for the Soft-Start time ( 7.5 ms ) and solve Equation 37 for the Soft-Start capacitor, $\mathrm{C}_{\mathrm{SS}}$ :

$$
\begin{align*}
\text { CSS } & =\mathrm{tSS} \cdot \text { ISS } / \mathrm{V}_{\mathrm{COMP}}  \tag{37}\\
& =7.5 \mathrm{~ms} \cdot 30 \mu \mathrm{~A} / 2.083 \mathrm{~V} \\
& =0.108 \mu \mathrm{~F} \text { or } 0.1 \mu \mathrm{~F}
\end{align*}
$$

$I_{\text {SS }}$ is the Soft-Start charge current from the data sheet.

## CS5323

## Three-Phase Buck Controller with 5-Bit DAC

The CS5323 is a three-phase step down controller that incorporates all control functions required to power next generation processors. Proprietary multi-phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced $V^{2 T M}$ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use.

The multi-phase architecture reduces input and output filter ripple, allowing for a reduction in filter size and inductor values with a corresponding increase in the output inductor current slew rate.

## Features

- Enhanced $\mathrm{V}^{2}$ Control Method
- 5-Bit DAC with $1.0 \%$ Tolerance
- Adjustable Output Voltage Positioning
- Programmable Frequency Set by Single Resistor
- 200 kHz to 800 kHz Operation (Per Phase)
- Current Sensed through Sense Resistors, or Buck Inductors
- Adjustable Current Sense Threshold
- Hiccup Mode Current Limit
- Over-Voltage Protection through Synchronous MOSFET's
- Individual Current Limits for Each Phase
- On-Board Current Sense Amplifiers
- $3.3 \mathrm{~V}, 1.0 \mathrm{~mA}$ Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through COMP Pin)

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SO-20L
DW SUFFIX
CASE 751D

PIN CONNECTIONS AND MARKING DIAGRAM


A $\quad=$ Assembly Location
WL, L = Wafer Lot
YY, $Y=$ Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5323GDW20 | SO-20L | 37 Units/Rail |
| CS5323GDWR20 | SO-20L | 1000 Tape \& Reel |



Figure 1. Application Diagram, 12 V to 1.7 V Converter

ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value | Unit |
| :--- | :---: | :---: | :---: |
| Operating Junction Temperature | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | 2.0 | kV |
| ESD Susceptibility (Human Body Model) |  |  |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Number | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 2 | COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 3 | $V_{F B}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 4 | $V_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 5-7 | CS1-CS3 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 8 | $\mathrm{CS}_{\text {REF }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 9 | ILIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 10 | REF | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| 11-15 | VID0-4 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| 16 | Gnd | 0 V | 0 V | $\begin{gathered} 0.4 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 100 \mathrm{~mA} \\ \mathrm{DC} \end{gathered}$ | N/A |
| 17-19 | GATE 1-3 | 16 V | -0.3 V | $0.1 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 25 \mathrm{~mA} \mathrm{DC}$ | $0.1 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 25 \mathrm{~mA} \mathrm{DC}$ |
| 20 | $\mathrm{V}_{\mathrm{CC}}$ | 16 V | -0.3 V | N/A | $\begin{gathered} 0.4 \mathrm{~A}, 1.0 \mu \mathrm{~s}, 100 \mathrm{~mA} \\ \mathrm{DC} \end{gathered}$ |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<85^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=100 \mathrm{pF}\right.$,
$R_{R(O S C)}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}$, $\mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $0=$ Connected to $\mathrm{V}_{\mathrm{SS}} ; 1=$ Open or Pull-up to 3.3 V )

| Accuracy (all codes) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ |  |  | $\pm 1.0$ | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {ID4 }}$ | VID3 | VID2 | VID1 | $\mathrm{V}_{\text {ID }}$ |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | - | 1.064 | 1.075 | 1.086 | V |
| 1 | 1 | 1 | 1 | 0 | - | 1.089 | 1.100 | 1.111 | V |
| 1 | 1 | 1 | 0 | 1 | - | 1.114 | 1.125 | 1.136 | V |
| 1 | 1 | 1 | 0 | 0 | - | 1.139 | 1.150 | 1.162 | V |
| 1 | 1 | 0 | 1 | 1 | - | 1.163 | 1.175 | 1.187 | V |
| 1 | 1 | 0 | 1 | 0 | - | 1.188 | 1.200 | 1.212 | V |
| 1 | 1 | 0 | 0 | 1 | - | 1.213 | 1.225 | 1.237 | V |
| 1 | 1 | 0 | 0 | 0 | - | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 1 | 1 | 1 | - | 1.262 | 1.275 | 1.288 | V |
| 1 | 0 | 1 | 1 | 0 | - | 1.287 | 1.300 | 1.313 | V |
| 1 | 0 | 1 | 0 | 1 | - | 1.312 | 1.325 | 1.338 | V |
| 1 | 0 | 1 | 0 | 0 | - | 1.337 | 1.350 | 1.364 | V |
| 1 | 0 | 0 | 1 | 1 | - | 1.361 | 1.375 | 1.389 | V |
| 1 | 0 | 0 | 1 | 0 | - | 1.386 | 1.400 | 1.414 | V |
| 1 | 0 | 0 | 0 | 1 | - | 1.411 | 1.425 | 1.439 | V |
| 1 | 0 | 0 | 0 | 0 | - | 1.436 | 1.450 | 1.465 | V |
| 0 | 1 | 1 | 1 | 1 | - | 1.460 | 1.475 | 1.490 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.485 | 1.500 | 1.515 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.510 | 1.525 | 1.540 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.535 | 1.550 | 1.566 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.559 | 1.575 | 1.591 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.584 | 1.600 | 1.616 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.609 | 1.625 | 1.641 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.634 | 1.650 | 1.667 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.683 | 1.700 | 1.717 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.708 | 1.725 | 1.742 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.733 | 1.750 | 1.768 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.757 | 1.775 | 1.793 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.782 | 1.800 | 1.818 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.807 | 1.825 | 1.843 | V |
| 0 | 0 | 0 | 0 | 0 | - | 1.832 | 1.850 | 1.869 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID4 }}, \mathrm{V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID }}$ | 1.00 | 1.25 | 1.50 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{\text {ID } 4}, \mathrm{~V}_{\text {ID3 }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID } 1}, \mathrm{~V}_{\text {ID }}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |
| Pull-up Voltage |  |  |  |  | - | 3.15 | 3.30 | 3.45 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<85^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=100 \mathrm{pF}\right.$, $R_{R(O S C)}=53.6 \mathrm{k}, \mathrm{C}_{\text {COMP }}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\text {REF }}=0.1 \mu \mathrm{~F}$, DAC Code $10000, \mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}$, $\mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Feedback Error Amplifier

| $V_{\text {FB }}$ Bias Current (Note 2) | $0.9 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.9 \mathrm{~V}$ | 17.6 | 19.0 | 20.6 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | $\mathrm{COMP}=0.5 \mathrm{~V}$ to $2.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V} ; \mathrm{DAC}=00000$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\mathrm{COMP}=0.5 \mathrm{~V}$ to $2.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V} ; \mathrm{DAC}=00000$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Discharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3 | 60 | 90 | - | dB |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ | - | 400 | - | kHz |
| PSRR @ 1 kHz | - | - | 70 | - | dB |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V}$; COMP Open; $\mathrm{DAC}=00000$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V}$; COMP Open; $\mathrm{DAC}=00000$ | - | 0.1 | 0.2 | V |
| Hiccup Latch Discharge Current | - | 2.0 | 5.0 | 10 | $\mu \mathrm{A}$ |
| COMP Discharge Ratio | - | 4.0 | 6.0 | 10 | - |

PWM Comparators

| Minimum Pulse Width | Measured from CSx to GATE(H) with 60 mV step between CSX and CS REF | - | 350 | 500 | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Channel Start Up Offset | $\mathrm{V}(\mathrm{CS} 1)=\mathrm{V}(\mathrm{CS} 2)=\mathrm{V}(\mathrm{CS} 3)=\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)$ <br> $\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$; Measure $\mathrm{V}(\mathrm{COMP})$ when <br> GATE (H) 1, 2 switch high | 0.3 | 0.4 | 0.5 | V |

## GATEs

| High Voltage | Measure $\mathrm{V}_{\mathrm{CC}}-\mathrm{GATEx}, \mathrm{I}_{\mathrm{GATEx}}=1.0 \mathrm{~mA}$ | - | 1.2 | 2.1 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Low Voltage | Measure GATEx, $\mathrm{I}_{\mathrm{GATEx}}=1.0 \mathrm{~mA}$ | - | 0.25 | 0.50 | V |
| Rise Time GATE | $1.0 \mathrm{~V}<\mathrm{GATE}<8.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | - | 30 | 60 | ns |
| Fall Time GATE | $8.0 \mathrm{~V}>$ GATE $>1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ | - | 30 | 60 | ns |

## Oscillator

| Switching Frequency | $\mathrm{R}_{\text {OSC }}=53.6 \mathrm{k}$ | 220 | 250 | 280 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | Note 3 R OSC $=32.4 \mathrm{k}$ | 300 | 400 | 500 | kHz |
| Switching Frequency | Note 3 R OSC $=16.2 \mathrm{k}$ | 600 | 800 | 1000 | kHz |
| Rosc Voltage |  | - | 1.00 | - | V |
| Phase Delay | Rising edge only | 105 | 120 | 135 | deg |

Adaptive Voltage Positioning

| $V_{\text {DRP }}$ Offset | $\begin{aligned} & \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS} 3=\mathrm{CS} \text { REF, } \mathrm{V}_{\mathrm{FB}}=\mathrm{COMP} \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | -20 | - | 20 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum V ${ }_{\text {DRP }}$ Voltage | $\begin{gathered} \left\|(C S 1=C S 2=C S 3)-C_{R E F}\right\|=50 \mathrm{mV}, \\ V_{F B}=C O M P, \text { Measure } V_{D R P}-C O M P \end{gathered}$ | 360 | 465 | 570 | mV |
| Current Share Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.7 | 3.0 | 3.5 | V/V |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of Rosc per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ( $0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<85^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<14 \mathrm{~V} ; \mathrm{C}_{\mathrm{GATE}}=100 \mathrm{pF}$, $R_{R(O S C)}=53.6 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code 10000, $\mathrm{C}_{\mathrm{VCC}}=0.1 \mu \mathrm{~F}, \mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Current Sensing and Sharing

| CS1-CS3 Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS ${ }_{\text {REF }}$ Input Bias Current | - | - | 0.6 | 2.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifier Gain | - | 3.7 | 4.2 | 4.7 | V/V |
| Current Sense Amp Mismatch (The sum of gain and offset errors) | $0<\left(C S x-S_{\text {REF }}\right)<50 \mathrm{mV}$ | -5.0 | - | 5.0 | mV |
| Current Sense Amplifiers Input Common Mode Range Limit | Note 4 | 0 | - | $\mathrm{V}_{\mathrm{CC}}-2$ | V |
| Current Sense Input to ILIM Gain | $0.25 \mathrm{~V}<1.20 \mathrm{~V}$ | 5.0 | 6.5 | 8.0 | $\mathrm{V} / \mathrm{V}$ |
| Current Limit Filter Slew Rate | Note 4 | 7.5 | 15 | 40 | $\mathrm{mV} / \mu \mathrm{s}$ |
| ILIM Bias Current | $0<\mathrm{I}_{\text {LIM }}<1.0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse by Pulse Current Limit: V(CSx) V (CS $\mathrm{CEF}^{\text {) }}$ | - | 75 | 105 | 115 | mV |
| Current Share Amplifier Bandwidth | Note 4 | 1.0 | - | - | mHz |

Reference Output

| $V_{\text {REF }}$ Output Voltage | $0 \mathrm{~mA}<\mathrm{I}\left(\mathrm{V}_{\text {REF }}\right)<1.0 \mathrm{~mA}$ | 3.2 | 3.3 | 3.4 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

## General Electrical Specifications

| $V_{C C}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP(no switching) | - | 23 | 28 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{CC}}$ Start Threshold | GATEs switching, COMP charging | 4.05 | 4.60 | 4.70 | V |
| $\mathrm{~V}_{\mathrm{CC}}$ Stop Threshold | GATEs stop switching, COMP discharging | 3.75 | 4.4 | 4.65 | V |
| $\mathrm{~V}_{\mathrm{CC}}$ Hysteresis | GATEs not switching, COMP not charging | 100 | 200 | 300 | mV |

4. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 20 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 1 | Rosc | A resistor from this pin to ground sets operating frequency and $\mathrm{V}_{\mathrm{FB}}$ bias current. |
| 2 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 3 | $V_{F B}$ | Voltage Feedback Pin. To use Adaptive Positioning, set the light load offset voltage by connecting a resistor between $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{CS}_{\text {REF. }}$ The resistor and the $\mathrm{V}_{\mathrm{FB}}$ bias current determine the offset. For no adaptive positioning connect $\mathrm{V}_{\mathrm{FB}}$ directly to CS REF- |
| 4 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for adaptive voltage positioning (AVP). The level of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $\mathrm{V}_{\mathrm{FB}}$ to set AVP or leave this pin open for no AVP. |
| 5-7 | CS1-CS3 | Current sense inputs. Connect current sense network for the corresponding phase to each CSx pin. |
| 8 | CS REF | Reference for Current Sense Amplifiers. To balance input offset voltages between the inverting and noninverting inputs of the Current Sense Amplifiers, connect a resistor between CS REF and the output voltage. The value should be $1 / 3$ of the value of the resistors connected to the CSx pins. |
| 9 | ILIM | Sets the threshold for hiccup mode current limit. Connect to reference through a resistive divider. |
| 10 | REF | Reference output. Decouple with $0.1 \mu \mathrm{~F}$. |
| 11-15 | VID0-VID4 | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |
| 16 | Gnd | IC Gnd. |
| 17-19 | GATE1-3 | GATE drive signal. |
| 20 | $\mathrm{V}_{\mathrm{CC}}$ | Power for IC. |



Fiqure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Oscillator Frequency


Figure 4. $\mathrm{V}_{\mathrm{FB}}$ Bias Current vs. Rosc Value

## APPLICATIONS INFORMATION

## FIXED FREQUENCY MULTI-PHASE CONTROL

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5323 uses a three-phase, fixed frequency, enhanced $\mathrm{V}^{2}$ architecture. Each phase is delayed $120^{\circ}$ from the previous phase. Normally the GATE transitions high at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator and bring the GATE low. Once the GATE goes low, it will remain low until the beginning of the next oscillator cycle. While the GATE is high, the enhanced $\mathrm{V}^{2}$ loop will respond to line and load transients. Once the GATE is low, the loop will not respond again until the beginning of the next cycle. Therefore, constant frequency, enhanced $\mathrm{V}^{2}$ will typically respond within the off-time of the converter.

The enhanced $\mathrm{V}^{2}$ architecture measures and adjusts current in each phase. An additional input ( $\mathrm{C}_{\mathrm{X}}$ ) for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 5.


Figure 5. Enhanced V ${ }^{2}$ Feedback and Current Sense Scheme

The inductor current is measured across $\mathrm{R}_{\mathrm{S}}$, amplified by CSA and summed with the OFFSET and Output Voltage at the non-inverting input of the PWM comparator. The inductor current provides the PWM ramp and as inductor current increases the voltage on the positive pin of the pwm
comparator rises and terminates the pwm cycle. If the inductor starts the cycle with a higher current the PWM cycle will terminate earlier providing negative feedback. The CS5323 provides a $\mathrm{C}_{\mathrm{X}}$ input for each phase, but the $\mathrm{CS}_{\mathrm{REF}}, \mathrm{V}_{\mathrm{FB}}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{V}_{\mathrm{FB}}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than phases with a smaller current signal.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. If the COMP pin is held steady and the inductor current changes there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$
\Delta \mathrm{V}=\mathrm{RS} \times \mathrm{CSA} \text { Gain } \times \Delta \mathrm{I}
$$

The single-phase power stage output impedance is;
Single Stage Impedance $=\Delta \mathrm{V} / \Delta \mathrm{I}=\mathrm{RS} \times$ CSA Gain.
The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few $\mu$ s of a transient before the feedback loop has repositioned the COMP pin.

The peak output current of each phase can also be calculated from;

$$
\text { Ipkout }(\text { per phase })=\frac{V_{\mathrm{COMP}}-\mathrm{V}_{\mathrm{FB}}-\mathrm{V}_{\mathrm{OFFSET}}}{\mathrm{R}_{\mathrm{S}} \times \mathrm{CSA} \text { Gain }}
$$

Figure 6 shows the step response of a single phase with the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides the pwm ramp through the Current Share Amplifier. The pwm cycle ends when the sum of the current signal, voltage signal and OFFSET exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next pwm cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the current signal level is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 6. Open Loop Operation

## Inductive Current Sensing

For lossless sensing current can be sensed across the inductor as shown below in Figure 7. In the diagram, L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal the values of R1 and C 1 are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} 1 \times \mathrm{C} 1$. If this criteria is met the current sense signal will be the same shape as the inductor current, the voltage signal at $C x$ will represent the instantaneous value of inductor current and the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$.


Figure 7. Lossless Inductive Current Sensing with Enhanced ${ }^{2}{ }^{2}$
When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be
considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 5.

## Current Sharing Accuracy

PCB traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at the same point for each phase and the connection to the $\mathrm{CS}_{\text {REF }}$ should be made so that no phase is favored. (In some cases, especially with inductive sensing, resistance of the pcb can be useful for increasing the current sense resistance.) The total current sense resistance used for calculations must include any pcb trace between the CS inputs and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier Input Mismatch and the value of the current sense element will determine the accuracy of current sharing between phases. The worst case Current Sense Amplifier Input Mismatch is 5 mV and will typically be within 3 mV . The difference in peak currents between phases will be the CSA Input Mismatch divided by the current sense resistance. If all current sense elements are of equal resistance a 3 mV mismatch with a $2 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## Operation at > 50\% Duty Cycle

For operation at duty cycles above $50 \%$ Enhanced V ${ }^{2}$ will exhibit subharmonic oscillation unless a compensation ramp is added to each phase. A circuit like the one on the left side of Figure 8 can be added to each current sense network to implement slope compensation. The value of R1 can be varied to adjust the ramp size.


Figure 8. External Slope Compensation Circuit

## Ramp Size and Current Sensing

Because the current ramp is used for both the PWM ramp and to sense current, the inductor and sense resistor values will be constrained. A small ramp will provide a quick transient response by minimizing the difference over which the COMP pin must travel between light and heavy loads, but a steady state ramp of $25 \mathrm{mV}_{\mathrm{P}-\mathrm{P}}$ or greater is typically required to prevent pulse skipping and minimize pulse width jitter. For resistive current sensing the combination of the inductor and sense resistor values must be chosen to provide a large enough steady state ramp. For large inductor values the sense resistor value must also be increased.

For inductive current sensing the RC network must meet the requirement of $L / R_{L}=R \times C$ to accurately sense the $A C$ and DC components of the current the signal. Again the values for L and $\mathrm{R}_{\mathrm{L}}$ will be constrained in order to provide a large enough steady state ramp with a compensated current sense signal. A smaller $L$, or a larger $R_{L}$ than optimum might be required. But unlike resistive sensing, with inductive sensing small adjustments can be made easily with the values of R and C to increase the ramp size if needed.

If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R} \times \mathrm{C}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R} \times \mathrm{C}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During transients the COMP pin will be required to overshoot along with the current signal in order to maintain the output voltage. The $\mathrm{V}_{\mathrm{DRP}}$ pin will also overshoot during transients and possibly slow the response. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 9 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}$, $\mathrm{R}_{\mathrm{L}}=1.6 \mathrm{~m} \Omega, \mathrm{R} 1=20 \mathrm{k}$ and $\mathrm{C} 1=.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of R1 should be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu \mathrm{~s}$ time constant. With this compensation the $\mathrm{I}_{\text {LIM }}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 9. Inductive Sensing waveform during a Step with Fast RC Time Constant ( $50 \mathrm{us} / \mathrm{div}$ )

## Current Limit

Two levels of overcurrent protection are provided. Any time the voltage on a Current Sense pin exceeds CS $_{\text {REF }}$ by more than the Single Phase Pulse by Pulse Current Limit, the pwm comparator for that phase is turned off. This provides fast peak current protection for individual phases. The outputs of all the currents are also summed and filtered to compare an averaged current signal to the voltage on the $\mathrm{I}_{\text {LIM }}$ pin. If this voltage is exceeded, the fault latch trips and the SS capacitor is discharged by a $5 \mu \mathrm{~A}$ source until the COMP pin reaches 0.2 V . Then soft-start begins. The converter will continue to operate in this mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the enhanced $\mathrm{V}^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET's to shut off, and the synchronous MOSFET's to turn on. This results in a "crowbar" action to clamp the output voltage and prevents damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in
order to reduce voltage excursions during transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher at light loads to reduce output voltage sag when the load current is stepped up and set lower during heavy loads to reduce overshoot when the load current is stepped up. For low current applications a droop resistor can provide fast accurate adaptive positioning. However at high currents, the loss in a droop resistor becomes excessive. For example; in a 50 A converter a $1 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond quickly to changes in load current. Figure 10 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 10. Adaptive Positioning
The CS5323 uses two methods to provide fast and accurate adaptive positioning. For low frequency positioning the $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{DRP}}$ pins are used to adjust the output voltage with varying load currents. For high frequency positioning, the current sense input pins can be used to control the power stage output impedance. The transition between fast and slow positioning is adjusted by the error amp compensation.

The CS5323 can be configured to adjust the output voltage based on the output current of the converter. The adaptive positioning circuit is designed to select the DAC setting as the maximum output voltage. (Refer to Figure 1 on page 2436.)

To set the no-load positioning a resistor (R9) is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to decrease the output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of ROSC. See Figure 4 on the datasheet.

During no load conditions the $\mathrm{V}_{\text {DRP }}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\mathrm{DRP}}$ resistor (R6). When output current
increases the $\mathrm{V}_{\text {DRP }}$ pin increases proportionally and the $\mathrm{V}_{\mathrm{DRP}}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to further decrease.

The $V_{F B}$ and $V_{\text {DRP }}$ pins take care of the slower and DC voltage positioning. The first few $\mu \mathrm{s}$ are controlled primarily by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

Note: Large levels of adaptive positioning can cause pulse width jitter.

## Error Amp Compensation

The transconductance error amplifier can be configured to provide both a slow soft-start and a fast transient response. C 4 in the main applications diagram controls soft-start. A $0.1 \mu \mathrm{~F}$ capacitor with the $30 \mu \mathrm{~A}$ error amplifier output capability will allow the output to ramp up at $0.3 \mathrm{~V} / \mathrm{ms}$ or 1.5 V in 5 ms .

R 10 is connected in series with C 4 to allow the error amplifier to slew quickly over a narrow range during load transients. Here the $30 \mu \mathrm{~A}$ error amplifier output capability works against $8 \mathrm{k} \Omega$ (R10) to limit the window of fast slewing too 240 mV - enough to allow for fast transients, but not enough to interfere with soft-start. This window will be noticeable as a step in the COMP pin voltage at start-up. The size of this step must be kept smaller than the Channel Start-Up Offset (nominally 0.4 V ) for proper soft-start operation. If adaptive positioning is used the R9 and R8 form a divider with the $\mathrm{V}_{\mathrm{DRP}}$ end held at the DAC voltage during start-up, which effectively makes the Channel Start-Up Offset larger.

C12 is included for error amp stability. A capacitive load is required on the error amp output. Use of values less than 1 nF may result in error amp oscillation of several MHz .

C 11 and the parallel resistance of the $\mathrm{V}_{\mathrm{FB}}$ resistor (R9) and the $V_{\text {DRP }}$ resistor (R6) are used to roll off the error amp gain. C28 adds a zero to the error amp response to boost the phase near the crossover frequency.

## UVLO

The CS5323 has one undervoltage lockout function connected to the $\mathrm{V}_{\mathrm{CC}}$ pin. In applications where the converter is powered from multiple voltages, additional UVLO protection might be required if the voltage powering the controller can turn on before other voltages.

For the $12 \mathrm{~V}_{\text {IN }}$ converter in Figure 1, the CS5323 UVLO function monitors the 5.0 V supply. If the 5.0 V supply comes up before the 12 V supply, the COMP pin will rise until it reaches the upper rail or until the 12 V supply comes up and the converter comes into regulation. If the delay between the 5.0 V and 12 V supplies is too long, soft-start will be compromised. A diode connected from the 12 V supply to the COMP pin can hold the COMP pin down until the 12 V supply starts to come up. Or, if a higher UVLO
threshold is needed, a circuit like the one in Figure 11 will lock out the converter until the 12 V supply reaches about 7.0 V.


Figure 11. External UVLO Circuit

## Remote Sense

In some applications that require remote output voltage sensing, there are conditions when the path of the feedback signal can be broken. In a voltage regulator module (VRM) the remote voltage feedback sense point is typically off the module. If the module is powered apart from the intended application, the feedback will be left open. On a motherboard, the feedback path might be broken when the processor socket is left open. Without the feedback connection the output voltage is likely to exceed the intended voltage. To protect the circuit from overvoltage conditions, a resistor can be connected between the local output voltage and the remote sense line as shown in Figure 12.


Figure 12. Remote Sense Connection

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to reroute the currents away from the
controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.
Voltage feedback should be taken from a point of the output or the output filter that doesn't favor any one phase. If the feedback connection is closer to one inductor than the others the ripple associated with that phase may appear larger than the ripple associated with the other phases and poor current sharing can result.
The current sense signal is typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as switch nodes and gate drive signals. The paths should be matched as well as possible. It is especially important that all current sense signals be picked off at similar points for accurate current sharing. If the current signal is taken from a place other than directly at the inductor any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistance and should be considered in design calculations. Capacitors for the current feedback networks should be placed as close to the current sense pins as practical.

## DESIGN PROCEDURE

## Current Sensing, Power Stage and Output Filter Components

1. Choose the output filter components to meet peak transient requirements. The formula below can be used to provide an approximate starting point for capacitor choice, but will be inadequate to calculate actual values.

$$
\Delta \mathrm{V}_{\mathrm{PEAK}}=(\Delta \mathrm{I} / \Delta \mathrm{T}) \times \mathrm{ESL}+\Delta \mathrm{I} \times \mathrm{ESR}
$$

Ideally the output filter should be simulated with models including ESR, ESL, circuit board parasitics and delays due to switching frequency and converter response. Typically both bulk capacitance (electrolytic, Oscon, etc,) and low impedance capacitance (ceramic chip) will be required. The bulk capacitance provides "hold up" during the converter response. The low impedance capacitance reduces steady state ripple and bypasses the bulk capacitance during slewing of output current.
2. For inductive current sensing (only) choose the current sense network RC to provide a 25 mV minimum ramp during steady state operation.

$$
\mathrm{R}=\left(\mathrm{V}_{\text {IN }}-\mathrm{V}_{\text {OUT }}\right) \times \frac{\mathrm{V}_{\text {OUT }} / \mathrm{V}_{\text {IN }}}{\mathrm{F} \times \mathrm{C} \times 25 \mathrm{mV}}
$$

Then choose the inductor value and inherent resistance to satisfy $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} \times \mathrm{C}$.
For ideal current sense compensation the ratio of $L$ and $R_{L}$ is fixed, so the values of $L$ and $R_{L}$ will be a compromise typically with the maximum value $\mathrm{R}_{\mathrm{L}}$ limited by conduction losses or inductor temperature rise and the minimum value of $L$ limited by ripple current.
3. For resistive current sensing choose $L$ and $R_{S}$ to provide a steady state ramp greater than 25 mV .

$$
\mathrm{L} / \mathrm{RS}_{\mathrm{S}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{TON} / 25 \mathrm{mV}
$$

Again the ratio of L and $\mathrm{R}_{\mathrm{L}}$ is fixed and the values of L and $\mathrm{R}_{\mathrm{S}}$ will be a compromise.
4. Calculate the high frequency output impedance (ConverterZ) of the converter during transients. This is the impedance of the Output filter ESR in parallel with the power stage output impedance (PwrstgZ) and will indicate how far from the original level $(\Delta \mathrm{VR})$ the output voltage will typically recover to within one switching cycle. For a good transient response $\Delta \mathrm{VR}$ should be less than the peak output voltage overshoot or undershoot.

$$
\begin{array}{r}
\Delta V R=\text { ConverterZ } \times \text { ESR } \\
\text { ConverterZ }=\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+ \text { ESR }}
\end{array}
$$

where:

$$
\text { PwrstgZ }=\text { RS } \times \text { CSA Gain } / 3
$$

Multiply the converterZ by the output current step size to calculate where the output voltage should recover to within the first switching cycle after a transient. If the ConverterZ is higher than the value required to recover to where the adaptive positioning is set the remainder of the recovery will be controlled by the error amp compensation and will typically recover in $10-20 \mu \mathrm{~s}$.

$$
\Delta \mathrm{VR}=\Delta \mathrm{I} \mathrm{OUT} \times \text { ConverterZ }
$$

Make sure that $\Delta \mathrm{VR}$ is less than the expected peak transient for a good transient response.
5. Adjust L and $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ as required to meet the best combination of transient response, steady state output voltage ripple and pulse width jitter.

## Current Limit

When the sum of the Current Sense amplifiers ( $\mathrm{V}_{\text {ITOTAL }}$ ) exceeds the voltage on the $\mathrm{I}_{\text {LIM }}$ pin the part will enter hiccup mode. For inductive sensing the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor resistance (or current sense resistor) at max temperature and max current. To set the level of the $I_{\text {LIM }}$ pin:
6. $\mathrm{V}_{\mathrm{I}(\mathrm{LIM})}=\mathrm{R} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS}$ to ILIM Gain
where:
R is $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$;
$I_{\text {OUT(LIM) }}$ is the current limit threshold.
For the overcurrent to work properly the inductor time constant $(\mathrm{L} / \mathrm{R})$ should be $\leq$ the Current sense RC. If the RC is too fast, during step loads the current waveform will appear larger than it is (typically for a few hundred $\mu \mathrm{s}$ ) and may trip the current limit at a level lower than the DC limit.

## Adaptive Positioning

7. To set the amount of voltage positioning below the DAC setting at no load connect a resistor ( $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ ) between the output voltage and the $\mathrm{V}_{\mathrm{FB}}$ pin. Choose $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ as;

$$
R V(F B)=N L \text { Position } / V_{F B} \text { Bias Current }
$$

See Figure 4 for $V_{F B}$ Bias Current.
8. To set the difference in output voltage between no load and full load, connect a resistor $\left(\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}\right)$ between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pins. $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ can be calculated in two steps. First calculate the difference between the $\mathrm{V}_{\mathrm{DRP}}$ and $V_{F B}$ pin at full load. (The $V_{F B}$ voltage should be the same as the DAC voltage during closed loop operation.) Then choose the $\mathrm{R}_{V(\mathrm{DRP})}$ to source enough current across $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ for the desired change in output voltage.

$$
\Delta V_{V}(D R P)=I O U T F L \times R \times C S \text { to } V_{D R P} \text { Gain }
$$

where:
$\mathrm{R}=\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ for one phase;
$I_{O U T F L}$ is the full load output current.

$$
\mathrm{RV}(\mathrm{DRP})=\Delta \mathrm{V}_{\mathrm{DRP}} \times \operatorname{RV}(\mathrm{FB}) / \Delta \mathrm{V}_{\mathrm{OUT}}
$$

## Calculate Input Filter Capacitor Current Ripple

The procedure below assumes that phases do not overlap and output inductor ripple current $(\mathrm{P}-\mathrm{P})$ is less than the average output current of one phase.
9. Calculate Input Current
$\mathrm{I}_{\mathrm{I}}=\frac{\mathrm{V}_{\text {OUT }} \times \mathrm{I}_{\mathrm{OUT}}}{\left(\text { Efficiency } \times \mathrm{V}_{\mathrm{IN}}\right)}$
10. Calculate Duty Cycle (per phase).

Duty Cycle $=\frac{\text { VOUT }}{\left(\text { Efficiency } \times \mathrm{V}_{\text {IN }}\right)}$
11. Calculate Apparent Duty Cycle.

## Apparent Duty Cycle $=$ Duty Cycle $\times \#$ of Phases

12. Calculate Input Filter Capacitor Ripple Current. Use the chart in Figure 13 to calculate the normalized ripple current ( $\mathrm{K}_{\mathrm{RMS}}$ ) based on the reciprocal of Apparent Duty Cycle. Then multiply the input current by $K_{\text {RMS }}$ to obtain the Input Filter Capacitor Ripple Current.

Ripple $(\mathrm{RMS})=\mathrm{I}_{\mathrm{I}} \times \mathrm{K}_{\mathrm{RMS}}$


Figure 13. Normalized Input Filter Capacitor Ripple Current

## DESIGN EXAMPLE

Choose the component values for lossless current sensing, adaptive positioning and current limit for a 12 V to 1.5 V 60 A converter. The adaptive positioning is chosen 20 mV below the maximum $\mathrm{V}_{\text {OUT }}$ at no load and 70 mV below the no-load position with 60 A out. The peak output voltage transient is 100 mV max during a 60 A step current. The overcurrent limit is nominally 75 A .

## Current Sensing, Power Stage and Output Filter Components

1. Assume $1.5 \mathrm{~m} \Omega$ of output filter ESR.
2. $\mathrm{R}=\left(\mathrm{VIN}-\mathrm{V}_{\mathrm{OUT}}\right) \times\left(\mathrm{V}_{\mathrm{OUT}} / \mathrm{VIN}_{\mathrm{IN}}\right) /(\mathrm{F} \times \mathrm{C} \times 25 \mathrm{mV})$

$$
=(12-1.5) \times(1.5 / 12) /(250 \mathrm{k} \times .01 \mu \mathrm{~F} \times 25 \mathrm{mV})
$$

$$
=21 \mathrm{k} \Omega \Rightarrow \text { Choose } 20 \mathrm{k} \Omega
$$

$\mathrm{L} / \mathrm{R}_{\mathrm{L}}=.01 \mu \mathrm{~F} \times 20 \mathrm{k} \Omega=200 \mu \mathrm{~s}$
Choose RL $=2.0 \mathrm{~m} \Omega$
$\mathrm{L}=2 \mathrm{~m} \Omega \times 200 \mu \mathrm{~s}=400 \mathrm{nH}$
3. $n / a$
4. PwrstgZ $=R_{L} \times$ CSA Gain $/ 3$

$$
=1.5 \mathrm{~m} \Omega \times 4.2 / 3=2.1 \mathrm{~m} \Omega
$$

$$
\begin{aligned}
\text { ConverterZ } & =\frac{\text { Pwrstg } Z \times \mathrm{ESR}}{\text { PwrstgZ }+\mathrm{ESR}} \\
& =\frac{2.8 \mathrm{~m} \Omega \times 1.5 \mathrm{~m} \Omega}{2.8 \mathrm{~m} \Omega+1.5 \mathrm{~m} \Omega} \cong 1.0 \mathrm{~m} \Omega
\end{aligned}
$$

$$
\Delta \mathrm{VR}=1.0 \mathrm{~m} \Omega \times 60 \mathrm{~A}=60 \mathrm{mV}
$$

5. n/a

## Current Limit

$$
\text { 6. } \begin{aligned}
\mathrm{V}_{\mathrm{I}(\mathrm{LIM})} & =R_{\mathrm{L}} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS} \text { to ILIM Gain } \\
& =1.5 \mathrm{~m} \Omega \times 75 \mathrm{~A} \times 6.5=731 \mathrm{mV}
\end{aligned}
$$

## Adaptive Positioning

9. $\mathrm{I}_{\mathrm{I}} \mathrm{N}=\frac{1.6 \mathrm{~V} \times 60 \mathrm{~A}}{\left(0.85 \times 12 \mathrm{~V}_{\mathrm{IN}}\right)}=9.4 \mathrm{~A}$
10. Duty Cycle $=\frac{1.6 \mathrm{~V}}{\left(0.85 \times 12 \mathrm{~V}_{\mathrm{IN}}\right)}=0.16$
11. Apparent Duty Cycle $=0.16 \times 3.0=0.48$
12. RMS ripple is $9.4 \mathrm{~A} \times 1.0=9.4 \mathrm{~A}$

$$
\begin{aligned}
& \text { 7. } \mathrm{RV}_{\mathrm{V}}(\mathrm{FB})=\mathrm{NL} \text { Position } / \mathrm{V}_{\mathrm{FB}} \text { Bias Current } \\
& =20 \mathrm{mV} / 19 \mu \mathrm{~A} \cong 1.00 \mathrm{k} \Omega \\
& \text { 8. } \Delta V_{\text {DRP }}=\text { RL } \times \text { IOUT } \times \text { Current Sense to VDRP Gain } \\
& =2 \mathrm{~m} \Omega \times 60 \mathrm{~A} \times 3=360 \mathrm{mV} \\
& R V(D R P)=\Delta V_{D R P} \times R V(F B) / \Delta V O U T \\
& =360 \mathrm{mV} \times 1.00 \mathrm{k} \Omega / 50 \mathrm{mV}=7.2 \mathrm{k} \Omega
\end{aligned}
$$

PACKAGE THERMAL DATA

| Parameter |  | SO-20L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 17 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 90 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS5332

## Two-Phase Buck Controller with Integrated Gate Drivers for VRM 9.0

The CS5332 is a two-phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi-phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced V ${ }^{2 T M}$ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use.

The CS5332 multi-phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in inductor values and a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

## Features

- Enhanced $\mathrm{V}^{2}$ Control Method
- VRM 9.0 Compatible 5-Bit DAC with $1.0 \%$ Accuracy
- Adjustable Output Voltage Positioning
- 4 On-Board GATE Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors, or Sense Resistors
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On-Board Current Sense Amplifiers
- $3.3 \mathrm{~V}, 1.0 \mathrm{~mA}$ Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through Soft Start Pin)
- Power Good Output with Internal Delay

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS5332GDW28 | SO-28L | 27 Units/Rail |
| CS5332GDWR28 | SO-28L | 1000 Tape \& Reel |



Figure 1. Application Diagram, Pentium ${ }^{\mathrm{TM}} 4$ Converter

## ABSOLUTE MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Operating Junction Temperature | Reflow: (SMD styles only) (Note 1 ) | 230 peak |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |
| Storage Temperature Range | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power for Logic | $\mathrm{V}_{\text {CCL }}$ | 16 V | -0.3 V | N/A | 50 mA |
| Power for GATE(L)1 | $\mathrm{V}_{\text {CCL1 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for GATE(L)2 | $\mathrm{V}_{\text {CCL2 }}$ | 16 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for GATE(H)1 | $\mathrm{V}_{\mathrm{CCH} 1}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power for GATE(H)2 | $\mathrm{V}_{\mathrm{CCH} 2}$ | 20 V | -0.3 V | N/A | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Power Good Output | PWRGD | 6.0 V | -0.3 V | 1.0 mA | 20 mA |
| Soft Start Capacitor | SS | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Compensation Network | COMP | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage Feedback Input | $V_{F B}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Output for Adjusting Adaptive Voltage Positioning | $\mathrm{V}_{\text {DRP }}$ | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Frequency Resistor | Rosc | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Reference Output | REF | 6.0 V | -0.3 V | 1.0 mA | 50 mA |
| High-Side FET Drivers | GATE(H)1-2 | 20 V | $\begin{gathered} -0.3 \mathrm{~V} \text { DC } \\ -2.0 \mathrm{~V} \text { for } 100 \mathrm{nS} \end{gathered}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Low-Side FET Drivers | GATE(L)1-2 | 16 V | $\begin{gathered} -0.3 \mathrm{~V} \mathrm{DC} \\ -2.0 \mathrm{~V} \text { for } 100 \mathrm{nS} \end{gathered}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | $1.5 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ |
| Return for Logic | LGND | N/A | N/A | 50 mA | N/A |
| Return for \#1 Driver | GND1 | 0.3 V | -0.3 V | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Return for \#2 Driver | GND2 | 0.3 V | -0.3 V | $2.0 \mathrm{~A}, 1.0 \mu \mathrm{~s} 200 \mathrm{~mA} \mathrm{DC}$ | N/A |
| Current Sense for Phases 1-2 | CS1-CS2 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Limit Set Point | ILIM | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Current Sense Reference | CS REF | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| Voltage ID DAC Inputs | VID0-4 | 6.0 V | -0.3 V | 1.0 mA | 1.0 mA |

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$;
$\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code 10000, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{l}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Voltage Identification DAC ( $0=$ Connected to $\mathrm{V}_{\mathrm{SS}} ; 1=$ Open or Pull-up to 3.3 V )

| Accuracy (all codes) |  |  |  |  | Measure $\mathrm{V}_{\mathrm{FB}}=\mathrm{COMP}$ |  |  | $\pm 1.0$ | \% |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VID4 | VID3 | VID2 | $V_{\text {ID1 }}$ | $\mathrm{V}_{\text {IDO }}$ |  |  |  |  |  |
| 1 | 1 | 1 | 1 | 1 | - | 1.064 | 1.075 | 1.086 | V |
| 1 | 1 | 1 | 1 | 0 | - | 1.089 | 1.100 | 1.111 | V |
| 1 | 1 | 1 | 0 | 1 | - | 1.114 | 1.125 | 1.136 | V |
| 1 | 1 | 1 | 0 | 0 | - | 1.139 | 1.150 | 1.162 | V |
| 1 | 1 | 0 | 1 | 1 | - | 1.163 | 1.175 | 1.187 | V |
| 1 | 1 | 0 | 1 | 0 | - | 1.188 | 1.200 | 1.212 | V |
| 1 | 1 | 0 | 0 | 1 | - | 1.213 | 1.225 | 1.237 | V |
| 1 | 1 | 0 | 0 | 0 | - | 1.238 | 1.250 | 1.263 | V |
| 1 | 0 | 1 | 1 | 1 | - | 1.262 | 1.275 | 1.288 | V |
| 1 | 0 | 1 | 1 | 0 | - | 1.287 | 1.300 | 1.313 | V |
| 1 | 0 | 1 | 0 | 1 | - | 1.312 | 1.325 | 1.338 | V |
| 1 | 0 | 1 | 0 | 0 | - | 1.337 | 1.350 | 1.364 | V |
| 1 | 0 | 0 | 1 | 1 | - | 1.361 | 1.375 | 1.389 | V |
| 1 | 0 | 0 | 1 | 0 | - | 1.386 | 1.400 | 1.414 | V |
| 1 | 0 | 0 | 0 | 1 | - | 1.411 | 1.425 | 1.439 | V |
| 1 | 0 | 0 | 0 | 0 | - | 1.436 | 1.450 | 1.465 | V |
| 0 | 1 | 1 | 1 | 1 | - | 1.460 | 1.475 | 1.490 | V |
| 0 | 1 | 1 | 1 | 0 | - | 1.485 | 1.500 | 1.515 | V |
| 0 | 1 | 1 | 0 | 1 | - | 1.510 | 1.525 | 1.540 | V |
| 0 | 1 | 1 | 0 | 0 | - | 1.535 | 1.550 | 1.566 | V |
| 0 | 1 | 0 | 1 | 1 | - | 1.559 | 1.575 | 1.591 | V |
| 0 | 1 | 0 | 1 | 0 | - | 1.584 | 1.600 | 1.616 | V |
| 0 | 1 | 0 | 0 | 1 | - | 1.609 | 1.625 | 1.641 | V |
| 0 | 1 | 0 | 0 | 0 | - | 1.634 | 1.650 | 1.667 | V |
| 0 | 0 | 1 | 1 | 1 | - | 1.658 | 1.675 | 1.692 | V |
| 0 | 0 | 1 | 1 | 0 | - | 1.683 | 1.700 | 1.717 | V |
| 0 | 0 | 1 | 0 | 1 | - | 1.708 | 1.725 | 1.742 | V |
| 0 | 0 | 1 | 0 | 0 | - | 1.733 | 1.750 | 1.768 | V |
| 0 | 0 | 0 | 1 | 1 | - | 1.757 | 1.775 | 1.793 | V |
| 0 | 0 | 0 | 1 | 0 | - | 1.782 | 1.800 | 1.818 | V |
| 0 | 0 | 0 | 0 | 1 | - | 1.807 | 1.825 | 1.843 | V |
| 0 | 0 | 0 | 0 | 0 | - | 1.832 | 1.850 | 1.869 | V |
| Input Threshold |  |  |  |  | $\mathrm{V}_{\text {ID } 4}, \mathrm{~V}_{\text {ID }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 1.00 | 1.25 | 1.50 | V |
| Input Pull-up Resistance |  |  |  |  | $\mathrm{V}_{I D 4}, \mathrm{~V}_{\text {ID }}, \mathrm{V}_{\text {ID2 }}, \mathrm{V}_{\text {ID1 }}, \mathrm{V}_{\text {ID0 }}$ | 25 | 50 | 100 | k $\Omega$ |
| Pull-up Voltage |  |  |  |  | - | 3.15 | 3.30 | 3.45 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}, \mathrm{DAC}$ Code 10000, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power-Good Output |  |  |  |  |  |
| Power Good Fault Delay | $C S_{\text {REF }}=\mathrm{V}_{\text {DAC }}$ to $\mathrm{V}_{\text {DAC }} \pm 15 \%$ | 25 | 50 | 125 | $\mu \mathrm{s}$ |
| Output Low Voltage | $\mathrm{CS}_{\text {REF }}=1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{PWRGD}}=4.0 \mathrm{~mA}$ | - | 0.25 | 0.40 | V |
| Output Leakage Current | $\mathrm{CS}_{\text {REF }}=1.45 \mathrm{~V}, \mathrm{PWRGD}=5.5 \mathrm{~V}$ | - | 0.1 | 10.0 | $\mu \mathrm{A}$ |
| Lower Threshold | \% of Nominal VID Code | -18 | -14 | -10 | \% |
| Upper Threshold | - | 1.9 | 2.0 | 2.1 | V |

Voltage Feedback Error Amplifier

| $V_{\text {FB }}$ Bias Current (Note 2) | $1.0 \mathrm{~V}<\mathrm{V}_{\mathrm{FB}}<1.9 \mathrm{~V}$ | 28.5 | 31 | 33.5 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMP Source Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.8 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Sink Current | $\begin{aligned} \mathrm{COMP} & =0.5 \mathrm{~V} \text { to } 2.0 \mathrm{~V} ; \\ \mathrm{V}_{\mathrm{FB}} & =1.9 \mathrm{~V} ; \mathrm{DAC}=00000 \end{aligned}$ | 15 | 30 | 60 | $\mu \mathrm{A}$ |
| COMP Max Voltage | $\mathrm{V}_{\mathrm{FB}}=1.8 \mathrm{~V}$ COMP Open; DAC $=00000$ | 2.4 | 2.7 | - | V |
| COMP Min Voltage | $\mathrm{V}_{\mathrm{FB}}=1.9 \mathrm{~V}$ COMP Open; $\mathrm{DAC}=00000$ | - | 0.1 | 0.2 | V |
| Transconductance | $-10 \mu \mathrm{~A}<\mathrm{I}_{\text {COMP }}<+10 \mu \mathrm{~A}$ | - | 32 | - | mmho |
| Output Impedance | - | - | 2.5 | - | $\mathrm{M} \Omega$ |
| Open Loop DC Gain | Note 3 | 60 | 90 | - | dB |
| Unity Gain Bandwidth | $0.01 \mu \mathrm{~F}$ COMP Capacitor | - | 400 | - | kHz |
| PSRR @ 1.0 kHz | - | - | 70 | - | dB |

## Soft Start

| Soft Start Charge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 15 | 30 | 50 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Soft Start DisCharge Current | $0.2 \mathrm{~V} \leq \mathrm{SS} \leq 3.0 \mathrm{~V}$ | 4.0 | 7.5 | 13.0 | $\mu \mathrm{~A}$ |
| Hiccup Mode Charge/Discharge Ratio | - | 3.0 | 4.0 | - | - |
| Peak Soft Start Charge Voltage | - | 3.3 | 4.0 | 4.2 | V |
| Soft Start DisCharge Threshold Voltage | - | 0.20 | 0.27 | 0.34 | V |


| PWM Comparators |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Minimum Pulse Width | Measured from CSx to GATE(H)x $\mathrm{V}\left(\mathrm{~V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS}_{\mathrm{REF}}\right)=1.0 \mathrm{~V}, \mathrm{~V}(\mathrm{COMP})=1.5 \mathrm{~V}$ <br> 60 mV step applied between $\mathrm{V}_{\mathrm{CSX}}$ and $V_{\text {CREF }}$ | - | 350 | 515 | ns |
| Channel Start Up Offset | $\mathrm{V}(\mathrm{CS} 1)=\mathrm{V}(\mathrm{CS} 2)=\mathrm{V}\left(\mathrm{V}_{\mathrm{FB}}\right)=\mathrm{V}\left(\mathrm{CS}_{\mathrm{REF}}\right)=0 \mathrm{~V}$; Measure V(COMP) when GATE(H)1, GATE(H)2, switch high | 0.3 | 0.4 | 0.5 | V |

2. The $\mathrm{V}_{\mathrm{FB}}$ Bias Current changes with the value of $\mathrm{R}_{\mathrm{OSC}}$ per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code 10000, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{l}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| GATE(H) and GATE(L) |  |  |  |  |  |
| High Voltage (AC) | Note 4 Measure $\mathrm{V}_{\text {CCLX }}$ - GATE(L)x or $\mathrm{V}_{\mathrm{CCHX}}-\operatorname{GATE}(\mathrm{H})_{\mathrm{X}}$ | - | 0 | 1.0 | V |
| Low Voltage (AC) | Note 4 Measure GATE(L) x or GATE(H) x | - | 0 | 0.5 | V |
| Rise Time GATE $(\mathrm{H})_{\mathrm{X}}$ | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\mathrm{CCHX}}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Rise Time GATE(L) X | 1.0 V < GATE < 8.0 V ; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time GATE(H)X | $8.0 \mathrm{~V}>\mathrm{GATE}>1.0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CCHX}}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| Fall Time GATE(L)X | $8.0 \mathrm{~V}>\mathrm{GATE}>1.0 \mathrm{~V}$; $\mathrm{V}_{\text {CCLX }}=10 \mathrm{~V}$ | - | 35 | 80 | ns |
| GATE(H) to GATE(L) Delay | GATE $(\mathrm{H})_{\mathrm{x}}<2.0 \mathrm{~V}, \mathrm{GATE}(\mathrm{L})_{\mathrm{x}}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE(L) to GATE(H) Delay | GATE $(\mathrm{L})_{\mathrm{x}}<2.0 \mathrm{~V}, \operatorname{GATE}(\mathrm{H})_{\mathrm{X}}>2.0 \mathrm{~V}$ | 30 | 65 | 110 | ns |
| GATE Pull-down | Force $100 \mu \mathrm{~A}$ into GATE Driver with no power applied to $\mathrm{V}_{\mathrm{CCHX}}$ and $\mathrm{V}_{\mathrm{CCLX}}=2.0 \mathrm{~V}$. | - | 1.2 | 1.6 | V |

Oscillator

| Switching Frequency | Measure any phase (ROSC $=32.4 \mathrm{k})$ | 300 | 400 | 500 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Switching Frequency | Note 4 Measure any phase (ROSC $=63.4 \mathrm{k}$ ) | 150 | 200 | 250 | kHz |
| Switching Frequency | Note 4 Measure any phase (ROSC $=16.2 \mathrm{k}$ ) | 600 | 800 | 1000 | kHz |
| Rosc Voltage | - | - | 1.00 | - | V |
| Phase Delay | Rising Edge Only | 165 | 180 | 195 | deg |

Adaptive Voltage Positioning

| $V_{\text {DRP }}$ Output Voltage to DAC Offset | $\begin{aligned} & \mathrm{CS} 1=\mathrm{CS} 2=\mathrm{CS}_{\mathrm{REF}}, \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP} \\ & \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | -15 | - | 15 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Maximum $\mathrm{V}_{\text {DRP }}$ Voltage | $\begin{aligned} & (\mathrm{CS1}=\mathrm{CS} 2)-\mathrm{C}_{\mathrm{REF}}=50 \mathrm{mV}, \\ & \mathrm{~V}_{\mathrm{FB}}=\mathrm{COMP}, \text { Measure } \mathrm{V}_{\mathrm{DRP}}-\mathrm{COMP} \end{aligned}$ | 240 | 310 | 380 | mV |
| Current Sense Amp to V ${ }_{\text {DRP }}$ Gain | - | 2.75 | 3.15 | 3.65 | V/V |

Current Sensing and Sharing

| CS ${ }_{\text {REF }}$ Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.5 | 4.0 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CS1-CS2 Input Bias Current | $\mathrm{V}(\mathrm{CSx})=\mathrm{V}\left(\mathrm{CS}_{\text {REF }}\right)=0 \mathrm{~V}$ | - | 0.2 | 2.0 | $\mu \mathrm{A}$ |
| Current Sense Amplifiers Gain | - | 2.80 | 3.15 | 3.53 | V/V |
| Current Sense Amp Mismatch | Note $40 \leq\left(\mathrm{CSx}-\mathrm{CS}_{\text {REF }}\right) \leq 50 \mathrm{mV}$ | -5.0 | - | 5.0 | mV |
| Current Sense Amplifiers Input Common Mode Range Limit | Note 4 | 0 | - | $\mathrm{V}_{\text {CCL }}-2$ | V |
| Current Sense Input to ILIM Gain | 0.25 V < $\mathrm{I}_{\text {LIM }}<1.20 \mathrm{~V}$ | 5.00 | 6.25 | 8.00 | V/V |
| Current Limit Filter Slew Rate | Note 4 | 4.0 | 10 | 26 | $\mathrm{mV} / \mathrm{\mu s}$ |
| ILIM Bias Current | $0<\mathrm{I}_{\text {LIM }}<1.0 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| Single Phase Pulse by Pulse Current Limit: V(CSx) - V(CS REF $)$ | - | 90 | 105 | 135 | mV |
| Current Share Amplifier Bandwidth | Note 4 | 1.0 | - | - | mHz |

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<70^{\circ} \mathrm{C} ; 0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.7 \mathrm{~V}<\mathrm{V}_{\mathrm{CCL}}<14 \mathrm{~V} ; 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CCH}}<20 \mathrm{~V}\right.$; $\mathrm{C}_{\mathrm{GATE}(\mathrm{H})}=3.3 \mathrm{nF}, \mathrm{C}_{\mathrm{GATE}(\mathrm{L})}=3.3 \mathrm{nF}, \mathrm{R}_{\mathrm{R}(\mathrm{OSC})}=32.4 \mathrm{k}, \mathrm{C}_{\mathrm{COMP}}=1.0 \mathrm{nF}, \mathrm{C}_{\mathrm{SS}}=0.1 \mu \mathrm{~F}, \mathrm{C}_{\mathrm{REF}}=0.1 \mu \mathrm{~F}$, DAC Code 10000, $\mathrm{C}_{\mathrm{VCC}}=1.0 \mu \mathrm{~F}$, $\mathrm{I}_{\mathrm{LIM}} \geq 1.0 \mathrm{~V}$; unless otherwise specified.)

| $\|c\| c\|c\| c\|c\| c\|c\|$ |
| :--- |
| Characteristic |
| Rest Conditions |
| Rerence Output |
| $V_{\text {REF }}$ Output Voltage |

General Electrical Specifications

| $\mathrm{V}_{\mathrm{CCL}}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 20.0 | 24.5 | mA |
| :--- | :--- | :--- | :--- | :---: | :---: |
| $\mathrm{~V}_{\mathrm{CCL} 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 4.0 | 5.5 | mA |
| $\mathrm{~V}_{\mathrm{CCL} 2}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 4.0 | 5.5 | mA |
| $\mathrm{~V}_{\mathrm{CCH} 1}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 2.8 | 4.0 | mA |
| $\mathrm{~V}_{\mathrm{CCH} 2}$ Operating Current | $\mathrm{V}_{\mathrm{FB}}=$ COMP (no switching) | - | 2.5 | 3.5 | mA |
| $\mathrm{~V}_{\mathrm{CCL}}$ Start Threshold | GATEs switching, Soft Start charging | 4.05 | 4.40 | 4.70 | V |
| $\mathrm{~V}_{\mathrm{CCL}}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 3.75 | 4.20 | 4.60 | V |
| $\mathrm{~V}_{\mathrm{CCL}}$ Hysteresis | GATEs not switching, Soft Start not charging | 100 | 200 | 300 | mV |
| $\mathrm{V}_{\mathrm{CCH} 1}$ Start Threshold | GATEs switching, Soft Start charging | 1.8 | 2.0 | 2.2 | V |
| $\mathrm{~V}_{\mathrm{CCH} 1}$ Stop Threshold | GATEs stop switching, Soft Start discharging | 1.55 | 1.75 | 1.90 | V |
| $\mathrm{~V}_{\mathrm{CCH} 1}$ Hysteresis | GATEs not switching, Soft Start not charging | 100 | 200 | 300 | mV |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 28 Lead SO Wide | PIN SYMBOL | FUNCTION |
| 1 | COMP | Output of the error amplifier and input for the PWM comparators. |
| 2 | $V_{\text {FB }}$ | Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{OUT}}$. The input current of the $\mathrm{V}_{\mathrm{FB}}$ pin and the resistor value determine output voltage offset for zero output current. Short $\mathrm{V}_{\mathrm{FB}}$ to $\mathrm{V}_{\mathrm{OUT}}$ for no AVP. |
| 3 | $\mathrm{V}_{\text {DRP }}$ | Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to $V_{F B}$ to set amount AVP or leave this pin open for no AVP. |
| 4-5 | CS1-CS2 | Current sense inputs. Connect current sense network for the corresponding phase to each input. |
| 6 | $C S_{\text {REF }}$ | Reference for current sense amplifiers and input for Power Good comparators. To balance input offset voltages between the inverting and non-inverting inputs of the current sense amplifiers, connect a resistor between CS $_{\text {REF }}$ and the output voltage. The value should be $2 / 5$ of the value of the resistors connected to the CSx pins. |
| 7 | PWRGD | Power-Good Output. Open collector output goes low when the $\mathrm{CS}_{\text {REF }}$ is out of regulation. |
| 8-12 | $\mathrm{V}_{\text {ID }}-\mathrm{V}_{\text {IDO }}$ | Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open. |
| 13 | ILIM | Sets threshold for current limit. Connect to reference through a resistive divider. |
| 14 | REF | Reference output. Decouple with $0.1 \mu \mathrm{~F}$ to LGND |
| 15 | $\mathrm{V}_{\mathrm{CCH} 2}$ | Power for GATE(H)2. |
| 16 | GATE(H)2 | High side driver \#2. |
| 17 | GND2 | Return for \#2 drivers. |
| 18 | GATE(L)2 | Low side driver \#2. |
| 19 | $\mathrm{V}_{\text {CCL2 }}$ | Power for GATE(L)2. |
| 20 | SS | Soft Start capacitor pin. The Soft Start capacitor controls both Soft Start time and hiccup mode frequency. The COMP pin is clamped below Soft Start during start up and hiccup mode. |
| 21 | LGND | Return for internal control circuits and IC substrate connection. |
| 22 | $\mathrm{V}_{\mathrm{CCH} 1}$ | Power for GATE(H)1. UVLO Sense for High Side Driver supply connects to this pin. |
| 23 | GATE(H)1 | High side driver \#1. |
| 24 | GND1 | Return for \#1 drivers. |
| 25 | GATE(L) 1 | Low side driver \#1. |
| 26 | $\mathrm{V}_{\text {CCL1 }}$ | Power for GATE(L)1. |
| 27 | $\mathrm{V}_{\text {CCL }}$ | Power for internal control circuits. UVLO Sense for Logic connects to this pin. |
| 28 | Rosc | A resistor from this pin to ground sets operating frequency and $\mathrm{V}_{\mathrm{FB}}$ bias current. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Oscillator Frequency


Figure 5. GATE(H) Rise-time vs. Load Capacitance measured from 1.0 V to 4.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 4. $\mathrm{V}_{\mathrm{FB}}$ Bias Current vs. Rosc Value


Figure 6. GATE(H) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 7. GATE(L) Rise-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .


Figure 8. GATE(L) Fall-time vs. Load Capacitance measured from 4.0 V to 1.0 V with $\mathrm{V}_{\mathrm{Cc}}$ at 5.0 V .

## APPLICATIONS INFORMATION

## FIXED FREQUENCY MULTI-PHASE CONTROL

In a multi-phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5332 uses a two-phase, fixed frequency, Enhanced V ${ }^{2}$ architecture. Each phase is delayed $180^{\circ}$ from the previous phase. Normally GATE(H) transitions high at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator and bring GATE(H) low. Once GATE $(\mathrm{H})$ goes low, it will remain low until the beginning of the next oscillator cycle. While GATE(H) is high, the Enhanced $\mathrm{V}^{2}$ loop will respond to line and load transients. Once GATE $(\mathrm{H})$ is low, the loop will not respond again until the beginning of the next cycle. Therefore, constant frequency Enhanced $\mathrm{V}^{2}$ will typically respond within the off-time of the converter.

The Enhanced $\mathrm{V}^{2}$ architecture measures and adjusts current in each phase. An additional input ( $\mathrm{C}_{\mathrm{X}}$ ) for inductor current information has been added to the $\mathrm{V}^{2}$ loop for each phase as shown in Figure 9.


Figure 9. Enhanced V ${ }^{2}$ Current Sense Scheme
The inductor current is measured across $\mathrm{R}_{\mathrm{S}}$, amplified by CSA and summed with the OFFSET and Output Voltage at the non-inverting input of the PWM comparator. The inductor current provides the PWM ramp and as inductor current increases the voltage on the positive pin of the PWM
comparator rises and terminates the PWM cycle. If the inductor starts the cycle with a higher current, the PWM cycle will terminate earlier providing negative feedback. The CS5332 provides a $\mathrm{C}_{\mathrm{X}}$ input for each phase, but the $\mathrm{CS}_{\mathrm{REF}}, \mathrm{V}_{\mathrm{FB}}$ and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same $\mathrm{V}_{\mathrm{FB}}$ and COMP pins, so that a phase with a larger current signal will turn off earlier than phases with a smaller current signal.
Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. If the COMP pin is held steady and the inductor current changes, there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$
\Delta \mathrm{V}=\mathrm{RS} \times \mathrm{CSA} \text { Gain } \times \Delta \mathrm{I}
$$

The single-phase power stage output impedance is;
Single Stage Impedance $=\Delta \mathrm{V} / \Delta \mathrm{I}=\mathrm{RS} \times$ CSA Gain.
The multi-phase power stage output impedance is the single-phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few $\mu$ s of a transient before the feedback loop has repositioned the COMP pin.
The peak output current of each phase can also be calculated from;

$$
\text { Ipkout }(\text { per phase })=\frac{V_{C O M P}-V_{F B}-V_{O F F S E T}}{R_{S} \times C S A}
$$

Figure 10 shows the step response of a single phase with the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides the PWM ramp through the Current Sense Amplifier. The PWM cycle ends when the sum of the current signal, voltage signal and OFFSET exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next PWM cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the $\mathrm{V}_{\mathrm{FB}}$ pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the current signal level is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.


Figure 10. Open Loop Operation

## Inductive Current Sensing

For lossless sensing current can be sensed across the inductor as shown in Figure 11. In the diagram, L is the output inductance and $\mathrm{R}_{\mathrm{L}}$ is the inherent inductor resistance. To compensate the current sense signal the values of R1 and C 1 are chosen so that $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} 1 \times \mathrm{C} 1$. If this criteria is met the current sense signal will be the same shape as the inductor current, the voltage signal at Cx will represent the instantaneous value of inductor current and the circuit can be analyzed as if a sense resistor of value $R_{L}$ was used as a sense resistor $\left(\mathrm{R}_{\mathrm{S}}\right)$.


Figure 11. Lossless Inductive Current Sensing with Enhanced $\mathbf{V}^{2}$
When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of $0.39 \%$ per ${ }^{\circ} \mathrm{C}$. The increase in winding resistance at higher temperatures should be
considered when setting the $\mathrm{I}_{\text {LIM }}$ threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 9.

## Current Sharing Accuracy

PCB traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at the same point for each phase and the connection to the $\mathrm{CS}_{\text {REF }}$ should be made so that no phase is favored. (In some cases, especially with inductive sensing, resistance of the pcb can be useful for increasing the current sense resistance.) The total current sense resistance used for calculations must include any pcb trace between the CS inputs and the $\mathrm{CS}_{\text {REF }}$ input that carries inductor current.

Current Sense Amplifier Input Mismatch and the value of the current sense element will determine the accuracy of current sharing between phases. The worst case Current Sense Amplifier Input Mismatch is 5.0 mV and will typically be within 3.0 mV . The difference in peak currents between phases will be the CSA Input Mismatch divided by the current sense resistance. If all current sense elements are of equal resistance, a 3.0 mV mismatch with a $2.0 \mathrm{~m} \Omega$ sense resistance will produce a 1.5 A difference in current between phases.

## Operation at > 50\% Duty Cycle

For operation at duty cycles above $50 \%$ Enhanced V ${ }^{2}$ will exhibit subharmonic oscillation unless a compensation ramp is added to each phase. A circuit like the one on the left side of Figure 12 can be added to each current sense network to implement slope compensation. The value of R1 can be varied to adjust the ramp size.


Figure 12. External Slope Compensation Circuit

## Ramp Size and Current Sensing

Because the current ramp is used for both the PWM ramp and to sense current, the inductor and sense resistor values will be constrained. A small ramp will provide a quick transient response by minimizing the difference over which the COMP pin must travel between light and heavy loads, but a steady state ramp of $25 \mathrm{mV}_{\mathrm{P}-\mathrm{P}}$ or greater is typically required to prevent pulse skipping and minimize pulse width jitter. For resistive current sensing, the combination of the inductor and sense resistor values must be chosen to provide a large enough steady state ramp. For large inductor values the sense resistor value must also be increased.

For inductive current sensing the RC network must meet the requirement of $L / R_{L}=R \times C$ to accurately sense the $A C$ and DC components of the current the signal. Again the values for L and $\mathrm{R}_{\mathrm{L}}$ will be constrained in order to provide a large enough steady state ramp with a compensated current sense signal. A smaller $L$, or a larger $R_{L}$ than optimum might be required. But unlike resistive sensing, with inductive sensing small adjustments can be made easily with the values of R and C to increase the ramp size if needed.

If RC is chosen to be smaller (faster) than $\mathrm{L} / \mathrm{R}_{\mathrm{L}}$, the AC portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $\mathrm{R} \times \mathrm{C}$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $\mathrm{R} \times \mathrm{C}$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During transients, the COMP pin will be required to overshoot along with the current signal in order to maintain the output voltage. The $\mathrm{V}_{\mathrm{DRP}}$ pin will also overshoot during transients and possibly slow the response. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of $\mathrm{L}=500 \mathrm{nH}$, $\mathrm{R}_{\mathrm{L}}=1.6 \mathrm{~m} \Omega, \mathrm{R} 1=20 \mathrm{k}$ and $\mathrm{C} 1=.01 \mu \mathrm{~F}$. For ideal current signal compensation the value of R1 should be $31 \mathrm{k} \Omega$. Due to the faster than ideal RC time constant there is an overshoot of $50 \%$ and the overshoot decays with a $200 \mu \mathrm{~s}$ time constant. With this compensation the $\mathrm{I}_{\text {LIM }}$ pin threshold must be set more than $50 \%$ above the full load current to avoid triggering hiccup mode during a large output load step.


Figure 13. Inductive Sensing waveform during a Load Step with Fast RC Time Constant ( $50 \mu \mathrm{~s} / \mathrm{div}$ )

## Current Limit

Two levels of overcurrent protection are provided. Any time the voltage on a Current Sense pin exceeds CS REF by more than the Single Phase Pulse by Pulse Current Limit, the PWM comparator for that phase is turned off. This provides fast peak current protection for individual phases. The outputs of all the currents are also summed and filtered to compare an averaged current signal to the voltage on the $\mathrm{I}_{\text {LIM }}$ pin. If this voltage is exceeded, the fault latch trips and the Soft Start capacitor is discharged by a $7.5 \mu \mathrm{~A}$ source until the COMP pin reaches 0.2 V . Then Soft-Start begins. The converter will continue to operate in this mode until the fault condition is corrected.

## Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the Enhanced $V^{2}$ control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns , causing the top MOSFET's to shut off, and the synchronous MOSFET's to turn on. This results in a "crowbar" action to clamp the output voltage and prevent damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

## Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in
order to reduce voltage excursions during transients. Adaptive voltage positioning can reduce peak-peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher than nominal at light loads to reduce output voltage sag when the load current is stepped up and set lower than nominal during heavy loads to reduce overshoot when the load current is stepped up. For low current applications a droop resistor can provide fast accurate adaptive positioning. However at high currents, the loss in a droop resistor becomes excessive. For example, in a 50 A converter a $1.0 \mathrm{~m} \Omega$ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond quickly to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped down and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.


Figure 14. Adaptive Positioning
The CS5332 can be configured to adjust the output voltage based on the output current of the converter. (Refer to Figure 1.)

To set the no-load positioning, a resistor is placed between the output voltage and $\mathrm{V}_{\mathrm{FB}}$ pin. The $\mathrm{V}_{\mathrm{FB}}$ bias current will develop a voltage across the resistor to decrease the output voltage. The $\mathrm{V}_{\mathrm{FB}}$ bias current is dependent on the value of $\mathrm{R}_{\mathrm{OSC}}$. See Figure 4 on the datasheet.

During no load conditions the $\mathrm{V}_{\mathrm{DRP}}$ pin is at the same voltage as the $\mathrm{V}_{\mathrm{FB}}$ pin, so none of the $\mathrm{V}_{\mathrm{FB}}$ bias current flows through the $\mathrm{V}_{\text {DRP }}$ resistor. When output current increases the $\mathrm{V}_{\mathrm{DRP}}$ pin increases proportionally and the $\mathrm{V}_{\mathrm{DRP}}$ pin current offsets the $\mathrm{V}_{\mathrm{FB}}$ bias current and causes the output voltage to decrease.

The $\mathrm{V}_{\mathrm{FB}}$ and $\mathrm{V}_{\mathrm{DRP}}$ pins take care of the slower and DC voltage positioning. The first few $\mu$ s are controlled primarily by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition
to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

Note: Large levels of adaptive positioning can cause pulse width jitter.

## Error Amp Compensation

The transconductance error amplifier requires a capacitor between the COMP pin and GND. Use of values less than 1.0 nF may result in error amp oscillation of several MHz .

The capacitor between the COMP pin and the inverting error amplifier input and the parallel resistance of the $\mathrm{V}_{\mathrm{FB}}$ resistor and the $\mathrm{V}_{\mathrm{DRP}}$ resistor are used to roll off the error amp gain. The gain is rolled off at a high enough frequency to give a quick transient response, but low enough to cross zero dB well below the switching frequency to minimize ripple and noise on the COMP pin.

## UVLO

The CS5332 has undervoltage lockout functions connected to two pins. One, intended for the logic and low-side drivers, with a 4.4 V turn-on threshold is connected to the $\mathrm{V}_{\text {CCL }}$ pin. A second, for the high side drivers, has a 2.0 V threshold and is connected to the $\mathrm{V}_{\mathrm{CCH} 1}$ pin.

The UVLO threshold for the high side drivers was chosen at a low value to allow for flexibility in the part and an input voltage as low as 3.3 V . In many applications this will be disabled or will only check that the applicable supply is on - not that it is at a high enough voltage to run the converter.

For the $12 \mathrm{~V}_{\text {IN }}$ converter in Figure 1. the UVLO pin for the high side driver is pulled up by the 5.0 V supply (through two diode drops) and the function is not used. The diode between the Soft Start pin and the 12 V supply holds the Soft Start pin near GND and prevents start-up while the 12 V supply is off. In an application where a higher UVLO threshold is necessary a circuit like the one in Figure 15 will lock out the converter until the 12 V supply exceeds 9.0 V .


Figure 15. External UVLO Circuit

## Remote Sense

In some applications that require remote output voltage sensing, there are conditions when the path of the feedback signal can be broken. In a voltage regulator module (VRM) the remote voltage feedback sense point is typically off the
module. If the module is powered apart from the intended application, the feedback will be left open. On a motherboard, the feedback path might be broken when the processor socket is left open. Without the feedback connection the output voltage is likely to exceed the intended voltage. To protect the circuit from overvoltage conditions, a resistor can be connected between the local output voltage and the remote sense line as shown in Figure 16.


Figure 16. Remote Sense Connection

## Soft Start Enable, and Hiccup Mode

A capacitor between the Soft Start pin and GND controls Soft Start and hiccup mode slopes. A $0.1 \mu \mathrm{~F}$ capacitor with $30 \mu \mathrm{~A}$ charge current will allow the output to ramp up at 0.3 $\mathrm{V} / \mathrm{ms}$ or 1.5 V in 5.0 ms at start-up.

When a fault is detected due to overcurrent or UVLO the converter will enter a low duty cycle hiccup mode. During hiccup mode the converter will not switch from the time a fault is detected until the Soft Start capacitor has discharged below the Soft Start Discharge Threshold and then charged back up above the Channel Start Up Offset.

The Soft Start pin will disable the converter when pulled below 0.3 V .

## Layout Guidelines

With the fast rise, high output currents of microprocessor applications, parasitic inductance and resistance should be
considered when laying out the power, filter and feedback signal sections of the board. Typically, a multi-layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to reroute the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

Voltage feedback should be taken from a point of the output or the output filter that doesn't favor any one phase. If the feedback connection is closer to one inductor than the others the ripple associated with that phase may appear larger than the ripple associated with the other phases and poor current sharing can result.

The current sense signal is typically tens of milli-volts. Noise pick-up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as switch nodes and gate drive signals. The paths should be matched as well as possible. It is especially important that all current sense signals be picked off at similar points for accurate current sharing. If the current signal is taken from a place other than directly at the inductor any additional resistance between the pick-off point and the inductor appears as part of the inherent inductor resistance and should be considered in design calculations. Capacitors for the current feedback networks should be placed as close to the current sense pins as practical.

## DESIGN PROCEDURE

## Current Sensing, Power Stage and Output Filter Components

1. Choose the output filter components to meet peak transient requirements. The formula below can be used to provide an approximate starting point for capacitor choice, but will be inadequate to calculate actual values.

$$
\Delta \mathrm{V}_{\mathrm{PEAK}}=(\Delta \mathrm{I} / \Delta \mathrm{T}) \times \mathrm{ESL}+\Delta \mathrm{I} \times \mathrm{ESR}
$$

Ideally the output filter should be simulated with models including ESR, ESL, circuit board parasitics and delays due to switching frequency and converter response. Typically both bulk capacitance (electrolytic, Oscon, etc,) and low impedance capacitance (ceramic chip) will be required. The bulk capacitance provides "hold up" during the converter response. The low impedance capacitance reduces steady state ripple and bypasses the bulk capacitance during slewing of output current.
2. For inductive current sensing (only) choose the current sense network RC to provide a 25 mV minimum ramp during steady state operation.

$$
R=\left(V_{\text {IN }}-V_{\text {OUT }}\right) \times \frac{V_{\text {OUT }} / V_{\text {IN }}}{F \times C \times 25 \mathrm{mV}}
$$

Then choose the inductor value and inherent resistance to satisfy $\mathrm{L} / \mathrm{R}_{\mathrm{L}}=\mathrm{R} \times \mathrm{C}$.
For ideal current sense compensation the ratio of $L$ and $R_{L}$ is fixed, so the values of $L$ and $R_{L}$ will be a compromise typically with the maximum value $\mathrm{R}_{\mathrm{L}}$ limited by conduction losses or inductor temperature rise and the minimum value of L limited by ripple current.
3. For resistive current sensing choose L and $\mathrm{R}_{\mathrm{S}}$ to provide a steady state ramp greater than 25 mV .

$$
\mathrm{L} / \mathrm{RS}_{\mathrm{S}}=\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times \mathrm{TON} / 25 \mathrm{mV}
$$

Again the ratio of $L$ and $R_{L}$ is fixed and the values of L and $\mathrm{R}_{\mathrm{S}}$ will be a compromise.
4. Calculate the high frequency output impedance (ConverterZ) of the converter during transients. This is the impedance of the Output filter ESR in parallel with the power stage output impedance (PwrstgZ) and will indicate how far from the original level ( $\Delta \mathrm{VR}$ ) the output voltage will typically recover to within one switching cycle. For a good transient response $\Delta \mathrm{VR}$ should be less than the peak output voltage overshoot or undershoot.

$$
\begin{array}{r}
\Delta \mathrm{VR}=\text { ConverterZ } \times \mathrm{ESR} \\
\text { ConverterZ }=\frac{\text { PwrstgZ } \times \mathrm{ESR}}{\text { PwrstgZ }+\mathrm{ESR}}
\end{array}
$$

where:

$$
\text { PwrstgZ }=R_{S} \times \text { CSA Gain/2.0 }
$$

Multiply the converterZ by the output current step size to calculate where the output voltage should recover to within the first switching cycle after a transient. If the ConverterZ is higher than the value required to recover to where the adaptive positioning is set, the remainder of the recovery will be controlled by the error amp compensation and will typically recover in $10-20 \mu \mathrm{~s}$.

$$
\Delta \mathrm{VR}=\Delta \mathrm{I} \text { OUT } \times \text { ConverterZ }
$$

Make sure that $\Delta \mathrm{VR}$ is less than the expected peak transient for a good transient response.
5. Adjust L and $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ as required to meet the best combination of transient response, steady state output voltage ripple and pulse width jitter.

## Current Limit

When the sum of the Current Sense amplifiers ( $\mathrm{V}_{\text {ITOTAL }}$ ) exceeds the voltage on the $\mathrm{I}_{\text {LIM }}$ pin the part will enter hiccup mode. For inductive sensing the $\mathrm{I}_{\text {LIM }}$ pin voltage should be set based on the inductor resistance (or current sense resistor) at max temperature and max current. To set the level of the $\mathrm{I}_{\text {LIM }}$ pin:
6. $\mathrm{V}_{\mathrm{I}(\mathrm{LIM})}=\mathrm{R} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS}$ to ILIM Gain
where:
R is $\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$;
$\mathrm{I}_{\mathrm{OUT}(\mathrm{LIM})}$ is the current limit threshold.
For the overcurrent to work properly the inductor time constant (L/R) should be $\leq$ the Current sense RC. If the RC is too fast, during step loads the current waveform will appear larger than it is (typically for a few hundred $\mu \mathrm{s}$ ) and may trip the current limit at a level lower than the DC limit.

## Adaptive Positioning

7. To set the amount of voltage positioning below the DAC setting at no load, connect a resistor $\left(\mathrm{R}_{\mathrm{V}}(\mathrm{FB})\right)$ between the output voltage and the $\mathrm{V}_{\mathrm{FB}}$ pin. Choose $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ as;

$$
R V(F B)=N L \text { Position } / V_{F B} \text { Bias Current }
$$

See Figure 4 for $V_{\text {FB }}$ Bias Current.
8. To set the difference in output voltage between no load and full load, connect a resistor $\left(\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}\right)$ between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pins. $\mathrm{R}_{\mathrm{V} \text { (DRP) }}$ can be calculated in two steps. First calculate the difference between the $\mathrm{V}_{\mathrm{DRP}}$ and $\mathrm{V}_{\mathrm{FB}}$ pin at full load. (The $\mathrm{V}_{\mathrm{FB}}$ voltage should be the same as the DAC voltage during closed loop operation.) Then choose the $\mathrm{R}_{\mathrm{V}(\mathrm{DRP})}$ to source enough current across $\mathrm{R}_{\mathrm{V}}(\mathrm{FB})$ for the desired change in output voltage.

$$
\Delta \mathrm{V}_{\mathrm{V}(\mathrm{DRP})}=\mathrm{IOUTFL} \times \mathrm{R} \times \mathrm{CS} \text { to } \mathrm{V}_{\mathrm{DRP}} \text { Gain }
$$

where:
$\mathrm{R}=\mathrm{R}_{\mathrm{L}}$ or $\mathrm{R}_{\mathrm{S}}$ for one phase;
IOUTFL is the full load output current.

$$
\mathrm{RV}(\mathrm{DRP})=\Delta \mathrm{V}_{\mathrm{DRP}} \times \operatorname{RV}(\mathrm{FB}) / \Delta \mathrm{V}_{\mathrm{OUT}}
$$

## Calculate Input Filter Capacitor Current Ripple

The procedure below assumes that phases do not overlap and output inductor ripple current $(\mathrm{P}-\mathrm{P})$ is less than the average output current of one phase.
9. Calculate Input Current
$\mathrm{IIN}_{\mathrm{N}}=\frac{\mathrm{V}_{\text {OUT }} \times \mathrm{IOUT}}{\left(\text { Efficiency } \times \mathrm{V}_{\text {IN }}\right)}$
10. Calculate Duty Cycle (per phase).

## Duty Cycle $=\frac{\mathrm{V}_{\text {OUT }}}{\left(\text { Efficiency } \times \mathrm{V}_{\text {IN }}\right)}$

11. Calculate Apparent Duty Cycle.

Apparent Duty Cycle $=$ Duty Cycle $\times \#$ of Phases
12. Calculate Input Filter Capacitor Ripple Current. Use the chart in Figure 17 to calculate the normalized ripple current ( $\mathrm{K}_{\mathrm{RMS}}$ ) based on the reciprocal of Apparent Duty Cycle. Then multiply the input current by $\mathrm{K}_{\mathrm{RMS}}$ to obtain the Input Filter Capacitor Ripple Current.


Figure 17. Normalized Input Filter Capacitor Ripple Current

## DESIGN EXAMPLE

Choose the component values for a $240 \mathrm{kHz}, 12 \mathrm{~V}$ to 1.525 V, 41 A converter with lossless current sensing, adaptive positioning and a 50 A current limit. The adaptive positioning is chosen 50 mV below the DAC setting at no load and 50 mV below the no-load position with 41 A out. The peak output voltage transient is 70 mV max during a 41 A step current.

## Current Sensing, Power Stage and Output Filter Components

1.Assume $1.5 \mathrm{~m} \Omega$ of output filter ESR.

$$
\begin{aligned}
& \text { 2.R } \begin{aligned}
& =\left(\mathrm{V}_{\mathrm{IN}}-\mathrm{V}_{\mathrm{OUT}}\right) \times\left(\mathrm{V}_{\mathrm{OUT}} / \mathrm{V} \mathrm{IN}\right) /(\mathrm{F} \times \mathrm{C} \times 25 \mathrm{mV}) \\
& =(12-1.55) \times(1.55 / 12) /(240 \mathrm{k} \times .01 \mu \mathrm{~F} \times 25 \mathrm{mV}) \\
& =22.5 \mathrm{k}
\end{aligned} \\
& \mathrm{~L} / \mathrm{R}_{\mathrm{L}}=.01 \mu \mathrm{~F} \times 22.5 \mathrm{k} \Omega=225 \mu \mathrm{~s} \\
& \begin{aligned}
\text { Choose } R \mathrm{~L} & =2.0 \mathrm{~m} \Omega
\end{aligned} \\
& \begin{aligned}
& \mathrm{L}=2.0 \mathrm{~m} \Omega \times 225 \mu \mathrm{~s}=450 \mathrm{nH} \\
& \text { 3. } \mathrm{n} / \mathrm{a}
\end{aligned} \\
& \begin{aligned}
\text { 4. } \text { PwrstgZ } & =R_{\mathrm{L}} \times \mathrm{CSA} \text { Gain } / 2.0 \\
& =2.0 \mathrm{~m} \Omega \times 3.15 / 2=3.1 \mathrm{~m} \Omega
\end{aligned}
\end{aligned}
$$

$$
\text { ConverterZ }=\frac{\text { PwrstgZ } \times \text { ESR }}{\text { PwrstgZ }+ \text { ESR }}
$$

$$
=\frac{3.1 \mathrm{~m} \Omega \times 1.5 \mathrm{~m} \Omega}{3.1 \mathrm{~m} \Omega+1.5 \mathrm{~m} \Omega} \cong 1.0 \mathrm{~m} \Omega
$$

$$
\Delta \mathrm{VR}=1.0 \mathrm{~m} \Omega \times 41 \mathrm{~A}=41 \mathrm{mV}
$$

5. n/a

## Current Limit

$$
\text { 6. } \begin{aligned}
\mathrm{V}_{\mathrm{I}(\mathrm{LIM})} & =\mathrm{R}_{\mathrm{L}} \times \operatorname{IOUT}(\mathrm{LIM}) \times \mathrm{CS} \text { to ILIM Gain } \\
& =2.0 \mathrm{~m} \Omega \times 50 \mathrm{~A} \times 6.25=625 \mathrm{mV}
\end{aligned}
$$

## Adaptive Positioning

$$
\text { 7. } \begin{aligned}
& \mathrm{RV}(\mathrm{FB})=\mathrm{NL} \text { Position } / \mathrm{V} \text { FB Bias Current } \\
&=50 \mathrm{mV} / 18 \mu \mathrm{~A}=2.78 \mathrm{k} \Omega \\
& \text { 8. } \begin{aligned}
\Delta \mathrm{V} R \mathrm{DP} & =\mathrm{R}_{\mathrm{L}} \times \mathrm{IOUT} \times \mathrm{Current} \text { Sense to } \mathrm{V} \text { DRP Gain } \\
& =2.0 \mathrm{~m} \Omega \times 41 \mathrm{~A} \times 3.1=254 \mathrm{mV} \\
\mathrm{RV}(\mathrm{DRP}) & =\Delta \mathrm{V} \mathrm{DRP} \times \mathrm{RV}(\mathrm{FB}) / \Delta \mathrm{V}_{\mathrm{OUT}} \\
& =254 \mathrm{mV} \times 2.78 \mathrm{k} \Omega / 50 \mathrm{mV}=25.4 \mathrm{k} \Omega
\end{aligned}
\end{aligned}
$$

9. $\mathrm{I}_{\mathrm{I}} \mathrm{N}=\frac{1.52 \mathrm{~V} \times 41 \mathrm{~A}}{\left(0.85 \times 12 \mathrm{~V}_{\mathrm{IN}}\right)}=6.1 \mathrm{~A}$
10. Duty Cycle $=\frac{1.52 \mathrm{~V}}{(0.85 \times 12 \mathrm{~V} \text { IN })}=0.15$
11. Apparent Duty Cycle $=0.15 \times 2.0=0.3$
12. RMS ripple is $6.1 \mathrm{~A} \times 1.5=9.2 \mathrm{~A}$


Figure 18. Additional Application Diagram, 5.0 V only to 2.5 V


Figure 19. Additional Application Diagram, 5.0 V to 1.6 V with 12 V Bias


Figure 20. Additional Application Diagram, 5.0 V only to 1.6 V
PACKAGE THERMAL DATA

| Parameter |  | SO-28L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 15 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 75 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC33501, MC33503

### 1.0 V, Rail-to-Rail, Single Operational Amplifiers

The MC33501/503 operational amplifier provides rail-to-rail operation on both the input and output. The output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the entire supply voltage range available. It is designed to work at very low supply voltages ( 1.0 V and ground), yet can operate with a supply of up to 7.0 V and ground. Output current boosting techniques provide high output current capability while keeping the drain current of the amplifier to a minimum.

- Low Voltage, Single Supply Operation (1.0 V and Ground to 7.0 V and Ground)
- High Input Impedance: Typically 40 fA Input Bias Current
- Typical Unity Gain Bandwidth @ 5.0 V = 4.0 MHz, @ $1.0 \mathrm{~V}=3.0 \mathrm{MHz}$
- High Output Current ( $\mathrm{I}_{\mathrm{SC}}=40 \mathrm{~mA} @ 5.0 \mathrm{~V}, 13 \mathrm{~mA} @ 1.0 \mathrm{~V}$ )
- Output Voltage Swings within 50 mV of Both Rails @ 1.0 V
- Input Voltage Range Includes Both Supply Rails
- High Voltage Gain: 100 dB Typical @ 1.0 V
- No Phase Reversal on the Output for Over-Driven Input Signals
- Input Offset Trimmed to 0.5 mV Typical
- Low Supply Current ( $\mathrm{I}_{\mathrm{D}}=1.2 \mathrm{~mA} /$ per Amplifier, Typical)
- $600 \Omega$ Drive Capability
- Extended Operating Temperature Range ( -40 to $105^{\circ} \mathrm{C}$ )


## Applications

- Single Cell NiCd/Ni MH Powered Systems
- Interface to DSP
- Portable Communication Devices
- Low Voltage Active Filters
- Telephone Circuits
- Instrumentation Amplifiers
- Audio Applications
- Power Supply Monitor and Control
- Transistor Count: 98


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC33501SNT1 | SOT23-5 | 3000 Tape \& Reel |
| MC33503SNT1 | SOT23-5 | 3000 Tape \& Reel |

## MC33501, MC33503



This device contains 98 active transistors per amplifier.
Figure 1. Simplified Block Diagram

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (V $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | 7.0 | V |
| ESD Protection Voltage at any Pin <br> Human Body Model | $\mathrm{V}_{\mathrm{ESD}}$ | 2000 | V |
| Voltage at Any Device Pin | $\mathrm{V}_{\mathrm{DP}}$ | $\mathrm{V}_{\mathrm{S}} \pm 0.3$ | V |
| Input Differential Voltage Range | $\mathrm{V}_{\text {IDR }}$ | $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ | V |
| Common Mode Input Voltage Range | $\mathrm{V}_{\mathrm{CM}}$ | $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ | V |
| Output Short Circuit Duration | $\mathrm{ts}_{\mathrm{S}}$ | Note 1 | s |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Note 1 | mW |

1. Power dissipation must be considered to ensure maximum junction temperature $\left(T_{J}\right)$ is not exceeded.
2. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}} / 2\right.$, $\mathrm{R}_{\mathrm{L}}$ to $\mathrm{V}_{\mathrm{CC}} / 2, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage }\left(\mathrm{V}_{\mathrm{CM}}=0 \text { to } \mathrm{V} \mathrm{CC}\right) \\ & \mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C} \\ & \hline \end{aligned}$ | $\mathrm{V}_{10}$ | $\begin{aligned} & -5.0 \\ & -7.0 \\ & -5.0 \\ & -7.0 \\ & -5.0 \\ & -7.0 \end{aligned}$ | $\begin{gathered} 0.5 \\ - \\ 0.5 \\ - \\ 0.5 \\ - \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 7.0 \\ & \\ & 5.0 \\ & 7.0 \\ & 5.0 \\ & 7.0 \end{aligned}$ | mV |
| Input Offset Voltage Temperature Coefficient ( $\mathrm{R}_{\mathrm{S}}=50 \Omega$ ) $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $105^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 8.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current ( $\mathrm{V}_{\mathrm{CC}}=1.0$ to 5.0 V ) | $1 I_{B B} \mid$ | - | 0.00004 | 1.0 | nA |
| Common Mode Input Voltage Range | $V_{\text {ICR }}$ | $\mathrm{V}_{\mathrm{EE}}$ | - | $\mathrm{V}_{\mathrm{CC}}$ | V |
| Large Signal Voltage Gain $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & R_{\mathrm{L}}=1.0 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k} \Omega \\ & \end{aligned}$ | Avol | $\begin{aligned} & 25 \\ & 5.0 \\ & 50 \\ & 25 \\ & \\ & 50 \\ & 25 \end{aligned}$ | $\begin{gathered} 100 \\ 50 \\ 500 \\ 100 \\ 500 \\ 200 \end{gathered}$ | - | kV/V |
|  | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{gathered} 0.9 \\ 0.85 \\ \\ 0.85 \\ 0.8 \\ \\ 2.9 \\ 2.8 \\ \\ 2.85 \\ 2.75 \\ \\ 4.9 \\ 4.75 \\ \\ 4.85 \\ 4.7 \end{gathered}$ | $\begin{gathered} 0.95 \\ 0.88 \\ - \\ - \\ 2.93 \\ 2.84 \\ - \\ - \\ \\ \hline \end{gathered}$ |  | V |

DC ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}} / 2$, $\mathrm{R}_{\mathrm{L}}$ to $\mathrm{V}_{\mathrm{CC}} / 2, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

\begin{tabular}{|c|c|c|c|c|c|}
\hline Characteristic \& Symbol \& Min \& Typ \& Max \& Unit <br>
\hline $$
\begin{aligned}
& \text { Output Voltage Swing, Low }\left(\mathrm{V}_{I D}= \pm 0.2 \mathrm{~V}\right) \\
& \mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\
& \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{L}}=600 \Omega \\
& \mathrm{~V}_{\mathrm{C}}=1.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C}\right) \\
& \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{L}}=600 \Omega \\
& \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\
& \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{L}}=600 \Omega \\
& \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C}\right) \\
& R_{\mathrm{L}}=10 \mathrm{k} \Omega \\
& R_{\mathrm{L}}=600 \Omega \\
& \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\
& \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{L}}=600 \Omega \\
& \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C}\right) \\
& R_{\mathrm{L}}=10 \mathrm{k} \Omega \\
& \mathrm{R}_{\mathrm{L}}=600 \Omega
\end{aligned}
$$ \& $\mathrm{V}_{\text {OL }}$ \& $$
\begin{gathered}
0.05 \\
0.1 \\
0.1 \\
0.15 \\
\\
0.05 \\
0.1 \\
\\
0.1 \\
0.15 \\
\\
0.05 \\
0.15 \\
\\
0.1 \\
0.2
\end{gathered}
$$ \& 0.02
0.05
-
-

0.02
0.08
-
-

0.02
0.1 \&  \& V <br>
\hline Common Mode Rejection ( $\mathrm{V}_{\text {in }}=0$ to 5.0 V ) \& CMR \& 60 \& 75 \& - \& dB <br>

\hline | Power Supply Rejection |
| :--- |
| $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=5.0 \mathrm{~V} /$ Ground to $3.0 \mathrm{~V} /$ Ground | \& PSR \& 60 \& 75 \& - \& dB <br>


\hline | Output Short Circuit Current ( $\mathrm{V}_{\text {in }}$ Diff $= \pm 1.0 \mathrm{~V}$ ) $V_{C C}=1.0 \mathrm{~V}$ |
| :--- |
| Source |
| Sink $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$ |
| Source |
| Sink $V_{C C}=5.0 \mathrm{~V}$ |
| Source |
| Sink | \& Isc \& \[

$$
\begin{aligned}
& 6.0 \\
& 10 \\
& \\
& 15 \\
& 40 \\
& 20 \\
& 40
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& 13 \\
& 13 \\
& \\
& 32 \\
& 64 \\
& 40 \\
& 70
\end{aligned}
$$

\] \& \[

$$
\begin{gathered}
26 \\
26 \\
60 \\
140 \\
140 \\
140
\end{gathered}
$$
\] \& mA <br>

\hline $$
\begin{aligned}
& \text { Power Supply Current (Per Amplifier, } \left.\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\
& \mathrm{V}_{C C}=1.0 \mathrm{~V} \\
& \mathrm{~V}_{C C}=3.0 \mathrm{~V} \\
& \mathrm{~V}_{C C}=5.0 \mathrm{~V} \\
& \mathrm{~V}_{C C}=1.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40 \text { to } 105^{\circ} \mathrm{C}\right) \\
& \mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40 \text { to } 105^{\circ} \mathrm{C}\right) \\
& \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40 \text { to } 105^{\circ} \mathrm{C}\right) \\
& \hline
\end{aligned}
$$ \& ID \& - \& 1.2

1.5

1.65 \& $$
\begin{gathered}
1.75 \\
2.0 \\
2.25 \\
2.0 \\
2.25 \\
2.5
\end{gathered}
$$ \& mA <br>

\hline
\end{tabular}

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}} / 2, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate $\left(\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=-2.0\right.$ to $2.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{A}_{\mathrm{V}}=1.0$ ) <br> Positive Slope <br> Negative Slope | SR |  | $\begin{aligned} & 3.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 6.0 \end{aligned}$ | V/ $/ \mathrm{s}$ |
| $\begin{gathered} \text { Gain Bandwidth Product (f } \mathrm{f}=100 \mathrm{kHz}) \\ \mathrm{V}_{\mathrm{CC}}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.5 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \end{gathered}$ | GBW | $\begin{aligned} & 2.0 \\ & 2.5 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 7.0 \\ & 8.0 \end{aligned}$ | MHz |
| Gain Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) | Am | - | 6.5 | - | dB |
| Phase Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) | $\phi_{\mathrm{m}}$ | - | 60 | - | Deg |
| Channel Separation ( $\mathrm{f}=1.0 \mathrm{~Hz}$ to $20 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=600 \Omega$ ) | CS | - | 120 | - | dB |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k} \Omega$, THD $\leq 1.0 \%$ ) | $\mathrm{BW}_{\mathrm{P}}$ | - | 200 | - | kHz |
| Total Harmonic Distortion ( $\mathrm{V}_{\mathrm{O}}=4.5 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{~A}_{\mathrm{V}}=1.0$ ) $\begin{aligned} & f=1.0 \mathrm{kHz} \\ & \mathrm{f}=10 \mathrm{kHz} \end{aligned}$ | THD |  | $\begin{gathered} 0.004 \\ 0.01 \end{gathered}$ |  | \% |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{R}_{\text {in }}$ | - | >1.0 | - | terra $\Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{C}_{\text {in }}$ | - | 2.0 | - | pF |
| Equivalent Input Noise Voltage ( $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}$, $\begin{aligned} & \left.\mathrm{R}_{\mathrm{S}}=100 \Omega\right) \\ & \mathrm{f}=1.0 \mathrm{kHz} \end{aligned}$ | $\mathrm{e}_{\mathrm{n}}$ | - | 30 | - | $\mathrm{nV} / \mathrm{VHz}$ |



Figure 2. Representative Block Diagram

## General Information

The MC33501/503 dual operational amplifier is unique in its ability to provide 1.0 V rail-to-rail performance on both the input and output by using a SMARTMOS ${ }^{T M}$ process. The amplifier output swings within 50 mV of both rails and is able to provide 50 mA of output drive current with a 5.0 V supply, and 10 mA with a 1.0 V supply. A 5.0 MHz bandwidth and a slew rate of $3.0 \mathrm{~V} / \mu \mathrm{s}$ is achieved with high speed depletion mode NMOS (DNMOS) and vertical PNP transistors. This device is characterized over a temperature range of $-40^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$.

## Circuit Information

## Input Stage

One volt rail-to-rail performance is achieved in the MC33501/503 at the input by using a single pair of depletion mode NMOS devices (DNMOS) to form a differential amplifier with a very low input current of 40 fA . The normal input common mode range of a DNMOS device, with an ion implanted negative threshold, includes ground and relies on the body effect to dynamically shift the threshold to a positive value as the gates are moved from ground towards the positive supply. Because the device is manufactured in a p-well process, the body effect coefficient is sufficiently large to ensure that the input stage will remain substantially saturated when the inputs are at the positive rail. This also applies at very low supply voltages. The 1.0 V rail-to-rail input stage consists of a DNMOS differential amplifier, a folded cascode, and a low voltage balanced mirror. The low voltage cascoded balanced mirror provides high 1st stage gain and base current cancellation without sacrificing signal integrity. Also, the input offset voltage is trimmed to less than 1.0 mV because of the limited available supply voltage. The body voltage of the input DNMOS differential pair is internally trimmed to minimize the input offset voltage. A common mode feedback path is also employed to enable the offset voltage to track over the input common mode voltage. The total operational amplifier quiescent current drop is $1.3 \mathrm{~mA} / \mathrm{amp}$.

## Output Stage

An additional feature of this device is an "on demand" base current cancellation amplifier. This feature provides base drive to the output power devices by making use of a buffer amplifier to perform a voltage-to-current conversion. This is done in direct proportion to the load conditions. This "on demand" feature allows these amplifiers to consume only a few micro-amps of current when the output stage is in its quiescent mode. Yet it provides high output current when required by the load. The rail-to-rail output stage current boost circuit provides 50 mA of output current with a 5.0 V supply (For a 1.0 V supply output stage will do 10 mA ) enabling the operational amplifier to drive a $600 \Omega$ load. A buffer is necessary to isolate the load current effects in the output stage from the input stage. Because of the low voltage conditions, a DNMOS follower is used to provide an essentially zero voltage level shift. This buffer isolates any load current changes on the output stage from loading the input stage. A high speed vertical PNP transistor provides excellent frequency performance while sourcing current. The operational amplifier is also internally compensated to provide a phase margin of 60 degrees. It has a unity gain of 5.0 MHz with a 5.0 V supply and 4.0 MHz with a 1.0 V supply.

## Low Voltage Operation

The MC33501/503 will operate at supply voltages from 0.9 to 7.0 V and ground. When using the MC33501/503 at supply voltages of less than 1.2 V , input offset voltage may increase slightly as the input signal swings within approximately 50 mV of the positive supply rail. This effect occurs only for supply voltages below 1.2 V , due to the input depletion mode MOSFETs starting to transition between the saturated to linear region, and should be considered when designing high side dc sensing applications operating at the positive supply rail. Since the device is rail-to-rail on both input and output, high dynamic range single battery cell applications are now possible.


Figure 3. Output Saturation versus Load Resistance


Figure 5. Input Current versus Temperature


Figure 6. Gain and Phase versus Frequency


Figure 7. Transient Response


Figure 4. Drive Output Source/Sink Saturation Voltage versus Load Current
t , TIME ( $1.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 8. Slew Rate


Figure 9. Maximum Power Dissipation versus Temperature


Figure 11. Output Voltage versus Frequency


Figure 13. Power Supply Rejection versus Frequency


Figure 10. Open Loop Voltage Gain versus Temperature


Figure 12. Common Mode Rejection versus Frequency


Figure 14. Output Short Circuit Current versus Output Voltage


Figure 15. Output Short Circuit Current versus Temperature


Figure 17. Input Offset Voltage Temperature Coefficient Distribution


Figure 19. Total Harmonic Distortion
Figure 19. Total Harmonic Distortion
versus Frequency with 1.0 V Supply


Figure 16. Supply Current per Amplifier versus Supply Voltage with No Load


Figure 18. Input Offset Voltage Distribution


Figure 20. Total Harmonic Distortion versus Frequency with 5.0 V Supply


Figure 21. Slew Rate versus Temperature


Figure 22. Gain Bandwidth Product versus Temperature


Figure 23. Voltage Gain and Phase versus Frequency


Figure 24. Gain and Phase Margin versus Temperature

$\mathrm{R}_{\mathrm{T}}$, DIFFERENTIAL SOURCE RESISTANCE ( $\Omega$ )
Figure 25. Gain and Phase Margin versus Differential Source Resistance


Figure 26. Feedback Loop Gain and Phase versus Capacitive Load


Figure 27. Channel Separation versus Frequency


Figure 29. Equivalent Input Noise Voltage versus Frequency


Figure 31. Useable Supply Voltage versus Temperature


Figure 28. Output Voltage Swing versus Supply Voltage


Figure 30. Gain and Phase Margin versus Supply Voltage


Figure 32. Open Loop Gain versus Supply Voltage

MC33501, MC33503


Figure 33. 1.0 V Oscillator


Figure 34. 1.0 V Voiceband Filter


Figure 35. Power Supply Application


Figure 36. 1.0 V Current Pump

## MC33502

### 1.0 V, Rail-to-Rail, Dual Operational Amplifier

The MC33502 operational amplifier provides rail-to-rail operation on both the input and output. The output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the entire supply voltage range available. It is designed to work at very low supply voltages ( 1.0 V and ground), yet can operate with a supply of up to 7.0 V and ground. Output current boosting techniques provide high output current capability while keeping the drain current of the amplifier to a minimum.

- Low Voltage, Single Supply Operation (1.0 V and Ground to 7.0 V and Ground)
- High Input Impedance: Typically 40 fA Input Current
- Typical Unity Gain Bandwidth @ 5.0 V = 5.0 MHz, @ $1.0 \mathrm{~V}=4.0 \mathrm{MHz}$
- High Output Current ( $\mathrm{I}_{\mathrm{SC}}=40 \mathrm{~mA} @ 5.0 \mathrm{~V}, 13 \mathrm{~mA} @ 1.0 \mathrm{~V}$ )
- Output Voltage Swings within 50 mV of Both Rails @ 1.0 V
- Input Voltage Range Includes Both Supply Rails
- High Voltage Gain: 100 dB Typical @ 1.0 V
- No Phase Reversal on the Output for Over-Driven Input Signals
- Input Offset Trimmed to 0.5 mV Typical
- Low Supply Current ( $\mathrm{I}_{\mathrm{D}}=1.2 \mathrm{~mA} /$ per Amplifier, Typical)
- $600 \Omega$ Drive Capability
- Extended Operating Temperature Range ( -40 to $105^{\circ} \mathrm{C}$ )


## Applications

- Single Cell NiCd/Ni MH Powered Systems
- Interface to DSP
- Portable Communication Devices
- Low Voltage Active Filters
- Telephone Circuits
- Instrumentation Amplifiers
- Audio Applications
- Power Supply Monitor and Control
- Compatible with VCX Logic


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com
MARKING
DIAGRAMS

PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33502P | PDIP-8 | 50 Units/Rail |
| MC33502D | SO-8 | 98 Units/Rail |
| MC33502DR2 | SO-8 | 2500 Tape \& Reel |



This device contains 98 active transistors per amplifier.

Figure 1. Simplified Block Diagram

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage (VCC to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | 7.0 | V |
| ESD Protection Voltage at any Pin Human Body Model | $V_{\text {ESD }}$ | 2000 | V |
| Voltage at Any Device Pin | $V_{\text {DP }}$ | $\mathrm{V}_{\mathrm{S}} \pm 0.3$ | V |
| Input Differential Voltage Range | $V_{\text {IDR }}$ | $\mathrm{V}_{\text {CC }}$ to $\mathrm{V}_{\text {EE }}$ | V |
| Common Mode Input Voltage Range | $\mathrm{V}_{\mathrm{CM}}$ | $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ | V |
| Output Short Circuit Duration | ts | Note 1 | s |
| Maximum Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Note 1 | mW |

1. Power dissipation must be considered to ensure maximum junction temperature $\left(T_{J}\right)$ is not exceeded.
2. ESD data available upon request.

## MC33502

DC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}} / 2\right.$, $\mathrm{R}_{\mathrm{L}}$ to $\mathrm{V}_{\mathrm{CC}} / 2, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage }\left(\mathrm{V}_{\mathrm{CM}}=0 \text { to } \mathrm{V} \mathrm{CC}\right) \\ & \mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{10}$ | $\begin{aligned} & -5.0 \\ & -7.0 \\ & -5.0 \\ & -7.0 \\ & -5.0 \\ & -7.0 \end{aligned}$ | 0.5 - 0.5 - 0.5 | $\begin{aligned} & 5.0 \\ & 7.0 \\ & \\ & 5.0 \\ & 7.0 \\ & 5.0 \\ & 7.0 \end{aligned}$ | mV |
| Input Offset Voltage Temperature Coefficient ( $\mathrm{R}_{\mathrm{S}}=50 \Omega$ ) $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $105^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 8.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current ( $\mathrm{V}_{\mathrm{CC}}=1.0$ to 5.0 V ) | $\left\|I_{\text {IB }}\right\|$ | - | 0.00004 | 10 | nA |
| Common Mode Input Voltage Range | $V_{\text {ICR }}$ | $\mathrm{V}_{\mathrm{EE}}$ | - | $\mathrm{V}_{\text {cc }}$ | V |
| Large Signal Voltage Gain $\begin{aligned} \mathrm{V}_{C C} & =1.0 \mathrm{~V}\left(\mathrm{~T}_{A}=25^{\circ} \mathrm{C}\right) \\ R_{\mathrm{L}} & =10 \mathrm{k} \Omega \\ R_{\mathrm{L}} & =1.0 \mathrm{k} \Omega \\ \mathrm{~V}_{C C} & =3.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ R_{\mathrm{L}} & =10 \mathrm{k} \Omega \\ R_{\mathrm{L}} & =1.0 \mathrm{k} \Omega \\ \mathrm{~V}_{\mathrm{CC}} & =5.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ R_{\mathrm{L}} & =10 \mathrm{k} \Omega \\ R_{\mathrm{L}} & =1.0 \mathrm{k} \Omega \end{aligned}$ | Avol | $\begin{aligned} & 25 \\ & 5.0 \\ & \\ & 50 \\ & 25 \\ & \\ & 50 \\ & 25 \end{aligned}$ | $\begin{gathered} 100 \\ 50 \\ 500 \\ 100 \\ 500 \\ 200 \end{gathered}$ | - | kV/V |
|  | $\mathrm{V}_{\mathrm{OH}}$ | 0.9 0.85 <br> 0.85 <br> 0.8 <br> 2.9 <br> 2.8 <br> 2.85 <br> 2.75 <br> 4.9 <br> 4.75 <br> 4.85 <br> 4.7 | 0.95 <br> 0.88 <br> - <br> - <br> 2.93 <br> 2.84 <br> - <br> 4.92 <br> 4.81 | - - - - - - - - - - - - - | V |

## MC33502

DC ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}} / 2, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{V}_{\mathrm{CC}} / 2, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | VOL | $\begin{gathered} 0.05 \\ 0.1 \\ 0.1 \\ 0.15 \\ \\ 0.05 \\ 0.1 \\ \\ 0.1 \\ 0.15 \\ \\ 0.05 \\ 0.15 \\ \\ 0.1 \\ 0.2 \end{gathered}$ | $\begin{gathered} 0.02 \\ 0.05 \\ - \\ - \\ 0.02 \\ 0.08 \\ - \\ - \\ \\ 0.02 \\ 0.1 \end{gathered}$ | - <br> - <br> - <br> - <br> - <br> - <br> - <br> - <br> - <br> - <br> - <br> - | V |
| Common Mode Rejection ( $\mathrm{V}_{\text {in }}=0$ to 5.0 V ) | CMR | 60 | 75 | - | dB |
| Power Supply Rejection <br> $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=5.0 \mathrm{~V} /$ Ground to $3.0 \mathrm{~V} /$ Ground | PSR | 60 | 75 | - | dB |
| Output Short Circuit Current ( $\mathrm{V}_{\text {in }}$ Diff $= \pm 1.0 \mathrm{~V}$ ) $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}$ <br> Source <br> Sink $V_{C C}=3.0 \mathrm{~V}$ <br> Source <br> Sink $V_{C C}=5.0 \mathrm{~V}$ <br> Source <br> Sink | Isc | $\begin{aligned} & 6.0 \\ & 10 \\ & 15 \\ & 40 \\ & 20 \\ & 40 \end{aligned}$ | $\begin{aligned} & 13 \\ & 13 \\ & \\ & 32 \\ & 64 \\ & \\ & 40 \\ & 70 \end{aligned}$ | $\begin{gathered} 26 \\ 26 \\ 60 \\ 140 \\ 140 \\ 140 \end{gathered}$ | mA |
| $\begin{aligned} & \text { Power Supply Current (Per Amplifier, } \left.\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{V}_{C C}=1.0 \mathrm{~V} \\ & \mathrm{~V}_{C C}=3.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=1.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40 \text { to } 105^{\circ} \mathrm{C}\right) \\ & \mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40 \text { to } 105^{\circ} \mathrm{C}\right) \\ & \mathrm{V}_{C \mathrm{C}}=5.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=-40 \text { to } 105^{\circ} \mathrm{C}\right) \\ & \hline \end{aligned}$ | ID | - | 1.2 1.5 1.65 | $\begin{gathered} 1.75 \\ 2.0 \\ 2.25 \\ 2.0 \\ 2.25 \\ 2.5 \end{gathered}$ | mA |

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}} / 2, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate $\left(\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=-2.0\right.$ to $2.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{A}_{\mathrm{V}}=1.0$ ) <br> Positive Slope <br> Negative Slope | SR | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 6.0 \end{aligned}$ | V/us |
| $\begin{aligned} & \text { Gain Bandwidth Product (f=100 kHz) } \\ & \mathrm{V}_{\mathrm{CC}}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \end{aligned}$ | GBW | $\begin{aligned} & 3.0 \\ & 3.5 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 4.0 \\ & 4.5 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 7.0 \\ & 8.0 \end{aligned}$ | MHz |
| Gain Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) | Am | - | 6.5 | - | dB |
| Phase Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) | $\phi_{m}$ | - | 60 | - | Deg |
| Channel Separation ( $\mathrm{f}=1.0 \mathrm{~Hz}$ to $20 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=600 \Omega$ ) | CS | - | 120 | - | dB |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k} \Omega$, THD $\leq 1.0 \%$ ) | $\mathrm{BW}_{\mathrm{P}}$ | - | 200 | - | kHz |
| Total Harmonic Distortion ( $\mathrm{V}_{\mathrm{O}}=4.5 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{~A}_{\mathrm{V}}=1.0$ ) $\begin{aligned} & f=1.0 \mathrm{kHz} \\ & \mathrm{f}=10 \mathrm{kHz} \end{aligned}$ | THD | - | $\begin{gathered} 0.004 \\ 0.01 \end{gathered}$ | - | \% |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{R}_{\text {in }}$ | - | >1.0 | - | terra $\Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{C}_{\text {in }}$ | - | 2.0 | - | pF |
| Equivalent Input Noise Voltage ( $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}$, $\begin{aligned} & \left.R_{\mathrm{S}}=100 \Omega\right) \\ & \mathrm{f}=1.0 \mathrm{kHz} \end{aligned}$ | $e_{n}$ | - | 30 | - | $\mathrm{nV} / \mathrm{VHz}$ |



Figure 2. Representative Block Diagram

## General Information

The MC33502 dual operational amplifier is unique in its ability to provide 1.0 V rail-to-rail performance on both the input and output by using a SMARTMOS ${ }^{T M}$ process. The amplifier output swings within 50 mV of both rails and is able to provide 50 mA of output drive current with a 5.0 V supply, and 10 mA with a 1.0 V supply. A 5.0 MHz bandwidth and a slew rate of $3.0 \mathrm{~V} / \mu$ s is achieved with high speed depletion mode NMOS (DNMOS) and vertical PNP transistors. This device is characterized over a temperature range of $-40^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$.

## Circuit Information

## Input Stage

One volt rail-to-rail performance is achieved in the MC33502 at the input by using a single pair of depletion mode NMOS devices (DNMOS) to form a differential amplifier with a very low input current of 40 fA . The normal input common mode range of a DNMOS device, with an ion implanted negative threshold, includes ground and relies on the body effect to dynamically shift the threshold to a positive value as the gates are moved from ground towards the positive supply. Because the device is manufactured in a p-well process, the body effect coefficient is sufficiently large to ensure that the input stage will remain substantially saturated when the inputs are at the positive rail. This also applies at very low supply voltages. The 1.0 V rail-to-rail input stage consists of a DNMOS differential amplifier, a folded cascode, and a low voltage balanced mirror. The low voltage cascoded balanced mirror provides high 1st stage gain and base current cancellation without sacrificing signal integrity. Also, the input offset voltage is trimmed to less than 1.0 mV because of the limited available supply voltage. The body voltage of the input DNMOS differential pair is internally trimmed to minimize the input offset voltage. A common mode feedback path is also employed to enable the offset voltage to track over the input common mode voltage. The total operational amplifier quiescent current drop is $1.3 \mathrm{~mA} / \mathrm{amp}$.

## Output Stage

An additional feature of this device is an "on demand" base current cancellation amplifier. This feature provides base drive to the output power devices by making use of a buffer amplifier to perform a voltage-to-current conversion. This is done in direct proportion to the load conditions. This "on demand" feature allows these amplifiers to consume only a few micro-amps of current when the output stage is in its quiescent mode. Yet it provides high output current when required by the load. The rail-to-rail output stage current boost circuit provides 50 mA of output current with a 5.0 V supply (For a 1.0 V supply output stage will do 10 mA ) enabling the operational amplifier to drive a $600 \Omega$ load. A buffer is necessary to isolate the load current effects in the output stage from the input stage. Because of the low voltage conditions, a DNMOS follower is used to provide an essentially zero voltage level shift. This buffer isolates any load current changes on the output stage from loading the input stage. A high speed vertical PNP transistor provides excellent frequency performance while sourcing current. The operational amplifier is also internally compensated to provide a phase margin of 60 degrees. It has a unity gain of 5.0 MHz with a 5.0 V supply and 4.0 MHz with a 1.0 V supply.

## Low Voltage Operation

The MC33502 will operate at supply voltages from 0.9 to 7.0 V and ground. When using the MC33502 at supply voltages of less than 1.2 V , input offset voltage may increase slightly as the input signal swings within approximately 50 mV of the positive supply rail. This effect occurs only for supply voltages below 1.2 V , due to the input depletion mode MOSFETs starting to transition between the saturated to linear region, and should be considered when designing high side dc sensing applications operating at the positive supply rail. Since the device is rail-to-rail on both input and output, high dynamic range single battery cell applications are now possible.


Figure 3. Output Saturation versus Load Resistance


Figure 5. Input Current versus Temperature


Figure 4. Drive Output Source/Sink Saturation Voltage versus Load Current


Figure 6. Gain and Phase versus Frequency
t , TIME ( $1.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 8. Slew Rate


Figure 9. Maximum Power Dissipation versus Temperature


Figure 11. Output Voltage versus Frequency


Figure 13. Power Supply Rejection versus Frequency


Figure 10. Open Loop Voltage Gain versus Temperature


Figure 12. Common Mode Rejection versus Frequency


Figure 14. Output Short Circuit Current versus Output Voltage


Figure 15. Output Short Circuit Current versus Temperature


Figure 17. Input Offset Voltage Temperature Coefficient Distribution


Figure 19. Total Harmonic Distortion
Figure 19. Total Harmonic Distortion
versus Frequency with 1.0 V Supply


Figure 16. Supply Current per Amplifier versus Supply Voltage with No Load


Figure 18. Input Offset Voltage Distribution


Figure 20. Total Harmonic Distortion versus Frequency with 5.0 V Supply


Figure 21. Slew Rate versus Temperature


Figure 22. Gain Bandwidth Product versus Temperature


Figure 23. Voltage Gain and Phase versus Frequency


Figure 24. Gain and Phase Margin versus Temperature

$\mathrm{R}_{\mathrm{T}}$, DIFFERENTIAL SOURCE RESISTANCE ( $\Omega$ )
Figure 25. Gain and Phase Margin versus Differential Source Resistance


Figure 26. Feedback Loop Gain and Phase versus Capacitive Load


Figure 27. Channel Separation versus Frequency


Figure 29. Equivalent Input Noise Voltage versus Frequency


Figure 31. Useable Supply Voltage versus Temperature


Figure 28. Output Voltage Swing versus Supply Voltage


Figure 30. Gain and Phase Margin versus Supply Voltage


Figure 32. Open Loop Gain versus Supply Voltage

## MC33502



Figure 33. 1.0 V Oscillator


Figure 34. 1.0 V Voiceband Filter


Figure 35. Power Supply Application


Figure 36. 1.0 V Current Pump

## MC33201, MC33202, MC33204

## Low Voltage, Rail-to-Rail Operational Amplifiers

The MC33201/2/4 family of operational amplifiers provide rail-to-rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages ( $\pm 0.9 \mathrm{~V}$ ) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

- Low Voltage, Single Supply Operation
(+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over-driven Input Signals
- High Output Current ( $\mathrm{I}_{\mathrm{SC}}=80 \mathrm{~mA}$, Typ)
- Low Supply Current ( $\mathrm{I}_{\mathrm{D}}=0.9 \mathrm{~mA}$, Typ)
- $600 \Omega$ Output Drive Capability
- Extended Operating Temperature Ranges
$\left(-40^{\circ}\right.$ to $+105^{\circ} \mathrm{C}$ and $-55^{\circ}$ to $\left.+125^{\circ} \mathrm{C}\right)$
- Typical Gain Bandwidth Product $=2.2 \mathrm{MHz}$

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ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 2505 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2505 of this data sheet.

PIN CONNECTIONS


CASE 751/846A

$$
\text { Output } 1 \text { Inputs } 1 \begin{cases}1 \\ \text { (Dual, Top View) }\end{cases}
$$




Figure 1. Circuit Schematic
(Each Amplifier)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | +13 | V |
| Input Differential Voltage Range | $\mathrm{V}_{\text {IDR }}$ | Note 1. | V |
| Common Mode Input Voltage Range (Note 2.) | $\mathrm{V}_{\mathrm{CM}}$ | $\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$ to | V |
|  |  | $\mathrm{V}_{\mathrm{EE}}-0.5 \mathrm{~V}$ |  |
| Output Short Circuit Duration | $\mathrm{t}_{\mathrm{S}}$ | Note 3. | sec |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Note 3. | mW |

DC ELECTRICAL CHARACTERISTICS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ )

| Characteristic | $\mathrm{V}_{\text {cc }}=2.0 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{cc}}=3.3 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage |  |  |  | mV |
| $\mathrm{V}_{10}$ (max) |  |  |  |  |
| MC33201 | $\pm 8.0$ | $\pm 8.0$ | $\pm 6.0$ |  |
| MC33202 | $\pm 10$ | $\pm 10$ | $\pm 8.0$ |  |
| MC33204 | $\pm 12$ | $\pm 12$ | $\pm 10$ |  |
| Output Voltage Swing |  |  |  |  |
| $\mathrm{V}_{\text {OH }}\left(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega\right)$ | 1.9 | 3.15 | 4.85 | $\mathrm{V}_{\text {min }}$ |
| $\mathrm{V}_{\text {OL }}\left(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega\right)$ | 0.10 | 0.15 | 0.15 | $V_{\text {max }}$ |
| Power Supply Current per Amplifier ( $\mathrm{I}_{\mathrm{D}}$ ) | 1.125 | 1.125 | 1.125 | mA |

Specifications at $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$ are guaranteed by the 2.0 V and 5.0 V tests. $\mathrm{V}_{\mathrm{EE}}=\mathrm{Gnd}$.
DC ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=$ Ground, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ```Input Offset Voltage ( \(\mathrm{V}_{\mathrm{CM}} 0 \mathrm{~V}\) to \(0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}} 1.0 \mathrm{~V}\) to 5.0 V ) MC33201: \(T_{A}=+25^{\circ} \mathrm{C}\) MC33201: \(T_{A}=-40^{\circ}\) to \(+105^{\circ} \mathrm{C}\) MC33201V: \(\mathrm{T}_{\mathrm{A}}=-55^{\circ}\) to \(+125^{\circ} \mathrm{C}\) MC33202: \(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) MC33202: \(\mathrm{T}_{\mathrm{A}}=-40^{\circ}\) to \(+105^{\circ} \mathrm{C}\) MC33202V: \(\mathrm{T}_{\mathrm{A}}=-55^{\circ}\) to \(+125^{\circ} \mathrm{C}\) MC33204: \(\quad \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\) MC33204: \(\mathrm{T}_{\mathrm{A}}=-40^{\circ}\) to \(+105^{\circ} \mathrm{C}\) MC33204V: \(\mathrm{T}_{\mathrm{A}}=-55^{\circ}\) to \(+125^{\circ} \mathrm{C}\)``` | 3 | $\left\|V_{10}\right\|$ | - - - - - - |  | $\begin{aligned} & 6.0 \\ & 9.0 \\ & 13 \\ & 8.0 \\ & 11 \\ & 14 \\ & 10 \\ & 13 \\ & 17 \end{aligned}$ | mV |
| $\begin{aligned} & \text { Input Offset Voltage Temperature Coefficient }\left(R_{S}=50 \Omega\right) \\ & T_{\mathrm{A}}=-40^{\circ} \text { to }+105^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | 4 | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | $\begin{aligned} & 2.0 \\ & 2.0 \end{aligned}$ | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Bias Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V} \text { to } 0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=1.0 \mathrm{~V} \text { to } 5.0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+105^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | 5, 6 | $\left\|I_{B B}\right\|$ | - | $\begin{gathered} 80 \\ 100 \end{gathered}$ | $\begin{aligned} & 200 \\ & 250 \\ & 500 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Offset Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V} \text { to } 0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=1.0 \mathrm{~V} \text { to } 5.0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+105^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | - | $\left\|{ }_{10}\right\|$ | - | $\begin{aligned} & 5.0 \\ & 10 \\ & - \end{aligned}$ | $\begin{gathered} 50 \\ 100 \\ 200 \end{gathered}$ | nA |
| Common Mode Input Voltage Range | - | $V_{\text {ICR }}$ | $\mathrm{V}_{\mathrm{EE}}$ | - | $\mathrm{V}_{\mathrm{CC}}$ | V |

1. The differential input voltage of each amplifier is limited by two internal parallel back-to-back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV .
3. Power dissipation must be considered to ensure maximum junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) is not exceeded. (See Figure 2)

DC ELECTRICAL CHARACTERISTICS (cont.) ( $\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Ground}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}\right) \\ & R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & R_{L}=600 \Omega \end{aligned}$ | 7 | Avol | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | $\begin{aligned} & 300 \\ & 250 \end{aligned}$ | - | kV/V |
| $\begin{aligned} & \text { Output Voltage Swing }\left(\mathrm{V}_{I D}= \pm 0.2 \mathrm{~V}\right) \\ & R_{L}=10 \mathrm{k} \Omega \\ & R_{L}=10 \mathrm{k} \Omega \\ & R_{L}=600 \Omega \\ & R_{L}=600 \Omega \end{aligned}$ | 8, 9, 10 | $\mathrm{V}_{\mathrm{OH}}$ <br> $V_{\text {OL }}$ <br> $V_{\mathrm{OH}}$ <br> $\mathrm{V}_{\mathrm{OL}}$ | $\begin{gathered} 4.85 \\ - \\ 4.75 \end{gathered}$ | $\begin{aligned} & 4.95 \\ & 0.05 \\ & 4.85 \\ & 0.15 \end{aligned}$ | $\begin{gathered} - \\ 0.15 \\ - \\ 0.25 \end{gathered}$ | V |
| Common Mode Rejection ( $\mathrm{V}_{\text {in }}=0 \mathrm{~V}$ to 5.0 V ) | 11 | CMR | 60 | 90 | - | dB |
| Power Supply Rejection Ratio $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=5.0 \mathrm{~V} / \mathrm{Gnd}$ to 3.0 $\mathrm{V} / \mathrm{Gnd}$ | 12 | PSRR | 500 | 25 | - | $\mu \mathrm{V} / \mathrm{V}$ |
| Output Short Circuit Current (Source and Sink) | 13, 14 | Isc | 50 | 80 | - | mA |
| $\begin{aligned} & \text { Power Supply Current per Amplifier }\left(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-40^{\circ} \text { to }+105^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-55^{\circ} \text { to }+125^{\circ} \mathrm{C} \end{aligned}$ | 15 | ID | - | $\begin{aligned} & 0.9 \\ & 0.9 \end{aligned}$ | $\begin{aligned} & 1.125 \\ & 1.125 \end{aligned}$ | mA |

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\right.$ Ground, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate $\left(\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=-2.0 \mathrm{~V} \text { to }+2.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~A}_{\mathrm{V}}=+1.0\right)$ | 16, 26 | SR | 0.5 | 1.0 | - | V/us |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | 17 | GBW | - | 2.2 | - | MHz |
| Gain Margin ( $\mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{C}_{L}=0 \mathrm{pF}$ ) | 20, 21, 22 | $\mathrm{A}_{\mathrm{M}}$ | - | 12 | - | dB |
| Phase Margin ( $\mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) | 20, 21, 22 | $\emptyset_{M}$ | - | 65 | - | Deg |
| Channel Separation ( $f=1.0 \mathrm{~Hz}$ to $20 \mathrm{kHz}, \mathrm{A}_{V}=100$ ) | 23 | CS | - | 90 | - | dB |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=600 \Omega$, $\mathrm{THD} \leq 1 \%$ ) |  | $\mathrm{BW}_{\mathrm{P}}$ | - | 28 | - | kHz |
| $\begin{aligned} & \text { Total Harmonic Distortion }\left(R_{L}=600 \Omega, V_{O}=1.0 V_{p p}, A_{V}=1.0\right) \\ & f=1.0 \mathrm{kHz} \\ & f=10 \mathrm{kHz} \end{aligned}$ | 24 | THD | - | $\begin{aligned} & 0.002 \\ & 0.008 \end{aligned}$ | - | \% |
| Open Loop Output Impedance $\left(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{f}=2.0 \mathrm{MHz}, \mathrm{~A}_{\mathrm{V}}=10\right)$ |  | $\left\|z_{0}\right\|$ | - | 100 | - | $\Omega$ |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) |  | $\mathrm{R}_{\text {in }}$ | - | 200 | - | k $\Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) |  | $\mathrm{C}_{\text {in }}$ | - | 8.0 | - | pF |
| $\begin{aligned} & \text { Equivalent Input Noise Voltage }\left(R_{S}=100 \Omega\right) \\ & f=10 \mathrm{~Hz} \\ & f=1.0 \mathrm{kHz} \end{aligned}$ | 25 | $\mathrm{e}_{\mathrm{n}}$ | - | $\begin{aligned} & 25 \\ & 20 \end{aligned}$ | - | $\begin{aligned} & \mathrm{nV} / \\ & \sqrt{\mathrm{Hz}} \end{aligned}$ |
| Equivalent Input Noise Current $\begin{aligned} & f=10 \mathrm{~Hz} \\ & f=1.0 \mathrm{kHz} \end{aligned}$ | 25 | $\mathrm{i}_{n}$ | - | $\begin{aligned} & 0.8 \\ & 0.2 \end{aligned}$ | - | $\frac{\mathrm{pA} /}{\sqrt{\mathrm{Hz}}}$ |



Figure 2. Maximum Power Dissipation versus Temperature


Figure 4. Input Offset Voltage Temperature Coefficient Distribution


Figure 6. Input Bias Current versus Common Mode Voltage


Figure 3. Input Offset Voltage Distribution


Figure 5. Input Bias Current versus Temperature


Figure 7. Open Loop Voltage Gain versus Temperature


Figure 8. Output Voltage Swing versus Supply Voltage


Figure 10. Output Voltage versus Frequency


Figure 12. Power Supply Rejection versus Frequency


Figure 9. Output Saturation Voltage versus Load Current


Figure 11. Common Mode Rejection versus Frequency


Figure 13. Output Short Circuit Current versus Output Voltage


Figure 14. Output Short Circuit Current versus Temperature


Figure 16. Slew Rate versus Temperature


Figure 18. Voltage Gain and Phase versus Frequency


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load


Figure 17. Gain Bandwidth Product versus Temperature


Figure 19. Voltage Gain and Phase versus Frequency


Figure 20. Gain and Phase Margin versus Temperature


Figure 22. Gain and Phase Margin versus Capacitive Load


Figure 24. Total Harmonic Distortion versus Frequency


Figure 21. Gain and Phase Margin versus Differential Source Resistance


Figure 23. Channel Separation versus Frequency


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency

## DETAILED OPERATING DESCRIPTION

## General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of $2.0 \mathrm{~V}, 3.3 \mathrm{~V}$ and 5.0 V and ground.

Since the common mode input voltage range extends from $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$, it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

## Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN-PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than $\mathrm{V}_{\mathrm{EE}}$, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.
In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive $600 \Omega$ loads. Because of this high output current capability, care should be taken not to exceed the $150^{\circ} \mathrm{C}$ maximum junction temperature.

t , TIME ( $5.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 26. Noninverting Amplifier Slew Rate

t, TIME ( $10 \mu \mathrm{~s} / \mathrm{DIV}$ )
Figure 27. Small Signal Transient Response


Figure 28. Large Signal Transient Response

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface
between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.


MC33201，MC33202，MC33204

ORDERING INFORMATION

| Operational Amplifier Function | Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| Single | MC33201D | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | SO－8 | 98 Units／Rail |
|  | MC33201DR2 |  | SO－8 | 2500 Units／Tape \＆Reel |
|  | MC33201P |  | Plastic DIP | 50 Units／Rail |
|  | MC33201VD | $\mathrm{T}_{\mathrm{A}}=-55^{\circ}$ to $125^{\circ} \mathrm{C}$ | SO－8 | 98 Units／Rail |
| Dual | MC33202D | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | SO－8 | 98 Units／Rail |
|  | MC33202DR2 |  | SO－8 | 2500 Units／Tape \＆Reel |
|  | MC33202DMR2 |  | Micro－8 | 4000 Units／Tape \＆Reel |
|  | MC33202P |  | Plastic DIP | 50 Units／Rail |
|  | MC33202VD | $\mathrm{T}_{\mathrm{A}}=-55^{\circ}$ to $125^{\circ} \mathrm{C}$ | SO－8 | 98 Units／Rail |
|  | MC33202VDR2 |  | SO－8 | 2500 Units／Tape \＆Reel |
|  | MC33202VP |  | Plastic DIP | 50 Units／Rail |
| Quad | MC33204D | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | SO－14 | 55 Units／Rail |
|  | MC33204DR2 |  | SO－14 | 2500 Units／Tape \＆Reel |
|  | MC33204DTB |  | TSSOP－14 | 96 Units／Rail |
|  | MC33204DTBR2 |  | TSSOP－14 | 2500 Units／Tape \＆Reel |
|  | MC33204P |  | Plastic DIP | 25 Units／Rail |
|  | MC33204VD | $\mathrm{T}_{\mathrm{A}}=-55^{\circ}$ to $125^{\circ} \mathrm{C}$ | SO－14 | 55 Units／Rail |
|  | MC33204VDR2 |  | SO－14 | 2500 Units／Tape \＆Reel |
|  | MC33204VP |  | Plastic DIP | 25 Units／Rail |

MARKING DIAGRAMS

| $\begin{gathered} \text { SO-8 } \\ \text { D SUFFIX } \\ \text { CASE } 751 \end{gathered}$ | $\begin{gathered} \text { SO-8 } \\ \text { VD SUFFIX } \\ \text { CASE } 751 \end{gathered}$ | PDIP－8 <br> P SUFFIX <br> CASE 626 | PDIP－8 <br> VP SUFFIX <br> CASE 626 | Micro－8 DM SUFFIX CASE 846A |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |
| $\begin{gathered} \text { SO-14 } \\ \text { D SUFFIX } \\ \text { CASE 751A } \end{gathered}$ | SO－14 VD SUFFIX CASE 751A | PDIP－14 P SUFFIX CASE 646 | PDIP－14 <br> VP SUFFIX <br> CASE 646 | TSSOP－14 DTB SUFFIX CASE 948G |
|  |  |  |  | $\begin{aligned} & 14 \\ & \text { A月 } \end{aligned}$ |
| MC33204D OAWLYWW OUQ 日 日 日 1 |  |  |  | MC33 <br> 204 <br> ALYW |
|  |  | X $=1$ or 2 <br> $A$ $=$ Assembly Lo <br> WL，L $=$ Wafer Lot <br> $Y Y, Y$ $=$ Year <br> WW，$W=$ Work Week  | cation | 1 |

## NCS2001

### 0.9 V, Rail-to-Rail, Single Operational Amplifier

The NCS2001 is an industry first sub-one volt operational amplifier that features a rail-to-rail common mode input voltage range, along with rail-to-rail output drive capability. This amplifier is guaranteed to be fully operational down to 0.9 V , providing an ideal solution for powering applications from a single cell Nickel Cadmium (NiCd) or Nickel Metal Hydride (NiMH) battery. Additional features include no output phase reversal with overdriven inputs, trimmed input offset voltage of 0.5 mV , extremely low input bias current of 40 pA , and a unity gain bandwidth of 1.4 MHz at 5.0 V . The tiny NCS2001 is the ideal solution for small portable electronic applications and is available in the space saving SOT23-5 and SC70-5 packages with two industry standard pinouts.

## Features

- 0.9 V Guaranteed Operation
- Rail-to-Rail Common Mode Input Voltage Range
- Rail-to-Rail Output Drive Capability
- No Output Phase Reversal for Over-Driven Input Signals
- 0.5 mV Trimmed Input Offset
- 10 pA Input Bias Current
- 1.4 MHz Unity Gain Bandwidth at $\pm 2.5 \mathrm{~V}, 1.1 \mathrm{MHz}$ at $\pm 0.5 \mathrm{~V}$
- Tiny SC70-5 and SOT23-5 Packages


## Typical Applications

- Single Cell NiCd/NiMH Battery Powered Applications
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand Held Instruments


This device contains 63 active transistors.

## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com

| SOT23-5 |
| :---: |
| (TSOP-5/SC59-5) |
| SN SUFFIX |
| CASE 483 |

DIAGRAMS

PIN CONNECTIONS


Style 1 Pinout (SN1T1, SQ1T1)


Style 2 Pinout (SN2T1, SQ2T1)

## ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 2520 of this data sheet.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | 7.0 | V |
| Input Differential Voltage Range (Note 1) | $\mathrm{V}_{\text {IDR }}$ | $\begin{gathered} \mathrm{V}_{\mathrm{EE}}-300 \mathrm{mV} \text { to } \\ 7.0 \mathrm{~V} \end{gathered}$ | V |
| Input Common Mode Voltage Range (Note 1) | VICR | $\begin{gathered} \mathrm{V}_{\mathrm{EE}}-300 \mathrm{mV} \text { to } \\ 7.0 \mathrm{~V} \end{gathered}$ | V |
| Output Short Circuit Duration (Note 2) | ${ }^{\text {tsc }}$ | Indefinite | sec |
| Junction Temperature | TJ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation and Thermal Characteristics SOT23-5 Package <br> Thermal Resistance, Junction to Air <br> Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ <br> SC70-5 Package <br> Thermal Resistance, Junction to Air Power Dissipation @ $T_{A}=70^{\circ} \mathrm{C}$ | $\begin{gathered} \mathrm{R}_{\text {QJA }} \\ \mathrm{P}_{\mathrm{D}} \\ \mathrm{R}_{\text {өJA }} \\ \mathrm{P}_{\mathrm{D}} \end{gathered}$ | $\begin{aligned} & 235 \\ & 340 \\ & \\ & 280 \\ & 286 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ mW <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ mW |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Protection at any Pin Human Body Model (Note 3) | $\mathrm{V}_{\text {ESD }}$ | 2000 | V |

1. Either or both inputs should not exceed the range of $\mathrm{V}_{\mathrm{EE}}-300 \mathrm{mV}$ to $\mathrm{V}_{\mathrm{EE}}+7.0 \mathrm{~V}$.
2. Maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.
$T_{J}=T_{A}+\left(P_{D} R_{\theta J A}\right)$
3. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS
( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =0.45 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.45 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =0^{\circ} \mathrm{C} \text { t } 70^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{10}$ | $\begin{aligned} & -6.0 \\ & -8.5 \\ & -9.5 \\ & -6.0 \\ & -7.0 \\ & -7.5 \\ & \hline \\ & -6.0 \\ & -7.5 \\ & -7.5 \end{aligned}$ | $\begin{gathered} 0.5 \\ - \\ - \\ 0.5 \\ - \\ - \\ 0.5 \\ - \end{gathered}$ | $\begin{aligned} & 6.0 \\ & 8.5 \\ & 9.5 \\ & 6.0 \\ & 7.0 \\ & 7.5 \\ & \\ & 6.0 \\ & 7.5 \\ & 7.5 \end{aligned}$ | mV |
| Input Offset Voltage Temperature Coefficient $\left(\mathrm{R}_{\mathrm{S}}=50\right)$ $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 8.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current ( $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}$ to 5.0 V ) | $I_{\text {IB }}$ | - | 10 | - | pA |
| Input Common Mode Voltage Range | $V_{\text {ICR }}$ | - | $\mathrm{V}_{\mathrm{EE}}$ to $\mathrm{V}_{\mathrm{CC}}$ | - | V |
| Large Signal Voltage Gain $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =0.45 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.45 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} & =10 \mathrm{k} \\ \mathrm{R}_{\mathrm{L}} & =2.0 \mathrm{k} \\ \mathrm{~V}_{\mathrm{CC}} & =1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} & =10 \mathrm{k} \\ \mathrm{R}_{\mathrm{L}} & =2.0 \mathrm{k} \\ \mathrm{~V}_{\mathrm{CC}} & =2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \\ \mathrm{R}_{\mathrm{L}} & =10 \mathrm{k} \\ \mathrm{R}_{\mathrm{L}} & =2.0 \mathrm{k} \end{aligned}$ | Avol | - 20 15 | $\begin{aligned} & 40 \\ & 20 \\ & 40 \\ & 40 \\ & 40 \\ & 40 \end{aligned}$ | - - - - - - | kV/V |

DC ELECTRICAL CHARACTERISTICS (continued)
( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ```Output Voltage Swing, High State Output ( \(\mathrm{V}_{\mathrm{ID}}=+0.5 \mathrm{~V}\) ) \(\mathrm{V}_{\mathrm{CC}}=0.45 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.45 \mathrm{~V}\) \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(70^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\) to \(105^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{V}_{\mathrm{CC}}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V}\) \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(70^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\) to \(105^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}\) \(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}\) to \(70^{\circ} \mathrm{C}\) \(\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\) \(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\) to \(105^{\circ} \mathrm{C}\) \(R_{L}=10 \mathrm{k}\) \(\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\)``` | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 0.40 \\ & 0.35 \\ & \\ & 0.40 \\ & 0.35 \\ & \\ & 0.40 \\ & 0.35 \\ & \\ & 1.45 \\ & 1.40 \\ & 1.45 \\ & 1.40 \\ & \\ & 1.45 \\ & 1.40 \\ & \\ & 2.45 \\ & 2.40 \\ & \\ & 2.45 \\ & 2.40 \\ & 2.45 \\ & 2.40 \end{aligned}$ | $\begin{gathered} 0.494 \\ 0.466 \\ - \\ - \\ - \\ - \\ 1.498 \\ 1.480 \\ - \\ - \\ - \\ - \\ - \\ 2.498 \\ 2.475 \end{gathered}$ |  | V |
| $\text { Output Voltage Swing, Low State Output }\left(\mathrm{V}_{\mathrm{ID}}=-0.5 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {OL }}$ | - - - - - - - - - - - - - - - - - - | $\begin{gathered} -0.494 \\ -0.480 \\ - \\ - \\ - \\ - \\ -1.493 \\ -1.480 \\ - \\ - \\ - \\ - \\ -2.492 \\ -2.479 \end{gathered}$ | -0.40 -0.35 -0.40 -0.35 -0.40 -0.35 -1.45 -1.40 -1.45 -1.40 -1.45 -1.40 -2.45 -2.40 -2.45 -2.40 -2.45 -2.40 | V |

DC ELECTRICAL CHARACTERISTICS (continued)
( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Common Mode Rejection Ratio ( $\mathrm{V}_{\text {in }}=0$ to 5.0 V ) | CMRR | 60 | 70 | - | dB |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=0.5 \mathrm{~V}$ to 2.5 V, $\mathrm{V}_{\mathrm{EE}}=-2.5 \mathrm{~V}$ ) | PSRR | 55 | 65 | - | dB |
| Output Short Circuit Current $\mathrm{V}_{\mathrm{CC}}=0.45 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.45 \mathrm{~V}, \mathrm{~V}_{\mathrm{ID}}= \pm 0.4 \mathrm{~V}$ <br> Source Current High Output State <br> Sink Current Low Output State $\mathrm{V}_{\mathrm{CC}}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{ID}}= \pm 0.5 \mathrm{~V}$ <br> Source Current High Output State Sink Current Low Output State $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{ID}}= \pm 0.5 \mathrm{~V}$ <br> Source Current High Output State Sink Current Low Output State | Isc | $\begin{gathered} 0.5 \\ - \\ 15 \\ - \\ 40 \end{gathered}$ | $\begin{gathered} 1.2 \\ -3.0 \\ 29 \\ -40 \\ \\ 76 \\ -96 \end{gathered}$ | $\begin{gathered} - \\ -1.5 \\ - \\ -20 \\ - \\ -50 \end{gathered}$ | mA |
| $\begin{aligned} & \text { Power Supply Current (Per Amplifier, } \left.\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{V}_{\mathrm{CC}}=0.45 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.45 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | ID | - - - - - - - - - | 0.51 - - 0.72 - - 0.82 | $\begin{aligned} & 1.10 \\ & 1.10 \\ & 1.10 \\ & 1.40 \\ & 1.40 \\ & 1.40 \\ & \\ & 1.50 \\ & 1.50 \\ & 1.50 \end{aligned}$ | mA |

## AC ELECTRICAL CHARACTERISTICS

( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{R}_{\text {in }}$ | - | > 1.0 | - | tera $\Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{C}_{\text {in }}$ | - | 3.0 | - | pF |
| Equivalent Input Noise Voltage ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $e_{n}$ | - | 100 | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| $\begin{aligned} & \hline \text { Gain Bandwidth Product }(f=100 \mathrm{kHz}) \\ & \mathrm{V}_{\mathrm{CC}}=0.45 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.45 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-1.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \end{aligned}$ | GBW | $\begin{gathered} - \\ - \\ 0.5 \end{gathered}$ | $\begin{aligned} & 1.1 \\ & 1.3 \\ & 1.4 \end{aligned}$ | - | MHz |
| Gain Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=5.0 \mathrm{pf}$ ) | Am | - | 6.5 | - | dB |
| Phase Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=5.0 \mathrm{pf}$ ) | ¢m | - | 60 | - | Deg |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{Vpp}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}, \mathrm{THD}=1.0 \%, \mathrm{~A}_{\mathrm{V}}=1.0$ ) | $\mathrm{BW}_{\mathrm{P}}$ | - | 80 | - | kHz |
| $\begin{aligned} & \text { Total Harmonic Distortion }\left(\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{Vpp}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}, \mathrm{~A}_{\mathrm{V}}=1.0\right) \\ & \mathrm{f}=1.0 \mathrm{kHz} \\ & \mathrm{f}=10 \mathrm{kHz} \end{aligned}$ | THD |  | $\begin{gathered} 0.008 \\ 0.08 \end{gathered}$ | - | \% |
| Slew Rate $\left(\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=-2.0 \mathrm{~V}\right.$ to $\left.2.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}, \mathrm{A}_{\mathrm{V}}=1.0\right)$ <br> Positive Slope <br> Negative Slope | SR | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 1.6 \\ & 1.6 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 6.0 \end{aligned}$ | V/us |



Figure 2. Split Supply Output Saturation vs. Load Resistance


Figure 3. Split Supply Output Saturation vs. Load Current


Figure 4. Input Bias Current vs. Temperature


Figure 5. Gain and Phase vs. Frequency

t , time ( $500 \mathrm{~ns} /$ Div)
Figure 6. Transient Response

t , time ( $1.0 \mu \mathrm{~s} /$ Div)
Figure 7. Slew Rate


Figure 8. Output Voltage vs. Frequency

f, Frequency (Hz)
Figure 10. Power Supply Rejection vs. Frequency

$\mathrm{V}_{\mathrm{S}}$, Supply Voltage (V)
Figure 12. Output Short Circuit Sourcing Current vs. Supply Voltage


Figure 9. Common Mode Rejection
vs. Frequency

$\mathrm{V}_{\mathrm{S}}$, Supply Voltage (V)
Figure 11. Output Short Circuit Sinking Current vs. Supply Voltage


Figure 13. Supply Current vs. Supply Voltage


Figure 14. Total Harmonic Distortion vs. Frequency with 1.0 V Supply


Figure 15. Total Harmonic Distortion vs. Frequency with 1.0 V Supply


Figure 16. Total Harmonic Distortion vs. Frequency with 5.0 V Supply


Figure 17. Total Harmonic Distortion vs. Frequency with 5.0 V Supply


Figure 18. Slew Rate vs. Temperature


Figure 19. Gain Bandwidth Product vs. Temperature


Figure 20. Voltage Gain and Phase vs. Frequency


Figure 22. Gain and Phase Margin vs. Differential Source Resistance


Figure 23. Gain and Phase Margin vs. Output Load Capacitance


Figure 25. Gain and Phase Margin vs. Supply Voltage


Figure 26. Open Loop Voltage Gain vs. Supply Voltage


Figure 28. Input Offset Voltage vs. Common Mode Input Voltage Range, $\mathrm{V}_{\mathrm{S}}= \pm 0.45 \mathrm{~V}$


Figure 27. Input Offset Voltage vs. Common Mode Input Voltage Range $\mathrm{V}_{\mathrm{S}}= \pm 2.5 \mathrm{~V}$


Figure 29. Common-Mode Input Voltage Range vs. Power Supply Voltage

## APPLICATION INFORMATION AND OPERATING DESCRIPTION

## GENERAL INFORMATION

The NCS2001 is an industry first rail-to-rail input, rail-to-rail output amplifier that features guaranteed sub one volt operation. This unique feature set is achieved with the use of a modified analog CMOS process that allows the implementation of depletion MOSFET devices. The amplifier has a 1.0 MHz gain bandwidth product, $2.2 \mathrm{~V} / \mu \mathrm{s}$ slew rate and is operational over a power supply range less than 0.9 V to as high as 7.0 V .

## Inputs

The input topology chosen for this device series is unconventional when compared to most low voltage operational amplifiers. It consists of an N -channel depletion mode differential transistor pair that drives a folded cascade stage and current mirror. This configuration extends the input common mode voltage range to encompass the $\mathrm{V}_{\mathrm{EE}}$ and $\mathrm{V}_{\mathrm{CC}}$ power supply rails, even when powered from a combined total of less than 0.9 volts. Figure 27 and 28 show the input common mode voltage range versus power supply voltage.

The differential input stage is laser trimmed in order to minimize offset voltage. The N -channel depletion mode MOSFET input stage exhibits an extremely low input bias current of less than 10 pA . The input bias current versus temperature is shown in Figure 4. Either one or both inputs can be biased as low as $\mathrm{V}_{\mathrm{EE}}$ minus 300 mV to as high as 7.0 V without causing damage to the device. If the input common mode voltage range is exceeded, the output will not display a phase reversal. If the maximum input positive or negative voltage ratings are to be exceeded, a series resistor must be used to limit the input current to less than 2.0 mA .

The ultra low input bias current of the NCS2001 allows the use of extremely high value source and feedback resistor without reducing the amplifier's gain accuracy. These high value resistors, in conjunction with the device input and printed circuit board parasitic capacitances $\mathrm{C}_{\mathrm{i}}$, will add an additional pole to the single pole amplifier in Figure 30. If low enough in frequency, this additional pole can reduce the phase margin and significantly increase the output settling time. The effects of $\mathrm{C}_{\mathrm{in}}$, can be canceled by placing a zero into the feedback loop. This is accomplished with the addition of capacitor $\mathrm{C}_{\mathrm{fb}}$. An approximate value for $\mathrm{C}_{\mathrm{fb}}$ can be calculated by:

$$
\mathrm{C}_{\mathrm{fb}}=\frac{\mathrm{R}_{\mathrm{in}} \times \mathrm{C}_{\mathrm{in}}}{\mathrm{R}_{\mathrm{fb}}}
$$



$$
\mathrm{C}_{\mathrm{in}}=\text { Input and printed circuit board capacitance }
$$

Figure 30. Input Capacitance Pole Cancellation

## Output

The output stage consists of complimentary P and N channel devices connected to provide rail-to-rail output drive. With a 2.0 k load, the output can swing within 50 mV of either rail. It is also capable of supplying over 75 mA when powered from 5.0 V and 1.0 mA when powered from 0.9 V .

When connected as a unity gain follower, the NCS2001 can directly drive capacitive loads in excess of 820 pF at room temperature without oscillating but with significantly reduced phase margin. The unity gain follower configuration exhibits the highest bandwidth and is most prone to oscillations when driving a high value capacitive load. The capacitive load in combination with the amplifier's output impedance, creates a phase lag that can result in an under-damped pulse response or a continuous oscillation. Figure 32 shows the effect of driving a large capacitive load in a voltage follower type of setup. When driving capacitive loads exceeding 820 pF , it is recommended to place a low value isolation resistor between the output of the op amp and the load, as shown in figure 31. The series resistor isolates the capacitive load from the output and enhances the phase margin. Refer to figure 33. Larger values of R will result in a cleaner output waveform but excessively large values will degrade the large signal rise and fall time and reduce the output amplitude. Depending upon the capacitor characteristics, the isolation resistor value will typically be between 50 to 500 ohms. The output drive capability for resistive and capacitive loads is shown in Figures 2, 3, and 23.


Isolation resistor $\mathrm{R}=50$ to 500
Figure 31. Capacitance Load Isolation

Note that the lowest phase margin is observed at cold temperature and low supply voltage.


Figure 32. Small Signal Transient Response with Large Capacitive Load


Figure 33. Small Signal Transient Response with Large Capacitive Load and Isolation Resistor.



The non-inverting input threshold levels are set so that the capacitor voltage oscillates between $1 / 3$ and $2 / 3$ of $\mathrm{V}_{\mathrm{CC}}$. This requires the resistors $\mathrm{R}_{1 \mathrm{a}}, \mathrm{R}_{1 \mathrm{~b}}$ and $\mathrm{R}_{2}$ to be of equal value. The following formula can be used to approximate the output frequency.

$$
\mathrm{f}_{\mathrm{O}}=\frac{1}{1.39 \mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}}
$$

Figure 34. 0.9 V Square Wave Oscillator


The timing capacitor $C_{T}$ will charge through diode $D_{2}$ and discharge through diode $D_{1}$, allowing a variable duty cycle. The pulse width of the signal can be programmed by adjusting the value of the trimpot. The capacitor voltage will oscillate between $1 / 3$ and $2 / 3$ of $V_{C C}$, since all the resistors at the non-inverting input are of equal value.

Figure 35. Variable Duty Cycle Pulse Generator


Figure 36. Positive Capacitance Multiplier


Figure 37. 1.0 V Voiceband Filter


Figure 38. High Compliance Current Sink


| $\mathbf{I}_{\mathbf{s}}$ | $\mathbf{V}_{\mathbf{O}}$ |
| :---: | :---: |
| 435 mA | 34.7 mV |
| 212 mA | 36.9 mV |

For best performance, use low tolerance resistors.

Figure 39. High Side Current Sense

ORDERING INFORMATION

| Device | Package | Shipping $^{\star}$ |
| :--- | :---: | :---: |
| NCS2001SN1T1 | SOT23-5 (TSOP-5/SC59-5) | 3000 Units on 7" Reel |
| NCS2001SN2T1 | SOT23-5 (TSOP-5/SC59-5) | 3000 Units on 7" Reel |
| NCS2001SQ1T1 | SC70-5 (SC-88A/SOT-353) | 3000 Units on 7" Reel |
| NCS2001SQ2T1 | SC70-5 (SC-88A/SOT-353) | 3000 Units on 7" Reel |

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


THIN SOT23-5
(TSOP-5/SC59-5)


SC70-5
(SC-88A/SOT-353)

## NCS7101

### 1.8 Volt Rail-to-Rail Operational Amplifier

The NCS7101 operational amplifier provides rail-to-rail operation on both the input and output. The output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the entire supply voltage range available. It is designed to work at very low supply voltages ( 1.8 V and ground), yet can operate with a supply of up to 10 V and ground. The NCS7101 is available in the space saving SOT23-5 package with two industry standard pinouts.

## Features

- Low Voltage, Single Supply Operation (1.8 V and Ground to 10 V and Ground)
- 1.0 pA Input Bias Current
- Unity Gain Bandwidth of 1.0 MHz at 5.0 V , 0.9 MHz at 1.8 V
- Output Voltage Swings Within 50 mV of Both Rails @ 1.8 V
- No Phase Reversal on the Output for Over-Driven Input Signals
- Input Offset Trimmed to 1.0 mV
- Low Supply Current ( $\mathrm{I}_{\mathrm{D}}=1.0 \mathrm{~mA}$ )
- Works Down to Two Discharged NiCd Battery Cells
- ESD Protected Inputs Up to 2.0 kV


## Typical Applications

- Dual NiCd/NiMH Cell Powered Systems
- Portable Communication Devices
- Low Voltage Active Filters
- Power Supply Monitor and Control
- Interface to DSP


This device contains 68 active transistors.
Figure 1. Typical Application

## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com

## LOW VOLTAGE <br> RAIL-TO-RAIL OPERATIONAL AMPLIFIER

| CASE 483 | MARKING <br> DIAGRAM |
| :--- | :--- |
| SOT23-5 |  |

## PIN CONNECTIONS



Style 1 Pin Out (SN1T1)


Style 2 Pin Out (SN2T1)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCS7101SN1T1 | SOT23-5 <br> (TSOP-5, <br> SC59-5) | 3000 Units/ <br> 7" Tape \& Reel |
| NCS7101SN2T1 | SOT23-5 <br> (TSOP-5, <br> SC59-5) | 3000 Units/ <br> 7" Tape \& Reel |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | 10 | V |
| Input Differential Voltage Range (Note 1) | $V_{\text {IDR }}$ | $\mathrm{V}_{\text {EE }}-300 \mathrm{mV}$ to 10 V | V |
| Input Common Mode Voltage Range (Note 1) | $V_{\text {ICR }}$ | $\mathrm{V}_{\mathrm{EE}}-300 \mathrm{mV}$ to 10 V | V |
| Output Short Circuit Duration (Note 2) | tsc | Indefinite | sec |
| Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation and Thermal Characteristics SOT23-5 Package <br> Thermal Resistance, Junction-to-Air Power Dissipation @ $T_{A}=70^{\circ} \mathrm{C}$ | $\begin{gathered} \mathrm{R}_{\text {QJA }} \\ \mathrm{P}_{\mathrm{D}} \end{gathered}$ | $\begin{aligned} & 220 \\ & 364 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ mW |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Protection at any Pin Human Body Model (Note 3) | $\mathrm{V}_{\text {ESD }}$ | 2000 | V |

1. Either or both inputs should not exceed the range of $\mathrm{V}_{\mathrm{EE}}-300 \mathrm{mV}$ to $\mathrm{V}_{\mathrm{EE}}+10 \mathrm{~V}$.
2. Maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded. $T_{J}=T_{A}+\left(P_{D} R_{\text {өJA }}\right)$
3. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS
( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=0, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

\begin{tabular}{|c|c|c|c|c|c|}
\hline Characteristics \& Symbol \& Min \& Typ \& Max \& Unit <br>
\hline Input Offset Voltage
$$
\begin{aligned}
\mathrm{V}_{\mathrm{CC}} & =0.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.9 \mathrm{~V} \\
\mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\
\mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\
\mathrm{~V}_{\mathrm{CC}} & =2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \\
\mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\
\mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\
\mathrm{~V}_{\mathrm{CC}} & =5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V} \\
\mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\
\mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}
\end{aligned}
$$ \& $\mathrm{V}_{10}$ \& $$
\begin{array}{r}
-7.0 \\
-9.0 \\
-7.0 \\
-9.0 \\
-7.0 \\
-9.0
\end{array}
$$ \& 0.6
-
0.6
-
0.6 \& $$
\begin{aligned}
& 7.0 \\
& 9.0 \\
& 7.0 \\
& 9.0 \\
& 7.0 \\
& 9.0
\end{aligned}
$$ \& mV <br>
\hline Input Offset Voltage Temperature Coefficient $\left(\mathrm{R}_{\mathrm{S}}=50\right)$
$$
\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C}
$$ \& $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ \& - \& 8.0 \& - \& $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br>
\hline Input Bias Current (VCC $=1.8 \mathrm{~V}$ to 10 V ) \& | ${ }_{\text {IB }}$ | \& - \& 1.0 \& - \& pA <br>
\hline Common Mode Input Voltage Range \& $V_{\text {ICR }}$ \& $\mathrm{V}_{\mathrm{EE}}$ \& - \& $\mathrm{V}_{\mathrm{CC}}$ \& V <br>
\hline Large Signal Voltage Gain
$$
\begin{gathered}
\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V} \\
\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\
\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega
\end{gathered}
$$ \& Avol \& $$
\begin{aligned}
& 16 \\
& 16
\end{aligned}
$$ \& 50
30 \& \& kV/V <br>
\hline $$
\begin{aligned}
& \text { Output Voltage Swing, High }\left(\mathrm{V}_{I D}= \pm 0.2 \mathrm{~V}\right) \\
& \mathrm{V}_{\mathrm{CC}}=0.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.9 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\
& \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \\
& \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \\
& \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\
& \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \\
& R_{\mathrm{L}}=2.0 \mathrm{k} \\
& \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\
& R_{\mathrm{L}}=600 \\
& R_{\mathrm{L}}=2.0 \mathrm{k} \\
& \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\
& R_{\mathrm{L}}=600 \\
& R_{\mathrm{L}}=2.0 \mathrm{k} \\
& \mathrm{~V}_{C C}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}\left(\mathrm{~T}_{A}=25^{\circ} \mathrm{C}\right) \\
& R_{\mathrm{L}}=600 \\
& R_{\mathrm{L}}=2.0 \mathrm{k} \\
& \mathrm{~T}_{\mathrm{A}}=40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\
& R_{\mathrm{L}}=600 \\
& R_{\mathrm{L}}=2.0 \mathrm{k}
\end{aligned}
$$ \& $\mathrm{V}_{\mathrm{OH}}$ \& 0.85
0.80
0.85
0.79

2.10
2.35

2.00
2.40

4.40
4.80

4.40
4.80 \& 0.88
0.82
-
-
-
2.21
2.44
-
-
4.60

4.88 \& | - |
| :--- |
| - |
| - |
| - |
| - |
| - |
| - |
| - |
| - |
| - |
| - |
| - |
| - | \& V <br>

\hline
\end{tabular}

DC ELECTRICAL CHARACTERISTICS (continued)
( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=0, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \text { Output Voltage Swing, Low }\left(\mathrm{V}_{I \mathrm{D}}= \pm 0.2 \mathrm{~V}\right) \\ & \mathrm{V}_{\mathrm{CC}}=0.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.9 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \\ & \mathrm{~V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \mathrm{R}_{\mathrm{L}}=600 \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{L}}=600 \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & R_{\mathrm{L}}=600 \\ & R_{\mathrm{L}}=2.0 \mathrm{k} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\ & \mathrm{R}_{\mathrm{L}}=600 \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - - - - - - - - - - - - - | -0.88 -0.82 - - -2.22 -2.38 - - -4.66 -4.88 | -0.85 -0.80 -0.85 -0.78 -2.10 -2.35 -2.00 -2.30 -4.40 -4.80 -4.35 -4.80 | V |
| Common Mode Rejection Ratio $\begin{aligned} & \mathrm{V}_{\text {in }}=0 \text { to } 10 \mathrm{~V} \\ & \mathrm{~V}_{\text {in }}=0 \text { to } 5.0 \mathrm{~V} \end{aligned}$ | CMRR | $\begin{aligned} & 65 \\ & 60 \end{aligned}$ | - |  | dB |
| Power Supply Rejection Ratio <br> $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=10 \mathrm{~V} /$ Ground, $\Delta \mathrm{V}_{\mathrm{S}}=2.5 \mathrm{~V}$ | PSRR | 65 | - | - | dB |
| Output Short Circuit Current ( $\mathrm{V}_{\text {in }}$ Diff $= \pm 1.0 \mathrm{~V}$ ) $\mathrm{V}_{\mathrm{CC}}=+0.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.9 \mathrm{~V}$ <br> Source <br> Sink $\mathrm{V}_{\mathrm{CC}}=+2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}$ <br> Source <br> Sink $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}$ <br> Source <br> Sink | Isc | $\begin{gathered} 20 \\ -60 \end{gathered}$ $50$ $-140$ | $\begin{gathered} 3.0 \\ -3.0 \\ \\ 25 \\ -25 \\ \\ 72 \\ -72 \end{gathered}$ | $\begin{gathered} - \\ 60 \\ -20 \\ 140 \\ -50 \\ -5 \end{gathered}$ | mA |
| $\begin{gathered} \text { Power Supply Current }(\mathrm{V} \text { O }=0 \mathrm{~V}) \\ \mathrm{V}_{\mathrm{CC}}=+0.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-0.9 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=+2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C} \end{gathered}$ | ID | - - - - - - | 0.97 - 1.05 - 1.13 - | $\begin{aligned} & 1.20 \\ & 1.30 \\ & 1.30 \\ & 1.40 \\ & 1.40 \\ & 1.50 \end{aligned}$ | mA |

AC ELECTRICAL CHARACTERISTICS
( $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{O}}=0, \mathrm{R}_{\mathrm{L}}$ to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate ( $\mathrm{V}_{\mathrm{O}}=-2.0$ to $2.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{A}_{\mathrm{V}}=1.0$ ) | SR | 0.7 | 1.2 | 3.0 | V/us |
| Gain Bandwidth Product ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ ) | GBW | 0.5 | 1.0 | 3.0 | MHz |
| Gain Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=5.0 \mathrm{pF}$ ) | Am | - | 6.5 | - | dB |
| Phase Margin ( $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=5.0 \mathrm{pF}$ ) | ¢m | - | 60 | - | Deg |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{Vpp}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$, THD $\leq 1.0 \%$ ) | $\mathrm{BW}_{\mathrm{P}}$ | - | 130 | - | kHz |
| $\begin{aligned} & \text { Total Harmonic Distortion }\left(\mathrm{V}_{\mathrm{O}}=4.0 \mathrm{Vpp}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~A}_{\mathrm{V}}=1.0\right) \\ & \begin{array}{l} \mathrm{f}=1.0 \mathrm{kHz} \\ \mathrm{f}=10 \mathrm{kHz} \end{array} \end{aligned}$ | THD | - | $\begin{gathered} 0.02 \\ 0.2 \end{gathered}$ | - | \% |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{R}_{\text {in }}$ | - | >1.0 | - | tera $\Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{C}_{\text {in }}$ | - | 2.0 | - | pF |
| Equivalent Input Noise Voltage (Freq = 1.0 kHz ) | $\mathrm{e}_{\mathrm{n}}$ | - | 140 | - | $\mathrm{nV} / \sqrt{ } \mathrm{Hz}$ |



Figure 2. Output Saturation Voltage versus Load Resistance


Figure 3. Output Saturation Voltage versus Load Current


Figure 4. Input Bias Current versus Temperature


Figure 5. Gain and Phase versus Frequency

t , time ( $500 \mathrm{~ns} /$ Div)
Figure 6. Transient Response

t , time ( $1.0 \mu \mathrm{~s} /$ Div)
Figure 7. Slew Rate


Figure 8. Output Voltage versus Frequency


Figure 10. Power Supply Rejection versus Frequency


Figure 12. Output Short Circuit Sourcing Current versus Supply Voltage


Figure 9. Common Mode Rejection versus Frequency


Figure 11. Output Short Circuit Sinking Current versus Supply Voltage


Figure 13. Supply Current versus Supply Voltage with No Load


Figure 14. Total Harmonic Distortion versus Frequency with 5.0 V Supply


Figure 15. Total Harmonic Distortion versus Frequency with 10 V Supply


Figure 16. Total Harmonic Distortion versus Frequency with 5.0 V Supply


Figure 18. Slew Rate versus Temperature (Avg.)


Figure 19. Gain Bandwidth Product versus Temperature


Figure 20. Voltage Gain and Phase versus Frequency


Figure 21. Gain and Phase Margin versus Temperature


Figure 22. Gain and Phase Margin versus Differential Source Resistance


Figure 24. Output Voltage Swing versus Supply Voltage


Figure 25. Gain and Phase Margin versus Supply Voltage


Figure 26. Open Loop Voltage Gain versus Supply Voltage (Split Supplies)


Figure 27. Input Offset Voltage versus Common Mode Input Voltage Range, $\mathrm{V}_{\mathrm{S}}= \pm \mathbf{2 . 5} \mathrm{V}$


Figure 28. Input Offset Voltage versus Common Mode Input Voltage Range, $\mathrm{V}_{\mathrm{S}}= \pm 0.9 \mathrm{~V}$


Figure 29. Common-Mode Input Voltage Range versus Power Supply Voltage

## APPLICATION INFORMATION AND OPERATING DESCRIPTION

## GENERAL INFORMATION

The NCS7101 is a rail-to-rail input, rail-to-rail output operational amplifier that features guaranteed 1.8 volt operation. This feature is achieved with the use of a modified analog CMOS process that allows the implementation of depletion MOSFET devices. The amplifier has a 1.0 MHz gain bandwidth product, $1.2 \mathrm{~V} / \mu \mathrm{s}$ slew rate and is operational over a power supply range less than 1.8 V to as high as 10 V .

## Inputs

The input topology of this device series is unconventional when compared to most low voltage operational amplifiers. It consists of an N -channel depletion mode differential transistor pair that drives a folded cascode stage and current mirror. This configuration extends the input common mode voltage range to encompass the $\mathrm{V}_{\mathrm{EE}}$ and $\mathrm{V}_{\mathrm{CC}}$ power supply rails, even when powered from a combined total of less than 1.8 volts. Figures 27 and 28 show the input common mode voltage range versus power supply voltage.

The differential input stage is laser trimmed in order to minimize offset voltage. The N-channel depletion mode MOSFET input stage exhibits an extremely low input bias current of less than 40 pA . The input bias current versus temperature is shown in Figure 4. Either one or both inputs can be biased as low as $\mathrm{V}_{\text {EE }}$ minus 300 mV to as high as 10 V without causing damage to the device. If the input common mode voltage range is exceeded, the output will not display a phase reversal but it may latch in the appropriate high or low state. The device can then be reset by removing and reapplying power. If the maximum input positive or negative voltage ratings are to be exceeded, a series resistor must be used to limit the input current to less than 2.0 mA .
The ultra low input bias current of the NCS7101 allows the use of extremely high value source and feedback resistor without reducing the amplifier's gain accuracy. These high value resistors, in conjunction with the device input and printed circuit board parasitic capacitances $\mathrm{C}_{\mathrm{in}}$, will add an additional pole to the single pole amplifier shown in Figure 30. If low enough in frequency, this additional pole can reduce the phase margin and significantly increase the output settling time. The effects of $\mathrm{C}_{\mathrm{in}}$, can be canceled by placing a zero into the feedback loop. This is accomplished with the addition of capacitor $\mathrm{C}_{\mathrm{fb}}$. An approximate value for $\mathrm{C}_{\mathrm{fb}}$ can be calculated by:

$$
\mathrm{C}_{\mathrm{fb}}=\frac{\mathrm{R}_{\mathrm{in}} \times \mathrm{C}_{\mathrm{in}}}{\mathrm{R}_{\mathrm{fb}}}
$$



$$
\mathrm{C}_{\text {in }}=\text { Input and printed circuit board capacitance }
$$

Figure 30. Input Capacitance Pole Cancellation

## Output

The output stage consists of complimentary P and N channel devices connected to provide rail-to-rail output drive. With a 2.0 k load, the output can swing within 100 mV of either rail. It is also capable of supplying over 95 mA when powered from 10 V and 3.0 mA when powered from 1.8 V .

When connected as a unity gain follower, the NCS7101 can directly drive capacitive loads in excess of 390 pF at room temperature without oscillating but with significantly reduced phase margin. The unity gain follower configuration exhibits the highest bandwidth and is most prone to oscillations when driving a high value capacitive load. The capacitive load in combination with the amplifier's output impedance, creates a phase lag that can result in an under-damped pulse response or a continuous oscillation. Figure 32 shows the effect of driving a large capacitive load in a voltage follower type of setup. When driving capacitive loads exceeding 390 pF , it is recommended to place a low value isolation resistor between the output of the op amp and the load, as shown in Figure 31. The series resistor isolates the capacitive load from the output and enhances the phase margin. Refer to Figure 33. Larger values of R will result in a cleaner output waveform but excessively large values will degrade the large signal rise and fall time and reduce the output's amplitude. Depending upon the capacitor characteristics, the isolation resistor value will typically be between 50 to 500 ohms. The output drive capability for resistive and capacitive loads is shown in Figures 2, 3, and 23.


Isolation resistor $\mathrm{R}=50$ to 500
Figure 31. Capacitance Load Isolation
Note that the lowest phase margin is observed at cold temperature and low supply voltage.


Figure 32. Small Signal Transient Response with Large Capacitive Load


Figure 33. Small Signal Transient Response with Large Capacitive Load and Isolation Resistor.


Output Voltage

Timing Capacitor
Voltage


The non-inverting input threshold levels are set so that the capacitor voltage oscillates between $1 / 3$ and $2 / 3$ of $V_{C C}$. This requires the resistors $R_{1 \mathrm{a}}, R_{1 b}$ and $R_{2}$ to be of equal value. The following formula can be used to approximate the output frequency.

$$
\mathrm{f}_{\mathrm{O}}=\frac{1}{1.39 \mathrm{R}_{\mathrm{T}} \mathrm{C}_{\mathrm{T}}}
$$

Figure 34. Square Wave Oscillator


The timing capacitor $C_{T}$ will charge through diode $D_{2}$ and discharge through diode $\mathrm{D}_{1}$, allowing a variable duty cycle. The pulse width of the signal can be programmed by adjusting the value of the trimpot. The capacitor voltage will oscillate between $1 / 3$ and $2 / 3$ of $\mathrm{V}_{\mathrm{CC}}$, since all the resistors at the non-inverting input are of equal value.

Figure 35. Variable Duty Cycle Pulse Generator


Figure 36. Positive Capacitance Multiplier



$$
\mathrm{f}_{\mathrm{L}}=\frac{1}{2 \pi \mathrm{R}_{1} \mathrm{C}_{1}} \approx 200 \mathrm{~Hz}
$$

$$
\mathrm{f}_{\mathrm{H}}=\frac{1}{2 \pi \mathrm{R}_{\mathrm{f}} \mathrm{C}_{\mathrm{f}}} \approx 4.0 \mathrm{kHz}
$$

$$
A_{f}=1+\frac{R_{f}}{R_{2}}=11
$$

Figure 37. Voice Band Filter


Figure 38. High Compliance Current Sink


Figure 39. High Side Current Sense

$i_{L}=\frac{V_{S}}{R_{1}}$, Note that $i_{L}$ is independent of $R_{L}$

Figure 40. Current Source


Figure 41. Current to Voltage Converter


Figure 42. Voltage to Current Converter


Figure 43. Differential Amplifier


Figure 44. Summing Amplifier

## MC33171, MC33172, MC33174

## Single Supply 3.0 V to 44 V, Low Power Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/72/74 series of monolithic operational amplifiers. These devices operate at $180 \mu \mathrm{~A}$ per amplifier and offer 1.8 MHz of gain bandwidth product and $2.1 \mathrm{~V} / \mu \mathrm{s}$ slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage includes ground potential ( $\mathrm{V}_{\mathrm{EE}}$ ). With a Darlington input stage, these devices exhibit high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33171/72/74 are specified over the industrial/ automotive temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic as well as the surface mount packages.

- Low Supply Current: $180 \mu \mathrm{~A}$ (Per Amplifier)
- Wide Supply Operating Range: 3.0 V to 44 V or $\pm 1.5 \mathrm{~V}$ to $\pm 22 \mathrm{~V}$
- Wide Input Common Mode Range, Including Ground ( $\mathrm{V}_{\mathrm{EE}}$ )
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/ $\mu \mathrm{s}$
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: -14.2 V to +14.2 V (with $\pm 15 \mathrm{~V}$ Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.03\%
- Excellent Phase Margin: $60^{\circ}$
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection
- ESD Diodes Provide Input Protection for Dual and Quad

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com

|  | PDIP-8 P SUFFIX CASE 626 SO-8 <br> D, VD SUFFIX CASE 751 |
| :---: | :---: |
|  | PDIP-14 <br> P, VP SUFFIX <br> CASE 646 |
|  | SO-14 <br> D, VD SUFFIX CASE 751A |
|  | $\begin{aligned} & \text { TSSOP-14 } \\ & \text { DTB SUFFIX } \\ & \text { CASE 948G } \end{aligned}$ |

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2545 of this data sheet.

See general marking information in the device marking section on page 2545 of this data sheet.

PIN CONNECTIONS


DUAL


(Top View)


Figure 1. Representative Schematic Diagram
(Each Amplifier)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}$ | $\pm 22$ | V |
| Input Differential Voltage Range | $\mathrm{V}_{\text {IDR }}$ | (Note 1) | V |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | (Note 1) | V |
| Output Short Circuit Duration (Note 2) | $\mathrm{t}_{\mathrm{SC}}$ | Indefinite | sec |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

DC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}\right.$ connected to ground, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

\begin{tabular}{|c|c|c|c|c|c|}
\hline Characteristics \& Symbol \& Min \& Typ \& Max \& Unit <br>
\hline $$
\begin{aligned}
& \text { Input Offset Voltage }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}\right) \\
& \mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 3) }
\end{aligned}
$$ \& $\mathrm{V}_{10}$ \& $$
\begin{aligned}
& - \\
& \text { - }
\end{aligned}
$$ \& $$
\begin{aligned}
& 2.0 \\
& 2.5
\end{aligned}
$$ \& $$
\begin{aligned}
& 4.5 \\
& 5.0 \\
& 6.5
\end{aligned}
$$ \& mV <br>
\hline Average Temperature Coefficient of Offset Voltage \& $\Delta \mathrm{V}_{\mathrm{IO}} / \Delta \mathrm{T}$ \& - \& 10 \& - \& $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br>
\hline $$
\begin{aligned}
& \text { Input Bias Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}\right) \\
& \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\text { Note 3) }
\end{aligned}
$$ \& $\mathrm{IIB}^{\text {I }}$ \& - \& 20 \& $$
\begin{aligned}
& 100 \\
& 200
\end{aligned}
$$ \& nA <br>
\hline $$
\begin{aligned}
& \text { Input Offset Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}\right) \\
& \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}(\text { Note 3) }
\end{aligned}
$$ \& 10 \& - \& 5.0 \& $$
\begin{aligned}
& 20 \\
& 40
\end{aligned}
$$ \& nA <br>
\hline $$
\begin{aligned}
& \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}\right) \\
& \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 3) }
\end{aligned}
$$ \& Avol \& $$
\begin{aligned}
& 50 \\
& 25
\end{aligned}
$$ \& 500 \& - \& V/mV <br>
\hline $$
\begin{aligned}
& \text { Output Voltage Swing } \\
& V_{C C}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, R_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } T_{\text {high }} \text { (Note 3) } \\
& \mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, R_{\mathrm{L}}=10 \mathrm{k}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 3) }
\end{aligned}
$$ \& $\mathrm{V}_{\mathrm{OH}}$

$\mathrm{V}_{\mathrm{OL}}$ \& \[
$$
\begin{gathered}
3.5 \\
13.6 \\
13.3
\end{gathered}
$$

\] \& \[

$$
\begin{gathered}
4.3 \\
14.2 \\
- \\
\hline 0.05 \\
-14.2
\end{gathered}
$$

\] \& | - |
| :---: |
| - |
| - |
| 0.15 |
| -13.6 |
| -13.3 | \& V <br>

\hline Output Short Circuit ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) Input Overdrive $=1.0 \mathrm{~V}$, Output to Ground Source Sink \& Isc \& \[
$$
\begin{aligned}
& 3.0 \\
& 15
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& 5.0 \\
& 27
\end{aligned}
$$
\] \& - \& mA <br>

\hline Input Common Mode Voltage Range

$$
\begin{aligned}
& \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 3) }
\end{aligned}
$$ \& VICR \& \multicolumn{3}{|c|}{\[

$$
\begin{aligned}
& V_{E E} \text { to }\left(V_{C C}-1.8\right) \\
& V_{E E} \text { to }\left(V_{C C}-2.2\right)
\end{aligned}
$$
\]} \& V <br>

\hline Common Mode Rejection Ratio ( $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k}$ ), $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ \& CMRR \& 80 \& 90 \& - \& dB <br>
\hline Power Supply Rejection Ratio ( $\mathrm{R}_{\mathrm{S}}=100 \Omega$ ), $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ \& PSRR \& 80 \& 100 \& - \& dB <br>

\hline $$
\begin{aligned}
& \text { Power Supply Current (Per Amplifier) } \\
& \mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\
& \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \text { (Note 3) }
\end{aligned}
$$ \& ID \&  \& \[

$$
\begin{aligned}
& 180 \\
& 220
\end{aligned}
$$

\] \& \[

$$
\begin{aligned}
& 250 \\
& 250 \\
& 300
\end{aligned}
$$
\] \& $\mu \mathrm{A}$ <br>

\hline
\end{tabular}

1. Either or both input voltages must not exceed the magnitude of $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$.
2. Power dissipation must be considered to ensure maximum junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) is not exceeded.
$\begin{array}{lll}\text { 3. MC3317x } & \mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} & \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C} \\ \text { MC317xV } & \mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C} & \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}\end{array}$

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}\right.$ connected to ground, $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Slew Rate }\left(\mathrm{V}_{\text {in }}=-10 \mathrm{~V} \text { to }+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}\right) \\ & \mathrm{A}_{\mathrm{V}}+1 \\ & \mathrm{~A}_{\mathrm{V}}-1 \end{aligned}$ | SR | 1.6 - | $\begin{aligned} & 2.1 \\ & 2.1 \end{aligned}$ | - | V/us |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | GBW | 1.4 | 1.8 | - | MHz |
| Power Bandwidth $A_{V}=+1.0 R_{L}=10 \mathrm{k}, \mathrm{~V}_{\mathrm{O}}=20 \mathrm{~V}_{\mathrm{pp}}, \mathrm{THD}=5 \%$ | BWp | - | 35 | - | kHz |
| Phase Margin $\begin{aligned} & R_{\mathrm{L}}=10 \mathrm{k} \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF} \end{aligned}$ | $\phi_{m}$ | - | $\begin{aligned} & 60 \\ & 45 \end{aligned}$ | - | Deg |
| Gain Margin $\begin{aligned} & R_{L}=10 k \\ & R_{L}=10 k, C_{L}=100 \mathrm{pF} \end{aligned}$ | $\mathrm{A}_{\mathrm{m}}$ | - | $\begin{aligned} & 15 \\ & 5.0 \end{aligned}$ | - | dB |
| Equivalent Input Noise Voltage $\mathrm{R}_{\mathrm{S}}=100 \Omega, \mathrm{f}=1.0 \mathrm{kHz}$ | $\mathrm{e}_{\mathrm{n}}$ | - | 32 | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Equivalent Input Noise Current ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $\mathrm{In}_{n}$ | - | 0.2 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |
| Differential Input Resistance $\mathrm{V}_{\mathrm{cm}}=0 \mathrm{~V}$ | $\mathrm{R}_{\text {in }}$ | - | 300 | - | $\mathrm{M} \Omega$ |
| Input Capacitance | $\mathrm{C}_{\text {in }}$ | - | 0.8 | - | pF |
| Total Harmonic Distortion $A_{V}=+10, R_{L}=10 \mathrm{k}, 2.0 \mathrm{~V}_{\mathrm{pp}} \leq \mathrm{V}_{\mathrm{O}} \leq 20 \mathrm{~V}_{\mathrm{pp}}, f=10 \mathrm{kHz}$ | THD | - | 0.03 | - | \% |
| Channel Separation ( $\mathrm{f}=10 \mathrm{kHz}$ ) | CS | - | 120 | - | dB |
| Open Loop Output Impedance ( $\mathrm{f}=1.0 \mathrm{MHz}$ ) | $\mathrm{z}_{0}$ | - | 100 | - | $\Omega$ |



Figure 2. Input Common Mode Voltage Range versus Temperature


Figure 3. Split Supply Output Saturation versus Load Current


Figure 4. Open Loop Voltage Gain and Phase versus Frequency


Figure 6. Normalized Gain Bandwidth Product and Slew Rate versus Temperature


Figure 8. Output Impedance and Frequency


Figure 5. Phase Margin and Percent Overshoot versus Load Capacitance


Figure 7. Small and Large Signal Transient Response


Figure 9. Supply Current versus Supply Voltage

## APPLICATIONS INFORMATION - CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the $\mathrm{V}_{\mathrm{EE}}$ potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to $\pm 44 \mathrm{~V}$, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\text {EE }}$ supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the $\mathrm{V}_{\mathrm{CC}}$ voltage by approximately 3.0 V and decrease below the $\mathrm{V}_{\mathrm{EE}}$ voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from $\mathrm{V}_{\mathrm{EE}}$ through either inputs' clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower ( 0.8 pF ) than that of a typical JFET ( 3.0 pF ), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D-to-A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd Order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For $10 \mathrm{k} \Omega$ of feedback resistance, the MC33171/72/74 family can typically settle to within $1 / 2 \mathrm{LSB}$ of 8 bits in $4.2 \mu \mathrm{~s}$, and within $1 / 2 \mathrm{LSB}$ of 12 bits in $4.8 \mu \mathrm{~s}$ for a 10 V step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically $\pm 2.1 \mathrm{~V} / \mu \mathrm{s}$. In the classic noninverting unity gain configuration the typical output positive slew rate is also $2.1 \mathrm{~V} / \mu \mathrm{s}$, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A $10 \mathrm{k} \Omega$ load resistance can typically swing within
0.8 V of the positive rail $\left(\mathrm{V}_{\mathrm{CC}}\right)$ and negative rail $\left(\mathrm{V}_{\mathrm{EE}}\right)$, providing a 28.4 Vpp swing from $\pm 15 \mathrm{~V}$ supplies. This large output swing becomes most noticeable at lower supply voltages.
The positive swing is limited by the saturation voltage of the current source transistor Q7, the VBE of the NPN pull-up transistor Q17, and the voltage drop associated with the short circuit resistance, R5. For sink currents less than 0.4 mA , the negative swing is limited by the saturation voltage of the pull-down transistor Q15, and the voltage drop across R4 and R5. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of $\mathrm{V}_{\mathrm{EE}}$. For sink currents ( $>0.4 \mathrm{~mA}$ ), diode D3 clamps the voltage across R4. Thus the negative swing is limited by the saturation voltage of Q 15 , plus the forward diode drop of $\mathrm{D} 3\left(\approx \mathrm{~V}_{\mathrm{EE}}+1.0 \mathrm{~V}\right)$. Therefore an unprecedented peak-to-peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.
If the load resistance is referenced to $\mathrm{V}_{\mathrm{CC}}$ instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to $\mathrm{V}_{\mathrm{CC}}$ during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.
Because the PNP output emitter-follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of $\left(\mathrm{V}_{\mathrm{EE}}+1.8 \mathrm{~V}\right)$. In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for current switching applications.
In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth product. The associated high frequency low output impedance ( $200 \Omega$ typ @ 1.0 MHz ) allows capacitive drive capability from 0 pF to 400 pF without oscillation in the noninverting unity gain configuration. The $60^{\circ}$ phase margin and 15 dB gain margin, as well as the general gain and phase characteristics, are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The AC characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 V , these amplifiers are functional to at least 3.0 V @ $25^{\circ} \mathrm{C}$. However slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity, or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input
pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.
The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for $\pm 15 \mathrm{~V}$ supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.


Figure 10. AC Coupled Noninverting Amplifier with Single +5.0 V Supply


BW ( -3.0 dB ) $=200 \mathrm{kHz}$

Figure 12. DC Coupled Inverting Amplifier Maximum Output Swing with Single +5.0 V Supply


Figure 14. Active High-Q Notch Filter


Figure 11. AC Coupled Inverting Amplifier with Single +5.0 V Supply


Offset Nulling range is approximately $\pm 80 \mathrm{mV}$ with a 10 k potentiometer, MC33171 only.

Figure 13. Offset Nulling Circuit


Choose Value $\mathrm{f}_{\mathrm{o}}, \mathrm{Q}, \mathrm{A}_{0}, \mathrm{C}$
For less than $10 \%$ error for operational amplifier, where $f_{0}$ and GBW are expressed in Hz .

Figure 15. Active Bandpass Filter

ORDERING INFORMATION

| Op Amp Function | Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| Single | MC33171D <br> MC33171DR2 <br> MC33171P | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | $\begin{aligned} & \text { SO-8 } \\ & \text { SO-8/Tape \& Reel } \\ & \text { Plastic DIP } \end{aligned}$ | 98 Units/Rail <br> 2500 Units/Tape \& Reel <br> 50 Units/Rail |
| Dual | MC33172D <br> MC33172DR2 <br> MC33172P | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | $\begin{aligned} & \hline \text { SO-8 } \\ & \text { SO-8/Tape \& Reel } \\ & \text { Plastic DIP } \end{aligned}$ | 98 Units/Rail <br> 2500 Units/Tape \& Reel <br> 50 Units/Rail |
|  | MC33172VD MC33172VDR2 | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | $\begin{aligned} & \hline \text { SO-8 } \\ & \text { SO-8/Tape \& Reel } \end{aligned}$ | 98 Units/Rail 2500 Units/Tape \& Reel |
| Quad | MC33174D <br> MC33174DR2 <br> MC33174DTB <br> MC33174DTBR2 <br> MC33174P | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-14 <br> SO-14/Tape \& Reel <br> SO-14 <br> SO-14/Tape \& Reel <br> Plastic DIP | 55 Units/Rail 2500 Units/Tape \& Reel 96 Units/Rail 2500 Units/Tape \& Reel 25 Units/Rail |
|  | MC33174VDR2 MC33174VP | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | SO-14/Tape \& Reel Plastic DIP | 2500 Units/Tape \& Reel 25 Units/Rail |

## MARKING DIAGRAMS



PDIP-14
P SUFFIX
CASE 646


| SO-14 | SO-14 |
| :---: | :---: |
| D SUFFIX | VD SUFFIX |
| CASE 751A | CASE 751A |
| 14 | 14 |
|  |  |
| MC33174D AWLYWW | MC33174VD |
| \# \\| \| \| \| |  |
| 1 | 1 |

TSSOP-14 DTB SUFFIX CASE 948G

14


| X | $=1$ or 2 |
| :--- | :--- |
| A | $=$ Assembly Location |
| WL, L | $=$ Wafer Lot |
| YY, Y | $=$ Year |
| WW, W | $=$ Work Week |

## MC33178, MC33179

## Low Power, Low Noise Operational Amplifiers

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only $420 \mu \mathrm{~A}$ of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance, symmetrical source and sink AC frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range, and are available in DIP and SOIC packages.

- $600 \Omega$ Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: $2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- Low Total Harmonic Distortion: 0.0024\%
(@ 1.0 kHz w/600 $\Omega$ Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/ $\mu \mathrm{s}$
- Dual Supply Operation: $\pm 2.0 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Performance


Figure 1. Representative Schematic Diagram (Each Amplifier)


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33178D | SO-8 | 98 Units/Rail |
| MC33178DR2 | SO-8 | 2500 Tape \& Reel |
| MC33178P | PDIP-8 | 50 Units/Rail |
| MC33179D | SO-14 | 55 Units/Rail |
| MC33179DR2 | SO-14 | 2500 Tape \& Reel |
| MC33179P | PDIP-14 | 25 Units/Rail |

## MC33178, MC33179

## PIN CONNECTIONS

DUAL
CASE 626/751

(Top View)

QUAD
CASE 646/751A

(Top View)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (VCC to $\left.\mathrm{V}_{\mathrm{EE}}\right)$ | $\mathrm{V}_{\mathrm{S}}$ | +36 | V |
| Input Differential Voltage Range | $\mathrm{V}_{\mathrm{IDR}}$ | Note 1 | V |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | Note 1 | V |
| Output Short Circuit Duration (Note 2) | $\mathrm{tsC}_{\mathrm{SC}}$ | Indefinite | sec |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{stg}}$ | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Note 2 | mW |

1. Either or both input voltages should not exceed $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$.
2. Power dissipation must be considered to ensure maximum junction temperature $\left(T_{J}\right)$ is not exceeded. (See power dissipation performance characteristic, Figure 2.)

DC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage }\left(\mathrm{R}_{\mathrm{S}}=50 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\mathrm{CC}}=+2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 3 | $\left\|\mathrm{V}_{10}\right\|$ |  |  | $\begin{aligned} & 3.0 \\ & 4.0 \end{aligned}$ | mV |
| Average Temperature Coefficient of Input Offset Voltage $\begin{aligned} & \left(\mathrm{R}_{\mathrm{S}}=50 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 3 | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 2.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Bias Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 4, 5 | $I_{B}$ | - | 100 | $\begin{aligned} & 500 \\ & 600 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Offset Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ |  | $\left\|l_{10}\right\|$ | - | 5.0 | $\begin{aligned} & 50 \\ & 60 \end{aligned}$ | nA |
| Common Mode Input Voltage Range $\left(\Delta \mathrm{V}_{1 \mathrm{O}}=5.0 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right)$ | 6 | $V_{\text {ICR }}$ | $-13$ | $\begin{aligned} & -14 \\ & \hline 14 \end{aligned}$ | $+13$ | V |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{O}}=-10 \mathrm{~V} \text { to }+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=600 \Omega\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 7, 8 | Avol | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 200 |  | kV/V |
| $\begin{aligned} & \hline \text { Output Voltage Swing }\left(\mathrm{V}_{\mathrm{ID}}= \pm 1.0 \mathrm{~V}\right) \\ &\left(\mathrm{V}_{\mathrm{CC}}\right.\left.=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}\right) \\ & R_{\mathrm{L}}=300 \Omega \\ & \mathrm{R}_{\mathrm{L}}=300 \Omega \\ & R_{\mathrm{L}}=600 \Omega \\ & R_{\mathrm{L}}=600 \Omega \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ &\left(\mathrm{~V}_{\mathrm{CC}}\right.\left.=+2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V}\right) \\ & R_{\mathrm{L}}=600 \Omega \\ & \mathrm{R}_{\mathrm{L}}=600 \Omega \end{aligned}$ | 9, 10, 11 | $\mathrm{V}_{\mathrm{O}}+$ <br> $\mathrm{V}_{\mathrm{O}}$ <br> $\mathrm{V}_{\mathrm{O}}+$ <br> $\mathrm{V}_{\mathrm{O}}$ <br> $\mathrm{V}_{\mathrm{O}^{+}}$ <br> $\mathrm{V}_{\mathrm{O}}$ <br> $\mathrm{V}_{\mathrm{O}}+$ <br> $\mathrm{V}_{\mathrm{O}}$ | $\begin{gathered} - \\ +12 \\ - \\ +13 \\ - \\ 1.1 \end{gathered}$ | $\begin{gathered} +12 \\ -12 \\ +13.6 \\ -13 \\ +14 \\ -13.8 \\ 1.6 \\ -1.6 \end{gathered}$ | $\begin{gathered} - \\ - \\ -12 \\ - \\ -13 \\ - \\ -1.1 \end{gathered}$ | V |
| Common Mode Rejection ( $\mathrm{V}_{\text {in }}= \pm 13 \mathrm{~V}$ ) | 12 | CMR | 80 | 110 | - | dB |
| Power Supply Rejection $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=+15 \mathrm{~V} /-15 \mathrm{~V},+5.0 \mathrm{~V} /-15 \mathrm{~V},+15 \mathrm{~V} /-5.0 \mathrm{~V}$ | 13 | PSR | 80 | 110 | - | dB |
| ```Output Short Circuit Current (VID = \pm1.0 V , Output to Ground) Source (VCC = 2.5 V to 15 V) Sink (VEE = -2.5 V to -15 V)``` | 14, 15 | Isc | $\begin{aligned} & +50 \\ & -50 \end{aligned}$ | $\begin{gathered} +80 \\ -100 \end{gathered}$ |  | mA |
| $\begin{aligned} & \text { Power Supply Current }\left(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-2.5 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}\right) \\ & \mathrm{MC}_{23178} \text { (Dual) } \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \\ & \mathrm{MC} 33199(\text { Quad })_{\mathrm{T}_{\mathrm{A}}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 16 | ID | - - - - | 1.7 | $\begin{aligned} & 1.4 \\ & 1.6 \\ & 2.4 \\ & 2.6 \end{aligned}$ | mA |

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate $\left(\mathrm{V}_{\text {in }}=-10 \mathrm{~V} \text { to }+10 \mathrm{~V}, R_{\mathrm{L}}=2.0 \mathrm{k} \Omega, C_{L}=100 \mathrm{pF}, \mathrm{~A}_{\mathrm{V}}=+1.0 \mathrm{~V}\right)$ | 17, 32 | SR | 1.2 | 2.0 | - | V/us |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | 18 | GBW | 2.5 | 5.0 | - | MHz |
| AC Voltage Gain ( $\mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{f}=20 \mathrm{kHz}$ ) | 19, 20 | $A_{\text {Vo }}$ | - | 50 | - | dB |
| Unity Gain Bandwidth (Open-Loop) ( $\mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) |  | BW | - | 3.0 | - | MHz |
| Gain Margin ( $\left.\mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}\right)$ | 21, 23, 24 | $\mathrm{A}_{\mathrm{m}}$ | - | 15 | - | dB |
| Phase Margin ( $\mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) | 22, 23, 24 | $\phi_{\mathrm{m}}$ | - | 60 | - | Deg |
| Channel Separation ( $\mathrm{f}=100 \mathrm{~Hz}$ to 20 kHz ) | 25 | CS | - | -120 | - | dB |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=20 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=600 \Omega, \mathrm{THD} \leq 1.0 \%$ ) |  | $\mathrm{BW}_{\mathrm{p}}$ | - | 32 | - | kHz |
| $\begin{aligned} & \text { Total Harmonic Distortion }\left(\mathrm{R}_{\mathrm{L}}=600 \Omega,, \mathrm{~V}_{\mathrm{O}}=2.0 \mathrm{~V}_{\mathrm{pp}}, \mathrm{~A}_{\mathrm{V}}=+1.0 \mathrm{~V}\right) \\ & \begin{array}{l} (\mathrm{f}=1.0 \mathrm{kHz}) \\ (\mathrm{f}=10 \mathrm{kHz}) \\ (\mathrm{f}=20 \mathrm{kHz}) \end{array} \end{aligned}$ | 26 | THD | $\begin{aligned} & - \\ & - \end{aligned}$ | $\begin{gathered} 0.0024 \\ 0.014 \\ 0.024 \end{gathered}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | \% |
| Open Loop Output Impedance $\left(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{f}=3.0 \mathrm{MHz}, \mathrm{~A}_{\mathrm{V}}=10 \mathrm{~V}\right)$ | 27 | $\left\|\mathrm{Z}_{\mathrm{O}}\right\|$ | - | 150 | - | $\Omega$ |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) |  | $\mathrm{R}_{\text {in }}$ | - | 200 | - | $k \Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) |  | $\mathrm{C}_{\text {in }}$ | - | 10 | - | pF |
| $\begin{aligned} & \text { Equivalent Input Noise Voltage }\left(R_{S}=100 \Omega,\right) \\ & f=10 \mathrm{~Hz} \\ & f=1.0 \mathrm{kHz} \end{aligned}$ | 28 | $e_{n}$ | - | $\begin{aligned} & 8.0 \\ & 7.5 \end{aligned}$ | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Equivalent Input Noise Current $\begin{aligned} & f=10 \mathrm{~Hz} \\ & \mathrm{f}=1.0 \mathrm{kHz} \end{aligned}$ | 29 | $\mathrm{i}_{\mathrm{n}}$ | - | $\begin{aligned} & 0.33 \\ & 0.15 \end{aligned}$ | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |



Figure 2. Maximum Power Dissipation versus Temperature


Figure 3. Input Offset Voltage versus Temperature for 3 Typical Units


Figure 4. Input Bias Current versus Common Mode Voltage


Figure 6. Input Common Mode Voltage Range versus Temperature


Figure 5. Input Bias Current versus Temperature


Figure 7. Open Loop Voltage Gain versus Temperature


Figure 8. Voltage Gain and Phase versus Frequency


Figure 9. Output Voltage Swing versus Supply Voltage


Figure 10. Output Saturation Voltage versus Load Current


Figure 12. Common Mode Rejection versus Frequency Over Temperature


Figure 14. Output Short Circuit Current versus Output Voltage


Figure 11. Output Voltage versus Frequency


Figure 13. Power Supply Rejection versus Frequency Over Temperature


Figure 15. Output Short Circuit Current versus Temperature


Figure 16. Supply Current versus Supply Voltage with No Load


Figure 18. Gain Bandwidth Product versus Temperature


Figure 20. Voltage Gain and Phase versus Frequency


Figure 17. Normalized Slew Rate versus Temperature


Figure 19. Voltage Gain and Phase versus Frequency


Figure 21. Open Loop Gain Margin versus Temperature


Figure 22. Phase Margin versus Temperature


Figure 24. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance


Figure 26. Total Harmonic Distortion versus Frequency


Figure 23. Phase Margin and Gain Margin versus Differential Source Resistance


Figure 25. Channel Separation versus Frequency


Figure 27. Output Impedance versus Frequency


Figure 28. Input Referred Noise Voltage versus Frequency


Figure 30. Percent Overshoot versus Load Capacitance

t , TIME ( $2.0 \mathrm{~ns} /$ DIV)
Figure 32. Small Signal Transient Response


Figure 29. Input Referred Noise Current versus Frequency

t , TIME ( $2.0 \mu \mathrm{~s} / \mathrm{DIV})$

Figure 31. Non-inverting Amplifier Slew Rate

t , TIME ( $5.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 33. Large Signal Transient Response


Figure 34. Telephone Line Interface Circuit

## APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its $60^{\circ}$ phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 24). The ability to drive a minimum $600 \Omega$ load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 34 both A2 and A3 are driving equivalent loads of approximately $600 \Omega$.

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection of 110 dB . This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion, is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the

MC33179 (quad op amp). Shorting more than one amplifier could easily exceed the junction temperature to the extent of causing permanent damage.

## Stability

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source of resistance is used ( $\mathrm{R} 1>1.0 \mathrm{k} \Omega$ ), a compensation capacitor equal to or greater than the input capacitance of the op amp ( 10 pF ) placed across the feedback resistor (see Figure 35) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance, it is important to choose the optimum value for that capacitor. This can be determined by the following Equation:

$$
\begin{equation*}
\mathrm{C}_{\mathrm{C}}=(1+[\mathrm{R} 1 / \mathrm{R} 2])^{2} \times \mathrm{C}_{\mathrm{L}}\left(\mathrm{Z}_{\mathrm{O}} / \mathrm{R}_{2}\right) \tag{1}
\end{equation*}
$$

where: $Z_{O}$ is the output impedance of the op amp.

For moderately high capacitive loads ( $500 \mathrm{pF}<\mathrm{C}_{\mathrm{L}}$ $<1500 \mathrm{pF}$ ) the addition of a compensation resistor on the order of $20 \Omega$ between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 36). For high capacitive loads ( $\mathrm{C}_{\mathrm{L}}>1500 \mathrm{pF}$ ), a combined compensation scheme should be used (see Figure 37). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of $\mathrm{C}_{\mathrm{C}}$ can be calculated using Equation (1). The Equation to calculate $\mathrm{R}_{\mathrm{C}}$ is as follows:

$$
\begin{equation*}
\mathrm{R}_{\mathrm{C}}=\mathrm{ZO} \times \mathrm{R} 1 / \mathrm{R} 2 \tag{2}
\end{equation*}
$$



Figure 36. Compensation Circuit for Moderate Capacitive Loads


Figure 37. Compensation Circuit for High Capacitive Loads

## LM324, LM324A, LM224, LM2902, LM2902V, NCV2902

## Quad Differential Input, Low Power Operational Amplifiers

The LM324 series are low-cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V (LM224, LM324, LM324A)
- Low Input Bias Currents: 100 nA Maximum (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation

MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | $\begin{aligned} & \hline \text { LM224 } \\ & \text { LM324, } \\ & \text { LM324A } \end{aligned}$ | LM2902, LM2902V | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltages Single Supply Split Supplies | $\begin{gathered} \mathrm{v}_{\mathrm{CC}} \\ \mathrm{v}_{\mathrm{CC}}, \mathrm{v}_{\mathrm{EE}} \end{gathered}$ | $\begin{gathered} 32 \\ \pm 16 \end{gathered}$ | $\begin{gathered} 26 \\ \pm 13 \end{gathered}$ | Vdc |
| Input Differential Voltage Range (Note 1) | $V_{\text {IDR }}$ | $\pm 32$ | $\pm 26$ | Vdc |
| Input Common Mode Voltage Range | VICR | -0.3 to 32 | -0.3 to 26 | Vdc |
| Output Short Circuit Duration | ${ }_{\text {tsc }}$ | Continuous |  |  |
| Junction Temperature | $\mathrm{T}_{J}$ | 150 |  | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 |  | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\text {A }}$ |  |  | ${ }^{\circ} \mathrm{C}$ |
| LM224 |  | -25 to +85 |  |  |
| LM324, 324A |  | 0 to +70 |  |  |
| LM2902 |  |  | -40 to +105 |  |
| LM2902V, NCV2902 |  |  | -40 to +125 |  |

[^37]This document contains information on a new product. Specifications and information herein are subject to change without notice.


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## PIN CONNECTIONS


(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2565 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2566 of this data sheet.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

2. LM 224 : $\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$

LM324/LM324A: $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
LM2902: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}$
LM2902V: $T_{\text {low }}=-40^{\circ} \mathrm{C}$, $T_{\text {high }}=+125^{\circ} \mathrm{C}$
NCV2902: $T_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
3. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common mode voltage range is $\mathrm{V}_{\mathrm{Cc}}-1.7 \mathrm{~V}$.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | LM224 |  |  | LM324A |  |  | LM324 |  |  | LM2902 |  |  | LM2902V |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Output VoltageHigh Limit ( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high to }} \mathrm{T}_{\text {low }}$ ) (Note 5) | $\mathrm{V}_{\mathrm{OH}}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | V |
| $\begin{gathered} \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}= \\ 2.0 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ |  | $3.3$ | 3.5 | - | 3.3 | 3.5 | - | 3.3 | 3.5 | - | 3.3 | 3.5 | - | 3.3 | 3.5 | - |  |
| $\begin{aligned} & V_{C C}=30 \mathrm{~V} \\ & (26 \mathrm{~V} \text { for } \mathrm{LM} 2902, \mathrm{~V}), \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \end{aligned}$ |  | 26 |  | - | $26$ | - | - | $26$ | - | - | 22 | - | - | $22$ | - | - |  |
| $\begin{aligned} & V_{\mathrm{CC}}=30 \mathrm{~V} \\ & (26 \mathrm{~V} \text { for } \mathrm{LM} 2902, \mathrm{~V}), \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{aligned}$ |  | 27 | 28 | - | 27 | 28 | - | 27 | 28 | - | 23 | 24 | - | 23 | 24 | - |  |
| Output Voltage Low Limit, $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }} \\ & (\text { Note 5) } \end{aligned}$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 5.0 | 20 | - | 5.0 | 20 | - | 5.0 | 20 | - | 5.0 | 100 | - | 5.0 | 100 | mV |
| Output Source Current $\begin{aligned} & \left(\mathrm{V}_{\mathrm{ID}}=+1.0 \mathrm{~V},\right. \\ & \left.\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ $T_{A}=T_{\text {high }} \text { to } T_{\text {low }}$ <br> (Note 5) | $\mathrm{l}+$ | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \end{aligned}$ | - | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \end{aligned}$ | - | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \end{aligned}$ | - | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { _ } \end{aligned}$ | $\begin{aligned} & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 40 \\ & 20 \end{aligned}$ | - | mA |
| Output Sink Current $\begin{gathered} \left(\mathrm{V}_{\mathrm{ID}}=-1.0 \mathrm{~V}\right. \\ \left.\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{gathered}$ | $\mathrm{l}-$ | 10 | $20$ | - | $10$ | $20$ | - | $10$ | 20 | - | $10$ | 20 | - | 10 | 20 | - | mA |
| $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }}$ <br> (Note 5) |  | 5.0 | 8.0 | - | 5.0 | 8.0 | - | 5.0 | 8.0 | - | 5.0 | 8.0 | - | 5.0 | 8.0 | - |  |
| $\begin{aligned} & \left(\mathrm{V}_{\mathrm{ID}}=-1.0 \mathrm{~V}\right. \\ & \mathrm{V}_{\mathrm{O}}=200 \mathrm{mV}, \\ & \left.\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \end{aligned}$ |  | 12 | 50 | - |  | 50 | - |  | 50 | - |  | - | - | - | - | - | $\mu \mathrm{A}$ |
| Output Short Circuit to Ground (Note 6) | ISC | - | 40 | 60 | - | 40 | 60 | - | 40 | 60 | - | 40 | 60 | - | 40 | 60 | mA |
| Power Supply Current ( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ ) <br> (Note 5) | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | mA |
| $\begin{aligned} & V_{C C}=30 \mathrm{~V} \\ & (26 \mathrm{~V} \text { for } \mathrm{LM} 2902, \mathrm{~V}), \\ & \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty \end{aligned}$ |  | - | - | $3.0$ | - | 1.4 | 3.0 | - | - | 3.0 | - | - | 3.0 | - | - | 3.0 |  |
| $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =5.0 \mathrm{~V}, \\ \mathrm{~V}_{\mathrm{O}} & =0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty \end{aligned}$ |  | - | - | 1.2 | - | 0.7 | 1.2 | - | - | 1.2 | - | - | 1.2 | - | - | 1.2 |  |

5. $\mathrm{LM} 224: \mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$

LM324/LM324A: $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
LM2902: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}$
LM2902V: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}$, $T_{\text {high }}=+125^{\circ} \mathrm{C}$
NCV2902: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
6. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common mode voltage range is $\mathrm{V}_{\mathrm{CC}}-1.7 \mathrm{~V}$.

## LM324, LM324A, LM224, LM2902, LM2902V, NCV2902



Figure 1. Representative Circuit Diagram (One-Fourth of Circuit Shown)

## CIRCUIT DESCRIPTION

The LM324 series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF ) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.


Single Supply


Figure 2. Large Signal Voltage Follower Response
Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.


Split Supplies

Figure 3.


Figure 4. Input Voltage Range


Figure 6. Large-Signal Frequency Response


Figure 8. Power Supply Current versus Power Supply Voltage


Figure 5. Open Loop Frequency


Figure 7. Small-Signal Voltage Follower Pulse Response (Noninverting)


Figure 9. Input Bias Current versus Power Supply Voltage

## LM324, LM324A, LM224, LM2902, LM2902V, NCV2902



$$
v_{0}=2.5 \mathrm{~V}\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right)
$$

Figure 10. Voltage Reference


Figure 11. Wien Bridge Oscillator


Figure 12. High Impedance Differential Amplifier


Figure 13. Comparator with Hysteresis


Figure 14. Bi-Quad Filter

## LM324, LM324A, LM224, LM2902, LM2902V, NCV2902



Figure 15. Function Generator


Figure 16. Multiple Feedback Bandpass Filter

Given: $f_{0}=$ center frequency
$A\left(f_{0}\right)=$ gain at center frequency
Choose value $\mathrm{f}_{0}, \mathrm{C}$
Then: $\quad R 3=\frac{Q}{\pi f_{0} C}$

$$
\mathrm{R} 1=\frac{\mathrm{R} 3}{2 \mathrm{~A}\left(\mathrm{f}_{0}\right)}
$$

$$
R 2=\frac{R 1 R 3}{4 Q^{2} R 1-R 3}
$$

For less than 10\% error from operational amplifier, $\frac{Q_{0} f_{0}}{B W}<0.1$
where $\mathrm{f}_{0}$ and BW are expressed in Hz .
If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

## LM324, LM324A, LM224, LM2902, LM2902V, NCV2902

ORDERING INFORMATION

| Device | Package | Operating Temperature Range | Shipping |
| :---: | :---: | :---: | :---: |
| LM224D | SO-14 | $-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ | 55 Units/Rail |
| LM224DR2 | SO-14 |  | 2500 Tape \& Reel |
| LM224N | PDIP-14 |  | 25 Units/Rail |
| LM324D | SO-14 | $0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | 55 Units/Rail |
| LM324DR2 | SO-14 |  | 2500 Tape \& Reel |
| LM324N | PDIP-14 |  | 25 Units/Rail |
| LM324AD | SO-14 |  | 55 Units/Rail |
| LM324ADR2 | SO-14 |  | 2500 Tape \& Reel |
| LM324AN | PDIP-14 |  | 25 Units/Rail |
| LM2902D | SO-14 | $-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | 55 Units/Rail |
| LM2902DR2 | SO-14 |  | 2500 Tape \& Reel |
| LM2902N | PDIP-14 |  | 25 Units/Rail |
| LM2902VD | SO-14 | $-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 55 Units/Rail |
| LM2902VDR2 | SO-14 |  | 2500 Tape \& Reel |
| LM2902VN | PDIP-14 |  | 25 Units/Rail |
| NCV2902DR2 | SO-14 |  | 2500 Tape \& Reel |

## LM324, LM324A, LM224, LM2902, LM2902V, NCV2902

MARKING DIAGRAMS

$$
\begin{aligned}
& \text { PDIP-14 } \\
& \text { N SUFFIX } \\
& \text { CASE } 646
\end{aligned}
$$



## LM358, LM258, LM2904, LM2904A, LM2904V, NCV2904

## Single Supply Dual Operational Amplifiers

Utilizing the circuit designs perfected for Quad Operational Amplifiers, these dual operational amplifiers feature low power drain, a common mode input voltage range extending to ground $/ \mathrm{V}_{\mathrm{EE}}$, and single supply or split supply operation. The LM358 series is equivalent to one-half of an LM324.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V , with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V (LM258/LM358)

$$
3.0 \mathrm{~V} \text { to } 26 \mathrm{~V}(\mathrm{LM} 2904, \mathrm{~A}, \mathrm{~V})
$$

- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation



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ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 2576 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2577 of this data sheet.


Figure 1.


Figure 2. Representative Schematic Diagram
(One-Half of Circuit Shown)

MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | $\begin{aligned} & \text { LM258 } \\ & \text { LM358 } \end{aligned}$ | LM2904, LM2904A LM2904V, NCV2904 | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltages Single Supply Split Supplies | $\begin{gathered} \mathrm{v}_{\mathrm{CC}} \\ \mathrm{v}_{\mathrm{CC}}, \mathrm{~V}_{\mathrm{EE}} \end{gathered}$ | $\begin{gathered} 32 \\ \pm 16 \end{gathered}$ | $\begin{gathered} 26 \\ \pm 13 \end{gathered}$ | Vdc |
| Input Differential Voltage Range (Note 1) | $\mathrm{V}_{\text {IDR }}$ | $\pm 32$ | $\pm 26$ | Vdc |
| Input Common Mode Voltage Range (Note 2) | $\mathrm{V}_{\text {ICR }}$ | -0.3 to 32 | -0.3 to 26 | Vdc |
| Output Short Circuit Duration | tsc | Continuous |  |  |
| Junction Temperature | $\mathrm{T}_{J}$ | 150 |  | ${ }^{\circ} \mathrm{C}$ |
| Thermal Resistance, Junction-to-Air (Note 3) | $\mathrm{R}_{\text {өJA }}$ | 238 |  | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 |  | ${ }^{\circ} \mathrm{C}$ |
| ESD Tolerance - Human Body Model (Note 4) | - | 2000 |  | V |
| ```Operating Ambient Temperature Range LM258 LM358 LM2904/LM2904A LM2904V, NCV2904``` | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} -25 \text { to }+85 \\ 0 \text { to }+70 \\ - \\ - \end{gathered}$ | $\begin{gathered} - \\ - \\ -40 \text { to }+105 \\ -40 \text { to }+125 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |

1. Split Power Supplies.
2. For Supply Voltages less than 32 V for the LM $258 / 358$ and 26 V for the LM2904, $\mathrm{A}, \mathrm{V}$, the absolute maximum input voltage is equal to the supply voltage.
R QJJ for Case 846A.
3. ESD data available upon request.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | LM258 |  |  | LM358 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Input Offset Voltage } \\ & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \text { to } 30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}), \\ & \mathrm{V}_{\mathrm{IC}}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{CC}}-1.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}} \simeq 1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=0 \Omega \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { (Note 5) } \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { (Note 5) } \end{aligned}$ | $\mathrm{V}_{10}$ | - | $2.0$ | $\begin{aligned} & 5.0 \\ & 7.0 \\ & 2.0 \end{aligned}$ | - | 2.0 - | $\begin{aligned} & 7.0 \\ & 9.0 \\ & 9.0 \end{aligned}$ | mV |
| Average Temperature Coefficient of Input Offset Voltage $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }}(\text { Note 5) }$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 7.0 | - | - | 7.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Offset Current <br> $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ (Note 5) Input Bias Current $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ (Note 5) | $\mathrm{I}_{\mathrm{I}}$ $I_{B}$ |  | $\begin{gathered} 3.0 \\ - \\ -45 \\ -50 \end{gathered}$ | $\begin{gathered} \hline 30 \\ 100 \\ -150 \\ -300 \end{gathered}$ | - - - - | $\begin{gathered} 5.0 \\ - \\ -45 \\ -50 \end{gathered}$ | $\begin{gathered} 50 \\ 150 \\ -250 \\ -500 \end{gathered}$ | nA |
| Average Temperature Coefficient of Input Offset Current $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }}(\text { Note 5) }$ | $\Delta l_{10} / \Delta \mathrm{T}$ | - | 10 | - | - | 10 | - | $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Common Mode Voltage Range (Note 6), } \\ & V_{C C}=30 \mathrm{~V} \\ & (26 \mathrm{~V} \text { for } \mathrm{LM} 2904, \mathrm{~V}) \\ & \mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}), \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }} \\ & \hline \end{aligned}$ | VICR | 0 <br> 0 |  | $28.3$ $28$ | $0$ | - - | $\begin{gathered} 28.3 \\ 28 \end{gathered}$ | V |
| Differential Input Voltage Range | $\mathrm{V}_{\text {IDR }}$ | - | - | $\mathrm{V}_{\mathrm{cc}}$ | - | - | $\mathrm{V}_{\mathrm{cc}}$ | V |
| $\begin{aligned} & \text { Large Signal Open Loop Voltage Gain } \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V} \text {, For Large } \mathrm{V}_{\mathrm{O}} \text { Swing, } \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }}(\text { Note } 5) \\ & \hline \end{aligned}$ | $A_{\text {VOL }}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ |  | - | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ |  | - | $\mathrm{V} / \mathrm{mV}$ |
| Channel Separation <br> $1.0 \mathrm{kHz} \leq \mathrm{f} \leq 20 \mathrm{kHz}$, Input Referenced | CS | - | -120 | - | - | -120 | - | dB |
| Common Mode Rejection $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ | CMR | 70 | 85 | - | 65 | 70 | - | dB |
| Power Supply Rejection | PSR | 65 | 100 | - | 65 | 100 | - | dB |
| $\begin{aligned} & \text { Output Voltage-High Limit } \\ & T_{A}=T_{\text {high }} \text { to } \mathrm{T}_{\text {low }}(\text { Note } 5) \\ & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for } \mathrm{LM} 2904, \mathrm{~V}), \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for } \mathrm{LM} 2904, \mathrm{~V}), \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 3.3 \\ & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 3.5 \\ - \\ 28 \end{gathered}$ | - | $\begin{aligned} & 3.3 \\ & 26 \\ & 27 \end{aligned}$ | $\begin{gathered} 3.5 \\ - \\ 28 \end{gathered}$ | - | V |
| Output Voltage-Low Limit $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }} \text { (Note 5) } \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | 5.0 | 20 | - | 5.0 | 20 | mV |
| Output Source Current $\mathrm{V}_{\mathrm{ID}}=+1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}$ | $\mathrm{I}^{+}$ | 20 | 40 | - | 20 | 40 | - | mA |
| $\begin{aligned} & \text { Output Sink Current } \\ & \mathrm{V}_{I D}=-1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V} \\ & \mathrm{~V}_{I D}=-1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=200 \mathrm{mV} \end{aligned}$ | $\mathrm{I}_{0}$ | $\begin{aligned} & 10 \\ & 12 \end{aligned}$ | $\begin{aligned} & 20 \\ & 50 \end{aligned}$ | - | $\begin{aligned} & 10 \\ & 12 \end{aligned}$ |  | - | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Output Short Circuit to Ground (Note 7) | Isc | - | 40 | 60 | - | 40 | 60 | mA |
| $\begin{aligned} & \text { Power Supply Current } \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }} \text { (Note 5) } \\ & \mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for } \mathrm{LM} 2904, \mathrm{~V}), \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty \\ & \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty \end{aligned}$ | Icc | - | $\begin{aligned} & 1.5 \\ & 0.7 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 1.2 \\ & \hline \end{aligned}$ | - |  |  | mA |

5. LM258: $\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$

LM2904/LM2904A: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}$
LM358: $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
LM2904V: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
NCV2904: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
6. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common mode voltage range is $\mathrm{V}_{\mathrm{CC}}-1.7 \mathrm{~V}$.
7. Short circuits from the output to $\mathrm{V}_{\mathrm{CC}}$ can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | LM2904 |  |  | LM2904A |  |  | LM2904V, NCV2904 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Input Offset Voltage } \\ & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \text { to } 30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}), \\ & \mathrm{V}_{I C}=0 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{CC}}-1.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}} \simeq 1.4 \mathrm{~V}, \mathrm{R}_{\mathrm{S}}=0 \Omega \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { (Note 8) } \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low ( }} \text { (Note 8) } \end{aligned}$ | $\mathrm{V}_{10}$ |  | $2.0$ | $\begin{aligned} & 7.0 \\ & 10 \\ & 10 \end{aligned}$ | - | $2.0$ | $\begin{aligned} & 7.0 \\ & 10 \\ & 10 \end{aligned}$ | - | - | $\begin{aligned} & 13 \\ & 10 \end{aligned}$ | mV |
| Average Temperature Coefficient of Input Offset Voltage $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }}(\text { Note 8) }$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 7.0 | - | - | 7.0 | - | - | 7.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Offset Current <br> $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ (Note 8) Input Bias Current <br> $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ (Note 8) | $\mathrm{I}_{\mathrm{I}}$ $I_{B}$ | $\begin{aligned} & - \\ & - \\ & - \\ & \text { - } \end{aligned}$ | $\begin{gathered} \hline 5.0 \\ 45 \\ -45 \\ -50 \end{gathered}$ | $\begin{array}{\|c\|} \hline 50 \\ 200 \\ -250 \\ -500 \end{array}$ | - - - | $\begin{array}{\|c\|} \hline 5.0 \\ 45 \\ -45 \\ -50 \end{array}$ | $\begin{gathered} \hline 50 \\ 200 \\ -100 \\ -250 \end{gathered}$ | - - - - | $\begin{gathered} 5.0 \\ 45 \\ -45 \\ -50 \end{gathered}$ | $\begin{array}{\|c\|} \hline 50 \\ 200 \\ -250 \\ -500 \end{array}$ | nA |
| Average Temperature Coefficient of Input Offset Current $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }} \text { (Note 8) }$ | $\Delta l_{10} / \Delta T$ | - | 10 | - | - | 10 | - | - | 10 | - | $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Common Mode Voltage Range (Note 9), } \\ & \mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}) \\ & \mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}), \\ & \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }} \\ & \hline \end{aligned}$ | VICR | $0$ $0$ |  | $\begin{array}{\|c\|} \hline 24.3 \\ 24 \end{array}$ | $0$ $0$ |  | $\begin{gathered} 24.3 \\ 24 \end{gathered}$ | $0$ $0$ |  | $\begin{gathered} 24.3 \\ 24 \end{gathered}$ | V |
| Differential Input Voltage Range | $\mathrm{V}_{\text {IDR }}$ | - | - | $\mathrm{V}_{\mathrm{CC}}$ | - | - | $\mathrm{V}_{\text {CC }}$ | - | - | $\mathrm{V}_{\mathrm{CC}}$ | V |
| Large Signal Open Loop Voltage Gain $R_{L}=2.0 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$, For Large $\mathrm{V}_{\mathrm{O}}$ Swing, $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ (Note 8) | Avol | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 | - | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 | - | $\begin{aligned} & 25 \\ & 15 \end{aligned}$ | 100 | - | V/mV |
| Channel Separation <br> $1.0 \mathrm{kHz} \leq \mathrm{f} \leq 20 \mathrm{kHz}$, Input Referenced | CS | - | -120 | - | - | -120 | - | - | -120 | - | dB |
| Common Mode Rejection $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ | CMR | 50 | 70 | - | 50 | 70 | - | 50 | 70 | - | dB |
| Power Supply Rejection | PSR | 50 | 100 | - | 50 | 100 | - | 50 | 100 | - | dB |
| $\begin{aligned} & \text { Output Voltage-High Limit } \\ & T_{A}=T_{\text {high }} \text { to } \mathrm{T}_{\text {low }}(\text { Note } 8) \\ & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}), \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{~V}_{\mathrm{CC}}=30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}), \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 3.3 \\ & 22 \\ & 23 \end{aligned}$ | $\begin{gathered} 3.5 \\ - \\ 24 \end{gathered}$ | - | $\begin{aligned} & 3.3 \\ & 22 \\ & 23 \end{aligned}$ | $\begin{gathered} 3.5 \\ - \\ 24 \end{gathered}$ | - | $\begin{aligned} & 3.3 \\ & 22 \\ & 23 \end{aligned}$ | $\begin{gathered} 3.5 \\ - \\ 24 \end{gathered}$ | - | V |
| Output Voltage-Low Limit $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }}(\text { Note 8) } \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | 5.0 | 20 | - | 5.0 | 20 | - | 5.0 | 20 | mV |
| Output Source Current $\mathrm{V}_{\mathrm{ID}}=+1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}$ | $\mathrm{l}_{0}+$ | 20 | 40 | - | 20 | 40 | - | 20 | 40 | - | mA |
| $\begin{aligned} & \text { Output Sink Current } \\ & \mathrm{V}_{I D}=-1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V} \\ & \mathrm{~V}_{I D}=-1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=200 \mathrm{mV} \end{aligned}$ | $\mathrm{I}_{0}$ | 10 | 20 | - | 10 | 20 | - | 10 | 20 | - | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Output Short Circuit to Ground (Note 10) | Isc | - | 40 | 60 | - | 40 | 60 | - | 40 | 60 | mA |
| $\begin{aligned} & \text { Power Supply Current } \\ & T_{A}=T_{\text {high }} \text { to } T_{\text {low }} \text { (Note 8) } \\ & V_{C C}=30 \mathrm{~V}(26 \mathrm{~V} \text { for LM2904, } \mathrm{V}), \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \\ & R_{\mathrm{L}}=\infty \\ & \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty \end{aligned}$ | $\mathrm{I}_{\mathrm{CC}}$ | - | 1.5 0.7 | 3.0 1.2 | - | 1.5 0.7 | 3.0 1.2 | - | 1.5 0.7 | $\begin{aligned} & 3.0 \\ & 1.2 \end{aligned}$ | mA |

8. $\mathrm{LM} 258: \mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$
$\mathrm{LM} 2904 / \mathrm{M} 2904 \mathrm{~A}: \mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {hi }}$

LM358: $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
LM2904/LM2904A: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C} \quad \mathrm{LM} 2904 \mathrm{~V}: \mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
NCV2904: $T_{\text {low }}=-40^{\circ} \mathrm{C}, T_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
9. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common mode voltage range is $\mathrm{V}_{\mathrm{CC}}-1.7 \mathrm{~V}$.
10. Short circuits from the output to $\mathrm{V}_{\mathrm{CC}}$ can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

## CIRCUIT DESCRIPTION

The LM358 series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF ) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.


Figure 4. Input Voltage Range


Figure 3. Large Signal Voltage Follower Response


Figure 5. Large-Signal Open Loop Voltage Gain


Figure 6. Large-Signal Frequency Response


Figure 7. Small Signal Voltage Follower Pulse Response (Noninverting)


Figure 9. Input Bias Current versus Supply Voltage


$$
\mathrm{V}_{0}=2.5 \mathrm{~V}\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right)
$$

Figure 10. Voltage Reference


Figure 11. Wien Bridge Oscillator


$$
e_{0}=C(1+a+b)\left(e_{2}-e_{1}\right)
$$

Figure 12. High Impedance Differential Amplifier


Figure 13. Comparator with Hysteresis


Figure 14. Bi-Quad Filter


Figure 15. Function Generator


Given: $\quad f_{0}=$ center frequency
$A\left(f_{0}\right)=$ gain at center frequency
Choose value $f_{0}, C$

Then: $\quad R 3=\frac{Q}{\pi f_{0} C}$
$\mathrm{R} 1=\frac{\mathrm{R} 3}{2 \mathrm{~A}\left(\mathrm{f}_{0}\right)}$

$$
\mathrm{R} 2=\frac{\mathrm{R} 1 \mathrm{R} 3}{4 \mathrm{Q}^{2} \mathrm{R} 1-\mathrm{R} 3}
$$

For less than $10 \%$ error from operational amplifier. $\frac{Q_{0} f_{0}}{B W}<0.1$ Where $\mathrm{f}_{0}$ and BW are expressed in Hz .

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Figure 16. Multiple Feedback Bandpass Filter

LM358, LM258, LM2904, LM2904A, LM2904V, NCV2904
ORDERING INFORMATION

| Device | Package | Operating Temperature Range | Shipping |
| :---: | :---: | :---: | :---: |
| LM358D | SO-8 | $0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | 98 Units/Rail |
| LM358DR2 | SO-8 |  | 2500 Tape \& Reel |
| LM358DMR2 | Micro8 |  | 4000 Tape \& Reel |
| LM358N | PDIP-8 |  | 50 Units/Rail |
| LM258D | SO-8 | $-25^{\circ}$ to $+85^{\circ} \mathrm{C}$ | 98 Units/Rail |
| LM258DR2 | SO-8 |  | 2500 Tape \& Reel |
| LM258DMR2 | Micro8 |  | 4000 Tape \& Reel |
| LM258N | PDIP-8 |  | 50 Units/Rail |
| LM2904D | SO-8 | $-40^{\circ}$ to $+105^{\circ} \mathrm{C}$ | 98 Units/Rail |
| LM2904DR2 | SO-8 |  | 2500 Tape \& Reel |
| LM2904DMR2 | Micro8 |  | 2500 Tape \& Reel |
| LM2904N | PDIP-8 |  | 50 Units/Rail |
| LM2904ADMR2 | Micro8 |  | 4000 Tape \& Reel |
| LM2904AN | PDIP-8 |  | 50 Units/Rail |
| LM2904VD | SO-8 | $-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | 98 Units/Rail |
| LM2904VDR2 | SO-8 |  | 2500 Tape \& Reel |
| LM2904VDMR2 | Micro8 |  | 4000 Tape \& Reel |
| LM2904VN | PDIP-8 |  | 50 Units/Rail |
| NCV2904DR2 | SO-8 |  | 2500 Tape \& Reel |

MARKING DIAGRAMS

> PDIP-8 N SUFFIX CASE 626



SO-8 D SUFFIX
CASE 751

SO-8 VD SUFFIX CASE 751



*This marking diagram also applies to NCV2904.

## MC3403, MC3303

## Single Supply Quad Operational Amplifiers

The MC3403 is a low cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741C. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one third of those associated with the MC1741C (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: $\pm 1.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741C
- Industry Standard Pinouts
- ESD Diodes Added for Increased Ruggedness


MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltages <br> Single Supply <br> Split Supplies | $\mathrm{V}_{\mathrm{CC}}$ <br> $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{EE}}$ | 36 <br> $\pm 18$ | Vdc |
| Input Differential Voltage Range (Note 1) | $\mathrm{V}_{\text {IDR }}$ | $\pm 36$ | Vdc |
| Input Common Mode Voltage Range <br> (Notes 1 and 2) | $\mathrm{V}_{\text {ICR }}$ | $\pm 18$ | Vdc |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range <br> MC3303 <br> MC3403 | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 |  |
| Junction Temperature | ${ }^{\circ} \mathrm{C}$ |  |  |

1. Split power supplies.
2. For supply voltages less than $\pm 18 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.

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## PIN CONNECTIONS


(Top View)

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC3303D | SO-14 | 55 Units/Rail |
| MC3303DR2 | SO-14 | 2500 Tape \& Reel |
| MC3303P | PDIP-14 | 25 Units/Rail |
| MC3403D | SO-14 | 55 Units/Rail |
| MC3403DR2 | SO-14 | 2500 Tape \& Reel |
| MC3403P | PDIP-14 | 25 Units/Rail |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}\right.$ for MC3403; $\mathrm{V}_{\mathrm{CC}}=+14 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=$ Gnd for $\mathrm{MC} 3303 \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | MC3403 |  |  | MC3303 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage <br> $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ (Note 1) | $\mathrm{V}_{10}$ | - | $2.0$ | $\begin{aligned} & 10 \\ & 12 \end{aligned}$ | - | $2.0$ | $\begin{aligned} & \hline 8.0 \\ & 10 \end{aligned}$ | mV |
| Input Offset Current $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ | $1{ }_{10}$ | - | $30$ | $\begin{gathered} 50 \\ 200 \end{gathered}$ | - | $30$ | $\begin{gathered} 75 \\ 250 \end{gathered}$ | nA |
| Large Signal Open Loop Voltage Gain $\begin{aligned} & \mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {high }} \text { to } \mathrm{T}_{\text {low }} \end{aligned}$ | Avol | $\begin{aligned} & 20 \\ & 15 \end{aligned}$ | 200 | - | $\begin{aligned} & 20 \\ & 15 \end{aligned}$ | 200 | - | V/mV |
| Input Bias Current $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {high }}$ to $\mathrm{T}_{\text {low }}$ | IB | - | -200 - | $\begin{aligned} & \hline-500 \\ & -800 \end{aligned}$ | - | -200 | $\begin{gathered} \hline-500 \\ -1000 \\ \hline \end{gathered}$ | nA |
| Output Impedance f = 20 Hz | $\mathrm{z}_{0}$ | - | 75 | - | - | 75 | - | $\Omega$ |
| Input Impedance f = 20 Hz | $\mathrm{z}_{\mathrm{i}}$ | 0.3 | 1.0 | - | 0.3 | 1.0 | - | $\mathrm{M} \Omega$ |
| $\begin{aligned} & \text { Output Voltage Range } \\ & R_{L}=10 \mathrm{k} \Omega \\ & R_{L}=2.0 \mathrm{k} \Omega \\ & R_{L}=2.0 \mathrm{k} \Omega, T_{A}=T_{\text {high }} \text { to } T_{\text {low }} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & \pm 12 \\ & \pm 10 \\ & \pm 10 \end{aligned}$ | $\begin{gathered} \pm 13.5 \\ \pm 13 \end{gathered}$ | - | $\begin{aligned} & 12 \\ & 10 \\ & 10 \end{aligned}$ | $\begin{gathered} 12.5 \\ 12 \\ - \end{gathered}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | V |
| Input Common Mode Voltage Range | VICR | $\begin{aligned} & +13 \mathrm{~V} \\ & -V_{E E} \end{aligned}$ | $\begin{aligned} & +13 \mathrm{~V} \\ & -V_{E E} \end{aligned}$ | - | $\begin{aligned} & +12 \mathrm{~V} \\ & -\mathrm{V}_{\mathrm{EE}} \end{aligned}$ | $\begin{gathered} +12.5 \mathrm{~V} \\ -\mathrm{V}_{\mathrm{EE}} \end{gathered}$ | - | V |
| Common Mode Rejection $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega$ | CMR | 70 | 90 | - | 70 | 90 | - | dB |
| Power Supply Current ( $\mathrm{V}_{\mathrm{O}}=0$ ) $\mathrm{R}_{\mathrm{L}}=\infty$ | $\mathrm{I}_{\mathrm{CC}}, \mathrm{I}_{\mathrm{EE}}$ | - | 2.8 | 7.0 | - | 2.8 | 7.0 | mA |
| Individual Output Short-Circuit Current (Note 2) | Isc | $\pm 10$ | $\pm 20$ | $\pm 45$ | $\pm 10$ | $\pm 30$ | $\pm 45$ | mA |
| Positive Power Supply Rejection Ratio | PSRR+ | - | 30 | 150 | - | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| Negative Power Supply Rejection Ratio | PSRR- | - | 30 | 150 | - | 30 | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| ```Average Temperature Coefficient of Input Offset Current \(T_{A}=T_{\text {high }}\) to \(T_{\text {low }}\)``` | $\Delta l_{10} / \Delta T$ | - | 50 | - | - | 50 | - | $\mathrm{pA} /{ }^{\circ} \mathrm{C}$ |
| Average Temperature Coefficient of Input Offset Voltage $T_{A}=T_{\text {high }} \text { to } T_{\text {low }}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Power Bandwidth $A_{V}=1, R_{L}=10 \mathrm{k} \Omega, V_{O}=20 \mathrm{~V}(p-p), T H D=5 \%$ | BWp | - | 9.0 | - | - | 9.0 | - | kHz |
| Small-Signal Bandwidth $A_{V}=1, R_{L}=10 \mathrm{k} \Omega, V_{O}=50 \mathrm{mV}$ | BW | - | 1.0 | - | - | 1.0 | - | MHz |
| Slew Rate $\mathrm{A}_{\mathrm{V}}=1, \mathrm{~V}_{\mathrm{i}}=-10 \mathrm{~V}$ to +10 V | SR | - | 0.6 | - | - | 0.6 | - | V/us |
| Rise Time $A_{V}=1, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}=50 \mathrm{mV}$ | ${ }_{\text {t }}^{\text {LLH }}$ | - | 0.35 | - | - | 0.35 | - | $\mu \mathrm{s}$ |
| Fall Time $A_{V}=1, R_{L}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}=50 \mathrm{mV}$ | ${ }_{\text {t }}^{\text {th }}$ | - | 0.35 | - | - | 0.35 | - | $\mu \mathrm{s}$ |
| Overshoot $A_{V}=1, R_{L}=10 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}=50 \mathrm{mV}$ | os | - | 20 | - | - | 20 | - | \% |
| Phase Margin $\mathrm{A}_{\mathrm{V}}=1, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}=200 \mathrm{pF}$ | ¢m | - | 60 | - | - | 60 | - | Degrees |
| $\begin{aligned} & \text { Crossover Distortion } \\ & \qquad\left(\mathrm{V}_{\text {in }}=30 \mathrm{mVpp}, \mathrm{~V}_{\text {out }}=2.0 \mathrm{Vpp}, \mathrm{f}=10 \mathrm{kHz}\right) \end{aligned}$ | - | - | 1.0 | - | - | 1.0 | - | \% |

1. $\mathrm{MC} 3303: \mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$

MC3403: $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
2. Not to exceed maximum package power dissipation.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | MC3403 |  |  | MC3303 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage | $\mathrm{V}_{10}$ | - | 2.0 | 10 | - | - | 10 | mV |
| Input Offset Current | 1 I | - | 30 | 50 | - | - | 75 | nA |
| Input Bias Current | $\mathrm{I}_{1 B}$ | - | -200 | -500 | - | - | -500 | nA |
| Large Signal Open Loop Voltage Gain $\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$ | Avol | 10 | 200 | - | 10 | 200 | - | $\mathrm{V} / \mathrm{mV}$ |
| Power Supply Rejection Ratio | PSRR | - | - | 150 | - | - | 150 | $\mu \mathrm{V} / \mathrm{V}$ |
| $\begin{aligned} & \text { Output Voltage Range (Note 3) } \\ & R_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & R_{\mathrm{L}}=10 \mathrm{k} \Omega, 5.0 \leq \mathrm{V}_{\mathrm{CC}} \leq 30 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{OR}}$ | $\begin{gathered} 3.3 \\ \mathrm{v}_{\mathrm{CC}}-2.0 \end{gathered}$ | $\begin{gathered} 3.5 \\ \mathrm{v}_{\mathrm{CC}}-1.7 \end{gathered}$ | - | $\begin{gathered} 3.3 \\ \mathrm{v}_{\mathrm{CC}}-2.0 \end{gathered}$ | $\begin{gathered} 3.5 \\ \mathrm{v}_{\mathrm{CC}}-1.7 \end{gathered}$ |  | Vpp |
| Power Supply Current | Icc | - | 2.5 | 7.0 | - | 2.5 | 7.0 | mA |
| $\begin{aligned} & \text { Channel Separation } \\ & \mathrm{f}=1.0 \mathrm{kHz} \text { to } 20 \mathrm{kHz} \\ & \text { (Input Referenced) } \end{aligned}$ | CS | - | -120 | - | - | -120 | - | dB |

3. Output will swing to ground with a $10 \mathrm{k} \Omega$ pull down resistor.


Figure 1. Representative Schematic Diagram
( $1 / 4$ of Circuit Shown)

## CIRCUIT DESCRIPTION


$20 \mu s / D I V$
Figure 2. Inverter Pulse Response

The MC3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input device Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first
stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF ) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient, thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.


Figure 3. Sine Wave Response


Figure 4. Open Loop Frequency Response


Figure 5. Power Bandwidth


Figure 7. Input Bias Current versus Temperature


Figure 9. Voltage Reference


Figure 6. Output Swing versus Supply Voltage


Figure 8. Input Bias Current versus Supply Voltage


Figure 10. Wien Bridge Oscillator


Figure 11. High Impedance Differential Amplifier

$V_{\text {inL }}=\frac{R 1}{R 1+R 2}\left(V_{\text {OL }}-V_{\text {ref }}\right)+V_{\text {ref }}$

$V_{\text {inH }}=\frac{R 1}{R 1+R 2}\left(V_{\text {OH }}-V_{\text {ref }}\right)+V_{\text {ref }}$
$\mathrm{V}_{\mathrm{h}}=\frac{\mathrm{R} 1}{\mathrm{R} 1+\mathrm{R} 2}\left(\mathrm{~V}_{\mathrm{OH}}-\mathrm{V}_{\mathrm{OL}}\right)$

Figure 12. Comparator with Hysteresis


Figure 13. Bi-Quad Filter

$$
\mathrm{V}_{\text {ref }}=\frac{1}{2} \mathrm{~V}_{\mathrm{CC}}
$$



$$
f=\frac{R 1+R_{C}}{4 C R_{f} R 1} \text { if } R 3=\frac{R 2 R 1}{R 2+R 1}
$$

Figure 14. Function Generator


Choose value $f_{0}, C$

$$
\text { Then: } \quad R 3=\frac{Q}{\pi f_{0} C} \quad R 1=\frac{R 3}{2 A\left(f_{0}\right)} \quad R 2=\frac{R 1 R 5}{4 Q^{2} R 1-R 5}
$$

For less than $10 \%$ error from operational amplifier $\frac{\mathrm{O}_{0} f_{0}}{B W}<0.1$
where $f_{0}$ and $B W$ are expressed in Hz .

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Figure 15. Multiple Feedback Bandpass Filter

## LM301A, LM201A

## Non Compensated Single Operational Amplifiers

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to $10 \mathrm{~V} / \mu \mathrm{s}$ can be obtained.

- Low Input Offset Current: 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics


Figure 1. Standard Compensation and Offset Balancing Circuit



## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| LM301AD | SO-8 | 98 Units/Rail |
| LM301ADR2 | SO-8 | 2500 Tape \& Reel |
| LM301AN | PDIP-8 | 50 Units/Rail |
| LM201AD | SO-8 | 98 Units/Rail |
| LM201ADR2 | SO-8 | 2500 Tape \& Reel |
| LM201AN | PDIP-8 | 50 Units/Rail |

Figure 3. Representative Circuit Schematic

MAXIMUM RATINGS

| Rating | Symbol | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: |
|  |  | LM201A | LM301A |  |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC},} \mathrm{V}_{\mathrm{EE}}$ | $\pm 22$ | $\pm 18$ | Vdc |
| Input Differential Voltage | $V_{\text {ID }}$ | $\longleftarrow \sim$ |  | V |
| Input Common Mode Range (Note 1) | VICR | $\longleftrightarrow$ |  | V |
| Output Short Circuit Duration | $\mathrm{t}_{\text {Sc }}$ | $\longleftarrow$ Continuous $\longrightarrow$ |  |  |
| Power Dissipation (Package Limitation) Plastic Dual-In-Line Package Derate above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | $P_{\text {D }}$ | 625 625 <br> 5.0 5.0 |  | $\begin{gathered} \mathrm{mW} \\ \mathrm{~mW} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -25 to +85 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | $\longleftarrow$ - ${ }^{\text {e }}$ to $+150 \longrightarrow$ |  | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(T_{A}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from $\pm 5.0 \mathrm{~V}$ to $\pm 20 \mathrm{~V}$ for the LM201A, and from $\pm 5.0 \mathrm{~V}$ to $\pm 15 \mathrm{~V}$ for the LM301A.

| Characteristic | Symbol | LM201A |  |  | LM301A |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage ( $\mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega$ ) | $\mathrm{V}_{10}$ | - | 0.7 | 2.0 | - | 2.0 | 7.5 | mV |
| Input Offset Current | 1 IO | - | 1.5 | 10 | - | 3.0 | 50 | nA |
| Input Bias Current | $\mathrm{IIB}^{\text {a }}$ | - | 30 | 75 | - | 70 | 250 | nA |
| Input Resistance | $\mathrm{r}_{\mathrm{i}}$ | 1.5 | 4.0 | - | 0.5 | 2.0 | - | $\mathrm{M} \Omega$ |
| Supply Current $\begin{aligned} & \mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}= \pm 20 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}= \pm 15 \mathrm{~V} \end{aligned}$ | $\mathrm{I}_{\mathrm{CC}}, \mathrm{l}_{\mathrm{EE}}$ | - | 1.8 |  |  | $\begin{gathered} - \\ 1.8 \end{gathered}$ | $3.0$ | mA |
| Large Signal Voltage Gain $\left(\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}>2.0 \mathrm{k} \Omega\right)$ | $A_{V}$ | 50 | 160 | - | 25 | 160 | - | V/mV |

The following specifications apply over the operating temperature range.

| Input Offset Voltage ( $\mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega$ ) | $\mathrm{V}_{10}$ | - | - | 3.0 | - | - | 10 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Current | 10 | - | - | 20 | - | - | 70 | nA |
| Avg Temperature Coefficient of Input Offset Voltage (Note 2) $\mathrm{T}_{\mathrm{A}}(\min ) \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{A}}(\max )$ | $\Delta \mathrm{V}_{\mathrm{IO}} / \Delta \mathrm{T}$ | - | 3.0 | 15 | - | 6.0 | 30 | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Avg Temperature Coefficient of Input Offset Current (Note 2) $\begin{aligned} & +25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{A}}(\max ) \\ & \mathrm{T}_{\mathrm{A}}(\min ) \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C} \end{aligned}$ | $\Delta l_{10} / \Delta T$ |  |  |  |  |  | 0.3 0.6 | $\mathrm{nA} /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current | $I_{1 B}$ | - | - | 100 | - | - | 300 | nA |
| Large Signal Voltage Gain $\left(\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}= \pm 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}>2.0 \mathrm{k} \Omega\right)$ | Avol | 25 | - | - | 15 | - | - | V/mV |
| $\begin{aligned} & \text { Input Voltage Range } \\ & \mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}= \pm 20 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}= \pm 15 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {ICR }}$ | -15 | - | $+15$ | $\begin{gathered} - \\ -12 \end{gathered}$ |  | $\begin{gathered} - \\ +12 \end{gathered}$ | V |
| Common Mode Rejection ( $\mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega$ ) | CMR | 80 | 96 | - | 70 | 90 | - | dB |
| Supply Voltage Rejection ( $\mathrm{R}_{\mathrm{S}} \leq 50 \mathrm{k} \Omega$ ) | PSR | 80 | 96 | - | 70 | 96 | - | dB |
| Output Voltage Swing $\left(\mathrm{V}_{\mathrm{CC}} / V_{\mathrm{EE}}= \pm 15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}= \pm 10 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{L}}>2.0 \mathrm{k} \Omega\right)$ | $\mathrm{V}_{\mathrm{O}}$ | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | $\begin{aligned} & \pm 12 \\ & \pm 10 \end{aligned}$ | $\begin{aligned} & \pm 14 \\ & \pm 13 \end{aligned}$ |  | V |
| Supply Currents ( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\mathrm{A}}(\mathrm{max}), \mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}= \pm 20 \mathrm{~V}$ ) | $\mathrm{I}_{\mathrm{CC},} \mathrm{l}_{\text {EE }}$ | - | 1.2 | 2.5 | - | - | - | mA |

1. For supply voltages less than $\pm 15 \mathrm{~V}$, the absolute maximum input voltage is equal to the supply voltage.
2. Guaranteed by design.


Figure 4. Minimum Input Voltage Range


Figure 6. Minimum Voltage Gain


Figure 8. Open Loop Frequency Response


Figure 5. Minimum Output Voltage Swing


Figure 7. Typical Supply Currents


Figure 9. Large Signal Frequency Response

## LM301A, LM201A



Figure 10. Voltage Follower Pulse Response


Figure 12. Large Signal Frequency Response


Figure 14. Single-Pole Compensation


Figure 11. Open Loop Frequency Response


Figure 13. Inverter Pulse Response


Figure 15. Feedforward Compensation

## TCA0372, TCA0372B

### 1.0 A Output Current, Dual Power Operational Amplifiers

The TCA0372 is a monolithic circuit intended for use as a power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. No deadband crossover distortion provides better performance for driving coils.

- Output Current to 1.0 A
- Slew Rate of $1.3 \mathrm{~V} / \mu \mathrm{s}$
- Wide Bandwidth of 1.1 MHz
- Internal Thermal Shutdown
- Single or Split Supply Operation
- Excellent Gain and Phase Margins
- Common Mode Input Includes Ground
- Zero Deadband Crossover Distortion


Figure 1. Representative Block Diagram


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| TCA0372DW | SO-16W | 47 Units/Rail |
| TCA0372DWR2 | SO-16W | 1000 Tape \& Reel |
| TCA0372DP1 | PDIP-8 | 50 Units/Rail |
| TCA0372BDP1 | PDIP-8 | 50 Units/Rail |
| TCA0372DP2 | PDIP-16 | 25 Units/Rail |
| TCA0372DM2EL | SOEIAJ-16 | 2500 Tape \& Reel |

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2593 of this data sheet.

## TCA0372, TCA0372B

## PIN CONNECTIONS


*Pins 4 and 9 to 16 are internally connected.

CASE 626


CASE 751G

(Top View)

CASE 966

(Top View)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (from $\mathrm{V}_{\mathrm{CC}}$ to $\left.\mathrm{V}_{\mathrm{EE}}\right)$ | 40 | V |  |
| Input Differential Voltage Range | $\mathrm{V}_{\mathrm{S}}$ | Note 1 | V |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IDR}}$ | Note 1 | V |
| Junction Temperature (Note 2) | $\mathrm{V}_{\mathrm{IR}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| DC Output Current | $\mathrm{T}_{\mathrm{stg}}$ | 1.0 | A |
| Peak Output Current (Nonrepetitive) | $\mathrm{I}_{\mathrm{O}}$ | 1.5 | A |

1. Either or both input voltages should not exceed the magnitude of $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$.
2. Power dissipation must be considered to ensure maximum junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) is not exceeded.

DC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}\right.$ connected to ground, $\mathrm{T}_{\mathrm{J}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage }\left(\mathrm{V}_{\mathrm{CM}}=0\right) \\ & \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}, \mathrm{~T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{V}_{10}$ |  | 1.0 | $\begin{aligned} & 15 \\ & 20 \end{aligned}$ | mV |
| Average Temperature Coefficient of Offset Voltage | $\Delta \mathrm{V}_{\mathrm{IO}} / \Delta \mathrm{T}$ | - | 20 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current ( $\mathrm{V}_{\mathrm{CM}}=0$ ) | $\mathrm{I}_{\mathrm{B}}$ | - | 100 | 500 | nA |
| Input Offset Current ( $\mathrm{V}_{\mathrm{CM}}=0$ ) | ${ }_{10}$ | - | 10 | 50 | nA |
| Large Signal Voltage Gain $\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}$ | Avol | 30 | 100 | - | V/mV |
| $\begin{aligned} & \text { Output Voltage Swing ( } \left.\mathrm{L}_{\mathrm{L}}=100 \mathrm{~mA}\right) \\ & \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \\ & \mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $\begin{aligned} & 14.0 \\ & 13.9 \end{aligned}$ | $\begin{gathered} 14.2 \\ - \\ -14.2 \end{gathered}$ | $\begin{gathered} - \\ - \\ -14.0 \\ -13.9 \end{gathered}$ | V |
| $\begin{aligned} & \text { Output Voltage Swing ( } \left.\mathrm{I}_{\mathrm{L}}=1.0 \mathrm{~A}\right) \\ & \mathrm{V}_{\mathrm{CC}}=+24 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=+24 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{J}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \\ & \mathrm{V}_{\mathrm{CC}}=+24 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{J}=+25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=+24 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{J}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $\begin{array}{r} 22.5 \\ 22.5 \end{array}$ | $\begin{gathered} 22.7 \\ - \\ 1.3 \end{gathered}$ | $\begin{gathered} - \\ - \\ 1.5 \\ 1.5 \end{gathered}$ | V |
| Input Common Mode Voltage Range $\begin{aligned} & \mathrm{T}_{J}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $V_{\text {ICR }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{EE}} \text { to }\left(\mathrm{V}_{\mathrm{CC}}-1.0\right) \\ & \mathrm{V}_{\mathrm{EE}} \text { to }\left(\mathrm{V}_{\mathrm{CC}}-1.3\right) \end{aligned}$ |  |  | V |
| Common Mode Rejection Ratio ( $\mathrm{R}_{\mathrm{S}}=10 \mathrm{k}$ ) | CMRR | 70 | 90 | - | dB |
| Power Supply Rejection Ratio ( $\mathrm{R}_{\mathrm{S}}=100 \Omega$ ) | PSRR | 70 | 90 | - | dB |
| Power Supply Current  <br> $\mathrm{T}_{J}=+25^{\circ} \mathrm{C}$ TCA0372 <br>  TCA0372B <br> $\mathrm{T}_{J}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ TCA0372 <br>  TCA0372B | ID | - | 5.0 8.0 - | $\begin{aligned} & 10 \\ & 10 \\ & 14 \\ & 14 \end{aligned}$ | mA |

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}\right.$ connected to ground, $\mathrm{T}_{\mathrm{J}}=+25^{\circ} \mathrm{C}$, unless otherwise noted. )

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Slew Rate }\left(V_{\text {in }}=-10 \mathrm{~V} \text { to }+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}\right) \\ & \mathrm{A}_{\mathrm{V}}=-1.0, T_{J}=T_{\text {low }} \text { to } T_{\text {high }} \end{aligned}$ | SR | 1.0 | 1.4 | - | V/us |
| $\begin{aligned} & \text { Gain Bandwidth Product }\left(\mathrm{f}=100 \mathrm{kHz}, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}\right) \\ & \mathrm{T}_{J}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{J}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | GBW | $\begin{aligned} & 0.9 \\ & 0.7 \end{aligned}$ | $1.4$ | - | MHz |
| $\begin{aligned} & \text { Phase Margin } T_{J}=T_{\text {low }} \text { to } T_{\text {high }} \\ & R_{L}=2.0 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF} \end{aligned}$ | $\phi_{\mathrm{m}}$ | - | 65 | - | Degrees |
| Gain Margin $\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k}, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$ | $\mathrm{A}_{\mathrm{m}}$ | - | 15 | - | dB |
| Equivalent Input Noise Voltage $R_{S}=100 \Omega, f=1.0 \text { to } 100 \mathrm{kHz}$ | $\mathrm{e}_{\mathrm{n}}$ | - | 22 | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Total Harmonic Distortion $A_{V}=-1.0, R_{L}=50 \Omega, V_{O}=0.5 \mathrm{VRMS}, f=1.0 \mathrm{kHz}$ | THD | - | 0.02 | - | \% |

NOTE: In case $\mathrm{V}_{\mathrm{EE}}$ is disconnected before $\mathrm{V}_{\mathrm{CC}}$, a diode between $\mathrm{V}_{\mathrm{EE}}$ and Ground is recommended to avoid damaging the device.


Figure 2. Supply Current versus Suppy Voltage with No Load


Figure 4. Voltage Gain and Phase versus Frequency

t, TIME ( $1.0 \mu \mathrm{~s} / \mathrm{DIV}$ )
Figure 6. Small Signal Transient Response


Figure 3. Output Saturation Voltage versus Load Current


Figure 5. Phase Margin versus Output Load Capacitance


Figure 7. Large Signal Transient Response


Figure 8. Sine Wave Reponse


Figure 9. Bidirectional DC Motor Control with Microprocessor-Compatible Inputs


For circuit stability, ensure that $R_{x}>\frac{2 R 3 \cdot R 1}{R_{M}}$ where, $R_{M}=$ internal resistance of motor.
The voltage available at the terminals of the motor is: $V_{M}=2\left(V_{1}-\frac{V_{S}}{2}\right)+\left|R_{0}\right| \cdot I_{M}$
where, $\left|R_{0}\right|=\frac{2 R 3 \cdot R 1}{R_{X}}$ and $I_{M}$ is the motor current.
Figure 10. Bidirectional Speed Control of DC Motors

## TCA0372, TCA0372B

## MARKING DIAGRAMS

> PDIP-8
> DP1 SUFFIX
> CASE 626

PDIP-16 DP2 SUFFIX CASE 648

SO-16W DW SUFFIX CASE 751G

| TCA0372DW AWLYYWW - |
| :---: |

SOEIAJ-16 DM2 SUFFIX CASE 966

```
A = Assembly Location
WL, L = Wafer Lot
YY,Y = Year
WW,W = Work Week
```


## LM833

## Low Noise, Audio Dual Operational Amplifier

The LM833 is a standard low-cost monolithic dual general-purpose operational amplifier employing Bipolar technology with innovative high-performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise ( $4.5 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ ), 15 MHz gain bandwidth product, $7.0 \mathrm{~V} / \mu \mathrm{s}$ slew rate, 0.3 mV input offset voltage with $2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ temperature coefficient of input offset voltage. The LM833 output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

For an improved performance dual/quad version, see the MC33079 family.

- Low Voltage Noise: $4.5 \mathrm{nV} / \sqrt{\mathrm{Hz}}$
- High Gain Bandwidth Product: 15 MHz
- High Slew Rate: 7.0 V/ $\mu \mathrm{s}$
- Low Input Offset Voltage: 0.3 mV
- Low T.C. of Input Offset Voltage: $2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- Low Distortion: 0.002\%
- Excellent Frequency Stability
- Dual Supply Operation


## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (VCC to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | +36 | V |
| Input Differential Voltage Range <br> (Note 1) | $\mathrm{V}_{\mathrm{IDR}}$ | 30 | V |
| Input Voltage Range (Note 1) | $\mathrm{V}_{\mathrm{IR}}$ | $\pm 15$ | V |
| Output Short Circuit Duration (Note 2) | $\mathrm{tsC}_{\mathrm{tc}}$ | Indefinite |  |
| Operating Ambient Temperature <br> Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\mathrm{stg}}$ | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation <br> (Notes 2 and 3) | $\mathrm{P}_{\mathrm{D}}$ | 500 | mW |

1. Either or both input voltages must not exceed the magnitude of $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$.
2. Power dissipation must be considered to ensure maximum junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) is not exceeded (see power dissipation performance characteristic).
3. Maximum value at $\mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$.

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## PIN CONNECTIONS


(Top View)

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| LM833N | PDIP-8 | 50 Units/Rail |
| LM833D | SO-8 | 98 Units/Rail |
| LM833DR2 | SO-8 | 2500 Tape \& Reel |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Voltage ( $\mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}$ ) | $\mathrm{V}_{10}$ | - | 0.3 | 5.0 | mV |
| Average Temperature Coefficient of Input Offset Voltage $\mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 2.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Offset Current ( $\left.\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right)$ | 10 | - | 10 | 200 | nA |
| Input Bias Current ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}$ ) | 1 IB | - | 300 | 1000 | nA |
| Common Mode Input Voltage Range | $V_{\text {ICR }}$ | $-12$ | $\begin{gathered} +14 \\ -14 \end{gathered}$ | +12 - | V |
| Large Signal Voltage Gain ( $\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}$ | AvoL | 90 | 110 | - | dB |
| Output Voltage Swing: $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{ID}}=1.0 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~V}_{I D}=1.0 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{I D}=1.0 \mathrm{~V} \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{ID}}=1.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{O}+} \\ & \mathrm{V}_{\mathrm{O}-} \\ & \mathrm{V}_{\mathrm{O}+} \\ & \mathrm{V}_{\mathrm{O}} \end{aligned}$ | $\begin{gathered} 10 \\ - \\ 12 \end{gathered}$ | $\begin{gathered} 13.7 \\ -14.1 \\ 13.9 \\ -14.7 \end{gathered}$ | $\begin{gathered} -10 \\ - \\ -12 \end{gathered}$ | V |
| Common Mode Rejection ( $\mathrm{V}_{\text {in }}= \pm 12 \mathrm{~V}$ ) | CMR | 80 | 100 | - | dB |
| Power Supply Rejection ( $\mathrm{V}_{\mathrm{S}}=15 \mathrm{~V}$ to 5.0 V, -15 V to -5.0 V) | PSR | 80 | 115 | - | dB |
| Power Supply Current ( $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$, Both Amplifiers) | ID | - | 4.0 | 8.0 | mA |

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate ( $\mathrm{V}_{\text {in }}=-10 \mathrm{~V}$ to $\left.+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{A}_{\mathrm{V}}=+1.0\right)$ | $\mathrm{S}_{\mathrm{R}}$ | 5.0 | 7.0 | - | $\mathrm{V} / \mu \mathrm{s}$ |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | GBW | 10 | 15 | - | MHz |
| Unity Gain Frequency (Open Loop) | $\mathrm{f}_{\mathrm{U}}$ | - | 9.0 | - | MHz |
| Unity Gain Phase Margin (Open Loop) | $\theta_{\mathrm{m}}$ | - | 60 | - | Deg |
| Equivalent Input Noise Voltage ( $\mathrm{R}_{\mathrm{S}}=100 \Omega, \mathrm{f}=1.0 \mathrm{kHz}$ ) | $e_{n}$ | - | 4.5 | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Equivalent Input Noise Current ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $\mathrm{i}_{\mathrm{n}}$ | - | 0.5 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=27 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$, THD $\leq 1.0 \%$ ) | BWP | - | 120 | - | kHz |
| $\begin{aligned} & \text { Distortion }\left(R_{L}=2.0 \mathrm{k} \Omega, f=20 \mathrm{~Hz} \text { to } 20 \mathrm{kHz}, \mathrm{~V}_{\mathrm{O}}=3.0 \mathrm{~V}_{\mathrm{rms}}\right. \text {, } \\ & \left.\mathrm{A}_{\mathrm{V}}=+1.0\right) \end{aligned}$ | THD | - | 0.002 | - | \% |
| Channel Separation ( $\mathrm{f}=20 \mathrm{~Hz}$ to 20 kHz ) | $\mathrm{C}_{S}$ | - | -120 | - | dB |



Figure 1. Maximum Power Dissipation versus Temperature


Figure 2. Input Bias Current versus Temperature


Figure 3. Input Bias Current versus Supply Voltage


Figure 5. DC Voltage Gain versus Temperature


Figure 7. Open Loop Voltage Gain and Phase versus Frequency


Figure 4. Supply Current versus Supply Voltage


Figure 6. DC Voltage Gain versus Supply Voltage


Figure 8. Gain Bandwidth Product versus Temperature


Figure 9. Gain Bandwidth Product versus Supply Voltage


Figure 11. Slew Rate versus Supply Voltage


Figure 13. Maximum Output Voltage versus Supply Voltage


Figure 10. Slew Rate versus Temperature


Figure 12. Output Voltage versus Frequency


Figure 14. Output Saturation Voltage versus Temperature


Figure 15. Power Supply Rejection versus Frequency


Figure 17. Total Harmonic Distortion versus Frequency


Figure 19. Input Referred Noise Current versus Frequency


Figure 16. Common Mode Rejection versus Frequency


Figure 18. Input Referred Noise Voltage versus Frequency


Figure 20. Input Referred Noise Voltage versus Source Resistance

## LM833



Figure 21. Inverting Amplifier
Figure 22. Noninverting Amplifier Slew Rate

t , TIME ( $200 \mathrm{~ns} /$ DIV)

Figure 23. Noninverting Amplifier Overshoot

## MC33077

## Low Noise Dual Operational Amplifier

The MC33077 is a precision high quality, high frequency, low noise monolithic dual operational amplifier employing innovative bipolar design techniques. Precision matching coupled with a unique analog resistor trim technique is used to obtain low input offset voltages. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product of the amplifier. In addition, the MC33077 offers low input noise voltage, low temperature coefficient of input offset voltage, high slew rate, high AC and DC open loop voltage gain and low supply current drain. The all NPN transistor output stage exhibits no deadband cross-over distortion, large output voltage swing, excellent phase and gain margins, low open loop output impedance and symmetrical source and sink AC frequency performance.

The MC33077 is tested over the automotive temperature range and is available in plastic DIP and SO-8 packages ( P and D suffixes).

- Low Voltage Noise: $4.4 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ @ 1.0 kHz
- Low Input Offset Voltage: 0.2 mV
- Low TC of Input Offset Voltage: $2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- High Gain Bandwidth Product: 37 MHz @ 100 kHz
- High AC Voltage Gain: 370 @ 100 kHz

$$
1850 @ 20 \mathrm{kHz}
$$

- Unity Gain Stable: with Capacitance Loads to 500 pF
- High Slew Rate: $11 \mathrm{~V} / \mu \mathrm{s}$
- Low Total Harmonic Distortion: 0.007\%
- Large Output Voltage Swing: +14 V to -14.7 V
- High DC Open Loop Voltage Gain: 400 k (112 dB)
- High Common Mode Rejection: 107 dB
- Low Power Supply Drain Current: 3.5 mA
- Dual Supply Operation: $\pm 2.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$


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## MARKING

 DIAGRAMS

> A $=$ Assembly Location
> WL, L $=$ Wafer Lot
> YY, Y $=$ Year
> WW, W $=$ Work Week

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33077D | SO-8 | 98 Units/Rail |
| MC33077DR2 | SO-8 | 2500 Tape \& Reel |
| MC33077P | PDIP-8 | 50 Units/Rail |



Figure 1. Representative Schematic Diagram (Each Amplifier)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (VCC to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | +36 | V |
| Input Differential Voltage Range | $\mathrm{V}_{\mathrm{IDR}}$ | Note 1 | V |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | Note 1 | V |
| Output Short Circuit Duration (Note 2) | $\mathrm{t}_{\mathrm{SC}}$ | Indefinite | sec |
| Maximum Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Note 2 | mW |

DC ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage ( } \left.\mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\left\|\mathrm{V}_{10}\right\|$ |  |  | $\begin{aligned} & 1.0 \\ & 1.5 \end{aligned}$ | mV |
| Average Temperature Coefficient of Input Offset Voltage $\mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 2.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Bias Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $I_{\text {IB }}$ |  | 280 | $\begin{aligned} & 1000 \\ & 1200 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Offset Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{l}_{10}$ | - | 15 | $\begin{aligned} & 180 \\ & 240 \end{aligned}$ | nA |
| Common Mode Input Voltage Range ( $\Delta \mathrm{V}_{\text {IO }},=5.0 \mathrm{mV}, \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ ) | $V_{\text {ICR }}$ | $\pm 13.5$ | $\pm 14$ | - | V |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{O}}= \pm 1.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | Avol | $\begin{aligned} & 150 \\ & 125 \end{aligned}$ | 400 | - | kV/V |
| $\begin{aligned} & \text { Output Voltage Swing }\left(\mathrm{V}_{I D}= \pm 1.0 \mathrm{~V}\right) \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{V}_{+}} \\ & \mathrm{V}_{\mathrm{O}} \\ & \mathrm{~V}_{\mathrm{O}+} \\ & \mathrm{V}_{\mathrm{O}} \end{aligned}$ | $\begin{gathered} +13.0 \\ - \\ +13.4 \end{gathered}$ | $\begin{aligned} & +13.6 \\ & -14.1 \\ & +14.0 \\ & -14.7 \end{aligned}$ | $\begin{gathered} - \\ -13.5 \\ - \\ -14.3 \end{gathered}$ | V |
| Common Mode Rejection ( $\mathrm{V}_{\text {in }}= \pm 13 \mathrm{~V}$ ) | CMR | 85 | 107 | - | dB |
| Power Supply Rejection (Note 3) $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=+15 \mathrm{~V} /-15 \mathrm{~V} \text { to }+5.0 \mathrm{~V} /-5.0 \mathrm{~V}$ | PSR | 80 | 90 | - | dB |
| Output Short Circuit Current ( $\mathrm{V}_{\mathrm{ID}}= \pm 1.0 \mathrm{~V}$, Output to Ground) Source <br> Sink | Isc | $\begin{aligned} & +10 \\ & -20 \end{aligned}$ | $\begin{aligned} & +26 \\ & -33 \end{aligned}$ | $\begin{aligned} & +60 \\ & +60 \end{aligned}$ | mA |
| Power Supply Current ( $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$, All Amplifiers) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | ID | - | 3.5 | $\begin{aligned} & 4.5 \\ & 4.8 \end{aligned}$ | mA |

1. Either or both input voltages should not exceed $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$ (See Applications Information).
2. Power dissipation must be considered to ensure maximum junction temperature ( $T_{J}$ ) is not exceeded (See power dissipation performance characteristic, Figure 2).
3. Measured with $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{EE}}$ simultaneously varied.

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate ( $\mathrm{V}_{\text {in }}=-10 \mathrm{~V}$ to $\left.+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{A}_{\mathrm{V}}=+1.0\right)$ | SR | 8.0 | 11 | - | V/us |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | GBW | 25 | 37 | - | MHz |
| $\begin{aligned} & \text { AC Voltage Gain }\left(R_{L}=2.0 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{f}=100 \mathrm{kHz} \\ & \mathrm{f}=20 \mathrm{kHz} \end{aligned}$ | Avo | - | $\begin{gathered} 370 \\ 1850 \end{gathered}$ |  | V/V |
| Unity Gain Bandwidth (Open Loop) | BW | - | 7.5 | - | MHz |
| Gain Margin ( $\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}$ ) | $\mathrm{A}_{\mathrm{m}}$ | - | 10 | - | dB |
| Phase Margin ( $\left.\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}\right)$ | $\varnothing_{\mathrm{m}}$ | - | 55 | - | Deg |
| Channel Separation ( $\mathrm{f}=20 \mathrm{~Hz}$ to $20 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}=10 \mathrm{~V}_{\mathrm{pp}}$ ) | CS | - | -120 | - | dB |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=27_{\mathrm{p}-\mathrm{p}}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$, THD $\leq 1 \%$ ) | $\mathrm{BW}_{\mathrm{p}}$ | - | 200 | - | kHz |
| $\begin{gathered} \text { Distortion }\left(R_{L}=2.0 \mathrm{k} \Omega\right) \\ A_{V}=+1.0, f=20 \mathrm{~Hz} \text { to } 20 \mathrm{kHz} \\ \mathrm{~V}_{\mathrm{O}}=3.0 \mathrm{~V}_{\text {rms }} \\ A_{V}=2000, \mathrm{f}=20 \mathrm{kHz} \\ \mathrm{~V}_{\mathrm{O}}=2.0 \mathrm{~V}_{\mathrm{pp}} \\ \mathrm{~V}_{\mathrm{O}}=10 \mathrm{~V}_{\mathrm{pp}} \\ \mathrm{~A}_{\mathrm{V}}=4000, \mathrm{f}=100 \mathrm{kHz} \\ \mathrm{~V}_{\mathrm{O}}=2.0 \mathrm{~V}_{\mathrm{pp}} \\ \mathrm{~V}_{\mathrm{O}}=10 \mathrm{~V} \end{gathered}$ | THD |  | $\begin{aligned} & 0.007 \\ & 0.215 \\ & 0.242 \\ & 0.3 .19 \\ & 0.316 \end{aligned}$ |  | \% |
| Open Loop Output Impedance ( $\left.\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{f}=\mathrm{f}_{\mathrm{U}}\right)$ | $\left\|\mathrm{Z}_{\mathrm{o}}\right\|$ | - | 36 | - | $\Omega$ |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{R}_{\text {in }}$ | - | 270 | - | k $\Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{C}_{\text {in }}$ | - | 15 | - | pF |
| $\begin{aligned} & \text { Equivalent Input Noise Voltage }\left(R_{S}=100 \Omega\right) \\ & \begin{aligned} f & =10 \mathrm{~Hz} \\ f & =1.0 \mathrm{kHz} \end{aligned} \end{aligned}$ | $\mathrm{e}_{\mathrm{n}}$ | - | $\begin{aligned} & 6.7 \\ & 4.4 \end{aligned}$ | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| $\begin{aligned} & \text { Equivalent Input Noise Current }(f=1.0 \mathrm{kHz}) \\ & \begin{array}{l} f=10 \mathrm{~Hz} \\ \mathrm{f}=1.0 \mathrm{kHz} \end{array} \end{aligned}$ | $\mathrm{i}_{\mathrm{n}}$ | - | $\begin{aligned} & 1.3 \\ & 0.6 \\ & \hline \end{aligned}$ | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |



Figure 2. Maximum Power Dissipation versus Temperature


Figure 3. Input Bias Current versus Supply Voltage


Figure 4. Input Bias Current versus Temperature

Figure 6. Input Bias Current versus Common Mode Voltage


Figure 5. Input Offset Voltage versus Temperature


Figure 7. Input Common Mode Voltage Range versus Temperature


Figure 8. Output Saturation Voltage versus Load Resistance to Ground


Figure 9. Output Short Circuit Current versus Temperature


Figure 10. Supply Current versus Temperature


Figure 12. Power Supply Rejection versus Frequency


Figure 14. Gain Bandwidth Product versus Temperature


Figure 11. Common Mode Rejection versus Frequency


Figure 13. Gain Bandwidth Product versus Supply Voltage


Figure 15. Maximum Output Voltage versus Supply Voltage


Figure 16. Output Voltage
versus Frequency


Figure 18. Open Loop Voltage Gain versus Temperature


Figure 20. Channel Separation versus Frequency


Figure 17. Open Loop Voltage Gain versus Supply Voltage


Figure 19. Output Impedance versus Frequency


Figure 21. Total Harmonic Distortion versus Frequency


Figure 22. Total Harmonic Distortion versus Frequency


Figure 24. Slew Rate versus Supply Voltage


Figure 26. Voltage Gain and Phase versus Frequency


Figure 23. Total Harmonic Distortion versus Output Voltage


Figure 25. Slew Rate versus Temperature


Figure 27. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance


Figure 28. Phase Margin versus Output Voltage


Figure 30. Input Referred Noise Voltage and Current versus Frequency


Figure 32. Phase Margin and Gain Margin versus Differential Source Resistance


Figure 29. Overshoot versus Output Load Capacitance


Figure 31. Total Input Referred Noise Voltage versus Source Resistant

t, TIME ( $2.0 \mu \mathrm{~s} / \mathrm{DIV}$ )

Figure 33. Inverting Amplifer Slew Rate

t , TIME ( $2.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 34. Non-inverting Amplifier Slew Rate

t , TIME ( $200 \mathrm{~ns} / \mathrm{DIV}$ )
Figure 35. Non-inverting Amplifier Overshoot


Figure 36. Low Frequency Noise Voltage versus Time

## APPLICATIONS INFORMATION

The MC33077 is designed primarily for its low noise, low offset voltage, high gain bandwidth product and large output swing characteristics. Its outstanding high frequency gain/phase performance make it a very attractive amplifier for high quality preamps, instrumentation amps, active filters and other applications requiring precision quality characteristics.

The MC33077 utilizes high frequency lateral PNP input transistors in a low noise bipolar differential stage driving a compensated Miller integration amplifier. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product. The output stage uses an all NPN transistor design which provides greater output voltage swing and improved frequency performance over more conventional stages by using both PNP and NPN transistors (Class AB). This combination produces an amplifier with superior characteristics.

Through precision component matching and innovative current mirror design, a lower than normal temperature coefficient of input offset voltage ( $2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ as opposed to 10 $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ ), as well as low input offset voltage, is accomplished.

The minimum common mode input range is from 1.5 V below the positive rail $\left(\mathrm{V}_{\mathrm{CC}}\right)$ to 1.5 V above the negative rail $\left(\mathrm{V}_{\mathrm{EE}}\right)$. The inputs will typically common mode to within 1.0 V of both negative and positive rails though degradation in offset voltage and gain will be experienced as the common mode voltage nears either supply rail. In practice, though not recommended, the input voltage may exceed $\mathrm{V}_{\mathrm{CC}}$ by approximately 3.0 V and decrease below the $\mathrm{V}_{\mathrm{EE}}$ by approximately 0.6 V without causing permanent damage to the device. If the input voltage on either or both inputs is less than approximately 0.6 V , excessive current may flow, if not limited, causing permanent damage to the device.

The amplifier will not latch with input source currents up to 20 mA , though in practice, source currents should be limited to 5.0 mA to avoid any parametric damage to the device. If both inputs exceed $\mathrm{V}_{\mathrm{CC}}$, the output will be in the high state and phase reversal may occur. No phase reversal will occur if the voltage on one input is within the common mode range and the voltage on the other input exceeds $\mathrm{V}_{\mathrm{CC}}$. Phase reversal may occur if the input voltage on either or both inputs is less than 1.0 V above the negative rail. Phase reversal will be experienced if the voltage on either or both inputs is less than $\mathrm{V}_{\mathrm{EE}}$.

Through the use of dual-doublet frequency compensation techniques, the gain bandwidth product has been greatly enhanced over other amplifiers using the conventional single pole compensation. The phase and gain error of the amplifier remains low to higher frequencies for fixed amplifier gain configurations.

With the all NPN output stage, there is minimal swing loss to the supply rails, producing superior output swing, no crossover distortion and improved output phase symmetry with output voltage excursions (output phase symmetry being the amplifiers ability to maintain a constant phase
relation independent of its output voltage swing). Output phase symmetry degradation in the more conventional PNP and NPN transistor output stage was primarily due to the inherent cut-off frequency mismatch of the PNP and NPN transistors used (typically 10 MHz and 300 MHz , respectively), causing considerable phase change to occur as the output voltage changes. By eliminating the PNP in the output, such phase change has been avoided and a very significant improvement in output phase symmetry as well as output swing has been accomplished.
The output swing improvement is most noticeable when operation is with lower supply voltages (typically $30 \%$ with $\pm 5.0 \mathrm{~V}$ supplies). With a 10 k load, the output of the amplifier can typically swing to within 1.0 V of the positive rail $\left(\mathrm{V}_{\mathrm{CC}}\right)$, and to within 0.3 V of the negative rail $\left(\mathrm{V}_{\mathrm{EE}}\right)$, producing a $28.7 \mathrm{~V}_{\mathrm{pp}}$ signal from $\pm 15 \mathrm{~V}$ supplies. Output voltage swing can be further improved by using an output pull-up resistor referenced to the $\mathrm{V}_{\mathrm{CC}}$. Where output signals are referenced to the positive supply rail, the pull-up resistor will pull the output to $\mathrm{V}_{\mathrm{CC}}$ during the positive swing, and during the negative swing, the NPN output transistor collector will pull the output very near $\mathrm{V}_{\mathrm{EE}}$. This configuration will produce the maximum attainable output signal from given supply voltages. The value of load resistance used should be much less than any feedback resistance to avoid excess loading and allow easy pull-up of the output.
Output impedance of the amplifier is typically less than $50 \Omega$ at frequencies less than the unity gain crossover frequency (see Figure 19). The amplifier is unity gain stable with output capacitance loads up to 500 pF at full output swing over the $-55^{\circ}$ to $+125^{\circ} \mathrm{C}$ temperature range. Output phase symmetry is excellent with typically $4^{\circ} \mathrm{C}$ total phase change over a 20 V output excursion at $25^{\circ} \mathrm{C}$ with a $2.0 \mathrm{k} \Omega$ and 100 pF load. With a $2.0 \mathrm{k} \Omega$ resistive load and no capacitance loading, the total phase change is approximately one degree for the same 20 V output excursion. With a $2.0 \mathrm{k} \Omega$ and 500 pF load at $125^{\circ} \mathrm{C}$, the total phase change is typically only $10^{\circ} \mathrm{C}$ for a 20 V output excursion (see Figure 28).
As with all amplifiers, care should be exercised to insure that one does not create a pole at the input of the amplifier which is near the closed loop corner frequency. This becomes a greater concern when using high frequency amplifiers since it is very easy to create such a pole with relatively small values of resistance on the inputs. If this does occur, the amplifier's phase will degrade severely causing the amplifier to become unstable. Effective source resistances, acting in conjunction with the input capacitance of the amplifier, should be kept to a minimum to avoid creating such a pole at the input (see Figure 32). There is minimal effect on stability where the created input pole is much greater than the closed loop corner frequency. Where amplifier stability is affected as a result of a negative feedback resistor in conjunction with the
amplifier's input capacitance, creating a pole near the closed loop corner frequency, lead capacitor compensation techniques (lead capacitor in parallel with the feedback resistor) can be employed to improve stability. The feedback resistor and lead capacitor RC time constant should be larger than that of the uncompensated input pole frequency. Having a high resistance connected to the noninverting input of the amplifier can create a like instability problem. Compensation for this condition can be accomplished by adding a lead capacitor in parallel with the noninverting input resistor of such a value as to make the RC time constant larger than the RC time constant of the uncompensated input resistor acting in conjunction with the amplifiers input capacitance.

For optimum frequency performance and stability, careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input output coupling. In order to reduce the input capacitance, the body of resistors connected to the input pins should be physically close to the input pins. This not only minimizes the input pole creation for optimum frequency response, but also minimizes extraneous signal "pickup" at this node. Power supplies should be decoupled with adequate capacitance as close as possible to the device supply pin.

In addition to amplifier stability considerations, input source resistance values should be low to take full advantage
of the low noise characteristics of the amplifier. Thermal noise (Johnson Noise) of a resistor is generated by thermally-charged carriers randomly moving within the resistor creating a voltage. The rms thermal noise voltage in a resistor can be calculated from:

$$
\mathrm{E}_{\mathrm{nr}}=/ \overline{4 \mathrm{kTR} \times \mathrm{BW}}
$$

## where:

$\mathrm{k}=$ Boltzmann's Constant ( $1.38 \times 10^{-23}$ joules $/ \mathrm{k}$ )
$\mathrm{T}=$ Kelvin temperature
R = Resistance in ohms
BW = Upper and lower frequency limit in Hertz.
By way of reference, a $1.0 \mathrm{k} \Omega$ resistor at $25^{\circ} \mathrm{C}$ will produce a $4.0 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ of rms noise voltage. If this resistor is connected to the input of the amplifier, the noise voltage will be gained-up in accordance to the amplifier's gain configuration. For this reason, the selection of input source resistance for low noise circuit applications warrants serious consideration. The total noise of the amplifier, as referred to its inputs, is typically only $4.4 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ at 1.0 kHz .

The output of any one amplifier is current limited and thus protected from a direct short to ground, However, under such conditions, it is important not to allow the amplifier to exceed the maximum junction temperature rating. Typically for $\pm 15 \mathrm{~V}$ supplies, any one output can be shorted continuously to ground without exceeding the temperature rating.


Note: All capacitors are non-polarized.

Figure 37. Voltage Noise Test Circuit ( 0.1 Hz to $10 \mathrm{~Hz}_{\mathrm{p}-\mathrm{p}}$ )

## MC33078, MC33079

## Low Noise Dual/Quad Operational Amplifiers

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions, tested over the automotive temperature range and available in the plastic DIP and SOIC packages (P and D suffixes).

- Dual Supply Operation: $\pm 5.0 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$
- Low Voltage Noise: $4.5 \mathrm{nV} / \sqrt{\mathrm{Hz}}$
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: $2.0 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$
- Low Total Harmonic Distortion: 0.002\%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/ $\mu \mathrm{s}$
- High Open Loop AC Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/ -14.6 V
- ESD Diodes Provided on the Inputs


Figure 1. Representative Schematic Diagram
(Each Amplifier)

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MARKING DIAGRAMS

DUAL


PDIP-8 P SUFFIX CASE 626


QUAD


14

$\begin{array}{ll}\text { A } & =\text { Assembly Location } \\ \text { WL, L } & =\text { Wafer Lot } \\ \text { YY, Y } & =\text { Year } \\ \text { WW, W } & =\text { Work Week }\end{array}$

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33078D | SO-8 | 98 Units/Rail |
| MC33078DR2 | SO-8 | 2500 Tape \& Reel |
| MC33078P | PDIP-8 | 50 Units/Rail |
| MC33079D | SO-14 | 55 Units/Rail |
| MC33079DR2 | SO-14 | 2500 Tape \& Reel |
| MC33079P | PDIP-14 | 25 Units/Rail |

## MC33078, MC33079

## PIN CONNECTIONS

DUAL
CASE 626/751


QUAD
CASE 646/751A


MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE})}$ | $\mathrm{V}_{\mathrm{S}}$ | +36 | V |
| Input Differential Voltage Range | $\mathrm{V}_{\mathrm{IDR}}$ | Note 1 | V |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | Note 1 | V |
| Output Short Circuit Duration (Note 2) | $\mathrm{t}_{\mathrm{SC}}$ | Indefinite | sec |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\mathrm{stg}}$ | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Note 2 | mW |

1. Either or both input voltages must not exceed the magnitude of $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$.
2. Power dissipation must be considered to ensure maximum junction temperature $\left(\mathrm{T}_{\mathrm{J}}\right)$ is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage }\left(\mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ &(\mathrm{MC} 3078) \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \\ & \text { (MC33079) } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\left\|\mathrm{V}_{10}\right\|$ | $\begin{aligned} & \text { - } \\ & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{gathered} 0.15 \\ - \\ 0.15 \end{gathered}$ | $\begin{aligned} & 2.0 \\ & 3.0 \\ & 2.5 \\ & 3.5 \end{aligned}$ | mV |
| Average Temperature Coefficient of Input Offset Voltage $\mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 2.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Bias Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $I_{\text {IB }}$ |  | 300 | $\begin{aligned} & 750 \\ & 800 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Offset Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | ${ }_{10}$ | - | 25 | $\begin{aligned} & 150 \\ & 175 \end{aligned}$ | nA |
| Common Mode Input Voltage Range ( $\Delta \mathrm{V}_{1 \mathrm{O}}=5.0 \mathrm{mV}, \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ ) | $V_{\text {ICR }}$ | $\pm 13$ | $\pm 14$ | - | V |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | Avol | $\begin{aligned} & 90 \\ & 85 \end{aligned}$ | 110 |  | dB |
| $\begin{aligned} & \text { Output Voltage Swing }\left(\mathrm{V}_{\mathrm{ID}}= \pm 1.0 \mathrm{~V}\right) \\ & \mathrm{R}_{\mathrm{L}}=600 \Omega \\ & \mathrm{R}_{\mathrm{L}}=600 \Omega \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega \end{aligned}$ | $\mathrm{V}_{\mathrm{O}^{+}}$ <br> $\mathrm{V}_{\mathrm{O}^{-}}$ <br> $\mathrm{V}_{\mathrm{O}^{+}}$ <br> $\mathrm{V}_{\mathrm{O}^{-}}$ <br> $\mathrm{V}_{\mathrm{O}^{+}}$ <br> $\mathrm{V}_{\mathrm{O}}-$ | $\begin{gathered} +13.2 \\ - \\ +13.5 \end{gathered}$ | $\begin{aligned} & +10.7 \\ & -11.9 \\ & +13.8 \\ & -13.7 \\ & +14.1 \\ & -14.6 \end{aligned}$ | $\begin{gathered} - \\ - \\ - \\ -13.2 \\ - \\ -14 \end{gathered}$ | V |
| Common Mode Rejection ( $\mathrm{V}_{\text {in }}= \pm 13 \mathrm{~V}$ ) | CMR | 80 | 100 | - | dB |
| Power Supply Rejection (Note 3) $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=+15 \mathrm{~V} /-15 \mathrm{~V} \text { to }+5.0 \mathrm{~V} /-5.0 \mathrm{~V}$ | PSR | 80 | 105 | - | dB |
| Output Short Circuit Current ( $\mathrm{V}_{\mathrm{ID}}=1.0 \mathrm{~V}$, Output to Ground) Source Sink | Isc | $\begin{aligned} & +15 \\ & -20 \end{aligned}$ | $\begin{aligned} & +29 \\ & -37 \end{aligned}$ | - | mA |
| Power Supply Current ( $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$, All Amplifiers) <br> (MC33078) $\begin{aligned} & T_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ <br> (MC33079) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | ID | - | $\begin{gathered} 4.1 \\ - \\ 8.4 \end{gathered}$ | $\begin{aligned} & 5.0 \\ & 5.5 \\ & 10 \\ & 11 \end{aligned}$ | mA |

3. Measured with $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{EE}}$ differentially varied simultaneously.

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate ( $\mathrm{V}_{\text {in }}=-10 \mathrm{~V}$ to $\left.+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF} \mathrm{A} \mathrm{V}^{\prime}=+1.0\right)$ | SR | 5.0 | 7.0 | - | $\mathrm{V} / \mu \mathrm{s}$ |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | GBW | 10 | 16 | - | MHz |
| Unity Gain Bandwidth (Open Loop) | BW | - | 9.0 | - | MHz |
| $\begin{aligned} & \text { Gain Margin }\left(R_{L}=2.0 \mathrm{k} \Omega\right) \\ & C_{L}=0 \mathrm{pF} \\ & \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF} \end{aligned}$ | $A_{m}$ | - | $\begin{aligned} & -11 \\ & -6.0 \end{aligned}$ | - | dB |
| $\begin{aligned} & \text { Phase Margin }\left(R_{L}=2.0 \mathrm{k} \Omega\right) \\ & C_{L}=0 \mathrm{pF} \\ & C_{L}=100 \mathrm{pF} \end{aligned}$ | $\phi_{\mathrm{m}}$ | - | $\begin{aligned} & 55 \\ & 40 \end{aligned}$ | - | Deg |
| Channel Separation ( $\mathrm{f}=20 \mathrm{~Hz}$ to 20 kHz ) | CS | - | -120 | - | dB |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=27 \mathrm{~V}_{\mathrm{pp}}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$, THD $\leq 1.0 \%$ ) | $\mathrm{BW}_{\mathrm{p}}$ | - | 120 | - | kHz |
| Total Harmonic Distortion ( $\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{f}=20 \mathrm{~Hz}$ to $20 \mathrm{kHz}, \mathrm{V}_{\mathrm{O}}=3.0 \mathrm{~V}_{\mathrm{rms}}, \mathrm{A}_{\mathrm{V}}=+1.0$ ) | THD | - | 0.002 | - | \% |
| Open Loop Output Impedance ( $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{f}=9.0 \mathrm{MHz}$ ) | $\left\|\mathrm{Z}_{\mathrm{O}}\right\|$ | - | 37 | - | $\Omega$ |
| Differential Input Resistance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{R}_{\text {in }}$ | - | 175 | - | k $\Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) | $\mathrm{C}_{\text {in }}$ | - | 12 | - | pF |
| Equivalent Input Noise Voltage ( $\mathrm{R}_{\mathrm{S}}=100 \Omega$, $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $\mathrm{e}_{\mathrm{n}}$ | - | 4.5 | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Equivalent Input Noise Current ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | $i_{n}$ | - | 0.5 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |



Figure 2. Maximum Power Dissipation versus Temperature


Figure 4. Input Bias Current versus Temperature

Figure 3. Input Bias Current versus Supply Voltage


Figure 5. Input Offset Voltage versus Temperature


Figure 6. Input Bias Current versus Common Mode Voltage


Figure 7. Input Common Mode Voltage Range versus Temperature


Figure 8. Output Saturation Voltage versus Load Resistance to Ground


Figure 9. Output Short Circuit Current versus Temperature


Figure 10. Supply Current versus Temperature


Figure 11. Common Mode Rejection versus Frequency


Figure 12. Power Supply Rejection versus Frequency


Figure 14. Gain Bandwidth Product versus Temperature


Figure 16. Output Voltage versus Frequency


Figure 13. Gain Bandwidth Product versus Supply Voltage


Figure 15. Maximum Output Voltage versus Supply Voltage


Figure 17. Open Loop Voltage Gain versus Supply Voltage


Figure 18. Open Loop Voltage Gain versus Temperature


Figure 20. Channel Separation versus Frequency


Figure 19. Output Impedance versus Frequency


Figure 21. Total Harmonic Distortion versus Frequency


Figure 22. Total Harmonic Distortion versus Output Voltage


Figure 23. Slew Rate versus Supply Voltage


Figure 24. Slew Rate versus Temperature


Figure 26. Open Loop Gain Margin and Phase Margin versus Load Capacitance


Figure 25. Voltage Gain and Phase versus Frequency


Figure 27. Overshoot versus Output Load Capacitance


Figure 28. Input Referred Noise Voltage and Current versus Frequency


Figure 29. Total Input Referred Noise Voltage versus Source Resistance

MC33078, MC33079

$\mathrm{R}_{\mathrm{T}}$, DIFFERENTIAL SOURCE RESISTANCE ( $\Omega$ )
Figure 30. Phase Margin and Gain Margin versus Differential Source Resistance

t , TIME ( $2.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 31. Inverting Amplifier Slew Rate

t, TIME ( $200 \mu \mathrm{~s} / \mathrm{DIV}$ )
Figure 33. Non-inverting Amplifier Overshoot

t , TIME ( $2.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 32. Non-inverting Amplifier Slew Rate

t , TIME ( $1.0 \mathrm{sec} / \mathrm{DIV}$ )
Figure 34. Low Frequency Noise Voltage versus Time


Note: All capacitors are non-polarized.
Figure 35. Voltage Noise Test Circuit
( 0.1 Hz to $10 \mathrm{~Hz}_{\mathrm{p}-\mathrm{p}}$ )

## MC33272A, MC33274A

## Single Supply, <br> High Slew Rate, <br> Low Input Offset Voltage Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip-R-Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual-doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33272/74 series is specified over $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ and are available in plastic DIP and SOIC surface mount packages.

- Input Offset Voltage Trimmed to $100 \mu \mathrm{~V}$ (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: $16 \mathrm{M} \Omega$
- Low Noise: $18 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: $10 \mathrm{~V} / \mu \mathrm{s}$
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ -14.6 V
- Low Total Harmonic Distortion: 0.003\%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or $\pm 1.5 \mathrm{~V}$ to $\pm 18 \mathrm{~V}$
- ESD Diodes Provide Added Protection to the Inputs



## ON Semiconductor ${ }^{\text {w }}$

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MARKING DIAGRAMS

QUAD


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$



| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33272AD | SO-8 | 98 Units/Rail |
| MC33272ADR2 | SO-8 | 2500 Tape \& Reel |
| MC33272AP | PDIP-8 | 50 Units/Rail |
| MC33274AD | SO-14 | 55 Units/Rail |
| MC33274ADR2 | SO-14 | 2500 Tape \& Reel |
| MC33274AP | PDIP-14 | 25 Units/Rail |

## MC33272A, MC33274A

## PIN CONNECTIONS



MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ | +36 | V |
| Input Differential Voltage Range | $\mathrm{V}_{\mathrm{IDR}}$ | Note 1 | V |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | Note 1 | V |
| Output Short Circuit Duration (Note 2) | $\mathrm{t}_{\mathrm{SC}}$ | Indefinite | sec |
| Maximum Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | Note 2 | mW |

1. Either or both input voltages should not exceed $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$.
2. Power dissipation must be considered to ensure maximum junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage }\left(R_{S}=10 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ &\left(\mathrm{V}_{\mathrm{CC}}\right.\left.=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \\ &\left(\mathrm{~V}_{\mathrm{CC}}\right.\left.=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ | 3 | $\left\|\mathrm{V}_{10}\right\|$ | - | $0.1$ | $\begin{aligned} & 1.0 \\ & 1.8 \\ & 2.0 \end{aligned}$ | mV |
| Average Temperature Coefficient of Input Offset Voltage $\mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C}$ | 3 | $\Delta \mathrm{V}_{1 \mathrm{O}} / \Delta \mathrm{T}$ | - | 2.0 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Bias Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 4, 5 | $I_{\text {IB }}$ | - | $300$ | $\begin{aligned} & 650 \\ & 800 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Offset Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ |  | $\left\|l_{10}\right\|$ | - | 3.0 - | $\begin{aligned} & 65 \\ & 80 \end{aligned}$ | nA |
| Common Mode Input Voltage Range ( $\Delta \mathrm{V}_{1 \mathrm{O}}=5.0 \mathrm{mV}, \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ ) $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | 6 | VICR | $\mathrm{V}_{\mathrm{EE}}$ to ( $\left.\mathrm{V}_{\mathrm{CC}}-1.8\right)$ |  |  | V |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V} \text { to } 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | 7 | $A_{\text {VOL }}$ | $\begin{aligned} & 90 \\ & 86 \end{aligned}$ | $100$ |  | dB |
| $\begin{aligned} & \text { Output Voltage Swing }\left(\mathrm{V}_{I D}= \pm 1.0 \mathrm{~V}\right) \\ &\left(\mathrm{V}_{\mathrm{CC}}\right.\left.=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}\right) \\ & R_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & R_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ & R_{\mathrm{L}}=10 \mathrm{k} \Omega \\ &\left(\mathrm{~V}_{\mathrm{CC}}\right.\left.=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}\right) \\ & R_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & R_{\mathrm{L}}=2.0 \mathrm{k} \Omega \end{aligned}$ | $8,9,12$ <br> 10, 11 | $\mathrm{V}_{\mathrm{O}}+$ <br> $\mathrm{V}_{\mathrm{O}}{ }^{-}$ <br> $\mathrm{V}_{\mathrm{O}}+$ <br> $\mathrm{V}_{\mathrm{O}}-$ <br> $\mathrm{V}_{\mathrm{OL}}$ <br> $V_{\mathrm{OH}}$ | $\begin{gathered} 13.4 \\ - \\ 13.4 \\ - \\ - \\ 3.7 \end{gathered}$ | $\begin{gathered} 13.9 \\ -13.9 \\ 14 \\ -14.7 \\ - \end{gathered}$ | $\begin{gathered} - \\ -13.5 \\ - \\ -14.1 \\ 0.2 \\ 5.0 \end{gathered}$ | V |
| Common Mode Rejection ( $\mathrm{V}_{\text {in }}=+13.2 \mathrm{~V}$ to -15 V ) | 13 | CMR | 80 | 100 | - | dB |
| Power Supply Rejection $\mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=+15 \mathrm{~V} /-15 \mathrm{~V},+5.0 \mathrm{~V} /-15 \mathrm{~V},+15 \mathrm{~V} /-5.0 \mathrm{~V}$ | 14, 15 | PSR | 80 | 105 | - | dB |
| Output Short Circuit Current (VID $=1.0 \mathrm{~V}$, Output to Ground) <br> Source <br> Sink | 16 | Isc | $\begin{aligned} & +25 \\ & -25 \end{aligned}$ | $\begin{aligned} & +37 \\ & -37 \end{aligned}$ | - | mA |
| $\begin{aligned} & \text { Power Supply Current Per Amplifier }\left(\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ &\left(\mathrm{V}_{\mathrm{CC}}\right.\left.=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \\ &\left(\mathrm{~V}_{\mathrm{CC}}\right.\left.=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \end{aligned}$ | 17 | Icc |  | $2.15$ | $\begin{gathered} 2.75 \\ 3.0 \\ 2.75 \end{gathered}$ | mA |

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristics | Figure | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Slew Rate $\left(\mathrm{V}_{\text {in }}=-10 \mathrm{~V} \text { to }+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}, \mathrm{~A}_{\mathrm{V}}=+1.0 \mathrm{~V}\right)$ | 18, 33 | SR | 8.0 | 10 | - | V/ $/ \mathrm{s}$ |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | 19 | GBW | 17 | 24 | - | MHz |
| AC Voltage Gain ( $\left.\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{f}=20 \mathrm{kHz}\right)$ | 20, 21, 22 | $A_{\text {Vo }}$ | - | 65 | - | dB |
| Unity Gain Bandwidth (Open Loop) |  | BW | - | 5.5 | - | MHz |
| Gain Margin ( $\left.\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}\right)$ | 23, 24, 26 | $\mathrm{A}_{\mathrm{m}}$ | - | 12 | - | dB |
| Phase Margin ( $\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=0 \mathrm{pF}$ ) | 23, 25, 26 | $\phi_{\mathrm{m}}$ | - | 55 | - | Deg |
| Channel Separation ( $\mathrm{f}=20 \mathrm{~Hz}$ to 20 kHz ) | 27 | CS | - | -120 | - | dB |
| Power Bandwidth ( $\mathrm{V}_{\mathrm{O}}=20 \mathrm{~V}$ pp, $\mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega$, THD $\leq 1.0 \%$ ) |  | $\mathrm{BW}_{\mathrm{P}}$ | - | 160 | - | kHz |
| Total Harmonic Distortion $\left(R_{L}=2.0 \mathrm{k} \Omega, f=20 \mathrm{~Hz} \text { to } 20 \mathrm{kHz}, \mathrm{~V}_{\mathrm{O}}=3.0 \mathrm{~V}_{\mathrm{rms}}, \mathrm{~A}_{\mathrm{V}}=+1.0\right)$ | 28 | THD | - | 0.003 | - | \% |
| Open Loop Output Impedance ( $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{f}=6.0 \mathrm{MHz}$ ) | 29 | $\left\|\mathrm{Z}_{\mathrm{O}}\right\|$ | - | 35 | - | $\Omega$ |
| Differential Input Resistance ( $\left.\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}\right)$ |  | $\mathrm{R}_{\text {in }}$ | - | 16 | - | $\mathrm{M} \Omega$ |
| Differential Input Capacitance ( $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ ) |  | $\mathrm{C}_{\text {in }}$ | - | 3.0 | - | pF |
| Equivalent Input Noise Voltage ( $\mathrm{R}_{\mathrm{S}}=100 \Omega, \mathrm{f}=1.0 \mathrm{kHz}$ ) | 30 | $\mathrm{e}_{\mathrm{n}}$ | - | 18 | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Equivalent Input Noise Current ( $\mathrm{f}=1.0 \mathrm{kHz}$ ) | 31 | $\mathrm{i}_{\mathrm{n}}$ | - | 0.5 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |



Figure 1. Equivalent Circuit Schematic
(Each Amplifier)


Figure 2. Maximum Power Dissipation versus Temperature


Figure 3. Input Offset Voltage versus Temperature for Typical Units


Figure 4. Input Bias Current versus Common Mode Voltage


Figure 5. Input Bias Current versus Temperature


Figure 6. Input Common Mode Voltage Range versus Temperature


Figure 7. Open Loop Voltage Gain versus Temperature


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage


Figure 10. Single Supply Output Saturation Voltage versus Load Resistance to Ground


Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to $\mathrm{V}_{\mathrm{Cc}}$


Figure 12. Output Voltage versus Frequency


Figure 13. Common Mode Rejection versus Frequency


Figure 14. Positive Power Supply Rejection versus Frequency


Figure 16. Output Short Circuit Current versus Temperature


Figure 18. Normalized Slew Rate versus Temperature


Figure 15. Negative Power Supply Rejection versus Frequency


Figure 17. Supply Current versus Supply Voltage


Figure 19. Gain Bandwidth Product versus Temperature


Figure 20. Voltage Gain and Phase versus Frequency


Figure 22. Open Loop Voltage Gain and Phase versus Frequency

Figure 24. Open Loop Gain Margin versus Temperature


Figure 21. Gain and Phase versus Frequency


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance


Figure 25. Phase Margin versus Temperature


Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance


Figure 28. Total Harmonic Distortion versus Frequency


Figure 27. Channel Separation versus Frequency


Figure 29. Output Impedance versus Frequency


Figure 31. Input Referred Noise Current versus Frequency


Figure 32. Percent Overshoot versus Load Capacitance

t , TIME ( $2.0 \mu \mathrm{~s} / \mathrm{DIV}$ )
Figure 33. Non-inverting Amplifier Slew Rate for the MC33274

t , TIME ( $2.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 35. Small Signal Transient Response for MC33274

t , TIME ( $2.0 \mathrm{~ns} /$ DIV)
Figure 34. Non-inverting Amplifier Overshoot for the MC33274

t , TIME ( $1.0 \mu \mathrm{~s} / \mathrm{DIV})$
Figure 36. Large Signal Transient Response for MC33274

## MC34071,2,4,A MC33071,2,4,A

## Single Supply 3.0 V to 44 V Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, $13 \mathrm{~V} / \mu \mathrm{s}$ slew rate and fast settling time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential $\left(\mathrm{V}_{\mathrm{EE}}\right)$. With a Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/74 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic DIP, SOIC and TSSOP surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: $13 \mathrm{~V} / \mu \mathrm{s}$
- Fast Settling Time: $1.1 \mu$ s to $0.1 \%$
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground ( $\mathrm{V}_{\mathrm{EE}}$ )
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: -14.7 V to +14 V (with $\pm 15 \mathrm{~V}$ Supplies)
- Large Capacitance Drive Capability: 0 pF to $10,000 \mathrm{pF}$
- Low Total Harmonic Distortion: 0.02\%
- Excellent Phase Margin: $60^{\circ}$
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2648 of this data sheet.

See general marking information in the device marking section on page 2649 of this data sheet.

## MC34071,2,4,A MC33071,2,4,A

## PIN CONNECTIONS

CASE 626/CASE 751

(Dual, Top View)

CASE 646/CASE 751A/CASE 948G



Figure 1. Representative Schematic Diagram
(Each Amplifier)

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage (from $\mathrm{V}_{\mathrm{EE}}$ to $\mathrm{V}_{\mathrm{CC}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | +44 | V |
| Input Differential Voltage Range | $\mathrm{V}_{\text {IDR }}$ | Note 1 | V |
| Input Voltage Range | $\mathrm{V}_{\text {IR }}$ | Note 1 | V |
| Output Short Circuit Duration (Note 2) | $\mathrm{t}_{\mathrm{SC}}$ | Indefinite | sec |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Either or both input voltages should not exceed the magnitude of $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{EE}}$.
2. Power dissipation must be considered to ensure maximum junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) is not exceeded (see Figure 2).

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\right.$ connected to ground, unless otherwise noted. See Note 3 for $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}$ )

| Characteristics | Symbol | A Suffix |  |  | Non-Suffix |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Input Offset Voltage }\left(R_{S}=100 \Omega, V_{C M}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{V}_{10}$ | - | $\begin{aligned} & 0.5 \\ & 0.5 \\ & - \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.0 \\ & 5.0 \end{aligned}$ | - | $\begin{aligned} & 1.0 \\ & 1.5 \\ & - \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 5.0 \\ & 7.0 \end{aligned}$ | mV |
| Average Temperature Coefficient of Input Offset Voltage $\begin{aligned} & \mathrm{R}_{\mathrm{S}}=10 \Omega, \mathrm{~V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\Delta \mathrm{V}_{10} / \Delta \mathrm{T}$ | - | 10 | - | - | 10 | - | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| $\begin{aligned} & \text { Input Bias Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | IB | - | 100 - | $\begin{aligned} & 500 \\ & 700 \end{aligned}$ | - | 100 | $\begin{aligned} & 500 \\ & 700 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Offset Current }\left(\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | 10 | - | 6.0 | $\begin{gathered} 50 \\ 300 \end{gathered}$ | - | 6.0 - | $\begin{gathered} 75 \\ 300 \end{gathered}$ | nA |
| Input Common Mode Voltage Range $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | VICR | $\begin{aligned} & V_{E E} \text { to }\left(V_{C C}-1.8\right) \\ & V_{E E} \text { to }\left(V_{C C}-2.2\right) \end{aligned}$ |  |  | $\begin{aligned} & V_{E E} \text { to }\left(V_{C C}-1.8\right) \\ & V_{E E} \text { to }\left(V_{C C}-2.2\right) \end{aligned}$ |  |  | V |
| $\begin{aligned} & \text { Large Signal Voltage Gain }\left(\mathrm{V}_{\mathrm{O}}= \pm 10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega\right) \\ & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{A}_{\mathrm{VOL}}$ | $\begin{aligned} & 50 \\ & 25 \end{aligned}$ | 100 | - | $\begin{aligned} & 25 \\ & 20 \end{aligned}$ | $100$ | - | V/mV |
| $\begin{aligned} & \text { Output Voltage Swing }\left(\mathrm{V}_{\mathrm{ID}}= \pm 1.0 \mathrm{~V}\right) \\ & \mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, R_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \\ & \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{gathered} 3.7 \\ 13.6 \\ 13.4 \end{gathered}$ | $\begin{gathered} 4.0 \\ 14 \\ - \end{gathered}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{gathered} 3.7 \\ 13.6 \\ 13.4 \end{gathered}$ | $\begin{gathered} 4.0 \\ 14 \\ - \end{gathered}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | V |
| $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =+15 \mathrm{~V}, \mathrm{~V}_{E E}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \\ \mathrm{~T}_{\mathrm{A}} & =\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | $\begin{gathered} \hline 0.1 \\ -14.7 \end{gathered}$ | $\begin{gathered} \hline 0.3 \\ -14.3 \\ -13.5 \end{gathered}$ | - | $\begin{gathered} \hline 0.1 \\ -14.7 \end{gathered}$ | $\begin{gathered} \hline 0.3 \\ -14.3 \\ -13.5 \end{gathered}$ | V |
| Output Short Circuit Current ( $\mathrm{V}_{\mathrm{ID}}=1.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}$, $\left.\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ <br> Source <br> Sink | Isc | $\begin{aligned} & 10 \\ & 20 \end{aligned}$ | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ | - | 10 20 | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ | - | mA |
| Common Mode Rejection $\mathrm{R}_{\mathrm{S}} \leq 10 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{ICR}}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | CMR | 80 | 97 | - | 70 | 97 | - | dB |
| $\begin{aligned} & \text { Power Supply Rejection }\left(\mathrm{R}_{\mathrm{S}}=100 \Omega\right) \\ & \mathrm{V}_{\mathrm{CC}} / \mathrm{V}_{\mathrm{EE}}=+16.5 \mathrm{~V} /-16.5 \mathrm{~V} \text { to }+13.5 \mathrm{~V} /-13.5 \mathrm{~V}, \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ | PSR | 80 | 97 | - | 70 | 97 | - | dB |
| Power Supply Current (Per Amplifier, No Load) $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=+2.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}, \\ \mathrm{~T}_{\mathrm{A}} & =\mathrm{T}_{\text {low }} \text { to } \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{I}_{\mathrm{D}}$ | - | $\begin{aligned} & 1.6 \\ & 1.9 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.5 \\ & 2.8 \end{aligned}$ | - | $\begin{aligned} & 1.6 \\ & 1.9 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.5 \\ & 2.8 \end{aligned}$ | mA |
| $\mathrm{T}_{\text {low }}$ $=-40^{\circ} \mathrm{C}$ for MC33071, 2, 4,/A   <br>  $=\mathrm{T}_{\text {high }}$ $=+85^{\circ} \mathrm{C}$ for MC33071, $\mathrm{CO}, 44071,2,4,4, / \mathrm{A}$  <br>  $=-40^{\circ} \mathrm{C}$ for MC34072, 4/V  $=+70^{\circ} \mathrm{C}$ for MC34071, $2,4, / \mathrm{A}$ <br>   $=+125^{\circ} \mathrm{C}$ for MC34072, $4 / \mathrm{V}$  |  |  |  |  |  |  |  |  |

AC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\right.$ connected to ground. $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted. $)$

| Characteristics | Symbol | A Suffix |  |  | Non-Suffix |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Slew Rate }\left(\mathrm{V}_{\text {in }}=-10 \mathrm{~V} \text { to }+10 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, C_{\mathrm{L}}=500 \mathrm{pF}\right) \\ & \mathrm{A}_{\mathrm{V}}=+1.0 \\ & \mathrm{~A}_{\mathrm{V}}=-1.0 \end{aligned}$ | SR | 8.0 | $\begin{aligned} & 10 \\ & 13 \end{aligned}$ |  | 8.0 | $\begin{aligned} & 10 \\ & 13 \end{aligned}$ | - | V/us |
| $\begin{aligned} & \text { Setting Time (10 V Step, } \left.\mathrm{AV}_{\mathrm{V}}=-1.0\right) \\ & \text { To } 0.1 \%(+1 / 2 \mathrm{LSB} \text { of } 9-\text {-Bits) } \\ & \text { To } 0.01 \%(+1 / 2 \mathrm{LSB} \text { of } 12-\mathrm{Bits}) \end{aligned}$ | $\mathrm{t}_{\text {s }}$ | - | $\begin{aligned} & 1.1 \\ & 2.2 \end{aligned}$ | - | - | $\begin{aligned} & 1.1 \\ & 2.2 \end{aligned}$ | - | $\mu \mathrm{s}$ |
| Gain Bandwidth Product ( $\mathrm{f}=100 \mathrm{kHz}$ ) | GBW | 3.5 | 4.5 | - | 3.5 | 4.5 | - | MHz |
| Power Bandwidth $A_{V}=+1.0, R_{L}=2.0 \mathrm{k} \Omega, V_{O}=20 \mathrm{~V}_{\mathrm{pp}}, T H D=5.0 \%$ | BW | - | 160 | - | - | 160 | - | kHz |
| $\begin{aligned} & \text { Phase margin } \\ & R_{L}=2.0 \mathrm{k} \Omega \\ & R_{L}=2.0 \mathrm{k} \Omega, C_{L}=300 \mathrm{pF} \end{aligned}$ | $\mathrm{f}_{\mathrm{m}}$ | - | $\begin{aligned} & 60 \\ & 40 \end{aligned}$ | - | - | $\begin{aligned} & 60 \\ & 40 \end{aligned}$ | - | Deg |
| Gain Margin $\begin{aligned} & R_{\mathrm{L}}=2.0 \mathrm{k} \Omega \\ & \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{L}}=300 \mathrm{pF} \end{aligned}$ | $A_{m}$ | - | $\begin{aligned} & 12 \\ & 4.0 \end{aligned}$ | - | - | $\begin{aligned} & 12 \\ & 4.0 \end{aligned}$ | - | dB |
| Equivalent Input Noise Voltage $\mathrm{R}_{\mathrm{S}}=100 \Omega, \mathrm{f}=1.0 \mathrm{kHz}$ | $\mathrm{e}_{\mathrm{n}}$ | - | 32 | - | - | 32 | - | $\mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Equivalent Input Noise Current $\mathrm{f}=1.0 \mathrm{kHz}$ | $\mathrm{i}_{\mathrm{n}}$ | - | 0.22 | - | - | 0.22 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |
| Differential Input Resistance $\mathrm{V}_{\mathrm{CM}}=0 \mathrm{~V}$ | $\mathrm{R}_{\text {in }}$ | - | 150 | - | - | 150 | - | $\mathrm{M} \Omega$ |
| Differential Input Capacitance $V_{\mathrm{CM}}=0 \mathrm{~V}$ | $\mathrm{C}_{\text {in }}$ | - | 2.5 | - | - | 2.5 | - | pF |
| Total Harmonic Distortion $\mathrm{A}_{\mathrm{V}}=+10, \mathrm{R}_{\mathrm{L}}=2.0 \mathrm{k} \Omega, 2.0 \mathrm{~V}_{\mathrm{pp}} \leq \mathrm{V}_{\mathrm{O}} \leq 20 \mathrm{~V}_{\mathrm{pp}}, \mathrm{f}=10 \mathrm{kHz}$ | THD | - | 0.02 | - | - | 0.02 | - | \% |
| Channel Separation ( $\mathrm{f}=10 \mathrm{kHz}$ ) | - | - | 120 | - | - | 120 | - | dB |
| Open Loop Output Impedance ( $\mathrm{f}=1.0 \mathrm{MHz}$ ) | \| $\mathrm{Z}_{\mathrm{O}}$ \| | - | 30 | - | - | 30 | - | W |



Figure 2. Power Supply Configurations


Offset nulling range is approximately $\pm 80 \mathrm{mV}$ with a 10 k potentiometer (MC33071, MC34071 only).

Figure 3. Offset Null Circuit


Figure 4. Maximum Power Dissipation versus Temperature for Package Types


Figure 5. Input Offset Voltage versus Temperature for Representative Units


Figure 6. Input Common Mode Voltage Range versus Temperature


Figure 7. Normalized Input Bias Current versus Temperature


Figure 8. Normalized Input Bias Current versus Input Common Mode Voltage


Figure 9. Split Supply Output Voltage
Swing versus Supply Voltage


Figure 10. Single Supply Output Saturation versus Load Resistance to $\mathrm{V}_{\mathrm{cc}}$


Figure 12. Single Supply Output Saturation versus Load Resistance to Ground


Figure 14. Output Impedance versus Frequency


Figure 13. Output Short Circuit Current versus Temperature


Figure 15. Output Voltage Swing versus Frequency


Figure 16. Total Harmonic Distortion versus Frequency


Figure 18. Open Loop Voltage Gain versus Temperature


Figure 20. Open Loop Voltage Gain and Phase versus Frequency


Figure 17. Total Harmonic Distortion versus Output Voltage Swing


Figure 19. Open Loop Voltage Gain and Phase versus Frequency


Figure 21. Normalized Gain Bandwidth Product versus Temperature


Figure 22. Percent Overshoot versus Load Capacitance


Figure 24. Gain Margin versus Load Capacitance


Figure 26. Gain Margin versus Temperature


Figure 23. Phase Margin versus Load Capacitance


Figure 25. Phase Margin versus Temperature


Figure 27. Phase Margin and Gain Margin versus Differential Source Resistance


Figure 28. Normalized Slew Rate versus Temperature

$2.0 \mu \mathrm{~s} / \mathrm{DIV}$

Figure 30. Small Signal Transient Response


Figure 32. Common Mode Rejection versus Frequency


Figure 29. Output Settling Time

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$


Figure 33. Power Supply Rejection versus Frequency


Figure 34. Supply Current versus Supply Voltage


Figure 36. Channel Separation versus Frequency


Figure 35. Power Supply Rejection versus Temperature


Figure 37. Input Noise versus Frequency

## APPLICATIONS INFORMATION CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the $\mathrm{V}_{\mathrm{EE}}$ potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to $\pm 44 \mathrm{~V}$, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between $\mathrm{V}_{\mathrm{EE}}$ and $\mathrm{V}_{\mathrm{CC}}$ supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the $\mathrm{V}_{\mathrm{CC}}$ voltage by approximately 3.0 V and decrease below the $\mathrm{V}_{\mathrm{EE}}$ voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source
up to approximately 5.0 mA of current from $\mathrm{V}_{\mathrm{EE}}$ through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower ( 2.5 pF ) than the typical JFET input gate capacitance ( 5.0 pF ), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D-to-A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2 nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher
values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For $2.0 \mathrm{k} \Omega$ of feedback resistance, the MC34071 series can settle to within $1 / 2$ LSB of 8 bits in $1.0 \mu \mathrm{~s}$, and within $1 / 2$ LSB of 12 -bits in $2.2 \mu \mathrm{~s}$ for a 10 V step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is $\pm 13 \mathrm{~V} / \mu \mathrm{s}$. In the classic noninverting unity gain configuration, the output positive slew rate is $+10 \mathrm{~V} / \mu \mathrm{s}$, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A $10 \mathrm{k} \Omega$ load resistance can swing within 1.0 V of the positive rail $\left(\mathrm{V}_{\mathrm{CC}}\right)$, and within 0.3 V of the negative rail ( $\mathrm{V}_{\mathrm{EE}}$ ), providing a $28.7 \mathrm{~V}_{\mathrm{pp}}$ swing from $\pm 15 \mathrm{~V}$ supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor $\mathrm{Q}_{7}$, and $\mathrm{V}_{\mathrm{BE}}$ of the NPN pull up transistor $\mathrm{Q}_{17}$, and the voltage drop associated with the short circuit resistance, $\mathrm{R}_{7}$. The negative swing is limited by the saturation voltage of the pull-down transistor $\mathrm{Q}_{16}$, the voltage drop $I_{L} R_{6}$, and the voltage drop associated with resistance $\mathrm{R}_{7}$, where $\mathrm{I}_{\mathrm{L}}$ is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of $\mathrm{V}_{\mathrm{EE}}$. For large valued sink currents ( $>5.0 \mathrm{~mA}$ ), diode D3 clamps the voltage across $\mathrm{R}_{6}$, thus limiting the negative swing to the saturation voltage of $\mathrm{Q}_{16}$, plus the forward diode drop of $\mathrm{D} 3\left(\approx \mathrm{~V}_{\mathrm{EE}}+1.0 \mathrm{~V}\right)$. Thus for a given supply voltage, unprecedented peak-to-peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to $\mathrm{V}_{\mathrm{CC}}$ instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to $\mathrm{V}_{\mathrm{CC}}$ during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC34071 series offers a 20 mA
minimum current sink capability, typically to an output voltage of $\left(\mathrm{V}_{\mathrm{EE}}+1.8 \mathrm{~V}\right)$. In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.
In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance ( $30 \Omega$ typ @ 1.0 MHz ) allows capacitive drive capability from 0 pF to $10,000 \mathrm{pF}$ without oscillation in the unity closed loop gain configuration. The $60^{\circ}$ phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V , these amplifiers are functional to $3.0 \mathrm{~V} @ 25^{\circ} \mathrm{C}$ although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for $\pm 15 \mathrm{~V}$ supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

## MC34071,2,4,A MC33071,2,4,A

(Typical Single Supply Applications $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ )


Figure 38. AC Coupled Noninverting Amplifier


Figure 40. DC Coupled Inverting Amplifier Maximum Output Swing


Figure 42. Active High-Q Notch Filter


Figure 39. AC Coupled Inverting Amplifier


Figure 41. Unity Gain Buffer TTL Driver


Given $\mathrm{f}_{0}=$ Center Frequency
$\mathrm{A}_{\mathrm{O}}=$ Gain at Center Frequency
Choose Value $f_{0}, Q, A_{0}, C$
Then:

$$
R 3=\frac{Q}{\pi f_{0} C} \quad R 1=\frac{R 3}{2 H_{0}} \quad R 2=\frac{R 1 R 3}{4 Q^{2} R 1-R 3}
$$

For less than $10 \%$ error from operational amplifier $\frac{Q_{0} f_{0}}{G B W}<0.1$
where $f_{0}$ and GBW are expressed in Hz .
$G B W=4.5 \mathrm{MHz}$ Typ.

Figure 43. Active Bandpass Filter

## MC34071,2,4,A MC33071,2,4,A



Settling Time
$1.0 \mu \mathrm{~s}$ (8-Bits, $1 / 2$ LSB)
Figure 44. Low Voltage Fast D/A Converter


Figure 46. LED Driver


Figure 48. AC/DC Ground Current Monitor


Figure 45. High Speed Low Voltage Comparator


Figure 47. Transistor Driver


Figure 49. Photovoltaic Cell Amplifier


Figure 50. Low Input Voltage Comparator with Hysteresis


$$
\begin{aligned}
& \frac{\mathrm{R} 2}{\mathrm{R} 1}=\frac{\mathrm{R} 4}{\mathrm{R} 3} \text { (Critical to CMRR) } \\
& \mathrm{V}_{0}=1\left(+\frac{\mathrm{R} 4}{\mathrm{R} 3}\right)\left(\mathrm{V} 2-\mathrm{V} 1 \frac{\mathrm{R} 4}{\mathrm{R} 3}\right)
\end{aligned}
$$

For (V2 $\geq$ V1), V $>0$
Figure 52. High Input Impedance Differential Amplifier



Figure 54. Low Voltage Peak Detector


Figure 51. High Compliance Voltage to Sink Current Converter


Figure 53. Bridge Current Amplifier


Figure 55. High Frequency Pulse Width Modulation

## MC34071,2,4,A MC33071,2,4,A

GENERAL ADDITIONAL APPLICATIONS INFORMATION $\mathrm{V}_{\mathrm{S}}= \pm 15.0 \mathrm{~V}$


Figure 56. Second Order Low-Pass Active Filter


Figure 58. Fast Settling Inverter


Figure 60. Basic Noninverting Amplifier


Figure 57. Second Order High-Pass Active Filter


Figure 59. Basic Inverting Amplifier

$\mathrm{BW}_{\mathrm{p}}=200 \mathrm{kHz}$
$\mathrm{V}_{\mathrm{o}}=20 \mathrm{~V}_{\mathrm{pp}}$
$\mathrm{SR}=10 \mathrm{~V} / \mu \mathrm{s}$

Figure 61. Unity Gain Buffer ( $\mathrm{A}_{\mathrm{V}}=\boldsymbol{+ 1 . 0}$ )

## MC34071,2,4,A MC33071,2,4,A



Figure 62. High Impedance Differential Amplifier


Figure 63. Dual Voltage Doubler

MC34071,2,4,A MC33071,2,4,A

ORDERING INFORMATION

| Op Amp Function | Device | Operating Temperature Range | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| Single | MC34071P, MC34071AP <br> MC34071D, MC34071AD <br> MC34071DR2, MC34071ADR2 | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | DIP-8 SO-8 SO-8 / Tape \& Reel | 50 Units / Rail 98 Units / Rail 2500 Units / Tape \& Reel |
|  | MC33071P, MC33071AP <br> MC33071D, MC33071AD <br> MC33071DR2, MC33071ADR2 | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | DIP-8 SO-8 SO-8 / Tape \& Reel | 50 Units / Rail 98 Units / Rail 2500 Units / Tape \& Reel |
| Dual | MC34072P, MC34072AP <br> MC34072D, MC34072AD <br> MC34072DR2, MC34072ADR2 | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | $\begin{gathered} \hline \text { DIP-8 } \\ \text { SO-8 } \\ \text { SO-8 / Tape \& Reel } \end{gathered}$ | 50 Units / Rail 98 Units / Rail 2500 Units / Tape \& Reel |
|  | MC33072P, MC33072AP <br> MC33072D, MC33072AD <br> MC33072DR2, MC33072ADR2 | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | DIP-8 SO-8 SO-8 / Tape \& Reel | 50 Units / Rail 98 Units / Rail 2500 Units / Tape \& Reel |
|  | MC34072VD MC34072VDR2 MC34072VP | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | $\begin{gathered} \text { SO-8 } \\ \text { SO-8 / Tape \& Reel } \\ \text { DIP-8 } \end{gathered}$ | 98 Units / Rail <br> 2500 Units / Tape \& Reel 50 Units / Rail |
| Quad | MC34074P, MC34074AP <br> MC34074D, MC34074AD <br> MC34074DR2, MC34074ADR2 | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | DIP-14 SO-14 SO-14 / Tape \& Reel | 25 Units / Rail 55 Units / Rail 2500 Units / Tape \& Reel |
|  | MC33074P, MC33074AP <br> MC33074D, MC33074AD <br> MC33074DR2, MC33074ADR2 <br> MC33074DTB, MC33074ADTB <br> MC33074DTBR2, MC33074ADTBR2 | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | DIP-14 SO-14 SO-14 / Tape \& Reel TSSOP-14 TSSOP-14 / Tape \& Reel | 25 Units / Rail <br> 55 Units / Rail <br> 2500 Units / Tape \& Reel <br> 96 Units / Rail <br> 2500 Units / Tape \& Reel |
|  | MC34074VD MC34074VDR2 MC34074VP | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+125^{\circ} \mathrm{C}$ | $\begin{gathered} \text { SO-14 } \\ \text { SO-14 / Tape \& Reel } \\ \text { DIP-14 } \end{gathered}$ | 55 Units / Rail 2500 Units / Tape \& Reel 25 Units / Rail |

## MC34071，2，4，A MC33071，2，4，A

MARKING DIAGRAMS


|  | $\begin{gathered} \text { SO-14 } \\ \text { D SUFFIX } \\ \text { CASE 751A } \end{gathered}$ |  | TSSOP－14 DTB SUFFIX CASE 948G |  |
| :---: | :---: | :---: | :---: | :---: |
| $14$ | $14$ | $14$ | $\begin{gathered} 14 \\ \text { 日月 日果 } \end{gathered}$ | $\begin{aligned} & 14 \\ & \text { 日月 日果 } \end{aligned}$ |
| $\left\{\begin{array}{c} \left.\begin{array}{c} \text { MC3x074D } \\ 0 \\ \text { AWLYWW } \\ 1 \end{array} \right\rvert\,-\square \square \square \square \end{array}\right.$ | $\left\{\begin{array}{l} \text { MC3x074AD } \\ \text { O AWLYWW } \\ 1 \end{array}\right.$ | $\left\{\begin{array}{c} \text { MC34074VD } \\ \text { o AWLYWW } \\ 1 \quad \square \sqcup \square \sqcup \square \square \end{array}\right.$ | MC33 <br> 074 <br> ALYW <br> BUEZU日 <br> 1 | MC33 $074 A$ ALYW OUVEVEB 1 |
|  |  | $x \quad=3$ or 4 |  |  |
|  |  | A＝Assembly Location |  |  |
|  |  | WL，L＝Wafer Lot |  |  |
|  |  | YY，Y＝Year |  |  |
|  |  | WW，W＝Work Week |  |  |

## LM211, LM311

## Single Comparators

The ability to operate from a single power supply of 5.0 V to 30 V or $\pm 15 \mathrm{~V}$ split supplies, as commonly used with operational amplifiers, makes the LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the $\mathrm{V}_{\mathrm{CC}}$ or the $\mathrm{V}_{\mathrm{EE}}$ supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 V at currents to 50 mA . Thus the LM211/LM311 can be used to drive relays, lamps or solenoids.


Split Power Supply with Offset Balance



Load Referred to Positive Supply


Strobe Capability

Figure 1. Typical Comparator Design Configurations


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com
PIN CONNECTIONS

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| LM211D | SO-8 | 98 Units/Rail |
| LM211DR2 | SO-8 | 2500 Tape \& Reel |
| LM311D | SO-8 | 98 Units/Rail |
| LM311DR2 | SO-8 | 2500 Tape \& Reel |
| LM311N | PDIP-8 | 50 Units/Rail |

## LM211, LM311

MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | LM211 | LM311 | Unit |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Total Supply Voltage | $\mathrm{V}_{\mathrm{CC}}+\mathrm{V}_{\mathrm{EE}} \mathrm{l}$ | 36 | 36 | Vdc |  |  |
| Output to Negative Supply Voltage | $\mathrm{V}_{\mathrm{O}}-\mathrm{V}_{\mathrm{EE}}$ | 50 | 40 | Vdc |  |  |
| Ground to Negative Supply Voltage | $\mathrm{V}_{\mathrm{EE}}$ | 30 | 30 | Vdc |  |  |
| Input Differential Voltage | $\mathrm{V}_{\mathrm{ID}}$ | $\pm 30$ | $\pm 30$ | Vdc |  |  |
| Input Voltage (Note 2) | $\mathrm{V}_{\mathrm{in}}$ | $\pm 15$ | $\pm 15$ | Vdc |  |  |
| Voltage at Strobe Pin | - | $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{CC}}-5$ | $\mathrm{~V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{CC}}-5$ | Vdc |  |  |
| Power Dissipation and Thermal Characteristics <br> Plastic DIP <br> $\quad$ Derate Above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  |  |  |  |  |  |
| Operating Ambient Temperature Range | $\mathrm{P}_{\mathrm{D}}$ |  |  | mW |  |  |
| Operating Junction Temperature | $1 / \theta_{\mathrm{JA}}$ |  | 5.0 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |  |  |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -25 to +85 | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |  |  |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted [Note 1])

| Characteristic | Symbol | LM211 |  |  | LM311 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| $\begin{aligned} & \text { Input Offset Voltage (Note 3) } \\ & R_{S} \leq 50 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & R_{S} \leq 50 \mathrm{k} \Omega, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \end{aligned}$ | $\mathrm{V}_{10}$ |  | $0.7$ | $\begin{aligned} & 3.0 \\ & 4.0 \end{aligned}$ | - | $2.0$ | $\begin{aligned} & 7.5 \\ & 10 \end{aligned}$ | mV |
| Input Offset Current (Note 3) $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ $\mathrm{T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*}$ | 10 | - | $1.7$ | $\begin{aligned} & 10 \\ & 20 \end{aligned}$ | - | $1.7$ | $\begin{aligned} & 50 \\ & 70 \end{aligned}$ | nA |
| $\begin{aligned} & \text { Input Bias Current } \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }^{*}}{ }^{*} \end{aligned}$ | $I_{\text {IB }}$ | - | $45$ | $\begin{aligned} & 100 \\ & 150 \end{aligned}$ | - | $45$ | $\begin{aligned} & 250 \\ & 300 \end{aligned}$ | nA |
| Voltage Gain | $A_{V}$ | 40 | 200 | - | 40 | 200 | - | V/mV |
| Response Time (Note 4) |  | - | 200 | - | - | 200 | - | ns |
| Saturation Voltage $\begin{aligned} & \mathrm{V}_{\mathrm{ID}} \leq-5.0 \mathrm{mV}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{I D} \leq-10 \mathrm{mV}, \mathrm{I}_{\mathrm{O}}=50 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}} \geq 4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \\ & \mathrm{~V}_{\mathrm{ID}}<\leq 6.0 \mathrm{mV}, \mathrm{I}_{\text {sink }} \leq 8.0 \mathrm{~mA} \\ & \mathrm{~V}_{\text {ID }}<\leq 10 \mathrm{mV}, \mathrm{I}_{\text {sink }} \leq 8.0 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ |  | $\begin{gathered} 0.75 \\ - \\ 0.23 \end{gathered}$ | $\begin{gathered} 1.5 \\ - \\ 0.4 \end{gathered}$ |  | $\begin{gathered} - \\ 0.75 \\ - \\ 0.23 \end{gathered}$ | $\begin{gathered} - \\ 1.5 \\ - \\ 0.4 \end{gathered}$ | V |
| Strobe "On" Current (Note 5) | Is | - | 3.0 | - | - | 3.0 | - | mA |
| $\begin{aligned} & \text { Output Leakage Current } \\ & V_{I D} \geq 5.0 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {strobe }}=3.0 \mathrm{~mA} \\ & \mathrm{~V}_{I D} \geq 10 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\text {strobe }}=3.0 \mathrm{~mA} \\ & \mathrm{~V}_{I D} \geq 5.0 \mathrm{mV}, \mathrm{~V}_{\mathrm{O}}=35 \mathrm{~V}, \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*} \end{aligned}$ |  | - | $\begin{gathered} 0.2 \\ - \\ 0.1 \end{gathered}$ | $\begin{gathered} 10 \\ - \\ 0.5 \end{gathered}$ | - | $\overline{-}$ | $\frac{-}{50}$ | $\begin{aligned} & \mathrm{nA} \\ & \mathrm{nA} \\ & \mu \mathrm{~A} \end{aligned}$ |
| Input Voltage Range ( $\mathrm{T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}{ }^{*}$ ) | $\mathrm{V}_{\text {ICR }}$ | -14.5 | $\begin{gathered} -14.7 \text { to } \\ 13.8 \end{gathered}$ | +13.0 | -14.5 | $\begin{gathered} -14.7 \text { to } \\ 13.8 \end{gathered}$ | +13.0 | V |
| Positive Supply Current | $\mathrm{I}_{\mathrm{CC}}$ | - | +2.4 | +6.0 | - | +2.4 | +7.5 | mA |
| Negative Supply Current | $\mathrm{I}_{\text {EE }}$ | - | -1.3 | -5.0 | - | -1.3 | -5.0 | mA |

*LM211: $\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$
LM311: $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$

1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 V supply up to $\pm 15 \mathrm{~V}$ supplies.
2. This rating applies for $\pm 15 \mathrm{~V}$ supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 mA to 5.0 mA .

## LM211, LM311



Figure 2. Circuit Schematic


Figure 3. Input Bias Current versus Temperature


Figure 5. Input Bias Current versus Differential Input Voltage


Figure 4. Input Offset Current versus Temperature


Figure 6. Common Mode Limits versus Temperature

## LM211, LM311




Figure 12. Output Saturation Voltage versus Output Current


Figure 13. Output Leakage Current versus Temperature


Figure 14. Power Supply Current versus Supply Voltage


Figure 15. Power Supply Current versus Temperature

## APPLICATIONS INFORMATION



Figure 16. Improved Method of Adding Hysteresis Without Applying Positive Feedback to the Inputs


Figure 17. Conventional Technique for Adding Hysteresis

## TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high speed comparator such as the LM211 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with $0.1 \mu \mathrm{~F}$ disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high ( $1.0 \mathrm{k} \Omega$ to $100 \mathrm{k} \Omega$ ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM211 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 16.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a $0.01 \mu \mathrm{~F}$ capacitor ( C 1 ) between Pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 16. For the fastest response time, tie both balance pins to $\mathrm{V}_{\mathrm{CC}}$.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = $10 \mathrm{k} \Omega$, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM211 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM211, and a $0.01 \mu \mathrm{~F}$ capacitor should be installed across Pins 5 and 6 . If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM211.
A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 17, the feedback resistor of $510 \mathrm{k} \Omega$ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than $100 \Omega$ such as $50 \mathrm{k} \Omega$, it would not be practical to simply increase the value of the positive feedback resistor proportionally above $510 \mathrm{k} \Omega$ to maintain the same amount of hysteresis.
When both inputs of the LM211 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM211 so that positive feedback would be disruptive, the circuit of Figure 16 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 mV to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz . The positive-feedback signal across the $82 \Omega$ resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the $5.0 \mathrm{k} \Omega$ pot and $3.0 \mathrm{k} \Omega$ resistor as shown.

## LM211, LM311



Figure 18. Zero-Crossing Detector Driving CMOS Logic


Figure 19. Relay Driver with Strobe Capability

## NCS2200 Series

## Advance Information <br> Low Voltage Comparators

The NCS2200 series is an industry first sub-one volt, low power comparator family. These devices consume only $10 \mu \mathrm{~A}$ of supply current. They are guaranteed to operate at a low voltage of 0.85 V which allows them to be used in systems that require less than 1.0 V and is fully operational up to 6.0 V which makes it convenient to be used in both 3.0 V and 5.0 V systems. Additional features include no output phase inversion when transitioning in/out of tri-state mode, internal hysteresis which allows for clean output switching, and rail-to-rail input performance. The NCS2200 series are available in the tiny SOT23-5 and SOT23-6 package and feature two industry standard pinouts.

The NCS22201/3 Series in the SOT23-6 package features an enable function which can be externally controlled. This lowers current consumption to $1.8 \mu \mathrm{~A}$ and allows for users to implement these devices in power sensitive applications such as portable electronics.

## Features

- Operating Voltage of 0.85 V to 6.0 V
- Rail-to-rail Input/Output Performance
- Low Supply Current of $10 \mu \mathrm{~A}$
- No Phase Inversion/Glitchless transitioning in or out of Tri-State Mode
- Complementary or Open Drain Output Configuration
- Available with the Enable Function
- Tiny SOT23-5 and SOT23-6 Package


## Typical Applications

- Single Cell NiCd/NiMH Battery Powered Applications
- Window Comparator
- Portable Electronics
- Voltage Detector
- Zero-Crossing Detectors
- Personal Digital Assistants


This device contains 93 active transistors.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com
SOT23-5
(TSOP-5, SC59-5)
SN SUFFIX
CASE 483
SOT23-6
(TSOP-6, SC59-6)
SN SUFFIX
CASE 318G

## PIN CONNECTIONS



Style 1 Pinout (SN1T1)


Style 2 Pinout (SN2T1)
SOT23-5
(NCS2200, NCS2202)


Style 2 Pinout (SN2T1) SOT23-6
(NCS2201, NCS2203)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2666 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2666 of this data sheet.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage Range ( $\mathrm{V}_{\mathrm{CC}}$ to $\mathrm{V}_{\mathrm{EE}}$ ) | $\mathrm{V}_{\mathrm{S}}$ | 6.0 | V |
| Non-inverting/Inverting Input to $\mathrm{V}_{\mathrm{EE}}$ | - | -0.1 to (V $\left.\mathrm{V}_{\mathrm{CC}}+0.1\right)$ | V |
| Thermal Resistance, Junction to Air | $\mathrm{R}_{\text {өJA }}$ | 238 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\text {A }}$ | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Output Short Circuit Duration Time (Note 1) | ts | Indefinite | s |
| ESD Tolerance (Note 2) Human Body Model Machine Model | - | $\begin{gathered} 2000 \\ 200 \end{gathered}$ | V |

1. The maximum package power dissipation limit must not be exceeded.
$P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}$
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{V}_{\mathrm{CC}}=0.85 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.) (Note 3)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Hysteresis $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{HYS}}$ | - | $\pm 3.0$ | - | mV |
| Input Offset Voltage $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{10}$ | - | $\pm 0.5$ | $\pm 5.0$ | mV |
| Common Mode Voltage Range | $\mathrm{V}_{\mathrm{CM}}$ | $\mathrm{V}_{\mathrm{EE}}-0.1$ | - | $\mathrm{V}_{\mathrm{CC}}+0.1$ | V |
| Output Leakage Current | ILEAK | - | TBD | - | $\mu \mathrm{A}$ |
| Common Mode Rejection $\mathrm{V}_{\mathrm{CM}}=\mathrm{V}_{\mathrm{CC}}$ | CMRR | - | 80 | - | dB |
| Input Bias Current | IB | - | 0.001 | 10 | nA |
| Power Supply Rejection $\Delta \mathrm{V}_{\mathrm{S}}=2.575$ | PSRR | - | - | - | dB |
| $\begin{aligned} & \text { Supply Current } \\ & \mathrm{V}_{\mathrm{CC}}=0.85 \mathrm{~V} \\ & T_{A}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{C C}=6.0 \mathrm{~V} \\ & T_{A}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\mathrm{CC}}$ | - | 10 | - | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Output Voltage High } \\ & \mathrm{I}_{\text {source }}=7.0 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CC}}=0.85 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=3.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=6.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | - | $\mathrm{V}_{C C}-0.2$ | - | V |

3. The limits over the extended temperature range are guaranteed by design only.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{V}_{\mathrm{CC}}=0.85 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.) (Note 4)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage Low $\begin{aligned} \mathrm{I}_{\text {sink }} & =7.0 \mathrm{~mA} \\ \mathrm{~V}_{C C} & =0.85 \mathrm{~V} \\ T_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\ T_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =3.0 \mathrm{~V} \\ T_{A} & =25^{\circ} \mathrm{C} \\ T_{A} & =-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =6.0 \mathrm{~V} \\ T_{A} & =25^{\circ} \mathrm{C} \\ T_{A} & =-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | 0.2 | - | V |
| Propagation Delay 10 mV Overdrive, $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $\begin{aligned} & \mathrm{t}_{\mathrm{PHL}} \\ & \mathrm{t}_{\mathrm{PLH}} \end{aligned}$ | - | $\begin{aligned} & 1.1 \\ & 1.1 \end{aligned}$ | - | $\mu \mathrm{s}$ |
| Output Voltage Fall Time $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $\mathrm{t}_{\text {FALL }}$ | - | 50 | - | ns |
| Output Voltage Rise Time $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $t_{\text {RISE }}$ | - | 50 | - | ns |
| Power-up Time | tpu | - | 50 | 100 | $\mu \mathrm{s}$ |
| Tri-state Leakage Current | $\mathrm{I}_{\text {TRI-LEAK }}$ | - | 3.0 | - | nA |

ENABLE FUNCTION (NCS2201/3 only) ELECTRICAL CHARACTERISTICS
(For all values $\mathrm{V}_{\mathrm{CC}}=0.85 \mathrm{~V}$ to $6.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.) (Note 4)

| Enable Voltage (High) | $\mathrm{V}_{\mathrm{EN}(\mathrm{HIGH})}$ | - | - | 2.2 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Enable Voltage (Low) | $\mathrm{V}_{\mathrm{EN}(\mathrm{LOW})}$ | 1.1 | - | - | V |
| Enable Hysteresis | $\mathrm{V}_{\mathrm{ENHY}}$ | - | 75 | - | mV |
| Enable Current | $\mathrm{I}_{\mathrm{EN}}$ | - | 275 | - | nA |
| Enable Settling Time | $\mathrm{t}_{\mathrm{EN}(\mathrm{ON})}$ | - | 45 | - | $\mu \mathrm{s}$ |
| Disable Settling Time | $\mathrm{t}_{\mathrm{EN}(\mathrm{OFF})}$ | - | 2.0 | - | $\mu \mathrm{s}$ |

4. The limits over the extended temperature range are guaranteed by design only.


Figure 1. NCS2200 Series Supply Current vs. Temperature


Figure 2. NCS2200 Series Supply Current vs. Output Transition Frequency


Figure 3. NCS2200 Series Supply Current vs. Supply Voltage


Figure 5. NCS2200 Series Output Voltage Low State vs. Output Sink Current


Figure 6. NCS2200 Series Output Voltage Low State vs. Temperature


Figure 7. NCS2200 Series Output Voltage High State vs. Temperature


Figure 9. NCS2200 Series Output Response Time vs. Supply Voltage


Figure 11. NCS2200 Series Propagation Delay vs. Input Overdrive


Figure 8. NCS2200 Series Propagation Delay vs. Temperature


Figure 10. NCS2200 Series Propagation Delay vs. Input Overdrive

$10 \mu \mathrm{~s} /$ Div

Figure 12. NCS2200 Series Power-Up Delay


Figure 13. NCS2200 Series Input Common Mode Voltage Range vs. Supply Voltage

## OPERATING DESCRIPTION

The NCS2200 Series is an industry first sub-one volt, low power comparators. These devices consume only $10 \mu \mathrm{~A}$ of supply current while achieving a typical propagation delay of $1.1 \mu \mathrm{~s}$ at 10 mV overdrive. They are guaranteed to operate at a low voltage of 0.85 V up to 6.0 V . This is accomplished by the use of a modified analog CMOS process which implements depletion MOSFET devices. The common-mode input voltage range extends 0.1 V above the upper and lower rail. They are available in SOT23-5 (compatible with the TSOP-5) and SOT23-6 packages. The SOT23-6 has the enable function which can be externally controlled. It allows for lower current consumption of 1.8 $\mu \mathrm{A}$. This makes the devices suitable for implementation in power sensitive applications such as portable electronics. When the enable pin is at a low level, the output will remain at a high or low level. The output will not respond to any changes at the input pins.


Figure 15. NCS230xSNxT1 Complementary Output Configuration


Figure 14. NCS2200 Series Disabled Supply Current

Conversely, when the enable pin is at a high level, the output will respond to change at the input pins. The enable pin should be connected to VCC when not in use. In addition, with the added feature of internal hysteresis, this allows for greater noise immunity and clean output switching.

## Output Stage

The NCS2200/1 has a complementary output which drives rail-to-rail output swing. The NCS2202/3 has an open drain N -channel output that can be pulled up to 6.0 V (max) with an external pull- up resistor. This allows for mixed-voltage system applications These devices can operate up to an 7.0 mA load. The output stage is designed so that shoot through current is minimized while switching. This enhancement eliminates the need for bypass capacitors. There is no output phase reversal when switching in or out of tri-state mode.


Figure 16. NCS230xSNxT1 Open Drain Output Configuration


The oscillation frequency can be programmed as follows:

$$
f=\frac{1}{T}=\frac{1}{2.2 R_{X} C_{X}}
$$

Figure 17. Schmitt Trigger Oscillator


The resistor divider $R_{1}$ and $R_{2}$ can be used to set the magnitude of the input pulse. The pulse width is set by adjusting $C_{1}$ and $R_{3}$.

Figure 18. One-Shot Multivibrator

## NCS2200 Series



This circuit converts 5 V logic to 3 V logic. Using the NCS2202/3 allows for full 5 V logic swing without creating overvoltage on the 3 V logic input.

Figure 19. Logic Level Translator


Figure 20. Zero-Crossing Detector

## NCS2200 Series

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


SOT23-5


SOT23-6

# NCS2200 Series 

ORDERING INFORMATION

| Device | Pinout Style | Output Type | Package | Shipping |
| :--- | :---: | :---: | :---: | :---: |
| NCS2200SN1T1 | 1 | Complementary | SOT23-5 |  |
| NCS2200SN2T1 | 2 | Complementary | SOT23-5 |  |
| NCS2201SN1T1 | 1 | Complementary, Enable | SOT23-6 |  |
| NCS2201SN2T1 | 2 | Complementary, Enable | SOT23-6 |  |
| NCS2202SN1T1 | 1 | Open Drain | SOT23-5 |  |
| NCS2202SN2T1 | Open Drain | SOT23-5 |  |  |
| NCS2203SN1T1 | 1 | Open Drain, Enable | SOT23-6 Reel |  |
| NCS2203SN2T1 | 2 | Open Drain, Enable | SOT23-6 |  |

PIN CONNECTIONS


SOT23-6 (NCS2201, NCS2203)

MARKING DIAGRAMS

SOT23-5
SN SUFFIX
CASE 483


1

SOT23-6
SN SUFFIX
CASE 318G


1
$x=1$ for NCS2200SN1T1
J for NCS2200SN2T1 M for NCS2202SN1T1 N for NCS2202SN2T1
$Y=$ Year
W = Work Week
$x=K$ for NCS2201SN1T1 L for NCS2201SN2T1 O for NCS2203SN1T1 P for NCS2203SN2T1
Y = Year
W = Work Week

## NCS2300 Series

## Advance Information <br> High Voltage Comparators

The NCS2300 Series are ultra-low power comparators. These devices consume only $11 \mu \mathrm{~A}$ of supply current. They operate at a wide voltage range of 1.7 V to 12 V . Additional features include no output phase inversion when transitioning in/out of tri-state mode, internal hysteresis which allows for clean output switching, and rail-to-rail input performance. The NCS2300 Series are available in the tiny SOT23-5 or SOT23-6 package with two industry standard pinouts.

The NCS2301/3 Series in the SOT23-6 package features an enable function which can be externally controlled. This lowers current consumption to $1.8 \mu \mathrm{~A}$ and allows for users to implement these devices in power sensitive applications such as portable electronics.

## Features

- Rail-to-Rail Input/Output Performance
- Low Supply Current of $11 \mu \mathrm{~A}$
- No Phase Inversion/Glitchless transitioning in or out of Tri-State Mode
- Complementary or Open Drain Output Configuration
- Available with the Enable Function
- Tiny SOT23-5 and SOT23-6 Package


## Typical Applications

- Portable Electronics
- Window Comparator
- Voltage Detector
- Zero-Crossing Detectors
- Personal Digital Assistants


This device contains 121 active transistors.

[^38] herein are subject to change without notice.

ON Semiconductor ${ }^{\text {T }}$
http://onsemi.com
SOT23-5
(TSOP-5, SC59-5)
SN SUFFIX
CASE 483

PIN CONNECTIONS


Style 1 Pinout (SN1T1)


Style 2 Pinout (SN2T1)
SOT23-5


Style 1 Pinout (SN1T1)


Style 2 Pinout (SN2T1)
SOT23-6

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 2677 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2677 of this data sheet.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage Range ( $\mathrm{V}_{\mathrm{CC}}$ to $\left.\mathrm{V}_{\mathrm{EE}}\right)$ | $\mathrm{V}_{\mathrm{S}}$ | 12 | V |
| Non-inverting/Inverting Input to $\mathrm{V}_{\mathrm{EE}}$ | - | -0.1 to $\left(\mathrm{V}_{\mathrm{CC}}+0.1\right)$ | V |
| Thermal Resistance, Junction to Air | $\mathrm{R}_{\text {日JA }}$ | 248 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Output Short Circuit Duration Time (Note 1) | $\mathrm{t}_{\mathrm{S}}$ | Indefinite | s |
| ESD Tolerance (Note 2) <br> Human Body Model <br> Machine Model | - |  | V |

1. The maximum package power dissipation limit must not be exceeded.
$P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}$
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.) (Note 3)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Hysteresis $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{HYS}}$ | - | $\pm 2.5$ | - | mV |
| Input Offset Voltage $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{10}$ | - | $\pm 0.5$ | $\pm 5.0$ | mV |
| Common Mode Voltage Range $\mathrm{V}_{\mathrm{CC}}>2.5 \mathrm{~V}$ | $\mathrm{V}_{\text {CM }}$ | $\mathrm{V}_{\mathrm{EE}}-0.1$ | - | $V_{C C}+0.1$ | V |
| Output Leakage Current | ILEAK | - | - | 1.0 | $\mu \mathrm{A}$ |
| Common Mode Rejection | CMRR | - | 80 | - | dB |
| Input Bias Current | $I_{\text {IB }}$ | - | 0.001 | 10 | nA |
| Power Supply Rejection | PSRR | - | 80 | - | dB |
| Supply Current $\begin{aligned} & \mathrm{V}_{I N_{+}}>\mathrm{V}_{I N-} \\ & \mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | ICC | - | 11 | - | $\mu \mathrm{A}$ |
| Output Voltage High State $\begin{aligned} & \mathrm{I}_{\text {source }}=8.0 \mathrm{~mA} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | - | $\mathrm{V}_{C C}-0.3$ | - | V |

3. The limits over the extended temperature range are guaranteed by design only.

## NCS2300 Series

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.) (Note 4)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage Low State $\begin{aligned} \mathrm{I}_{\text {sink }} & =8.0 \mathrm{~mA} \\ \mathrm{~T}_{\mathrm{A}} & =25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =0^{\circ} \mathrm{C} \text { to } 70^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to } 105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | 0.3 | - | V |
| Propagation Delay 10 mV Overdrive, $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $\begin{aligned} & \mathrm{t}_{\mathrm{PHL}} \\ & \mathrm{t}_{\mathrm{PLH}} \end{aligned}$ | - | $\begin{aligned} & 1.4 \\ & 1.2 \end{aligned}$ | - | $\mu \mathrm{s}$ |
| Output Voltage Fall Time $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $\mathrm{t}_{\text {FALL }}$ | - | 32 | - | ns |
| Output Voltage Rise Time $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ | $\mathrm{t}_{\text {RISE }}$ | - | 23 | - | ns |
| Power-up Time | tpu | - | 35 | 100 | $\mu \mathrm{s}$ |
| Disabled Supply Current Enable Pin = 0 | ICC(OFF) | - | 1.8 | - | $\mu \mathrm{A}$ |
| Enable Voltage (High) | $\mathrm{V}_{\text {EN(HIGH) }}$ | - | - | 2.2 | V |
| Enable Voltage (Low) | $\mathrm{V}_{\text {EN(LOW }}$ | 1.1 | - | - | V |
| Enable Hysteresis | $\mathrm{V}_{\text {ENHYS }}$ | - | 75 | - | mV |
| Enable Pull-up Current | $\mathrm{I}_{\text {EN }}$ | - | 275 | - | nA |
| Tri-state Leakage Current | $I_{\text {TRIL-LEAK }}$ | - | 3.0 | - | nA |
| Enable Settling Time | $\mathrm{t}_{\text {EN(ON) }}$ | - | 45 | - | $\mu \mathrm{S}$ |
| Disable Settling Time | $\mathrm{t}_{\text {EN(OFF) }}$ | - | 2.0 | - | $\mu \mathrm{s}$ |

4. The limits over the extended temperature range are guaranteed by design only.


Figure 1. NCS2300 Series Supply Current vs. Temperature


Figure 2. NCS2300 Series Supply Current vs. Output Transition Frequency


Figure 3. NCS2300 Series Supply Current vs. Supply Voltage


Figure 5. NCS2300 Series Output Voltage Low State vs. Output Sink Current


Figure 4. NCS2300/1 Output Voltage High State vs. Output Source Current

Figure 6. NCS2300 Series Output Voltage Low State vs. Temperature


Figure 7. NCS2300 Series Output Voltage High State vs. Temperature


Figure 9. NCS2300 Series Output Response Time vs. Supply Voltage


Figure 11. NCS2300 Series Propagation Delay vs. Input Overdrive


Figure 8. NCS2300 Series Propagation Delay vs. Temperature


Figure 10. NCS2300 Series Propagation Delay vs. Input Overdrive

$10 \mu \mathrm{~s} /$ Div
Figure 12. NCS2300 Series Power-Up Delay


Figure 13. NCS2300 Series Input Common Mode Voltage vs. Supply Voltage

## OPERATING DESCRIPTION

The NCS2300 Series are ultra-low power comparators. These devices consume only $11 \mu \mathrm{~A}$ of supply current while achieving a typical propagation delay of $1.1 \mu \mathrm{~s}$ at 10 mV overdrive. They are guaranteed to operate at a low voltage of 1.7 V up to 12 V . This is accomplished by the use of a modified analog CMOS process which implements depletion MOSFET devices. The common-mode input voltage range extends 0.1 V above the upper and lower rail. They are available in SOT23-5 (compatible with the TSOP-5) and SOT23-6 packages. The SOT23-6 has the enable function which can be externally controlled. It allows for lower current consumption of $1.8 \mu \mathrm{~A}$. This makes the devices suitable for implementation in power sensitive applications such as portable electronics. When the enable pin is at a low level, the output will remain at a high or low level. The output will not respond to any changes at the input pins.


Figure 15. NCS230xSNxT1 Complementary Output Configuration


Figure 14. NCS2300 Series Disabled Supply Current

Conversely, when the enable pin is at a high level, the output will respond to change at the input pins. The enable pin should be connected to VCC when not in use. In addition, with the added feature of internal hysteresis, this allows for greater noise immunity and clean output switching.

## Output Stage

The NCS2300/1 has a complementary output which drives rail-to-rail output swing. The NCS2302/3 has an open drain N -channel output that can be pulled up to 12 V (max) with an external pull- up resistor. This allows for mixed-voltage system applications These devices can operate up to an 8.0 mA load. The output stage is designed so that shoot through current is minimized while switching. This enhancement eliminates the need for bypass capacitors. There is no output phase reversal when switching in or out of tri-state mode.


Figure 16. NCS230xSNxT1 Open Drain Output Configuration


The oscillation frequency can be programmed as follows:

$$
f=\frac{1}{T}=\frac{1}{2.2 R_{X} C_{X}}
$$

Figure 17. Schmitt Trigger Oscillator


The resistor divider $R_{1}$ and $R_{2}$ can be used to set the magnitude of the input pulse. The pulse width is set by adjusting $C_{1}$ and $R_{3}$.

Figure 18. One-Shot Multivibrator

## NCS2300 Series



This circuit converts 5 V logic to 3 V logic. In using the NCS2202/3 allows for full 5 V logic swing without creating overvoltage on the 3 V logic input.

Figure 19. Logic Level Translator


Figure 20. Zero-Crossing Detector

NCS2300 Series


Figure 21. First-Event Detector

## NCS2300 Series

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


SOT23-5


SOT23-6

## NCS2300 Series

ORDERING INFORMATION

| Device | Pinout Style | Output Type | Package | Shipping |
| :---: | :---: | :---: | :---: | :---: |
| NCS2300SN1T1 | 1 | Complementary | SOT23-5 | 3000 Tape \& Reel |
| NCS2300SN2T1 | 2 | Complementary | SOT23-5 |  |
| NCS2301SN1T1 | 1 | Complementary, Enable | SOT23-6 |  |
| NCS2301SN2T1 | 2 | Complementary, Enable | SOT23-6 |  |
| NCS2302SN1T1 | 1 | Open Drain | SOT23-5 |  |
| NCS2302SN2T1 | 2 | Open Drain | SOT23-5 |  |
| NCS2303SN1T1 | 1 | Open Drain, Enable | SOT23-6 |  |
| NCS2303SN2T1 | 2 | Open Drain, Enable | SOT23-6 |  |

## MARKING DIAGRAMS

SOT23-5
SN SUFFIX
CASE 483


1

SOT23-6
SN SUFFIX
CASE 318G


1
$x=A$ for NCS2300SN1T1 B for NCS2300SN2T1 E for NCS2302SN1T1 F for NCS2302SN2T1
$Y=$ Year
W = Work Week
x = C for NCS2301SN1T1 D for NCS2301SN2T1 G for NCS2303SN1T1 H for NCS2303SN2T1
Y = Year
W = Work Week

## LM393, LM293, LM2903, LM2903V, NCV2903

## Low Offset Voltage Dual Comparators

The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range-to-ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer, automotive, and industrial electronics.

- Wide Single-Supply Range: 2.0 Vdc to 36 Vdc
- Split-Supply Range: $\pm 1.0$ Vdc to $\pm 18$ Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance


Figure 1. Representative Schematic Diagram
(Diagram shown is for 1 comparator)


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


## PIN CONNECTIONS


(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| LM293D | SO-8 | 98 Units/Rail |
| LM293DR2 | SO-8 | 2500 Tape \& Reel |
| LM393D | SO-8 | 98 Units/Rail |
| LM393DR2 | SO-8 | 2500 Tape \& Reel |
| LM393N | PDIP-8 | 50 Units/Rail |
| LM2903D | SO-8 | 98 Units/Rail |
| LM2903DR2 | SO-8 | 2500 Tape \& Reel |
| LM2903N | PDIP-8 | 50 Units/Rail |
| LM2903VD | SO-8 | 98 Units/Rail |
| LM2903VDR2 | SO-8 | 2500 Tape \& Reel |
| LM2903VN | PDIP-8 | 50 Units/Rail |
| NCV2903DR2 | SO-8 | 2500 Tape \& Reel |

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2683 of this data sheet.

## LM393, LM293, LM2903, LM2903V, NCV2903

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $V_{\text {CC }}$ | +36 or $\pm 18$ | Vdc |
| Input Differential Voltage Range | $V_{\text {IDR }}$ | 36 | Vdc |
| Input Common Mode Voltage Range | $V_{\text {ICR }}$ | -0.3 to +36 | Vdc |
| Output Short Circuit-to-Ground Output Sink Current (Note 1) | $\begin{aligned} & I_{\mathrm{SC}} \\ & I_{\text {Sink }} \end{aligned}$ | $\begin{gathered} \text { Continuous } \\ 20 \end{gathered}$ | mA |
| Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Derate above $25^{\circ} \mathrm{C}$ | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ 1 / \mathrm{R}_{\theta \mathrm{JJA}} \end{gathered}$ | $\begin{gathered} 570 \\ 5.7 \end{gathered}$ | $\begin{gathered} \mathrm{mW} \\ \mathrm{~mW} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Operating Ambient Temperature Range <br> LM293 <br> LM393 <br> LM2903 <br> LM2903V, NCV2903 | $\mathrm{T}_{\mathrm{A}}$ | $\begin{aligned} & -25 \text { to }+85 \\ & 0 \text { to }+70 \\ & -40 \text { to }+105 \\ & -40 \text { to }+125 \end{aligned}$ | ${ }^{\circ} \mathrm{C}$ |
| Maximum Operating Junction Temperature LM393, 2903, LM2903V <br> LM293, NCV2903 | $\mathrm{T}_{\mathrm{J} \text { (max) }}$ | $\begin{aligned} & 150 \\ & 150 \end{aligned}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. The maximum output current may be as high as 20 mA , independent of the magnitude of $\mathrm{V}_{\mathrm{CC}}$, output short circuits to $\mathrm{V}_{\mathrm{CC}}$ can cause excessive heating and eventual destruction.

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{Vdc}, \mathrm{T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }}$, unless otherwise noted.)

| Characteristic | Symbol | LM293, LM393 |  |  | LM2903, LM2903V |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage (Note 3) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{V}_{10}$ | - | $\pm 1.0$ - | $\begin{gathered} \pm 5.0 \\ 9.0 \end{gathered}$ |  | $\begin{gathered} \pm 2.0 \\ 9.0 \end{gathered}$ | $\begin{gathered} \pm 7.0 \\ 15 \end{gathered}$ | mV |
| Input Offset Current $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }} \end{aligned}$ | 10 |  | $\pm 5.0$ - | $\begin{array}{r}  \pm 50 \\ \pm 150 \\ \hline \end{array}$ |  | $\begin{array}{r}  \pm 5.0 \\ \pm 50 \\ \hline \end{array}$ | $\begin{gathered} \pm 50 \\ \pm 200 \end{gathered}$ | nA |
| Input Bias Current (Note 4) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }} \end{aligned}$ | $I_{\text {IB }}$ |  | 25 | $\begin{aligned} & 250 \\ & 400 \\ & \hline \end{aligned}$ |  | $\begin{gathered} 25 \\ 200 \\ \hline \end{gathered}$ | $\begin{aligned} & 250 \\ & 500 \\ & \hline \end{aligned}$ | nA |
| Input Common Mode Voltage Range (Note 4) $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }} \end{aligned}$ | VICR | $0$ | - | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}-1.5 \\ & \mathrm{~V}_{\mathrm{CC}}-2.0 \end{aligned}$ |  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}-1.5 \\ & \mathrm{~V}_{\mathrm{CC}}-2.0 \\ & \hline \end{aligned}$ | V |
| Voltage Gain $\mathrm{R}_{\mathrm{L}} \geq 15 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | Avol | 50 | 200 | - | 25 | 200 | - | V/mV |
| Large Signal Response Time $V_{\text {in }}=$ TTL Logic Swing, $\mathrm{V}_{\text {ref }}=1.4 \mathrm{Vdc}$ $\mathrm{V}_{\mathrm{RL}}=5.0 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | - | 300 | - | - | 300 | - | ns |
| Response Time (Note 6) $\mathrm{V}_{\mathrm{RL}}=5.0 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | ${ }_{\text {t }}^{\text {tin }}$ | - | 1.3 | - | - | 1.5 | - | $\mu \mathrm{s}$ |
| Input Differential Voltage (Note 7) All $\mathrm{V}_{\text {in }} \geq$ Gnd or V - Supply (if used) | $\mathrm{V}_{\text {ID }}$ | - | - | $\mathrm{V}_{\mathrm{CC}}$ | - | - | $\mathrm{V}_{\mathrm{CC}}$ | V |
| Output Sink Current $\mathrm{V}_{\mathrm{in}} \geq 1.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{in+}}=0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{O}} \leq 1.5 \mathrm{Vdc} \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\mathrm{I}_{\text {Sink }}$ | 6.0 | 16 | - | 6.0 | 16 | - | mA |
| Output Saturation Voltage $\begin{aligned} & \mathrm{V}_{\text {in }} \geq 1.0 \mathrm{Vdc}, \mathrm{~V}_{\text {in }+}=0, \mathrm{I}_{\text {Sink }} \leq 4.0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | 150 | $\begin{aligned} & 400 \\ & 700 \\ & \hline \end{aligned}$ | - | $200$ | $\begin{aligned} & 400 \\ & 700 \\ & \hline \end{aligned}$ | mV |
| $\begin{aligned} & \text { Output Leakage Current } \\ & \mathrm{V}_{\text {in- }}=0 \mathrm{~V}, \mathrm{~V}_{\text {in }+} \geq 1.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{O}}=5.0 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~V}_{\text {in- }}=0 \mathrm{~V}, \mathrm{~V}_{\text {in }} \geq 1.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{O}}=30 \mathrm{Vdc}, \\ & \mathrm{~T}_{\text {low }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\text {high }} \end{aligned}$ | ${ }^{\text {lOL }}$ | - | $0.1$ | $1000$ | - | $0.1$ | $1000$ | nA |
| Supply Current <br> $R_{L}=\infty$ Both Comparators, $T_{A}=25^{\circ} \mathrm{C}$ <br> $\mathrm{R}_{\mathrm{L}}=\infty$ Both Comparators, $\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}$ | $I_{\text {cc }}$ | - | $0.4$ | $\begin{aligned} & 1.0 \\ & 2.5 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 1.0 \\ & 2.5 \\ & \hline \end{aligned}$ | mA |

LM293 $\mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ} \mathrm{C}$
LM393 T $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
LM2903 $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}$
$\mathrm{LM} 2903 \mathrm{~V} \mathrm{~T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
NCV2903 $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
2. The maximum output current may be as high as 20 mA , independent of the magnitude of $\mathrm{V}_{\mathrm{CC}}$, output short circuits to $\mathrm{V}_{\mathrm{CC}}$ can cause excessive heating and eventual destruction.
3. At output switch point, $\mathrm{V}_{\mathrm{O}} \simeq 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}}=0 \Omega$ with $\mathrm{V}_{\mathrm{Cc}}$ from 5.0 Vdc to 30 Vdc , and over the full input common mode range ( 0 V to $\mathrm{V}_{\mathrm{CC}}=-1.5 \mathrm{~V}$ ).
4. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
5. Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is $\mathrm{V}_{\mathrm{CC}}-1.5 \mathrm{~V}$.
6. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
7. The comparator will exhibit proper output state if one of the inputs becomes greater than $\mathrm{V}_{\mathrm{CC}}$, the other input must remain within the common mode range. The low input state must not be less than -0.3 V of ground or minus supply.

LM293/393


Figure 2. Input Bias Current versus Power Supply Voltage


Figure 4. Output Saturation Voltage versus Output Sink Current


Figure 6. Power Supply Current versus Power Supply Voltage

LM2903


Figure 3. Input Bias Current versus Power Supply Voltage


Figure 5. Output Saturation Voltage versus Output Sink Current


Figure 7. Power Supply Current versus Power Supply Voltage

## LM393, LM293, LM2903, LM2903V, NCV2903

## APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions $\left(\mathrm{V}_{\mathrm{OL}}\right.$ to $\left.\mathrm{V}_{\mathrm{OH}}\right)$. To alleviate this situation, input resistors $<10 \mathrm{k} \Omega$ should be used.


D1 prevents input from going negative by more than 0.6 V .

$$
\mathrm{R} 1+\mathrm{R} 2=\mathrm{R} 3
$$

$R 3 \leq \frac{R 5}{10}$ for small error in zero crossing.
Figure 8. Zero Crossing Detector (Single Supply)


Figure 10. Free-Running Square-Wave Oscillator

The addition of positive feedback $(<10 \mathrm{mV})$ is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3 V should not be used.


Figure 9. Zero Crossing Detector (Split Supply)


Figure 11. Time Delay Generator


Figure 12. Comparator with Hysteresis

# LM393，LM293，LM2903，LM2903V，NCV2903 

MARKING DIAGRAMS

PDIP－8
N SUFFIX
CASE 626

|  | ${ }^{8}$ |
| :---: | :---: |
| $\begin{gathered} \text { LM393N } \\ \text { AWL } \\ \text { OYWW } \end{gathered}$ | LM2903N AWL YYWW |
| 1甘甘甘 | 1甘甘甘 |



$$
\begin{array}{ll}
\mathrm{X} & =2 \text { or } 3 \\
\mathrm{~A} & =\text { Assembly Location } \\
\mathrm{WL}, \mathrm{~L} & =\text { Wafer Lot } \\
\mathrm{YY}, \mathrm{Y} & =\text { Year } \\
\mathrm{WW}, \mathrm{~W} & =\text { Work Week } \\
\text { *This marking diagram also applies to NCV2903. }
\end{array}
$$

## LM339, LM239, LM2901, <br> LM2901V, NCV2901, MC3302

## Single Supply Quad Comparators

These comparators are designed for use in level detection, low-level sensing and memory applications in consumer, automotive, and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: $\pm 5.0 \mathrm{nA}$ (Typ)
- Low Input Offset Voltage
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Power Supply Voltage } \\ & \text { LM239/LM339/LM2901, V } \\ & \text { MC3302 } \end{aligned}$ | $\mathrm{V}_{\mathrm{CC}}$ | $\begin{aligned} & +36 \text { or } \pm 18 \\ & +30 \text { or } \pm 15 \end{aligned}$ | Vdc |
| $\begin{aligned} & \text { Input Differential Voltage Range } \\ & \text { LM239/LM339/LM2901, V } \\ & \text { MC3302 } \end{aligned}$ | $V_{\text {IDR }}$ | $\begin{aligned} & 36 \\ & 30 \end{aligned}$ | Vdc |
| Input Common Mode Voltage Range | VICMR | -0.3 to $\mathrm{V}_{\mathrm{CC}}$ | Vdc |
| Output Short Circuit to Ground (Note 1) | ISC | Continuous |  |
| Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Plastic Package <br> Derate above $25^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | $\begin{aligned} & 1.0 \\ & 8.0 \end{aligned}$ | $\begin{gathered} \mathrm{W} \\ \mathrm{~mW} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| ```Operating Ambient Temperature Range LM239 MC3302 LM2901 LM2901V, NCV2901 LM339``` | $\mathrm{T}_{\mathrm{A}}$ | $\begin{gathered} -25 \text { to }+85 \\ -40 \text { to }+85 \\ -40 \text { to }+105 \\ -40 \text { to }+125 \\ 0 \text { to }+70 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. The maximum output current may be as high as 20 mA , independent of the magnitude of $\mathrm{V}_{\mathrm{CC}}$. Output short circuits to $\mathrm{V}_{\mathrm{CC}}$ can cause excessive heating and eventual destruction.

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PIN CONNECTIONS

(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2689 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2689 of this data sheet.


NOTE: Diagram shown is for 1 comparator.
Figure 1. Circuit Schematic

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Characteristic | Symbol | LM239/339 |  |  | LM2901/2901V |  |  | MC3302 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage (Note 3.) | $\mathrm{V}_{10}$ | - | $\pm 2.0$ | $\pm 5.0$ | - | $\pm 2.0$ | $\pm 7.0$ | - | $\pm 3.0$ | $\pm 20$ | mVdc |
| Input Bias Current (Notes 3., 4.) (Output in Analog Range) | IB | - | 25 | 250 | - | 25 | 250 | - | 25 | 500 | nA |
| Input Offset Current (Note 3.) | $\mathrm{I}_{10}$ | - | $\pm 5.0$ | $\pm 50$ | - | $\pm 5.0$ | $\pm 50$ | - | $\pm 3.0$ | $\pm 100$ | nA |
| Input Common Mode Voltage Range | $\mathrm{V}_{\text {ICMR }}$ | 0 | - | $\begin{gathered} \mathrm{V}_{\mathrm{CC}} \\ -1.5 \end{gathered}$ | 0 | - | $\begin{gathered} \mathrm{V}_{\mathrm{CC}} \\ -1.5 \end{gathered}$ | 0 | - | $\begin{array}{r} \hline \mathrm{V}_{\mathrm{CC}} \\ -1.5 \end{array}$ | V |
| $\begin{aligned} & \text { Supply Current } \\ & \begin{array}{l} R_{L}=\infty \text { (For All Comparators) } \\ R_{L}=\infty, \mathrm{V}_{\mathrm{CC}}=30 \mathrm{Vdc} \\ \hline \end{array} \end{aligned}$ | Icc |  | $\begin{aligned} & 0.8 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.5 \end{aligned}$ |  | $\begin{aligned} & 0.8 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.5 \end{aligned}$ |  | $\begin{aligned} & 0.8 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.5 \end{aligned}$ | mA |
| Voltage Gain $\mathrm{R}_{\mathrm{L}} \geq 15 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{Vdc}$ | Avol | 50 | 200 | - | 25 | 100 | - | 25 | 100 | - | V/mV |
| $\begin{aligned} & \text { Large Signal Response Time } \\ & V_{I}=T T L \text { Logic Swing, } \\ & V_{\text {ref }}=1.4 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{RL}}=5.0 \mathrm{Vdc}, \\ & \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega \end{aligned}$ | - | - | 300 | - | - | 300 | - | - | 300 | - | ns |
| Response Time (Note 5.) $\mathrm{V}_{\mathrm{RL}}=5.0 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=5.1 \mathrm{k} \Omega$ | - | - | 1.3 | - | - | 1.3 | - | - | 1.3 | - | $\mu \mathrm{S}$ |
| Output Sink Current $\begin{aligned} & \mathrm{V}_{1}(-) \geq+1.0 \mathrm{Vdc}, \mathrm{~V}_{1}(+)=0, \\ & \mathrm{~V}_{\mathrm{O}} \leq 1.5 \mathrm{Vdc} \end{aligned}$ | $I_{\text {Sink }}$ | 6.0 | 16 | - | 6.0 | 16 | - | 6.0 | 16 | - | mA |
| $\begin{aligned} & \text { Saturation Voltage } \\ & \mathrm{V}_{\mathrm{l}}(-) \geq+1.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{l}}(+)=0, \\ & \mathrm{I}_{\text {sink }} \leq 4.0 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\text {sat }}$ | - | 130 | 400 | - | 130 | 400 | - | 130 | 500 | mV |
| Output Leakage Current $\begin{aligned} & \mathrm{V}_{\mathrm{l}}(+) \geq+1.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{l}}(-)=0, \\ & \mathrm{~V}_{\mathrm{O}}=+5.0 \mathrm{Vdc} \end{aligned}$ | ${ }_{\text {lOL }}$ | - | 0.1 | - | - | 0.1 | - | - | 0.1 | - | nA |

2. (LM239) $T_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ}$
(LM339) $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
(MC3302) $T_{\text {low }}=-40^{\circ} \mathrm{C}, T_{\text {high }}=+85^{\circ} \mathrm{C}$
$\left(\right.$ LM2901 ) $T_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ}$
(LM2901V) $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
(NCV2901) $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
3. At the output switch point, $\mathrm{V}_{\mathrm{O}} \simeq 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}} \leq 100 \Omega 5.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{CC}} \leq 30 \mathrm{Vdc}$, with the inputs over the full common mode range ( 0 Vdc to $\left.\mathrm{V}_{\mathrm{Cc}}-1.5 \mathrm{Vdc}\right)$.
4. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
5. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

PERFORMANCE CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ [Note 6.])

| Characteristic | Symbol | LM239/339 |  |  | LM2901/2901V |  |  | MC3302 |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |  |
| Input Offset Voltage (Note 7.) | $\mathrm{V}_{10}$ | - | - | $\pm 9.0$ | - | - | $\pm 15$ | - | - | $\pm 40$ | mVdc |
| Input Bias Current (Notes 7., 8.) (Output in Analog Range) | $I_{\text {IB }}$ | - | - | 400 | - | - | 500 | - | - | 1000 | nA |
| Input Offset Current (Note 7.) | $\mathrm{I}_{10}$ | - | - | $\pm 150$ | - | - | $\pm 200$ | - | - | $\pm 300$ | nA |
| Input Common Mode Voltage Range | VICMR | 0 | - | $\begin{gathered} \hline \mathrm{V}_{\mathrm{CC}} \\ -2.0 \end{gathered}$ | 0 | - | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}} \\ & -2.0 \end{aligned}$ | 0 | - | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{cc}} \\ & -2.0 \end{aligned}$ | V |
| $\begin{aligned} & \text { Saturation Voltage } \\ & \mathrm{V}_{\mathrm{l}}(-) \geq+1.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{l}}(+)=0, \\ & \mathrm{I}_{\text {sink }} \leq 4.0 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\text {sat }}$ | - | - | 700 | - | - | 700 | - | - | 700 | mV |
| $\begin{aligned} & \text { Output Leakage Current } \\ & \mathrm{V}_{\mathrm{I}}(+) \geq+1.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{l}}(-)=0, \\ & \mathrm{~V}_{\mathrm{O}}=30 \mathrm{Vdc} \end{aligned}$ | ${ }_{\text {loL }}$ | - | - | 1.0 | - | - | 1.0 | - | - | 1.0 | $\mu \mathrm{A}$ |
| Differential Input Voltage All $V_{1} \geq 0 \mathrm{Vdc}$ | $\mathrm{V}_{\text {ID }}$ | - | - | $\mathrm{V}_{\mathrm{CC}}$ | - | - | $\mathrm{V}_{\text {CC }}$ | - | - | $\mathrm{V}_{\mathrm{CC}}$ | Vdc |

6. $(\mathrm{LM} 239) \mathrm{T}_{\text {low }}=-25^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+85^{\circ}$
(LM339) $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$
(MC3302) $T_{\text {low }}=-40^{\circ} \mathrm{C}, T_{\text {high }}=+85^{\circ} \mathrm{C}$
(LM2901) $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+105^{\circ}$
(LM2901V) $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$
(NCV2901) $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.
7. At the output switch point, $\mathrm{V}_{\mathrm{O}} \simeq 1.4 \mathrm{Vdc}, \mathrm{R}_{\mathrm{S}} \leq 100 \Omega 5.0 \mathrm{Vdc} \leq \mathrm{V}_{\mathrm{CC}} \leq 30 \mathrm{Vdc}$, with the inputs over the full common mode range ( 0 Vdc to $\left.\mathrm{V}_{\mathrm{CC}}-1.5 \mathrm{Vdc}\right)$.
8. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
9. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.


Figure 2. Inverting Comparator with Hystersis

$\mathrm{R} 2 \approx \mathrm{R} 1 / / \mathrm{R}_{\mathrm{ref}}$
Amount of Hysteresis $\mathrm{V}_{\mathrm{H}}$
$\mathrm{V}_{\mathrm{H}}=\frac{\mathrm{R} 2}{\mathrm{R} 2+\mathrm{R} 3}\left[\left(\mathrm{~V}_{\mathrm{O}(\text { max })}-\mathrm{V}_{\mathrm{O}(\text { min })}\right]\right.$

Figure 3. Noninverting Comparator with Hysteresis

Typical Characteristics
( $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ (each comparator) unless otherwise noted.)


Figure 4. Normalized Input Offset Voltage


Figure 5. Input Bias Current


Figure 6. Output Sink Current versus Output Saturation Voltage


Figure 7. Driving Logic


Figure 8. Squarewave Oscillator

## LM339, LM239, LM2901, LM2901V, NCV2901, MC3302

## APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions $\left(\mathrm{V}_{\mathrm{OL}}\right.$ to $\left.\mathrm{V}_{\mathrm{OH}}\right)$. To alleviate this situation input resistors $<10 \mathrm{k} \Omega$ should be used. The


D1 prevents input from going negative by more than 0.6 V .

$$
\mathrm{R} 1+\mathrm{R} 2=\mathrm{R} 3
$$

$R 3 \leq \frac{R 5}{10}$ for small error in zero crossing

Figure 9. Zero Crossing Detector (Single Supply)
addition of positive feedback ( $<10 \mathrm{mV}$ ) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than -300 mV should not be used.
$\mathrm{V}_{\text {in(min) }} \approx 0.4 \mathrm{~V}$ peak for $1 \%$ phase distortion $(\Delta \Theta)$.


Figure 10. Zero Crossing Detector (Split Supplies)

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| LM239D | SO-14 | 55 Units/Rail |
| LM239DR2 | SO-14 | 2500 Units/Tape \& Reel |
| LM239N | PDIP-14 | 25 Units/Rail |
| LM339D | SO-14 | 55 Units/Rail |
| LM339DR2 | SO-14 | 2500 Units/Tape \& Reel |
| LM339N | PDIP-14 | 25 Units/Rail |
| LM2901D | SO-14 | 55 Units/Rail |
| LM2901DR2 | SO-14 | 2500 Units/Tape \& Reel |
| LM2901N | PDIP-14 | 25 Units/Rail |
| LM2901VDR2 | SO-14 | 2500 Units/Tape \& Reel |
| LM2901VN | PDIP-14 | 25 Units/Rail |
| NCV2901DR2 | SO-14 | 2500 Units/Tape \& Reel |
| MC3302D | SO-14 | 55 Units/Rail |
| MC3302DR2 | SO-14 | 2500 Units/Tape \& Reel |
| MC3302P | PDIP-14 | 25 Units/Rail |

## MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY, $Y=$ Year
WW = Work Week
*This marking diagram also applies to NCV2901.

## Overvoltage Crowbar Sensing Circuit

This overvoltage protection circuit (OVP) protects sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. The device senses the overvoltage condition and quickly "crowbars" or short circuits the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

The protection voltage threshold is adjustable and the MC3423 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

## MC3423

## OVERVOLTAGE SENSING CIRCUIT

## SEMICONDUCTOR TECHNICAL DATA

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Differential Power Supply Voltage | $\mathrm{V}_{\mathrm{Cc}}-\mathrm{V}_{\mathrm{EE}}$ | 40 | Vdc |
| Sense Voltage (1) | $\mathrm{V}_{\text {Sense1 }}$ | 6.5 | Vdc |
| Sense Voltage (2) | $\mathrm{V}_{\text {Sense2 }}$ | 6.5 | Vdc |
| Remote Activation Input Voltage | $\mathrm{V}_{\text {act }}$ | 7.0 | Vdc |
| Output Current | $\mathrm{I}_{\mathrm{O}}$ | 300 | mA |
| Operating Ambient Temperature <br> Range | $\mathrm{T}_{\mathrm{A}}$ | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## Simplified Application



## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| MC 3423 D | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | $\mathrm{SO}-8$ |
| MC 3423 P 1 |  | Plastic DIP |

ELECTRICAL CHARACTERISTICS $\left(5.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}} \leq 36 \mathrm{~V}, \mathrm{~T}_{\text {low }}<\mathrm{T}_{\mathrm{A}}, \mathrm{T}_{\text {high }}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage Range | $\mathrm{V}_{\text {CC }}-\mathrm{V}_{\mathrm{EE}}$ | 4.5 | - | 40 | Vdc |
| Output Voltage $\left(I_{\mathrm{O}}=100 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{O}}$ | $\mathrm{V}_{\mathrm{CC}}-2.2$ | $\mathrm{V}_{\text {CC }}-1.8$ | - | Vdc |
| Indicator Output Voltage $\left(\mathrm{l}_{\mathrm{O}(\mathrm{lnd})}=1.6 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {OL }}(\mathrm{lnd})$ | - | 0.1 | 0.4 | Vdc |
| Sense Trip Voltage $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $V_{\text {Sense1 }}$, <br> $V_{\text {Sense2 }}$ | 2.45 | 2.6 | 2.75 | Vdc |
| Temperature Coefficient of $\mathrm{V}_{\text {Sense1 }}$ (Figure 2) | TCV $\mathrm{S}^{1}$ | - | 0.06 | - | \%/ ${ }^{\circ} \mathrm{C}$ |
| Remote Activation Input Current $\begin{aligned} & \left(\mathrm{V}_{I H}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}=5.0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}=5.0 \mathrm{~V}\right) \end{aligned}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{H}} \\ & \mathrm{I}_{\mathrm{IL}} \end{aligned}$ | - | $\begin{gathered} 5.0 \\ -120 \end{gathered}$ | $\begin{gathered} 40 \\ -180 \end{gathered}$ | $\mu \mathrm{A}$ |
| Source Current | $I_{\text {Source }}$ | 0.1 | 0.2 | 0.3 | mA |
| Output Current Risetime $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\mathrm{r}}$ | - | 400 | - | $\mathrm{mA} / \mathrm{\mu s}$ |
| Propagation Delay Time $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{t}_{\mathrm{pd}}$ | - | 0.5 | - | $\mu \mathrm{s}$ |
| Supply Current | ID | - | 6.0 | 10 | mA |

NOTES: $\mathrm{T}_{\text {low }}$ to $\mathrm{T}_{\text {high }}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$


Figure 1. Representative Block Diagram


Figure 2. Sense Voltage Test Circuit

$\mathrm{V}_{\text {trip }}=\mathrm{V}_{\text {ref }}\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right) \approx 2.6 \mathrm{~V}\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right)$
$\mathrm{R} 2 \leq 10 \mathrm{k} \Omega$ for minimum drift

For minimum value of $R_{G}$, see Figure 9 .
*See text for explanation.

Figure 3. Basic Circuit Configuration


$$
\begin{aligned}
& \mathrm{C}_{1}>\frac{\mathrm{R}_{\mathrm{S}}}{\mathrm{R}_{1} \mathrm{R}_{2}}\left(\mathrm{R}_{1}+\mathrm{R}_{2}\right) 10 \mu \mathrm{~F} \\
& \mathrm{R}_{\mathrm{S}}=\left(\frac{\mathrm{VS}-10}{25}\right) \mathrm{k} \Omega \\
& \mathrm{~V}_{\text {trip }}=\mathrm{V}_{\text {ref }}\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right) \approx 2.6 \mathrm{~V}\left(1+\frac{\mathrm{R} 1}{\mathrm{R} 2}\right) \\
& * \mathrm{R} 2 \leq 10 \mathrm{k} \Omega
\end{aligned}
$$

Q1: $\mathrm{V}_{\mathrm{S}} \leq 50 \mathrm{~V}$; 2N6504 or equivalent $\mathrm{V}_{\mathrm{S}} \leq 100 \mathrm{~V}$; 2N6505 or equivalent $\mathrm{V}_{\mathrm{S}} \leq 200 \mathrm{~V}$; 2N6506 or equivalent $\mathrm{V}_{\mathrm{S}} \leq 400 \mathrm{~V}$; 2 N 6507 or equivalent $\mathrm{V}_{\mathrm{S}} \leq 600 \mathrm{~V} ; 2 \mathrm{~N} 6508$ or equivalent $\mathrm{V}_{\mathrm{S}} \leq 800 \mathrm{~V}$; 2N6509 or equivalent

Figure 4. Circuit Configuration for Supply Voltage Above 36 V


R3 $\geq \frac{V_{\text {trip }}}{10 \mathrm{~mA}}$


$$
v_{10} \square
$$

$$
\mathrm{t}_{\mathrm{d}}=\frac{\mathrm{V}_{\text {ref }}}{I_{\text {source }}} \times \mathrm{C} \approx\left[12 \times 10^{3}\right] \mathrm{C}
$$

(See Figure 10)

Figure 5. Basic Configuration for Programmable Duration
of Overvoltage Condition Before Trip

## APPLICATION INFORMATION

## Basic Circuit Configuration

The basic circuit configuration of the MC3423 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V , and in Figure 4 for trip voltages above 36 V . The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, $\mathrm{R}_{\mathrm{G}}$, is given in Figure 9. Using this value of $\mathrm{R}_{\mathrm{G}}$, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423. If lower output currents are required, $\mathrm{R}_{\mathrm{G}}$ can be increased in value. The switch, S 1 , shown in Figure 3 may be used to reset the crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

The circuit configurations shown in Figures 3 and 4 will have a typical propagating delay of $1.0 \mu \mathrm{~s}$. If faster operation is desired, Pin 3 may be connected to Pin 2 with Pin 4 left floating. This will result in decreasing the propagating delay to approximately $0.5 \mu \mathrm{~s}$ at the expense of a slightly increased TC for the trip voltage value.

## Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping

In many instances, the MC3423 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from Pin 3 to $\mathrm{V}_{\mathrm{EE}}$. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When $\mathrm{V}_{\mathrm{CC}}$ rises above the trip point set by R1 and R2, an internal current source (Pin 4) begins charging the capacitor, C, connected to Pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate $\cong 10$ times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds $\mathrm{V}_{\mathrm{Z} 1}+1.4 \mathrm{~V}$.


Figure 6. Configuration for Programmable Duration of Overvoltage Condition Before Trip/With Immediate Trip at High Overvoltages

## Additional Features

## 1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423. This output is an open collector transistor which saturates when the OVP is activated. In addition, it can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

## 2. Remote Activation Input

Another feature of the MC3423 is its remote activation input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V , the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V , the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that Pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423 can be used to activate another MC3423 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (Pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.


Figure 7. Circuit Configuration for Activating One MC3423 from Another

Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

## Crowbar SCR Considerations

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, $\mathrm{C}_{\text {out }}$. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or $\mathrm{I}^{2} \mathrm{t}$. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

## di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities depending on the severity of the occasion.


Figure 8. R1 versus Trip Voltage


Figure 9. Minimum $\mathbf{R}_{\mathrm{G}}$ versus Supply Voltage


Figure 10. Capacitance versus Minimum Overvoltage Duration


Figure 11. Typical Crowbar OVP Circuit Configurations


Figure 12. Crowbar SCR Surge Current Waveform


Figure 13. Circuit Elements Affecting SCR Surge and di/dt

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the
gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving ( 3 to 5 times $\mathrm{I}_{\mathrm{GT}}$ ) the SCR gate with a fast $<1.0 \mu$ s rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than $50 \mathrm{~A}(\mathrm{RMS})$ rating might be $200 \mathrm{~A} / \mu \mathrm{s}$, assuming a gate current of five times $\mathrm{I}_{\mathrm{GT}}$ and $<1.0 \mu$ s rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the DC bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

## Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance - see Figure 13) to a safe level which is consistent with the systems requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

## A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11 A , it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an $\mathrm{I}^{2} \mathrm{t}$ rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

## CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

| Device | $\mathbf{I}_{\text {RMS }}$ | $\mathbf{I}_{\text {FSM }}$ | Package |
| :--- | :---: | :---: | :---: |
| 2N6400 Series | 16 A | 160 A | TO-220 Plastic |
| 2N6504 Series | 25 A | 160 A | TO-220 Plastic |
| 2N1842 Series | 16 A | 125 A | Metal Stud |
| 2N2573 Series | 25 A | 260 A | Metal TO-3 Type |
| 2N681 Series | 25 A | 200 A | Metal Stud |
| MCR3935-1 Series | 35 A | 350 A | Metal Stud |
| MCR81-5 Series | 80 A | 1000 A | Metal Stud |

## NCP3712ASNT1

## Over Voltage Protected High Side Switch

This switch is primarily intended to protect loads from transients by isolating the load from the transient energy rather than absorbing it.

## Features

- Capable of Switching Loads of up to 200 mA without External Rboost
- Switch Shuts Off in Response to an Over Voltage Input Transient
- Features Active Turn Off for Fast Input Transient Protection
- Flexible Over Voltage Protection Threshold Set with External Zener
- Automatic Recovery after Transient Decays Below Threshold
- Withstands Input Transients up to 105 V Peak
- Guaranteed Off State with Enbl Input
- ESD Resistant in Accordance with the 2000 V Human Body Model
- Extremely Low Saturation Voltage


## Applications Include:

- High Voltage Transient Isolation
- Power Switching to Electronic Modules
- DC Power Distribution in Line Operated Equipment
- Buffering Sensitive Circuits from Poorly Regulated Power Supplies
- Pre-conditioning of Voltage Regulator Input Voltage


Figure 1. Typical Application Circuit

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ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP3712ASNT1 | TSOP-6 | 3000 Units |
|  | (SOT23-6, SC59-6) | on 7" Reel |

MAXIMUM RATINGS* ( $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ unless otherwise noted) (Note 1)

| Rating |  | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Input-to-Output Voltage |  | $V_{\text {io }}$ | 105 | V |
| Reverse Input-to-Vz. Voltage |  | $\mathrm{V}_{\text {in(rev) }}$ | -9.0 | V |
| Reverse Input-to-Rboost Voltage |  | $\mathrm{V}_{\text {in(rev })}$ | -5.0 | V |
| Output Load Current - Continuous |  | $\mathrm{I}_{\text {load }}$ | -300 | mA |
| Enbl Input Current - Continuous |  | lenbl | 5.0 | mA |
| Vz Input Current - Continuous |  | $\mathrm{I}_{\mathrm{z}}$ | 3.0 | mA |
| Rboost Input Current - Continuous |  | $l_{\text {boost }}$ | 10 | mA |
| Junction Temperature |  | $\mathrm{T}_{\mathrm{J}}$ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range |  | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Device Power Dissipation (Minimum Footprint) |  | $\mathrm{P}_{\mathrm{D}}$ | 300 | mW |
| Derate Above $25^{\circ} \mathrm{C}$ |  | - | 2.4 | $\mathrm{mW} /{ }^{\circ} \mathrm{C}$ |
| Latch-up Performance: | Positive Negative | ${ }_{\text {Latch-up }}$ | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | mA |

*Maximum Ratings are those values beyond which damage to the device may occur.

1. This device contains ESD protection and exceeds the following tests: Human Body Model 1500 V per MIL-STD-883, Method 3015.
Machine Model Method 150 V .

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{in}}=12.5 \mathrm{~V}_{\mathrm{DC}}\right.$ Ref to $\mathrm{Gnd}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

OFF CHARACTERISTICS

| Input-Output Breakdown Voltage (@ Iout = $200 \mu \mathrm{~A}$ ) | $\mathrm{V}_{\text {(BRio) }}$ | 105 | - | - | Vdc |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Reverse Breakdown Voltage (@ Iout $=-1.0 \mathrm{~mA} \mathrm{Pulse)}$ | $\mathrm{V}_{\text {(-BRout) }}$ | - | -0.7 | - | Vdc |
| Output Leakage Current $\left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {enbl }}=30 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\text {load(off) }}$ | - | - | -100 | $\mu \mathrm{Adc}$ |
| Guaranteed "Off" State "ENBL NOT" Voltage $\quad$ ( $\mathrm{l}_{0} \leq 100 \mu \mathrm{~A}$ ) | $\mathrm{V}_{\text {enbl(off) }}$ | 13 | - | - | Vdc |
| Required "Off" State $\mathrm{I}_{\mathrm{z}}$ Current ( $\mathrm{R}_{\text {load }}=100 \Omega$ ) | $\mathrm{I}_{\text {(off) }}$ | 150 | - | - | $\mu \mathrm{Adc}$ |
| $\begin{aligned} & \mathrm{V}_{\text {in(off) }} \\ & \left(\mathrm{V}_{\mathrm{z}}=16 \mathrm{~V}, \mathrm{I}_{\text {load }}=100 \mathrm{~mA}, \mathrm{R}_{\text {enbl }}=1500 \Omega\right) \end{aligned}$ | $\mathrm{V}_{\text {off }}$ | 15.5 | - | 18.7 | Vdc |

## ON CHARACTERISTICS

| Input-Output On Voltage $\left(\mathrm{I}_{\mathrm{o}}=100 \mathrm{~mA}, \mathrm{I}_{\mathrm{enbl}}=-3.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {io(on) }}$ | - | 0.2 | 0.5 | Vdc |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathrm{I}_{\text {(on) }}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | - | $\begin{aligned} & -200 \\ & -200 \\ & -300 \end{aligned}$ | mAdc |
| $\begin{aligned} & \mathrm{V}_{\text {in(on })} \\ & \left(\mathrm{V}_{\mathrm{z}}=16 \mathrm{~V}, \mathrm{I}_{\text {load }}=100 \mathrm{~mA}, \mathrm{R}_{\text {enbl }}=1500 \Omega\right) \end{aligned}$ | $\mathrm{V}_{\text {on }}$ | 8.5 | - | 10.5 | Vdc |
| "ENBL NOT" Input Current $\left(\mathrm{I}_{\mathrm{o}}=100 \mathrm{~mA}, \mathrm{~V}_{\mathrm{io}(\text { on })}=0.35 \mathrm{Vdc}, \mathrm{R}_{\text {enbl }}=1500 \Omega\right)$ | lenbl | - | - | -1.0 | mAdc |

## SWITCHING CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Units |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay Time: |  |  |  |  | $\mu \mathrm{S}$ |
| Hi to Lo Prop Delay; Fig. $3\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {enbl }}=13.5 \mathrm{~V}\right)$ | $\mathrm{t}_{\text {PHL }}$ | - | 1.5 | - |  |
| Lo to Hi Prop Delay; Fig. $3\left(\mathrm{~V}_{\text {in }}=13.5 \mathrm{~V}, \mathrm{~V}_{\text {enbl }}=0 \mathrm{~V}\right)$ | $\mathrm{t}_{\text {PLH }}$ | - | 1.5 | - |  |
| Transition Times: |  |  |  |  | $\eta \mathrm{S}$ |
| Fall Time; Fig. $4\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {enbl }}=13.5 \mathrm{~V}\right)$ | $\mathrm{t}_{\mathrm{f}}$ | - | 75 | - |  |
| Rise Time; Fig. $4\left(\mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {enbl }}=0 \mathrm{~V}\right)$ | $\mathrm{t}_{\mathrm{r}}$ | - | 400 | - |  |

## INTERNAL RESISTORS

| Input Leakage Resistor | R 2 | 7.0 | 10 | 13 | $\mathrm{k} \Omega$ |
| :--- | :--- | :--- | :--- | :---: | :---: |
| Input Resistor | R 1 | 3.3 | 4.7 | 6.1 | $\mathrm{k} \Omega$ |
| Output Leakage Resistor | R 4 | 1.4 | 2.4 | 3.2 | $\mathrm{k} \Omega$ |
| Enable Input Resistor | R 3 | 1.4 | 2.4 | 3.2 | $\mathrm{k} \Omega$ |



Figure 2. Typical Applications Circuit for Load Dump Transient Protection


Figure 3. Enable NOT Switching Waveforms


Figure 4. Load Dump Waveforms

## INFORMATION FOR USING THE TSOP-6 SURFACE MOUNT PACKAGE MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


## TSOP-6 POWER DISSIPATION

The power dissipation of the TSOP-6 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $\mathrm{T}_{\mathrm{J}(\max )}$, the maximum rated junction temperature of the die, $\mathrm{R}_{\theta \mathrm{JA}}$, the thermal resistance from the device junction to ambient, and the operating temperature, $\mathrm{T}_{\mathrm{A}}$. Using the values provided on the data sheet for the TSOP-6 package, $\mathrm{P}_{\mathrm{D}}$ can be calculated as follows:

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $\mathrm{T}_{\mathrm{A}}$ of $25^{\circ} \mathrm{C}$, one can calculate the power dissipation of the device which in this case is 950 milliwatts.

$$
P_{D}=\frac{150^{\circ} \mathrm{C}-25^{\circ} \mathrm{C}}{132^{\circ} \mathrm{C} / \mathrm{W}}=950 \text { milliwatts }
$$

The $132^{\circ} \mathrm{C} / \mathrm{W}$ for the TSOP-6 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 950 milliwatts. There are other alternatives to achieving higher power dissipation from the TSOP-6 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad ${ }^{\mathrm{TM}}$. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be $100^{\circ} \mathrm{C}$ or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of $10^{\circ} \mathrm{C}$.
- The soldering temperature and time shall not exceed $260^{\circ} \mathrm{C}$ for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be $5^{\circ} \mathrm{C}$ or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.
*     * Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.


## MC34161, MC33161

## Universal Voltage Monitors

The MC34161/MC33161 are universal voltage monitors intended for use in a wide variety of voltage sensing applications. These devices offer the circuit designer an economical solution for positive and negative voltage detection. The circuit consists of two comparator channels each with hysteresis, a unique Mode Select Input for channel programming, a pinned out 2.54 V reference, and two open collector outputs capable of sinking in excess of 10 mA . Each comparator channel can be configured as either inverting or noninverting by the Mode Select Input. This allows over, under, and window detection of positive and negative voltages. The minimum supply voltage needed for these devices to be fully functional is 2.0 V for positive voltage sensing and 4.0 V for negative voltage sensing.

Applications include direct monitoring of positive and negative voltages used in appliance, automotive, consumer, and industrial equipment.

- Unique Mode Select Input Allows Channel Programming
- Over, Under, and Window Voltage Detection
- Positive and Negative Voltage Detection
- Fully Functional at 2.0 V for Positive Voltage Sensing and 4.0 V for Negative Voltage Sensing
- Pinned Out 2.54 V Reference with Current Limit Protection
- Low Standby Current
- Open Collector Outputs for Enhanced Device Flexibility


This device contains 141 transistors.

Figure 1. Simplified Block Diagram
(Positive Voltage Window Detector Application)

See detailed ordering and shipping information in the package dimensions section on page 2714 of this data sheet.


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| X | $=3$ or 4 |
| :--- | :--- |
| A | $=$ Assembly Location |
| WL, L | $=$ Wafer Lot |
| $Y Y, Y$ | $=$ Year |
| WW, W | $=$ Work Week |

PIN CONNECTIONS

ORDERING INFORMATION

## MC34161, MC33161

## MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Input Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| Comparator Input Voltage Range | $V_{\text {in }}$ | -1.0 to +40 | V |
| Comparator Output Sink Current (Pins 5 and 6) (Note 2) | $\mathrm{I}_{\text {Sink }}$ | 20 | mA |
| Comparator Output Voltage | $V_{\text {out }}$ | 40 | V |
| Power Dissipation and Thermal Characteristics (Note 2) <br> P Suffix, Plastic Package, Case 626 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> D Suffix, Plastic Package, Case 751 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=70^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> DM Suffix, Plastic Package, Case 846A <br> Thermal Resistance, Junction-to-Ambient | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {日JA }}$ | $\begin{aligned} & 800 \\ & 100 \\ & 450 \\ & 178 \\ & 240 \end{aligned}$ | mW ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> mW <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ <br> ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature (Note 3) <br> MC34161 <br> MC33161 | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+105 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per MIL-STD-883, Method 3015 .

Machine Model Method 200 V .
2. Maximum package power dissipation must be observed.
3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34161 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34161 $-40^{\circ} \mathrm{C}$ for MC33161 $+105^{\circ} \mathrm{C}$ for MC33161

## MC34161, MC33161

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right.$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Notes 4 and 5], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMPARATOR INPUTS |  |  |  |  |  |
| $\begin{array}{ll} \hline \text { Threshold Voltage, } \mathrm{V}_{\text {in }} \text { Increasing } & \left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {min }} \text { to } \mathrm{T}_{\text {max }}\right) \end{array}$ | $\mathrm{V}_{\text {th }}$ | $\begin{aligned} & 1.245 \\ & 1.235 \end{aligned}$ | $1.27$ | $\begin{aligned} & 1.295 \\ & 1.295 \end{aligned}$ | V |
| Threshold Voltage Variation ( $\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}$ to 40 V ) | $\Delta \mathrm{V}_{\text {th }}$ | - | 7.0 | 15 | mV |
| Threshold Hysteresis, $\mathrm{V}_{\text {in }}$ Decreasing | $\mathrm{V}_{\mathrm{H}}$ | 15 | 25 | 35 | mV |
| Threshold Difference $\left\|\mathrm{V}_{\text {th1 }}-\mathrm{V}_{\text {th2 }}\right\|$ | $V_{D}$ | - | 1.0 | 15 | mV |
| Reference to Threshold Difference ( $\mathrm{V}_{\text {ref }}-\mathrm{V}_{\text {in } 1}$ ), ( $\mathrm{V}_{\text {ref }}-\mathrm{V}_{\text {in2 }}$ ) | $V_{\text {RTD }}$ | 1.20 | 1.27 | 1.32 | V |
| $\begin{array}{ll} \text { Input Bias Current } & \left(\mathrm{V}_{\text {in }}=1.0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{array}$ | $I_{\text {IB }}$ | - | $\begin{aligned} & 40 \\ & 85 \end{aligned}$ | $\begin{aligned} & 200 \\ & 400 \end{aligned}$ | nA |

MODE SELECT INPUT

| Mode Select Threshold Voltage (Figure 6) | Channel 1 |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
|  | Channel 2 |

## COMPARATOR OUTPUTS

| Output Sink Saturation Voltage $\left(I_{\text {Sink }}=2.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 0.05 | 0.3 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\left(I_{\text {Sink }}=10 \mathrm{~mA}\right)$ |  |  |  |  |  |
| $\left(I_{\text {Sink }}=0.25 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=1.0 \mathrm{~V}\right)$ |  | - | 0.22 | 0.6 |  |
| Off-State Leakage Current $\left(\mathrm{V}_{\mathrm{OH}}=40 \mathrm{~V}\right)$ |  | - | 0.02 | 0.2 |  |

REFERENCE OUTPUT

| Output Voltage $\left(\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {ef }}$ | 2.48 | 2.54 | 2.60 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Load Regulation $\left(\mathrm{I}_{\mathrm{O}}=0 \mathrm{~mA}\right.$ to 2.0 mA$)$ | Reg $_{\text {load }}$ | - | 0.6 | 15 | mV |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}\right.$ to 40 V$)$ | Regline | - | 5.0 | 15 | mV |
| Total Output Variation over Line, Load, and Temperature | $\Delta \mathrm{V}_{\text {ref }}$ | 2.45 | - | 2.60 | V |
| Short Circuit Current | $\mathrm{I}_{\mathrm{SC}}$ | - | 8.5 | 30 | mA |

TOTAL DEVICE

| Power Supply Current ( $\left.\mathrm{V}_{\text {Mode }}, \mathrm{V}_{\text {in1 }}, \mathrm{V}_{\text {in2 }}=\mathrm{Gnd}\right)$ | $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right)$ <br> $\left(\mathrm{V}_{\mathrm{CC}}=40 \mathrm{~V}\right)$ |  | - | 450 | 700 | $\mu \mathrm{~A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Voltage Range (Positive Sensing) |  | $\mathrm{V}_{\mathrm{CC}}$ | 2.0 | - | 40 | V |
| (Negative Sensing) |  | 4.0 | - | 40 |  |  |

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34161
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34161
$+105^{\circ} \mathrm{C}$ for MC33161


Figure 2. Comparator Input Threshold Voltage


Figure 4. Output Propagation Delay Time versus Percent Overdrive


Figure 6. Mode Select Thresholds


Figure 3. Comparator Input Bias Current versus Input Voltage


Figure 5. Output Voltage versus Supply Voltage


Figure 7. Mode Select Input Current versus Input Voltage


Figure 8. Reference Voltage versus Supply Voltage


Figure 10. Reference Voltage Change versus Source Current


Figure 12. Supply Current versus Supply Voltage


Figure 9. Reference Voltage versus Ambient Temperature


Figure 11. Output Saturation Voltage versus Output Sink Current


Figure 13. Supply Current versus Output Sink Current

## MC34161, MC33161



Figure 14. MC34161 Representative Block Diagram

| Mode Select <br> Pin 7 | Input 1 <br> Pin 2 | Output 1 <br> Pin 6 | Input 2 <br> Pin 3 | Output 2 <br> Pin 5 | Comments |
| :---: | :---: | :---: | :---: | :---: | :--- |
| GND | 0 | 0 | 0 | 0 | Channels 1 \& 2: Noninverting |
| $\mathrm{V}_{\text {ref }}$ | 0 | 1 | 1 | 1 |  |
| $\mathrm{~V}_{\mathrm{CC}}$ (>2.0 V) | 0 | 0 | 0 | 1 | Channel 1: Noninverting |
|  | 1 | 1 | 1 | 0 | Channel 2: Inverting |

Figure 15. Truth Table

## FUNCTIONAL DESCRIPTION

## Introduction

To be competitive in today's electronic equipment market, new circuits must be designed to increase system reliability with minimal incremental cost. The circuit designer can take a significant step toward attaining these goals by implementing economical circuitry that continuously monitors critical circuit voltages and provides a fault signal in the event of an out-of-tolerance condition. The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. The main objectives of this series was to configure a device that can be used in as many voltage sensing applications as possible while minimizing cost. The flexibility objective is achieved by the utilization of a unique Mode Select input that is used in conjunction with traditional circuit building blocks. The cost objective is achieved by processing the device on a standard Bipolar Analog flow, and by limiting the package to eight pins. The device consists of two comparator channels each with hysteresis, a mode select input for channel programming, a pinned out reference, and two open collector outputs. Each comparator channel can be configured as either inverting or noninverting by the Mode Select input. This allows a single device to perform over, under, and window detection of positive and negative voltages. A detailed description of each section of the device is given below with the representative block diagram shown in Figure 14.

## Input Comparators

The input comparators of each channel are identical, each having an upper threshold voltage of $1.27 \mathrm{~V} \pm 2.0 \%$ with 25 mV of hysteresis. The hysteresis is provided to enhance output switching by preventing oscillations as the comparator thresholds are crossed. The comparators have an input bias current of 60 nA at their threshold which approximates a $21.2 \mathrm{M} \Omega$ resistor to ground. This high impedance minimizes loading of the external voltage divider for well defined trip points. For all positive voltage sensing applications, both comparator channels are fully functional at a $\mathrm{V}_{\mathrm{CC}}$ of 2.0 V . In order to provide enhanced device ruggedness for hostile industrial environments, additional circuitry was designed into the inputs to prevent device latch-up as well as to suppress electrostatic discharges (ESD).

## Reference

The 2.54 V reference is pinned out to provide a means for the input comparators to sense negative voltages, as well as a means to program the Mode Select input for window detection applications. The reference is capable of sourcing in excess of 2.0 mA output current and has built-in short circuit protection. The output voltage has a guaranteed tolerance of $\pm 2.4 \%$ at room temperature.

The 2.54 V reference is derived by gaining up the internal 1.27 V reference by a factor of two. With a power supply voltage of 4.0 V , the 2.54 V reference is in full regulation, allowing the device to accurately sense negative voltages.

## Mode Select Circuit

The key feature that allows this device to be flexible is the Mode Select input. This input allows the user to program each of the channels for various types of voltage sensing applications. Figure 15 shows that the Mode Select input has three defined states. These states determine whether Channel 1 and/or Channel 2 operate in the inverting or noninverting mode. The Mode Select thresholds are shown in Figure 6. The input circuitry forms a tristate switch with thresholds at 0.63 V and $\mathrm{V}_{\text {ref }}+0.23 \mathrm{~V}$. The mode select input current is $10 \mu \mathrm{~A}$ when connected to the reference output, and $42 \mu \mathrm{~A}$ when connected to a $\mathrm{V}_{\mathrm{CC}}$ of 5.0 V , refer to Figure 7.

## Output Stage

The output stage uses a positive feedback base boost circuit for enhanced sink saturation, while maintaining a relatively low device standby current. Figure 11 shows that the sink saturation voltage is about 0.2 V at 8.0 mA over temperature. By combining the low output saturation characteristics with low voltage comparator operation, this device is capable of sensing positive voltages at a $\mathrm{V}_{\mathrm{CC}}$ of 1.0 V . These characteristics are important in undervoltage sensing applications where the output must stay in a low state as $\mathrm{V}_{\mathrm{CC}}$ approaches ground. Figure 5 shows the Output Voltage versus Supply Voltage in an undervoltage sensing application. Note that as $\mathrm{V}_{\mathrm{CC}}$ drops below the programmed 4.5 V trip point, the output stays in a well defined active low state until $\mathrm{V}_{\mathrm{CC}}$ drops below 1.0 V .

## APPLICATIONS

The following circuit figures illustrate the flexibility of this device. Included are voltage sensing applications for over, under, and window detectors, as well as three unique configurations. Many of the voltage detection circuits are shown with the open collector outputs of each channel connected together driving a light emitting diode (LED). This 'ORed' connection is shown for ease of explanation and it is only required for window detection applications.

Note that many of the voltage detection circuits are shown with a dashed line output connection. This connection gives the inverse function of the solid line connection. For example, the solid line output connection of Figure 16 has the LED 'ON' when input voltage $\mathrm{V}_{\mathrm{S}}$ is above trip voltage $\mathrm{V}_{2}$, for overvoltage detection. The dashed line output connection has the LED ' ON ' when $\mathrm{V}_{\mathrm{S}}$ is below trip voltage $\mathrm{V}_{2}$, for undervoltage detection.


The above figure shows the MC34161 configured as a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $\mathrm{V}_{\mathrm{S} 1}$ or $\mathrm{V}_{\mathrm{S} 2}$ exceeds $\mathrm{V}_{2}$. With the dashed line output connection, the circuit becomes a dual positive undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when $\mathrm{V}_{\mathrm{S} 1}$ or $\mathrm{V}_{\mathrm{S} 2}$ falls below $\mathrm{V}_{1}$.

For known resistor values, the voltage trip points are:

$$
\mathrm{V}_{1}=\left(\mathrm{V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H}}\right)\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right) \quad \mathrm{V}_{2}=\mathrm{V}_{\mathrm{th}}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)
$$

For a specific trip voltage, the required resistor ratio is:

$$
\frac{R_{2}}{R_{1}}=\frac{V_{1}}{V_{t h}-V_{H}}-1 \quad \frac{R_{2}}{R_{1}}=\frac{V_{2}}{V_{t h}}-1
$$

Figure 16. Dual Positive Overvoltage Detector


The above figure shows the MC34161 configured as a dual positive undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when $\mathrm{V}_{\mathrm{S} 1}$ or $\mathrm{V}_{\mathrm{S} 2}$ falls below $\mathrm{V}_{1}$. With the dashed line output connection, the circuit becomes a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $V_{S 1}$ or $V_{S 2}$ exceeds $V_{2}$.

For known resistor values, the voltage trip points are:

$$
\mathrm{V}_{1}=\left(\mathrm{V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H}}\right)\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right) \quad \mathrm{V}_{2}=\mathrm{V}_{\mathrm{th}}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)
$$

For a specific trip voltage, the required resistor ratio is:

$$
\frac{R_{2}}{R_{1}}=\frac{V_{1}}{V_{t h}-V_{H}}-1 \quad \frac{R_{2}}{R_{1}}=\frac{V_{2}}{V_{t h}}-1
$$

Figure 17. Dual Positive Undervoltage Detector


The above figure shows the MC34161 configured as a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-\mathrm{V}_{\mathrm{S} 1}$ or $-\mathrm{V}_{\mathrm{S} 2}$ exceeds $\mathrm{V}_{2}$. With the dashed line output connection, the circuit becomes a dual negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when $-\mathrm{V}_{\mathrm{S} 1}$ or $-\mathrm{V}_{\mathrm{S} 2}$ falls below $\mathrm{V}_{1}$.

For known resistor values, the voltage trip points are:

$$
\mathrm{V}_{1}=\frac{\mathrm{R}_{1}}{\mathrm{R}_{2}}\left(\mathrm{~V}_{\text {th }}-\mathrm{V}_{\text {ref }}\right)+\mathrm{V}_{\text {th }} \quad \mathrm{V}_{2}=\frac{\mathrm{R}_{1}}{\mathrm{R}_{2}}\left(\mathrm{~V}_{\text {th }}-\mathrm{V}_{\mathrm{H}}-\mathrm{V}_{\text {ref }}\right)+\mathrm{V}_{\text {th }}-\mathrm{V}_{\mathrm{H}}
$$

For a specific trip voltage, the required resistor ratio is:

$$
\frac{R_{1}}{R_{2}}=\frac{V_{1}-V_{\text {th }}}{V_{\text {th }}-V_{\text {ref }}} \quad \frac{R_{1}}{R_{2}}=\frac{V_{2}-V_{\text {th }}+V_{H}}{V_{\text {th }}-V_{H}-V_{\text {ref }}}
$$

Figure 18. Dual Negative Overvoltage Detector


The above figure shows the MC34161 configured as a dual negative undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when $-V_{S 1}$ or $-V_{S 2}$ falls below $V_{1}$. With the dashed line output connection, the circuit becomes a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-\mathrm{V}_{\mathrm{S} 1}$ or $-\mathrm{V}_{\mathrm{S} 2}$ exceeds $\mathrm{V}_{2}$.

For known resistor values, the voltage trip points are:

$$
\mathrm{V}_{1}=\frac{\mathrm{R}_{1}}{\mathrm{R}_{2}}\left(\mathrm{~V}_{\text {th }}-\mathrm{V}_{\mathrm{ref}}\right)+\mathrm{V}_{\text {th }} \quad \mathrm{V}_{2}=\frac{\mathrm{R}_{1}}{\mathrm{R}_{2}}\left(\mathrm{~V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H}}-\mathrm{V}_{\mathrm{ref}}\right)+\mathrm{V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H}}
$$

For a specific trip voltage, the required resistor ratio is:

$$
\frac{R_{1}}{R_{2}}=\frac{V_{1}-V_{\text {th }}}{V_{\text {th }}-V_{\text {ref }}} \quad \frac{R_{1}}{R_{2}}=\frac{V_{2}-V_{\text {th }}+V_{H}}{V_{\text {th }}-V_{H}-V_{\text {ref }}}
$$

Figure 19. Dual Negative Undervoltage Detector


The above figure shows the MC34161 configured as a positive voltage window detector. This is accomplished by connecting channel 1 as an undervoltage detector, and channel 2 as an overvoltage detector. When the input voltage $\mathrm{V}_{S}$ falls out of the window established by $\mathrm{V}_{1}$ and $\mathrm{V}_{4}$, the LED will turn 'ON'. As the input voltage falls within the window, $V_{S}$ increasing from ground and exceeding $V_{2}$, or $\mathrm{V}_{\mathrm{S}}$ decreasing from the peak towards ground and falling below $\mathrm{V}_{3}$, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage $\mathrm{V}_{\mathrm{S}}$ is within the window.

For known resistor values, the voltage trip points are:
For a specific trip voltage, the required resistor ratio is:

$$
\begin{array}{ll}
\mathrm{V}_{1}=\left(\mathrm{V}_{\mathrm{th} 1}-\mathrm{V}_{\mathrm{H} 1}\right)\left(\frac{\mathrm{R}_{3}}{\mathrm{R}_{1}+\mathrm{R}_{2}}+1\right) & \mathrm{V}_{3}=\left(\mathrm{V}_{\mathrm{th} 2}-\mathrm{V}_{\mathrm{H} 2}\right)\left(\frac{\mathrm{R}_{2}+\mathrm{R}_{3}}{\mathrm{R}_{1}}+1\right) \\
\mathrm{V}_{2}=\mathrm{V}_{\mathrm{th} 1}\left(\frac{\mathrm{R}_{3}}{\mathrm{R}_{1}+\mathrm{R}_{2}}+1\right) & \frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}=\frac{\mathrm{V}_{3}\left(\mathrm{~V}_{\mathrm{th} 2}-\mathrm{V}_{\mathrm{H} 2}\right)}{\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{th} 1}-\mathrm{V}_{\mathrm{H} 1}\right)}-1
\end{array} \frac{\mathrm{R}_{3}}{\mathrm{R}_{1}}=\frac{\mathrm{V}_{3}\left(\mathrm{~V}_{1}-\mathrm{V}_{\mathrm{th} 1}+\mathrm{V}_{\mathrm{H} 1}\right)}{\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{th} 2}-\mathrm{V}_{\mathrm{H} 2}\right)}
$$

Figure 20. Positive Voltage Window Detector


The above figure shows the MC34161 configured as a negative voltage window detector. When the input voltage $-\mathrm{V}_{\mathrm{S}}$ falls out of the window established by $\mathrm{V}_{1}$ and $\mathrm{V}_{4}$, the LED will turn 'ON'. As the input voltage falls within the window, $-\mathrm{V}_{\mathrm{S}}$ increasing from ground and exceeding $\mathrm{V}_{2}$, or $-\mathrm{V}_{\mathrm{S}}$ decreasing from the peak towards ground and falling below $\mathrm{V}_{3}$, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage $-\mathrm{V}_{\mathrm{S}}$ is within the window.

For known resistor values, the voltage trip points are:

$$
\begin{aligned}
& V_{1}=\frac{R_{1}\left(V_{\text {th2 }}-V_{\text {ref }}\right)}{R_{2}+R_{3}}+V_{\text {th2 }} \\
& V_{2}=\frac{R_{1}\left(V_{\text {th2 }}-V_{H 2}-V_{\text {ref }}\right)}{R_{2}+R_{3}}+V_{\text {th2 }}-V_{H 2} \\
& V_{3}=\frac{\left(R_{1}+R_{2}\right)\left(V_{\text {th }}-V_{\text {ref }}\right)}{R_{3}}+V_{\text {th1 }} \\
& V_{4}=\frac{\left(R_{1}+R_{2}\right)\left(V_{\text {th } 1}-V_{H 1}-V_{\text {ref }}\right)}{R_{3}}+V_{\text {th1 }}-V_{H 1}
\end{aligned}
$$

For a specific trip voltage, the required resistor ratio is:

$$
\begin{aligned}
& \frac{R_{1}}{R_{2}+R_{3}}=\frac{V_{1}-V_{\text {th2 }}}{V_{\text {th2 }}-V_{\text {ref }}} \\
& \frac{R_{1}}{R_{2}+R_{3}}=\frac{V_{2}-V_{\text {th2 }}+V_{H 2}}{V_{\text {th2 }}-V_{H 2}-V_{\text {ref }}} \\
& \frac{R_{3}}{R_{1}+R_{2}}=\frac{V_{\text {th1 }}-V_{\text {ref }}}{V_{3}-V_{\text {th1 }}} \\
& \frac{R_{3}}{R_{1}+R_{2}}=\frac{V_{\text {th1 }}-V_{H 1}-V_{\text {ref }}}{V_{4}+V_{H 1}-V_{\text {th } 1}}
\end{aligned}
$$

Figure 21. Negative Voltage Window Detector


The above figure shows the MC34161 configured as a positive and negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when either $-\mathrm{V}_{\mathrm{S} 1}$ exceeds $\mathrm{V}_{2}$, or $\mathrm{V}_{\mathrm{S} 2}$ exceeds $\mathrm{V}_{4}$. With the dashed line output connection, the circuit becomes a positive and negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn ' ON ' when either $\mathrm{V}_{\mathrm{S} 2}$ falls below $\mathrm{V}_{3}$, or $-\mathrm{V}_{\mathrm{S} 1}$ falls below $\mathrm{V}_{1}$.

For known resistor values, the voltage trip points are:

> For a specific trip voltage, the required resistor ratio is:

$$
\begin{array}{ll}
\mathrm{V}_{1}=\frac{\mathrm{R}_{3}}{\mathrm{R}_{4}}\left(\mathrm{~V}_{\mathrm{th} 1}-\mathrm{V}_{\mathrm{ref}}\right)+\mathrm{V}_{\mathrm{th} 1} & \mathrm{~V}_{3}=\left(\mathrm{V}_{\mathrm{th} 2}-\mathrm{V}_{\mathrm{H} 2}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)\right. \\
\mathrm{V}_{2}=\frac{\mathrm{R}_{3}}{\mathrm{R}_{4}}\left(\mathrm{~V}_{\mathrm{th} 1}-\mathrm{V}_{\mathrm{H} 1}-\mathrm{V}_{\mathrm{ref}}\right)+\mathrm{V}_{\mathrm{th} 1}-\mathrm{V}_{\mathrm{H} 1} & \mathrm{~V}_{4}=\mathrm{V}_{\mathrm{th} 2}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)
\end{array}
$$

$$
\begin{array}{ll}
\frac{R_{3}}{R_{4}}=\frac{\left(V_{1}-V_{\text {th1 }}\right)}{\left(V_{\text {th1 }}-V_{\text {ref }}\right)} & \frac{R_{2}}{R_{1}}=\frac{V_{4}}{V_{\text {th2 }}}-1 \\
\frac{R_{3}}{R_{4}}=\frac{\left(V_{2}-V_{\text {th1 }}+V_{H 1}\right)}{\left(V_{\text {th1 }}-V_{H 1}-V_{\text {ref }}\right)} & \frac{R_{2}}{R_{1}}=\frac{V_{3}}{V_{\text {th2 }}-V_{H 2}}-1
\end{array}
$$

Figure 22. Positive and Negative Overvoltage Detector


The above figure shows the MC34161 configured as a positive and negative undervoltage detector. As the input voltage decreases toward ground, the LED will turn ' ON' when either $\mathrm{V}_{\mathrm{S} 1}$ falls below $\mathrm{V}_{1}$, or $-\mathrm{V}_{\mathrm{S} 2}$ falls below $\mathrm{V}_{3}$. With the dashed line output connection, the circuit becomes a positive and negative overvoltage detector. As the input voltage increases from the ground, the LED will turn 'ON' when either $V_{S 1}$ exceeds $V_{2}$, or $-V_{S 1}$ exceeds $V_{1}$.

For known resistor values, the voltage trip points are:
For a specific trip voltage, the required resistor ratio is:

Figure 23. Positive and Negative Undervoltage Detector

$$
\begin{aligned}
& \mathrm{V}_{1}=\left(\mathrm{V}_{\mathrm{th} 1}-\mathrm{V}_{\mathrm{H} 1}\right)\left(\frac{\mathrm{R}_{4}}{\mathrm{R}_{3}}+1\right) \quad \mathrm{V}_{3}=\frac{\mathrm{R}_{1}}{\mathrm{R}_{2}}\left(\mathrm{~V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{ref}}\right)+\mathrm{V}_{\mathrm{th} 2} \\
& \mathrm{~V}_{2}=\mathrm{V}_{\mathrm{th} 1}\left(\frac{\mathrm{R}_{4}}{\mathrm{R}_{3}}+1\right) \quad \mathrm{V}_{4}=\frac{\mathrm{R}_{1}}{\mathrm{R}_{2}}\left(\mathrm{~V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H} 2}-\mathrm{V}_{\mathrm{ref}}\right)+\mathrm{V}_{\mathrm{th} 2}-\mathrm{V}_{\mathrm{H} 2} \\
& \frac{R_{4}}{R_{3}}=\frac{V_{2}}{V_{t h 1}}-1 \\
& \frac{R_{1}}{R_{2}}=\frac{V_{4}+V_{H 2}-V_{\text {th2 }}}{V_{\text {th2 }}-V_{H 2}-V_{\text {ref }}} \\
& \frac{R_{4}}{R_{3}}=\frac{V_{1}}{V_{\text {th1 }}-V_{H 1}}-1 \quad \frac{R_{1}}{R_{2}}=\frac{V_{3}-V_{\text {th2 }}}{V_{\text {th2 }}-V_{\text {ref }}}
\end{aligned}
$$



The above figure shows the MC34161 configured as an overvoltage detector with an audio alarm. Channel 1 monitors input voltage $V_{S}$ while channel 2 is connected as a simple RC oscillator. As the input voltage increases from ground, the output of channel 1 allows the oscillator to turn 'ON' when $\mathrm{V}_{\mathrm{S}}$ exceeds $\mathrm{V}_{2}$.

For known resistor values, the voltage trip points are:

$$
\mathrm{V}_{1}=\left(\mathrm{V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H}}\right)\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right) \mathrm{V}_{2}=\mathrm{V}_{\mathrm{th}}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right)
$$

For a specific trip voltage, the required resistor ratio is:

$$
\frac{R_{2}}{R_{1}}=\frac{V_{1}}{V_{t h}-V_{H}}-1 \quad \frac{R_{2}}{R_{1}}=\frac{V_{2}}{V_{t h}}-1
$$

Figure 24. Overvoltage Detector with Audio Alarm


The above figure shows the MC34161 configured as a microprocessor reset with a time delay. Channel 2 monitors input voltage $\mathrm{V}_{\mathrm{S}}$ while channel 1 performs the time delay function. As the input voltage decreases towards ground, the output of channel 2 quickly discharges $\mathrm{C}_{\mathrm{DLY}}$ when $\mathrm{V}_{\mathrm{S}}$ falls below $\mathrm{V}_{1}$. As the input voltage increases from ground, the output of channel 2 allows $R_{D L Y}$ to charge $C_{D L Y}$ when $V_{S}$ exceeds $V_{2}$.

For known resistor values, the voltage trip points are: For a specific trip voltage, the required resistor ratio is:

$$
\mathrm{V}_{1}=\left(\mathrm{V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H}}\right)\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right) \quad \mathrm{V}_{2}=\mathrm{V}_{\mathrm{th}}\left(\frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}+1\right) \quad \frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}=\frac{\mathrm{V}_{1}}{\mathrm{~V}_{\mathrm{th}}-\mathrm{V}_{\mathrm{H}}}-1 \quad \frac{\mathrm{R}_{2}}{\mathrm{R}_{1}}=\frac{\mathrm{V}_{2}}{\mathrm{~V}_{\mathrm{th}}}-1
$$

For known $R_{D L Y} C_{D L Y}$ values, the reset time delay is:

$$
\mathrm{t}_{\mathrm{DLY}}=\mathrm{R}_{\mathrm{DLY}} C_{D L Y} \ln \quad\left(\frac{1}{1-\frac{\mathrm{V}_{\mathrm{th}}}{\mathrm{~V}_{\mathrm{CC}}}}\right)
$$

Figure 25. Microprocessor Reset with Time Delay


The above circuit shows the MC34161 configured as an automatic line voltage selector. The IC controls the triac, enabling the circuit to function as a fullwave voltage doubler or a fullwave bridge. Channel 1 senses the negative half cycles of the AC line voltage. If the line voltage is less than150 V, the circuit will switch from bridge mode to voltage doubling mode after a preset time delay. The delay is controlled by the $100 \mathrm{k} \Omega$ resistor and the $10 \mu \mathrm{~F}$ capacitor. If the line voltage is greater than 150 V , the circuit will immediately return to fullwave bridge mode.

Figure 26. Automatic AC Line Voltage Selector

## MC34161, MC33161



Figure 27. Step-Down Converter

| Test | Conditions | Results |
| :--- | :--- | :--- |
| Line Regulation | $\mathrm{V}_{\text {in }}=9.5 \mathrm{~V}$ to $24 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$ | $40 \mathrm{mV}= \pm 0.1 \%$ |
| Load Regulation | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0.25 \mathrm{~mA}$ to 250 mA | $2.0 \mathrm{mV}= \pm 0.2 \%$ |
| Output Ripple | $\mathrm{V}_{\mathrm{in}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$ | 50 mVpp |
| Efficiency | $\mathrm{V}_{\text {in }}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}$ | $87.8 \%$ |

The above figure shows the MC34161 configured as a step-down converter. Channel 1 monitors the output voltage while Channel 2 performs the oscillator function. Upon initial power-up, the converters output voltage will be below nominal, and the output of Channel 1 will allow the oscillator to run. The external switch transistor will eventually pump-up the output capacitor until its voltage exceeds the input threshold of Channel 1. The output of Channel 1 will then switch low and disable the oscillator. The oscillator will commence operation when the output voltage falls below the lower threshold of Channel 1.

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC34161D | SO-8 | 98 Units/Rail |
| MC34161DR2 | SO-8 | 2500 Tape \& Reel |
| MC34161DMR2 | Micro8 | 4000 Tape \& Reel |
| MC34161P | PDIP-8 | 50 Units/Rail |
| MC33161D | SO-8 | 98 Units/Rail |
| MC33161DR2 | SO-8 | 2500 Tape \& Reel |
| MC33161DMR2 | Micro8 | 4000 Tape \& Reel |
| MC33161P | PDIP-8 | 50 Units/Rail |

## NCP300, NCP301

## Voltage Detector Series

The NCP300 and NCP301 series are second generation ultra-low current voltage detectors. These devices are specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is paramount

Each series features a highly accurate under voltage detector with hysteresis which prevents erratic system reset operation as the comparator threshold is crossed.

The NCP300 series consists of complementary output devices that are available with either an active high or active low reset output. The NCP301 series has an open drain N -channel output with either an active high or active low reset output.

The NCP300 and NCP301 device series are available in the Thin SOT-23-5 package with seven standard under voltage thresholds. Additional thresholds that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

## Features

- Quiescent Current of $0.5 \mu \mathrm{~A}$ Typical
- High Accuracy Under Voltage Threshold of $2.0 \%$
- Wide Operating Voltage Range of 0.8 V to 10 V
- Complementary or Open Drain Reset Output
- Active Low or Active High Reset Output


## Typical Applications

- Microprocessor Reset Controller
- Low Battery Detection
- Power Fail Indicator
- Battery Backup Detection

* The representative block diagrams depict active low reset output 'L' suffix devices. The comparator inputs are interchanged for the active high output ' H ' suffix devices.

This device contains 25 active transistors.
Figure 1. Representative Block Diagrams

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Power Supply Voltage (Pin 2) | $V_{\text {in }}$ | 12 | V |
| Output Voltage (Pin 1) <br> Complementary, NCP300 <br> N-Channel Open Drain, NCP301 | $\mathrm{V}_{\text {OUT }}$ | $\begin{gathered} -0.3 \text { to } V_{\text {in }}+0.3 \\ -0.3 \text { to } 12 \end{gathered}$ | V |
| Output Current (Pin 1) (Note 2) | Iout | 70 | mA |
| Thermal Resistance Junction to Air | $\mathrm{R}_{\text {өJA }}$ | 250 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Latch-up Performance <br> Positive <br> Negative | lıatch-up | $200$ | mA |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300/1-0.9 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET }}$ | 0.882 | 0.900 | 0.918 | V |
| Detector Threshold Hysteresis (Pin 2, Vin Increasing) | $\mathrm{V}_{\text {HYS }}$ | 0.027 | 0.045 | 0.063 | V |
| Supply Current (Pin 2) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.8 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=2.9 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ | - | $\begin{aligned} & 0.20 \\ & 0.45 \end{aligned}$ | $\begin{aligned} & 0.6 \\ & 1.2 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in }(\text { min }}$ ) | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP300 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | lout | $\begin{aligned} & 0.01 \\ & 0.05 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 0.05 \\ & 0.50 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right)$ <br> Pch Source Current, NCP300 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=0.8 \mathrm{~V}\right) \end{aligned}$ | lout | $\begin{gathered} 1.05 \\ 0.011 \\ 0.014 \end{gathered}$ | $\begin{gathered} 2.5 \\ 0.04 \\ 0.08 \end{gathered}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP300 Series Output Transition, High to Low Output Transition, Low to High N-Channel Open Drain NCP301 Series Output Transition, High to Low Output Transition, Low to High | $t_{\text {pHL }}$ <br> $t_{\text {pLH }}$ <br> $t_{p H L}$ <br> $t_{\text {pLH }}$ | - - - | $\begin{gathered} 97 \\ 77 \\ 97 \\ - \end{gathered}$ | $\begin{gathered} - \\ 300 \\ - \\ 300 \end{gathered}$ | $\mu \mathrm{S}$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300/1-1.8 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $V_{\text {DET- }}$ | 1.764 | 1.80 | 1.836 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.054 | 0.090 | 0.126 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=1.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=3.8 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.23 \\ & 0.48 \end{aligned}$ | $\begin{aligned} & 0.7 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP300 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ | - | mA |
| Reset Output Current (Pin 1, Active High ' H ' Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP300 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | lout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP300 Series Output Transition, High to Low Output Transition, Low to High <br> N-Channel Open Drain NCP301 Series Output Transition, High to Low Output Transition, Low to High | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - - - - | $\begin{aligned} & 73 \\ & 94 \\ & 73 \end{aligned}$ | $\begin{gathered} -\overline{1} \\ 300 \\ - \\ 300 \end{gathered}$ | us |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300/1-2.0 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 1.960 | 2.00 | 2.040 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.06 | 0.10 | 0.14 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=1.9 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=4.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.23 \\ & 0.48 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & \hline 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP300 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | lout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ | - | mA |
| Reset Output Current (Pin 1, Active High ' H ' Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP300 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | lout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP300 Series Output Transition, High to Low Output Transition, Low to High <br> N-Channel Open Drain NCP301 Series Output Transition, High to Low Output Transition, Low to High | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - | $\begin{gathered} 55 \\ 108 \\ \\ 55 \end{gathered}$ | $\begin{gathered} - \\ 300 \\ - \\ 300 \end{gathered}$ | us |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300/1-2.7 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 2.646 | 2.700 | 2.754 | V |
| Detector Threshold Hysteresis (Pin 2, Vin Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.081 | 0.135 | 0.189 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=2.6 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=4.7 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.26 \\ & 0.46 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP300, NCP301 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP300 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP300, NCP301 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP300 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP300 Series Output Transition, High to Low Output Transition, Low to High N-Channel Open Drain NCP301 Series Output Transition, High to Low Output Transition, Low to High | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - - - - | $\begin{gathered} 55 \\ 115 \end{gathered}$ $55$ | $\begin{gathered} -\overline{0} \\ 300 \\ - \\ 300 \end{gathered}$ | us |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300/1-3.0 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 2.94 | 3.00 | 3.06 | V |
| Detector Threshold Hysteresis (Pin 2, Vin Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.09 | 0.15 | 0.21 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=2.87 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.27 \\ & 0.47 \end{aligned}$ | $\begin{aligned} & 0.9 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP300, NCP301 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP300 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP300, NCP301 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP300 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ | - | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP300 Series Output Transition, High to Low Output Transition, Low to High N-Channel Open Drain NCP301 Series Output Transition, High to Low Output Transition, Low to High | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - - - - | $\begin{gathered} 49 \\ 115 \end{gathered}$ <br> 49 | - 300 - 300 | us |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300/1-4.5 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 4.410 | 4.500 | 4.590 | V |
| Detector Threshold Hysteresis (Pin 2, Vin Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.135 | 0.225 | 0.315 | V |
| $\begin{aligned} & \text { Supply Current }(\text { Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=4.34 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=6.5 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.33 \\ & 0.52 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.4 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP300, NCP301 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP300 $\left(\mathrm{V}_{\text {OUT }}=5.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.5 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 3.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP300, NCP301 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP300 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP300 Series Output Transition, High to Low Output Transition, Low to High N-Channel Open Drain NCP301 Series Output Transition, High to Low Output Transition, Low to High | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - - - - | $\begin{gathered} 49 \\ 130 \\ \\ 49 \end{gathered}$ | $\begin{gathered} -\overline{0} \\ 300 \\ - \\ 300 \end{gathered}$ | $\mu \mathrm{s}$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300/1-4.7 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 4.606 | 4.70 | 4.794 | V |
| Detector Threshold Hysteresis (Pin 2, Vin Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.141 | 0.235 | 0.329 | V |
| $\begin{aligned} & \text { Supply Current (Pin } 2) \\ & \left(\mathrm{V}_{\text {in }}=4.54 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=6.7 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.34 \\ & 0.53 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.4 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L’ Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP300 $\left(\mathrm{V}_{\text {OUT }}=5.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ \\ 1.5 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 3.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) <br> Nch Sink Current, NCP300, NCP301 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP300 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | lout | $\begin{gathered} 6.3 \\ \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ | - | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP300 Series Output Transition, High to Low Output Transition, Low to High N-Channel Open Drain NCP301 Series Output Transition, High to Low Output Transition, Low to High | $\begin{gathered} \mathrm{t}_{\mathrm{pHL}} \\ \mathrm{t}_{\mathrm{pLH}} \\ \mathrm{t}_{\mathrm{pHL}} \\ \mathrm{t}_{\mathrm{pLH}} \\ \hline \end{gathered}$ | - - - - | $\begin{gathered} 45 \\ 130 \\ \\ 45 \end{gathered}$ | $\begin{gathered} \overline{-} \\ 300 \\ \overline{3} \\ \hline \end{gathered}$ | $\mu \mathrm{s}$ |



NCP300 and NCP301 series are measured with a 10 pF capacitive load. NCP301 has an additional 470 k pullup resistor connected from the reset output to +5.0 V . The reset output voltage waveforms are shown for the active low ' L ' devices. The upper detector threshold, $\mathrm{V}_{\mathrm{DET}}+$ is the sum of the lower detector threshold, $\mathrm{V}_{\mathrm{DET}}$ plus the input hysteresis, $\mathrm{V}_{\mathrm{HYS}}$.

Figure 2. Propagation Delay Measurement Conditions

## NCP300, NCP301

Table 1. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP300 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current |  | Pch Source Current |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $\mathrm{V}_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High | $V_{\text {in }}$ Low | $V_{\text {in }}$ High |  |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\mathrm{HYS}}$ (V) |  |  | $\stackrel{l}{\text { in }}_{(\mu \mathrm{A})(1)}$ | $\stackrel{\mathrm{l}_{\text {in }}}{(\mu \mathrm{A})(2)}$ | $\underset{(\mathrm{mA})^{(3)}}{\mathrm{I}^{2}}$ | $\underset{(\mathrm{mA})^{(4)}}{\mathrm{I}_{\text {IOUT }}}$ | $\underset{(\mathrm{mA})^{(5)}}{\mathrm{I}^{(5)}}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ | Typ |
| NCP300LSN09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.3 | 0.5 | 0.05 | 0.5 | 2.0 |
| NCP300LSN10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  |  |  |  |  |
| NCP300LSN11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  | 1.0 |  |
| NCP300LSN12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |  |
| NCP300LSN13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |  |
| NCP300LSN14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |  |
| NCP300LSN15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  |  |  |  |
| NCP300LSN16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  | 2.0 |  |
| NCP300LSN17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |  |
| NCP300LSN18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |  |
| NCP300LSN19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |  |
| NCP300LSN20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 |  |  |  |  |  |
| NCP300LSN21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |  |
| NCP300LSN22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |  |
| NCP300LSN23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |  |
| NCP300LSN24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |  |
| NCP300LSN25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |  |
| NCP300LSN26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |  |
| NCP300LSN27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |  |
| NCP300LSN28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |  |
| NCP300LSN29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |  |
| NCP300LSN30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 |  |  |  |  |  |
| NCP300LSN31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |  |
| NCP300LSN32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |  |
| NCP300LSN33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |  |
| NCP300LSN34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |  |
| NCP300LSN35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |  |
| NCP300LSN36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |  |
| NCP300LSN37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |  |
| NCP300LSN38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |  |
| NCP300LSN39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |  |
| NCP300LSN40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 0.4 | 0.6 |  |  |  |
| NCP300LSN41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |  |
| NCP300LSN42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |  |
| NCP300LSN43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |  |
| NCP300LSN44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |  |
| NCP300LSN45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |  |
| NCP300LSN46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |  |
| NCP300LSN47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |  |
| NCP300LSN48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |  |
| NCP300LSN49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.05 \mathrm{~V}$, Active Low 'L' Suffix Devices
(4) Condition 4: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active Low 'L' Suffix Devices
(5) Condition 5: $0.9-3.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{in}}=4.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=2.4 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=5.9 \mathrm{~V}$, Active Low 'L' Suffix Devices

## NCP300, NCP301

Table 2. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP300 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current | Pch Source Current |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $V_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High | $V_{\text {in }}$ Low | $V_{\text {in }}$ High |  |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\text {HYS }}(\mathrm{V})$ |  |  | $\stackrel{\mathrm{l}_{\text {in }}}{(\mu \mathrm{A})}{ }^{(1)}$ | ${\underset{\text { in }}{(2 \mathrm{~A})}}_{(2)}^{\mathbf{l}^{2}}$ | $\underset{(\mathrm{mA})^{(3)}}{\mathrm{I}_{\text {OUT }}}$ | $\underset{(\mathrm{mA})^{(4)}}{\mathrm{I}^{2}}$ | $\underset{(\mathrm{mA})^{(5)}}{\mathrm{I}^{(5)}}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ | Typ |
| NCP300HSN09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.3 | 0.5 | 2.5 | 0.04 | 0.08 |
| NCP300HSN10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  |  |  |  |  |
| NCP300HSN11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  |  | 0.18 |
| NCP300HSN12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |  |
| NCP300HSN13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |  |
| NCP300HSN14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |  |
| NCP300HSN15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  | 11 |  |  |
| NCP300HSN16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  |  | 0.6 |
| NCP300HSN17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |  |
| NCP300HSN18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |  |
| NCP300HSN19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |  |
| NCP300HSN20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 |  |  |  |  |  |
| NCP300HSN21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |  |
| NCP300HSN22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |  |
| NCP300HSN23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |  |
| NCP300HSN24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |  |
| NCP300HSN25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |  |
| NCP300HSN26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |  |
| NCP300HSN27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |  |
| NCP300HSN28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |  |
| NCP300HSN29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |  |
| NCP300HSN30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 |  |  |  |  |  |
| NCP300HSN31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |  |
| NCP300HSN32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |  |
| NCP300HSN33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |  |
| NCP300HSN34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |  |
| NCP300HSN35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |  |
| NCP300HSN36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |  |
| NCP300HSN37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |  |
| NCP300HSN38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |  |
| NCP300HSN39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |  |
| NCP300HSN40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 0.4 |  |  |  |  |
| NCP300HSN41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |  |
| NCP300HSN42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |  |
| NCP300HSN43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |  |
| NCP300HSN44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |  |
| NCP300HSN45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |  |
| NCP300HSN46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |  |
| NCP300HSN47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |  |
| NCP300HSN48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |  |
| NCP300HSN49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-1.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.5-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active High 'H' Suffix Devices
(4) Condition 4: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.4 \mathrm{~V}$, Active High 'H' Suffix Devices
(5) Condition 5: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.8 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND} ; 1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND} ; 1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND}$, Active High ' H ' Suffix Devices

Table 3. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP301 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $V_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High | $V_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\mathrm{HYS}}$ (V) |  |  | $\stackrel{\mathrm{l}}{\text { in }}_{(\mu \mathrm{A})(1)}$ | $\underset{(\mu \mathrm{A})(2)}{\mathrm{l}_{\text {in }}}$ | $\begin{gathered} \mathrm{I}_{\mathrm{OUT}} \\ (\mathrm{~mA})^{(3)} \end{gathered}$ | $\begin{gathered} \mathrm{I}_{\text {OUT }} \\ (\mathrm{mA})^{(4)} \end{gathered}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ |
| NCP301LSN09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.3 | 0.5 | 0.05 | 0.5 |
| NCP301LSN10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  |  |  |  |
| NCP301LSN11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  | 1.0 |
| NCP301LSN12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |
| NCP301LSN13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |
| NCP301LSN14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |
| NCP301LSN15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  |  |  |
| NCP301LSN16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  | 2.0 |
| NCP301LSN17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |
| NCP301LSN18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |
| NCP301LSN19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |
| NCP301LSN20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 |  |  |  |  |
| NCP301LSN21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |
| NCP301LSN22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |
| NCP301LSN23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |
| NCP301LSN24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |
| NCP301LSN25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |
| NCP301LSN26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |
| NCP301LSN27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |
| NCP301LSN28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |
| NCP301LSN29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |
| NCP301LSN30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 |  |  |  |  |
| NCP301LSN31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |
| NCP301LSN32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |
| NCP301LSN33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |
| NCP301LSN34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |
| NCP301LSN35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |
| NCP301LSN36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |
| NCP301LSN37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |
| NCP301LSN38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |
| NCP301LSN39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |
| NCP301LSN40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 0.4 |  |  |  |
| NCP301LSN41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |
| NCP301LSN42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |
| NCP301LSN43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |
| NCP301LSN44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |
| NCP301LSN45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |
| NCP301LSN46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |
| NCP301LSN47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |
| NCP301LSN48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |
| NCP301LSN49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.05 \mathrm{~V}$, Active Low 'L’ Suffix Devices
(4) Condition 4: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V} ; 1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V} ; 1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active Low 'L' Suffix Devices

Table 4. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-1.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.5-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active High 'H' Suffix Devices

## NCP300, NCP301



Figure 3. NCP300/1 Series 0.9 V
Detector Threshold Voltage versus Temperature


Figure 5. NCP300/1 Series 4.5 V
Detector Threshold Voltage versus Temperature


Figure 4. NCP300/1 Series 2.7 V Detector Threshold Voltage versus Temperature


Figure 6. NCP300H/1L Series 0.9 V Reset Output Voltage versus Input Voltage


Figure 7. NCP300H/1L Series 2.7 V
Reset Output Voltage versus Input Voltage


Figure 8. NCP300H/1L Series 4.5 V Reset Output Voltage versus Input Voltage


Figure 9. NCP300H/1L Series 0.9 V Reset Output Sink Current versus Output Voltage


Figure 11. NCP300H/1L Series 4.5 V Reset Output Sink Current versus Output Voltage


Figure 13. NCP300/1 Series 2.7 V Input Current versus Input Voltage


Figure 10. NCP300H/1L Series 2.7 V Reset Output Sink Current versus Output Voltage


Figure 12. NCP300/1 Series 0.9 V Input Current versus Input Voltage


Figure 14. NCP300/1 Series 4.5 V Input Current versus Input Voltage


Figure 15. NCP300H/1L Series 0.9 V Reset Output Sink Current versus Input Voltage


Figure 17. NCP300H/1L Series 4.5 V Reset Output Sink Current versus Input Voltage


Figure 19. NCP300H Series 2.7 V
Reset Output Source Current versus Input Voltage


Figure 16. NCP300H/1L Series 2.7 V Reset Output Sink Current versus Input Voltage


Figure 18. NCP300H Series 0.9 V Reset Output Source Current versus Input Voltage


Figure 20. NCP300H Series 4.5 V
Reset Output Source Current versus Input Voltage

## OPERATING DESCRIPTION

The NCP300 and NCP301 series devices are second generation ultra-low current voltage detectors. Figures 21 and 22 show a timing diagram and a typical application. Initially consider that input voltage $\mathrm{V}_{\text {in }}$ is at a nominal level and it is greater than the voltage detector upper threshold $\left(\mathrm{V}_{\mathrm{DET}+}\right)$, and the reset output (Pin 1) will be in the high state for active low devices, or in the low state for active high devices. If there is a power interruption and $V_{\text {in }}$ becomes significantly deficient, it will fall below the lower detector threshold ( $\mathrm{V}_{\text {DET- }}$ ). This sequence of events causes the Reset output to be in the low state for active low devices, or in the
high state for active high devices. After completion of the power interruption, $\mathrm{V}_{\text {in }}$ will again return to its nominal level and become greater than the $\mathrm{V}_{\mathrm{DET}+}$. The voltage detector has built-in hysteresis to prevent erratic reset operation as the comparator threshold is crossed.
Although these device series are specifically designed for use as reset controllers in portable microprocessor based systems, they offer a cost-effective solution in numerous applications where precise voltage monitoring is required. Figure 22 through Figure 29 shows various application examples.


Figure 21. Timing Waveforms

## APPLICATION CIRCUIT INFORMATION



Figure 22. Microprocessor Reset Circuit


Figure 23. Battery Charge Indicator


Figure 24. Window Voltage Detector

## APPLICATION CIRCUIT INFORMATION



Figure 25. Dual Power Supply Undervoltage Supervision


Figure 26. Microprocessor Reset Circuit with Additional Hysteresis

Comparator hysteresis can be increased with the addition of resistor $\mathrm{R}_{\mathrm{H}}$. The hysteresis equations have been simplified and do not account for the change of input current $l_{\text {in }}$ as $V_{\text {in }}$ crosses the comparator threshold. The internal resistance, $\mathrm{R}_{\mathrm{in}}$ is simply calculated using $\mathrm{l}_{\text {in }}=0.26 \mu \mathrm{~A}$ at 2.6 V .
$V_{\text {in }}$ Decreasing:

$$
\mathrm{V}_{\mathrm{th}}=\left(\frac{\mathrm{R}_{\mathrm{H}}}{\mathrm{R}_{\mathrm{in}}}+1\right)\left(\mathrm{V}_{\mathrm{DET}-}\right)
$$

$V_{\text {in }}$ Increasing:

$$
\mathrm{V}_{\mathrm{th}}=\left(\frac{\mathrm{R}_{\mathrm{H}}}{\mathrm{R}_{\mathrm{in}} \| \mathrm{R}_{\mathrm{L}}}+1\right)\left(\mathrm{V}_{\mathrm{DET}-}+\mathrm{V}_{\mathrm{HYS}}\right)
$$

| Test Data |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathbf{V}_{\text {th }}$ Decreasing <br> $(\mathbf{m V})$ | $\mathbf{V}_{\text {th }}$ Increasing <br> $(\mathbf{m V})$ | $\mathbf{V}_{\mathbf{H Y s}}$ <br> $(\mathbf{m V})$ | $\mathbf{R}_{\mathbf{H}}$ <br> $(\Omega)$ | $\mathbf{R}_{\mathbf{L}}$ <br> $(\mathbf{k} \Omega)$ |
| 2.70 | 2.84 | 0.135 | 0 | - |
| 2.70 | 2.87 | 0.17 | 100 | 10 |
| 2.70 | 2.88 | 0.19 | 100 | 6.8 |
| 2.70 | 2.91 | 0.21 | 100 | 4.3 |
| 2.70 | 2.90 | 0.20 | 220 | 10 |
| 2.70 | 2.94 | 0.24 | 220 | 6.8 |
| 2.70 | 2.98 | 0.28 | 220 | 4.3 |
| 2.70 | 2.70 | 0.27 | 470 | 10 |
| 2.70 | 3.04 | 0.34 | 470 | 6.8 |
| 2.70 | 3.15 | 0.35 | 470 | 4.3 |

$\mathrm{V}_{\text {HYS }}=\mathrm{V}_{\text {in }}$ Increasing $-\mathrm{V}_{\text {in }}$ Decreasing


Figure 27. Simple Clock Oscillator


This circuit monitors the current at the load. As current flows through the load, a voltage drop with respect to ground appears across $R_{\text {sense }}$ where $V_{\text {sense }}=I_{\text {load }}{ }^{*} R_{\text {sense. }}$. The following conditions apply:

If: Then:
$\mathrm{I}_{\text {Load }}<\mathrm{V}_{\text {DET- }} / \mathrm{R}_{\text {sense }}$ $\mathrm{L}_{\text {Load }} \geq\left(\mathrm{V}_{\text {DET-+ }} \mathrm{V}_{\text {HYS }}\right) / \mathrm{R}_{\text {sense }}$

Reset Output $=0 \mathrm{~V}$
Reset Output = $\mathrm{V}_{\mathrm{DD}}$

Figure 28. Microcontroller System Load Sensing


A simple voltage monitor can be constructed by connecting several voltage detectors as shown above. Each LED will sequentially turn on when the respective voltage detector threshold ( $\mathrm{V}_{\mathrm{DET}}+\mathrm{V}_{\mathrm{HYS}}$ ) is exceeded. Note that detector thresholds ( $\mathrm{V}_{\text {DET- }}$ ) that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

Figure 29. LED Bar Graph Voltage Monitor

## NCP300, NCP301

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


THIN SOT-23-5

ORDERING INFORMATION

| Device | Threshold Voltage | Output Type | Reset | Marking | Package (Qty/Reel) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP300LSN09T1 | 0.9 | CMOS | Active Low | SEJ | 3000 Units on 7 inch Reel |
| NCP300LSN18T1 | 1.8 |  |  | SFK |  |
| NCP300LSN20T1 | 2.0 |  |  | SHE |  |
| NCP300LSN27T1 | 2.7 |  |  | SEE |  |
| NCP300LSN28T1 | 2.8 |  |  | SED |  |
| NCP300LSN30T1 | 3.0 |  |  | SEC |  |
| NCP300LSN33T1 | 3.3 |  |  | SKV |  |
| NCP300LSN34T1 | 3.4 |  |  | SKU |  |
| NCP300LSN44T1 | 4.4 |  |  | SKK |  |
| NCP300LSN45T1 | 4.5 |  |  | SEA |  |
| NCP300LSN47T1 | 4.7 |  |  | SDZ |  |
| NCP300HSN09T1 | 0.9 |  |  | SDY |  |
| NCP300HSN18T1 | 1.8 |  |  | SFJ |  |
| NCP300HSN27T1 | 2.7 |  | Active | SDU |  |
| NCP300HSN30T1 | 3.0 |  | High | SDS |  |
| NCP300HSN45T1 | 4.5 |  |  | SDQ |  |
| NCP300HSN47T1 | 4.7 |  |  | SDP |  |
| NCP301LSN09T1 | 0.9 |  |  | SFF |  |
| NCP301LSN12T1 | 1.2 |  |  | SNN |  |
| NCP301LSN18T1 | 1.8 |  |  | SFN |  |
| NCP301LSN20T1 | 2.0 |  |  | SFD |  |
| NCP301LSN22T1 | 2.2 |  |  | SNG |  |
| NCP301LSN25T1 | 2.5 |  |  | SNF |  |
| NCP301LSN27T1 | 2.7 |  | $\begin{aligned} & \text { Active } \\ & \text { Low } \end{aligned}$ | SFA |  |
| NCP301LSN28T1 | 2.8 |  |  | SEZ |  |
| NCP301LSN30T1 | 3.0 | Open |  | SEY |  |
| NCP301LSN33T1 | 3.3 | Drain |  | SNB |  |
| NCP301LSN40T1 | 4.0 |  |  | SMU |  |
| NCP301LSN45T1 | 4.5 |  |  | SEV |  |
| NCP301LSN47T1 | 4.7 |  |  | SEU |  |
| NCP301HSN09T1 | 0.9 |  | Active High | SET |  |
| NCP301HSN18T1 | 1.8 |  |  | SFM |  |
| NCP301HSN27T1 | 2.7 |  |  | SEP |  |
| NCP301HSN30T1 | 3.0 |  |  | SEN |  |
| NCP301HSN45T1 | 4.5 |  |  | SEL |  |

NOTE: The ordering information lists seven standard under voltage thresholds with active low outputs. Additional active low threshold devices, ranging from 0.9 V to 4.9 V in 100 mV increments and NCP300/NCP301 active high output devices, ranging from 0.9 V to 4.9 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability. The electrical characteristics of these additional devices are shown in Tables 1 and 2.

## NCP304, NCP305

## Voltage Detector Series

The NCP304 and NCP305 series are second generation ultra-low current voltage detectors. These devices are specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is paramount.

Each series features a highly accurate under voltage detector with hysteresis which prevents erratic system reset operation as the comparator threshold is crossed.

The NCP304 series consists of complementary output devices that are available with either an active high or active low reset output. The NCP305 series has an open drain N-channel output with an active low reset output.

The NCP304 and NCP305 device series are available in the SC-82AB package with seven standard under voltage thresholds. Additional thresholds that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

## Features

- Quiescent Current of $1.0 \mu \mathrm{~A}$ Typical
- High Accuracy Under Voltage Threshold of $2.0 \%$
- Wide Operating Voltage Range of 0.8 V to 10 V
- Complementary or Open Drain Reset Output
- Active Low or Active High Reset Output


## Typical Applications

- Microprocessor Reset Controller
- Low Battery Detection
- Power Fail Indicator
- Battery Backup Detection


## PIN CONNECTIONS AND <br> MARKING DIAGRAM



## ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 2759 of this data sheet.

NCP305LSQxxT1
Open Drain Output Configuration


This device contains 38 active transistors.

## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


1
SC-82AB
SQ SUFFIX
CASE 419C
$\qquad$

NCP304xSQxxT1
Complementary Output Configuration

* The representative block diagram depicts active low reset output 'L' suffix devices. The comparator input is interchanged for the active high output ' H ' suffix devices.

Figure 1. Representative Block Diagrams

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Power Supply Voltage (Pin 2) | $\mathrm{V}_{\text {in }}$ | 12 | V |
| Output Voltage (Pin 1) <br> Complementary, NCP304 <br> N-Channel Open Drain, NCP305 | $\mathrm{V}_{\text {OUT }}$ |  | V |
| Output Current (Pin 1) (Note 2) |  | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ <br> -0.3 to 12 |  |
| Thermal Resistance Junction to Air | $\mathrm{I}_{\text {OUT }}$ | 70 | mA |
| Operating Junction Temperature Range | $\mathrm{R}_{\text {日JA }}$ | 285 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Latch-up Performance <br> Positive <br> Negative | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304/5-0.9 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET }}$ | 0.882 | 0.900 | 0.918 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.027 | 0.045 | 0.063 | V |
| Supply Current (Pin 2) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.8 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=2.9 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\text {in }}$ | - | $\begin{gathered} 0.8 \\ - \end{gathered}$ | $\begin{aligned} & 2.4 \\ & 3.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in }(\text { min }}$ ) | $-$ | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | IOUT | $\begin{aligned} & 0.01 \\ & 0.05 \\ & \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 0.05 \\ & 0.50 \\ & 2.0 \end{aligned}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right)$ <br> Pch Source Current, NCP304 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=0.8 \mathrm{~V}\right) \end{aligned}$ | IOUT | $\begin{aligned} & 1.05 \\ & \\ & 0.011 \\ & 0.014 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & \\ & 0.04 \\ & 0.08 \end{aligned}$ | $\begin{aligned} & - \\ & - \end{aligned}$ | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP304 Series Output Transition, High to Low (Note 3) Output Transition, Low to High (Note 3) N-Channel Open Drain NCP305 Series Output Transition, High to Low (Note 3) Output Transition, Low to High (Note 3) | $t_{\text {pHL }}$ <br> $t_{\text {pLH }}$ <br> $t_{p H L}$ <br> $t_{\text {pLH }}$ | - - - - | $\begin{gathered} 18 \\ 6.0 \\ 18 \\ - \end{gathered}$ | $\begin{gathered} - \\ 100 \\ - \\ 100 \end{gathered}$ | $\mu \mathrm{s}$ |

3. In the case of CMOS Output Type: The time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to (+ $\mathrm{V}_{\mathrm{DET}}$ ) +2.0 V and output voltage level becoming to $\mathrm{V}_{\mathrm{DD}} / 2$. In the case of $\mathrm{N}_{\mathrm{CH}}$ Open Drain Output Type: Output pin is pulled up with a resistance of $470 \mathrm{k} \Omega$ to 5.0 V , the time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to $\left(+\mathrm{V}_{\mathrm{DET}}\right)+2.0 \mathrm{~V}$ and output voltage level becoming to 2.5 .

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304/5-1.8 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 1.764 | 1.80 | 1.836 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.054 | 0.090 | 0.126 | V |
| $\begin{aligned} & \hline \text { Supply Current }(\text { Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=1.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=3.8 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.8 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 2.4 \\ & 3.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP304, NCP305 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ | - | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP304 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ | - | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP304 Series Output Transition, High to Low (Note 4) Output Transition, Low to High (Note 4) N-Channel Open Drain NCP305 Series Output Transition, High to Low (Note 4) Output Transition, Low to High (Note 4) | $\mathrm{t}_{\mathrm{pH}}$ $t_{p L H}$ <br> $\mathrm{t}_{\mathrm{pH}}$ $\mathrm{t}_{\mathrm{pLH}}$ | - - - - | $\begin{aligned} & 14 \\ & 15 \\ & \\ & 14 \end{aligned}$ | $\begin{gathered} - \\ 100 \\ - \\ 100 \end{gathered}$ | $\mu \mathrm{S}$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304/5-2.0 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 1.960 | 2.00 | 2.040 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.06 | 0.10 | 0.14 | V |
| $\begin{aligned} & \hline \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=1.9 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=4.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.9 \\ & 1.1 \end{aligned}$ | $\begin{aligned} & 2.7 \\ & 3.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L’ Suffix Devices) Nch Sink Current, NCP304, NCP305 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | lout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP304, NCP305 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP304 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | lout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ \\ 0.04 \\ 0.6 \end{gathered}$ | - | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP304 Series Output Transition, High to Low (Note 4) Output Transition, Low to High (Note 4) N-Channel Open Drain NCP305 Series Output Transition, High to Low (Note 4) Output Transition, Low to High (Note 4) | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - | 13 15 13 | $\begin{gathered} - \\ 100 \\ - \\ 100 \end{gathered}$ | us |

4. In the case of CMOS Output Type: The time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to $\left(+\mathrm{V}_{\mathrm{DET}}\right)+2.0 \mathrm{~V}$ and output voltage level becoming to $\mathrm{V}_{\mathrm{DD}} / 2$. In the case of $\mathrm{N}_{\mathrm{CH}}$ Open Drain Output Type: Output pin is pulled up with a resistance of $470 \mathrm{k} \Omega$ to 5.0 V , the time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to $\left(+\mathrm{V}_{\mathrm{DET}}\right)+2.0 \mathrm{~V}$ and output voltage level becoming to 2.5.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304/5-2.7 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 2.646 | 2.700 | 2.754 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.081 | 0.135 | 0.189 | V |
| $\begin{aligned} & \hline \text { Supply Current }(\text { Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=2.6 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=4.7 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.9 \\ & 1.1 \end{aligned}$ | $\begin{aligned} & 2.7 \\ & 3.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP304, NCP305 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ | - | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP304 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ | - | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP304 Series Output Transition, High to Low (Note 5) Output Transition, Low to High (Note 5) N-Channel Open Drain NCP305 Series Output Transition, High to Low (Note 5) Output Transition, Low to High (Note 5) | $\mathrm{t}_{\mathrm{pH}}$ $t_{p L H}$ <br> $\mathrm{t}_{\mathrm{pH}}$ $\mathrm{t}_{\mathrm{pLH}}$ | - - - - | $\begin{aligned} & 12 \\ & 19 \\ & 12 \end{aligned}$ | $\begin{gathered} - \\ 100 \\ - \\ 100 \end{gathered}$ | us |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304/5-3.0 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 2.94 | 3.00 | 3.06 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.09 | 0.15 | 0.21 | V |
| $\begin{aligned} & \hline \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=2.87 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 1.0 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.6 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | lout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP304, NCP305 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP304 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=G N D, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | lout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ \\ 0.04 \\ 0.6 \end{gathered}$ | - | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP304 Series Output Transition, High to Low (Note 5) Output Transition, Low to High (Note 5) N-Channel Open Drain NCP305 Series Output Transition, High to Low (Note 5) Output Transition, Low to High (Note 5) | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - | $\begin{aligned} & 12 \\ & 19 \\ & 12 \end{aligned}$ | - 100 - 100 | us |

5. In the case of CMOS Output Type: The time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to $\left(+\mathrm{V}_{\mathrm{DET}}\right)+2.0 \mathrm{~V}$ and output voltage level becoming to $\mathrm{V}_{\mathrm{DD}} / 2$. In the case of $\mathrm{N}_{\mathrm{CH}}$ Open Drain Output Type: Output pin is pulled up with a resistance of $470 \mathrm{k} \Omega$ to 5.0 V , the time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to $\left(+\mathrm{V}_{\mathrm{DET}}\right)+2.0 \mathrm{~V}$ and output voltage level becoming to 2.5.

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304/5-4.5 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $V_{\text {DET- }}$ | 4.410 | 4.500 | 4.590 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.135 | 0.225 | 0.315 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=4.34 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=6.5 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | - | $\begin{aligned} & 3.0 \\ & 3.9 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & \hline 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=5.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.5 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 3.0 \end{gathered}$ | - | mA |
| Reset Output Current (Pin 1, Active High ' H ' Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP304 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | lout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP304 Series Output Transition, High to Low (Note 6) Output Transition, Low to High (Note 6) N-Channel Open Drain NCP305 Series Output Transition, High to Low (Note 6) Output Transition, Low to High (Note 6) | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - | $\begin{aligned} & 10 \\ & 21 \\ & 10 \end{aligned}$ | $\begin{gathered} - \\ 100 \\ - \\ 100 \end{gathered}$ | us |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304/5-4.7 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 4.606 | 4.70 | 4.794 | V |
| Detector Threshold Hysteresis (Pin 2, Vin Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.141 | 0.235 | 0.329 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=4.54 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=6.7 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ | - | $\begin{aligned} & 1.1 \\ & 1.3 \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 3.9 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L’ Suffix Devices) <br> Nch Sink Current, NCP304, NCP305 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=5.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | lout | $\begin{gathered} 0.01 \\ 1.0 \\ \\ 1.5 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 3.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High ' H ' Suffix Devices) Nch Sink Current, NCP304, NCP305 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP304 $\left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right)$ $\left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right)$ | lout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| Propagation Delay Input to Output (Figure 2) Complementary Output NCP304 Series Output Transition, High to Low (Note 6) Output Transition, Low to High (Note 6) N-Channel Open Drain NCP305 Series Output Transition, High to Low (Note 6) Output Transition, Low to High (Note 6) | $\begin{aligned} & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \mathrm{t}_{\mathrm{pHL}} \\ & \mathrm{t}_{\mathrm{pLH}} \\ & \hline \end{aligned}$ | - | $\begin{aligned} & 10 \\ & 21 \\ & 10 \end{aligned}$ | $\begin{gathered} - \\ 100 \\ - \\ 100 \end{gathered}$ | $\mu \mathrm{S}$ |

6. In the case of CMOS Output Type: The time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to $\left(+\mathrm{V}_{\mathrm{DET}}\right)+2.0 \mathrm{~V}$ and output voltage level becoming to $\mathrm{V}_{\mathrm{DD}} / 2$. In the case of $\mathrm{N}_{\mathrm{CH}}$ Open Drain Output Type: Output pin is pulled up with a resistance of $470 \mathrm{k} \Omega$ to 5.0 V , the time interval between the rising edge of $\mathrm{V}_{\mathrm{DD}}$ input pulse from 0.7 V to $\left(+\mathrm{V}_{\mathrm{DET}}\right)+2.0 \mathrm{~V}$ and output voltage level becoming to 2.5.


NCP304 and NCP305 series are measured with a 10 pF capacitive load. NCP305 has an additional 470 k pullup resistor connected from the reset output to +5.0 V . The reset output voltage waveforms are shown for the active low ' L ' devices. The upper detector threshold, $\mathrm{V}_{\mathrm{DET}+}$ is the sum of the lower detector threshold, $\mathrm{V}_{\mathrm{DET}}$ plus the input hysteresis, $\mathrm{V}_{\mathrm{HYS}}$.

Figure 2. Propagation Delay Measurement Conditions

## NCP304, NCP305

Table 1. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP304 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current |  | Pch <br> Source <br> Current |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $V_{\text {in }}$ Low | $V_{\text {in }}$ High | $V_{\text {in }}$ Low | $V_{\text {in }}$ High |  |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\mathrm{HYS}}$ (V) |  |  | ${\underset{\text { in }}{(1)}}_{(\mu \mathrm{A})(1)}$ | $\stackrel{l}{\text { in }}_{(\mu \mathrm{A})(2)}$ | $\begin{gathered} \text { IOUT }_{(3)} \\ (\mathrm{mA})^{(3)} \end{gathered}$ | $\begin{gathered} \text { IOUT }^{(\mathrm{mA})}{ }^{(4)} \end{gathered}$ | $\underset{(\mathrm{mA})^{(5)}}{\mathrm{I}_{\text {OUT }}}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ | Typ |
| NCP304LSQ09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.8 | 0.9 | 0.05 | 0.5 | 2.0 |
| NCP304LSQ10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  | 1.0 |  |  |  |
| NCP304LSQ11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  | 1.0 |  |
| NCP304LSQ12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |  |
| NCP304LSQ13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |  |
| NCP304LSQ14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |  |
| NCP304LSQ15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  |  |  |  |
| NCP304LSQ16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  | 2.0 |  |
| NCP304LSQ17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |  |
| NCP304LSQ18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |  |
| NCP304LSQ19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |  |
| NCP304LSQ20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 | 0.9 | 1.1 |  |  |  |
| NCP304LSQ21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |  |
| NCP304LSQ22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |  |
| NCP304LSQ23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |  |
| NCP304LSQ24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |  |
| NCP304LSQ25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |  |
| NCP304LSQ26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |  |
| NCP304LSQ27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |  |
| NCP304LSQ28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |  |
| NCP304LSQ29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |  |
| NCP304LSQ30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 | 1.0 | 1.2 |  |  |  |
| NCP304LSQ31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |  |
| NCP304LSQ32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |  |
| NCP304LSQ33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |  |
| NCP304LSQ34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |  |
| NCP304LSQ35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |  |
| NCP304LSQ36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |  |
| NCP304LSQ37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |  |
| NCP304LSQ38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |  |
| NCP304LSQ39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |  |
| NCP304LSQ40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 1.1 | 1.3 |  |  | 3.0 |
| NCP304LSQ41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |  |
| NCP304LSQ42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |  |
| NCP304LSQ43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |  |
| NCP304LSQ44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |  |
| NCP304LSQ45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |  |
| NCP304LSQ46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |  |
| NCP304LSQ47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |  |
| NCP304LSQ48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |  |
| NCP304LSQ49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET }}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.05 \mathrm{~V}$, Active Low 'L' Suffix Devices
(4) Condition 4: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active Low 'L’ Suffix Devices
(5) Condition 5: $0.9-3.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{in}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=2.4 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=5.9 \mathrm{~V}$, Active Low 'L' Suffix Devices

## NCP304, NCP305

Table 2. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP304 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | $\begin{gathered} \text { Nch } \\ \text { Sink } \\ \text { Current } \end{gathered}$ | Pch Source Current |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $V_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High | $V_{\text {in }}$ Low | $V_{\text {in }}$ High |  |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\mathrm{HYS}}$ (V) |  |  | $\stackrel{\mathrm{l}}{\text { in }}_{(\mu \mathrm{A})}$ | ${\underset{\text { in }}{ }}_{(\mu \mathrm{A})^{(2)}}$ | $\stackrel{\text { Iout }}{(\mathrm{mA})^{(3)}}$ | $\underset{(\mathrm{mA})^{(4)}}{\mathrm{I}_{\text {OUT }}}$ | $\begin{aligned} & \text { Iout }_{(5)} \\ & (\mathrm{mA})(5) \end{aligned}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ | Typ |
| NCP304HSQ09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.8 | 0.9 | 2.5 | 0.04 | 0.08 |
| NCP304HSQ10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  | 1.0 |  |  |  |
| NCP304HSQ11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  |  | 0.18 |
| NCP304HSQ12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |  |
| NCP304HSQ13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |  |
| NCP304HSQ14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |  |
| NCP304HSQ15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  | 11 |  |  |
| NCP304HSQ16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  |  | 0.6 |
| NCP304HSQ17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |  |
| NCP304HSQ18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |  |
| NCP304HSQ19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |  |
| NCP304HSQ20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 | 0.9 | 1.1 |  |  |  |
| NCP304HSQ21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |  |
| NCP304HSQ22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |  |
| NCP304HSQ23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |  |
| NCP304HSQ24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |  |
| NCP304HSQ25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |  |
| NCP304HSQ26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |  |
| NCP304HSQ27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |  |
| NCP304HSQ28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |  |
| NCP304HSQ29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |  |
| NCP304HSQ30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 | 1.0 | 1.2 |  |  |  |
| NCP304HSQ31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |  |
| NCP304HSQ32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |  |
| NCP304HSQ33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |  |
| NCP304HSQ34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |  |
| NCP304HSQ35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |  |
| NCP304HSQ36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |  |
| NCP304HSQ37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |  |
| NCP304HSQ38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |  |
| NCP304HSQ39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |  |
| NCP304HSQ40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 1.1 | 1.3 |  |  |  |
| NCP304HSQ41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |  |
| NCP304HSQ42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |  |
| NCP304HSQ43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |  |
| NCP304HSQ44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |  |
| NCP304HSQ45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |  |
| NCP304HSQ46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |  |
| NCP304HSQ47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |  |
| NCP304HSQ48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |  |
| NCP304HSQ49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET }}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{in}}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.5-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active High 'H' Suffix Devices
(4) Condition 4: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.4 \mathrm{~V}$, Active High 'H' Suffix Devices
(5) Condition 5: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.8 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND} ; 1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND} ; 1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND}$, Active High ' H ' Suffix Devices

## NCP304, NCP305

Table 3. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP305 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $V_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High | $\mathrm{V}_{\text {in }}$ Low | $V_{\text {in }}$ High |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\mathrm{HYS}}$ (V) |  |  | ${\underset{\text { in }}{(1 \mathrm{~A})}}_{(1)}$ | ${\underset{\text { in }}{ }}_{(\mu \mathrm{A})(2)}$ | $\underset{(\mathrm{mA})^{(3)}}{\mathrm{I}^{2}}$ | $\underset{(\mathrm{mA})^{(4)}}{\mathrm{I}^{2}}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ |
| NCP305LSQ09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.8 | 0.9 | 0.05 | 0.5 |
| NCP305LSQ10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  | 1.0 |  |  |
| NCP305LSQ11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  | 1.0 |
| NCP305LSQ12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |
| NCP305LSQ13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |
| NCP305LSQ14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |
| NCP305LSQ15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  |  |  |
| NCP305LSQ16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  | 2.0 |
| NCP305LSQ17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |
| NCP305LSQ18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |
| NCP305LSQ19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |
| NCP305LSQ20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 | 0.9 | 1.1 |  |  |
| NCP305LSQ21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |
| NCP305LSQ22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |
| NCP305LSQ23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |
| NCP305LSQ24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |
| NCP305LSQ25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |
| NCP305LSQ26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |
| NCP305LSQ27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |
| NCP305LSQ28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |
| NCP305LSQ29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |
| NCP305LSQ30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 | 1.0 | 1.2 |  |  |
| NCP305LSQ31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |
| NCP305LSQ32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |
| NCP305LSQ33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |
| NCP305LSQ34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |
| NCP305LSQ35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |
| NCP305LSQ36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |
| NCP305LSQ37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |
| NCP305LSQ38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |
| NCP305LSQ39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |
| NCP305LSQ40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 1.1 | 1.3 |  |  |
| NCP305LSQ41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |
| NCP305LSQ42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |
| NCP305LSQ43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |
| NCP305LSQ44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |
| NCP305LSQ45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |
| NCP305LSQ46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |
| NCP305LSQ47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |
| NCP305LSQ48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |
| NCP305LSQ49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET }}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.05 \mathrm{~V}$, Active Low 'L' Suffix Devices
(4) Condition 4: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V} ; 1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V} ; 1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active Low 'L’ Suffix Devices


Figure 3. NCP304/5 Series 0.9 V Detector Threshold Voltage vs. Temperature


Figure 5. NCP304/5 Series 4.5 V Detector Threshold Voltage vs. Temperature


Figure 4. NCP304/5 Series 2.7 V Detector Threshold Voltage vs. Temperature


Figure 6. NCP304H/5L Series 0.9 V Reset Output Voltage vs. Input Voltage


Figure 7. NCP304H/5L Series 2.7 V Reset Output Voltage vs. Input Voltage


Figure 8. NCP304H/5L Series 4.5 V Reset Output Voltage vs. Input Voltage


Figure 9. NCP304H/5H Series 2.7 V Reset Output Voltage vs. Input Voltage


Figure 11. NCP304H/5L Series 2.7 V Reset Output Sink Current vs. Output Voltage


Figure 13. NCP304H Series 2.7 V Reset Output Source Current vs. Output Voltage


Figure 10. NCP304H/5L Series 0.9 V Reset Output Sink Current vs. Output Voltage


Figure 12. NCP304H/5L Series 4.5 V Reset Output Sink Current vs. Output Voltage


Figure 14. NCP304/5 Series 0.9 V Input Current vs. Input Voltage


Figure 15. NCP304/5 Series 2.7 V Input Current vs. Input Voltage


Figure 17. NCP304H/5L Series 0.9 V Reset Output Sink Current vs. Input Voltage


Figure 19. NCP304H/5L Series 4.5 V
Reset Output Sink Current vs. Input Voltage


Figure 16. NCP304/5 Series 4.5 V Input Current vs. Input Voltage


Figure 18. NCP304H/5L Series 2.7 V Reset Output Sink Current vs. Input Voltage


Figure 20. NCP304H/5H Series 2.7 V Reset Output Sink Current vs. Input Voltage


Figure 21. NCP304H Series 0.9 V
Reset Output Source Current vs. Input Voltage


Figure 23. NCP304H Series 4.5 V
Reset Output Source Current vs. Input Voltage


Figure 22. NCP304H Series 2.7 V Reset Output Source Current vs. Input Voltage


Figure 24. NCP304H Series 2.7 V Reset Output Source Current vs. Input Voltage

## OPERATING DESCRIPTION

The NCP304 and NCP305 series devices are second generation ultra-low current voltage detectors. Figures 25 and 26 show a timing diagram and a typical application. Initially consider that input voltage $\mathrm{V}_{\text {in }}$ is at a nominal level and it is greater than the voltage detector upper threshold $\left(\mathrm{V}_{\mathrm{DET}+}\right)$, and the reset output (Pin 1) will be in the high state for active low devices, or in the low state for active high devices. If there is a power interruption and $V_{\text {in }}$ becomes significantly deficient, it will fall below the lower detector threshold ( $\mathrm{V}_{\text {DET- }}$ ). This sequence of events causes the Reset output to be in the low state for active low devices, or in the
high state for active high devices. After completion of the power interruption, $\mathrm{V}_{\text {in }}$ will again return to its nominal level and become greater than the $\mathrm{V}_{\mathrm{DET}+}$. The voltage detector has built-in hysteresis to prevent erratic reset operation as the comparator threshold is crossed.
Although these device series are specifically designed for use as reset controllers in portable microprocessor based systems, they offer a cost-effective solution in numerous applications where precise voltage monitoring is required. Figure 26 through Figure 32 shows various application examples.


Figure 25. Timing Waveforms

APPLICATION CIRCUIT INFORMATION


Figure 26. Microprocessor Reset Circuit


Figure 27. Battery Charge Indicator


Figure 28. Dual Power Supply Undervoltage Supervision


Figure 29. Microprocessor Reset Circuit with Additional Hysteresis

Comparator hysteresis can be increased with the addition of resistor $R_{H}$. The hysteresis equations have been simplified and do not account for the change of input current $l_{\text {in }}$ as $V_{\text {in }}$ crosses the comparator threshold. The internal resistance, $\mathrm{R}_{\mathrm{in}}$ is simply calculated using $\mathrm{I}_{\text {in }}=0.26 \mu \mathrm{~A}$ at 2.6 V .
$V_{\text {in }}$ Decreasing:

$$
\mathrm{V}_{\mathrm{th}}=\left(\frac{\mathrm{R}_{\mathrm{H}}}{\mathrm{R}_{\mathrm{in}}}+1\right)\left(\mathrm{V}_{\mathrm{DET}-}\right)
$$

$\mathrm{V}_{\text {in }}$ Increasing:

$$
\mathrm{V}_{\mathrm{th}}=\left(\frac{\mathrm{R}_{\mathrm{H}}}{\mathrm{R}_{\mathrm{in}} \| \mathrm{R}_{\mathrm{L}}}+1\right)\left(\mathrm{V}_{\mathrm{DET}-}+\mathrm{V}_{\mathrm{HYS}}\right)
$$

$\mathrm{V}_{\text {HYS }}=\mathrm{V}_{\text {in }}$ Increasing $-\mathrm{V}_{\text {in }}$ Decreasing

| Test Data |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathbf{V}_{\text {th }}$ Decreasing <br> $(\mathbf{m V})$ | $\mathbf{V}_{\text {th }}$ Increasing <br> $(\mathbf{m V})$ | $\mathbf{V}_{\text {HYs }}$ <br> $(\mathbf{m V})$ | $\mathbf{R}_{\mathbf{H}}$ <br> $(\Omega)$ | $\mathbf{R}_{\mathbf{L}}$ <br> $(\mathbf{k} \boldsymbol{\Omega})$ |
| 2.70 | 2.84 | 0.135 | 0 | - |
| 2.70 | 2.87 | 0.17 | 100 | 10 |
| 2.70 | 2.88 | 0.19 | 100 | 6.8 |
| 2.70 | 2.91 | 0.21 | 100 | 4.3 |
| 2.70 | 2.90 | 0.20 | 220 | 10 |
| 2.70 | 2.94 | 0.24 | 220 | 6.8 |
| 2.70 | 2.98 | 0.28 | 220 | 4.3 |
| 2.70 | 2.70 | 0.27 | 470 | 10 |
| 2.70 | 3.04 | 0.34 | 470 | 6.8 |
| 2.70 | 3.15 | 0.35 | 470 | 4.3 |



| Test Data |  |  |
| :---: | :---: | :---: |
| $\mathbf{C}(\mu \mathrm{F})$ | $\mathrm{f}_{\mathrm{OsC}}(\mathbf{k H z})$ | $\mathrm{I}_{\mathbf{Q}}(\mu \mathbf{A})$ |
| 0.01 | 2590 | 21.77 |
| 0.1 | 490 | 21.97 |
| 1.0 | 52 | 22.07 |

Figure 30. Simple Clock Oscillator


This circuit monitors the current at the load. As current flows through the load, a voltage drop with respect to ground appears across $R_{\text {sense }}$ where $V_{\text {sense }}=I_{\text {load }}{ }^{*} R_{\text {sense. }}$. The following conditions apply:
If:
$I_{\text {Load }}<\mathrm{V}_{\text {DET- }} / \mathrm{R}_{\text {sense }}$
$\mathrm{l}_{\text {Load }} \geq\left(\mathrm{V}_{\mathrm{DET}}+\mathrm{V}_{\text {HYS }}\right) / \mathrm{R}_{\text {sense }}$

Then:
Reset Output = 0 V
Reset Output $=V_{D D}$

Figure 31. Microcontroller Systems Load Sensing


A simple voltage monitor can be constructed by connecting several voltage detectors as shown above. Each LED will sequentially turn on when the respective voltage detector threshold ( $\mathrm{V}_{\mathrm{DET}-}+\mathrm{V}_{\mathrm{HYS}}$ ) is exceeded. Note that detector thresholds ( $\mathrm{V}_{\text {DET- }}$ ) that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

Figure 32. LED Bar Graph

## INFORMATION FOR USING THE SC-82AB SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


ORDERING INFORMATION

| Device | Threshold Voltage | Output Type | Reset | Marking | Package (Qty/Reel) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP304LSQ09T1 | 0.9 | CMOS | Active Low | SHG | 3000 Units on 7 inch Reel |
| NCP304LSQ18T1 | 1.8 |  |  | SGX |  |
| NCP304LSQ20T1 | 2.0 |  |  | SGV |  |
| NCP304LSQ27T1 | 2.7 |  |  | SGN |  |
| NCP304LSQ30T1 | 3.0 |  |  | SGJ |  |
| NCP304LSQ33T1 | 3.3 |  |  | SGG |  |
| NCP304LSQ40T1 | 4.0 |  |  | SFY |  |
| NCP304LSQ42T1 | 4.2 |  |  | SFU |  |
| NCP304LSQ45T1 | 4.5 |  |  | SFS |  |
| NCP304LSQ47T1 | 4.7 |  |  | SFQ |  |
| NCP304HSQ09T1 | 0.9 |  | Active High | SNQ |  |
| NCP304HSQ18T1 | 1.8 |  |  | SNZ |  |
| NCP304HSQ20T1 | 2.0 |  |  | SOB |  |
| NCP304HSQ27T1 | 2.7 |  |  | SOI |  |
| NCP304HSQ29T1 | 2.9 |  |  | SOK |  |
| NCP304HSQ30T1 | 3.0 |  |  | SOL |  |
| NCP304HSQ45T1 | 4.5 |  |  | SPA |  |
| NCP304HSQ47T1 | 4.7 |  |  | SPC |  |
| NCP305LSQ09T1 | 0.9 | Open <br> Drain | Active Low | SIZ | 3000 Units on 7 inch Reel |
| NCP305LSQ16T1 | 1.6 |  |  | SIR |  |
| NCP305LSQ18T1 | 1.8 |  |  | SIP |  |
| NCP305LSQ20T1 | 2.0 |  |  | SIN |  |
| NCP305LSQ22T1 | 2.2 |  |  | SIK |  |
| NCP305LSQ23T1 | 2.3 |  |  | SIJ |  |
| NCP305LSQ24T1 | 2.4 |  |  | SII |  |
| NCP305LSQ25T1 | 2.5 |  |  | SIH |  |
| NCP305LSQ27T1 | 2.7 |  |  | SIF |  |
| NCP305LSQ28T1 | 2.8 |  |  | SIE |  |
| NCP305LSQ29T1 | 2.9 |  |  | SID |  |
| NCP305LSQ30T1 | 3.0 |  |  | SIC |  |
| NCP305LSQ32T1 | 3.2 |  |  | SIA |  |
| NCP305LSQ33T1 | 3.3 |  |  | SHZ |  |
| NCP305LSQ40T1 | 4.0 |  |  | SHR |  |
| NCP305LSQ45T1 | 4.5 |  |  | SHL |  |
| NCP305LSQ47T1 | 4.7 |  |  | SHJ |  |
| NCP305LSQ49T1 | 4.9 |  |  | SHH |  |

NOTE: The ordering information lists seven standard under voltage thresholds with active low outputs. Additional active low threshold devices, ranging from 0.9 V to 4.9 V in 100 mV increments and NCP304 active high output devices, ranging from 0.9 V to 4.9 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability. The electrical characteristics of these additional devices are shown in Tables 1 and 2.

## Undervoltage Sensing Circuit

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA , and operation is guaranteed down to 1.0 V input with low standby current. These devices are packaged in 3-pin TO-226AA, 8-pin SO-8 and Micro-8 surface mount packages.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

- Trimmed-In-Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at $25^{\circ} \mathrm{C}$
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 V Input
- Low Standby Current
- Economical TO-226AA, SO-8 and Micro-8 Surface Mount Packages

Representative Block Diagram


Pin numbers adjacent to terminals are for the 3-pin TO-226AA package. Pin numbers in parenthesis are for the 8 -lead packages.

MC34064 MC33064

## UNDERVOLTAGE SENSING CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE CASE 29 (TO-226AA)


Pin 1. $\overline{\text { Reset }}$
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE CASE 751
(SO-8)


DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro-8)


ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
| :---: | :---: | :---: |
| MC34064D-5 | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | SO-8 |
| MC34064DM-5 |  | Micro-8 |
| MC34064P-5 |  | TO-226AA |
| MC33064D-5 | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-8 |
| MC33064DM-5 |  | Micro-8 |
| MC33064P-5 |  | TO-226AA |

This device contains 21 active transistors.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Input Supply Voltage | $V_{\text {in }}$ | -1.0 to 10 | V |
| Reset Output Voltage | $\mathrm{V}_{\mathrm{O}}$ | 10 | V |
| Reset Output Sink Current (Note 1) | $I_{\text {Sink }}$ | Internally Limited | mA |
| Clamp Diode Forward Current, Pin 1 to 2 (Note 1) | $\mathrm{I}_{\mathrm{F}}$ | 100 | mA |
| Power Dissipation and Thermal Characteristics <br> P Suffix, Plastic Package <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> D Suffix, Plastic Package Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air <br> DM Suffix, Plastic Package Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> PD <br> $\mathrm{R}_{\text {日JA }}$ | $\begin{aligned} & 625 \\ & 200 \\ & 625 \\ & 200 \\ & 520 \\ & 240 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature <br> MC34064 <br> MC33064 | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| COMPARATOR |  |  |  |  |  |
| Threshold Voltage |  |  |  |  |  |
| High State Output (Vin Increasing) | $\mathrm{V}_{\text {IH }}$ | 4.5 | 4.61 | 4.7 | V |
| Low State Output (Vin Decreasing) | $\mathrm{V}_{\mathrm{H}}$ | 4.5 | 4.59 | 4.7 |  |
| Hysteresis | 0.01 | 0.02 | 0.05 |  |  |

## RESET OUTPUT

| Output Sink Saturation | $\mathrm{V}_{\mathrm{OL}}$ |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\left(\mathrm{V}_{\text {in }}=4.0 \mathrm{~V}, \mathrm{I}_{\text {ink }}=8.0 \mathrm{~mA}\right)$ |  | - | 0.46 | 1.0 |  |
| $\left(\mathrm{~V}_{\text {in }}=4.0 \mathrm{~V}, \mathrm{I}_{\text {ink }}=2.0 \mathrm{~mA}\right)$ | - | 0.15 | 0.4 |  |  |
| $\left(\mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}\right.$, $\left.\mathrm{I}_{\text {Sink }}=0.1 \mathrm{~mA}\right)$ |  | - | - | 0.1 |  |
| Output Sink Current $\left(\mathrm{V}_{\text {in }}\right.$, Reset $\left.=4.0 \mathrm{~V}\right)$ |  | $\mathrm{I}_{\text {Sink }}$ | 10 | 27 | 60 |
| Output Off-State Leakage $\left(\mathrm{V}_{\text {in }}\right.$, Reset $\left.=5.0 \mathrm{~V}\right)$ | $\mathrm{I})$ | - | 0.02 | 0.5 | $\mu \mathrm{~A}$ |
| Clamp Diode Forward Voltage, Pin 1 to $2\left(\mathrm{I}_{\mathrm{F}}=10 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{F}}$ | 0.6 | 0.9 | 1.2 | V |

## TOTAL DEVICE

| Operating Input Voltage Range | $\mathrm{V}_{\text {in }}$ | 1.0 to 6.5 | - | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Quiescent Input Current $\left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {in }}$ | - | 390 | 500 | $\mu \mathrm{~A}$ |

NOTES: 1. Maximum package power dissipation limits must be observed.

[^39]

Figure 1. Reset Output Voltage versus Input Voltage


Figure 3. Comparator Threshold Voltage versus Temperature


Figure 5. Reset Output Saturation versus Sink Current


Figure 2. Reset Output Voltage versus Input Voltage


Figure 4. Input Current versus Input Voltage


Figure 6. Reset Delay Time


Figure 7. Clamp Diode Forward Current versus Voltage


Figure 8. Low Voltage Microprocessor Reset


Figure 9. Low Voltage Microprocessor Reset with Additional Hysteresis


Figure 10. Voltage Monitor


Figure 11. Solar Powered Battery Charger


Figure 12. Low Power Switching Regulator


Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 V threshold of the MC 34064 , its output grounds the gate of the $\mathrm{L}^{2}$ MOSFET.

Figure 13. MOSFET Low Voltage Gate Drive Protection

## MC34164, MC33164

## Micropower Undervoltage Sensing Circuits

The MC34164 series are undervoltage sensing circuits specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is required. These devices offer the designer an economical solution for low voltage detection with a single external resistor. The MC34164 series features a bandgap reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 6.0 mA , and guaranteed operation down to 1.0 V input with extremely low standby current. These devices are packaged in 3-pin TO-226AA, 8-pin SO-8 and Micro8 ${ }^{\text {TM }}$ surface mount packages.

Applications include direct monitoring of the 3.0 or 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

- Temperature Compensated Reference
- Monitors 3.0 V (MC34164-3) or 5.0 V (MC34164-5) Power Supplies
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 6.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation With 1.0 V Input
- Extremely Low Standby Current: As Low as $9.0 \mu \mathrm{~A}$
- Economical TO-226AA, SO-8 and Micro8 Surface Mount Packages


Pin numbers adjacent to terminals are for the 3-pin TO-226AA package. Pin numbers in parenthesis are for the 8 -lead packages.

This device contains 28 active transistors.
Figure 1. Representative Block Diagram

## ON Semiconductor

http://onsemi.com


## PIN CONNECTIONS



ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 2771 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2771 of this data sheet.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Input Supply Voltage | $V_{\text {in }}$ | －1．0 to 12 | V |
| Reset Output Voltage | $\mathrm{V}_{0}$ | －1．0 to 12 | V |
| Reset Output Sink Current | $I_{\text {Sink }}$ | Internally Limited | mA |
| Clamp Diode Forward Current，Pin 1 to 2 （Note 1） | $\mathrm{I}_{\mathrm{F}}$ | 100 | mA |
| Power Dissipation and Thermal Characteristics P Suffix，Plastic Package Maximum Power Dissipation＠ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance，Junction－to－Air <br> D Suffix，Plastic Package Maximum Power Dissipation＠ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance，Junction－to－Air DM Suffix，Plastic Package Maximum Power Dissipation＠ $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ Thermal Resistance，Junction－to－Air | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $P_{D}$ <br> $R_{\text {日JA }}$ | $\begin{aligned} & 700 \\ & 178 \\ & 700 \\ & 178 \\ & 520 \\ & 240 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | ＋150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range MC34164 Series MC33164 Series | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+125 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE：ESD data available upon request．

## MC34164－3，MC33164－3 SERIES

ELECTRICAL CHARACTERISTICS（For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ，for min／max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies［Notes 2 \＆3］，unless otherwise noted．）

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMPARATOR |  |  |  |  |  |
| Threshold Voltage High State Output（ $\mathrm{V}_{\text {in }}$ Increasing） Low State Output（Vin Decreasing） Hysteresis（ $\mathrm{I}_{\text {Sink }}=100 \mu \mathrm{~A}$ ） | $\begin{aligned} & V_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \\ & \mathrm{~V}_{\mathrm{H}} \end{aligned}$ | $\begin{aligned} & 2.55 \\ & 2.55 \\ & 0.03 \end{aligned}$ | $\begin{aligned} & 2.71 \\ & 2.65 \\ & 0.06 \end{aligned}$ | $\begin{aligned} & 2.80 \\ & 2.80 \end{aligned}$ | V |

## RESET OUTPUT

| Output Sink Saturation $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=2.4 \mathrm{~V}, I_{\text {Sink }}=1.0 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\mathrm{in}}=1.0 \mathrm{~V}, I_{\text {Sink }}=0.25 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | － | $\begin{gathered} 0.14 \\ 0.1 \end{gathered}$ | $\begin{aligned} & 0.4 \\ & 0.3 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Sink Current（ $\mathrm{V}_{\text {in }}$ ，Reset $=2.4 \mathrm{~V}$ ） | $I_{\text {Sink }}$ | 6.0 | 12 | 30 | mA |
| $\begin{aligned} & \text { Output Off-State Leakage } \\ & \left(\mathrm{V}_{\text {in }}, \text { Reset }=3.0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}, \text { Reset }=10 \mathrm{~V}\right) \end{aligned}$ | ${ }^{1} \mathrm{R}$（leak） | － | $\begin{aligned} & 0.02 \\ & 0.02 \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 1.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Clamp Diode Forward Voltage，Pin 1 to 2 （ $\mathrm{I}_{\mathrm{F}}=5.0 \mathrm{~mA}$ ） | $\mathrm{V}_{\mathrm{F}}$ | 6.0 | 0.9 | 1.2 | V |

TOTAL DEVICE

| Operating Input Voltage Range | $\mathrm{V}_{\text {in }}$ | 1.0 to 10 | - | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Quiescent Input Current | $\mathrm{I}_{\text {in }}$ |  |  |  | $\mu \mathrm{A}$ |
| $V_{\text {in }}=3.0 \mathrm{~V}$ |  | - | 9.0 | 15 |  |
| $\mathrm{~V}_{\text {in }}=6.0 \mathrm{~V}$ |  | - | 24 | 40 |  |

1．Maximum package power dissipation limits must be observed．
2．Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible．
3． $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34164 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34164

## MC34164, MC33164

MC34164-5, MC33164-5 SERIES
ELECTRICAL CHARACTERISTICS (For typical values $T_{A}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Notes 5 \& 6], unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| COMPARATOR |  |  |  |  |  |
| Threshold Voltage |  |  |  |  | V |
| High State Output (Vin ${ }_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{IH}}$ | 4.15 | 4.33 | 4.45 |  |
| Low State Output ( $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {IL }}$ | 4.15 | 4.27 | 4.45 |  |
| Hysteresis ( ISink $=100 \mu \mathrm{~A}$ ) | $\mathrm{V}_{\mathrm{H}}$ | 0.02 | 0.09 | - |  |

## RESET OUTPUT

| Output Sink Saturation $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=4.0 \mathrm{~V}, I_{\text {Sink }}=1.0 \mathrm{~mA}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.0 \mathrm{~V}, I_{\text {Sink }}=0.25 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | $\begin{gathered} 0.14 \\ 0.1 \end{gathered}$ | $\begin{aligned} & 0.4 \\ & 0.3 \end{aligned}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Sink Current ( $\left.\mathrm{V}_{\text {in }}, \overline{\text { Reset }}=4.0 \mathrm{~V}\right)$ | $I_{\text {Sink }}$ | 7.0 | 20 | 50 | mA |
| $\begin{aligned} & \text { Output Off-State Leakage } \\ & \left(\mathrm{V}_{\text {in }}, \text { Reset }=5.0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}, \text { Reset }=10 \mathrm{~V}\right) \end{aligned}$ | ${ }^{1} \mathrm{R}$ (leak) | - | $\begin{aligned} & 0.02 \\ & 0.02 \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 2.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Clamp Diode Forward Voltage, Pin 1 to $2\left(\mathrm{I}_{\mathrm{F}}=5.0 \mathrm{~mA}\right)$ | $V_{F}$ | 0.6 | 0.9 | 1.2 | V |

TOTAL DEVICE

| Operating Input Voltage Range | $\mathrm{V}_{\text {in }}$ | 1.0 to 10 | - | - | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Quiescent Input Current | $\mathrm{I}_{\text {in }}$ |  |  |  | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}$ |  | - | 12 | 20 |  |
| $\mathrm{~V}_{\text {in }}=10 \mathrm{~V}$ |  | - | 32 | 50 |  |

4. Maximum package power dissipation limits must be observed.
5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34164

$$
\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C} \text { for MC34164 }
$$

$=-40^{\circ} \mathrm{C}$ for MC33164
$=+125^{\circ} \mathrm{C}$ for MC33164


Figure 1. MC3X164-3 Reset Output Voltage versus Input Voltage


Figure 2. MC3X164-5 Reset Output Voltage versus Input Voltage


Figure 3. MC3X164-3 Reset Output Voltage versus Input Voltage


Figure 5. MC3X164-3 Comparator Threshold Voltage versus Temperature


Figure 7. MC3X164-3 Input Current versus Input Voltage


Figure 4. MC3X164-5 Reset Output
Voltage versus Input Voltage


Figure 6. MC3X164-5 Comparator Threshold Voltage versus Temperature


Figure 8. MC3X164-5 Input Current versus Input Voltage


Figure 9. MC3X164-3 Reset Output
Saturation versus Sink Current


Figure 11. Clamp Diode Forward Current versus Voltage


Figure 10. MC3X164-5 Reset Output
Saturation versus Sink Current


Figure 12. Reset Delay Time (MC3X164-5 Shown)


A time delayed reset can be accomplished with the addition of $C_{D L Y}$. For systems with extremely fast power supply rise times (<500 ns) it is recommended that the RCDLY time constant be greater than $5.0 \mu \mathrm{~s}$. $\mathrm{V}_{\text {th }}(\mathrm{MPU})$ is the microprocessor reset input threshold.

Figure 13. Low Voltage Microprocessor Reset

## MC34164, MC33164



Comparator hysteresis can be increased with the addition of resistor $\mathrm{R}_{H}$. The hysteresis equation has been simplified and does not account for the change of input current $\mathrm{I}_{\text {in }}$ as $\mathrm{V}_{\text {in }}$ crosses the comparator threshold (Figure 8). An increase of the lower threshold $\Delta \mathrm{V}_{\text {th(lower) }}$ will be observed due to $\mathrm{I}_{\text {in }}$ which is typically $10 \mu \mathrm{~A}$ at 4.3 V . The equations are accurate to $\pm 10 \%$ with $\mathrm{R}_{\mathrm{H}}$ less than $1.0 \mathrm{k} \Omega$ and $\mathrm{R}_{\mathrm{L}}$ between $4.3 \mathrm{k} \Omega$ and $43 \mathrm{k} \Omega$.

Figure 14. Low Voltage Microprocessor Reset With Additional Hysteresis (MC3X164-5 Shown)


Figure 15. Voltage Monitor


Figure 16. Solar Powered Battery Charger


Figure 17. MOSFET Low Voltage Gate Drive Protection Using the MC3X164-5

## MC34164，MC33164

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33164D－3 | SO－8 | 98 Units／Rail |
| MC33164D－3R2 | SO－8 | 2500 Units／Tape \＆Reel |
| MC33164DM－3R2 | Micro8 | 4000 Units／Tape \＆Reel |
| MC33164P－3 | TO－92 | 2000 Units／Box |
| MC33164P－3RA | TO－92 | 2000 Units／Tape \＆Reel |
| MC33164P－3RP | TO－92 | 2000 Units／Pack |
| MC33164D－5 | SO－8 | 98 Units／Rail |
| MC33164D－5R2 | SO－8 | 2500 Units／Tape \＆Reel |
| MC33164DM－5R2 | Micro8 | 4000 Units／Tape \＆Reel |
| MC33164P－5 | TO－92 | 2000 Units／Box |
| MC33164P－5RA | TO－92 | 2000 Units／Tape \＆Reel |
| MC33164P－5RP | TO－92 | 2000 Units／Pack |
| MC34164D－3 | SO－8 | 98 Units／Rail |
| MC34164D－3R2 | SO－8 | 2500 Units／Tape \＆Reel |
| MC34164DM－3R2 | Micro8 | 4000 Units／Tape \＆Reel |
| MC334164P－3 | TO－92 | 2000 Units／Box |
| MC34164P－3RP | TO－92 | 2000 Units／Pack |
| MC34164D－5 | SO－8 | 98 Units／Rail |
| MC34164D－5R2 | SO－8 | 2500 Units／Tape \＆Reel |
| MC34164DM－5R2 | Micro8 | 4000 Units／Tape \＆Reel |
| MC334164P－5 | TO－92 | 2000 Units／Box |
| MC34164P－5RA | TO－92 | 2000 Units／Tape \＆Reel |
| MC34164P－5RP | TO－92 | 2000 Units／Pack |
|  |  |  |

## MARKING DIAGRAMS

| SO－8 <br> D SUFFIX | Micro8 <br> CASE 751 |
| :---: | :---: |
| MC3S164DM |  |
| CASE 846A |  |


| Micro8 |
| :---: |
| C34164DM |
| ASE 846A |
| 8 \％月团 |
| M1y0 |
| Yww |
| A |
|  |
| 目日月 |


$x \quad=$ Device Number 3 or 4
$y \quad=$ Suffix Number 3 or 5
A＝Assembly Location
WL，L＝Wafer Lot
YY，Y＝Year
WW，W＝Work Week

## Very Low Supply Current 3-Pin Microprocessor Reset Monitor

The NCP803 is a cost-effective system supervisor circuit designed to monitor $\mathrm{V}_{\mathrm{CC}}$ in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within $10 \mu \mathrm{sec}$ of $\mathrm{V}_{\mathrm{CC}}$ falling through the reset voltage threshold. Reset is maintained active for a minimum of 140 msec after $\mathrm{V}_{\mathrm{CC}}$ rises above the reset threshold. The NCP803 has an open drain active-low RESET output. The output of the NCP803 is guaranteed valid down to $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}$ and is available in a SOT-23 package.

The NCP803 is optimized to reject fast transient glitches on the $\mathrm{V}_{\mathrm{CC}}$ line. Low supply current of $1.0 \mu \mathrm{~A}\left(\mathrm{~V}_{\mathrm{CC}}=3.2 \mathrm{~V}\right)$ make this device suitable for battery powered applications.

## Features

- Precision $\mathrm{V}_{\mathrm{CC}}$ Monitor for $2.5 \mathrm{~V}, 3.0 \mathrm{~V}, 3.3 \mathrm{~V}$, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.6 V to 4.9 V Available in 100 mV Steps
- 140 msec Guaranteed Minimum $\overline{\text { RESET Output Duration }}$
- $\overline{\text { RESET }}$ Output Guaranteed to $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}$
- Low $1.0 \mu \mathrm{~A}$ Supply Current
- $\mathrm{V}_{\mathrm{CC}}$ Transient Immunity
- Small SOT-23 Package
- No External Components
- Wide Operating Temperature: $-40^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$


## Typical Applications

- Computers
- Embedded Systems
- Battery Powered Equipment
- Critical $\mu$ P Power Supply Monitoring


Figure 1. Typical Application Diagram


NOTE: *SOT-23 is equivalent to JEDEC (TO-236)

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCP803SNxxxT1 | SOT-23 | $3000 /$ Tape \& Reel |

NOTE: The "xxx" denotes a suffix for $\mathrm{V}_{\mathrm{cc}}$ voltage threshold options - see page 2777 for more details.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2777 of this data sheet.

NCP803

ABSOLUTE MAXIMUM RATINGS* (Note 1)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ to GND ) | $\mathrm{V}_{\mathrm{CC}}$ | 6.0 | V |
| RESET |  | -0.3 to $\left(\mathrm{V}_{\mathrm{CC}}+0.3\right)$ | V |
| Input Current, $\mathrm{V}_{\mathrm{CC}}$ |  | 20 | mA |
| Output Current, RESET |  | 20 | mA |
| dV/dt ( $\mathrm{V}_{\mathrm{CC}}$ ) |  | 100 | $\mathrm{~V} / \mathrm{sec}$ |
| Thermal Resistance, Junction to Air |  | 491 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature Range | $\mathrm{R}_{\text {日JA }}$ | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 Seconds) | $\mathrm{T}_{\text {stg }}$ | +260 | ${ }^{\circ} \mathrm{C}$ |
| Latch-up performance: | $\mathrm{T}_{\text {sol }}$ | mA |  |

*Maximum Ratings are those values beyond which damage to the device may occur.

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 4000 V per MIL-STD-883, Method 3015.
Machine Model Method 400 V .
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}} \quad \text { with } T_{J(\max )}=150^{\circ} \mathrm{C}
$$

ELECTRICAL CHARACTERISTICS $T_{A}=-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. (Note 3)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ Range $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.2 \end{aligned}$ |  | $\begin{aligned} & 5.5 \\ & 5.5 \end{aligned}$ | V |
| Supply Current $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =3.3 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =85^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \\ \mathrm{~V}_{\mathrm{CC}} & =5.5 \mathrm{~V} \\ \mathrm{~T}_{\mathrm{A}} & =-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}} & =85^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \end{aligned}$ | ${ }^{\text {c }}$ C |  | $\begin{gathered} 0.5 \\ - \\ 0.8 \end{gathered}$ | $\begin{aligned} & 1.2 \\ & 2.0 \\ & \\ & 1.8 \\ & 2.5 \end{aligned}$ | $\mu \mathrm{A}$ |
| Reset Threshold (Note 4) <br> NCP803SN490 $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \end{aligned}$ <br> NCP803SN463 $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}$ $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C}$ <br> NCP803SN438 $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \end{aligned}$ <br> NCP803SN308 $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \text { to }+105^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {TH }}$ | $\begin{aligned} & 4.83 \\ & 4.78 \\ & 4.66 \\ & \\ & 4.56 \\ & 4.50 \\ & 4.40 \\ & \\ & 4.31 \\ & 4.25 \\ & 4.16 \\ & \\ & 3.04 \\ & 3.00 \\ & 2.92 \end{aligned}$ | 4.9 <br> - <br> 4.63 <br> - <br> 4.38 <br> - <br> 3.08 | $\begin{aligned} & 4.97 \\ & 5.02 \\ & 5.14 \\ & \\ & 4.70 \\ & 4.75 \\ & 4.86 \\ & \\ & 4.45 \\ & 4.50 \\ & 4.56 \\ & \\ & 3.11 \\ & 3.15 \\ & 3.23 \end{aligned}$ | V |

3. Production testing done at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, over temperature limits guaranteed by design.
4. Contact your ON Semiconductor sales representative for other threshold voltage options.

ELECTRICAL CHARACTERISTICS (continued) $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
(Note 5)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Reset Threshold (continued) | $\mathrm{V}_{\text {TH }}$ |  |  |  | V |
| NCP803SN293 |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 2.89 | 2.93 | 2.96 |  |
| $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | 2.85 | - | 3.00 |  |
| $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |  | 2.78 | - | 3.08 |  |
| NCP803SN263 |  |  |  |  |  |
| $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 2.59 | 2.63 | 2.66 |  |
| $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | 2.55 | - | 2.70 |  |
| $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |  | 2.50 | - | 2.76 |  |
| NCP803SN232 |  |  |  |  |  |
| $\mathrm{T}_{\text {A }}=+25^{\circ} \mathrm{C}$ |  | 2.28 | 2.32 | 2.35 |  |
| $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | 2.25 | - | 2.38 |  |
| $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |  | 2.21 | - | 2.45 |  |
| NCP803SN160 |  |  |  |  |  |
| $\mathrm{T}_{\text {A }}=+25^{\circ} \mathrm{C}$ |  | 1.58 | 1.6 | 1.62 |  |
| $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | 1.56 | - | 1.64 |  |
| $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |  | 1.52 | - | 1.68 |  |
| Reset Temperature Coefficient |  | - | 30 | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{CC}}$ to Reset Delay $\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {TH }}$ to $\left(\mathrm{V}_{\mathrm{TH}}-100 \mathrm{mV}\right)$ |  | - | 10 | - | $\mu \mathrm{sec}$ |
| Reset Active Timeout Period |  | 140 | 240 | 460 | msec |
| RESET Output Voltage Low | $\mathrm{V}_{\mathrm{OL}}$ | - | - | 0.3 | V |
| $\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {TH }}-0.2 \mathrm{~V}$ |  |  |  |  |  |
| $1.6 \mathrm{~V} \leq \mathrm{V}_{\text {TH }} \leq 2.0 \mathrm{~V}, \mathrm{I}_{\text {SINK }}=0.5 \mathrm{~mA}$ |  |  |  |  |  |
| $2.1 \mathrm{~V} \leq \mathrm{V}_{\text {TH }} \leq 4.0 \mathrm{~V}, \mathrm{I}_{\mathrm{SINK}}=1.2 \mathrm{~mA}$ |  |  |  |  |  |
| $4.1 \mathrm{~V} \leq \mathrm{V}_{\text {TH }} \leq 4.9 \mathrm{~V}$, $\mathrm{I}_{\text {SINK }}=3.2 \mathrm{~mA}$ |  |  |  |  |  |
| RESET Leakage Current <br> $\mathrm{V}_{\mathrm{CC}}>\mathrm{V}_{\mathrm{TH}}$, RESET De-asserted | ILEAK | - | - | 1 | $\mu \mathrm{A}$ |

5. Production testing done at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, over temperature limits guaranteed by design.

## PIN DESCRIPTION

| Pin No. | Symbol | Description |
| :---: | :---: | :--- |
| 1 | GND | Ground |
| 2 | RESET | RESET output remains low while $V_{C C}$ is below the reset voltage threshold, and for 240 msec (typ.) <br> after $V_{C C}$ rises above reset threshold. |
| 3 | $\mathrm{~V}_{\mathrm{CC}}$ | Supply Voltage: $\mathrm{C}=100 \mathrm{nF}$ is recommended as a bypass capacitor between $\mathrm{V}_{\mathrm{CC}}$ and GND. |

## APPLICATIONS INFORMATION

## $\mathrm{V}_{\mathrm{Cc}}$ Transient Rejection

The NCP803 provides accurate $\mathrm{V}_{\mathrm{CC}}$ monitoring and reset timing during power-up, power-down, and brownout/sag conditions, and rejects negative-going transients (glitches) on the power supply line. Figure 2 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies under the curve will not generate a reset signal. Combinations above the curve are detected as a brownout or power-down. Typically, transient that goes 100 mV below the reset threshold and lasts $5 \mu \mathrm{~s}$ or less will not cause a reset pulse. Transient immunity can be improved by adding a capacitor in close proximity to the $\mathrm{V}_{\mathrm{CC}}$ pin.


Figure 2. Maximum Transient Duration vs. Overdrive for Glitch Rejection at $25^{\circ} \mathrm{C}$

## Processors With Bidirectional I/O Pins

Some $\mu$ P's (such as Motorola 68HC11) have bi-directional reset pins which interface easily with the Open Drain RESET output of the NCP803. As shown in Figure 3, one can connect directly to the RESET output of the NCP803 to the $\overline{\text { RESET }}$ pin of the $\mu \mathrm{P}$. The pull-up resistor avoids an undetermined voltage of the $\overline{\text { RESET }}$ pin.


Figure 3. Interfacing to Bidirectional Reset I/O

## NCP803 RESET Output Allows Use With Two Power Supplies

In numerous applications the pull-up resistor placed on the $\overline{\mathrm{RESET}}$ output is connected to the supply voltage monitored by the IC. Nevertheless, a different supply voltage can also power this output and so level-shift from the monitored supply to reset the $\mu$ P. However, if the NCP803's supply goes below 1 V , the $\overline{\text { RESET }}$ output ability to sink current will decrease and the result is a high state on the pin even though the supply's IC is under the threshold level. This occurs at a $\mathrm{V}_{\mathrm{CC}}$ level that depends on the $\mathrm{R}_{\text {pull-up }}$ value and the voltage to which it is connected.


Figure 4. RESET Output with Two Power Supplies

NCP803
TYPICAL CHARACTERISTICS


Figure 5. Supply Current vs. Supply Voltage


Figure 7. Supply Current vs. Supply Voltage


Figure 9. Power-up Reset Timeout vs. Temperature


Figure 6. Supply Current vs. Supply Voltage


Figure 8. Normalized Reset Threshold Voltage vs. Temperature


Figure 10. Power-down Reset Timeout vs. Temperature (Overdrive = 20 mV )

NCP803

## TAPING FORM

Component Taping Orientation for 3L SOT-23 (JEDEC-236) Devices


Tape \& Reel Specifications Table

| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
| :---: | :---: | :---: | :---: | :---: |
| SOT-23 | 8 mm | 4 mm | 3000 | 7 inches |

MARKING AND THRESHOLD INFORMATION

| ON Semiconductor Part \# | $\mathbf{V}_{\text {TH }}{ }^{*}$ | Marking (Note 6) |
| :--- | :--- | :---: |
| NCP803SN263T1 | 2.63 | SQCM |
| NCP803SN308T1 | 3.08 | SQEM |

*Contact your ON Semiconductor sales representative for other threshold voltage options.
6. $M=$ Monthly Date Code

## MAX809 Series, MAX810 Series

## Very Low Supply Current 3-Pin Microprocessor Reset Monitors

The MAX809 and MAX810 are cost-effective system supervisor circuits designed to monitor $\mathrm{V}_{\mathrm{CC}}$ in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within $10 \mu \mathrm{sec}$ of $\mathrm{V}_{\mathrm{CC}}$ falling through the reset voltage threshold. Reset is maintained active for a minimum of 140 msec after $\mathrm{V}_{\mathrm{CC}}$ rises above the reset threshold. The MAX810 has an active-high RESET output while the MAX809 has an active-low $\overline{\text { RESET }}$ output. The output of the MAX809 is guaranteed valid down to $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}$. Both devices are available in a SOT-23 package.

The MAX809/810 are optimized to reject fast transient glitches on the $\mathrm{V}_{\mathrm{CC}}$ line. Low supply current of $1.0 \mu \mathrm{~A}\left(\mathrm{~V}_{\mathrm{CC}}=3.2 \mathrm{~V}\right)$ makes these devices suitable for battery powered applications.

## Features

- Precision $\mathrm{V}_{\mathrm{CC}}$ Monitor for $2.5 \mathrm{~V}, 3.0 \mathrm{~V}, 3.3 \mathrm{~V}$, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.6 V to 4.9 V Available in 100 mV Steps
- 140 msec Guaranteed Minimum $\overline{\text { RESET Output Duration }}$
- $\overline{\text { RESET }}$ Output Guaranteed to $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}$
- Low Supply Current
- $\mathrm{V}_{\mathrm{CC}}$ Transient Immunity
- Small SOT-23 Package
- No External Components
- Wide Operating Temperature: $-40^{\circ} \mathrm{C}$ to $105^{\circ} \mathrm{C}$


## Typical Applications

- Computers
- Embedded Systems
- Battery Powered Equipment
- Critical $\mu$ P Power Supply Monitoring


Figure 1. Typical Application Diagram

## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


PIN CONFIGURATION


NOTE: *SOT-23 is equivalent to JEDEC (TO-236)
** RESET is for MAX809
*** RESET is for MAX810
ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MAX809xTR | SOT-23 | 3000 Tape/Reel |
| MAX809SNxxxT1 | SOT-23 | 3000 Tape/Reel |
| MAX810xTR | SOT-23 | 3000 Tape/Reel |

NOTE: The " $x$ " and " $x x x$ " denotes a suffix for $V_{c c}$ voltage threshold options - see page 2785 for more details.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2785 of this data sheet.

## MAX809 Series, MAX810 Series

PIN DESCRIPTION

| Pin No. | Symbol | Description |
| :---: | :---: | :--- |
| 1 | GND | Ground |
| 2 | RESET (MAX809) | RESET output remains low while $\mathrm{V}_{\mathrm{CC}}$ is below the reset voltage threshold, and for 240 msec (typ.) <br> after $\mathrm{V}_{\mathrm{CC}}$ rises above reset threshold |
| 2 | RESET (MAX810) | RESET output remains high while $\mathrm{V}_{\mathrm{CC}}$ is below the reset voltage threshold, and for 240 msec <br> (typ.) after $\mathrm{V}_{\mathrm{CC}}$ rises above reset threshold |
| 3 | $\mathrm{~V}_{\mathrm{CC}}$ | Supply Voltage (typ.) |

ABSOLUTE MAXIMUM RATINGS* (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage (V $\mathrm{V}_{\text {CC }}$ to GND) | $\mathrm{V}_{\mathrm{CC}}$ | 6.0 | V |
| RESET |  | -0.3 to ( $\left.\mathrm{V}_{\mathrm{CC}}+0.3\right)$ | V |
| Input Current, $\mathrm{V}_{\text {CC }}$ |  | 20 | mA |
| Output Current, RESET |  | 20 | mA |
| dV/dt ( $\mathrm{V}_{\mathrm{Cc}}$ ) |  | 100 | $\mathrm{V} / \mathrm{\mu sec}$ |
| Thermal Resistance, Junction to Air | $\mathrm{R}_{\theta \mathrm{JA}}$ | 491 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature Range <br> (Data given for MAX809 threshold levels: $1.60 \mathrm{~V}, 2.32 \mathrm{~V}, 2.93 \mathrm{~V}$, <br> 4.63 V and 4.90 V ) | $\mathrm{T}_{\mathrm{A}}$ | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |
| Operating Temperature Range <br> (Data given for MAX809 threshold levels: $2.63 \mathrm{~V}, 3.08 \mathrm{~V}, 4.00 \mathrm{~V}$ and 4.38 V ; MAX810 threshold levels: $2.63 \mathrm{~V}, 2.93 \mathrm{~V}, 3.08 \mathrm{~V}$, 4.38 V and 4.63 V ) | $\mathrm{T}_{\text {A }}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature (Soldering, 10 Seconds) | $\mathrm{T}_{\text {sol }}$ | +260 | ${ }^{\circ} \mathrm{C}$ |
| $\begin{array}{ll}\text { Latch-up performance: } & \text { Positive } \\ & \text { Negative }\end{array}$ | ILatch-up | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | mA |

*Maximum Ratings are those values beyond which damage to the device may occur.

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 350 V .
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}} \quad \text { with } T_{J(\max )}=150^{\circ} \mathrm{C}
$$

ELECTRICAL CHARACTERISTICS $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. (Note 3) The following data is given for MAX809 threshold levels: $1.60 \mathrm{~V}, 2.32 \mathrm{~V}, 2.93 \mathrm{~V}, 4.63 \mathrm{~V}$ and 4.90 V .

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ Range |  |  |  |  | V |
| $\mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$ |  | 1.0 | - | 5.5 |  |
| $\mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |  | 1.2 | - | 5.5 |  |
| Supply Current | ICC |  |  |  | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | - | 0.5 | 1.2 |  |
| $\mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |  | - | - | 2.0 |  |
| $\mathrm{~V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | - | 0.8 | 1.8 |  |
| $\mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ |  | - | - | 2.5 |  |

3. Production testing done at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, over temperature limits guaranteed by design.

## MAX809 Series, MAX810 Series

ELECTRICAL CHARACTERISTICS (continued) $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+105^{\circ} \mathrm{C}$ unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$. (Note 4) The following data is given for MAX809 threshold levels: $1.60 \mathrm{~V}, 2.32 \mathrm{~V}, 2.93 \mathrm{~V}, 4.63 \mathrm{~V}$ and 4.90 V .

4. Production testing done at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, over temperature limits guaranteed by design.
5. Contact your ON Semiconductor sales representative for other threshold voltage options.

## MAX809 Series, MAX810 Series

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=$ Full Range, $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ for $\mathrm{L} / \mathrm{M} / \mathrm{J}, 3.3 \mathrm{~V}$ for $\mathrm{T} / \mathrm{S}, 3.0 \mathrm{~V}$ for R ) (Note 6) The following data is given for MAX809 threshold levels: $2.63 \mathrm{~V}, 3.08 \mathrm{~V}, 4.00 \mathrm{~V}$ and 4.38 V ; MAX810 threshold levels: $2.63 \mathrm{~V}, 2.93 \mathrm{~V}, 3.08 \mathrm{~V}, 4.38 \mathrm{~V}$ and 4.63 V .

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ Range $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=0^{\circ} \mathrm{C} \text { to }+70^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 1.2 \end{aligned}$ | - | $\begin{aligned} & 5.5 \\ & 5.5 \end{aligned}$ | V |
| Supply Current MAX8xxM/MAX809J/MAX810L: $\mathrm{V}_{\mathrm{CC}}<5.5 \mathrm{~V}$ MAX8xxR/T/MAX810S: $\mathrm{V}_{\mathrm{CC}}<3.6 \mathrm{~V}$ | Icc |  | $\begin{aligned} & 24 \\ & 17 \end{aligned}$ | $\begin{aligned} & 60 \\ & 50 \end{aligned}$ | $\mu \mathrm{A}$ |
| $\begin{array}{\|l} \text { Reset Threshold (Note 6) } \\ \text { MAX810L: } T_{A}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \text { MAX8xxM: } \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \text { MAX809J: } \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \text { MAX8xxT: } \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \text { MAX810S: } \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{A}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ \text { MAX8xxR: } \mathrm{T}_{A}=25^{\circ} \mathrm{C} \\ \mathrm{~T}_{A}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{array}$ | $\mathrm{V}_{\text {TH }}$ | $\begin{aligned} & 4.56 \\ & 4.50 \\ & 4.31 \\ & 4.25 \\ & 3.93 \\ & 3.89 \\ & 3.04 \\ & 3.00 \\ & 2.89 \\ & 2.85 \\ & 2.59 \\ & 2.55 \end{aligned}$ | $\begin{gathered} 4.63 \\ - \\ 4.38 \\ - \\ 4.00 \\ - \\ 3.08 \\ - \\ 2.93 \\ - \\ 2.63 \end{gathered}$ | $\begin{aligned} & 4.70 \\ & 4.75 \\ & 4.45 \\ & 4.50 \\ & 4.06 \\ & 4.10 \\ & 3.11 \\ & 3.15 \\ & 2.96 \\ & 3.00 \\ & 2.66 \\ & 2.70 \end{aligned}$ | V |
| Reset Threshold Temperature Coefficient |  | - | 30 | - | ppm/ $/{ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{CC}}$ to Reset Delay $\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{TH}}$ to $\left(\mathrm{V}_{\mathrm{TH}}-100 \mathrm{mV}\right)$ |  | - | 20 | - | $\mu \mathrm{sec}$ |
| Reset Active Timeout Period |  | 140 | 240 | 560 | msec |
| $\begin{aligned} & \hline \text { RESET Output Voltage Low }(\mathrm{MAX} 809) \\ & \text { MAX809R } / \mathrm{T}: \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{TH}} \mathrm{~min}, \mathrm{I}_{\mathrm{SINK}}=1.2 \mathrm{~mA} \\ & \text { MAX809M/J: } \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{TH}} \mathrm{~min}, \mathrm{I}_{\text {IINK }}=3.2 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CC}}>1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{SINK}}=50 \mu \mathrm{~A} \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | - | $\begin{aligned} & 0.3 \\ & 0.4 \\ & 0.3 \end{aligned}$ | V |
| $\begin{aligned} & \hline \text { RESET Output Voltage High (MAX809) } \\ & \text { MAX809R/T: } V_{C C}>V_{\text {TH }} \max , I_{\text {SOURCE }}=500 \mu \mathrm{~A} \\ & \text { MAX809M } / \mathrm{J}: \mathrm{V}_{\text {CC }}>\mathrm{V}_{\text {TH }} \text { max, } \text { I }_{\text {SOURCE }}=800 \mu \mathrm{~A} \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{gathered} 0.8 \mathrm{~V}_{\mathrm{CC}} \\ \mathrm{~V}_{\mathrm{CC}}-1.5 \end{gathered}$ | - | - | V |
| $\begin{aligned} & \text { RESET Output Voltage Low }(\text { MAX810 }) \\ & \text { MAX810R/S/T: } \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {TH }} \max , \mathrm{I}_{\text {SINK }}=1.2 \mathrm{~mA} \\ & \text { MAX810L/M: } \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {TH }} \max , I_{\text {SINK }}=3.2 \mathrm{~mA} \end{aligned}$ | V OL | - | - | $\begin{aligned} & 0.3 \\ & 0.4 \end{aligned}$ | V |
| $\begin{array}{\|l} \hline \text { RESET Output Voltage High (MAX810) } \\ 1.8<\mathrm{V}_{\mathrm{CC}}<\mathrm{V}_{\mathrm{TH}} \mathrm{~min}, \text { ISOURCE }=150 \mu \mathrm{~A} \end{array}$ | $\mathrm{V}_{\mathrm{OH}}$ | 0.8 VCC | - | - | V |

6. Production testing done at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, over temperature limits guaranteed by design.

## MAX809 Series, MAX810 Series

## APPLICATIONS INFORMATION

## $\mathrm{V}_{\mathrm{Cc}}$ Transient Rejection

The MAX809 provides accurate $\mathrm{V}_{\mathrm{CC}}$ monitoring and reset timing during power-up, power-down, and brownout/sag conditions, and rejects negative-going transients (glitches) on the power supply line. Figure 2 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. Any combination of duration and overdrive which lies under the curve will not generate a reset signal. Combinations above the curve are detected as a brownout or power-down. Typically, transient that goes 100 mV below the reset threshold and lasts $5 \mu \mathrm{~s}$ or less will not cause a reset pulse. Transient immunity can be improved by adding a capacitor in close proximity to the $\mathrm{V}_{\mathrm{CC}}$ pin of the MAX809.



Figure 2. Maximum Transient Duration vs. Overdrive for Glitch Rejection at $25^{\circ} \mathrm{C}$

## RESET Signal Integrity During Power-Down

The MAX809 RESET output is valid to $\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}$. Below this voltage the output becomes an "open circuit" and does not sink current. This means CMOS logic inputs to the $\mu \mathrm{P}$ will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in situations where $\overline{\mathrm{RESET}}$ must be maintained
valid to $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$, a pull-down resistor must be connected from $\overline{\text { RESET }}$ to ground to discharge stray capacitances and hold the output low (Figure 3). This resistor value, though not critical, should be chosen such that it does not appreciably load $\overline{\text { RESET }}$ under normal operation ( $100 \mathrm{k} \Omega$ will be suitable for most applications).


Figure 3. Ensuring RESET Valid to $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$

## Processors With Bidirectional I/O Pins

Some $\mu$ P's (such as Motorola 68HC11) have bi-directional reset pins. Depending on the current drive capability of the processor pin, an indeterminate logic level may result if there is a logic conflict. This can be avoided by adding a $4.7 \mathrm{k} \Omega$ resistor in series with the output of the MAX809 (Figure 4). If there are other components in the system which require a reset signal, they should be buffered so as not to load the reset line. If the other components are required to follow the reset I/O of the $\mu \mathrm{P}$, the buffer should be connected as shown with the solid line.


Figure 4. Interfacing to Bidirectional Reset I/O

## MAX809 Series, MAX810 Series

TYPICAL CHARACTERISTICS
The following data is given for MAX809 threshold levels: $1.60 \mathrm{~V}, 2.32 \mathrm{~V}, 2.93 \mathrm{~V}, 4.63 \mathrm{~V}$ and 4.90 V .


Figure 5. Supply Current vs. Supply Voltage


Figure 7. Normalized Power-Up Reset vs. Temperature


Figure 6. Supply Current vs. Supply Voltage

Figure 8. Normalized Reset Threshold Voltage
vs. Temperature

## MAX809 Series, MAX810 Series

TYPICAL CHARACTERISTICS
The following data is given for MAX809 threshold levels: $2.63 \mathrm{~V}, 3.08 \mathrm{~V}, 4.00 \mathrm{~V}$ and 4.38 V ; MAX810 threshold levels: $2.63 \mathrm{~V}, 2.93 \mathrm{~V}, 3.08 \mathrm{~V}, 4.38 \mathrm{~V}$ and 4.63 V.


Figure 9. Supply Current vs. Temperature (No Load, MAX8xxR/T, MAX810S)


Figure 11. Power-Down Reset Delay vs. Temperature and Overdrive (MAX8xxR/T, MAX810S)


Figure 13. Power-Up Reset Timeout vs. Temperature


Figure 10. Supply Current vs. Temperature (No Load, MAX8xxM/MAX809J, MAX810L)


Figure 12. Power-Down Reset Delay vs. Temperature and Overdrive (MAX8xxM/MAX809J, MAX810L)


Figure 14. Normalized Reset Threshold vs. Temperature

## MAX809 Series, MAX810 Series

## TAPING FORM

## Component Taping Orientation for 3L SOT-23 (JEDEC-236) Devices



Tape \& Reel Specifications Table

| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
| :---: | :---: | :---: | :---: | :---: |
| SOT-23 | 8 mm | 4 mm | 3000 | 7 inches |

MARKING AND THRESHOLD INFORMATION

| ON Semiconductor Part \# | $\mathrm{V}_{\text {TH }}{ }^{*}$ | Description | Marking |
| :---: | :---: | :---: | :---: |
| MAX809SN160T1 | 1.60 | Push-Pull RESET | SAAm |
| MAX809SN232T1 | 2.32 |  | SQPm |
| MAX809STR | 2.93 |  | SPTm |
| MAX809LTR | 4.63 |  | SPWm |
| MAX809SN490T1 | 4.90 |  | SBHm |
| MAX809MTR | 4.38 |  | J2yw |
| MAX809TTR | 3.08 |  | J3yw |
| MAX809RTR | 2.63 |  | J5yw |
| MAX809JTR | 4.00 |  | J6yw |
| MAX810MTR | 4.38 | Push-Pull RESET | K2yw |
| MAX810TTR | 3.08 |  | K3yw |
| MAX810RTR | 2.63 |  | K5yw |
| MAX810LTR | 4.63 |  | K1yw |
| MAX810STR | 2.93 |  | K4yw |

*Contact your ON Semiconductor sales representative for other threshold voltage options.
$\mathrm{m}=$ Date Code
y $=$ Year
w = Work Week

## NCP302, NCP303

## Voltage Detector Series with Programmable Delay

The NCP302 and NCP303 series are second generation ultra-low current voltage detectors that contain a programmable time delay generator. These devices are specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is paramount.

Each series features a highly accurate under voltage detector with hysteresis and an externally programmable time delay generator. This combination of features prevents erratic system reset operation.

The NCP302 series consists of complementary output devices that are available with either an active high or active low reset. The NCP303 series has an open drain N -channel output with an active low reset output.

## Features

- Quiescent Current of $0.5 \mu \mathrm{~A}$ Typical
- High Accuracy Under Voltage Threshold of $2.0 \%$
- Externally Programmable Time Delay Generator
- Wide Operating Voltage Range of 0.8 V to 10 V
- Complementary or Open Drain Output
- Active Low or Active High Reset


## Typical Applications

- Microprocessor Reset Controller
- Low Battery Detection
- Power Fail Indicator
- Battery Backup Detection

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


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THIN SOT-23-5 SN SUFFIX CASE 483

## PIN CONNECTIONS AND

 MARKING DIAGRAM
$x x x=302$ or 303
Y = Year
W = Work Week
(Top View)

## ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 2810 of this data sheet.

NCP302xSNxxT1 Complementary Output Configuration


NCP303LSNxxT1
Open Drain Output Configuration


* Inverter for active low devices. Buffer for active high devices. This device contains 28 active transistors.

Figure 1. Representative Block Diagrams

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Input Power Supply Voltage (Pin 2) | $\mathrm{V}_{\text {in }}$ | 12 | V |
| Delay Capacitor Pin Voltage (Pin 5) | $\mathrm{V}_{\text {CD }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ | V |
| $\begin{array}{l}\text { Output Voltage (Pin 1) } \\ \text { Complementary, NCP302 } \\ \text { N-Channel Open Drain, NCP303 }\end{array}$ | $\mathrm{V}_{\text {OUT }}$ | -0.3 to $\mathrm{V}_{\text {in }}+0.3$ |  |
| Output Current (Pin 1) (Note 2) |  | -0.3 to 12 |  |$]$|  |
| :--- |
| Thermal Resistance Junction to Air |
| Operating Junction Temperature Range |
| Storage Temperature Range |
| Latch-up Performance <br> Positive <br> Negative |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3-0.9 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 0.882 | 0.900 | 0.918 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.027 | 0.045 | 0.063 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=0.8 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=2.9 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ | - | $\begin{aligned} & 0.20 \\ & 0.45 \end{aligned}$ | $\begin{aligned} & 0.6 \\ & 1.2 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | lout | $\begin{aligned} & 0.01 \\ & 0.05 \\ & 1.0 \end{aligned}$ | $\begin{aligned} & 0.05 \\ & 0.50 \\ & 2.0 \end{aligned}$ | - | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) <br> Nch Sink Current, NCP302, NCP303 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right)$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right)$ $\left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=0.8 \mathrm{~V}\right)$ | IOUT | $\begin{aligned} & 1.05 \\ & 0.011 \\ & 0.014 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 0.04 \\ & 0.08 \end{aligned}$ |  | mA |
| $\mathrm{C}_{\mathrm{D}}$ Delay Pin Threshold Voltage (Pin 5) $\left(\mathrm{V}_{\text {in }}=0.99 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {TCD }}$ | 0.50 | 0.67 | 0.84 | V |
| Delay Capacitor Pin Sink Current (Pin 5) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.1 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.5 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{CD}}$ | $\begin{aligned} & 2.0 \\ & 10 \end{aligned}$ | $\begin{aligned} & 120 \\ & 300 \end{aligned}$ |  | $\mu \mathrm{A}$ |
| Delay Pullup Resistance (Pin 5) | $\mathrm{R}_{\mathrm{D}}$ | 0.5 | 1.0 | 2.0 | $\mathrm{M} \Omega$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3-1.8 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 1.764 | 1.80 | 1.836 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.054 | 0.090 | 0.126 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=1.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=3.8 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.23 \\ & 0.48 \end{aligned}$ | $\begin{aligned} & 0.7 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP302, NCP303 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | lout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP302 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| $\mathrm{C}_{\mathrm{D}}$ Delay Pin Threshold Voltage (Pin 5) $\left(\mathrm{V}_{\mathrm{in}}=1.98 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {TCD }}$ | 0.99 | 1.34 | 1.68 | V |
| Delay Capacitor Pin Sink Current (Pin 5) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.1 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.5 \mathrm{~V}\right) \end{aligned}$ | $I_{C D}$ | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{gathered} 120 \\ 1600 \end{gathered}$ | - | $\mu \mathrm{A}$ |
| Delay Pullup Resistance (Pin 5) | $\mathrm{R}_{\mathrm{D}}$ | 0.5 | 1.0 | 2.0 | $\mathrm{M} \Omega$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3-2.0 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 1.960 | 2.00 | 2.040 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.06 | 0.10 | 0.14 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=1.9 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=4.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.23 \\ & 0.48 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP302, NCP303 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP302 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| $\mathrm{C}_{\mathrm{D}}$ Delay Pin Threshold Voltage (Pin 5) $\left(\mathrm{V}_{\text {in }}=2.2 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {TCD }}$ | 1.10 | 1.49 | 1.87 | V |
| Delay Capacitor Pin Sink Current (Pin 5) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.1 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.5 \mathrm{~V}\right) \end{aligned}$ | $I_{C D}$ | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{gathered} 120 \\ 1600 \end{gathered}$ | - | $\mu \mathrm{A}$ |
| Delay Pullup Resistance (Pin 5) | $\mathrm{R}_{\mathrm{D}}$ | 0.5 | 1.0 | 2.0 | $\mathrm{M} \Omega$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3-2.7 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 2.646 | 2.700 | 2.754 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.081 | 0.135 | 0.189 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=2.6 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=4.7 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.26 \\ & 0.46 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP302, NCP303 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | lout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP302 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| $\mathrm{C}_{\mathrm{D}}$ Delay Pin Threshold Voltage (Pin 5) $\left(\mathrm{V}_{\text {in }}=2.97 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {TCD }}$ | 1.49 | 2.01 | 2.53 | V |
| Delay Capacitor Pin Sink Current (Pin 5) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.1 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.5 \mathrm{~V}\right) \end{aligned}$ | $I_{C D}$ | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{gathered} 120 \\ 1600 \end{gathered}$ | - | $\mu \mathrm{A}$ |
| Delay Pullup Resistance (Pin 5) | $\mathrm{R}_{\mathrm{D}}$ | 0.5 | 1.0 | 2.0 | $\mathrm{M} \Omega$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3-3.0 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 2.94 | 3.00 | 3.06 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.09 | 0.15 | 0.21 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=2.87 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=5.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.27 \\ & 0.47 \end{aligned}$ | $\begin{aligned} & 0.9 \\ & 1.3 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) <br> Nch Sink Current, NCP302, NCP303 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=4.5 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.0 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 2.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP302 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| $\mathrm{C}_{\mathrm{D}}$ Delay Pin Threshold Voltage (Pin 5) $\left(\mathrm{V}_{\text {in }}=3.3 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {TCD }}$ | 1.65 | 2.23 | 2.81 | V |
| Delay Capacitor Pin Sink Current (Pin 5) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.1 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.5 \mathrm{~V}\right) \end{aligned}$ | $I_{C D}$ | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{gathered} 120 \\ 1600 \end{gathered}$ | - | $\mu \mathrm{A}$ |
| Delay Pullup Resistance (Pin 5) | $\mathrm{R}_{\mathrm{D}}$ | 0.5 | 1.0 | 2.0 | $\mathrm{M} \Omega$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3-4.5 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 4.410 | 4.500 | 4.590 | V |
| Detector Threshold Hysteresis (Pin 2, $\mathrm{V}_{\text {in }}$ Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.135 | 0.225 | 0.315 | V |
| $\begin{aligned} & \text { Supply Current (Pin } 2) \\ & \left(\mathrm{V}_{\text {in }}=4.34 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=6.5 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.33 \\ & 0.52 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.4 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max })}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {in(min) }}$ | - | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=5.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | lout | $\begin{gathered} 0.01 \\ 1.0 \\ \\ 1.5 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 3.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP302 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| $\mathrm{C}_{\mathrm{D}}$ Delay Pin Threshold Voltage (Pin 5) $\left(\mathrm{V}_{\mathrm{in}}=4.95 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {TCD }}$ | 2.25 | 3.04 | 3.83 | V |
| Delay Capacitor Pin Sink Current (Pin 5) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.1 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.5 \mathrm{~V}\right) \end{aligned}$ | $I_{C D}$ | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{gathered} 120 \\ 1600 \end{gathered}$ | - | $\mu \mathrm{A}$ |
| Delay Pullup Resistance (Pin 5) | $\mathrm{R}_{\mathrm{D}}$ | 0.5 | 1.0 | 2.0 | $\mathrm{M} \Omega$ |

ELECTRICAL CHARACTERISTICS (For all values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| NCP302/3-4.7 |  |  |  |  |  |
| Detector Threshold (Pin 2, $\mathrm{V}_{\text {in }}$ Decreasing) | $\mathrm{V}_{\text {DET- }}$ | 4.606 | 4.70 | 4.794 | V |
| Detector Threshold Hysteresis (Pin 2, Vin Increasing) | $\mathrm{V}_{\mathrm{HYS}}$ | 0.141 | 0.235 | 0.329 | V |
| $\begin{aligned} & \text { Supply Current (Pin 2) } \\ & \left(\mathrm{V}_{\text {in }}=4.54 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=6.7 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{l}_{\text {in }}$ |  | $\begin{aligned} & 0.34 \\ & 0.53 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 1.4 \end{aligned}$ | $\mu \mathrm{A}$ |
| Maximum Operating Voltage (Pin 2) | $\mathrm{V}_{\text {in(max }}$ | - | - | 10 | V |
| Minimum Operating Voltage (Pin 2) $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to } 85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\text {in(min) }}$ |  | $\begin{aligned} & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & 0.70 \\ & 0.80 \end{aligned}$ | V |
| Reset Output Current (Pin 1, Active Low 'L’ Suffix Devices) <br> Nch Sink Current, NCP302, NCP303 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.05 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.70 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=0.50 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ <br> Pch Source Current, NCP302 $\left(\mathrm{V}_{\text {OUT }}=5.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}\right)$ | Iout | $\begin{gathered} 0.01 \\ 1.0 \\ 1.5 \end{gathered}$ | $\begin{gathered} 0.05 \\ 2.0 \\ 3.0 \end{gathered}$ |  | mA |
| Reset Output Current (Pin 1, Active High 'H' Suffix Devices) Nch Sink Current, NCP302, NCP303 $\left(\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}\right)$ <br> Pch Source Current, NCP302 $\begin{aligned} & \left(\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {OUT }}=\mathrm{GND}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}\right) \end{aligned}$ | Iout | $\begin{gathered} 6.3 \\ \\ 0.011 \\ 0.525 \end{gathered}$ | $\begin{gathered} 11 \\ \\ 0.04 \\ 0.6 \end{gathered}$ |  | mA |
| $\mathrm{C}_{\mathrm{D}}$ Delay Pin Threshold Voltage (Pin 5) $\left(\mathrm{V}_{\text {in }}=5.17 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {TCD }}$ | 2.59 | 3.49 | 4.40 | V |
| Delay Capacitor Pin Sink Current (Pin 5) $\begin{aligned} & \left(\mathrm{V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.1 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CD}}=0.5 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{I}_{\text {CD }}$ | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{gathered} 120 \\ 1600 \end{gathered}$ | - | $\mu \mathrm{A}$ |
| Delay Pullup Resistance (Pin 5) | $\mathrm{R}_{\mathrm{D}}$ | 0.5 | 1.0 | 2.0 | $\mathrm{M} \Omega$ |

## NCP302, NCP303



NCP302 and NCP303 series are measured with a 10 pF capacitive load. NCP303 has an additional 470 k pullup resistor connected from the reset output to +5.0 V . The reset output voltage waveforms are shown for the active low ' $L$ ' devices. Output time delay $t_{D 1}$ and $t_{D 2}$ are dependent upon the delay capacitance. Refer to Figures 12, 13, and 14. The upper detector threshold, $\mathrm{V}_{\mathrm{DET}}$ is the sum of the lower detector threshold, $\mathrm{V}_{\mathrm{DET}}$ plus the input hysteresis, $\mathrm{V}_{\mathrm{HYS}}$.

Figure 2. Measurement Conditions for $t_{D 1}$ and $t_{D 2}$

## NCP302, NCP303

Table 1. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP302 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current |  | Pch Source Current |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $V_{\text {in }}$ Low | $V_{\text {in }}$ High | $V_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High |  |
| Part Number | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\mathrm{HYS}}(\mathrm{V})$ |  |  | ${\underset{\text { in }}{(1)}}_{(\mu \mathrm{A})(1)}$ | ${\underset{\text { in }}{(\mu \mathrm{A})}}_{(2)}$ | ${ }_{(\mathrm{mA})^{(3)}}$ | $\begin{gathered} \text { Iout } \\ (\mathrm{mA})(4) \end{gathered}$ | $\begin{aligned} & \text { Iout } \\ & (\mathrm{mA})^{(5)} \end{aligned}$ |
|  | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ | Typ |
| NCP302LSN09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.3 | 0.5 | 0.05 | 0.5 | 2.0 |
| NCP302LSN10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  |  |  |  |  |
| NCP302LSN11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  | 1.0 |  |
| NCP302LSN12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |  |
| NCP302LSN13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |  |
| NCP302LSN14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |  |
| NCP302LSN15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  |  |  |  |
| NCP302LSN16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  | 2.0 |  |
| NCP302LSN17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |  |
| NCP302LSN18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |  |
| NCP302LSN19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |  |
| NCP302LSN20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 |  |  |  |  |  |
| NCP302LSN21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |  |
| NCP302LSN22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |  |
| NCP302LSN23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |  |
| NCP302LSN24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |  |
| NCP302LSN25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |  |
| NCP302LSN26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |  |
| NCP302LSN27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |  |
| NCP302LSN28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |  |
| NCP302LSN29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |  |
| NCP302LSN30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 |  |  |  |  |  |
| NCP302LSN31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |  |
| NCP302LSN32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |  |
| NCP302LSN33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |  |
| NCP302LSN34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |  |
| NCP302LSN35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |  |
| NCP302LSN36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |  |
| NCP302LSN37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |  |
| NCP302LSN38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |  |
| NCP302LSN39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |  |
| NCP302LSN40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 0.4 | 0.6 |  |  | 3.0 |
| NCP302LSN41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |  |
| NCP302LSN42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |  |
| NCP302LSN43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |  |
| NCP302LSN44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |  |
| NCP302LSN45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |  |
| NCP302LSN46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |  |
| NCP302LSN47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |  |
| NCP302LSN48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |  |
| NCP302LSN49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.05 \mathrm{~V}$, Active Low 'L' Suffix Devices
(4) Condition 4: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active Low 'L’ Suffix Devices
(5) Condition 5: $0.9-3.9 \mathrm{~V}, \mathrm{~V}_{\mathrm{in}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=2.4 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=8.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=5.9 \mathrm{~V}$, Active Low 'L' Suffix Devices

## NCP302, NCP303

Table 2. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP302 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current | Pch Source Current |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $\mathrm{V}_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High | $V_{\text {in }}$ Low | $V_{\text {in }}$ High |  |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\text {HYS }}(\mathrm{V})$ |  |  | $\operatorname{lin}_{(\mu \mathrm{A})(1)}$ |  | $\underset{(\mathrm{mA})^{(3)}}{\mathrm{I}_{\text {OUT }}}$ | $\underset{(\mathrm{mA})^{(4)}}{\mathrm{I}_{\text {OUT }}}$ | $\begin{aligned} & \text { Iout } \\ & (\mathrm{mA})^{(5)} \end{aligned}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ | Typ |
| NCP302HSN09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.3 | 0.5 | 2.5 | 0.04 | 0.08 |
| NCP302HSN10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  |  |  |  |  |
| NCP302HSN11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  |  | 0.18 |
| NCP302HSN12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |  |
| NCP302HSN13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |  |
| NCP302HSN14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |  |
| NCP302HSN15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  | 11 |  |  |
| NCP302HSN16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  |  | 0.6 |
| NCP302HSN17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |  |
| NCP302HSN18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |  |
| NCP302HSN19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |  |
| NCP302HSN20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 |  |  |  |  |  |
| NCP302HSN21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |  |
| NCP302HSN22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |  |
| NCP302HSN23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |  |
| NCP302HSN24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |  |
| NCP302HSN25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |  |
| NCP302HSN26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |  |
| NCP302HSN27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |  |
| NCP302HSN28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |  |
| NCP302HSN29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |  |
| NCP302HSN30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 |  |  |  |  |  |
| NCP302HSN31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |  |
| NCP302HSN32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |  |
| NCP302HSN33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |  |
| NCP302HSN34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |  |
| NCP302HSN35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |  |
| NCP302HSN36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |  |
| NCP302HSN37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |  |
| NCP302HSN38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |  |
| NCP302HSN39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |  |
| NCP302HSN40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 0.4 |  |  |  |  |
| NCP302HSN41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |  |
| NCP302HSN42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |  |
| NCP302HSN43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |  |
| NCP302HSN44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |  |
| NCP302HSN45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |  |
| NCP302HSN46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |  |
| NCP302HSN47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |  |
| NCP302HSN48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |  |
| NCP302HSN49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET }}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-1.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{in}}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$; $1.5-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=5.0 \mathrm{~V}$, $\mathrm{V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active High 'H' Suffix Devices
(4) Condition 4: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.4 \mathrm{~V}$, Active High 'H' Suffix Devices
(5) Condition 5: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.8 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND} ; 1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND} ; 1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=\mathrm{GND}$, Active High ' H ' Suffix Devices

Table 3. ELECTRICAL CHARACTERISTIC TABLE FOR 0.9-4.9 V

| NCP303 Series | Detector Threshold |  |  | Detector Threshold Hysteresis |  |  | Supply Current |  | Nch Sink Current |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $V_{\text {in }}$ Low | $V_{\text {in }}$ High | $\mathrm{V}_{\text {in }}$ Low | $\mathrm{V}_{\text {in }}$ High |
|  | $\mathrm{V}_{\text {DET- }}(\mathrm{V})$ |  |  |  |  |  | $\mathrm{V}_{\text {HYS }}(\mathrm{V})$ |  |  | ${\underset{\text { in }}{(1)}}_{(\mu \mathrm{A})}$ | ${\underset{\text { in }}{ }{ }_{(\mu \mathrm{A})(2)}}^{\text {(2) }}$ | $\mathrm{IOUT}_{(\mathrm{mA})}^{(3)}$ | $\begin{gathered} \mathrm{I}_{\mathrm{OUT}} \\ (\mathrm{~mA})^{(4)} \end{gathered}$ |
| Part Number | Min | Typ | Max | Min | Typ | Max | Typ | Typ | Typ | Typ |
| NCP303LSN09T1 | 0.882 | 0.9 | 0.918 | 0.027 | 0.045 | 0.063 | 0.3 | 0.5 | 0.05 | 0.5 |
| NCP303LSN10T1 | 0.980 | 1.0 | 1.020 | 0.030 | 0.050 | 0.070 |  |  |  |  |
| NCP303LSN11T1 | 1.078 | 1.1 | 1.122 | 0.033 | 0.055 | 0.077 |  |  |  | 1.0 |
| NCP303LSN12T1 | 1.176 | 1.2 | 1.224 | 0.036 | 0.060 | 0.084 |  |  |  |  |
| NCP303LSN13T1 | 1.274 | 1.3 | 1.326 | 0.039 | 0.065 | 0.091 |  |  |  |  |
| NCP303LSN14T1 | 1.372 | 1.4 | 1.428 | 0.042 | 0.070 | 0.098 |  |  |  |  |
| NCP303LSN15T1 | 1.470 | 1.5 | 1.530 | 0.045 | 0.075 | 0.105 |  |  |  |  |
| NCP303LSN16T1 | 1.568 | 1.6 | 1.632 | 0.048 | 0.080 | 0.112 |  |  |  | 2.0 |
| NCP303LSN17T1 | 1.666 | 1.7 | 1.734 | 0.051 | 0.085 | 0.119 |  |  |  |  |
| NCP303LSN18T1 | 1.764 | 1.8 | 1.836 | 0.054 | 0.090 | 0.126 |  |  |  |  |
| NCP303LSN19T1 | 1.862 | 1.9 | 1.938 | 0.057 | 0.095 | 0.133 |  |  |  |  |
| NCP303LSN20T1 | 1.960 | 2.0 | 2.040 | 0.060 | 0.100 | 0.140 |  |  |  |  |
| NCP303LSN21T1 | 2.058 | 2.1 | 2.142 | 0.063 | 0.105 | 0.147 |  |  |  |  |
| NCP303LSN22T1 | 2.156 | 2.2 | 2.244 | 0.066 | 0.110 | 0.154 |  |  |  |  |
| NCP303LSN23T1 | 2.254 | 2.3 | 2.346 | 0.069 | 0.115 | 0.161 |  |  |  |  |
| NCP303LSN24T1 | 2.352 | 2.4 | 2.448 | 0.072 | 0.120 | 0.168 |  |  |  |  |
| NCP303LSN25T1 | 2.450 | 2.5 | 2.550 | 0.075 | 0.125 | 0.175 |  |  |  |  |
| NCP303LSN26T1 | 2.548 | 2.6 | 2.652 | 0.078 | 0.130 | 0.182 |  |  |  |  |
| NCP303LSN27T1 | 2.646 | 2.7 | 2.754 | 0.081 | 0.135 | 0.189 |  |  |  |  |
| NCP303LSN28T1 | 2.744 | 2.8 | 2.856 | 0.084 | 0.140 | 0.196 |  |  |  |  |
| NCP303LSN29T1 | 2.842 | 2.9 | 2.958 | 0.087 | 0.145 | 0.203 |  |  |  |  |
| NCP303LSN30T1 | 2.940 | 3.0 | 3.060 | 0.090 | 0.150 | 0.210 |  |  |  |  |
| NCP303LSN31T1 | 3.038 | 3.1 | 3.162 | 0.093 | 0.155 | 0.217 |  |  |  |  |
| NCP303LSN32T1 | 3.136 | 3.2 | 3.264 | 0.096 | 0.160 | 0.224 |  |  |  |  |
| NCP303LSN33T1 | 3.234 | 3.3 | 3.366 | 0.099 | 0.165 | 0.231 |  |  |  |  |
| NCP303LSN34T1 | 3.332 | 3.4 | 3.468 | 0.102 | 0.170 | 0.238 |  |  |  |  |
| NCP303LSN35T1 | 3.430 | 3.5 | 3.570 | 0.105 | 0.175 | 0.245 |  |  |  |  |
| NCP303LSN36T1 | 3.528 | 3.6 | 3.672 | 0.108 | 0.180 | 0.252 |  |  |  |  |
| NCP303LSN37T1 | 3.626 | 3.7 | 3.774 | 0.111 | 0.185 | 0.259 |  |  |  |  |
| NCP303LSN38T1 | 3.724 | 3.8 | 3.876 | 0.114 | 0.190 | 0.266 |  |  |  |  |
| NCP303LSN39T1 | 3.822 | 3.9 | 3.978 | 0.117 | 0.195 | 0.273 |  |  |  |  |
| NCP303LSN40T1 | 3.920 | 4.0 | 4.080 | 0.120 | 0.200 | 0.280 | 0.4 |  |  |  |
| NCP303LSN41T1 | 4.018 | 4.1 | 4.182 | 0.123 | 0.205 | 0.287 |  |  |  |  |
| NCP303LSN42T1 | 4.116 | 4.2 | 4.284 | 0.126 | 0.210 | 0.294 |  |  |  |  |
| NCP303LSN43T1 | 4.214 | 4.3 | 4.386 | 0.129 | 0.215 | 0.301 |  |  |  |  |
| NCP303LSN44T1 | 4.312 | 4.4 | 4.488 | 0.132 | 0.220 | 0.308 |  |  |  |  |
| NCP303LSN45T1 | 4.410 | 4.5 | 4.590 | 0.135 | 0.225 | 0.315 |  |  |  |  |
| NCP303LSN46T1 | 4.508 | 4.6 | 4.692 | 0.138 | 0.230 | 0.322 |  |  |  |  |
| NCP303LSN47T1 | 4.606 | 4.7 | 4.794 | 0.141 | 0.235 | 0.329 |  |  |  |  |
| NCP303LSN48T1 | 4.704 | 4.8 | 4.896 | 0.144 | 0.240 | 0.336 |  |  |  |  |
| NCP303LSN49T1 | 4.802 | 4.9 | 4.998 | 0.147 | 0.245 | 0.343 |  |  |  |  |

(1) Condition 1: $0.9-2.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.10 \mathrm{~V} ; 3.0-3.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\text {DET- }}-0.13 \mathrm{~V} ; 4.0-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}-0.16 \mathrm{~V}$
(2) Condition 2: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=\mathrm{V}_{\mathrm{DET}-}+2.0 \mathrm{~V}$
(3) Condition 3: $0.9-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.7 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.05 \mathrm{~V}$, Active Low 'L' Suffix Devices
(4) Condition 4: $0.9-1.0 \mathrm{~V}, \mathrm{~V}_{\text {in }}=0.85 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V} ; 1.1-1.5 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.0 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V} ; 1.6-4.9 \mathrm{~V}, \mathrm{~V}_{\text {in }}=1.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0.5 \mathrm{~V}$, Active Low 'L' Suffix Devices


Figure 3. NCP302/3 Series 0.9 V Detector Threshold Voltage vs. Temperature


Figure 5. NCP302/3 Series 4.5 V Detector Threshold Voltage vs. Temperature


Figure 4. NCP302/3 Series 2.7 V
Detector Threshold Voltage vs. Temperature


Figure 6. NCP302/3 Series 0.9 V
$C_{D}$ Delay Pin Threshold Voltage vs. Temperature


Figure 7. NCP302/3 Series 2.7 V
$C_{D}$ Delay Pin Threshold Voltage vs. Temperature


Figure 8. NCP302/3 Series 4.5 V
$C_{D}$ Delay Pin Threshold Voltage vs. Temperature


Figure 9. NCP302/3 Series 0.9 V
$C_{D}$ Delay Pin Sink Current vs. Voltage


Figure 11. NCP302/3 Series 4.5 V $C_{D}$ Delay Pin Sink Current vs. Voltage


Figure 13. NCP302/3 Series 2.7 V Output Time Delay vs. Capacitance


Figure 10. NCP302/3 Series 2.7 V $C_{D}$ Delay Pin Sink Current vs. Voltage


Figure 12. NCP302/3 Series 0.9 V Output Time Delay vs. Capacitance


Figure 14. NCP302/3 Series 4.5 V Output Time Delay vs. Capacitance

## NCP302, NCP303



Figure 15. NCP302H/3L Series 0.9 V Reset Output Voltage vs. Input Voltage


Figure 17. NCP302H/3L Series 4.5 V Reset Output Voltage vs. Input Voltage


Figure 19. NCP302H/3L Series 2.7 V Reset Output Sink Current vs. Output Voltage


Figure 16. NCP302H/3L Series 2.7 V Reset Output Voltage vs. Input Voltage


Figure 18. NCP302H/3L Series 0.9 V Reset Output Sink Current vs. Output Voltage


Figure 20. NCP302H/3L Series 4.5 V
Reset Output Sink Current vs. Output Voltage


Figure 21. NCP302/3 Series 0.9 V Input Current vs. Input Voltage


Figure 23. NCP302/3 Series 4.5 V Input Current vs. Input Voltage


Figure 25. NCP302/3 Series 2.7 V
Reset Output Time Delay vs. Temperature


Figure 22. NCP302/3 Series 2.7 V Input Current vs. Input Voltage


Figure 24. NCP302/3 Series 0.9 V
Reset Output Time Delay vs. Temperature


Figure 26. NCP302/3 Series 4.5 V Reset Output Time Delay vs. Temperature


Figure 27. NCP302H/3L Series 0.9 V Reset Output Sink Current vs. Input Voltage


Figure 29. NCP302H/3L Series 4.5 V Reset Output Sink Current vs. Input Voltage


Figure 31. NCP302/3 Series 2.7 V
$C_{D}$ Delay Pin Sink Current vs. Input Voltage


Figure 28. NCP302H/3L Series 2.7 V Reset Output Sink Current vs. Input Voltage


Figure 30. NCP302/3 Series 0.9 V $C_{D}$ Delay Pin Sink Current vs. Input Voltage


Figure 32. NCP302/3 Series 4.5 V
$C_{D}$ Delay Pin Sink Current vs. Input Voltage


Figure 33. NCP302H Series 0.9 V
Reset Output Source Current vs. Input Voltage


Figure 35. NCP302H Series 4.5 V Reset Output Source Current vs. Input Voltage


Figure 34. NCP302H Series 2.7 V
Reset Output Source Current vs. Input Voltage


Figure 36. NCP302/3 Series Delay Resistance vs. Temperature

## OPERATING DESCRIPTION

The NCP302 and NCP303 series devices consist of a precision voltage detector that drives a time delay generator. Figures 37 and 38 show a timing diagram and a typical application. Initially consider that input voltage $V_{i n}$ is at a nominal level and it is greater than the voltage detector upper threshold ( $\mathrm{V}_{\mathrm{DET}+}$ ). The voltage at Pin 5 and capacitor $\mathrm{C}_{\mathrm{D}}$ will be at the same level as $\mathrm{V}_{\mathrm{in}}$, and the reset output (Pin 1) will be in the high state for active low devices, or in the low state for active high devices. If there is a power interruption and $\mathrm{V}_{\text {in }}$ becomes significantly deficient, it will fall below the lower detector threshold ( $\mathrm{V}_{\mathrm{DET}}$ ) and the external time delay capacitor $C_{D}$ will be immediately discharged by an internal N-channel MOSFET that connects to Pin 5. This sequence of events causes the Reset output to be in the low state for active low devices, or in the high state for active high devices. After completion of the power interruption,
$\mathrm{V}_{\text {in }}$ will again return to its nominal level and become greater than the $\mathrm{V}_{\mathrm{DET}+\text {. }}$ The voltage detector will turn off the N -channel MOSFET and allow pullup resistor $\mathrm{R}_{\mathrm{D}}$ to charge external capacitor $\mathrm{C}_{\mathrm{D}}$, thus creating a programmable delay for releasing the reset signal. When the voltage at Pin 5 exceeds the inverter/buffer threshold, typically $0.675 \mathrm{~V}_{\mathrm{in}}$, the reset output will revert back to its original state. The reset output time delay versus capacitance is shown in Figures 12 through 14. The voltage detector and inverter/buffer have built-in hysteresis to prevent erratic reset operation.

Although these device series are specifically designed for use as reset controllers in portable microprocessor based systems, they offer a cost-effective solution in numerous applications where precise voltage monitoring and time delay are required. Figures 38 through 45 show various application examples.


Figure 37. Timing Waveforms

## APPLICATION CIRCUIT INFORMATION



Figure 38. Microprocessor Reset Circuit


Figure 39. Battery Charge Indicator


Figure 40. Missing Pulse Detector or Frequency Detector


Figure 41. Microprocessor Reset Circuit with Additional Hysteresis

Comparator hysteresis can be increased with the addition of resistor $R_{H}$. The hysteresis equations have been simplified and do not account for the change of input current $l_{\text {in }}$ as $V_{\text {in }}$ crosses the comparator threshold. The internal resistance, $\mathrm{R}_{\mathrm{in}}$ is simply calculated using $\mathrm{I}_{\text {in }}=0.26 \mu \mathrm{~A}$ at 2.6 V .
$V_{\text {in }}$ Decreasing:

$$
\mathrm{V}_{\mathrm{th}}=\left(\frac{\mathrm{R}_{\mathrm{H}}}{\mathrm{R}_{\mathrm{in}}}+1\right)\left(\mathrm{V}_{\mathrm{DET}-}\right)
$$

$\mathrm{V}_{\text {in }}$ Increasing:

$$
\mathrm{V}_{\mathrm{th}}=\left(\frac{\mathrm{R}_{\mathrm{H}}}{\mathrm{R}_{\mathrm{in}} \| \mathrm{R}_{\mathrm{L}}}+1\right)\left(\mathrm{V}_{\mathrm{DET}-}+\mathrm{V}_{\mathrm{HYS}}\right)
$$

$\mathrm{V}_{\text {HYS }}=\mathrm{V}_{\text {in }}$ Increasing $-\mathrm{V}_{\text {in }}$ Decreasing

| Test Data |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathbf{V}_{\text {th }}$ Decreasing <br> $(\mathbf{m V})$ | $\mathbf{V}_{\text {th }}$ Increasing <br> $(\mathbf{m V})$ | $\mathbf{V}_{\mathbf{H Y s}}$ <br> $(\mathbf{m V})$ | $\mathbf{R}_{\mathrm{H}}$ <br> $(\Omega)$ | $\mathbf{R}_{\mathbf{L}}$ <br> $(\mathbf{k} \Omega)$ |
| 2.70 | 2.84 | 0.135 | 0 | - |
| 2.70 | 2.87 | 0.17 | 100 | 10 |
| 2.70 | 2.88 | 0.19 | 100 | 6.8 |
| 2.70 | 2.91 | 0.21 | 100 | 4.3 |
| 2.70 | 2.90 | 0.20 | 220 | 10 |
| 2.70 | 2.94 | 0.24 | 220 | 6.8 |
| 2.70 | 2.98 | 0.28 | 220 | 4.3 |
| 2.70 | 2.70 | 0.27 | 470 | 10 |
| 2.70 | 3.04 | 0.34 | 470 | 6.8 |
| 2.70 | 3.15 | 0.35 | 470 | 4.3 |



Figure 42. Simple Clock Oscillator


This circuit monitors the current at the load. As current flows through the load, a voltage drop with respect to ground appears across $R_{\text {sense }}$ where $V_{\text {sense }}=I_{\text {load }}{ }^{*} R_{\text {sense. }}$. The following conditions apply:

If:
$I_{\text {Load }}<\mathrm{V}_{\mathrm{DET}} / \mathrm{R}_{\text {sense }}$
$\mathrm{L}_{\text {Load }} \geq\left(\mathrm{V}_{\text {DET- }}+\mathrm{V}_{\text {HYS }}\right) / R_{\text {sense }}$

Then:
Reset Output = 0 V
Reset Output $=\mathrm{V}_{\mathrm{DD}}$

Figure 43. Microcontroller Systems Load Sensing


A simple voltage monitor can be constructed by connecting several voltage detectors as shown above. Each LED will sequentially turn on when the respective voltage detector threshold ( $\mathrm{V}_{\mathrm{DET}-}+\mathrm{V}_{\mathrm{HYS}}$ ) is exceeded. Note that detector thresholds ( $\mathrm{V}_{\text {DET- }}$ ) that range from 0.9 V to 4.9 V in 100 mV steps can be manufactured.

Figure 44. LED Bar Graph Voltage Monitor


For monitoring power supplies with a time delay reset, only a single NCP303 with delay capacitor is required.

Figure 45. Multiple Power Supply Undervoltage Supervision with Time Delay Reset

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


THIN SOT-23-5

ORDERING INFORMATION


NOTE: The ordering information lists seven standard under voltage thresholds with active low outputs. Additional active low threshold devices, ranging from 0.9 V to 4.9 V in 100 mV increments and NCP 302 active high output devices, ranging from 0.9 V to 4.9 V in 100 mV increments can be manufactured. Contact your ON Semiconductor representative for availability. The electrical characteristics of these additional devices are shown in Tables 1 and 2.

## MAX707, MAX708 $\mu$ P Supervisory Circuits

The MAX707/708 are cost-effective system supervisor circuits designed to monitor Vcc in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within $20 \mu \mathrm{sec}$ of Vcc falling through the reset voltage threshold. Reset is maintained with 200 mS of delay time after Vcc rise above the reset threshold. The MAX707/708 have a low quiescent current of $12 \mu \mathrm{~A}$ at $\mathrm{Vcc}=3.3 \mathrm{~V}$, an active-high RESET and active-low $\overline{\text { RESET }}$ with a push-pull output. The output is guaranteed valid down to $\mathrm{Vcc}=1.0 \mathrm{~V}$. The MAX707/708 have a Manual Reset $\overline{\mathrm{MR}}$ input and a +1.25 V threshold detector for power-fail input PFI. These devices are available in a Micro8 and SOIC-8 package.

## Features

- Precision Supply-Voltage Monitor MAX707: 4.63 V Reset Threshold Voltage MAX708: Standard Reset Threshold Voltages (Typical): $4.38 \mathrm{~V}, 3.08 \mathrm{~V}, 2.93 \mathrm{~V}, 2.63 \mathrm{~V}$
- Reset Threshold Available from 1.6 V to 4.9 V with 100 mV Increments (Factory Option)
- 200 mS (Typ) Reset Timeout Delay
- $12 \mu \mathrm{~A}(\mathrm{Vcc}=3.3 \mathrm{~V})$ Quiescent Current
- Active_High and Active_Low Reset Output
- Guaranteed RESET_L and RESET Output Valid to Vcc $=1.0 \mathrm{~V}$
- Voltage Monitor for Power-Fail or Low-Battery Warning
- 8 Pin SO or Micro8 Package


## Applications

- Computers
- Embedded System
- Battery Powered Equipment
- Critical $\mu$ P Power Supply Monitor


Figure 1. Representative Block Diagram


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


PIN CONFIGURATION


## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2819 of this data sheet.

MAXIMUM RATINGS (Note 1)

| Rating |  | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Supply Voltage |  | $\mathrm{V}_{\mathrm{CC}}$ | 6.0 | V |
| Output Voltage |  | $V_{\text {out }}$ | -0.3 to ( $\left.\mathrm{V}_{\mathrm{CC}}+0.3\right)$ | V |
| Output Current (All Outputs) |  | $\mathrm{l}_{\text {out }}$ | 20 | mA |
| Input Current (V) $\mathrm{V}_{\text {CC }}$ and GND) |  | $\mathrm{l}_{\text {in }}$ | 20 | mA |
| Thermal Resistance Junction to Air | $\begin{aligned} & \text { Micro8 } \\ & \text { SO-8 } \end{aligned}$ | $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 248 \\ & 187 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Ambient Temperature |  | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | $\mathrm{T}_{\text {stg }}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Latch-Up Performance | Positive Negative | ILATCH-UP | $\begin{aligned} & 300 \\ & 280 \end{aligned}$ | mA |

1. This device series contains ESD protection and exceeds the following tests:

Human Body Model 2000 V per MIL-STD-883, Method 3015.
Machine Model Method 200 V .
2. The maximum package power dissipation limit must not be exceeded.

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}} \quad \text { with } T_{J(\max )}=150^{\circ} \mathrm{C}
$$

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=1.0 \mathrm{~V}\right.$ to $5.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, unless otherwise noted. Typical values are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Voltage Range | $\mathrm{V}_{\mathrm{CC}}$ | 1.0 | - | 5.5 | V |
| $\begin{gathered} \text { Supply Current } \\ \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5.5 \mathrm{~V} \end{gathered}$ | ICC |  | $\begin{aligned} & 12 \\ & 16 \end{aligned}$ | $\begin{aligned} & 22 \\ & 28 \end{aligned}$ | $\mu \mathrm{A}$ |
| Reset Threshold <br> MAX707 $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ <br> MAX708 $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ <br> MAX708T $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ MAX708S $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ MAX708R $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {TH }}$ | $\begin{aligned} & 4.56 \\ & 4.50 \\ & \\ & 4.31 \\ & 4.25 \\ & 3.03 \\ & 3.00 \\ & \\ & 2.89 \\ & 2.85 \\ & \\ & 2.59 \\ & 2.55 \end{aligned}$ | 4.63 <br> 4.38 <br> 3.08 <br> 2.93 <br> 2.63 | $\begin{aligned} & 4.70 \\ & 4.75 \\ & \\ & 4.45 \\ & 4.50 \\ & \\ & 3.13 \\ & 3.15 \\ & \\ & 2.97 \\ & 3.00 \\ & \\ & 2.67 \\ & 2.70 \end{aligned}$ | V |
| Reset Threshold Hysteresis | $\mathrm{V}_{\mathrm{HYS}}$ | - | $0.01 \mathrm{~V}_{\text {TH }}$ | - | mV |
| $\mathrm{V}_{\mathrm{CC}}$ Falling Reset Delay ( $\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{TH}}+0.2 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{TH}}-0.2 \mathrm{~V}$ ) | $t_{\text {PD }}$ | - | 20 | - | $\mu \mathrm{S}$ |
| Reset Active Timeout Period | $\mathrm{t}_{\mathrm{RP}}$ | 140 | 200 | 330 | mS |
| $\begin{aligned} & \text { RESET_L, RESET_H Output Low Voltage } \\ & \mathrm{V}_{\mathrm{CC}} \geq 1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{Ol}}=100 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}>2.7 \mathrm{~V}, \mathrm{I}_{\mathrm{Ol}}=1.2 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{CC}}>4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{ol}}=3.2 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\text {ol }}$ | - | - | $\begin{aligned} & 0.3 \\ & 0.3 \\ & 0.3 \end{aligned}$ | V |
| RESET_L, RESET_H Output High Voltage $\begin{aligned} & \mathrm{V}_{\mathrm{CC}} \geq 1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{oh}}=50 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}>2.7 \mathrm{~V}, \mathrm{I}_{\mathrm{oh}}=500 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}>4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{oh}}=800 \mu \mathrm{~A} \end{aligned}$ | Voh | $\begin{aligned} & 0.8 \mathrm{~V}_{\mathrm{CC}} \\ & 0.8 \mathrm{~V}_{\mathrm{CC}} \\ & 0.8 \mathrm{~V}_{\mathrm{CC}} \end{aligned}$ | - | - | V |
| MR_L Pull-up Resistance | $\mathrm{R}_{\text {MRI }}$ | 50 | - | - | K $\Omega$ |
| MR_L Pulse Width ( $\mathrm{V}_{\text {TH }}(\max )<\mathrm{V}_{\mathrm{CC}}<5.5 \mathrm{~V}$ ) | $\mathrm{t}_{\text {MR }}$ | 1.0 | - | - | $\mu \mathrm{S}$ |
| MR_L Glitch Rejection ( $\left.\mathrm{V}_{\mathrm{TH}}(\mathrm{max})<\mathrm{V}_{\mathrm{CC}}<5.5 \mathrm{~V}\right)$ | - | - | 0.1 | - | $\mu \mathrm{S}$ |
| MR_L High_level Input Threshold ( $\left.\mathrm{V}_{\mathrm{TH}}(\mathrm{max})<\mathrm{V}_{\mathrm{CC}}<5.5 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{IH}}$ | $0.7 \mathrm{~V}_{\text {cc }}$ | - | - | V |
| MR_L Low_level Input Threshold ( $\mathrm{V}_{\text {TH }}(\max )<\mathrm{V}_{\text {CC }}<5.5 \mathrm{~V}$ ) | $\mathrm{V}_{\text {IL }}$ | - | - | $0.3 \mathrm{~V}_{\mathrm{CC}}$ | V |
| MR_L to RESET_L and RESET_H Output Delay $\left(\mathrm{V}_{\mathrm{TH}}(\max )<\mathrm{V}_{\mathrm{CC}}<5.5 \mathrm{~V}\right)$ | $\mathrm{t}_{\text {MD }}$ | - | 0.2 | - | $\mu \mathrm{S}$ |
| PFI Input Threshold (VCC $=3.3 \mathrm{~V}$, PFI Falling) | - | 1.20 | 1.25 | 1.3 | V |
| PFI Input Current | - | -250 | 0.01 | 250 | nA |
| PFI to PFO Delay ( $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {OVERDRIVE }}=15 \mathrm{mV}$ ) | - | - | 3.0 | - | $\mu \mathrm{S}$ |
| $\begin{gathered} \hline \text { PFO_L Output Low Voltage } \\ \mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}, \mathrm{I}_{\mathrm{ol}}=1.2 \mathrm{~mA} \\ \mathrm{~V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{ol}}=3.2 \mathrm{~mA} \end{gathered}$ | Vol | - | - | $\begin{aligned} & 0.3 \\ & 0.3 \end{aligned}$ | V |
| $\begin{gathered} \text { PFO_L Output High Voltage } \\ \mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}, \mathrm{I}_{\mathrm{oh}}=500 \mu \mathrm{~A} \\ \mathrm{~V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{oh}}=800 \mu \mathrm{~A} \end{gathered}$ | $\mathrm{V}_{\text {oh }}$ | $\begin{aligned} & 0.8 \mathrm{~V}_{\mathrm{CC}} \\ & 0.8 \mathrm{~V}_{\mathrm{CC}} \end{aligned}$ | - | - | V |

MAX707, MAX708

PIN DESCRIPTION (Pin No. with parentheses is for Micro8 package.)

| Pin No. | Symbol | Description |
| :---: | :---: | :--- |
| $1(3)$ | MR | Manual Reset Input. MR can be driven from TTL/CMOS logic or from a manual Reset switch. This input, <br> when floating, is internally pulled up to $\mathrm{V}_{\mathrm{CC}}$ with $50 \mathrm{~K} \Omega$ resistor. |
| $2(4)$ | $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage: $\mathrm{C}=100 \mathrm{nF}$ is recommended as a bypass capacitor between $\mathrm{V}_{\mathrm{CC}}$ and GND. |
| $3(5)$ | GND | Ground Reference |
| $4(6)$ | PFI | Power Fail Voltage Monitor Input. When PFI is less than 1.25 V, PFO goes low. Connect PFI to GND or <br> $\mathrm{V}_{\mathrm{CC}}$ when not used. |
| $5(7)$ | PFO | Power Fail Monitor Output. When PFI is less than 1.25 V , it goes low and sinks current. Otherwise, it <br> remains high. |
| $6(8)$ | NC | Non-connective Pin |
| $7(1)$ | RESET | Active Low RESET can be triggered by $\mathrm{V}_{\mathrm{CC}}$ below the threshold level or by a low signal on MR. It <br> remains low for 200 ms (typ.) after $\mathrm{V}_{\mathrm{CC}}$ rises above the reset threshold. |
| $8(2)$ | RESET | Active high RESET output the inverse of RESET one. |



Figure 2. MAX707/708 Series 1.60 V Reset Output Sink Current vs. Output Voltage


Figure 4. MAX707/708 Series 2.93 V Reset
Output Sink Current vs. Output Voltage


Figure 6. MAX707/708 Series 4.90 V Reset Output Sink Current vs. Output Voltage


Figure 3. MAX707/708 Series 1.60 V Reset Output Source Current vs. Input Voltage


Figure 5. MAX707/708 Series 2.93 V Reset Output Source Current vs. Input Voltage


Figure 7. MAX707/708 Series 4.90 V Reset Output Source Current vs. Input Voltage


Figure 8. MAX707/708 Series 1.60 V Detector Threshold Voltage vs. Temperature


Figure 10. MAX707/708 Series 4.90 V Detector Threshold Voltage vs. Temperature


Figure 9. MAX707/708 Series 2.93 V Detector Threshold Voltage vs. Temperature


Figure 11. MAX707/708 Series Vcc Falling Reset Delay vs. Temperature

## MAX707, MAX708

## APPLICATIONS INFORMATION

## Microprocessor Reset

To generate a processor reset, the manual Reset input allows different reset sources. A pushbutton switch can be
one of these. It is effectively debounced by the $1.0 \mu \mathrm{~s}$ minimum reset pulse width. As $\overline{\mathrm{MR}}$ is TTL/CMOS logic compatible, it can be driven by an external logic line.


Figure 12. RESET and MR Timing

## $\mathrm{V}_{\text {CC }}$ Transient Rejection

The MAX707/708 provides accurate $\mathrm{V}_{\mathrm{CC}}$ monitoring and reset timing during power-up, power-down, and brownout/sag conditions, and rejects negative glitches on the power supply line. Figure 13 shows the maximum transient duration vs. maximum negative excursion
(overdrive) for glitch rejection. For a given overdrive, the point of the curve is the maximum width of the glitch allowed before the device generates a reset signal. Transient immunity can be improved by adding a capacitor ( 100 nF for example) in close proximity to the $\mathrm{V}_{\mathrm{CC}}$ pin of the MAX707/708.


Figure 13. Maximum Transient Duration vs. Overdrive for Glitch Rejection at $25^{\circ} \mathrm{C}$

## RESET Signal Integrity During Power-Down

The MAX707/708 $\overline{\text { RESET }}$ output is valid until $\mathrm{V}_{\mathrm{CC}}$ falls below 1.0 V . Then, the output becomes an open circuit and no longer sinks current. This means CMOS logic inputs of the $\mu \mathrm{P}$ will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in the case RESET must be maintained valid to $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$, a pull down resistor must be connected from $\overline{\text { RESET }}$ to ground to discharge stray capacitances and hold the output low (Figure 14). This resistor value, though not critical, should be chosen large enough not to load $\overline{\mathrm{RESET}}$ and small enough to pull it to ground. $\mathrm{R}=100 \mathrm{k} \Omega$ will be suitable for most applications.


Figure 14. Ensuring RESET Valid to $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$

## Interfacing with $\mu \mathrm{Ps}$ with Bidirectional I/O Pins

Some $\mu$ Ps (such as Motorola 68HC11) have bidirectional reset pins. If, for example, the $\overline{\text { RESET output is driven high }}$ and the $\mu \mathrm{P}$ wants to put it low, indeterminate logic level may result. This can be avoided by adding a $4.7 \mathrm{k} \Omega$ resistor in series with the output of the MAX707/708 (Figure 15). If there are other components in the system that require a reset signal, they should be buffered so as not to load the reset line.


If the other components are required to follow the reset I/O of the $\mu \mathrm{P}$, the buffer should be connected as shown with the solid line.


Figure 15. Interfacing to Bidirectional Reset I/O

## Monitoring Additional Supply Levels

When connecting a voltage divider to PFI and adjusting it properly, you can monitor a voltage different than the unregulated DC one. As shown in Figure 16, to increase noise immunity, hysteresis may be added to the power-fail comparator just by a resistor between PFO and PFI. Not to unbalance the potential divider network, R3 should be 10 times the sum of the two resistors R1 and R2. If required, a capacitor between PFI and GND will reduce the sensitivity of the circuit to high-frequency noise on the line being monitored. The $\overline{\mathrm{PFO}}$ output may be connected to $\overline{\mathrm{MR}}$ input to generate a low level on the $\overline{\operatorname{RESET}}$ when Vcc_1 drops out of tolerance. Thus a $\overline{\text { RESET }}$ is generated when one of the two voltages is below its threshold level.


$$
\mathrm{VL}=1.25+\mathrm{R} 1 \times\left(\frac{1.25}{\mathrm{R} 2}+\frac{1.25-\mathrm{Vcc} \_2}{\mathrm{R} 3}\right)
$$

$$
\mathrm{VH}=1.25 \times\left(1+\mathrm{R} 1 \times\left(\frac{\mathrm{R} 2+\mathrm{R} 3}{\mathrm{R} 2 \times \mathrm{R} 3}\right)\right)
$$

$$
\mathrm{VHYS}=\mathrm{VH}-\mathrm{VL}=\frac{\mathrm{R} 1 \times \mathrm{Vcc} 2}{\mathrm{R} 3}
$$

Figure 16. Monitoring Additional Supply Levels

MAX707, MAX708

ORDERING INFORMATION

| Device | Package | Marking | Shipping |
| :--- | :---: | :---: | :---: |
| MAX707ESA-T | SO-8 | S707 | 2500 Tape \& Reel |
| MAX708ESA-T | SO-8 | S708 | 2500 Tape \& Reel |
| MAX708xESA-T (Note 3) | SO-8 | S708x | 2500 Tape \& Reel |
| MAX707CUA-T | Micro8 | SAC | 4000 Tape \& Reel |
| MAX708CUA-T | Micro8 | SAD | 4000 Tape \& Reel |
| MAX708xCUA-T (Note 3) | Micro8 | SAy (Note 4) | 4000 Tape \& Reel |

3. The " $x$ " denotes a suffix for $\mathrm{V}_{\mathrm{CC}}$ threshold - see Table 1.
4. The " y " denotes a suffix for $\mathrm{V}_{\mathrm{CC}}$ threshold - see Table 2.

Table 1. Suffix "x"

| Suffix | Reset Vcc Threshold (V) |
| :---: | :---: |
| T | 3.08 |
| S | 2.93 |
| R | 2.63 |

Table 2. Suffix " $y$ "

| Suffix | Reset Vcc Threshold (V) |
| :---: | :---: |
| E | 3.08 |
| F | 2.93 |
| G | 2.63 |

## Integrated Relay/ Inductive Load Driver

- Provides a Robust Driver Interface between D.C. Relay Coil and Sensitive Logic Circuits
- Optimized to Switch Relays from a 3 V to 5 V Rail
- Capable of Driving Relay Coils Rated up to 2.5 W at 5 V
- Features Low Input Drive Current \& Good Back-to-Front Transient Isolation
- Internal Zener Eliminates Need for Free-Wheeling Diode
- Internal Zener Clamp Routes Induced Current to Ground for Quieter System Operation
- Guaranteed Off State with No Input Connection
- Supports Large Systems with Minimal Off-State Leakage
- ESD Resistant in Accordance with the 2000 V Human Body Model
- Low Sat Voltage Reduces System Current Drain by Allowing Use of Higher Resistance Relay Coils


## Applications Include:

- Telecom: Line Cards, Modems, Answering Machines, FAX Machines, Feature Phone Electronic Hook Switch
- Computer \& Office: Photocopiers, Printers, Desktop Computers
- Consumer: TVs \& VCRs, Stereo Receivers, CD Players, Cassette Recorders, TV Set Top Boxes
- Industrial: Small Appliances, White Goods, Security Systems, Automated Test Equipment, Garage Door Openers


## RELAY/INDUCTIVE LOAD DRIVER SILICON SMALLBLOCK ${ }^{\text {™ }}$ INTEGRATED CIRCUIT



- Automotive: 5.0 V Driven Relays, Motor Controls, Power Latches, Lamp Drivers
This device is intended to replace an array of three to six discrete components with an integrated SMT part. It is available in a SOT-23 package. It can be used to switch 3 to 6 Vdc inductive loads such as relays, solenoids, incandescent lamps, and small DC motors without the need of a free-wheeling diode.

MAXIMUM RATINGS $\left(T_{J}=25^{\circ} \mathrm{C}\right.$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 6.0 | Vdc |
| Input Voltage | $\mathrm{V}_{\text {in(fwd) }}$ | 6.0 | Vdc |
| Reverse Input Voltage | $\mathrm{V}_{\text {in(rev) }}$ | -0.5 | Vdc |
| Repetitive Pulse Zener Energy Limit (Duty Cycle $\leq 0.01 \%$ ) | Ezpk | 50 | mJ |
| Output Sink Current - Continuous | $\mathrm{I}_{\mathrm{O}}$ | 500 | mA |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

## MDC3105LT1

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Total Device Power Dissipation ${ }^{(1)}$ | $\mathrm{P}_{\mathrm{D}}$ | 225 | mW |
| Derate above $25^{\circ} \mathrm{C}$ |  | 1.8 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Thermal Resistance Junction to Ambient | $\mathrm{R}_{\text {日JA }}$ | 556 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

1. FR-5 PCB of $1^{\prime \prime} \times 0.75^{\prime \prime} \times 0.062^{\prime \prime}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- |


| Output Zener Breakdown Voltage <br> (@ IT = 10 mA Pulse) | $\mathrm{V}_{\text {(BRout) }}$ | 6.2 | 6.6 | 7.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\mathrm{V}_{\text {(-BRout) }}$ | - | -0.7 | - | V |
| Output Leakage Current @ 0 Input Voltage $\begin{aligned} & \left(\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{Vdc}, \mathrm{~V}_{\text {in }}=\mathrm{O} . \mathrm{C} ., \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{Vdc}, \mathrm{~V}_{\text {in }}=\mathrm{O} . \mathrm{C} ., \mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}\right) \end{aligned}$ | loo | - | - | $\begin{aligned} & 5.0 \\ & 30 \end{aligned}$ | $\mu \mathrm{A}$ |
| Guaranteed "OFF" State Input Voltage ( $\mathrm{l}_{\mathrm{O}} \leq 100 \mu \mathrm{~A}$ ) | $\mathrm{V}_{\text {in(off) }}$ | - | - | 0.4 | V |

ON CHARACTERISTICS

| Input Bias Current ( $\mathrm{H}_{\text {FE }}$ Limited) $\left(\mathrm{l}_{\mathrm{O}}=250 \mathrm{~mA}, \mathrm{~V}_{\mathrm{O}}=0.25 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right)$ | $\mathrm{l}_{\text {in }}$ | - | 1.5 | 2.5 | mAdc |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Saturation Voltage $\left(\mathrm{l}_{\mathrm{O}}=250 \mathrm{~mA}, \mathrm{l}_{\mathrm{in}}=1.5 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{O} \text { (sat) }}$ | - | 0.25 | 0.4 | Vdc |
| $\begin{aligned} & \text { Output Sink Current -Continuous } \\ & \quad\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{CE}}=0.25 \mathrm{Vdc}, \mathrm{I}_{\text {in }}=1.5 \mathrm{~mA}\right) \end{aligned}$ | $\mathrm{I}_{(0 \text { (on) }}$ | 200 | 250 | - | mA |

TYPICAL APPLICATION-DEPENDENT SWITCHING PERFORMANCE
SWITCHING CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay Times: |  |  |  |  | nS |
| High to Low Propagation Delay; Figure 1 ( $5.0 \mathrm{~V} 74 \mathrm{HC04)}$ | $t_{\text {PHL }}$ | - | 55 | - |  |
| Low to High Propagation Delay; Figure 1 ( 5.0 V 74 HC 04 ) | tpli | - | 430 | - |  |
| High to Low Propagation Delay; Figures 1, 13 (3.0 V 74HC04) | $t_{\text {PHL }}$ | - | 85 | - |  |
| Low to High Propagation Delay; Figures 1, 13 (3.0 V 74HC04) | tpli | - | 315 | - |  |
| High to Low Propagation Delay; Figures 1, 14 (5.0 V 74LS04) | $t_{\text {PHL }}$ | - | 55 | - |  |
| Low to High Propagation Delay; Figures 1, 14 (5.0 V 74LS04) | tpLH | - | 2.4 | - | $\mu \mathrm{S}$ |
| Transition Times: |  |  |  |  | nS |
| Fall Time; Figure 1 ( 5.0 V 74 HC 04 ) | $t_{f}$ | - | 45 | - |  |
| Rise Time; Figure 1 ( 5.0 V 74 HC 04 ) | $t_{r}$ | - | 160 | - |  |
| Fall Time; Figures 1, 13 ( 3.0 V 74 HC 04 ) | $t_{f}$ | - | 70 | - |  |
| Rise Time; Figures 1, 13 (3.0 V 74HC04) | tr | - | 195 | - |  |
| Fall Time; Figures 1, 14 ( 5.0 V 74 LS 04 ) | $t_{f}$ | - | 45 | - |  |
| Rise Time; Figures 1, 14 (5.0 V 74LS04) | $\mathrm{tr}_{\mathrm{r}}$ | - | 2.4 | - | $\mu \mathrm{S}$ |



Figure 1. Switching Waveforms

# MDC3105LT1 

TYPICAL PERFORMANCE CHARACTERISTICS
(ON CHARACTERISTICS)


Figure 2. Transistor DC Current Gain


Figure 4. Threshold Effects


Figure 6. Output Saturation Voltage versus
I .II.


Figure 3. Input V-I Requirement Compared to Possible Source Logic Outputs


Figure 5. Transistor Output V-I Characteristic


Figure 7. Zener Clamp Voltage versus Zener

TYPICAL PERFORMANCE CHARACTERISTICS
(OFF CHARACTERISTICS)


Figure 8. Output Leakage Current versus Temperature


Figure 9. Output Leakage Current versus Supply Voltage


Figure 10. Safe Operating Area


Figure 11. Zener Repetitive Pulse Energy Limit on L/R Time Constant


Figure 12. Transient Thermal Response

## Using TTR Designing for Pulsed Operation

For a repetitive pulse operating condition, time averaging allows one to increase a device's peak power dissipation rating above the average rating by dividing by the duty cycle of the repetitive pulse train. Thus, a continuous rating of 200 mW of dissipation is increased to 1.0 W peak for a $20 \%$ duty cycle pulse train. However, this only holds true for pulse widths which are short compared to the thermal time constant of the semiconductor device to which they are applied.

For pulse widths which are significant compared to the thermal time constant of the device, the peak operating condition begins to look more like a continuous duty operating condition over the time duration of the pulse. In these cases, the peak power dissipation rating cannot be merely time averaged by dividing the continuous power rating by the duty cycle of the pulse train. Instead, the average power rating can only be scaled up a reduced amount in accordance with the device's transient thermal response, so that the device's max junction temperature is not exceeded.

Figure 12 of the MDC3105LT1 data sheet plots its transient thermal resistance, $\mathrm{r}(\mathrm{t})$ as a function of pulse width in ms for various pulse train duty cycles as well as for a single pulse and illustrates this effect. For short pulse widths near the left side of the chart, $\mathrm{r}(\mathrm{t})$, the factor, by which the continuous duty thermal resistance is multiplied to determine how much the peak power rating can be increased above the average power rating, approaches the duty cycle of the pulse train, which is the expected value. However, as the pulse width is increased, that factor eventually approaches 1.0 for all duty cycles indicating that the pulse width is sufficiently long to appear as a continuous duty condition to this device. For the MDC3105LT1, this pulse width is about 100 seconds. At this and larger pulse widths, the peak power dissipation capability is the same as the continuous duty power capability.

To use Figure 12 to determine the peak power rating for a specific application, enter the chart with the worst case pulse condition, that is the max pulse width and max duty cycle and determine the worst case $r(t)$ for your application. Then calculate the peak power dissipation allowed by using the equation,

$$
\begin{gathered}
\mathrm{Pd}(\mathrm{pk})=\left(\mathrm{T}_{\mathrm{Jmax}}-\mathrm{T}_{\text {Amax }}\right) \div\left(\mathrm{R}_{\theta \mathrm{JA}}{ }^{*} \mathrm{r}(\mathrm{t})\right) \\
\mathrm{Pd}(\mathrm{pk})=\left(150^{\circ} \mathrm{C}-\mathrm{T}_{\text {Amax }}\right) \div\left(556^{\circ} \mathrm{C} / \mathrm{W}^{*} \mathrm{r}(\mathrm{t})\right)
\end{gathered}
$$

Thus for a $20 \%$ duty cycle and a $\mathrm{PW}=40 \mathrm{~ms}$, Figure 12 yields $r(t)=0.3$ and when entered in the above equation, the max allowable $\mathrm{Pd}(\mathrm{pk})=390 \mathrm{~mW}$ for a max $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$.

Also note that these calculations assume a rectangular pulse shape for which the rise and fall times are insignificant compared to the pulse width. If this is not the case in a specific application, then the $\mathrm{V}_{\mathrm{O}}$ and $\mathrm{I}_{\mathrm{O}}$ waveforms should be multiplied together and the resulting power waveform integrated to find the total dissipation across the device. This then would be the number that has to be less than or equal to
the $\operatorname{Pd}(\mathrm{pk})$ calculated above. A circuit simulator having a waveform calculator may prove very useful for this purpose.

## Notes on SOA and Time Constant Limitations

Figure 10 is the Safe Operating Area (SOA) for the MDC3105LT1. Device instantaneous operation should never be pushed beyond these limits. It shows the SOA for the Transistor "ON" condition as well as the SOA for the zener during the turn-off transient. The max current is limited by the Izpk capability of the zener as well as the transistor in addition to the max input current through the resistor. It should not be exceeded at any temperature. The BJT power dissipation limits are shown for various pulse widths and duty cycles at an ambient temperature of $25^{\circ} \mathrm{C}$. The voltage limit is the max $\mathrm{V}_{\mathrm{CC}}$ that can be applied to the device. When the input to the device is switched off, the BJT "ON" current is instantaneously dumped into the zener diode where it begins its exponential decay. The zener clamp voltage is a function of that BJT current level as can be seen by the bowing of the $\mathrm{V}_{\mathrm{Z}}$ versus $\mathrm{I}_{\mathrm{Z}}$ curve at the higher currents. In addition to the zener's current limit impacting this device's 500 mA max rating, the clamping diode also has a peak energy limit as well. This energy limit was measured using a rectangular pulse and then translated to an exponential equivalent using the $2: 1$ relationship between the $\mathrm{L} / \mathrm{R}$ time constant of an exponential pulse and the pulse width of a rectangular pulse having equal energy content. These $\mathrm{L} / \mathrm{R}$ time constant limits in ms appear along the $\mathrm{V}_{\mathrm{Z}}$ versus $I_{Z}$ curve for the various values of $I_{Z}$ at which the Pd lines intersect the $\mathrm{V}_{\mathrm{CC}}$ limit. The $\mathrm{L} / \mathrm{R}$ time constant for a given load should not exceed these limits at their respective currents. Precise L/R limits on zener energy at intermediate current levels can be obtained from Figure 11.

## Designing with this Data Sheet

1. Determine the maximum inductive load current (at $\max \mathrm{V}_{\mathrm{CC}}$, min coil resistance \& usually minimum temperature) that the MDC3105 will have to drive and make sure it is less than the max rated current.
2. For pulsed operation, use the Transient Thermal Response of Figure 12 and the instructions with it to determine the maximum limit on transistor power dissipation for the desired duty cycle and temperature range.
3. Use Figures $10 \& 11$ with the SOA notes above to insure that instantaneous operation does not push the device beyond the limits of the SOA plot.
4. While keeping any $\mathrm{V}_{\mathrm{O} \text { (sat) }}$ requirements in mind, determine the max input current needed to achieve that output current from Figures $2 \& 6$.
5. For levels of input current below $100 \mu \mathrm{~A}$, use the input threshold curves of Figure 4 to verify that
there will be adequate input current available to turn on the MDC3105 at all temperatures.
6. For levels of input current above $100 \mu \mathrm{~A}$, enter Figure 3 using that max input current and determine the input voltage required to drive the MDC3105 from the solid $V_{\text {in }}$ versus $I_{i n}$ line. Select a suitable drive source family from those whose dotted lines cross the solid input characteristic line to the right of the $\mathrm{I}_{\mathrm{in}}, \mathrm{V}_{\text {in }}$ point.
7. Using the max output current calculated in step 1 , check Figure 7 to insure that the range of zener clamp voltage over temperature will satisfy all system \& EMI requirements.
8. Using Figures $8 \& 9$, insure that "OFF" state leakage over temperature and voltage extremes does not violate any system requirements.
9. Review circuit operation and insure none of the device max ratings are being exceeded.

APPLICATIONS DIAGRAMS


Figure 13. A 200 mW, 5.0 V Dual Coil Latching Relay Application with 3.0 V-HCMOS Level Translating Interface

## Max Continuous Current Calculation

for TX2-5V Relay, R1 $=178 \Omega$ Nominal $@ R_{A}=25^{\circ} \mathrm{C}$
Assuming $\pm 10 \%$ Make Tolerance,
$\mathrm{R} 1=178 \Omega{ }^{*} 0.9=160 \Omega \operatorname{Min} @ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$
$\mathrm{T}_{\mathrm{C}}$ for Annealed Copper Wire is $0.4 \% /{ }^{\circ} \mathrm{C}$
$R 1=160 \Omega$ * $\left[1+(0.004)^{*}\left(-40^{\circ}-25^{\circ}\right)\right]=118 \Omega \operatorname{Min} @-40^{\circ} \mathrm{C}$
$\mathrm{I}_{\mathrm{O}} \mathrm{Max}=(5.5 \mathrm{~V}$ Max $-0.25 \mathrm{~V}) / 118 \Omega=45 \mathrm{~mA}$


Figure 14. A 140 mW , 5.0 V Relay with TTL Interface


Figure 15. A Quad $5.0 \mathrm{~V}, 360 \mathrm{~mW}$ Coil Relay Bank

TYPICAL OPERATING WAVEFORMS


Figure 16. 20 Hz Square Wave Input


Figure 18. 20 Hz Square Wave Response


Figure 17. 20 Hz Square Wave Response


Figure 19. 20 Hz Square Wave Response

## INFORMATION FOR USING THE SOT-23 SURFACE MOUNT PACKAGE MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


SOT-23

## SOT-23 POWER DISSIPATION

The power dissipation of the SOT-23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $\mathrm{T}_{\mathrm{J}(\max )}$, the maximum rated junction temperature of the die, $\mathrm{R}_{\theta \mathrm{JA}}$, the thermal resistance from the device junction to ambient, and the operating temperature, $\mathrm{T}_{\mathrm{A}}$. Using the values provided on the data sheet for the SOT-23 package, $\mathrm{P}_{\mathrm{D}}$ can be calculated as follows:

$$
P_{D}=\frac{T_{J(\max )}-T_{A}}{R_{\theta J A}}
$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $\mathrm{T}_{\mathrm{A}}$ of $25^{\circ} \mathrm{C}$, one can
calculate the power dissipation of the device which in this case is 225 milliwatts.

$$
\mathrm{P}_{\mathrm{D}}=\frac{150^{\circ} \mathrm{C}-25^{\circ} \mathrm{C}}{556^{\circ} \mathrm{C} / \mathrm{W}}=225 \text { milliwatts }
$$

The $556^{\circ} \mathrm{C} / \mathrm{W}$ for the SOT-23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad ${ }^{\text {TM }}$. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be $100^{\circ} \mathrm{C}$ or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of $10^{\circ} \mathrm{C}$.
- The soldering temperature and time should not exceed $260^{\circ} \mathrm{C}$ for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be $5^{\circ} \mathrm{C}$ or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling
* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.


## Advance Information

## Integrated Relay/Solenoid

Driver
RELAY/SOLENOID DRIVER SILICON MONOLITHIC CIRCUIT BLOCK

- Optimized to Switch 3 V to 5 V Relays from a 5 V Rail
- Compatible with "TX" and "TQ" Series Telecom Relays Rated up to 625 mW at 3 V to 5 V
- Features Low Input Drive Current
- Internal Zener Clamp Routes Induced Current to Ground Rather Than Back to Supply
- Guaranteed Off State with No Input Connection
- Supports Large Systems with Minimal Off-State Leakage
- ESD Resistant in Accordance with the 2000 V Human Body Model
- Provides a Robust Driver Interface Between Relay Coil and Sensitive Logic Circuits


## Applications include

- Telecom Line Cards and Telephony
- Industrial Controls
- Security Systems
- Appliances and White Goods
- Automated Test Equipment
- Automotive Controls

This device is intended to replace an array of three to six discrete components with an integrated part. It can be used to switch other 3 to 5 Vdc Inductive Loads such as solenoids and small DC motors.


CASE 29-11, STYLE 14
TO-92

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 6.0 | Vdc |
| Recommended Operating Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | $2.0-5.5$ | Vdc |
| Input Voltage | $\mathrm{V}_{\text {in(fwd) }}$ | 6.0 | Vdc |
| Reverse Input Voltage | $\mathrm{V}_{\text {in(rev) }}$ | -0.5 | Vdc |
| Output Sink Current -Continuous | $\mathrm{I}_{\mathrm{O}}$ | 300 | mA |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
| :--- | :---: | :---: | :---: |
| Total Device Dissipation <br> (1) <br> Derate above $25^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | 625 | mW |
| Thermal Resistance Junction to Ambient | $\mathrm{R}_{\theta \mathrm{JA}}$ | 200 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

1. FR-5 PCB of $1^{\prime \prime} \times 0.75^{\prime \prime} \times 0.062^{\prime \prime}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OFF CHARACTERISTICS |  |  |  |  |  |
| Output Zener Breakdown Voltage <br> (@IT = 10 mA Pulse) | $\begin{aligned} & V_{\text {(BRout) }} \\ & V_{\text {(-BRout) }} \end{aligned}$ | $6.4$ | $\begin{gathered} \hline 6.8 \\ -0.7 \end{gathered}$ | 7.2 | V |
| Output Leakage Current @ 0 Input Voltage $\begin{aligned} & \left(\mathrm{V}_{\text {out }}=5.5 \mathrm{Vdc}, \mathrm{~V}_{\text {in }}=\mathrm{O} . \mathrm{C} ., \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\text {out }}=5.5 \mathrm{Vdc}, \mathrm{~V}_{\text {in }}=\mathrm{O} . \mathrm{C} ., \mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}\right) \end{aligned}$ | loo | - | - | $\begin{aligned} & 5.0 \\ & 30 \end{aligned}$ | $\mu \mathrm{A}$ |

ON CHARACTERISTICS

| Input Bias Current @ $\mathrm{V}_{\text {in }}=4.0 \mathrm{Vdc}$ $\left(\mathrm{I}_{\mathrm{O}}=250 \mathrm{~mA}, \mathrm{~V}_{\text {out }}=0.4 \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right)$ (correlated to a measurement @ $25^{\circ} \mathrm{C}$ ) | $\mathrm{l}_{\text {in }}$ | - | 2.5 | - | mAdc |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Saturation Voltage $\left(\mathrm{l}_{\mathrm{O}}=250 \mathrm{~mA}, \mathrm{~V}_{\mathrm{in}}=4.0 \mathrm{Vdc}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}\right)$ $\text { (correlated to a measurement @ } 25^{\circ} \mathrm{C} \text { ) }$ |  | - | 0.2 | 0.4 | Vdc |
| $\begin{aligned} & \text { Output Sink Current - Continuous } \\ & \left(T_{\mathrm{A}}=-40^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{CE}}=0.4 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{in}}=4.0 \mathrm{Vdc}\right) \\ & \left(\text { correlated to a measurement } @ 25^{\circ} \mathrm{C}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{C} \text { (on) }}$ | 250 | - | - | mA |

## TYPICAL APPLICATION-DEPENDENT SWITCHING PERFORMANCE

SWITCHING CHARACTERISTICS

| Characteristic | Symbol | $\mathrm{V}_{\mathrm{cc}}$ | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay Times: |  |  |  |  |  | ns |
| High to Low Propagation Delay; Figures 1, 2 ( 5.0 V 74 HC 04 ) | $\mathrm{t}_{\text {PHL }}$ | 5.5 | - | 55 | - |  |
| Low to High Propagation Delay; Figures 1, 2 (5.0 V 74HC04) | $t_{\text {PLH }}$ | 5.5 | - | 430 | - |  |
| High to Low Propagation Delay; Figures 1, 3 (3.0 V 74HC04) | $t_{\text {PHL }}$ | 5.5 | - | 85 | - |  |
| Low to High Propagation Delay; Figures 1, 3 (3.0 V 74HC04) | $t_{\text {PLH }}$ | 5.5 | - | 315 | - |  |
| High to Low Propagation Delay; Figures 1, 4 (5.0 V 74LS04) | $t_{\text {PHL }}$ | 5.5 | - | 55 | - |  |
| Low to High Propagation Delay; Figures 1, 4 (5.0 V 74LS04) | tplh | 5.5 | - | 2385 | - |  |
| Transition Times: |  |  |  |  |  | ns |
| Fall Time; Figures 1, 2 ( $5.0 \mathrm{~V} 74 \mathrm{HC04}$ ) | $t_{f}$ | 5.5 | - | 45 | - |  |
| Rise Time; Figures 1, 2 ( 5.0 V 74 HC 04 ) | $\mathrm{t}_{\mathrm{r}}$ | 5.5 | - | 160 | - |  |
| Fall Time; Figures 1, 3 (3.0 V 74HC04) | $t_{f}$ | 5.5 | - | 70 | - |  |
| Rise Time; Figures 1, 3 (3.0 V 74HC04) | $\mathrm{tr}_{\mathrm{r}}$ | 5.5 | - | 195 | - |  |
| Fall Time; Figures 1, 4 (5.0 V 74LS04) | $t_{f}$ | 5.5 | - | 45 | - |  |
| Rise Time; Figures 1, 4 ( $5.0 \mathrm{~V} 74 \mathrm{LSO4}$ ) | $t_{r}$ | 5.5 | - | 2400 | - |  |
| Input Slew Rate ${ }^{(1)}$ | $\Delta \mathrm{V} / \Delta \mathrm{t}$ in | 5.5 | TBD | - | - | V/ms |

1. Minimum input slew rate must be followed to avoid overdissipating the device.


Figure 1. Switching Waveforms


Figure 2. A $\mathbf{3 . 0} \mathbf{- V}$, $200-\mathrm{mW}$ Dual Coil Latching Relay Application with 5.0 V -HCMOS Interface


Figure 3. A 3.0-V, 200-mW Dual Coil Latching Relay Application with 3.0 V-HCMOS Interface


Figure 4. A 3.0-V, 200-mW Dual Coil Latching Relay Application with TTL Interface


Figure 5. Typical 5.0 V, 140 mW Coil Dual Relay Application

TYPICAL OPERATING WAVEFORMS
(Circuit of Figure 5)


Figure 6. 20 Hz Square Wave Input


Figure 8. 20 Hz Square Wave Response


Figure 10. Pulsed Current Gain


Figure 7. 20 Hz Square Wave Response


Figure 9. 20 Hz Square Wave Response


Figure 11. Collector Saturation Region

## MC1413, MC1413B, NCV1413B

## High Voltage, High Current Darlington Transistor Arrays

The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 500 mA permit them to drive incandescent lamps.

The MC1413, B with a $2.7 \mathrm{k} \Omega$ series input resistor is well suited for systems utilizing a 5.0 V TTL or CMOS Logic.


Figure 1. Representative Schematic Diagram


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PIN CONNECTIONS

(Top View)
ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC1413D | SO-16 | 48 Units/Rail |
| MC1413DR2 | SO-16 | 2500 Tape \& Reel |
| MC1413P | PDIP-16 | 25 Units/Rail |
| MC1413BD | SO-16 | 48 Units/Rail |
| MC1413BDR2 | SO-16 | 2500 Tape \& Reel |
| MC1413BP | PDIP-16 | 25 Units/Rail |
| NCV1413BDR2 | SO-16 | 2500 Tape \& Reel |

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2839 of this data sheet.

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, and rating apply to any one device in the package, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Output Voltage | $\mathrm{V}_{\mathrm{O}}$ | 50 | V |
| Input Voltage | $V_{1}$ | 30 | V |
| Collector Current - Continuous | $\mathrm{I}_{\mathrm{C}}$ | 500 | mA |
| Base Current - Continuous | $\mathrm{I}_{\mathrm{B}}$ | 25 | mA |
| Operating Ambient Temperature Range <br> MC1413 <br> MC1413B <br> NCV1413B | $\mathrm{T}_{\text {A }}$ | $\begin{aligned} & -20 \text { to }+85 \\ & -40 \text { to }+85 \\ & -40 \text { to }+125 \end{aligned}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Thermal Resistance, Junction-to-Ambient Case 648, P Suffix Case 751B, D Suffix | $R \theta_{\mathrm{JA}}$ | $\begin{gathered} 67 \\ 100 \end{gathered}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case Case 648, P Suffix Case 751B, D Suffix | $R \theta_{\mathrm{Jc}}$ | $\begin{aligned} & 22 \\ & 20 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Characteristic |  | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Leakage Current $\begin{aligned} & \left(\mathrm{V}_{\mathrm{O}}=50 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}\right) \\ & \left(\mathrm{V}_{\mathrm{O}}=50 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right) \end{aligned}$ | All Types All Types | $I_{\text {CEX }}$ | - | - | $\begin{gathered} 100 \\ 50 \end{gathered}$ | $\mu \mathrm{A}$ |
| Collector-Emitter Saturation Voltage $\begin{aligned} & \left(I_{C}=350 \mathrm{~mA}, \mathrm{I}_{\mathrm{B}}=500 \mu \mathrm{~A}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=200 \mathrm{~mA}, \mathrm{I}_{\mathrm{B}}=350 \mu \mathrm{~A}\right) \\ & \left(\mathrm{I}_{\mathrm{C}}=100 \mathrm{~mA}, \mathrm{I}_{\mathrm{B}}=250 \mu \mathrm{~A}\right) \end{aligned}$ | All Types All Types All Types | $\mathrm{V}_{\text {CE(sat) }}$ | - | $\begin{gathered} 1.1 \\ 0.95 \\ 0.85 \end{gathered}$ | $\begin{aligned} & 1.6 \\ & 1.3 \\ & 1.1 \end{aligned}$ | V |
| Input Current - On Condition $\left(\mathrm{V}_{\mathrm{I}}=3.85 \mathrm{~V}\right)$ | MC1413, B | $I_{\text {(on) }}$ | - | 0.93 | 1.35 | mA |
| $\begin{array}{r} \text { Input Voltage - On Condition } \\ \left(\mathrm{V}_{\mathrm{CE}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=200 \mathrm{~mA}\right) \\ \left(\mathrm{V}_{\mathrm{CE}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=250 \mathrm{~mA}\right) \\ \left(\mathrm{V}_{\mathrm{CE}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=300 \mathrm{~mA}\right) \end{array}$ | MC1413, B <br> MC1413, B <br> MC1413, B | $V_{1(0 n)}$ | - | - | $\begin{aligned} & 2.4 \\ & 2.7 \\ & 3.0 \end{aligned}$ | V |
| Input Current - Off Condition $\left(\mathrm{I}_{\mathrm{C}}=500 \mu \mathrm{~A}, \mathrm{~T}_{\mathrm{A}}=85^{\circ} \mathrm{C}\right)$ | All Types | $I_{\text {(off) }}$ | 50 | 100 | - | $\mu \mathrm{A}$ |
| DC Current Gain $\left(\mathrm{V}_{\mathrm{CE}}=2.0 \mathrm{~V}, \mathrm{I}_{\mathrm{C}}=350 \mathrm{~mA}\right)$ |  | $\mathrm{h}_{\text {FE }}$ | 1000 | - | - | - |
| Input Capacitance |  | $\mathrm{C}_{1}$ | - | 15 | 30 | pF |
| Turn-On Delay Time ( $50 \% \mathrm{E}_{\mathrm{l}}$ to $50 \% \mathrm{E}_{\mathrm{O}}$ ) |  | $\mathrm{t}_{\text {on }}$ | - | 0.25 | 1.0 | $\mu \mathrm{S}$ |
| Turn-Off Delay Time ( $50 \% \mathrm{E}_{1}$ to $50 \% \mathrm{E}_{\mathrm{O}}$ ) |  | $\mathrm{t}_{\text {off }}$ | - | 0.25 | 1.0 | $\mu \mathrm{s}$ |
| Clamp Diode Leakage Current $\left(\mathrm{V}_{\mathrm{R}}=50 \mathrm{~V}\right)$ | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{I}_{\mathrm{R}}$ | - | - | $\begin{gathered} 50 \\ 100 \end{gathered}$ | $\mu \mathrm{A}$ |
| Clamp Diode Forward Voltage ( $\mathrm{I}_{\mathrm{F}}=350 \mathrm{~mA}$ ) |  | $V_{F}$ | - | 1.5 | 2.0 | V |

NOTE: NCV1413B $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.


Figure 2. Output Current versus Input Voltage


Figure 4. Typical Output Characteristics


Figure 3. Output Current versus Input Current


Figure 5. Input Characteristics - MC1413, B


Figure 6. Maximum Collector Current versus Duty Cycle (and Number of Drivers in Use)

## MC1413，MC1413B，NCV1413B

## MARKING DIAGRAMS

> PDIP-16
> P SUFFIX
> CASE 648


$$
\begin{gathered}
\text { SO-16 } \\
\text { D SUFFIX } \\
\text { CASE 751B }
\end{gathered}
$$

16
且月 日 月 日 月 Н 月
MC1413D AWLYWW \＃リ リ 日

16
 MC1413BD AWLYWW
 1

A＝Assembly Location
WL＝Wafer Lot
YY，Y＝Year
WW＝Work Week
＊This marking diagram also applies to NCV1413B．

## MC34271

## Liquid Crystal Display and Backlight Integrated Controller

The MC34271 is a low power dual switching voltage regulator, specifically designed for handheld and laptop applications, to provide several regulated output voltages using a minimum of external parts. Two uncommitted switching regulators feature a very low standby bias current of $5.0 \mu \mathrm{~A}$, and an operating current of 7.0 mA capable of supplying output currents in excess of 200 mA .

Both devices have three additional features. The first is an ELD Output that can be used to drive a backlight or a liquid crystal display. The ELD output frequency is the clock divided by 256 . The second feature allows four additional output bias voltages, in specific proportions to $\mathrm{V}_{\mathrm{B}}$, one of the switching regulated output voltages. It allows use of mixed logic circuitry and provides a voltage bias for N -Channel load control MOSFETs ${ }^{\mathrm{TM}}$. The third feature is an Enable input that allows a logic level signal to turn-"off" or turn-"on" both switching regulators.

Due to the low bias current specifications, this device is ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

## MC34271 Features:

- Low Standby Bias Current of $5.0 \mu \mathrm{~A}$
- Uncommitted Switching Regulators Allow Both Positive and Negative Supply Voltages
- Logic Enable Allows Microprocessor Control of All Outputs
- Synchronizable to External Clock
- Mode Commandable for ELD and LCD Interface
- Frequency Synchronizable
- Auxiliary Output Bias Voltages Enable Load Control via N-Channel FETs
MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Input Voltage | $V_{D D}$ | 16 | Vdc |
| Power Dissipation and Thermal Characteristics Maximum Power Dissipation - Case 873 Thermal Resistance, Junction-to-Ambient Thermal Resistance, Junction-to-Case | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $\mathrm{R}_{\text {өJC }}$ | $\begin{gathered} 1.43 \\ 100 \\ 60 \end{gathered}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{w} \end{gathered}$ |
| Output \#1 and \#2 Switch Current | $\mathrm{ISL}_{\text {\& }} \mathrm{I}_{\text {SB }}$ | 500 | mA |
| Output \#1 and \#2 "Off"-State Voltage | $V_{\text {SL }}$ | 60 | Vdc |
| Feedback Enable MOSFETs "Off"-State Voltage | $\mathrm{V}_{\mathrm{LF}}$ | 20 | Vdc |
| Operating Junction Temperature | TJ | 125 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\text {A }}$ | 0 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

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PIN CONNECTIONS AND MARKING DIAGRAM

(Top View)
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC34271FB | QFP-32 | 250 Units / Tray |

Representative Block Diagram


This device contains 350 active transistors

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{DD}}=6.0 \mathrm{~V}$, for typical values $\mathrm{T}_{\mathrm{A}}=$ Low to High [Note 1], for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| Reference Voltage ( $\mathrm{T}_{J}=25^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{\text {ref }}$ | 1.225 | 1.250 | 1.275 | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ to 12.5 V ) | Regline | - | 2.0 | 10 | mV |
| Load Regulation ( $\mathrm{l}_{0}=0$ to $120 \mu \mathrm{~A}$ ) | Regload | - | 2.0 | 10 | mV |
| Total Variation (Line, Load and Temperature) | $\mathrm{V}_{\text {ref }}$ | 1.215 | - | 1.285 | V |

ERROR AMPLIFIERS

| Input Offset Voltage $\left(\mathrm{V}_{\mathrm{CM}}=1.25 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{IO}}$ | - | 1.0 | 10 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current $\left(\mathrm{V}_{\mathrm{CM}}=1.25 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | 120 | 600 | nA |
| Open Loop Voltage Gain $\left(\mathrm{V}_{\mathrm{CM}}=1.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{COMP}}=2.0 \mathrm{~V}\right)$ | $\mathrm{A}_{\mathrm{VOL}}$ | 80 | 100 | - | dB |
| Output Voltage Swing |  |  |  |  | V |
| High State $\left(\mathrm{I}_{\mathrm{OH}}=-100 \mu \mathrm{~A}\right)$ | $\mathrm{Ve}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{A}}-1.5$ | 4.0 | 5.5 |  |
| Low State $\left(\mathrm{IOL}_{\mathrm{OL}}=100 \mu \mathrm{~A}\right)$ | $\mathrm{Ve}_{\mathrm{OL}}$ | 0 | - | 1.0 |  |

## BIAS VOLTAGE

| Voltage $\left(\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}\right.$ to $\left.12.5 \mathrm{~V}, \mathrm{I}_{\mathrm{O}}=0\right)$ | $\mathrm{V}_{\mathrm{A}}$ | 4.6 | 5.0 | 5.4 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

## OSCILLATOR AND PWM SECTIONS

| Total Frequency Variation Over Line and Temperature $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ to $10 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=0^{\circ}$ to $70^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{T}}=169 \mathrm{k}$ | fosc | 90 | 115 | 140 | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Duty Cycle at Each Output Maximum Minimum | $\begin{aligned} & \mathrm{DC}_{\text {max }} \\ & \mathrm{DC}_{\text {min }} \end{aligned}$ | $92$ | $95$ | $\overline{0}$ | \% |
| Sync Input <br> Input Resistance $\left(\mathrm{V}_{\text {sync }}=3.5 \mathrm{~V}\right.$ ) Minimum Sync Pulse Width | $R_{\text {sync }}$ <br> $\mathrm{T}_{\mathrm{p}}$ | 25 | $\begin{aligned} & 50 \\ & 1.0 \end{aligned}$ | 100 | $\begin{aligned} & \mathrm{k} \Omega \\ & \mu \mathrm{~s} \end{aligned}$ |

## OUTPUT MOSFETs

| Output Voltage - "On"-State $\left(\mathrm{I}_{\text {sink }}=200 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 150 | 250 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Current - "Off"-State $\left(\mathrm{V}_{\mathrm{OH}}=40 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{OH}}$ | - | 0.1 | 1.0 | $\mu \mathrm{~A}$ |
| Rise and Fall Times | $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | - | 50 | - | ns |

## EL DISCHARGE OUTPUT (ELD) AND DRV ${ }_{1}$

| Output Voltage - "On"-State $\left(I_{\text {sink }}=100 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 30 | 100 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Voltage - "On"-State $\left(\mathrm{I}_{\text {sink }}=50 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OL}}$ | - | 2.0 | 2.5 | V |
| Output Voltage - "Off"-State $\left(\mathrm{I}_{\text {source }}=-100 \mu \mathrm{~A}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{DD}}-0.5$ | 5.9 | - | V |
| Output Voltage - "Off"-State $\left(\mathrm{I}_{\text {source }}=-50 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{DD}}-3.5$ | 3.3 | - | V |

FEEDBACK ENABLE SWITCHES ( $\mathrm{DS}_{1}, \mathrm{DS}_{2}$ )

| Output Voltage - "Low"-State $\left(\mathrm{I}_{\text {sink }}=1.0 \mathrm{~mA}\right)$ | Vfe OL | - | 10 | 100 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Current - "Off"-State $\left(\mathrm{V}_{\mathrm{OH}}=12.5 \mathrm{~V}\right)$ | Ifeor | - | 0.6 | 1.0 | $\mu \mathrm{~A}$ |

## SWITCHED V ${ }_{\text {DD }}$ OUTPUT (SW ${ }_{1}$ )

| Output Voltage |  |  |  |  | V |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Switch "On" $\left(E N_{1}=1, I_{\text {source }}=100 \mu \mathrm{~A}\right)$ | $\mathrm{Vsw}_{\mathrm{OH}}$ | 5.5 | 5.9 | 6.0 |  |
| Switch "Off" $\left(E N_{1}=0, I_{\text {sink }}=100 \mu \mathrm{~A}\right)$ | $\mathrm{Vsw}_{\mathrm{OL}}$ | 0 | 0.1 | 0.2 |  |

## AUXILIARY VOLTAGE OUTPUTS

| $\mathrm{V}_{0}$ Enable Switch |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| "On"-Resistance: $\mathrm{V}_{\mathrm{B}}$ to $\mathrm{V}_{0}$ | Rds | 0 | 2.0 | 10 | $\Omega$ |
| "Off"-State Leakage Current $\left(\mathrm{V}_{\mathrm{B}}=10 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{kg}}$ | 0 | 0.1 | 2.0 | $\mu \mathrm{~A}$ |
| $\mathrm{~V}_{0}$ Voltage $\left(\mathrm{V}_{\mathrm{B}}=30 \mathrm{~V}, \mathrm{I}_{\text {source }}=0 \mathrm{~mA}\right)$ | $\mathrm{V}_{0}$ | 29.5 | 29.9 | 30 | V |
| $\mathrm{~V}_{0}$ Resistance $\left(\mathrm{I}_{\text {source }}=4.0 \mathrm{~mA}\right)$ | $\mathrm{R}_{0}$ | 20 | 40 | 60 | $\Omega$ |

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) ( $\mathrm{V}_{\mathrm{DD}}=6.0 \mathrm{~V}$, for typical values $\mathrm{T}_{\mathrm{A}}=$ Low to High [Note 1], for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AUXILIARY VOLTAGE OUTPUTS |  |  |  |  |  |
| $V_{1}, V_{2}, V_{3}, V_{4}$ Outputs |  | 0.0500 | 0.0520 | 0.0535 |  |
| $1-V_{1} / V_{0}$ Ratio |  | 0.1010 | 0.1035 | 0.1065 |  |
| $1-V_{2} / V_{0}$ Ratio |  | 0.1010 | 0.1035 | 0.1065 |  |
| $V_{3} / V_{0}$ Ratio |  | 0.0500 | 0.0520 | 0.0535 |  |
| $V_{4} / V_{0}$ Ratio | $R_{0}$ | 20 | 40 | 60 | $\Omega$ |
| Output Resistance (I 1 source $=4.0 \mathrm{~mA})$ | $\mathrm{I}_{\text {ss }}$ | 5.0 | 10 | 20 | mA |
| Output Short Circuit Current |  |  |  |  |  |

LOGIC INPUTS (EN ${ }_{1}$, EN $_{2}$, MODE)

| Input Low State | $\mathrm{V}_{\mathrm{IL}}$ | 0 | - | 0.8 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input High State | $\mathrm{V}_{\mathrm{IH}}$ | 2.0 | - | 6.0 | V |
| Input Impedance | $\mathrm{R}_{\text {in }}$ | 25 | 50 | 100 | $\mathrm{k} \Omega$ |

SOFT START CONTROL ( $\mathbf{S S}_{\mathbf{1}}, \mathbf{S S}_{2}$ )

| Charge Current (Capacitor Voltage $=1.0 \mathrm{~V}$ to 4.0 V ) | $\mathrm{I}_{\text {chg }}$ | 0.5 | 1.0 | 2.5 | $\mu \mathrm{~A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Discharge Current (Capacitor Voltage $=1.0 \mathrm{~V}$ ) | $\mathrm{I}_{\text {dschg }}$ | 250 | 650 | - | $\mu \mathrm{A}$ |

TOTAL SUPPLY CURRENT

| $V_{D D}$ Current <br> Standby Mode $\left(\mathrm{EN}_{1}=\mathrm{EN}_{2}=0\right)$ | $\begin{aligned} & V_{D D}=6.0 \mathrm{~V} \\ & V_{D D}=16 \mathrm{~V} \end{aligned}$ | ${ }^{\text {ICC }}$ | - | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 15 \end{aligned}$ | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{D D}$ Current <br> Backlight "On" (EN $=1 ; \mathrm{EN}_{2}=0$ ) |  | $I_{\text {cc }}$ | - | 0.7 | 3.0 | mA |
| $V_{D D}$ Current <br> LCD "On" (No Inductor) ( $\mathrm{EN}_{1}=0 ; \mathrm{EN}_{2}=1$ ) |  | ${ }^{\text {ICC }}$ | - | 0.9 | 2.0 | mA |
| $\mathrm{V}_{\mathrm{B}}$ Current ( $\mathrm{V}_{0}=35 \mathrm{~V}$ ) |  | 10 | - | 1.2 | 3.0 | mA |

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.


Figure 1. Switch Output Duty Cycle versus Compensation Voltage


Figure 2. Error Amp Open Loop Gain and Phase versus Frequency


Figure 3. Reference Voltage Change versus Reference Current


Figure 5. FET Drain Voltage versus Sink Current


Figure 4. Quiescent Current versus Supply Voltage


Figure 6. ELD and DRV ${ }_{1}$ Switch Output Source and Sink Saturation versus Current


Figure 7. $V_{\text {ref }}$ and $V_{A}$ Variation versus Temperature


Figure 8. Oscillator Frequency Variation versus Temperature


Figure 9. Frequency versus Timing


Figure 10. $\mathrm{V}_{\mathrm{A}}, \mathrm{V}_{\text {ref }}$ versus $\mathrm{V}_{\mathrm{DD}}$

## OPERATING DESCRIPTION

The MC34271 is a monolithic, fixed frequency power switching regulator specifically designed for dc to dc converter and battery powered applications. This device operates as a fixed frequency, voltage mode regulator containing all the active functions required to directly implement step-up, step-down and voltage inverting converters with a minimum number of external components. Potential markets include battery powered, handheld, automotive, computer, industrial and cost sensitive consumer products. A description of each section is given below with the representative block diagram shown in Figure 11

## Oscillator

The oscillator frequency is programmed by resistor $\mathrm{R}_{\mathrm{T}}$. The charge to discharge ratio is controlled to yield a $95 \%$ maximum duty cycle at the switch outputs. During the fall time of the internal sawtooth waveform, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gates high, disabling the output switching MOSFETs. The internal sawtooth waveform has a nominal peak voltage of 3.3 V and a valley voltage of 1.7 V .

## Pulse Width Modulators

Both pulse width modulators consist of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied to the inverting input. A third input to the comparator has a 0.5 mA typical current source that can be used to implement soft start. Output switch conduction is initiated when the ramp waveform is discharged to the valley voltage. As the ramp voltage increases to a voltage that exceeds the error amplifier output, the latch resets, terminating output MOSFET conduction for the duration of the oscillator ramp. This PWM/latch combination prevents multiple output pulses during a given oscillator cycle.

Each PWM circuit is enabled by a logic input. When disabled, the entire block is turned off, drawing only leakage current from the power source. Shared circuits, like the
reference and oscillator, can be activated by either $\mathrm{EN}_{1}$ or $\mathrm{EN}_{2}$.

Circuit \#1 has an ELD output which may be used to drive an LCD or backlight. Its output frequency is the oscillator frequency divided by 1024.

## Error Amplifiers and Reference

Each error amplifier is provided with access to both inverting and noninverting inputs, and the output. The Error Amplifiers' Common Mode Input Range is 0 to 2.5 V . The amplifiers have a minimum dc voltage gain of 60 dB . The 1.25 V reference has an accuracy of $\pm 4.0 \%$ at room temperature.

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistive divider from the output to the error amplifier inverting input, and a series resistor-capacitor from the error amplifier output also to the to the inverting input. The step down converter is easiest to compensate for stability. The step-up and voltage inverting configurations, when operated as continuous conduction boost or flyback converters, are more difficult to compensate, and may require a lower loop design bandwidth.

## MOSFET Switch Outputs

The output MOSFETs are designed to switch a maximum of 60 V , with a peak drain current capability of 500 mA . In circuit \#1 an additional $\mathrm{DRV}_{1}$ output is provided for interfacing with an external MOSFET.The gates of the MOSFETs are held low when the circuit is disabled.

## Auxiliary Output Voltages

Output voltages $\mathrm{V}_{0}$ through $\mathrm{V}_{4}$ are provided for use as references or bias voltages. $\mathrm{V}_{0}$ is the circuit \#2 output voltage, when an internal FET switch is activated. The other auxiliary output voltages are proportional to $\mathrm{V}_{\mathrm{B}}$. The amplifiers for $V_{1}$ and $V_{2}$ are powered from $V_{0}$, while the amplifiers for $V_{3}$ and $V_{4}$ are powered from $V_{D D}$.

Figure 11. Representative Block Diagram Electroluminescent Backlight Configuration


Figure 12. Auxiliary Supply Configuration


Figure 13. EL PANEL Drive Circuit


## MC33441

## Electroluminescent Lamp Driver IC

The MC33441 is a DC-AC inverter integrated circuit for driving EL lamps. It can boost the supply voltage to the level required by EL lamps and also provide high voltage AC lamp excitation. It consists of an oscillator, a frequency divider, a coil driving circuit and a switched H -bridge network. The input supply voltage range is from 1.8 V to 3.5 V and is capable to supply a typical 140 Vpp AC output voltage. The standby current of the device is typically 10nA which is ideal for low power portable products. Externally, one inductor and one resistor are needed to generate the desirable voltage charge and to fine tune the oscillator's frequency. This device is offered in 8-Pin TSSOP miniature package. The operating temperature is $-20^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.

## Features:

- Battery Operation $1.8 \mathrm{~V}-3.5 \mathrm{~V}$
- Typical Voltage Output 140Vpp
- Typical Standby Current 10nA
- Internal Oscillator with External Tuning Resistor
- Enable Control Pin with a 300K Internal Pull-Down Resistor
- $8-$ Pin TSSOP Package $($ Thickness $=1.05 \mathrm{~mm}$, Width $=4.5 \mathrm{~mm}$,

Length $=3.1 \mathrm{~mm} \&$ Lead Pitch $=0.65 \mathrm{~mm})$
Types of Applications:

- Pagers, Cellular Phones, Portable CD Players/Minidisks
- Databanks, Calculators


## Simplified Block Diagram



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TSSOP-8 DTB SUFFIX CASE 948J

## PIN CONNECTIONS AND

 MARKING DIAGRAM
(Top View)
A =Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC33441DTBR2 | TSSOP-8 | 2500 Units / Reel |

## MC33441

Figure 1. Test Circuit


PIN FUNCTION DESCRIPTION

| Pin No. <br> (TSSOP-8) | Name |  |
| :---: | :--- | :--- |
| Pin 1 | VDD | Description |
| Pin 2 | ENB | Enable the whole device to operate |
| Pin 3 | RT1 | Internal oscillator's fine tuning resistance input |
| Pin 4 | VSS | Analog/Power ground |
| Pin 5 | COIL | Coil/Inductance input |
| Pin 6 | Filter | EL Filter |
| Pin 7 | EL2 | EL lamp driver output 2 |
| Pin 8 | EL1 | EL lamp driver output 1 |

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Max | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{DD}}$ | 7.5 | V |
| Digital Input Voltage Range | LOGIC $=0$ <br> LOGIC $=1$ | 0.5 <br> $\mathrm{~V}_{\mathrm{DD}}$ | V |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}(\max )}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -20 to +70 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -50 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | 300 | mW |
| Thermal Resistance, Junction-to-Air | $\mathrm{R}_{\theta \mathrm{JA}}$ | 178 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

DC ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{DD}}=2.65 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, Lamp Capacitance $=2.2 \mathrm{nF}$, Coil $=1 \mathrm{mH}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage | $V_{D D}$ | 1.8 | - | 3.5 | V |
| Output Voltage ( $1.8 \mathrm{~V}<\mathrm{V}_{\mathrm{DD}} \leq 3.5 \mathrm{~V}$ ) | $V_{E L}$ | 120 | 140 | 160 | V |
| Peak Coil Current ( $1.8 \mathrm{~V}<\mathrm{V}_{\mathrm{DD}} \leq 3.5 \mathrm{~V}$ ) | ICOIL | - | 70 | 150 | mA |
| Average Coil Current from Battery ( $1.8 \mathrm{~V}<\mathrm{V}_{\mathrm{DD}} \leq 3.5 \mathrm{~V}$ ) | IvDD | - | 35 | 75 | mA dc avg |
| Standby Current ( $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}, \mathrm{ENB}=0$ ) | Istand | - | 10 | 100 | nA |
| Clock Frequency ( $\mathrm{R}_{\mathrm{EXT}}=125 \mathrm{~K} \Omega$ ) | $\mathrm{F}_{\text {osc }}$ | 112 | 140 | 168 | kHz |
| Lamp Drive Frequency ( $\mathrm{F}_{\text {osc }}$ Divide by 384 ) | $\mathrm{F}_{\mathrm{EL}}$ | - | 364.6 | - | Hz |
| Coil Drive Frequency ( $\mathrm{Fosc}^{\text {Divide by }} 4$ ) | $\mathrm{F}_{\text {coil }}$ | - | 35 | - | kHz |
| Coil Drive Clock Duty Cycle | DC ${ }_{\text {COIL }}$ | - | 75 | - | \% |
| EL Lamp Capacitance Range | $\mathrm{C}_{\mathrm{EL}}$ | - | 2.2 | - | nF |

Figure 2. Output Waveform



Figure 3. Output Waveform vs. Time

## OPERATING DESCRIPTION

## General

The MC33441 is a DC-AC inverter integrated circuit for driving EL lamps. It can boost the supply voltage to the level required by EL lamps and also provide high voltage AC lamp excitation. It consists of an oscillator, a frequency divider, a coil driving circuit and a switched H -bridge network. The input supply voltage range is from 1.8 V to 3.5 V and is capable to supply a typical 140 Vpp AC output voltage. The standby current of the device is typically 10 nA which is ideal for low power portable products. Externally, one inductor and one resistor are needed to generate the desirable voltage charge and to fine tune the oscillator's frequency. This device is offered in 8 -Pin TSSOP packages. The operating temperature is $-20^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.

## Oscillator and Frequency Divider

Two circuits are put together to form the oscillator. They are Vref and Ibias. The functionality of Vref block is to generate a zero temperature coefficient (TC) voltage reference which is about 1.27 V . This 1.27 V will then be used in Ibias circuit to provide current biasing to all of the internal circuits with the value equal to Vref divided by an internal resistor. Besides of that, an external resistor is also connected to this circuit block for setting the oscillator's frequency. The temperature coefficient is dominated by the value of that resistor. Therefore, if a low TC resistor is used, the oscillator frequency's TC can be kept low.

The current mirrors with the induced current equal to the Vref divided by an external resistor are used to charge and discharge an internal capacitor to provide a $50 \%$ duty cycle clock signal. This original clock pulse will then be fed into the frequency divider which will generate two additional clock signals with different frequency and duty cycle to the coil-driver and the H -bridge circuits. The oscillator frequency is governed by the following equation:
$\mathrm{F}_{\mathrm{OSC}}=\left(\frac{1}{6 \times \mathrm{R}_{\mathrm{EXT}} \times \mathrm{C}_{\mathrm{INT}}} \mathrm{Hz}\right)=\frac{1.667 \times 10^{10}}{R_{\mathrm{EXT}}} \mathrm{Hz}$
$\mathrm{F}_{\mathrm{COIL}}=\mathrm{F}_{\mathrm{OSC}} \div 4$
$\mathrm{F}_{\mathrm{EL}}=\mathrm{F}_{\mathrm{OSC}} \div 384$
where $\mathrm{C}_{\text {INT }}$ is about 10 pF .

## Coil Driver

The coil driver is basically a simplified boost converter. It takes a higher frequency clock signal from the frequency divider to turn on/off the main switch alternatively. When the main switch is on, current will flow through the coil to ground. Once the switch is being turned off, the energy stored in the coil will be released to the external capacitor (EL lamp) through an internal diode. According to the frequency of the clock signals between the coil driver and the H -bridge, the external capacitor (EL lamp) will be charging to the desirable level.

Current limit circuit (typical 70mA \& max. 150mA) is implemented in this device. Since the current through the coil will increase corresponding to the input voltage, if the input voltage is high and the inductance of the coil is small, the coil can be saturated. The current limit feature is used to avoid this happen. The main switch is parallel to a much smaller switch which has their collector and their base connected together. However, the emitter of the smaller switch is tied to a sensing resistor while the emitter of the main switch is connected to ground. The coil current will split into two according to the sizing ratio between the main and the smaller switch. The current through the smaller switch will also flow through the sensing resistor and generates a voltage. If the voltage across this sensing resistor is above the pre-set value, then both switches
will be turned off and the energy will release to the EL lamp. And, those switches will remain off until the next clock cycle.

## H-Bridge Network

To achieve the 140 V peak-to-peak voltage, H-bridge network is used to charge and discharge the EL lamp. The switching frequency of the bridge network is controlled by a clock signal from the divider with its frequency much lower than the one to the coil-driver. Moreover, to reduce the current consumption, the biasing current to the two low-side switches of the H -bridge is not activated until the coil-driver circuit needed to release the energy to the EL lamp. Then, the biasing circuit will be on and be ready before the main switch in the coil-driver really starts to turn off.

## External Components

System designer will base on the application to decide the size and the type of the EL lamp to be used. The external resistance ( $\mathrm{R}_{\mathrm{EXT}}$ ) at RT1 pin determines the excitation frequency ( $\mathrm{F}_{\mathrm{EL}}$ ) for the lamp. The relationship between $\mathrm{R}_{\mathrm{EXT}}$ and the frequency is:
$\mathrm{F}_{\mathrm{EL}}=\mathrm{F}_{\mathrm{OSC}} \div 384$
By substitute the equation of FOSC from Oscillator \& Frequency Divider.

$$
\mathrm{F}_{\mathrm{EL}}=\frac{4.341 \times 10^{7}}{R_{\mathrm{EXT}}} \mathrm{~Hz}
$$

so
$R_{E X T}=\frac{4.341 \times 10^{7}}{F_{E L}} \Omega$

Moreover, if a low TC resistor is used, the oscillator frequency's TC can be kept low. The filter capacitor is to provide a smooth and more stable output waveform for the EL lamp. The value of this capacitor depends on the input voltage and the coil's inductance value. Equations below can be used to estimate filter capacitor's value at different input voltage.

## Best Case Approximation for the Filter Capacitor: <br> $\mathrm{C}_{\text {FILTER }}=0.026 \times\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\text {SW }}\right)^{2} /\left(\mathrm{L} \times \mathrm{F}_{\mathrm{OSC}}{ }^{2}\right)$

## Worst Case Approximation for the Filter Capacitor:

$\mathrm{C}_{\text {FILTER }}=0.085 \times\left(\mathrm{V}_{\text {in }}-\mathrm{V}_{\mathrm{SW}}\right)^{2} /\left(\mathrm{L} \times \mathrm{F}_{\mathrm{OSC}^{2}}{ }^{2}\right)$
where $\mathrm{V}_{\text {IN }}$ is the input voltage, $\mathrm{V}_{\text {SW }}$ is voltage across the switch when it is on, L is the coil's value and $\mathrm{F}_{\text {OSC }}$ is the clock frequency.
Measurement below is recorded with the condition: coil $=1 \mathrm{mH}$, EL lamp $=2.2 \mathrm{nF}$ and at room temperature.

Table 1: Reference for C $_{\text {FILTER }}$

| VDD | $\mathbf{R}_{\text {EXT }}$ | C $_{\text {FILTER }}$ |
| :---: | :---: | :---: |
| 1.8 V | $100 \mathrm{~K}-130 \mathrm{~K} \Omega$ | $5 \mathrm{n}-10 \mathrm{nF}$ |
| 2.0 V | $100 \mathrm{~K}-130 \mathrm{~K} \Omega$ | $10 \mathrm{n}-22 \mathrm{nF}$ |
| 2.5 V | $100 \mathrm{~K}-130 \mathrm{~K} \Omega$ | $10 \mathrm{n}-22 \mathrm{nF}$ |
| 3.0 V | $100 \mathrm{~K}-130 \mathrm{~K} \Omega$ | $22 \mathrm{nF}-33 \mathrm{nF}$ |



Figure 4. Oscillator Frequency vs. $\mathrm{R}_{\mathrm{EXT}}$


Figure 6. Current Consumption vs. Coil Inductance


Figure 8. Output Voltage vs. REXT


Figure 5. Lamp Frequency vs. $\mathrm{R}_{\mathrm{EXT}}$


Figure 7. Current Consumption vs. VDD


Figure 9. Output Voltage vs. Coil Inductance

## APPLICATION INFORMATION

## EL Lamp Selection

EL lamps are a laminate which exhibit a capacitance on the order of 2.5 nF to 3.5 nF per square inch. The light will emit as the high voltage is applied across the electrodes of this capacitance. The color of the emitted light is determined by the type of chemical used and the frequency of the excitation voltage. On the other hand, the lamp brightness increases approximately the square of the applied voltage and nearly linear to the excitation frequency. Once a lamp has been selected, the operating frequency and the essential voltage for the optimum performance is determined. Then, the driver circuit can begin to design.

## Inductor Selection (L1)

Use a $1 \mathrm{mH} / 0.15 \mathrm{~A}$ inductor for MC33441. Higher inductor values can be used to reduce the peak transient coil current from the battery supply. As the value of the inductor (L1), increases, the resistor (R1) value may need to increase correspondingly to provide optimum performance. While a lower inductor values lead to smaller physical size, it will generate a higher peak coil current. A lower resistor (R1) value should be used when a lower inductance coil is being used.

The inductor must have a saturation current rating equal to or bigger than the peak coil current which is 150 mA .

## Filter Capacitor Selection (C2)

See Table 1 for the estimated value of the filter capacitors based on the input voltage supply. Since the maximum voltage of the filter capacitor can reach 70 V or even 80 V , capacitor with high voltage rating will be required.

## Resistor Selection (R1)

Since the fundamental frequency of the oscillator is set by the external resistor (R1), the temperature coefficient of the frequency is dominated by the value of this resistor. A low temperature coefficient (TC) resistor is suggested to use for keeping the variation of oscillator's frequency low against the operation temperature range. (See Page 4, Fig. 3 \& Fig. 4)
$R 1=R_{E X T}=\frac{4.341 \times 10^{7}}{\mathrm{~F}_{\mathrm{EL}}} \Omega$

## Layout

The MC33441 is high output voltage operation make PC board layout critical to minimize ground bounce and noise. Locate input bypass capacitor, filter capacitor and oscillator's resistor as close to the device pins as possible.


Figure 10. MC33441 Demo Board Schematic

## COMPONENT SUPPLIER

| Supplier | Part Number | Description | Phone |
| :--- | :--- | :--- | :---: |
| Tech-Wave Industrial Co., Ltd. | Part\# CC-0012 | EL-Lamp: $14.5 \mathrm{~mm} \times 47 \mathrm{~mm}$ Color: <br> Yellow-Green | $(886)-2-22692827$ |
| Coils Electronics Co., Ltd. | Part\# CRCH664- <br> $102 \mathrm{~K}-831015$ | Inductor: $1 \mathrm{mH} / 0.15 \mathrm{~A}$ | (852)-2341-5539 |

Figure 11. MC33441 PC Board - Top View


Figure 12. MC33441 Component Placement Guide - Component Side


Figure 13. MC33441 PC Board - Bottom View


## CS1087

## Vacuum Fluorescent Display Tube Driver

The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 32-bit shift register, a 32-bit transparent data latch, a metal mask ROM, six 20 mA anode output drivers, twenty-three 2 mA anode output drivers, and three 50 mA grid drivers with output enables.

## Features

- Power On Reset
- Display Dimming Possible
- Three, 50 mA Grid Drivers
- Anode Options - DIP-40 and PCLL-44:
- 6 @ 20 mA
- 23 @ 2 mA
- Anode Options - SO-28L:
- 3 @ 20 mA
- 15 @ 2 mA


Figure 1. Application Diagram


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PLCC-44 FN SUFFIX CASE 777


SO-28L DW SUFFIX CASE 751F

ORDERING INFORMATION*

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS1087XN40 | DIP-40 <br> WIDE BODY | 9 Units/Rail |
| CS1087XFN44 | PLCC-44 | 23 Units/Rail |
| CS1087XFNR44 | PLCC-44 | 500 Tape \& Reel |
| CS1087XDW28 | SO-28L | 27 Units/Rail |
| CS1087XDWR28 | SO-28L | 1000 Tape \& Reel |

*For additional package options, consult your local ON Semiconductor sales office.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2863 of this data sheet.

## MAXIMUM RATINGS＊

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage（ $\mathrm{V}_{\mathrm{BB}}$ ） |  | -0.6 to +18 | V |
| Input Voltages（DIN，CLK，STB，GREN） |  | -0.6 to +6.0 | V |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility（Human Body Model） |  | 2.0 | kV |
| ESD Susceptibility（Machine Model） |  | 200 | V |
| Package Thermal Resistance，DIP－40 <br> Junction－to－Case，R ${ }_{\text {日JC }}$ <br> Junction－to－Ambient，R RJA |  | $\begin{aligned} & 20 \\ & 45 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| ```Package Thermal Resistance, PLCC-44 Junction-to-Case, R⿴囗⿱一兀口 Junction-to-Ambient, R RJA``` |  | $\begin{aligned} & 16 \\ & 55 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Package Thermal Resistance，SO－28L <br> Junction－to－Case，R RJC <br> Junction－to－Ambient，R $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{aligned} & 15 \\ & 75 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering： | Wave Solder（through hole styles only）Note 1 Reflow（SMD styles only）Note 2 | 260 Peak <br> 230 Peak | ${ }^{\circ} \mathrm{C}$ |

1． 10 second maximum．
2． 60 second maximum above $183^{\circ} \mathrm{C}$ ．
＊The maximum package power dissipation must be observed．

ELECTRICAL CHARACTERISTICS（ $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}} \leq 16.5 \mathrm{~V}$ ，Gnd $=0 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 105^{\circ} \mathrm{C}$ ；unless otherwise stated．Note 3．）

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {BB }}$ Input |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{BB}}$ Input Voltage | － | 8.0 | － | 16.5 | V |
| $\mathrm{I}_{\mathrm{BB} 0}$ Current | No outputs active， $\mathrm{V}_{\mathrm{BB}}=16.5 \mathrm{~V}$ | － | 2.0 | 5.0 | mA |
| Reset Mode | All outputs forced low． | － | 6.5 | 7.5 | V |

$\mathrm{D}_{\text {IN }}$, CLK，STB Inputs

| $\mathrm{V}_{\mathrm{IL} 1}$ ，Input Low Voltage | - | - | - | 1.6 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{IH}}$, Input High Voltage | - | 3.3 | - | - | V |
| $\mathrm{I}_{\mathrm{IL}}$, Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}}$ | - | 7.5 | 20.0 | $\mu \mathrm{~A}$ |

GREN Input

| $\mathrm{V}_{\mathrm{IL}}$, Input Low Voltage | - | - | - | 1.6 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{IH}}$, Input High Voltage | - | 3.3 | - | - | V |
| $\mathrm{I}_{\mathrm{IH}}$ ，Input Pull－down Current | $\mathrm{V}_{\mathrm{IN}}=3.325 \mathrm{~V}$ | - | 30 | 60 | $\mu \mathrm{~A}$ |

GRID1，GRID2，GRID3 Outputs

| $\mathrm{I}_{\mathrm{OL}}$ | Sink Current | 1.0 | - | - | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 50 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | IOUT $=-50 \mathrm{~mA}, \mathrm{~V}_{\mathrm{BB}}=12 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{BB}}-0.75$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

3．Designed to meet these characteristics over the stated voltage and temperature ranges，though may not be $100 \%$ parametrically tested in production．

ELECTRICAL CHARACTERISTICS (continued) ( $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}} \leq 16.5 \mathrm{~V}$, $\mathrm{Gnd}=0 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 105^{\circ} \mathrm{C}$; unless otherwise stated. Note 4.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AN24-AN29 Outputs |  |  |  |  |  |
| loL | Sink Current | 400 | - | - | $\mu \mathrm{A}$ |
| IOH | Source Current | 20 | - | - | mA |
| $\mathrm{V}_{\text {OL }}$ | lout $=400 \mu \mathrm{~A}$ | - | - | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{l}_{\text {OUT }}=-20 \mathrm{~mA}, \mathrm{~V}_{\text {BB }}=12 \mathrm{~V}$ | $V_{B B}-0.5$ | - | $V_{B B}$ | V |

AN1 - AN23 Outputs

| $\mathrm{I}_{\mathrm{OL}}$ | Sink Current | 100 | - | - | $\mu \mathrm{A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 2.0 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{I}_{\text {OUT }}=100 \mu \mathrm{~A}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | lout $=-2.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{BB}}=12 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{BB}}-0.5$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

## Dout Output

| $\mathrm{IOL}_{\mathrm{OL}}$ | Sink Current | 1.0 | - | - | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 1.0 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | $\mathrm{I}_{\text {OUT }}=-1.0 \mathrm{~mA}$ | 3.9 | - | 5.1 | V |

AC Characteristics: Input and Output Timing

| $\mathrm{F}_{\mathrm{C}}$, CLK Frequency | - | 0 | - | 1.0 | MHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TCL, CLK Low Time | - | 200 | - | - | ns |
| $\mathrm{T}_{\text {CH, }}$, CLK High Time | - | 200 | - | - | ns |
| TCR, CLK Rise Time | - | - | - | 100 | ns |
| TCF, CLK Fall Time | - | - | - | 100 | ns |
| $T_{\text {CD }}$, CLK Low to Dout Propagation Delay | - | - | - | 200 | ns |
| $\mathrm{T}_{\text {SC }}$, STB Low to CLK High Time | - | 50 | - | - | ns |
| $\mathrm{T}_{\text {ST }}$, STB High Time | - | 500 | - | - | ns |
| TAN, STB High to Anode Output Propagation Delay | - | - | - | 5.0 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GL}}$, Grid Turn On Propagation Delay | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}$ | - | - | 2.0 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GO}}$, Grid Turn Off Propagation Delay | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}$ | - | - | 5.0 | $\mu \mathrm{s}$ |
| TGR, Grid Rise Time | At rated load. Note 5. | 0.50 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GF}}$, Grid Fall Time | At rated load. Note 5. | 0.35 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {AR }}$, Anode Rise Time | At rated load. Note 5. | 0.40 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {AF }}$, Anode Fall Time | At rated load. Note 5. | 0.40 | - | 2.50 | $\mu \mathrm{s}$ |

4. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be $100 \%$ parametrically tested in production.
5. Grid and anode rise/fall times are measured from $10 \%$ and $90 \%$ points. Output currents are at the maximum rated currents for the respective stages.

## PACKAGE LEAD DESCRIPTION

| Package Lead Number |  |  | Lead Symbol | Function |
| :---: | :---: | :---: | :---: | :---: |
| 40L DIP | 44L PLCC | SO-28L | (29 Anode Configuration) |  |
| 1 | 14 | 1 | GRID1 | 50 mA grid output. |
| 2 | 15 | 2 | GRID2 | 50 mA grid output. |
| 3 | 16 | 3 | GRID3 | 50 mA grid output. |
| 4 | 17 | - | AN1 | 2.0 mA anode output. |
| 5 | 18 | 4 | AN2 | 2.0 mA anode output. |
| 6 | 19 | 5 | AN3 | 2.0 mA anode output. |
| 7 | 20 | 6 | AN4 | 2.0 mA anode output. |
| 8 | 21 | - | AN5 | 2.0 mA anode output. |
| 9 | 22 | 7 | AN6 | 2.0 mA anode output. |
| 10 | 24 | - | AN7 | 2.0 mA anode output. |
| 11 | 25 | - | AN8 | 2.0 mA anode output. |
| 12 | 26 | 8 | AN9 | 2.0 mA anode output. |
| 13 | 27 | - | AN10 | 2.0 mA anode output. |
| 14 | 28 | 9 | AN11 | 2.0 mA anode output. |
| 15 | 29 | 10 | AN12 | 2.0 mA anode output. |
| 16 | 30 | 11 | AN13 | 2.0 mA anode output. |
| 17 | 31 | 12 | AN14 | 2.0 mA anode output. |
| 18 | 32 | 13 | AN15 | 2.0 mA anode output. |
| 19 | 33 | - | AN16 | 2.0 mA anode output. |
| 20 | 35 | 14 | GND | Ground connection. |
| 21 | 36 | 15 | AN17 | 2.0 mA anode output. |
| 22 | 37 | - | AN18 | 2.0 mA anode output. |
| 23 | 38 | 16 | AN19 | 2.0 mA anode output. |
| 24 | 39 | 17 | AN20 | 2.0 mA anode output. |
| 25 | 40 | 18 | AN21 | 2.0 mA anode output. |
| 26 | 41 | 19 | AN22 | 2.0 mA anode output. |
| 27 | 42 | - | AN23 | 2.0 mA anode output. |
| 28 | 43 | 20 | AN24 | 20 mA anode output. |
| 29 | 44 | 21 | AN25 | 20 mA anode output. |
| 30 | 2 | 22 | AN26 | 20 mA anode output. |
| 31 | 3 | - | AN27 | 20 mA anode output. |
| 32 | 4 | - | AN28 | 20 mA anode output. |
| 33 | 5 | - | AN29 | 20 mA anode output. |
| 34 | 6 | 23 | Dout | Shift register data output. |
| 35 | 7 | 24 | $\mathrm{D}_{\text {IN }}$ | Shift register data input. |
| 36 | 8 | 25 | CLK | Shift register clock input. |
| 37 | 9 | 26 | STB | Transfer contents of shift registers to output stages. |
| 38 | 10 | 27 | GREN | Grid outputs enable. |
| 39 | 1, 11, 12, 23, 34 | - | NC | No connection. |
| 40 | 13 | 28 | $\mathrm{V}_{\mathrm{BB}}$ | Supply voltage input. |



Figure 2. Block Diagram

## OPERATION DESCRIPTION

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the $\mathrm{D}_{\text {IN }}$ pin at the rising edge of the CLK input. Thirty two bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the STB input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register/latch will cause the corresponding output to turn on. A logic low input to the shift register/latch will cause the corresponding output to turn off. Please note that if the STB is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.

The three GRID outputs are gated by the GREN input. When GREN is low, the GRID outputs are forced low regardless of the state of the corresponding latch output. When GREN is high, the GRID outputs correspond to the state of their respective latch outputs. The anode outputs, AN1 to AN29 are always enabled.

The Dout pin is the output of the last stage of the shift register to allow serial cascading of this IC with other devices. Data from the last stage of the shift register is supplied to the $D_{\text {OUT }}$ pin delayed by $1 / 2$ CLK cycle. Data on the $\mathrm{D}_{\text {OUT }}$ output changes with the falling edges of the CLK to prevent logic race conditions between the CLK and the $\mathrm{D}_{\text {IN }}$ of the next IC in the serial chain.

## CS1087

## APPLICATION INFORMATION

Table 1. Bit Pattern, G = Grid, A = Anode.

| Bit \# | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin Name | G1 | G2 | G3 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 | A13 |
| Bit \# | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Pin Name | A14 | A15 | A16 | A17 | A18 | A19 | A20 | A21 | A22 | A23 | A24 | A25 | A26 | A27 | A28 | A29 |



* Selected grid goes high only if input bit pattern from shift register to grid is high.

Figure 3. Typical Operation

Unused grid and anode drivers should have their respective bits set to logic low in the data stream.

Multiple grid or anode drivers may be connected together, but must be programmed to the same logic state for proper device operation. Maximum package power must be observed and care must be taken to maintian junction temperature below $+150^{\circ} \mathrm{C}$.

Care must be taken when interfacing this part to a microprocessor. The $\mathrm{D}_{\mathrm{OUT}}$ output $\mathrm{V}_{\mathrm{OH}}$ is specified at 3.9 V
to 5.1 V at an $\mathrm{I}_{\mathrm{OUT}}$ of -1.0 mA . Lower current loads will result in a higher output voltage. $\mathrm{V}_{\mathrm{OH}}=5.2 \mathrm{~V}(\mathrm{typ})$ with no load. $\mathrm{V}_{\mathrm{OH}}=5.7 \mathrm{~V}$ (max) with no load. Protection or workarounds for the device may be needed at the application level. No protection is needed when interfacing with other parts in this family (CS1087, CS1088, or CS1089).

MARKING DIAGRAMS



PIN CONNECTIONS

PLCC－44 FN SUFFIX CASE 777

A＝Assembly Location
WL，L＝Wafer Lot YY， $\mathrm{Y}=$ Year WW，W＝Work Week


|  | CS1087 <br> AWLYYWW |
| :---: | :---: |
|  | 晾昭昭 |

## CS1088

## Vacuum Fluorescent Display Tube Driver

The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 34-bit shift register, a 34-bit transparent data latch, a metal mask ROM, six 20 mA anode output drivers, twenty-five 2 mA anode output drivers, and three 50 mA grid drivers with output enables.

## Features

- Power On Reset
- Display Dimming Possible
- Three, 50 mA Grid Drivers
- Anodes:
- 6 @ 20 mA
$-25 @ 2 \mathrm{~mA}$


Figure 1. Application Diagram

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## ORDERING INFORMATION*

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS1088XN40 | DIP-40 <br> WIDE BODY | 9 Units/Rail |

*For additional package options, consult your local ON Semiconductor sales office.

## MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{BB}}$ ) |  | -0.6 to +18 | V |
| Input Voltages ( $\mathrm{D}_{\text {IN }}$, CLK, STB, GREN) |  | -0.6 to +6.0 | V |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| ESD Susceptibility (Machine Model) |  | 200 | V |
| Package Thermal Resistance, DIP-40 Junction-to-Case, R ®Jc Junction-to-Ambient, R ®JA |  | $\begin{aligned} & 20 \\ & 45 \end{aligned}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak <br> 230 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (8.0 V $\leq \mathrm{V}_{\mathrm{BB}} \leq 16.5 \mathrm{~V}$, Gnd $=0 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 105^{\circ} \mathrm{C}$; unless otherwise stated. Note 3.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | $\mathrm{V}_{\mathrm{BB}}$ Input | $\mathrm{V}_{\mathrm{BB}}$ Input Voltage | - | 8.0 | - | 16.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{BB} 0}$ Current | No outputs active, $\mathrm{V}_{\mathrm{BB}}=16.5 \mathrm{~V}$ | - | 2.0 | 5.0 | mA |
| Reset Mode | All outputs forced low. | - | 6.5 | 7.5 | V |

$\mathrm{D}_{\text {IN }}$, CLK, STB Inputs

| $\mathrm{V}_{\mathrm{IL} 1}$, Input Low Voltage | - | - | - | 1.6 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{IH}}$, Input High Voltage | - | 3.3 | - | - | V |
| $\mathrm{I}_{\mathrm{IL}}$, Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}}$ | - | 7.5 | 20.0 | $\mu \mathrm{~A}$ |

## GREN Input

| $\mathrm{V}_{\mathrm{IL}}$, Input Low Voltage | - | - | - | 1.6 | V |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{IH}}$, Input High Voltage | - | 3.3 | - | - | V |
| $\mathrm{I}_{\mathrm{IH}}$, Input Pull-down Current | $\mathrm{V}_{\mathbb{I N}}=3.325 \mathrm{~V}$ | - | 30 | 60 | $\mu \mathrm{~A}$ |

GRID1, GRID2, GRID3 Outputs

| $\mathrm{I}_{\mathrm{OL}}$ | Sink Current | 1.0 | - | - | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 50 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | $\mathrm{I}_{\text {OUT }}=-50 \mathrm{~mA}, \mathrm{~V}_{\mathrm{BB}}=12 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{BB}}-0.75$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

## AN24 - AN29 Outputs

| $\mathrm{I}_{\mathrm{OL}}$ | Sink Current | 400 | - | - | $\mu \mathrm{A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 20 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{l}_{\text {OUT }}=400 \mu \mathrm{~A}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | $\mathrm{I}_{\text {OUT }}=-20 \mathrm{~mA}, \mathrm{~V}_{\mathrm{BB}}=12 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{BB}}-0.5$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

3. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be $100 \%$ parametrically tested in production.

ELECTRICAL CHARACTERISTICS (continued) ( $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}} \leq 16.5 \mathrm{~V}$, Gnd $=0 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 105^{\circ} \mathrm{C}$; unless otherwise stated. Note 4.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| AN1 - AN23 Outputs |  |  |  |  |  |
| IOL | Sink Current | 100 | - | - | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 2.0 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{l}_{\mathrm{OUT}}=100 \mu \mathrm{~A}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | $\mathrm{l}_{\mathrm{OUT}}=-2.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{BB}}=12 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{BB}}-0.5$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

AC Characteristics: Input and Output Timing

| $\mathrm{F}_{\mathrm{C}}$, CLK Frequency | - | 0 | - | 1.0 | MHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TCL, CLK Low Time | - | 200 | - | - | ns |
| $\mathrm{T}_{\text {CH }}$, CLK High Time | - | 200 | - | - | ns |
| $\mathrm{T}_{\text {CR }}$, CLK R Rise Time | - | - | - | 100 | ns |
| TCF, CLK Fall Time | - | - | - | 100 | ns |
| TSC, STB Low to CLK High Time | - | 50 | - | - | ns |
| $\mathrm{T}_{\text {ST }}$, STB High Time | - | 500 | - | - | ns |
| TAN , STB High to Anode Output Propagation Delay | - | - | - | 5.0 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GL}}$, Grid Turn On Propagation Delay | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}$ | - | - | 2.0 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GO}}$, Grid Turn Off Propagation Delay | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}$ | - | - | 5.0 | $\mu \mathrm{s}$ |
| TGR, Grid Rise Time | At rated load. Note 5 | 0.50 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GF}}$, Grid Fall Time | At rated load. Note 5 | 0.35 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {AR }}$, Anode Rise Time | At rated load. Note 5 | 0.40 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {AF }}$, Anode Fall Time | At rated load. Note 5 | 0.40 | - | 2.50 | $\mu \mathrm{s}$ |

4. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be $100 \%$ parametrically tested in production.
5. Grid and anode rise / fall times are measured from $10 \%$ and $90 \%$ points. Output currents are at the maximum rated currents for the respective stages.

## PACKAGE LEAD DESCRIPTION

| Package Lead Number | Lead Symbol |  |
| :---: | :---: | :---: |
| 40L DIP | (31 Anode Configuration) | Function |
| 1 | GRID1 | 50 mA grid output. |
| 2 | GRID2 | 50 mA grid output. |
| 3 | GRID3 | 50 mA grid output. |
| 4 | AN1 | 2.0 mA anode output. |
| 5 | AN2 | 2.0 mA anode output. |
| 6 | AN3 | 2.0 mA anode output. |
| 7 | AN4 | 2.0 mA anode output. |
| 8 | AN5 | 2.0 mA anode output. |
| 9 | AN6 | 2.0 mA anode output. |
| 10 | AN7 | 2.0 mA anode output. |
| 11 | AN8 | 2.0 mA anode output. |
| 12 | AN9 | 2.0 mA anode output. |
| 13 | AN10 | 2.0 mA anode output. |
| 14 | AN11 | 2.0 mA anode output. |
| 15 | AN12 | 2.0 mA anode output. |
| 16 | AN13 | 2.0 mA anode output. |
| 17 | AN14 | 2.0 mA anode output. |
| 18 | AN15 | 2.0 mA anode output. |
| 19 | AN16 | 2.0 mA anode output. |
| 20 | GND | Ground connection. |
| 21 | AN17 | 2.0 mA anode output. |
| 22 | AN18 | 2.0 mA anode output. |
| 23 | AN19 | 2.0 mA anode output. |
| 24 | AN20 | 2.0 mA anode output. |
| 25 | AN21 | 2.0 mA anode output. |
| 26 | AN22 | 2.0 mA anode output. |
| 27 | AN23 | 2.0 mA anode output. |
| 28 | AN24 | 20 mA anode output. |
| 29 | AN25 | 20 mA anode output. |
| 30 | AN26 | 20 mA anode output. |
| 31 | AN27 | 20 mA anode output. |
| 32 | AN28 | 20 mA anode output. |
| 33 | AN29 | 20 mA anode output. |
| 34 | AN30 | 2.0 mA anode output. |
| 35 | $\mathrm{D}_{\text {IN }}$ | Shift register data input. |
| 36 | CLK | Shift register clock input. |
| 37 | STB | Transfer contents of shift registers to output stages. |
| 38 | GREN | Grid outputs enable. |
| 39 | AN31 | 2.0 mA anode output. |
| 40 | $\mathrm{V}_{\mathrm{BB}}$ | Supply voltage input. |



Figure 2. Block Diagram

## OPERATION DESCRIPTION

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the $\mathrm{D}_{\text {IN }}$ pin at the rising edge of the CLK input. Thirty four bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the STB input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register/latch will cause the corresponding output to turn on. A logic low input to the shift register/latch will
cause the corresponding output to turn off. Please note that if the STB is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.
The three GRID outputs are gated by the GREN input. When GREN is low, the GRID outputs are forced low regardless of the state of the corresponding latch output. When GREN is high, the GRID outputs correspond to the state of their respective latch outputs. The anode outputs, AN1 to AN31 are always enabled.

## CS1088

## APPLICATION INFORMATION

Table 1. Bit Pattern, G = Grid, A = Anode.

| Bit \# | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin Name | G1 | G2 | G3 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 | A13 | A14 |


| Bit \# | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin Name | A15 | A16 | A17 | A18 | A19 | A20 | A21 | A22 | A23 | A24 | A25 | A26 | A27 | A28 | A29 | A30 | A31 |



* Selected grid goes high only if input bit pattern from shift register to grid is high.

Figure 3. Typical Operation

Unused grid and anode drivers should have their respective bits set to logic low in the data stream.

Multiple grid or anode drivers may be connected together, but must be programmed to the same logic state for proper
device operation. Maximum package power must be observed and care must be taken to maintian junction temperature below $+150^{\circ} \mathrm{C}$.

## MARKING DIAGRAMS



DIP-40 WIDE BODY N SUFFIX CASE 711

A =Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

PIN CONNECTIONS


## CS1089

## Vacuum Fluorescent Display Tube Driver

The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 32-bit shift register, a 32-bit transparent data latch, a metal mask ROM, six 20 mA anode output drivers, twenty-three 2 mA anode output drivers, and three 50 mA grid drivers with output enables.

## Features

- Power On Reset
- Display Dimming Possible
- Three, 50 mA Grid Drivers
- Anodes:
- 6 @ 20 mA
- 23 @ 2 mA


Figure 1. Application Diagram


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DIP-40
WIDE BODY N SUFFIX CASE 711


PLCC-44
FN SUFFIX
CASE 777

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS1089XN40 | DIP-40 <br> WIDE BODY | 9 Units/Rail |
| CS1089XFN44 | PLCC-44 | 23 Units/Rail |
| CS1089XFNR44 | PLCC-44 | 500 Tape \& Reel |

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2877 of this data sheet.

## MAXIMUM RATINGS*

| Parameter |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{BB}}$ ) |  | -0.6 to +18 | V |
| Input Voltages ( $\mathrm{D}_{\text {IN }}, \mathrm{CLK}$, STB, GREN) |  | -0.6 to +6.0 | V |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| ESD Susceptibility (Machine Model) |  | 200 | V |
| ```Package Thermal Resistance, DIP-40 Junction-to-Case, R өJc Junction-to-Ambient, R RJJA``` |  | $\begin{aligned} & 20 \\ & 45 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{w} \end{aligned}$ |
| Package Thermal Resistance, PLCC-44 Junction-to-Case, R ®Jc Junction-to-Ambient, $\mathrm{R}_{\theta \mathrm{JA}}$ |  | $\begin{aligned} & 16 \\ & 55 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{w} \end{aligned}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 Peak 230 Peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.
ELECTRICAL CHARACTERISTICS (8.0 V $\leq \mathrm{V}_{\mathrm{BB}} \leq 16.5 \mathrm{~V}$, Gnd $=0 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 105^{\circ} \mathrm{C}$; unless otherwise stated. Note 3.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $V_{B B}$ Input |  |  |  |  |  |
| $V_{B B}$ Input Voltage | - | 8.0 | - | 16.5 | V |
| $\mathrm{I}_{\mathrm{BB} 0}$ Current | No outputs active, $\mathrm{V}_{\mathrm{BB}}=16.5 \mathrm{~V}$ | - | 2.0 | 5.0 | mA |
| Reset Mode | All outputs forced low. | - | 6.5 | 7.5 | V |

$\mathrm{D}_{\text {IN }}$, CLK, STB Inputs

| $\mathrm{V}_{\mathrm{IL} 1}$, Input Low Voltage | - | - | - | 1.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{IH}}$, Input High Voltage | - | 3.3 | - | - | V |
| $\mathrm{I}_{\mathrm{IL}}$, Input Current | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}}$ | - | 7.5 | 20.0 | $\mu \mathrm{~A}$ |

## GREN Input

| $\mathrm{V}_{\mathrm{IL}}$, Input Low Voltage | - | - | - | 1.6 | V |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{\mathrm{IH}}$, Input High Voltage | - | 3.3 | - | - | V |
| $\mathrm{I}_{\mathrm{IH}}$, Input Pull-down Current | $\mathrm{V}_{\mathrm{IN}}=3.325 \mathrm{~V}$ | - | 30 | 60 | $\mu \mathrm{~A}$ |

GRID1, GRID2, GRID3 Outputs

| $\mathrm{I}_{\mathrm{OL}}$ | Sink Current | 1.0 | - | - | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 50 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | $\mathrm{I}_{\text {OUT }}=-50 \mathrm{~mA}, \mathrm{~V}_{\mathrm{BB}}=12 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{BB}}-0.75$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

## AN24 - AN29 Outputs

| $\mathrm{I}_{\mathrm{OL}}$ | Sink Current | 400 | - | - | $\mu \mathrm{A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 20 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{l}_{\text {OUT }}=400 \mu \mathrm{~A}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | $\mathrm{I}_{\text {OUT }}=-20 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{BB}}-0.5$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

3. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be $100 \%$ parametrically tested in production.

ELECTRICAL CHARACTERISTICS (continued) ( $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}} \leq 16.5 \mathrm{~V}$, Gnd $=0 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 105^{\circ} \mathrm{C}$; unless otherwise stated. Note 4.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| AN1 - AN23 Outputs |  |  |  |  |  |
| IOL | Sink Current | 100 | - | - | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 2.0 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | lout $=100 \mu \mathrm{~A}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OG}}$ | lout $=-2.0 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{BB}}-0.5$ | - | $\mathrm{V}_{\mathrm{BB}}$ | V |

Dout Output

| $\mathrm{I}_{\mathrm{OL}}$ | Sink Current | 1.0 | - | - | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{OH}}$ | Source Current | 1.0 | - | - | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{l}_{\text {OUT }}=1.0 \mathrm{~mA}$ | - | - | 0.5 | V |
| $\mathrm{~V}_{\mathrm{OH}}$ | lout $=-1.0 \mathrm{~mA}$ | 3.9 | - | 5.1 | V |

AC Characteristics: Input and Output Timing

| $\mathrm{F}_{\mathrm{C}}$, CLK Frequency | - | 0 | - | 1.0 | MHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TCL, CLK Low Time | - | 200 | - | - | ns |
| $\mathrm{T}_{\text {CH }}$, CLK High Time | - | 200 | - | - | ns |
| $\mathrm{T}_{\text {CR }}$, CLK Rise Time | - | - | - | 100 | ns |
| TCF, CLK Fall Time | - | - | - | 100 | ns |
| TCD, CLK Low to Dout Propagation Delay | - | - | - | 200 | ns |
| TSC, STB Low to CLK High Time | - | 50 | - | - | ns |
| $\mathrm{T}_{\text {ST }}$, STB High Time | - | 500 | - | - | ns |
| TAN , STB High to Anode Output Propagation Delay | - | - | - | 5.0 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GL}}$, Grid Turn On Propagation Delay | $V_{B B}=12 \mathrm{~V}$ | - | - | 2.0 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GO}}$, Grid Turn Off Propagation Delay | $\mathrm{V}_{\mathrm{BB}}=12 \mathrm{~V}$ | - | - | 5.0 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{GR}}$, Grid Rise Time | At rated load. Note 5. | 0.50 | - | 2.00 | $\mu \mathrm{s}$ |
| T ${ }_{\text {GF }}$, Grid Fall Time | At rated load. Note 5. | 0.35 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {AR }}$, Anode Rise Time | At rated load. Note 5. | 0.40 | - | 2.00 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\text {AF }}$, Anode Fall Time | At rated load. Note 5. | 0.40 | - | 2.50 | $\mu \mathrm{s}$ |

4. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be $100 \%$ parametrically tested in production.
5. Grid and anode rise / fall times are measured from $10 \%$ and $90 \%$ points. Output currents are at the maximum rated currents for the respective stages.

## PACKAGE LEAD DESCRIPTION

| Package Lead Number |  | Lead Symbol | Function |
| :---: | :---: | :---: | :---: |
| 40L DIP | 44L PLCC | (29 Anode Configuration) |  |
| 1 | 14 | GRID1 | 50 mA grid output. |
| 2 | 15 | GRID2 | 50 mA grid output. |
| 3 | 16 | GRID3 | 50 mA grid output. |
| 4 | 17 | AN1 | 2.0 mA anode output. |
| 5 | 18 | AN2 | 2.0 mA anode output. |
| 6 | 19 | AN3 | 2.0 mA anode output. |
| 7 | 20 | AN4 | 2.0 mA anode output. |
| 8 | 21 | AN5 | 2.0 mA anode output. |
| 9 | 22 | AN6 | 2.0 mA anode output. |
| 10 | 24 | AN7 | 2.0 mA anode output. |
| 11 | 25 | AN8 | 2.0 mA anode output. |
| 12 | 26 | AN9 | 2.0 mA anode output. |
| 13 | 27 | AN10 | 2.0 mA anode output. |
| 14 | 28 | AN11 | 2.0 mA anode output. |
| 15 | 29 | AN12 | 2.0 mA anode output. |
| 16 | 30 | AN13 | 2.0 mA anode output. |
| 17 | 31 | AN14 | 2.0 mA anode output. |
| 18 | 32 | AN15 | 2.0 mA anode output. |
| 19 | 33 | AN16 | 2.0 mA anode output. |
| 20 | 35 | GND | Ground connection. |
| 21 | 36 | AN17 | 2.0 mA anode output. |
| 22 | 37 | AN18 | 2.0 mA anode output. |
| 23 | 38 | AN19 | 2.0 mA anode output. |
| 24 | 39 | AN20 | 2.0 mA anode output. |
| 25 | 40 | AN21 | 2.0 mA anode output. |
| 26 | 41 | AN22 | 2.0 mA anode output. |
| 27 | 42 | AN23 | 2.0 mA anode output. |
| 28 | 43 | AN24 | 20 mA anode output. |
| 29 | 44 | AN25 | 20 mA anode output. |
| 30 | 2 | AN26 | 20 mA anode output. |
| 31 | 3 | AN27 | 20 mA anode output. |
| 32 | 4 | AN28 | 20 mA anode output. |
| 33 | 5 | AN29 | 20 mA anode output. |
| 34 | 6 | Dout | Shift register data output. |
| 35 | 7 | $\mathrm{D}_{\mathrm{IN}}$ | Shift register data input. |
| 36 | 8 | CLK | Shift register clock input. |
| 37 | 9 | STB | Transfer contents of shift registers to output stages. |
| 38 | 10 | GREN | Grid outputs enable. |
| 39 | 1, 11, 12, 23, 34 | NC | No connection. |
| 40 | 13 | $V_{B B}$ | Supply voltage input. |



Figure 2. Block Diagram

## OPERATION DESCRIPTION

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the $\mathrm{D}_{\text {IN }}$ pin at the rising edge of the CLK input. Thirty two bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the STB input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register/latch will cause the corresponding output to turn on. A logic low input to the shift register/latch will cause the corresponding output to turn off. Please note that if the STB is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.

The three GRID outputs are gated by the GREN input. When GREN is low, the GRID outputs are forced low regardless of the state of the corresponding latch output. When GREN is high, the GRID outputs correspond to the state of their respective latch outputs. The anode outputs, AN1 to AN29 are always enabled.

The $D_{\text {OUT }}$ pin is the output of the last stage of the shift register to allow serial cascading of this IC with other devices. Data from the last stage of the shift register is supplied to the $D_{\text {OUT }}$ pin delayed by $1 / 2$ CLK cycle. Data on the $\mathrm{D}_{\text {OUT }}$ output changes with the falling edges of the CLK to prevent logic race conditions between the CLK and the $\mathrm{D}_{\text {IN }}$ of the next IC in the serial chain.

## CS1089

## APPLICATION INFORMATION

Table 1. Bit Pattern, G = Grid, A = Anode.

| Bit \# | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Pin Name | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 |
| Bit \# | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Pin Name | A23 | A22 | A21 | A20 | A19 | A18 | A17 | G3 | A24 | A25 | A26 | A27 | A28 | A29 | G1 | G2 |



* Selected grid goes high only if input bit pattern from shift register to grid is high.

Figure 3. Typical Operation

Unused grid and anode drivers should have their respective bits set to logic low in the data stream.

Multiple grid or anode drivers may be connected together, but must be programmed to the same logic state for proper device operation. Maximum package power must be observed and care must be taken to maintian junction temperature below $+150^{\circ} \mathrm{C}$.

Care must be taken when interfacing this part to a microprocessor. The $\mathrm{D}_{\mathrm{OUT}}$ output $\mathrm{V}_{\mathrm{OH}}$ is specified at 3.9 V
to 5.1 V at an $\mathrm{I}_{\mathrm{OUT}}$ of -1.0 mA . Lower current loads will result in a higher output voltage. $\mathrm{V}_{\mathrm{OH}}=5.2 \mathrm{~V}$ (typ) with no load. $\mathrm{V}_{\mathrm{OH}}=5.7 \mathrm{~V}$ (max) with no load. Protection or workarounds for the device may be needed at the application level. No protection is needed when interfacing with other parts in this family (CS1087, CS1088, or CS1089).

MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
$\mathrm{YY}, \mathrm{Y} \quad=$ Year
WW, W = Work Week

PIN CONNECTIONS


## CS8312

## IGBT Ignition Predriver with Dynamic Current Regulation

The CS8312 is a bipolar microprocessor interface IC designed to drive an IGBT (or logic level MOSFETs) powering large inductive loads in harsh operating environments. The IC's dynamic current limit function lets the microprocessor adjust the current limit threshold to the real time needs of the system.

CLI, the current limit input, sets the current limit for the IGBT high or low as directed by the system microprocessor. CLI also raises and lowers the threshold on the diagnostic FLAG output signal. The FLAG output signals the microprocessor when the current level approaches current limit on the IGBT. The CTRL input enables the FLAG function.

## Features

- $\mu \mathrm{P}$ Compatible Inputs
- Adjustable Current Limit Thresholds
- External Sense Resistor
- Flag Signal to Indicate Output Status


Figure 1. Block Diagram


ON Semiconductor ${ }^{\text {w }}$

## http://onsemi.com



PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8312YN8 | DIP-8 | 50 Units/Rail |
| CS8312YD8 | SO-8 | 95 Units/Rail |
| CS8312YDR8 | SO-8 | 2500 Tape \& Reel |

## ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage |  | -0.3 to 12 | V |
| Digital Input Currents |  | 2.0 | mA |
| Internal Power Dissipation ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) |  | 700 | mW |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +165 | ${ }^{\circ} \mathrm{C}$ |
| Electrostatic Discharge (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering | Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2 | 260 peak 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 10 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}\right.$,
$-0.2 \mathrm{~V} \leq$ Differential Ground Voltage $\leq 0.8 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

General

| Power Supply Including Ripple Voltage | - | 7.0 | - | 10 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Ripple Frequency | - | 10 | - | 60 | kHz |
| Differential Ground Frequency | - | 10 | - | 60 | kHz |
| Quiescent Current, $\mathrm{I}_{\mathrm{Q}}$ Turn On Turn Off | $\begin{aligned} & \mathrm{V}_{\text {CTRL }}=5.5 \mathrm{~V} \\ & \mathrm{~V}_{\text {CTRL }}=-0.3 \mathrm{~V} \end{aligned}$ | - | - | $\begin{aligned} & 15 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Supply Voltage Rejection | $\mathrm{V}_{\text {CTRL }}=5.5 \mathrm{~V}$ | 30 | - | - | dB |
| Differential Ground Rejection Ratio | $\mathrm{V}_{\text {CTRL }}=5.5 \mathrm{~V}$ | 30 | - | - | dB |
| Differential Ground Current Ratio | $\begin{aligned} & \mathrm{V}_{\text {CTRL }}=-0.3 \mathrm{~V}, \\ & \left(\mathrm{~V}_{\text {SENSE- }}-\mathrm{V}_{\text {GND }}\right) \mathrm{DC}=1.0 \mathrm{~V} \\ & \left(\mathrm{~V}_{\text {SENSE }}-\mathrm{V}_{\mathrm{GND}}\right) \mathrm{AC}=0.6 \mathrm{~V} \end{aligned}$ | - | - | 3.0 | mA |
| Unity Gain Bandwidth | $\mathrm{V}_{\text {CTRL }}=5.5 \mathrm{~V}$ | 400 | - | - | kHz |
| Turn On Delay | CTRL Increasing | - | - | 30 | $\mu \mathrm{s}$ |
| Turn Off Delay | CTRL Decreasing | - | - | 30 | $\mu \mathrm{s}$ |

## Control Function

| Input Voltage Range | ICTRL $=2.0 \mathrm{~mA}$ | -0.3 | - | 5.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Threshold |  |  |  |  |  |
| Turn On | CTRL Increasing | - | - | 3.5 | V |
| Turn Off | CTRL Decreasing | 1.5 | - | - | V |
| Hysteresis |  | 0.4 | - | 2.0 | V |
| Voltage | ICTRL $=10 \mu \mathrm{~A}$ max | - | - | 1.1 | V |
| Input Capacitance | - | - | - | 50 | pF |

## Current Limit Increase Function

| Input Voltage Range | $\mathrm{I}_{\text {CTRL }}=2.0 \mathrm{~mA}$ | -0.3 | - | 5.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Threshold |  |  |  |  |  |
| Turn On | CLI Increasing | - | - | 3.5 | V |
| Turn Off | CLI Decreasing | 1.5 | - | - | V |
| Hysteresis |  | 0.4 | - | 2.0 | V |
| Voltage | $\mathrm{I}_{\text {CLI }}=10 \mu \mathrm{Amax}$ | - | - | 1.1 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 10 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}\right.$,
$-0.2 \mathrm{~V} \leq$ Differential Ground Voltage $\leq 0.8 \mathrm{~V}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Current Limit Increase Function (continued)

| Input Capacitance | - | - | - | 50 | pF |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Stage |  |  |  |  |  |
| Iout | - | - | - | 5.0 | mA |
| Clamp Voltage | $\mathrm{V}_{\text {CTRL }}=5.5 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=1.0 \mathrm{~mA}$ | 4.0 | - | 5.5 | V |
| Output Off Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CTRL}}=-0.3 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=10 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CTRL}}=-0.3 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=200 \mu \mathrm{~A} \end{aligned}$ |  | - | $\begin{aligned} & 0.5 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |

## Flag Function

| Output Low | $\mathrm{V}_{\text {CTRL }}=5.5 \mathrm{~V}, \mathrm{I}_{\text {FLAG }}=1.5 \mathrm{~mA}$ | - | - | 0.9 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Leakage Current | $\mathrm{V}_{\text {CTRL }}=-0.3 \mathrm{~V}$ | - | - | 10 | $\mu \mathrm{A}$ |
| Output Capacitance | - | - | - | 50 | pF |
| Turn On ( $\left.\mathrm{V}_{\text {SENSE+ }}-\mathrm{V}_{\text {SENSE- }}\right)$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CTRL}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CLI}}=-0.3 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CTRL}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CLI}}=5.5 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 210 \\ & 300 \end{aligned}$ | $225$ | $\begin{aligned} & 240 \\ & 350 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Turn Off Delay | CTRL Decreasing | - | - | 10 | $\mu \mathrm{s}$ |
| Turn On Delay | - | - | - | 10 | $\mu \mathrm{s}$ |
| Disable Time | - | 100 | - | 450 | $\mu \mathrm{s}$ |

Sense Function

| Input Voltage Range | - | -0.3 | - | 2.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Sense Regulation Voltage | $\mathrm{V}_{\mathrm{CTRL}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CLI}}=-0.3 \mathrm{~V}$ | 270 | 295 | 320 | mV |
|  | $\mathrm{V}_{\mathrm{CTRL}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{CLI}}=5.5 \mathrm{~V}$ | 380 | 410 | 440 | mV |
| Input Leakage Current | $\mathrm{V}_{\mathrm{CTRL}}=5.5 \mathrm{~V}$ | - | - | 5.0 | $\mu \mathrm{~A}$ |
| Propagation Delay | $\mathrm{V}_{\mathrm{CTRL}}=5.5 \mathrm{~V}$ | - | - | 20 | $\mu \mathrm{~s}$ |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  | FIN SYMBOL |  |
| :---: | :---: | :---: | :--- |
| DIP-8 | SO-8 |  | Indicates whether current through the IGBT has reached a pre- <br> set level. |
| 1 | 1 | SENSE + | Positive input to current comparator. |
| 2 | 2 | SENSE- | Ground (SENSE-) for current sense resistor. |
| 3 | 3 | GND | Ground connection. |
| 4 | 4 | OUT | Output voltage to IGBT (MOSFET) gate. |
| 5 | 5 | CLI | Current limit input increase. |
| 6 | 6 | CTRL | Control input. |
| 7 | 7 | VCC |  |
| 8 | 8 | Supply voltage. |  |

## CIRCUIT DESCRIPTION

## Flag Function (See Figure 2)

The flag indicates when the voltage across the two sense pins is approaching a current limit level that has been determined by the value of the external sense resistor ( $\mathrm{R}_{\text {SENSE }}$ ) and the state of the CTRL and CLI pins. If the voltage across the sense pins (SENSE+, SENSE-) is less than the flag turn-on voltage, then the FLAG is off. When the voltage between the sense pins equals the FLAG turn on voltage, the FLAG will latch on until the CTRL pin goes low. FLAG is disabled whenever CTRL is low. Changing the CLI pin from low to high will increase nominal FLAG turn on voltage by approximately $45 \%$.

Table 1. FLAG Timing Sequence

| State | CONTROL | SENSE $_{+}$ | FLAG |
| :---: | :---: | :---: | :---: |
| 0 | Low | $X$ | OFF |
| 1 | High | Below Threshold | OFF |
| 2 | High | Above Threshold | ON |
| 3 | High | $X$ | ON |
| 0 | Low | $X$ | OFF |

## Output Stage

The CS8312 output (OUT) saturates and supplies voltage to the IGBT (or MOSFET) gate once the CTRL switches from low to high. As current through the IGBT (MOSFET) increases and the voltage across the sense resistor passes the flag turn on voltage, the FLAG will turn on. If the current through the sense resistor continues to rise and the sense resistor voltage reaches the regulation sense voltage, then the gate voltage will fall to a level that regulates the driver and maintains the regulation sense voltage at the sense resistor.

## Current Limit Function

Changing the CLI pin from a logic low to a logic high increases the FLAG turn on voltage by approximately 45\% and the regulation sense voltage by approximately $39 \%$ respectively.


Figure 2. Application and Test Diagram

PACKAGE THERMAL DATA

| Parameter |  | DIP-8 | SO-8 | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 52 | 45 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 100 | 165 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS7054

## Low Side PWM FET Controller

The CS7054 is a monolithic integrated circuit designed primarily to control the rotor speed of permanent magnet, direct current (DC) brush motors. It drives the gate of an N channel power MOSFET or IGBT with a user-adjustable, fixed frequency, variable duty cycle, pulse width modulated (PWM) signal. The CS7054 can also be used to control other loads such as incandescent bulbs and solenoids. Inductive current from the motor or solenoid is recirculated through an external diode.

The CS7054 accepts a DC level input signal of 0 to 5.0 V to control the pulse width of the output signal. This signal can be generated by a potentiometer referenced to the on-chip 5.0 V linear regulator, or a filtered $0 \%$ to $100 \%$ PWM signal also referenced to the 5.0 V regulator.

The IC is placed in a sleep state by pulling the CTL lead below 0.5 V . In this mode everything on the chip is shut down except for the on-chip regulator and the overall current draw is less than $275 \mu \mathrm{~A}$. There are a number of on-chip diagnostics that look for potential failure modes and can disable the external power MOSFET.

## Features

- 200 mA Peak PWM Gate Drive Output
- Patented Voltage Compensation Circuit
- $100 \%$ Duty Cycle Capability
- $5.0 \mathrm{~V}, \pm 3.0 \%$ Linear Regulator
- Low Current Sleep Mode
- Overvoltage Protection
- Overcurrent Protection of External MOSFET/IGBT
- Output Inhibit

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> PIN CONNECTIONS AND MARKING DIAGRAMS


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS7054YN14 | DIP-14 | 25 Units/Rail |
| CS7054YDW16 | SO-16L | 46 Units/Rail |
| CS7054YDWR16 | SO-16L | 1000 Tape \& Reel |



Figure 1. Application Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Storage Temperature | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {CC }}$ | -0.3 to 30 | V |
| Supply Voltage Range (Load Dump $=26 \mathrm{~V}$ w/Series $51 \Omega$ Resistor) $\mathrm{VCC}_{\text {C }}$ Peak Transient Voltage | 40 | V |
| Input Voltage Range (at any input) | -0.3 to 10 | V |
| Maximum Junction Temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| Lead Temperature Soldering | Wave Solder (through hole styles only) Note 1 <br> Reflow (SMD styles only) Note 2 | 260 peak <br> 230 peak |
| ${ }^{\circ} \mathrm{C}$ |  |  |

1. 10 seconds max.
2. 60 seconds max above $183^{\circ} \mathrm{C}$
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}}<16 \mathrm{~V} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | 

Control (CTL)

| Control Input Current | CTL = 0 V to 5.0 V | -2.0 | 0.1 | 2.0 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Sleep Mode Threshold | - | 8.0 | 10 | 12 | $\% \mathrm{~V}_{\text {REG }}$ |
| Sleep Mode Hysteresis | - | 50 | 100 | 150 | mV |

Current Sense

| Differential Voltage Sense | $\mathrm{I}_{\mathrm{ADJ}}=51.2 \% \mathrm{~V}_{\mathrm{REG}}$ and $\mathrm{R}_{\mathrm{CS} 1}=51 \Omega$ | 60.5 | - | 79.5 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{ADJ}}$ Input Current | $\mathrm{I}_{\mathrm{ADJ}}=0 \mathrm{~V}$ to 5.0 V | -5.0 | 0.3 | 2.0 | $\mu \mathrm{~A}$ |

Linear Regulator

| Output Voltage | $\mathrm{V}_{\mathrm{CC}}=13.2 \mathrm{~V}$ | 4.85 | 5.00 | 5.15 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

Inhibit

| Inhibit Threshold | - | 40 | 50 | 60 | $\% V_{\text {REG }}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Inhibit Hysteresis | - | 150 | 325 | 575 | mV |

## External Drive (OUTPUT)

| Output Frequency | $\mathrm{R}_{\mathrm{OSC}}=105 \mathrm{k} \Omega, \mathrm{C}, \mathrm{OSC}=390 \mathrm{pF}$ | 17 | 20 | 23 | kHz |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Voltage to Duty Cycle Conversion | $\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=30 \% \mathrm{~V}_{\mathrm{REG}}$ | 26.3 | - | 38.5 | $\%$ |
|  | $\mathrm{~V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=70 \% \mathrm{~V}_{\mathrm{REG}}$ | - | 81.5 | $\%$ |  |
| Output Rise Time | $\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\mathrm{GATE}}=5.0 \mathrm{nF}$ | - | 0.25 | 1.0 | $\mu \mathrm{~s}$ |
| Output Fall Time | $\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\mathrm{GATE}}=5.0 \mathrm{nF}$ | - | 0.3 | 1.0 | $\mu \mathrm{~s}$ |
| Output Sink Current | $\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\mathrm{GATE}}=5.0 \mathrm{nF}$ | - | 400 | - | mA |
| Output Source Current | $\mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\mathrm{GATE}}=5.0 \mathrm{nF}$ | - | 400 | - | mA |
| Output High Voltage | $\mathrm{l}_{\mathrm{OUT}}=1.0 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{CC}}-1.7$ | - | - | V |
| Output Low Voltage | lout $=-1.0 \mathrm{~mA}$ | - | - | 1.3 | V |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| DIP-14 | SO-16L |  |  |
| 1 | 1 | OUTPUT | MOSFET Gate Drive. |
| 2 | 2 | GND | Ground. |
| 3 | 3 | FLT | Fault time out capacitor. |
| 4 | 4 | Cosc | Oscillator capacitor. |
| 5 | 5 | ROSC | Oscillator resistor. |
| 6 | 6 | CTL | Pulse width control input. |
| 7 | 7, 8, 15 | NC | No connection. |
| 8 | 9 | $\mathrm{V}_{\text {REG }}$ | 5.0 V linear regulator. |
| 9 | 10 | ISENSE- | Current sense minus. |
| 10 | 11 | $\mathrm{I}_{\text {SENSE }+}$ | Current sense plus. |
| 11 | 12 | $\mathrm{I}_{\text {ADJ }}$ | Current limit adjust. |
| 12 | 13 | INH | Output Inhibit. |
| 13 | 14 | PGND | Power ground for on chip clamp. |
| 14 | 16 | $\mathrm{V}_{\mathrm{CC}}$ | Positive power supply input. |



Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. $\mathrm{V}_{\text {REG }}$ vs. Temperature @ $\mathrm{V}_{\mathrm{CC}}=8.0 \mathrm{~V}$


Figure 5. $\mathrm{V}_{\text {REG }}$ vs. Temperature $@ \mathrm{~V}_{\mathrm{CC}}=16 \mathrm{~V}$


Figure 4. $\mathrm{V}_{\mathrm{REG}}$ vs. Temperature $@ \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$


Figure 6. OUTPUT Saturation Voltage (Sourcing Current) vs Temperature


Figure 7. OUTPUT Voltage (Sinking Current) vs Temperature

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## Oscillator

The IC sets up a constant frequency triangle wave at the Cosc lead whose frequency is determined by the external components $\mathrm{R}_{\mathrm{OSC}}$ and $\mathrm{C}_{\mathrm{OSC}}$ by the following equation:

$$
\text { Frequency }=\frac{0.83}{\text { ROSC } \times \operatorname{COSC}}
$$

The peak and valley of the triangle wave are proportional to $\mathrm{V}_{\mathrm{CC}}$ by the following:

$$
\begin{aligned}
& \text { VALLEY }=0.2 \times V_{C C} \\
& V_{\text {PEAK }}=0.8 \times V_{C C}
\end{aligned}
$$

This is required to make the voltage compensation function properly. In order to keep the frequency of the oscillator constant the current that charges CosC must also vary with supply. $\mathrm{R}_{\mathrm{OSC}}$ sets up the current which charges COSC. The voltage across $\mathrm{R}_{\mathrm{OSC}}$ is $50 \%$ of $\mathrm{V}_{\mathrm{CC}}$ and therefore:

$$
\mathrm{I} \mathrm{ROSC}=0.5 \times \frac{\mathrm{VCC}}{\mathrm{ROSC}}
$$

$\mathrm{I}_{\text {ROSC }}$ is multiplied by two (2) internally and transferred to the C OSC lead. Therefore:

$$
\mathrm{I} \operatorname{cosc}= \pm \frac{\mathrm{V}_{\mathrm{CC}}}{\mathrm{ROSC}_{\mathrm{OSC}}}
$$

The period of the oscillator is:

$$
\mathrm{T}=2 \mathrm{COSC} \times \frac{\mathrm{VPEAK}-\mathrm{VVALLEY}}{\mathrm{I} \operatorname{COSC}}
$$

The $\mathrm{R}_{\text {OSC }}$ and COSC components can be varied to create frequencies over the range of 15 Hz to 25 kHz . With the suggested values of $105 \mathrm{k} \Omega$ and 390 pF for $\mathrm{R}_{\mathrm{OSC}}$ and $\mathrm{C}_{\mathrm{OSC}}$ respectively, the nominal frequency will be approximately 20 kHz . $\mathrm{I}_{\mathrm{ROSC}}$, at $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}$, will be $66.7 \mu \mathrm{~A}$. $\mathrm{I}_{\mathrm{ROSC}}$ should not change over a more than $2: 1$ ratio and therefore C OSC should be changed to adjust the oscillator frequency.

## Voltage Duty Cycle Conversion

The IC translates an input voltage at the CTL lead into a duty cycle at the OUTPUT lead. The transfer function incorporates ON Semiconductor's patented Voltage Compensation method to keep the average voltage and current across the load constant regardless of fluctuations in the supply voltage. The duty cycle is varied based upon the input voltage and supply voltage by the following equation:

$$
\text { Duty Cycle }=100 \% \times \frac{2.8 \times \mathrm{V}_{\mathrm{CTL}}}{\mathrm{~V}_{\mathrm{CC}}}
$$

An internal DC voltage equal to:

$$
V_{D C}=\left(1.683 \times V_{C T L}\right)+V_{V A L L E Y}
$$

is compared to the oscillator voltage to produce the compensated duty cycle. The transfer is set up so that at $\mathrm{V}_{\mathrm{CC}}$ $=14 \mathrm{~V}$ the duty will equal $\mathrm{V}_{\mathrm{CTL}}$ divided by $\mathrm{V}_{\text {REG }}$. For
example at $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}, \mathrm{~V}_{\mathrm{REG}}=5.0 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{CTL}}=2.5 \mathrm{~V}$, the duty cycle would be $50 \%$ at the output. This would place a 7.0 V average voltage across the load. If $\mathrm{V}_{\mathrm{CC}}$ then drops to 10 V , the IC would change the duty cycle to $70 \%$ and hence keep the average load voltage at 7.0 V .


Figure 8. Voltage Compensation

### 5.0 V Linear Regulator

There is a $5.0 \mathrm{~V}, 5.0 \mathrm{~mA}$ linear regulator available at the $\mathrm{V}_{\mathrm{REG}}$ lead for external use. This voltage acts as a reference for many internal and external functions. It has a drop out of approximately 1.5 V at room temperature and does not require an external capacitor for stability.

## Current Sense and Timer

The IC differentially monitors the load current on a cycle by cycle basis at the $I_{\text {SENSE }+}$ and $\mathrm{I}_{\text {SENSE- }}$ leads. The differential voltage across these two leads is amplified internally and compared to the voltage at the $\mathrm{I}_{\mathrm{ADJ}}$ lead. The gain, $\mathrm{A}_{\mathrm{V}}$, is set internally and externally by the following equation:

$$
A V=\frac{V_{I(A D J)}}{\text { ISENSE }+-I_{\text {SENSE }-}}=\frac{37000}{1000+\mathrm{R}_{\mathrm{CS}}}
$$

The current limit ( $\mathrm{I}_{\mathrm{LIM}}$ ) is set by the external current sense resistor ( $\mathrm{R}_{\text {SENSE }}$ ) placed across the $\mathrm{I}_{\text {SENSE }}$ and $\mathrm{I}_{\text {SENSE- }}$ terminals and the voltage at the $\mathrm{I}_{\mathrm{ADJ}}$ lead.

$$
\operatorname{ILIM}=\frac{1000+\mathrm{R}_{\mathrm{CS}}}{37000} \times \frac{\mathrm{V}_{\mathrm{I}}(\mathrm{ADJ})}{\mathrm{RSENSE}^{2}}
$$

The $\mathrm{R}_{\mathrm{CS}}$ resistors and $\mathrm{C}_{\mathrm{CS}}$ components form a differential low pass filter which filters out high frequency noise generated by the switching of the external MOSFET and the associated lead noise. $\mathrm{R}_{\mathrm{CS}}$ also forms an error term in the gain of the $\mathrm{I}_{\text {LIM }}$ equation because the $\mathrm{I}_{\text {SENSE }}$ and $\mathrm{I}_{\text {SENSE- }}$ leads are low impedance inputs thereby creating a good current sensing amplifier. Both leads source $50 \mu \mathrm{~A}$ while the chip is in run mode. $\mathrm{R}_{\mathrm{CS}}$ should be much less than $1000 \Omega$ to minimize error in the $\mathrm{I}_{\mathrm{LIM}}$ equation. $\mathrm{I}_{\mathrm{ADJ}}$ should be biased between 1.0 V and 4.0 V .

When the current through the external MOSFET exceeds $\mathrm{I}_{\text {LIM, }}$, an internal latch is set and the output pulls the gate of the MOSFET low for the remainder of the oscillator cycle (fault mode). At the start of the next cycle, the latch is reset and the IC reverts back to run mode until another fault occurs. If a number of faults occur in a given period of time, the IC "times out" and disables the MOSFET for a long period of time to let it cool off. This is accomplished by charging the C CLT capacitor each time an over current condition occurs. If a cycle goes by with no overcurrent fault occurring, an even smaller amount of charge will be removed from $\mathrm{C}_{\mathrm{FLT}}$. If enough faults occur together, eventually $\mathrm{C}_{\mathrm{FLT}}$ will charge up to 2.4 V and the fault latch will be set. The fault latch will not be reset until the $\mathrm{C}_{\mathrm{FLT}}$ discharges to 0.6 V . This action will continue indefinitely if the fault persists.

The off time and on time are set by the following:

$$
\begin{aligned}
& \text { Off Time }=C_{F L T} \times \frac{2.4 \mathrm{~V}-0.6 \mathrm{~V}}{4.5 \mu \mathrm{~A}} \\
& \text { On Time }=\mathrm{C}_{\mathrm{FLT}} \times \frac{2.4 \mathrm{~V}-0.6 \mathrm{~V}}{\mathrm{I}_{\mathrm{AVG}}}
\end{aligned}
$$

where:

$$
\begin{gathered}
\mathrm{I} \mathrm{AVG}=(295.5 \mu \mathrm{~A} \times \mathrm{DC})-[4.5 \mu \mathrm{~A} \times(1-\mathrm{DC})] \\
\mathrm{I} \mathrm{AVG}=(300 \mu \mathrm{~A} \times \mathrm{DC})-4.5 \mu \mathrm{~A} \\
\mathrm{DC}=\mathrm{PWM} \text { Duty Cycle }
\end{gathered}
$$

## Sleep State

This device will enter into a low current mode ( $<275 \mu \mathrm{~A}$ ) when CTL lead is brought to less than 0.5 V . All functions are disabled in this mode, except for the regulator.

## Inhibit

When the inhibit voltage is greater than 2.5 V the internal latch is set and the external MOSFET will be turned off for the remainder of the oscillator cycle. The latch is then reset at the start of the next cycle.

## Overvoltage Shutdown

The IC will disable the output during an overvoltage event. This is a real time fault event and does not set the
internal latch and therefore is independent of the oscillator timing (i.e. asynchronous). There is no undervoltage lockout. The device will shutdown gracefully once it runs out of headroom. This happens at the point when VREG falls out of regulation.

## Reverse Battery

The CS7054 will not survive a reverse battery condition. Therefore, a series diode is required between the battery and the $\mathrm{V}_{\mathrm{CC}}$ lead.

## Load Dump

$\mathrm{V}_{\mathrm{CC}}$ is internally clamped to 30 V . It is recommended that a $51 \Omega$ resistor, ( $\mathrm{R}_{\mathrm{S}}$ ) is placed in series with $\mathrm{V}_{\mathrm{CC}}$ to limit the current flow into the IC in the event of a 40 V peak transient condition.

## Using the CS7054 as a Frequency Converter

Figure 9 shows the CS7054 configured for use as a frequency converter. In the setup shown, a 150 Hz square wave from a microprocessor is converted to a 10 kHz square wave. The duty cycle of each waveform is identical. The amplitude of the input waveform is 5.0 V , but does not need to be. The input amplitude requirement just needs to be high enough to switch the external bipolar transistor. The 10 kHz oscillator frequency is setup per the oscillator section of this data sheet.

The external resistor divider composed of the 3.6 k and 6.2 k resistors supplies 5.0 V to the CTL pin when the input duty cycle is at $100 \%$. This also makes the output waveform 100\%.

The RC filter ( $1.0 \mathrm{M} \Omega$ and $0.1 \mu \mathrm{~F}$ ) sets up a pole at 1.6 Hz :

$$
\begin{aligned}
f & =\frac{1}{2 \pi R C}=\frac{1}{2 \pi\left[1 \mathrm{M} \Omega+\left(\frac{(6.2 \mathrm{k})(3.6 \mathrm{k})}{6.2 \mathrm{k}+3.6 \mathrm{k}}\right)\right](0.1 \mu \mathrm{~F})} \\
& =1.6 \mathrm{~Hz}
\end{aligned}
$$

In this case, the pole is 2 orders of magnitude below the input waveform. Care must be taken to provide the appropriate DC level on the control pin in addition to providing the required response time.
*Note the current limit feature of the CS7054 has been defeated by grounding the ISENSE+ and the $\mathrm{I}_{\text {SENSE- }}$ pins and connecting the $\mathrm{I}_{\mathrm{ADJ}}$ lead to $\mathrm{V}_{\text {REG }}$.


Figure 9. Frequency Converter

PACKAGE THERMAL DATA

| Parameter |  | DIP-14 | SO-16L | Unit |
| :--- | ---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 48 | 23 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 85 | 105 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS4124

## High Side PWM FET Controller

The CS4124 is a monolithic integrated circuit designed primarily to control the rotor speed of permanent magnet, direct current (DC) brush motors. It drives the gate of an N channel power MOSFET or IGBT with a user-adjustable, fixed frequency, variable duty cycle, pulse width modulated (PWM) signal. The CS4124 can also be used to control other loads such as incandescent bulbs and solenoids. Inductive current from the motor or solenoid is recirculated through an external diode.

The CS4124 accepts a DC level input signal of 0 to 5.0 V to control the pulse width of the output signal. This signal can be generated by a potentiometer referenced to the on-chip 5.0 V linear regulator, or a filtered $0 \%$ to $100 \%$ PWM signal also referenced to the 5.0 V regulator.

The IC is placed in a sleep state by pulling the CTL lead below 0.5 V . In this mode everything on the chip is shutdown except for the on-chip regulator and the overall current draw is less than $275 \mu \mathrm{~A}$. There are a number of on-chip diagnostics that look for potential failure modes and can disable the external power MOSFET.

## Features

- 150 mA Peak PWM Gate Drive Output
- Patented Voltage Compensation Circuit
- $100 \%$ Duty Cycle Capability
- $5.0 \mathrm{~V}, \pm 3.0 \%$ Linear Regulator
- Low Current Sleep Mode
- Overvoltage Protection
- Boost Mode Power Supply
- Output Inhibit

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http://onsemi.com


PIN CONNECTION AND MARKING DIAGRAM


ORDERING INFORMATION*

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS4124YN16 | DIP-16 | 25 Units/Rail |

* Contact your local sales representative for 16 -lead SOIC wide package.


Figure 1. Applications Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| Storage Temperature Range | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{CC}}$ | -0.3 to 30 | V |
| $\mathrm{V}_{\text {CC }}$ Peak Transient Voltage (load dump $=26 \mathrm{~V}$ w/ series $10 \Omega$ resistor) | 40 | V |
| Input Voltage Range (at any input) | -0.3 to 10 | V |
| Maximum Junction Temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering Wave Solder (through hole styles only) Note 1 | 260 peak | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |

1. 10 seconds max.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (4.0 $\mathrm{V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ Supply |  |  |  |  |  |
| Operating Current Supply | $\begin{aligned} & 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 18 \mathrm{v} \\ & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<7.0 \mathrm{~V}, 18 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V} \end{aligned}$ | $-$ | $5.0$ | $\begin{aligned} & 10 \\ & 15 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Quiescent Current | $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ | - | 170 | 275 | $\mu \mathrm{A}$ |
| Overvoltage Shutdown | - | 26.5 | - | 29 | V |

Control (CTL)

| Control Input Current | $\mathrm{CTL}=0 \mathrm{~V}$ to 5.0 V | -2.0 | 0.1 | 2.0 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Sleep Mode Threshold | - | $8.0 \%$ | $10 \%$ | $12 \%$ | $\mathrm{~V}_{\mathrm{REG}}$ |
| Sleep Mode Hysteresis | $7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}$ | 50 | 100 | 150 | mV |
|  | $4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<7.0 \mathrm{~V}$ | 10 | - | 150 | mV |

## Control Sense

| Differential Voltage Sense | $\begin{aligned} & 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 18 \mathrm{~V}: \\ & I_{\mathrm{ADJ}}=1.0 \mathrm{~V} \text { and } \mathrm{R}_{\mathrm{CS} 1}=51 \Omega \\ & I_{\mathrm{ADJ}}=4.0 \mathrm{~V} \text { and } \mathrm{R}_{\mathrm{CS} 1}=51 \Omega \\ & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<7.0 \mathrm{~V}: \\ & I_{\mathrm{ADJ}}=1.0 \mathrm{~V} \text { and } \mathrm{R}_{\mathrm{CS} 1}=51 \Omega \\ & 18 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}: \\ & I_{\mathrm{ADJ}}=1.0 \mathrm{~V} \text { and } \mathrm{R}_{\mathrm{CS} 1}=51 \Omega \\ & I_{\mathrm{ADJ}}=4.0 \mathrm{~V} \text { and } \mathrm{R}_{\mathrm{CS} 1}=51 \Omega \end{aligned}$ | $\begin{gathered} 18 \\ 104 \\ \\ 15 \\ \\ 15 \\ 102 \end{gathered}$ |  | $\begin{gathered} 34 \\ 125 \\ \\ 39 \\ \\ 39 \\ 130 \end{gathered}$ | mV <br> mV <br> mV <br> mV <br> mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {ADJ }}$ Input Current | $4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}, \mathrm{I}_{\text {ADJ }}=0 \mathrm{~V}$ to 5.0 V | -2.0 | 0.3 | 2.0 | $\mu \mathrm{A}$ |

## Linear Regulator

| Output Voltage, $\mathrm{V}_{\mathrm{REG}}$ | $\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}$ | 2.0 | - | - | V |
| :--- | :--- | :--- | :--- | :--- | :---: |
|  | $\mathrm{V}_{\mathrm{CC}}=13.2 \mathrm{~V}$ | 4.85 | - | 5.15 | V |
|  | $\mathrm{~V}_{\mathrm{CC}}=26 \mathrm{~V}$ | 4.85 | - | 5.20 | V |

Inhibit

| Inhibit Threshold | - | $40 \%$ | $50 \%$ | $60 \%$ | $\mathrm{~V}_{\text {REG }}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Inhibit Hysteresis | $4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 7.0 \mathrm{~V}$ | 100 | - | 500 | mV |
|  | $7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}$ | 150 | 325 | 500 | mV |

External Drive (OUTPUT)

| Output Frequency | $\begin{aligned} & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<7.0 \mathrm{~V}: \\ & \mathrm{R}_{\mathrm{OSC}}=93.1 \mathrm{k} \Omega, \mathrm{C}_{\mathrm{OSC}}=470 \mathrm{pF} \\ & 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 18 \mathrm{~V}: \\ & \mathrm{R}_{\mathrm{OSC}}=93.1 \mathrm{k} \Omega, \mathrm{C}_{\text {OSC }}=470 \mathrm{pF} \\ & 18 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}: \\ & \mathrm{R}_{\mathrm{OSC}}=93.1 \mathrm{k} \Omega, \mathrm{C}_{\text {OSC }}=470 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & 10 \\ & 17 \\ & 17 \end{aligned}$ | 20 20 | $\begin{aligned} & 25 \\ & 23 \\ & 25 \end{aligned}$ | $\begin{aligned} & \mathrm{kHz} \\ & \mathrm{kHz} \\ & \mathrm{kHz} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Voltage to Duty Cycle Conversion | $\begin{aligned} & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<7.0 \mathrm{~V}: \\ & \mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=1.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=2.0 \mathrm{~V} \\ & 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 18 \mathrm{~V}: \\ & \mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=30 \% \mathrm{~V}_{\mathrm{REG}} \\ & \mathrm{~V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=55.8 \% \mathrm{~V}_{\mathrm{REG}} \\ & 18 \mathrm{~V}<\mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}: \\ & \mathrm{V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=1.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=13 \mathrm{~V}, \mathrm{CTL}=3.5 \mathrm{~V} \end{aligned}$ | $\begin{gathered} 65 \\ 100 \\ \\ 28.3 \\ 56.0 \\ \\ 11.8 \\ 34.2 \end{gathered}$ |  | 75 - <br> 36.3 <br> 64.0 <br> 21.8 <br> 44.2 | \% <br> \% <br> \% <br> \% <br> \% <br> \% |
| Output Rise Time | $\begin{aligned} & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V} \text { : } \\ & \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\mathrm{GATE}}=5.0 \mathrm{nF} \end{aligned}$ | - | . 25 | 1.0 | $\mu \mathrm{s}$ |
| Output Fall Time | $\begin{aligned} & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}: \\ & \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\mathrm{GATE}}=5.0 \mathrm{nF} \end{aligned}$ | - | . 30 | 1.0 | $\mu \mathrm{s}$ |

ELECTRICAL CHARACTERISTICS (continued) (4.0 $\mathrm{V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V} ;-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

External Drive (OUTPUT) (continued)

| Output Sink Current | $\begin{aligned} & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<7.0 \mathrm{~V} \text { : } \\ & \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\text {GATE }}=5.0 \mathrm{nF} \\ & 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}: \\ & \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\text {GATE }}=5.0 \mathrm{nF} \end{aligned}$ |  | $\begin{aligned} & 150 \\ & 300 \end{aligned}$ |  | mA <br> mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Source Current | $\begin{aligned} & 4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}}<7.0 \mathrm{~V} \text { : } \\ & \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\mathrm{GATE}}=5.0 \mathrm{nF} \\ & 7.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 26 \mathrm{~V}: \\ & \mathrm{R}_{\mathrm{GATE}}=6.0 \Omega, \mathrm{C}_{\text {GATE }}=5.0 \mathrm{nF} \end{aligned}$ |  | $\begin{aligned} & 150 \\ & 300 \end{aligned}$ | - | mA <br> mA |
| Output High Voltage | IOUT $=1.0 \mathrm{~mA}$ | $\mathrm{V}_{\text {BOOST }}=1.7$ | - | - | V |
| Output Low Voltage | I ${ }_{\text {OUT }}=-1.0 \mathrm{~mA}$ | - | - | 1.3 | V |

Charge Pump (DRV)

| Boost Voltage | - | $V_{C C}+6.4$ | - | - | $V$ |
| :--- | :---: | :---: | :---: | :---: | :---: |

## PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 16 Lead PDIP | PIN SYMBOL | FUNCTION |
| 1 | OUTPUT | MOSFET gate drive. |
| 2 | BOOST | Boost voltage. |
| 3 | FLT | Fault time out capacitor. |
| 4 | Rosc | Oscillator resistor. |
| 5 | Cosc | Oscillator capacitor. |
| 6 | CTL | Pulse width control input. |
| 7 | PGND | Power ground for on chip clamp. |
| 8 | $\mathrm{V}_{\text {CC }}$ | Positive power supply input. |
| 9 | $\mathrm{V}_{\text {REG }}$ | 5.0 V linear regulator. |
| 10 | SNI | Sense inductor current. |
| 11 | PMP | Collector of boost power transistor. |
| 12 | ISENSE- | Current sense minus. |
| 13 | ISENSE+ | Current sense plus. |
| 14 | $\mathrm{I}_{\text {ADj }}$ | Current limit adjust. |
| 15 | INH | Output Inhibit. |
| 16 | GND | Ground. |



Figure 2. Block Diagram

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. $\mathrm{V}_{\text {REG }}$ vs. Temperature @ $\mathrm{I}_{\text {LOAD }}=5.0 \mathrm{~mA}$


Figure 5. OUTPUT Voltage (Sinking Current) vs. Temperature


Figure 4. $\mathrm{V}_{\text {REG }}$ vs. Temperature $@ \mathrm{~V}_{\mathrm{CC}}=4.0 \mathrm{~V}$


Figure 6. OUTPUT Saturation Voltage (Sourcing Current) vs. Temperature

## APPLICATIONS INFORMATION

## THEORY OF OPERATION

## Oscillator

The IC sets up a constant frequency triangle wave at the Cosc lead whose frequency is related to the external components $\mathrm{R}_{\mathrm{OSC}}$ and $\mathrm{C}_{\mathrm{OSC}}$, by the following equation:

$$
\text { Frequency }=\frac{0.83}{\text { ROSC } \times \text { COSC }}
$$

The peak and valley of the triangle wave are proportional to $\mathrm{V}_{\mathrm{CC}}$ by the following:

$$
\begin{aligned}
& \text { VVALLEY }=0.1 \times V_{C C} \\
& V_{\text {PEAK }}=0.7 \times V_{C C}
\end{aligned}
$$

This is required to make the voltage compensation function properly. In order to keep the frequency of the oscillator constant the current that charges Cosc must also vary with supply. $\mathrm{R}_{\mathrm{OSC}}$ sets up the current which charges COSC. The voltage across $\mathrm{R}_{\mathrm{OSC}}$ is $50 \%$ of $\mathrm{V}_{\mathrm{CC}}$ and therefore:

$$
\mathrm{I} \mathrm{ROSC}=0.5 \times \frac{\mathrm{VCC}}{\mathrm{ROSC}}
$$

$\mathrm{I}_{\text {ROSC }}$ is multiplied by (2) internally and transferred to the Cosc lead. Therefore:

$$
\mathrm{I} \operatorname{cosc}= \pm \frac{\mathrm{VCC}_{\mathrm{CC}}}{\mathrm{ROSC}_{\mathrm{OS}}}
$$

The period of the oscillator is:

$$
\mathrm{T}=2 \mathrm{COSC} \times \frac{\mathrm{VPEAK}-\mathrm{V}_{\mathrm{VALLEY}}}{\mathrm{I} \operatorname{COSC}}
$$

The $\mathrm{R}_{\text {OSC }}$ and COSC components can be varied to create frequencies over the range of 15 Hz to 25 kHz . With the suggested values of $93.1 \mathrm{k} \Omega$ and 470 pF for $\mathrm{R}_{\mathrm{OSC}}$ and $\mathrm{C}_{\mathrm{OSC}}$, the nominal frequency will be approximately 20 kHz . $\mathrm{I}_{\text {ROSC }}$, at $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}$, will be $66.7 \mu \mathrm{~A}$. $\mathrm{I}_{\text {ROSC }}$ should not change over a more than $2: 1$ ratio and therefore $\mathrm{C}_{\text {OSC }}$ should be changed to adjust the oscillator frequency.

## Voltage Duty Cycle Conversion

The IC translates an input voltage at the CTL lead into a duty cycle at the OUTPUT lead. The transfer function incorporates ON Semiconductor's patented Voltage Compensation method to keep the average voltage and current across the load constant regardless of fluctuations in the supply voltage. The duty cycle is varied based upon the input voltage and supply voltage by the following equation:

$$
\text { Duty Cycle }=100 \% \times \frac{2.8 \times \mathrm{V}_{\mathrm{CTL}}}{\mathrm{~V}_{\mathrm{CC}}}
$$

An internal DC voltage equal to:

$$
V_{D C}=\left(1.683 \times V_{C T L}\right)+V_{V A L L E Y}
$$

is compared to the oscillator voltage to produce the compensated duty cycle. The transfer is set up so that when $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}$ the duty cycle will equal $\mathrm{V}_{\mathrm{CTL}}$ divided by $\mathrm{V}_{\mathrm{REG}}$. For example at $\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}, \mathrm{~V}_{\text {REG }}=5.0 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{CTL}}=2.5 \mathrm{~V}$,
the duty cycle would be $50 \%$ at the output. This would place a 7.0 V average voltage across the load. If $\mathrm{V}_{\mathrm{CC}}$ then drops to 10 V , the IC would change the duty cycle to $70 \%$ and hence keep the average load voltage at 7.0 V .


Figure 7. Voltage Compensation

### 5.0 V Linear Regulator

There is a $5.0 \mathrm{~V}, 5.0 \mathrm{~mA}$ linear regulator available at the $\mathrm{V}_{\mathrm{REG}}$ lead for external use. This voltage acts as a reference for many internal and external functions. It has a drop out of approximately 1.5 V at room temperature.

## Current Sense and Timer

The IC differentially monitors the load current on a cycle by cycle basis at the ISENSE+ and ISENSE- leads. The differential voltage across these two leads is amplified internally and compared to the voltage at the $\mathrm{I}_{\text {ADJ }}$ lead. The gain, $A_{V}$ is set internally and externally by the following equation:

$$
A V=\frac{\left.V_{I(A D J}\right)}{\text { ISENSE }+- \text { ISENSE }-}=\frac{37000}{1000+R_{C S}}
$$

The current limit ( $\mathrm{I}_{\mathrm{LIM}}$ ) is set by the external current sense resistor ( $\mathrm{R}_{\text {SENSE }}$ ) placed across the $\mathrm{I}_{\text {SENSE }}$ and $\mathrm{I}_{\text {SENSE- }}$ terminals and the voltage at the $\mathrm{I}_{\mathrm{ADJ}}$ lead.

$$
\mathrm{I} \mathrm{LIM}=\frac{1000+\mathrm{R}_{\mathrm{CS}}}{37000} \times \frac{\mathrm{V}_{\mathrm{I}}(\mathrm{ADJ})}{\mathrm{R}_{\text {SENSE }}}
$$

The $\mathrm{R}_{\mathrm{CS}}$ resistors and $\mathrm{C}_{\mathrm{CS}}$ components form a differential low pass filter which filters out high frequency noise generated by the switching of the external MOSFET and the associated lead noise. $\mathrm{R}_{\mathrm{CS}}$ also forms an error term in the gain of the $\mathrm{I}_{\text {LIM }}$ equation because the $\mathrm{I}_{\text {SENSE+ }}$ and $\mathrm{I}_{\text {SENSE- }}$ leads are low impedance inputs thereby creating a good current sensing amplifier. Both leads source $50 \mu \mathrm{~A}$ while the chip is in run mode. $\mathrm{I}_{\mathrm{ADJ}}$ should be biased between 1.0 V and 4.0 V. When the current through the external MOSFET exceeds $\mathrm{I}_{\mathrm{LIM}}$, an internal latch is set and the output pulls the gate of the MOSFET low for the remainder of the oscillator
cycle (fault mode). At the start of the next cycle, the latch is reset and the IC reverts back to run mode until another fault occurs. If a number of faults occur in a given period of time, the IC "times out" and disables the MOSFET for a long period of time to let it cool off. This is accomplished by charging the $\mathrm{C}_{\mathrm{FLT}}$ capacitor each time an over current condition occurs. If a cycle goes by with no overcurrent fault occurring, an even smaller amount of charge will be removed from $\mathrm{C}_{\text {FLT }}$. If enough faults occur together, eventually $\mathrm{C}_{\mathrm{FLT}}$ will charge up to 2.4 V and the fault latch will be set. The fault latch will not be reset until C $\mathrm{C}_{\text {FT }}$ discharges to 0.6 V . This action will continue indefinitely if the fault persists.

The off time and on time are set by the following:

$$
\begin{aligned}
& \text { Off Time }=\text { CFLT } \times \frac{2.4 \mathrm{~V}-0.6 \mathrm{~V}}{4.5 \mathrm{~A}} \\
& \text { On Time }=\text { CFLT } \times \frac{2.4 \mathrm{~V}-0.6 \mathrm{~V}}{\mathrm{I}_{\mathrm{AVG}}}
\end{aligned}
$$

where:

$$
\begin{gathered}
\mathrm{I} \mathrm{AVG}=(295.5 \mu \mathrm{~A} \times \mathrm{DC})-[4.5 \mu \mathrm{~A} \times(1-\mathrm{DC})] \\
\mathrm{I} \mathrm{AVG}=(300 \mu \mathrm{~A} \times \mathrm{DC})-4.5 \mu \mathrm{~A} \\
\mathrm{DC}=\text { PWM Duty Cycle }
\end{gathered}
$$

## Boost Switch Mode Power Supply

The CS4124 has an integrated boost mode power supply which charges the gate of the external high-side MOSFET to greater than 5.0 V above $\mathrm{V}_{\mathrm{CC}}$. Three leads are used for voltage boost. They are Boost, PMP and SNI. The PMP lead is the collector of a darlington tied NPN power transistor. This device charges the inductor during its on time. The boost lead is the input to chip from the external reservoir capacitor. The SNI lead is the emitter of the power NPN and is connected externally to the $\mathrm{R}_{\mathrm{SNI}}$ resistor.

The power supply is controlled by the oscillator. At the start of a cycle an R-S flip flop is set the internal power NPN transistor is turned on and energy begins to build up in the
inductor. The $\mathrm{R}_{\mathrm{SNI}}$ resistor sets the peak current of the inductor by tripping a comparator when the voltage across the resistor is 450 mV . The flip flop is reset and the inductor delivers its stored energy to the load. The ripple voltage ( $\mathrm{V}_{\text {RIPPLE }}$ ) at the Boost lead is controlled by CBoost. A snubber circuit, made up of a series resistor and capacitor, is required to dampen the ringing of the inductor. A value of $4.0 \Omega$ is recommended for $\mathrm{R}_{\mathrm{SNI}}$.

A zener diode is needed between the boost output voltage and the battery. This will clamp the boost lead to a specified value above the battery to prevent damage to the IC. A 9.0 volt zener diode is recommended.

## Sleep State

This device will enter into a low current mode ( $<275 \mu \mathrm{~A}$ ) when CTL lead is brought to less than 0.5 V . All functions are disabled in this mode, except for the regulator.

## Inhibit

When the inhibit is greater than 2.5 V the internal latch is set and the external MOSFET will be turned off for the remainder of the oscillator cycle. The latch is then reset at the start of the next cycle.

## Overvoltage Shutdown

The IC will disable the output during an overvoltage event. This is a real time fault event and does not set the internal latch and therefore is independent of the oscillator timing (i.e. asynchronous). There is 325 mV (typical) of hysteresis on the overvoltage function. There is no undervoltage lockout. The device will shutdown gracefully once it runs out of headroom.

## Reverse Battery

The CS4124 will not survive a reverse battery condition. A series diode is required between the battery and the $\mathrm{V}_{\mathrm{CC}}$ lead for reverse battery.

## Load Dump

A $10 \Omega$ resistor, (RS) is placed in series with $\mathrm{V}_{\mathrm{CC}}$ to limit the current into the IC during 40 V peak transient conditions.

PACKAGE THERMAL DATA

| Parameter |  | DIP-16 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 42 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 80 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC34152, MC33152, NCV33152

## High Speed Dual MOSFET Drivers

The MC34152/MC33152 are dual noninverting high speed drivers specifically designed for applications that require low current digital signals to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS/LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent system erratic operation at low supply voltages.

Typical applications include switching power supplies, dc-to-dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

This device is available in dual-in-line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs




## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC34152D | SO-8 | 98 Units/Rail |
| MC34152DR2 | SO-8 | 2500 Tape \& Reel |
| MC34152P | PDIP-8 | 50 Units/Rail |
| MC33152D | SO-8 | 98 Units/Rail |
| MC33152DR2 | SO-8 | 2500 Tape \& Reel |
| MC33152P | PDIP-8 | 50 Units/Rail |
| MC33152VDR2 | SO-8 | 2500 Tape \& Reel |
| NCV33152DR2 | SO-8 | 2500 Tape \& Reel |

Figure 1. Representative Diagram

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $V_{\text {CC }}$ | 20 | V |
| Logic Inputs (Note 1) | $V_{\text {in }}$ | -0.3 to $+\mathrm{V}_{\text {CC }}$ | V |
| Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to $\mathrm{V}_{\mathrm{CC}}$ ) | $\begin{gathered} \mathrm{lo} \\ \mathrm{l}(\text { (clamp) } \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | A |
| Power Dissipation and Thermal Characteristics <br> D Suffix, Plastic Package Case 751 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=50^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> P Suffix, Plastic Package, Case 626 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=50^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{gathered} 0.56 \\ 180 \\ \\ 1.0 \\ 100 \end{gathered}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature MC34152 <br>  MC33152 <br>  MC33152V, NCV33152 | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \\ -40 \text { to }+125 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Electrostatic Discharge Sensitivity (ESD) Human Body Model (HBM) Machine Model (MB) | - | $\begin{gathered} 2000 \\ 200 \end{gathered}$ | V |

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or $\mathrm{V}_{\mathrm{CC}}$, whichever is less.
2. Maximum package power dissipation limits must be observed.

## MC34152, MC33152, NCV33152

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LOGIC INPUTS |  |  |  |  |  |
| Input Threshold Voltage High State Logic 1 Low State Logic 0 | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | 2.6 | $\begin{aligned} & 1.75 \\ & 1.58 \end{aligned}$ | $\overline{0.9}$ | V |
| Input Current <br> High State $\left(\mathrm{V}_{\mathrm{IH}}=2.6 \mathrm{~V}\right)$ <br> Low State ( $\mathrm{V}_{\text {IL }}=0.8 \mathrm{~V}$ ) | $\begin{aligned} & I_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{IL}} \end{aligned}$ | - | $\begin{gathered} 100 \\ 20 \end{gathered}$ | $\begin{aligned} & 300 \\ & 100 \end{aligned}$ | $\mu \mathrm{A}$ |

## DRIVE OUTPUT

| Output Voltage |  |  |  |  | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Low State ( $\mathrm{l}_{\text {sink }}=10 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {OL }}$ | - | 0.8 | 1.2 |  |
| $\left(l_{\text {sink }}=50 \mathrm{~mA}\right)$ |  | - | 1.1 | 1.5 |  |
| $\left(I_{\text {sink }}=400 \mathrm{~mA}\right)$ |  | - | 1.8 | 2.5 |  |
| High State ( $\left.\mathrm{I}_{\text {source }}=10 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ | 10.5 | 11.2 | - |  |
| $\left(l_{\text {source }}=50 \mathrm{~mA}\right)$ |  | 10.4 | 11.1 | - |  |
| $\left(I_{\text {source }}=400 \mathrm{~mA}\right)$ |  | 10 | 10.8 | - |  |
| Output Pull-Down Resistor | RPD | - | 100 | - | k $\Omega$ |

SWITCHING CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$

| Propagation Delay ( $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ ) |  |  |  |  |  | ns |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Logic Input to: $\begin{aligned} & \text { Drive Output Rise } \\ & \\ & \text { Drive Output Fall }\end{aligned}$ | Drive Output Rise (10\% Input to $10 \%$ Output) Drive Output Fall ( $90 \%$ Input to $90 \%$ Output) | tPLH (IN/OUT) tPHL (IN/OUT) |  | $\begin{aligned} & 55 \\ & 40 \end{aligned}$ | $\begin{aligned} & 120 \\ & 120 \end{aligned}$ |  |
| Drive Output Rise Time (10\% to 90\%) | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF} \\ & \mathrm{C}_{\mathrm{L}}=2.5 \mathrm{nF} \end{aligned}$ | $\mathrm{t}_{r}$ | - | 14 36 | 30 - | ns |
| Drive Output Fall Time (90\% to 10\%) | $\begin{aligned} & C_{L}=1.0 \mathrm{nF} \\ & C_{L}=2.5 \mathrm{nF} \end{aligned}$ | $t_{f}$ | - | $\begin{aligned} & 15 \\ & 32 \end{aligned}$ | 30 | ns |

## TOTAL DEVICE

| Power Supply Current | $I_{C C}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Standby (Logic Inputs Grounded) |  | - | 6.0 | 8.0 |  |
| Operating (C $\mathrm{C}=1.0 \mathrm{nF}$ Drive Outputs 1 and $2, \mathrm{f}=100 \mathrm{kHz}$ ) |  | - | 10.5 | 15 |  |
| Operating Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 6.5 | - | 18 | V |

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34152, $-40^{\circ} \mathrm{C}$ for MC33152, $-40^{\circ} \mathrm{C}$ for MC33152V
$\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34152, $+85^{\circ} \mathrm{C}$ for MC33152, $+125^{\circ} \mathrm{C}$ for MC33152V
NCV33152: $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}, \mathrm{T}_{\text {high }}=+125^{\circ} \mathrm{C}$. Guaranteed by design. NCV prefix is for automotive and other applications requiring site and change control.


Figure 2. Switching Characteristics Test CIrcuit


Figure 3. Switching Waveform Definitions


Figure 4. Logic Input Current versus Input Voltage

Figure 6. Drive Output High to Low Propagation Delay versus Logic Input Overdrive Voltage


Figure 5. Logic Input Threshold Voltage versus Temperature


Figure 7. Drive Output Low to High Propagation Delay versus Logic Input Overdrive Voltage

$50 \mathrm{~ns} /$ DIV

Figure 8. Propagation Delay


Figure 10. Drive Output Saturation Voltage versus Load Current

$10 \mathrm{~ns} / \mathrm{DIV}$

Figure 12. Drive Output Rise Time


Figure 9. Drive Output Clamp Voltage versus Clamp Current


Figure 11. Drive Output Saturation Voltage versus Temperature

$10 \mathrm{~ns} / \mathrm{DIV}$
Figure 13. Drive Output Fall Time


Figure 14. Drive Output Rise and Fall Time versus Load Capacitance


Figure 16. Supply Current versus Input Frequency


Figure 15. Supply Current versus Drive Output Load Capacitance


Figure 17. Supply Current versus Supply Voltage

## APPLICATIONS INFORMATION

## Description

The MC34152 is a dual noninverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

## Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V . The input thresholds are insensitive to $\mathrm{V}_{\mathrm{CC}}$ making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to $\mathrm{V}_{\mathrm{CC}}$. This allows the output of one channel to directly drive the input of a second channel for master-slave operation. Each input has a $30 \mathrm{k} \Omega$ pull-down resistor so that an unconnected open input will cause the associated Drive Output to be in a known low state.

## Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of $2.4 \Omega$ at 1.0 A . The low 'on' resistance allows high output currents to be attained at a lower $\mathrm{V}_{\mathrm{CC}}$ than with comparative CMOS drivers. Each output has a $100 \mathrm{k} \Omega$ pull-down resistor to keep the MOSFET gate low when $\mathrm{V}_{\mathrm{CC}}$ is less than 1.4 V . No over current or thermal protection has been designed into the device, so output shorting to $\mathrm{V}_{\mathrm{CC}}$ or ground must be avoided.
Parasitic inductance in series with the load will cause the driver outputs to ring above $\mathrm{V}_{\mathrm{CC}}$ during the turn-on transition, and below ground during the turn-off transition. With CMOS drivers, this mode of operation can cause a destructive output latch-up condition. The MC34152 is immune to output latch-up. The Drive Outputs contain an internal diode to $\mathrm{V}_{\mathrm{CC}}$ for clamping positive voltage transients. When operating with $\mathrm{V}_{\mathrm{CC}}$ at 18 V , proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull-up transistor. Since full supply voltage is applied
across the NPN pull-up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 20, 21, and 22 show a method of using external Schottky diode clamps to reduce driver power dissipation.

## Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as $\mathrm{V}_{\mathrm{CC}}$ rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V , yielding about 500 mV of hysteresis.

## Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$
T_{J}=T_{A}+P_{D}\left(R_{\theta J A}\right)
$$

where: $\quad T_{J}=$ Junction Temperature
$\mathrm{T}_{\mathrm{A}}=$ Ambient Temperature
$P_{D}=$ Power Dissipation
$R_{\theta J A}=$ Thermal Resistance Junction to Ambient
There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$
P_{D}=P_{Q}+P_{C+P} T
$$

where: $\quad P_{Q}=$ Quiescent Power Dissipation
$P_{C}=$ Capacitive Load Power Dissipation
$\mathrm{P}_{\mathrm{T}}=$ Transition Power Dissipation
The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 17. The device's quiescent power dissipation is:

$$
\mathrm{P}_{\mathrm{Q}}=\mathrm{V}_{\mathrm{CC}}\left(\mathrm{I}_{\mathrm{CCL}}[1-\mathrm{D}]+\mathrm{I}_{\mathrm{CCH}}[\mathrm{D}]\right)
$$

$$
\text { where: } \quad \begin{aligned}
& \mathrm{I}_{\mathrm{CCL}}=\text { Supply Current with Low State Drive } \\
& \text { Outputs } \\
& \mathrm{I}_{\mathrm{CCH}}=\text { Supply Current with High State Drive } \\
& \text { Outputs } \\
& \mathrm{D}=\text { Output Duty Cycle }
\end{aligned}
$$

The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$
\text { where: } \begin{aligned}
\mathrm{P}_{\mathrm{C}} & =\mathrm{V}_{\mathrm{CC}}\left(\mathrm{~V}_{\mathrm{OH}}-\mathrm{V}_{\mathrm{OL}}\right) \mathrm{C}_{\mathrm{L}} \mathrm{f} \\
\mathrm{~V}_{\mathrm{OH}} & =\text { High State Drive Output Voltage } \\
\mathrm{V}_{\mathrm{OL}} & =\text { Low State Drive Output Voltage } \\
\mathrm{C}_{\mathrm{L}} & =\text { Load Capacitance } \\
\mathrm{f} & =\text { Frequency }
\end{aligned}
$$

When driving a MOSFET, the calculation of capacitive load power $\mathrm{P}_{\mathrm{C}}$ is somewhat complicated by the changing
gate to source capacitance $\mathrm{C}_{\mathrm{GS}}$ as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 18 shows a curve of gate voltage versus gate charge for the ON Semiconductor MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on,' the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge $\mathrm{Q}_{\mathrm{g}}$ of 110 nC is required when operating the MOSFET with a drain to source voltage $\mathrm{V}_{\mathrm{DS}}$ of 400 V .


Figure 18. Gate-to-Source Voltage versus Gate charge
The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$
P_{C(M O S F E T)}=V_{C C} Q_{g} f
$$

The flat region from 10 nC to 55 nC is caused by the drain-to-gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34152 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34152 at a higher $\mathrm{V}_{\mathrm{CC}}$, additional charge can be provided to bring the gate above 10 V . This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.
The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$
\begin{aligned}
& \mathrm{P}_{\mathrm{T}} \approx \mathrm{~V}_{\mathrm{CC}}\left(1.08 \mathrm{~V}_{\mathrm{CC}} \mathrm{C}_{\mathrm{L}} \mathrm{f}-8 \times 10^{-4}\right) \\
& \mathrm{P}_{\mathrm{T}} \text { must be greater than zero. }
\end{aligned}
$$

Switching time characterization of the MC34152 is performed with fixed capacitive loads. Figure 14 shows that for small capacitance loads, the switching speed is limited by transistor turn-on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

## LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards. When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive
performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the $\mathrm{V}_{\mathrm{CC}}$ pin and ground as the layout will permit. Suggested capacitors are a low inductance $0.1 \mu \mathrm{~F}$ ceramic in parallel with a $4.7 \mu \mathrm{~F}$ tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

Proper printed circuit board layout is extremely critical and cannot be over emphasized.


Series gate resistor $\mathrm{R}_{\mathrm{g}}$ may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. $R_{g}$ will decrease the MOSFET switching speed. Schottky diode $\mathrm{D}_{1}$ can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. MOSFET Parasitic Oscillations


Figure 22. Isolated MOSFET Drive


In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn-on and turn-off times.

Figure 23. Controlled MOSFET Drive


The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor $\mathrm{C}_{1}$.

Figure 24. Bipolar Transistor Drive


## MC34151, MC33151

## High Speed Dual MOSFET Drivers

The MC34151/MC33151 are dual inverting high speed drivers specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

Typical applications include switching power supplies, dc to dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual-in-line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026


Figure 1. Representative Block Diagram


## ON Semiconductor ${ }^{\text {T }}$

http://onsemi.com


PIN CONNECTIONS

(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC34151D | SO-8 | 98 Units/Rail |
| MC34151DR2 | SO-8 | 2500 Tape \& Reel |
| MC34151P | PDIP-8 | 50 Units/Rail |
| MC33151D | SO-8 | 98 Units/Rail |
| MC33151DR2 | SO-8 | 2500 Tape \& Reel |
| MC33151P | PDIP-8 | 50 Units/Rail |
| MC33151VDR2 | SO-8 | 2500 Units/Rail |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 20 | V |
| Logic Inputs (Note 1) | $V_{\text {in }}$ | -0.3 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to $\mathrm{V}_{\mathrm{CC}}$ ) | $\underset{\substack{\mathrm{IO} \\ \mathrm{l}(\text { clamp })}}{ }$ | $\begin{aligned} & 1.5 \\ & 1.0 \end{aligned}$ | A |
| Power Dissipation and Thermal Characteristics D Suffix SO-8 Package Case 751 Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=50^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air P Suffix 8-Pin Package Case 626 Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=50^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> PD <br> $\mathrm{R}_{\text {日JA }}$ | $\begin{aligned} & 0.56 \\ & 180 \\ & \\ & 1.0 \\ & 100 \end{aligned}$ | $\begin{gathered} W \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature <br> MC34151 <br> MC33151 | $\mathrm{T}_{\mathrm{A}}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+85 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS
$\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}\right.$, for typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the only operating ambient temperature range that applies [Note 3], unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LOGIC INPUTS |  |  |  |  |  |
| $\begin{array}{r} \text { Input Threshold Voltage - High State Logic } 1 \\ \text { - Low State Logic } 0 \end{array}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\\| I} \end{aligned}$ | $2.6$ | $\begin{aligned} & 1.75 \\ & 1.58 \end{aligned}$ | $\overline{0.8}$ | V |
| $\begin{aligned} & \text { Input Current - } \text { High State }\left(\mathrm{V}_{\mathrm{IH}}=2.6 \mathrm{~V}\right) \\ & \text { - Low State }\left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}\right) \end{aligned}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{H}} \\ & \mathrm{I}_{\mathrm{LL}} \end{aligned}$ | - | $\begin{gathered} 200 \\ 20 \end{gathered}$ | $\begin{aligned} & 500 \\ & 100 \end{aligned}$ | $\mu \mathrm{A}$ |

## DRIVE OUTPUT



SWITCHING CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$

| Propagation Delay ( $10 \%$ Input to $10 \%$ Output, $C_{L}=1.0 \mathrm{nF}$ ) Logic Input to Drive Output Rise Logic Input to Drive Output Fall | tpLH(in/out) tpHL(in/out) | - | $\begin{aligned} & 35 \\ & 36 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive Output Rise Time (10\% to 90\%) $C_{L}=1.0 \mathrm{nF}$ $C_{L}=2.5 \mathrm{nF}$ | $\mathrm{tr}_{r}$ | - | 14 31 | 30 - | ns |
| Drive Output Fall Time ( $90 \%$ to $10 \%$ ) $C_{L}=1.0 \mathrm{nF}$ $C_{L}=2.5 \mathrm{nF}$ | $t_{f}$ | - | $\begin{aligned} & 16 \\ & 32 \end{aligned}$ | 30 | ns |

## TOTAL DEVICE

| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Standby (Logic Inputs Grounded) |  | - | 6.0 | 10 |  |
| Operating (C $=1.0 \mathrm{nF}$ Drive Outputs 1 and $2, \mathrm{f}=100 \mathrm{kHz})$ |  | - | 10.5 | 15 |  |
| Operating Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 6.5 | - | 18 | V |

1. For optimum switching speed, the maximum input voltage should be limited to 10 V or $\mathrm{V}_{\mathrm{CC}}$, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34151 $\quad \mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34151
$-40^{\circ} \mathrm{C}$ for MC33151 $+85^{\circ} \mathrm{C}$ for MC33151


Figure 2. Switching Characteristics Test Circuit


Figure 3. Switching Waveform Definitions


Figure 4. Logic Input Current versus Input Voltage


Figure 6. Drive Output Low-to-High Propagation Delay versus Logic Overdrive Voltage


Figure 5. Logic Input Threshold Voltage versus Temperature


Figure 7. Drive Output High-to-Low Propagation Delay versus Logic Input Overdrive Voltage

$50 \mathrm{~ns} /$ DIV
Figure 8. Propagation Delay


Figure 10. Drive Output Saturation Voltage versus Load Current


Figure 12. Drive Output Rise Time


Figure 9. Drive Output Clamp Voltage versus Clamp Current


Figure 11. Drive Output Saturation Voltage versus Temperature


Figure 13. Drive Output Fall Time


Figure 14. Drive Output Rise and Fall Time versus Load Capacitance


Figure 16. Supply Current versus Input Frequency


Figure 15. Supply Current versus Drive Output Load Capacitance


Figure 17. Supply Current versus Supply Voltage

## APPLICATIONS INFORMATION

## Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

## Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V . The input thresholds are insensitive to $\mathrm{V}_{\mathrm{CC}}$ making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to $\mathrm{V}_{\mathrm{CC}}$. This allows the output of one channel to directly drive the input of a second channel for master-slave operation. Each input has a $30 \mathrm{k} \Omega$ pull-down resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

## Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of $2.4 \Omega$ at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower $\mathrm{V}_{\mathrm{CC}}$ than with comparative CMOS drivers. Each output has a $100 \mathrm{k} \Omega$ pull-down resistor to keep the MOSFET gate low when $\mathrm{V}_{\mathrm{CC}}$ is less than 1.4 V . No over current or thermal protection has been designed into the device, so output shorting to $\mathrm{V}_{\mathrm{CC}}$ or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above $\mathrm{V}_{\mathrm{CC}}$ during the turn-on transition, and below ground during the turn-off transition. With CMOS drivers, this mode of operation can cause a destructive output latch-up condition. The MC34151 is immune to output latch-up. The Drive Outputs contain an internal diode to $\mathrm{V}_{\mathrm{CC}}$ for clamping positive voltage transients. When operating with $\mathrm{V}_{\mathrm{CC}}$ at 18 V , proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull-up transistor. Since full supply voltage is applied across
the NPN pull-up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 20, 21, and 22 show a method of using external Schottky diode clamps to reduce driver power dissipation.

## Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as $\mathrm{V}_{\mathrm{CC}}$ rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V , yielding about 500 mV of hysteresis.

## Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:
where:

$$
\begin{aligned}
\mathrm{T}_{\mathrm{J}} & =\mathrm{T}_{\mathrm{A}}+\mathrm{P}_{\mathrm{D}}\left(\mathrm{R}_{\theta \mathrm{JA}}\right) \\
\mathrm{T}_{\mathrm{J}} & =\text { Junction Temperature } \\
\mathrm{T}_{\mathrm{A}} & =\text { Ambient Temperature } \\
\mathrm{P}_{\mathrm{D}} & =\text { Power Dissipation } \\
\mathrm{R}_{\theta \mathrm{JA}} & =\text { Thermal Resistance Junction to Ambient }
\end{aligned}
$$

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$
\text { where: } \quad \begin{aligned}
& \mathrm{P}_{\mathrm{D}}=\mathrm{P}_{\mathrm{Q}}+\mathrm{P}_{\mathrm{C}}+\mathrm{P}_{\mathrm{T}} \\
& \mathrm{P}_{\mathrm{Q}}=\mathrm{Quiescent} \text { Power Dissipation } \\
& \mathrm{P}_{\mathrm{C}}=\text { Capacitive Load Power Dissipation } \\
& \mathrm{P}_{\mathrm{T}}=\text { Transition Power Dissipation }
\end{aligned}
$$

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 17. The device's quiescent power dissipation is:

$$
\mathrm{P}_{\mathrm{Q}}=\mathrm{V}_{\mathrm{CC}}\left(\mathrm{I}_{\mathrm{CCL}}(1-\mathrm{D})+\mathrm{I}_{\mathrm{CCH}}(\mathrm{D})\right)
$$

where: $\quad \mathrm{I}_{\mathrm{CCL}}=$ Supply Current with Low State Drive Outputs
$\mathrm{I}_{\mathrm{CCH}}=$ Supply Current with High State Drive Outputs
D = Output Duty Cycle
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$
\text { where: } \quad \begin{aligned}
\mathrm{P}_{\mathrm{C}} & =\mathrm{V}_{\mathrm{CC}}\left(\mathrm{~V}_{\mathrm{OH}}-\mathrm{V}_{\mathrm{OL}}\right) \mathrm{C}_{\mathrm{L}} \mathrm{f} \\
\mathrm{~V}_{\mathrm{OH}} & =\text { High State Drive Output Voltage } \\
\mathrm{V}_{\mathrm{OL}} & =\text { Low State Drive Output Voltage } \\
\mathrm{C}_{\mathrm{L}} & =\text { Load Capacitance } \\
\mathrm{f} & =\text { frequency }
\end{aligned}
$$

When driving a MOSFET, the calculation of capacitive load power $\mathrm{P}_{\mathrm{C}}$ is somewhat complicated by the changing gate to source capacitance $\mathrm{C}_{\mathrm{GS}}$ as the device switches. To aid in this calculation, power MOSFET manufacturers provide
gate charge information on their data sheets. Figure 18 shows a curve of gate voltage versus gate charge for the ON Semiconductor MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on', the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge $\mathrm{Q}_{\mathrm{g}}$ of 110 nC is required when operating the MOSFET with a drain to source voltage $\mathrm{V}_{\mathrm{DS}}$ of 400 V .


Figure 18. Gate-To-Source Voltage versus Gate Charge

The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$
P_{C}(M O S F E T)=V_{C} Q_{g} f
$$

The flat region from 10 nC to 55 nC is caused by the drain-to-gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher $\mathrm{V}_{\mathrm{CC}}$, additional charge can be provided to bring the gate above 10 V . This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$
\begin{aligned}
& P_{\mathrm{T}}=V_{C C}\left(1.08 \mathrm{~V}_{\mathrm{CC}} C_{\mathrm{L}} f-8 \text { y } 10^{-4}\right) \\
& \mathrm{P}_{\mathrm{T}} \text { must be greater than zero. }
\end{aligned}
$$

Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 14 shows that for small capacitance loads, the switching speed is limited by transistor turn-on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

## LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards. When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For


The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. Enhanced System Performance with Common Switching Regulators


Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above $\mathrm{V}_{\mathrm{CC}}$ and below ground.

Figure 21. Direct Transformer Drive
optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the $\mathrm{V}_{\mathrm{CC}}$ pin and ground as the layout will permit. Suggested capacitors are a low inductance $0.1 \mu \mathrm{~F}$ ceramic in parallel with a $4.7 \mu \mathrm{~F}$ tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

Proper printed circuit board layout is extremely critical and cannot be over emphasized.



#### Abstract

Series gate resistor $\mathrm{R}_{\mathrm{g}}$ may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. $\mathrm{R}_{\mathrm{g}}$ will decrease the MOSFET switching speed. Schottky diode $D_{1}$ can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.


Figure 20. MOSFET Parasitic Oscillations


Figure 22. Isolated MOSFET Drive

## MC34151, MC33151



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Figure 25. Dual Charge Pump Converter

| Output Load Regulation |  |  |
| :---: | :---: | :---: |
| $\mathbf{I}_{\mathbf{O}}(\mathbf{m A})$ | $+\mathbf{V}_{\mathbf{O}}(\mathbf{V})$ | $-\mathbf{V}_{\mathbf{O}}(\mathbf{V})$ |
| 0 | 27.7 | -13.3 |
| 1.0 | 27.4 | -12.9 |
| 10 | 26.4 | -11.9 |
| 20 | 25.5 | -11.2 |
| 30 | 24.6 | -10.5 |
| 50 | 22.6 | -9.4 |

## Single IGBT Gate Driver

The MC33153 is specifically designed as an IGBT driver for high power applications that include ac induction motor control, brushless dc motor control and uninterruptable power supplies. Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors. Device protection features include the choice of desaturation or overcurrent sensing and undervoltage detection. These devices are available in dual-in-line and surface mount packages and include the following features:

- High Current Output Stage: 1.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimized for IGBT's
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors


This device contains 133 active transistors.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Power Supply Voltage } \\ & \mathrm{V}_{\mathrm{CC}} \text { to } \mathrm{V}_{\mathrm{EE}} \\ & \text { Kelvin Ground to } \mathrm{V}_{\mathrm{EE}} \text { (Note 1) } \end{aligned}$ | $\begin{gathered} \mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}} \\ \mathrm{KGnd}-\mathrm{V}_{\mathrm{EE}} \end{gathered}$ | $\begin{aligned} & 20 \\ & 20 \end{aligned}$ | V |
| Logic Input | $V_{\text {in }}$ | $\mathrm{V}_{\mathrm{EE}}-0.3$ to $\mathrm{V}_{\text {CC }}$ | V |
| Current Sense Input | $\mathrm{V}_{\text {S }}$ | -0.3 to $\mathrm{V}_{\text {CC }}$ | V |
| Blanking/Desaturation Input | $V_{B D}$ | -0.3 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Gate Drive Output <br> Source Current <br> Sink Current <br> Diode Clamp Current | Io | $\begin{aligned} & 1.0 \\ & 2.0 \\ & 1.0 \end{aligned}$ | A |
| Fault Output Source Current Sink Current | $\mathrm{I}_{\text {FO }}$ | $\begin{aligned} & 25 \\ & 10 \end{aligned}$ | mA |
| Power Dissipation and Thermal Characteristics <br> D Suffix SO-8 Package, Case 751 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=50^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> P Suffix DIP-8 Package, Case 626 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=50^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {日JA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{aligned} & 0.56 \\ & 180 \\ & \\ & 1.0 \\ & 100 \end{aligned}$ | $\begin{gathered} \mathrm{W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~W} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}\right.$, Kelvin Gnd connected to $\mathrm{V}_{\mathrm{EE}}$. For typical values
$T_{A}=25^{\circ} \mathrm{C}$, for min/max values $T_{A}$ is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LOGIC INPUT |  |  |  |  |  |
| Input Threshold Voltage <br> High State (Logic 1) <br> Low State (Logic 0) | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | $1.2$ | $\begin{array}{r} 2.70 \\ 2.30 \end{array}$ | $3.2$ | V |
| Input Current <br> High State $\left(\mathrm{V}_{\mathrm{IH}}=3.0 \mathrm{~V}\right)$ <br> Low State ( $\mathrm{V}_{\mathrm{IL}}=1.2 \mathrm{~V}$ ) | $\begin{aligned} & I_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{IL}} \end{aligned}$ | - | $\begin{gathered} 130 \\ 50 \end{gathered}$ | $\begin{aligned} & 500 \\ & 100 \end{aligned}$ | $\mu \mathrm{A}$ |

DRIVE OUTPUT

| Output Voltage |  |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Low State ( $\mathrm{I}_{\text {Sink }}=1.0 \mathrm{~A}$ ) | $\mathrm{V}_{\mathrm{OL}}$ | - | 2.0 | 2.5 |  |
| High State ( S $_{\text {Source }}=500 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{OH}}$ | 12 | 13.9 | - |  |
| Output Pull-Down Resistor | $\mathrm{R}_{\text {PD }}$ | - | 100 | 200 | $\mathrm{k} \Omega$ |

## FAULT OUTPUT

| Output voltage |  |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\quad$ Low State $\left(I_{\text {Sink }}=5.0 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{FL}}$ | - | 0.2 | 1.0 | V |
| High State $\left(I_{\text {Source }}=20 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{FH}}$ | 12 | 13.3 | - |  |

## SWITCHING CHARACTERISTICS

| Propagation Delay ( $50 \%$ Input to $50 \%$ Output $C_{L}=1.0 \mathrm{nF}$ ) Logic Input to Drive Output Rise Logic Input to Drive Output Fall | tpLH(in/out) <br> tpHL (in/out) | - | $\begin{gathered} 80 \\ 120 \end{gathered}$ | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | ns |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive Output Rise Time (10\% to 90\%) $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ | $\mathrm{t}_{\mathrm{r}}$ | - | 17 | 55 | ns |
| Drive Output Fall Time (90\% to 10\%) $\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}$ | $\mathrm{t}_{\mathrm{f}}$ | - | 17 | 55 | ns |

NOTES: 1. Kelvin Ground must always be between $\mathrm{V}_{\mathrm{EE}}$ and $\mathrm{V}_{\mathrm{CC}}$.

[^40]
## MC33153

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=0 \mathrm{~V}\right.$, Kelvin Gnd connected to $\mathrm{V}_{\mathrm{EE}}$. For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}$ is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| SWITCHING CHARACTERISTICS (continued) |  |  |  |  |  |
| Propagation Delay | $\operatorname{tp}_{P}(\mathrm{OC})$ | - | 0.3 | 1.0 | $\mu \mathrm{~s}$ |
| Current Sense Input to Drive Output | $\mathrm{t}_{\mathrm{P}(\mathrm{FLT})}$ | - | 0.3 | 1.0 |  |
| Fault Blanking/Desaturation Input to Drive Output |  |  |  |  |  |

UVLO

| Startup Voltage | $V_{\text {CC start }}$ | 11.3 | 12 | 12.6 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Disable Voltage | $\mathrm{V}_{\text {CC dis }}$ | 10.4 | 11 | 11.7 | V |

COMPARATORS

| Overcurrent Threshold Voltage $\left(\mathrm{V}_{\text {Pin8 }}>7.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\text {SOC }}$ | 50 | 65 | 80 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Short Circuit Threshold Voltage $\left(\mathrm{V}_{\text {Pin8 }}>7.0 \mathrm{~V}\right)$ | $\mathrm{V}_{\mathrm{SSC}}$ | 100 | 130 | 160 | mV |
| Fault Blanking/Desaturation Threshold $\left(\mathrm{V}_{\text {Pin1 }}>100 \mathrm{mV}\right)$ | $\mathrm{V}_{\mathrm{th}(\mathrm{FLT})}$ | 6.0 | 6.5 | 7.0 | V |
| Current Sense Input Current $\left(\mathrm{V}_{\mathrm{SI}}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{SI}}$ | - | -1.4 | -10 | $\mu \mathrm{~A}$ |

FAULT BLANKING/DESATURATION INPUT

| Current Source $\left(\mathrm{V}_{\text {Pin8 }}=0 \mathrm{~V}, \mathrm{~V}_{\text {Pin4 }}=0 \mathrm{~V}\right)$ | $\mathrm{I}_{\text {chg }}$ | -200 | -270 | -300 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Discharge Current $\left(\mathrm{V}_{\text {Pin8 }}=15 \mathrm{~V}, \mathrm{~V}_{\text {Pin4 }}=5.0 \mathrm{~V}\right)$ | $\mathrm{I}_{\mathrm{dsch}}$ | 1.0 | 2.5 | - | mA |

TOTAL DEVICE

| Power Supply Current | $I_{C C}$ |  |  |  | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Standby (V $\mathrm{V}_{\text {in }}=\mathrm{V}_{\mathrm{CC}}$, Output Open) |  | - | 7.2 | 14 |  |
| Operating ( $\left.\mathrm{C}_{\mathrm{L}}=1.0 \mathrm{nF}, \mathrm{f}=20 \mathrm{kHz}\right)$ |  | - | 7.9 | 20 |  |

NOTES: 1. Kelvin Ground must always be between $\mathrm{V}_{\mathrm{EE}}$ and $\mathrm{V}_{\mathrm{CC}}$.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
$\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}$ for MC33153 $\quad \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}$ for MC33153


Figure 1. Input Current versus Input Voltage


Figure 2. Output Voltage versus Input Voltage


Figure 3. Input Threshold Voltage versus Temperature


Figure 5. Drive Output Low State Voltage versus Temperature


Figure 7. Drive Output High State Voltage versus Temperature


Figure 4. Input Threshold Voltage versus Supply Voltage


Figure 6. Drive Output Low State Voltage versus Sink Current


Figure 8. Drive Output High State Voltage versus Source Current


Figure 9. Drive Output Voltage versus Current Sense Input Voltage


Figure 11. Overcurrent Protection Threshold Voltage versus Temperature


Figure 13. Short Circuit Comparator Threshold Voltage versus Temperature


Figure 10. Fault Output Voltage versus Current Sense Input Voltage


Figure 12. Overcurrent Protection Threshold Voltage versus Supply Voltage


Figure 14. Short Circuit Comparator Threshold Voltage versus Supply Voltage


Figure 15. Current Sense Input Current versus Voltage


Figure 17. Fault Blanking/Desaturation Comparator Threshold Voltage versus Temperature


Figure 16. Drive Output Voltage versus Fault Blanking/Desaturation Input Voltage


Figure 18. Fault Blanking/Desaturation Comparator Threshold Voltage versus Supply Voltage


Figure 19. Fault Blanking/Desaturation Current Source versus Temperature


Figure 20. Fault Blanking/Desaturation Current Source versus Supply Voltage


Figure 21. Fault Blanking/Desaturation Current Source versus Input Voltage


Figure 23. Fault Output Low State Voltage versus Sink Current


Figure 25. Drive Output Voltage versus Supply Voltage


Figure 22. Fault Blanking/Desaturation Discharge Current versus Input Voltage


Figure 24. Fault Output High State Voltage versus Source Current


Figure 26. UVLO Thresholds versus Temperature


Figure 27. Supply Current versus Supply Voltage


Figure 28. Supply Current versus Temperature


Figure 29. Supply Current versus Input Frequency

## OPERATING DESCRIPTION

## GATE DRIVE

## Controlling Switching Times

The most important design aspect of an IGBT gate drive is optimization of the switching characteristics. The switching characteristics are especially important in motor control applications in which PWM transistors are used in a bridge configuration. In these applications, the gate drive circuit components should be selected to optimize turn-on, turn-off and off-state impedance. A single resistor may be used to control both turn-on and turn-off as shown in Figure 30. However, the resistor value selected must be a compromise in turn-on abruptness and turn-off losses. Using a single resistor is normally suitable only for very low frequency PWM. An optimized gate drive output stage is shown in Figure 31. This circuit allows turn-on and turn-off to be optimized separately. The turn-on resistor, $\mathrm{R}_{\mathrm{on}}$, provides control over the IGBT turn-on speed. In motor control circuits, the resistor sets the turn-on di/dt that controls how fast the free-wheel diode is cleared. The interaction of the IGBT and free-wheeling diode determines
the turn-on dv/dt. Excessive turn-on dv/dt is a common problem in half-bridge circuits. The turn-off resistor, $\mathrm{R}_{\text {off }}$, controls the turn-off speed and ensures that the IGBT remains off under commutation stresses. Turn-off is critical to obtain low switching losses. While IGBTs exhibit a fixed minimum loss due to minority carrier recombination, a slow gate drive will dominate the turn-off losses. This is particularly true for fast IGBTs. It is also possible to turn-off an IGBT too fast. Excessive turn-off speed will result in large overshoot voltages. Normally, the turn-off resistor is a small fraction of the turn-on resistor.

The MC33153 contains a bipolar totem pole output stage that is capable of sourcing 1.0 amp and sinking 2.0 amps peak. This output also contains a pull down resistor to ensure that the IGBT is off whenever there is insufficient $\mathrm{V}_{\mathrm{CC}}$ to the MC33153.

In a PWM inverter, IGBTs are used in a half-bridge configuration. Thus, at least one device is always off. While
the IGBT is in the off-state, it will be subjected to changes in voltage caused by the other devices. This is particularly a problem when the opposite transistor turns on.

When the lower device is turned on, clearing the upper diode, the turn-on dv/dt of the lower device appears across the collector emitter of the upper device. To eliminate shoot-through currents, it is necessary to provide a low sink impedance to the device that is in the off-state. In most applications the turn-off resistor can be made small enough to hold off the device that is under commutation without causing excessively fast turn-off speeds.


Figure 30. Using a Single Gate Resistor


Figure 31. Using Separate Resistors for Turn-On and Turn-Off

A negative bias voltage can be used to drive the IGBT into the off-state. This is a practice carried over from bipolar Darlington drives and is generally not required for IGBTs. However, a negative bias will reduce the possibility of shoot-through. The MC33153 has separate pins for $\mathrm{V}_{\mathrm{EE}}$ and Kelvin Ground. This permits operation using a $+15 /-5.0 \mathrm{~V}$ supply.

## INTERFACING WITH OPTOISOLATORS

## Isolated Input

The MC33153 may be used with an optically isolated input. The optoisolator can be used to provide level shifting, and if desired, isolation from ac line voltages. An optoisolator with a very high dv/dt capability should be used, such as the Hewlett Packard HCPL4053. The IGBT gate turn-on resistor should be set large enough to ensure
that the opto's dv/dt capability is not exceeded. Like most optoisolators, the HCPL4053 has an active low open-collector output. Thus, when the LED is on, the output will be low. The MC33153 has an inverting input pin to interface directly with an optoisolator using a pull up resistor. The input may also be interfaced directly to 5.0 V CMOS logic or a microcontroller.

## Optoisolator Output Fault

The MC33153 has an active high fault output. The fault output may be easily interfaced to an optoisolator. While it is important that all faults are properly reported, it is equally important that no false signals are propagated. Again, a high dv/dt optoisolator should be used.

The LED drive provides a resistor programmable current of 10 to 20 mA when on, and provides a low impedance path when off. An active high output, resistor, and small signal diode provide an excellent LED driver. This circuit is shown in Figure 32.


Figure 32. Output Fault Optoisolator

## UNDERVOLTAGE LOCKOUT

It is desirable to protect an IGBT from insufficient gate voltage. IGBTs require 15 V on the gate to achieve the rated on-voltage. At gate voltages below 13 V , the on-voltage increases dramatically, especially at higher currents. At very low gate voltages, below 10 V , the IGBT may operate in the linear region and quickly overheat. Many PWM motor drives use a bootstrap supply for the upper gate drive. The UVLO provides protection for the IGBT in case the bootstrap capacitor discharges.

The MC33153 will typically start up at about 12 V . The UVLO circuit has about 1.0 V of hysteresis and will disable the output if the supply voltage falls below about 11 V .

## PROTECTION CIRCUITRY

## Desaturation Protection

Bipolar Power circuits have commonly used what is known as "Desaturation Detection". This involves monitoring the collector voltage and turning off the device if this voltage rises above a certain limit. A bipolar transistor will only conduct a certain amount of current for a given base drive. When the base is overdriven, the device is in
saturation. When the collector current rises above the knee, the device pulls out of saturation. The maximum current the device will conduct in the linear region is a function of the base current and the dc current gain $\left(\mathrm{h}_{\mathrm{FE}}\right)$ of the transistor.

The output characteristics of an IGBT are similar to a Bipolar device. However, the output current is a function of gate voltage instead of current. The maximum current depends on the gate voltage and the device type. IGBTs tend to have a very high transconductance and a much higher current density under a short circuit than a bipolar device. Motor control IGBTs are designed for a lower current density under shorted conditions and a longer short circuit survival time.

The best method for detecting desaturation is the use of a high voltage clamp diode and a comparator. The MC33153 has a Fault Blanking/Desaturation Comparator which senses the collector voltage and provides an output indicating when the device is not fully saturated. Diode D1 is an external high voltage diode with a rated voltage comparable to the power device. When the IGBT is "on" and saturated, D1 will pull down the voltage on the Fault Blanking/Desaturation Input. When the IGBT pulls out of saturation or is "off", the current source will pull up the input and trip the comparator. The comparator threshold is 6.5 V , allowing a maximum on-voltage of about 5.8 V .

A fault exists when the gate input is high and $\mathrm{V}_{\mathrm{CE}}$ is greater than the maximum allowable $\mathrm{V}_{\mathrm{CE}(\mathrm{sat)}}$. The output of the Desaturation Comparator is ANDed with the gate input signal and fed into the Short Circuit and Overcurrent Latches. The Overcurrent Latch will turn-off the IGBT for the remainder of the cycle when a fault is detected. When input goes high, both latches are reset. The reference voltage is tied to the Kelvin Ground instead of the $\mathrm{V}_{\mathrm{EE}}$ to make the threshold independent of negative gate bias. Note that for proper operation of the Desaturation Comparator and the Fault Output, the Current Sense Input must be biased above the Overcurrent and Short Circuit Comparator thresholds. This can be accomplished by connecting Pin 1 to $\mathrm{V}_{\mathrm{CC}}$.


Figure 33. Desaturation Detection

The MC33153 also features a programmable fault blanking time. During turn-on, the IGBT must clear the opposing free-wheeling diode. The collector voltage will remain high until the diode is cleared. Once the diode has
been cleared, the voltage will come down quickly to the $\mathrm{V}_{\mathrm{CE}(\mathrm{sat})}$ of the device. Following turn-on, there is normally considerable ringing on the collector due to the COSS capacitance of the IGBTs and the parasitic wiring inductance. The fault signal from the Desaturation Comparator must be blanked sufficiently to allow the diode to be cleared and the ringing to settle out.

The blanking function uses an NPN transistor to clamp the comparator input when the gate input is low. When the input is switched high, the clamp transistor will turn "off", allowing the internal current source to charge the blanking capacitor. The time required for the blanking capacitor to charge up from the on-voltage of the internal NPN transistor to the trip voltage of the comparator is the blanking time.

If a short circuit occurs after the IGBT is turned on and saturated, the delay time will be the time required for the current source to charge up the blanking capacitor from the $\mathrm{V}_{\mathrm{CE}(\mathrm{sat})}$ level of the IGBT to the trip voltage of the comparator. Fault blanking can be disabled by leaving Pin 8 unconnected.

## Sense IGBT Protection

Another approach to protecting the IGBTs is to sense the emitter current using a current shunt or Sense IGBTs. This method has the advantage of being able to use high gain IGBTs which do not have any inherent short circuit capability. Current sense IGBTs work as well as current sense MOSFETs in most circumstances. However, the basic problem of working with very low sense voltages still exists. Sense IGBTs sense current through the channel and are therefore linear with respect to the collector current. Because IGBTs have a very low incremental on-resistance, sense IGBTs behave much like low-on resistance current sense MOSFETs. The output voltage of a properly terminated sense IGBT is very low, normally less than 100 mV .
The sense IGBT approach requires fault blanking to prevent false tripping during turn-on. The sense IGBT also requires that the sense signal is ignored while the gate is low. This is because the mirror output normally produces large transient voltages during both turn-on and turn-off due to the collector to mirror capacitance. With non-sensing types of IGBTs, a low resistance current shunt ( 5.0 to $50 \mathrm{~m} \Omega$ ) can be used to sense the emitter current. When the output is an actual short circuit, the inductance will be very low. Since the blanking circuit provides a fixed minimum on-time, the peak current under a short circuit can be very high. A short circuit discern function is implemented by the second comparator which has a higher trip voltage. The short circuit signal is latched and appears at the Fault Output. When a short circuit is detected, the IGBT should be turned-off for several milliseconds allowing it to cool down before it is turned back on. The sense circuit is very similar to the desaturation circuit. It is possible to build a combination circuit that provides protection for both Short Circuit capable IGBTs and Sense IGBTs.

## APPLICATION INFORMATION

Figure 34 shows a basic IGBT driver application. When driven from an optoisolator, an input pull up resistor is required. This resistor value should be set to bias the output transistor at the desired current. A decoupling capacitor should be placed close to the IC to minimize switching noise.

A bootstrap diode may be used for a floating supply. If the protection features are not required, then both the Fault Blanking/Desaturation and Current Sense Inputs should both be connected to the Kelvin Ground (Pin 2). When used with a single supply, the Kelvin Ground and $\mathrm{V}_{\mathrm{EE}}$ pins should be connected together. Separate gate resistors are recommended to optimize the turn-on and turn-off drive.


Figure 34. Basic Application


Figure 35. Dual Supply Application

When used in a dual supply application as in Figure 35, the Kelvin Ground should be connected to the emitter of the IGBT. If the protection features are not used, then both the Fault Blanking/Desaturation and the Current Sense Inputs should be connected to Ground. The input optoisolator should always be referenced to $\mathrm{V}_{\mathrm{EE}}$ -

If desaturation protection is desired, a high voltage diode is connected to the Fault Blanking/Desaturation pin. The
blanking capacitor should be connected from the Desaturation pin to the $V_{E E}$ pin. If a dual supply is used, the blanking capacitor should be connected to the Kelvin Ground. The Current Sense Input should be tied high because the two comparator outputs are ANDed together. Although the reverse voltage on collector of the IGBT is clamped to the emitter by the free-wheeling diode, there is normally considerable inductance within the package itself. A small resistor in series with the diode can be used to protect the IC from reverse voltage transients.


Figure 36. Desaturation Application
When using sense IGBTs or a sense resistor, the sense voltage is applied to the Current Sense Input. The sense trip voltages are referenced to the Kelvin Ground pin. The sense voltage is very small, typically about 65 mV , and sensitive to noise. Therefore, the sense and ground return conductors should be routed as a differential pair. An RC filter is useful in filtering any high frequency noise. A blanking capacitor is connected from the blanking pin to $\mathrm{V}_{\mathrm{EE}}$. The stray capacitance on the blanking pin provides a very small level of blanking if left open. The blanking pin should not be grounded when using current sensing, that would disable the sense. The blanking pin should never be tied high, that would short out the clamp transistor.


Figure 37. Sense IGBT Application

## CS1112

## Quad Power Output Driver

The CS1112 is a Power Output Driver. The IC incorporates four protected DMOS low-side drivers designed to drive inductive and resistive loads in an automotive environment. The outputs are controlled by an 8-bit serial peripheral interface (SPI) or its associated parallel input. Each output contains overcurrent protection, open load detection, and inductive flyback clamps. The device is overvoltage protected. Overcurrent and open load faults are reported over the SPI port, and at the STATUS lead.

## I/O Control

SPI communication is initiated by asserting CSB low. Data at the SI lead is transferred on the rising edge of SCLK. The MSB is transferred first. The outputs become active at the rising edge of CSB. Diagnostic status bits are transferred out the SO lead at the falling edge of SCLK. The SO lead is high impedance while CSB is high. An open drain output, (STATUS) reports a fault (short to $\mathrm{V}_{\mathrm{PWR}}$, GND, or open load) has occurred at one or more of the outputs.

## Protection

Each output independently detects shorts to $V_{\text {PWR }}$ while the output is "on" and open load/short to ground while the output is "off". The fault register will be set if a fault occurs at the output. The fault register will be reset if the fault condition is removed from the output. The fault data is latched when CSB is asserted low.

If an overcurrent condition or short circuit to $V_{\text {BATT }}$ occurs, the output goes into a low duty cycle mode for the duration of the fault. The outputs are disabled during an overvoltage or undervoltage condition.

## Features

- 4.0 MHz Serial Input Bus
- Parallel Input Control
- $1.0 \Omega$ DMOS Drivers (typ)
- Power On Reset
- Internal Flyback Clamps
- Status Output
- Fault Protection
- 46 V Peak Transient
- Power Limiting
- Undervoltage
- Overvoltage
- Fault Reporting
- Open Load
- Short Circuit
- 8 Internally Fused Leads

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SO-24L DW SUFFIX CASE 751E

## PIN CONNECTIONS AND MARKING DIAGRAM



$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS1112YDWF24 | SO-24L | 31 Units/Rail |
| CS1112YDWFR24 | SO-24L | 1000 Tape \& Reel |

## CS1112

## APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| DC Supply ( $\mathrm{V}_{\text {PWR }}$ ) | -0.3 to 30 | V |
| Output DC Voltage (Out 0, 1, 2, 3) | 46 | V |
| $V_{\text {DD }}$ Supply Voltage | -0.3 to +7.0 | V |
| Peak Transient ( 1.0 ms rise time, 300 ms period, 32 V Load Dump @ $14 \mathrm{~V} \mathrm{~V}_{\text {PWR }}$ ) | 46 | V |
| Digital Input Voltage | -0.3 to $\mathrm{V}_{\mathrm{DD}}+0.3$ | V |
| Single Pulse Avalanche Energy ( $\mathrm{I}=450 \mathrm{~mA}$ )(Out 0, 1, 2, 3) | 50 | mJ |
| Operating Junction Temperature, $\mathrm{T}_{J}$ | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Capability (Human Body Model) | 1.5 | kV |
| Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{PWR}}<17 \mathrm{~V}, 4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{DD}}<5.5 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$,
$5.5 \mathrm{~V}<\mathrm{V}_{\text {PWR }}<25 \mathrm{~V}$, (Outputs Functional); unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltages and Currents |  |  |  |  |  |
| V ${ }_{\text {DD }}$ Power On Reset Threshold | Outputs Latched Off By Event | 2.5 | 3.0 | 3.5 | V |
| $V_{\text {DD }}$ Power On Reset Hysteresis | - | - | 200 | - | mV |
| $\mathrm{V}_{\text {PWR }}$ Undervoltage | Outputs Latched Off By Event | 4.0 | 4.5 | 5.0 | V |
| $\mathrm{V}_{\text {PWR }}$ Overvoltage Lockout | Outputs Latched Off By Event | 30 | 35 | 45 | V |
| Digital Supply Current, IV(DD) | All Outputs On (@350 mA) | - | - | 5.0 | mA |
| Analog Supply Current, IV(PWR) | All Outputs On (@350 mA) | - | - | 5.0 | mA |
| Sleep Current, $\mathrm{I}_{\mathrm{V} \text { (PWR) }}$ | $\mathrm{V}_{\mathrm{DD}} \leq 0.5 \mathrm{~V}$ | - | - | 10 | $\mu \mathrm{A}$ |

Digital Inputs and Outputs

| $V_{\text {IN }}$ High | SI, SCLK, CSB, INO, IN1, IN2, IN3 | 70 | - | - | \% $\mathrm{V}_{\mathrm{DD}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IN }}$ Low | SI, SCLK, CSB, INO, IN1, IN2, IN3 | - | - | 30 | \% $\mathrm{V}_{\mathrm{DD}}$ |
| $\mathrm{V}_{\text {IN }}$ Hysteresis | - | - | 230 | - | mV |
| Input Pulldown Current | SI, INO, IN1, IN2, IN3, $\mathrm{V}_{\text {IN }}=30 \% \mathrm{~V}_{\mathrm{DD}}$ | - | - | 25 | $\mu \mathrm{A}$ |
| Input Pullup Current | $C S B, V_{I N}=70 \% V_{D D}$ | - | - | -25 | $\mu \mathrm{A}$ |
| Status Low | $\mathrm{I}_{\text {STATUS }}=0.5 \mathrm{~mA}$ | - | 0.1 | 0.5 | V |

Fault Detection/Timing

| Overcurrent Sense Time, tss | Overcurrent Sense Time, R $\mathrm{OSC}=82 \mathrm{k} \Omega$ | 25 | 62.5 | 100 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Overcurrent Shutdown Time | Overcurrent Shutdown Time, R $\mathrm{OSC}=82 \mathrm{k} \Omega$ | 1.60 | 3.94 | 6.3 | ms |
| Fault Duty Cycle | After the first fault cycle, Note 1 | 1.4 | 1.56 | 1.7 | $\%$ |
| Open Load Trip Point | IN = Low | 40 | 50 | 60 | $\% \mathrm{~V}_{\mathrm{DD}}$ |
| Open Load Sense Time | Open Load Sense Time, R $\mathrm{OSC}=82 \mathrm{k} \Omega$ | 12.5 | - | 100 | $\mu \mathrm{~s}$ |

Power Outputs

| $V_{\text {Drain }}$ Clamp | $\mathrm{I}_{\mathrm{D}}=20 \mathrm{~mA}, \mathrm{t}$ CLAMP $=100 \mu \mathrm{~s}$ | 48 | 52 | 64 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drain Leakage Current | $V_{\text {DRAIN }}=17 \mathrm{~V}$ | - | - | 25 | $\mu \mathrm{A}$ |
| Drain Leakage Current | $V_{\text {drain }}=46 \mathrm{~V}$ | - | - | 400 | $\mu \mathrm{A}$ |
| $\mathrm{R}_{\mathrm{DS} \text { (ON) }}$ | $\mathrm{V}_{\text {PWR }}=13 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=0.5 \mathrm{~A}$ | - | 1.0 | 2.0 | $\Omega$ |
| Current Limit | Note 2 | 3.0 | 4.5 | 6.0 | A |
| Reverse Diode Drop | Reverse Diode Drop I = 350 mA | - | - | 1.4 | V |
| Fall Time Delay, $\mathrm{t}_{\text {phl }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{PWR}}=13 \mathrm{~V}, \mathrm{R}_{\mathrm{LOAD}}=33 \Omega, \\ & \text { Note } 3 \text { (see Figure 2) } \end{aligned}$ | - | - | 10 | $\mu \mathrm{S}$ |
| Rise Time Delay, ${ }_{\text {tplh }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{PWR}}=13 \mathrm{~V}, \mathrm{R}_{\mathrm{LOAD}}=33 \Omega, \\ & \text { Note } 3 \text { (see Figure 2) } \end{aligned}$ | - | - | 15 | $\mu \mathrm{S}$ |
| Rise Time, $\mathrm{t}_{\mathrm{r}}$ | $\mathrm{V}_{\text {PWR }}=13 \mathrm{~V}, \mathrm{R}_{\text {LOAD }}=33 \Omega$ | 0.4 | - | 10 | $\mu \mathrm{s}$ |
| Fall Time, $\mathrm{t}_{\mathrm{f}}$ | $\mathrm{V}_{\text {PWR }}=13 \mathrm{~V}, \mathrm{R}_{\text {LOAD }}=33 \Omega$ | 0.4 | - | 10 | $\mu \mathrm{s}$ |

1. Guaranteed by design.
2. A duty cycle mode will initiate at a minimum of 1.0 A and before the current limit.
3. Output turn on delay and turn off delay from rising edge of CSB to the output reaching $50 \%$ of $\mathrm{V}_{\text {PWR }}$.

## CS1112

ELECTRICAL CHARACTERISTICS (continued) ( $9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{PWR}}<17 \mathrm{~V}, 4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{DD}}<5.5 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C}$,
$5.5 \mathrm{~V}<\mathrm{V}_{\mathrm{PWR}}<25 \mathrm{~V}$, (Outputs Functional); unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Serial Peripheral Interface | $\mathrm{V}_{\text {PWR }}=14 \mathrm{~V}$ |  |  |  |  |
| SCLK Clock Period | $\mathrm{C}_{\mathrm{O}}=200 \mathrm{pF}$ | 250 | - | - | ns |
| MAX Input Capacitance | SI, SCLK, Note 1 | - | - | 12 | pF |
| $V_{\text {Out }}$ High | $\mathrm{SO}, \mathrm{I} \mathrm{I}_{\mathrm{OH}}=1.0 \mathrm{~mA}$ | $V_{D D}-1.0$ | - | - | V |
| V OUT Low | $\mathrm{SO}, \mathrm{IOL}=1.0 \mathrm{~mA}$ | - | - | 0.5 | V |
| SCLK High Time | $\begin{aligned} & \mathrm{F}_{\text {SCLK }}=4.0 \mathrm{MHz}, \mathrm{SCLK}=2.0 \mathrm{~V} \text { to } 2.0 \mathrm{~V} \\ & \text { (see Figure 1) } \end{aligned}$ | 125 | - | - | ns |
| SCLK Low Time | $\begin{aligned} & \text { FSCLK }=4.0 \mathrm{MHz}, \mathrm{SCLK}=0.8 \mathrm{~V} \text { to } 0.8 \mathrm{~V} \\ & \text { (see Figure 1) } \end{aligned}$ | 125 | - | - | ns |
| SI Setup Time | $\begin{aligned} & \mathrm{SI}=0.8 \mathrm{~V} / 2.0 \mathrm{~V} \text { to } \mathrm{SCLK}=2.0 \mathrm{~V} \text { at } 4.0 \mathrm{MHz} \text {; } \\ & \text { Note } 1 \text { (see Figure 1) } \end{aligned}$ | 25 | - | - | ns |
| SI Hold Time | $\mathrm{SCLK}=2.0 \mathrm{~V}$ to $\mathrm{SI}=0.8 \mathrm{~V} / 2.0 \mathrm{~V}$ at 4.0 MHz ; <br> Note 1 (see Figure 1) | 25 | - | - | ns |
| SO Rise Time | $\begin{aligned} & \mathrm{C}_{\mathrm{LD}}=200 \mathrm{pF}\left(0.1 \mathrm{~V} \mathrm{DD} \text { to } 0.9 \mathrm{~V}_{\mathrm{DD}}\right) ; \\ & \text { Note } 1 \end{aligned}$ | - | 25 | 50 | ns |
| SO Fall Time | $\begin{aligned} & \mathrm{C}_{\mathrm{LD}}=200 \mathrm{pF}\left(0.9 \mathrm{~V}_{\mathrm{DD}} \text { to } 0.1 \mathrm{~V}_{\mathrm{DD}}\right) ; \\ & \text { Note } 1 \end{aligned}$ | - | - | 50 | ns |
| CSB Setup Time | $\begin{aligned} & \mathrm{CSB}=0.8 \mathrm{~V} \text { to } \mathrm{SCLK}=2.0 \mathrm{~V} \\ & \text { (see Figure 1) Note } 1 \end{aligned}$ | 60 | - | - | ns |
| CSB Hold Time | $\begin{aligned} & \mathrm{SCLK}=0.8 \mathrm{~V} \text { to } \mathrm{CSB}=2.0 \mathrm{~V} \\ & \text { (see Figure 1) Note } 1 \end{aligned}$ | 75 | - | - | ns |
| SO Delay Time | $\begin{aligned} & \text { SCLK }=0.8 \mathrm{~V} \text { to } \mathrm{SO} \text { Data Valid, } \mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V} \\ & \mathrm{C}_{\mathrm{LD}}=200 \mathrm{pF} \text { at } 4.0 \mathrm{MHz} \\ & \text { (see Figure 1); Note } 1 \end{aligned}$ | - | 65 | 125 | ns |
| Xfer Delay Time | CSB rising edge to next falling edge. Note 1 | 1.0 | - | - | $\mu \mathrm{s}$ |

1. Guaranteed by design.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| 24 Lead SOIC | PIN SYMBOL |  |
| 1 | $V_{\text {DD }}$ | FUNCTION |
| 2 | V PWR | Input voltage to bias logic and control circuitry. |
| 3 | OUT0 | Input voltage to bias gate drive circuitry. |
| 4 | INO | Open drain output one. |
| $5,6,7,8$ |  |  |
| $17,18,19,20$ | GND | Parallel input one. |
| 9 | IN1 | Ground Reference. |
| 10 | OUT1 | Parallel input two. |
| 11 | SI | Open drain output two. |
| 12 | CSB | SPI serial input. |
| 13 | SCLK | SPI active low chip select. |
| 14 | SO | SPI clock input. |

PACKAGE PIN DESCRIPTION (continued)

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| 24 Lead SOIC | PIN SYMBOL |  |
| 15 | OUT2 | Open drain output three. |
| 16 | IN2 | Parallel input three. |
| 21 | IN3 | Parallel input four. |
| 22 | OUT3 | Open drain output four. |
| 23 | STATUS | Open drain output, which is asserted when an open load or <br> overcurrent condition occurs at any of the outputs. |
| 24 | ROSC | $82 \mathrm{k} \Omega$ resistor tied to ground to set up accurate internal cur- <br> rent sources. |

## CIRCUIT DESCRIPTION

## Typical Operation

Control of the CS1112 can be done using the Serial Peripheral Interface (SPI) port using the Data Input information in Table 1, or the outputs can be controlled via the parallel inputs (IN0, IN1, IN2, IN3). IN0 controls OUT0, IN1 controls OUT1, IN2 controls OUT2, and IN3 controls

OUT3. Turning the output drivers on is an OR function with the SPI input and the parallel inputs.

Note: To prevent damage to the IC or the output load, $\mathrm{V}_{\mathrm{DD}}$ must be above the Power on Reset threshold ( 3.5 V ) before IN0, IN1, IN2, or IN3 are asserted high ( $<70 \% \mathrm{~V}_{\mathrm{DD}}$ ).

TIMING DIAGRAM


Table 1. SPI Inputs

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| X | X | X | X | OUT3 | OUT2 | OUT1 | OUT0 |

[^41]SERIAL PERIPHERAL INTERFACE TIMING REQUIREMENTS


Figure 1.


Figure 2.

## BLOCK DIAGRAM



## APPLICATION INFORMATION

## CIRCUIT DESCRIPTION

The CS1112 was developed for use in very noisy and very harsh environments such as seen in an automobile system. The device has four low-side switches all controlled through an 8-bit Serial Peripheral Interface (SPI) port. Control of the outputs is also OR'd with parallel inputs. This is a critical feature enhancement over similar devices because of the ease in which the parallel inputs can be used to control the outputs in a Pulse Width Modulation (PWM) mode. Creating a PWM mode using just the serial port input is not a practical application.

This part uses ON Semiconductor's POWERSENSE ${ }^{\text {TM }}$ process technology. POWERSENSE combines the robustness of Bipolar with the dense logic capability of CMOS, and the power capabilities of DMOS.

Power consumption is kept to a minimum using POWERSENSE in comparison to a bipolar technology. A bipolar process requires DC bias currents to power-up the integrated circuit. This is needed in many applications requiring analog circuitry, but is not needed here. Digital POWERSENSE logic dissipates power only when switching because that is when transient gate charging current flows. POWERSENSE logic requires little space, and is a good economical solution. The DMOS side of the process provides a robust user interface to the outside world on each of the outputs. Peak transient capability of each output is rated at a maximum of 46 V (typical of an automotive load dump transient).

The CS1112 uses quasi-vertical DMOS transistors resulting in an output resistance $\left(\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}\right)$ at each output of less than $1.0 \Omega @ 13 \mathrm{~V}$ and $500 \mathrm{~mA} @ 25^{\circ} \mathrm{C}$.

The part can be put in a sleep mode where the part draws less than $2.0 \mu \mathrm{~A}$ of bias current from $\mathrm{V}_{\text {PWR. }}$. The part enters this sleep mode when $\mathrm{V}_{\mathrm{DD}} \leq 0.5 \mathrm{~V}$. Maximum quiescent current for the device is 5.0 mA maximum for any combination of output drivers enabled.

Fault reporting is controlled by the CS1112. Overcurrent and short to $\mathrm{V}_{\text {BATT }}$ are detected when the output is on. Open load and short to ground are detected when the output is off. Faults are reported out of the serial output (SO) pin as a new 8 -bit word is being fed into the serial input (SI) pin.

Figure 3 highlights the SPI interface between the microprocessor and the CS1112. The SPI control inputs and all other logic inputs are compatible with 5.0 V CMOS logic levels.


Figure 3.
The four communication lines which define the SPI interface are the SI, SO, CSB, and SCLK. The parallel inputs, which control the outputs can also connect to the same microprocessor, a separate microprocessor, or any other sensor or electrical device which meets the voltage requirements of the $\operatorname{CS} 1112\left(\mathrm{~V}_{\mathrm{IN}(\max )}=\mathrm{V}_{\mathrm{DD}}+0.3 \mathrm{~V}\right)$.

SPI communication is as follows (2 scenarios):

## 1. 8-Bit Normal Operation

CSB pin is brought low activating the SPI port. Faults detected since the last CSB low to high transition are latched into the serial register when CSB goes low. 8 command bits are clocked into the SI pin. The four fault bits are clocked out of the SO pin. CSB pin is brought high translating the final 4 bits to the outputs turning them on or off. Faults are then detected and saved in the fault register when CSB goes low.
2. 16-Bit Operation For Command Verify

CSB pin is brought low activating the SPI port. 16 bits are clocked into the SI pin (the last 4 are the 4 control pins for the four outputs). CSB pin is brought high translating the last 4 bits to the outputs turning them on or off.
CSB pin is brought low activating the SPI port. 16 new bits are clocked into the SI pin. As the new bits are being clocked in, the first 8 bits being clocked out of the SO pin are the fault bits, followed by the first 8 bits which were clocked in (the verification bits). The verification bits should replicate the command bits.
Serial clock frequencies up to 4.0 MHz can be used by the CS1112.

Internal pull-up circuitry is provided on the Chip Select Bar (CSB) pin. Internal active pulldowns are provided on the parallel input pins (IN0, IN1, IN2, IN3, and SI pin).

A product highlight of this part is its ability to be daisy-chained with other parts which follow the SPI protocol as defined in Figure 1. Figure 4 displays this aspect. The serial output of each device is fed into the serial input of the next device. All data bits are clocked into their respective registers, while the CSB pin is low. The drivers are switched to the resulting command when the CSB pin is brought back high.


Figure 4.
Multiple SPI port devices can also be connected in a parallel fashion (Figure 5) instead of the daisy-chained connection previously shown. The microprocessor controls the CS1112 in a multiplex fashion allowing the serial data input to be input to the device when the device is activated through the CSB pin. This creates a system whose number of outputs is a multiple of 4 . Figure 5 displays a 12 output setup.


Figure 5.
Figure 6 displays the device controlling 4 outputs with the use of its SPI port. Figure 7 displays the device controlling 1 output with the SPI port, and 3 outputs being controlled
with the parallel inputs allowing them to run in a PWM mode.


Figure 6.


Figure 7.
The CS1112 provides a very efficient way of controlling 4 output drivers by minimizing the number of I/O pins through use of the SPI port, and still provides the flexibility of pulse width modulating the output drivers where needed. The use of the SPI also allows the integrated circuit to communicate directly with the microprocessor.

While designed for an automotive environment, the CS1112 can be used in other applications in the computer market, industrial market, telecommunications market, or any other instance where numerous drivers are needed. All parts are $100 \%$ tested and guaranteed to meet all parameters specified in the electrical characteristics. These specifications cover the entire voltage range for $\mathrm{V}_{\mathrm{PWR}}$ (9.0 V to 17 V ), and $\mathrm{V}_{\mathrm{DD}}(4.5 \mathrm{~V}$ to 5.5 V$)$.

## FAULT MODE OPERATION

The CS1112 provides protection for a multitude of system faults and conditions. These include Overvoltage, Current Limit, Open Circuit, Output Short to Power, Output Short to Ground, and Flyback Clamp.

## Overvoltage

The IC is constantly monitoring the voltage on the VPWR pin. If the voltage on this pin exceeds the Overvoltage Shutdown Threshold (typically 35 V ), all outputs immediately turn off. The programmed outputs (via serial or parallel input) turn back on once the voltage is brought back down below this level.

## Current Limit/Short to $\mathrm{V}_{\text {BATT }}$

When the output current exceeds the Overcurrent (4.5 A typical) for the Short Circuit/Overcurrent Sense Time (typically $62.5 \mu \mathrm{~s}$ ) as it would do during an output short to $\mathrm{V}_{\text {BATT }}$, its fault status bit will be latched to a logic one. The fault status bit remains latched until the rising edge of CSB. The output will go into a low duty cycle mode (typically $1.56 \%$ ) as long as the overcurrent condition exists, and the channel is on. This protects the integrated circuit from damaging itself due to its thermal limits.

## Open Circuit/Short to Ground

Open circuit conditions are detected while the outputs are off. A fault bit is set when the Open Load "Off" Detection Voltage (typically $0.5 \times \mathrm{V}_{\mathrm{DD}}$ ) is present for the Open Load "Off" Sense Time (typically $62.5 \mu \mathrm{~s}$ ) as it would do during an output short to ground.

## Flyback Clamp

While the flyback clamp is not a fault mode, it is a protection feature of the CS1112. When driving inductive loads, it is normal to observe high voltage spikes on the output pin due to the stored energy in the windings when the device is turned off. On-chip clamps on the outputs limit the voltage amplitude on the pin to prevent damage to the device. Each output has an Output Clamp which limits the output voltage to 52 V (typical when measured at 20 mA for $100 \mu \mathrm{~s}$ ).

## PIN FUNCTION DESCRIPTION

## SI

The SI (Serial Input) receives serial 8-bit or 16-bit words sent most significant bit first. Data is clocked in on the rising edge of SCLK. An internal active pull-down is connected to this input. CMOS logic levels are required on this pin.

## SO

The SO (Serial Output) can be connected to the serial data input pin of the microprocessor, or it can be daisy-chained to the serial input (SI) of another SPI compatible device. This pin is tri-stated unless a low CSB pin selects the device.

The signal on this pin is clocked from the falling edge of the SCLK pin. The serial output data provides fault information for each output and returns most significant bit (bit 7) first. Bits 0 through 3 are output fault bits for outputs 0 through 3 , respectively. In 8 -bit SPI mode, bits $0-3$, under normal conditions return all zeros representing no faults. A 1 indicates a fault. The output from this pin conforms to CMOS logic levels.

## Rosc

An $82 \mathrm{k} \Omega$ resistor tied to ground sets up an accurate internal current source.

## CSB

The CSB (Chip Select Bar) is the select pin when the microprocessor wants to communicate with the CS1112. A low on this pin enables the SPI communication with the device and enables the SO pin. After the digital word is clocked into the IC, a transition from low to high on the CSB pin translates the last 4 bits of information turning the outputs on or off. An internal active pull-up is connected to this input. CMOS logic levels are required on this pin.

## SCLK

The SCLK (Serial Clock) clocks the internal shift registers. This pin controls the data being shifted into the SI pin, and data being shifted out of the SO pin. CMOS logic levels are required on this pin.

## INO, IN1, IN2, IN3

These pins control their corresponding numbered output. These are the parallel input pins which may be used to PWM the outputs. They have 230 mV of hysteresis. These inputs are OR'd with their corresponding input bit in the serial control byte. An internal active pull-down is connected to these pins. CMOS logic levels are required on these pins.

## OUTO, OUT1, OUT2, OUT3

These pins are the output low-side driver pins. They all have typically $1.0 \Omega \mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ at $\mathrm{V}_{\mathrm{PWR}}=13 \mathrm{~V}$. Current limit on these pins has a minimum specification of 3.0 A . A low duty cycle mode ( $1.5 \%$ typ.) will initiate at a minimum of 1 A and before the current limit.

## $V_{\text {PWR }}$

14 V Battery voltage input. $5.0 \mathrm{~mA}(\max )$ is needed.
$V_{D D}$
5.0 V Supply input. 5.0 mA (max) is needed.

## STATUS

Open drain output. This pin goes low when an open load or overcurrent condition occurs on any of the outputs. This provides immediate notification to the controller that a fault is present. The controller can subsequently query the device (serially) to determine its origin.

## CS1112

PACKAGE THERMAL DATA

| Parameter |  | SO-24L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS1107

## Single Relay Driver IC

This ASIC provides up to 350 mA of drive current for driving a relay. On-chip diagnostic features include open and short circuit detection in the on state, duty cycle current limit control, and thermal shutdown. Faults are reported on the Fault lead. Fault is an active-low output. An on-chip zener provides protection from flyback pulses from the relay. Internal pull-down circuitry is provided to ensure the output pin turns off when the Control pin is floating.

## Features

- Fault Detection
- Open Circuit
- Short Circuit
- Overtemperature
- On-Chip Flyback Protection
- Low Standby Current
- Internally Fused Leads in SO-8 Package


Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Storage Temperature |  | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\mathrm{CC}}$, $\overline{\text { Fault, }}$, Control |  | -0.5 to 6.0 | V |
| ESD Capability (Human Body Model) |  | 2.0 | kV |
| Peak Transient Voltage (output off mode, output pin only) | (26 V Load Dump @ 14 V V ${ }_{\text {BAT }}$ ) | 40 | V |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(4.75 \leq \mathrm{V}_{\mathrm{CC}} \leq 5.25 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Requirements |  |  |  |  |  |
| $\mathrm{V}_{\text {CC }}$ Quiescent Current | Output ON | - | 3.0 | 6.0 | mA |
| $\mathrm{V}_{\text {CC }}$ Quiescent Current | Output OFF | - | 70 | 250 | $\mu \mathrm{A}$ |

## Output

| Leakage Current | $\mathrm{V}_{\text {BAT }}=14 \mathrm{~V}$ | - | 0 | 100 | $\mu \mathrm{~A}$ |
| :--- | :--- | :--- | :--- | :---: | :---: |
| Saturation Voltage | IOUTPUT $=350 \mathrm{~mA}$ | - | 1.1 | 1.5 | V |
|  | IOUTPUT $=180 \mathrm{~mA}$ | - | 0.9 | 1.3 | V |
| $\mathrm{~V}_{\text {CLAMP }}$ | $\mathrm{V}_{\text {CC }}<4.5 \mathrm{~V}$, I OUTPUT $=180 \mathrm{~mA}$ | 29 | 33 | 36 | V |

Current Sense

| Short Circuit Current | - | 350 | 500 | 650 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Open Circuit Current | Output in the ON state | 20 | 40 | 60 | mA |

## Control-Input

| Input Voltage | Logic $=$ High <br> Logic $=$ Low | 2.0 <br> - | - <br> - | 0.8 |  |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Current | Control $=\mathrm{V}_{\mathrm{CC}}$ | - | 40 | 80 | $\mu \mathrm{~A}$ |

Fault Output - (Open Collector)

| Output Low Voltage | $\mathrm{I}_{\text {FAULT }}=250 \mu \mathrm{~A}$ (sink) | - | 0.24 | 0.40 | V |
| :--- | :--- | :--- | :--- | :--- | :---: | :---: |

## Overtemperature Shutdown

| $T_{J}$ Output Disable Threshold | (Guaranteed by Design) | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{T}_{\boldsymbol{J}}$ Hysteresis | (Guaranteed by Design) | 5.0 | - | - | ${ }^{\circ} \mathrm{C}$ |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| 8 Lead SO Narrow | PIN SYMBOL |  |
| 1 | Output | Open collector output. |
| 2 | $V_{\mathrm{CC}}$ | 5.0 V regulated supply input. |
| 3 | Fault | Open collector diagnostic output low during open load, short <br> circuit and overtemperature conditions. |
| 4 | Control | TTL compatible input. A high on this pin turns the output on. |
| $5,6,7,8$ | Ground | Signal ground. |

## CS1107

## CIRCUIT DESCRIPTION

The CS1107 relay driver IC provides up to 350 mA of drive current in a low-side configuration. The Output driver pin is controlled through the TTL compatible Control input pin. A high condition on the Control pin turns the output pin on.

The Fault pin reports short circuit, open circuit, and overtemperature conditions on the IC. If a fault is present, the open collector output $\overline{\text { Fault }}$ pin will be low. Typical numbers for faults are: exceeding 500 mA of drive current will report a short circuit. Less than 40 mA (typical) will report an open circuit. A temperature fault will be reported when the die temperature exceeds $180^{\circ} \mathrm{C}$ (typical). Faults
are only reported when the Control pin is high, due to the low quiescent current when the Control pin is low and the output device is turned off.
Overcurrent protection is provided by duty cycle control. When the Output current exceeds the current limit threshold, the output enters duty cycle mode to reduce power dissipation of the IC to a safe level. The higher the threshold is exceeded the lower the duty cycle becomes.
A 33 V on-chip zener diode on the Output pin protects the device from flyback pulses when a relay is turned off. The saturation voltage of this pin will not exceed 1.5 V at 350 mA .


Figure 2. Applications Diagram

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 25 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 110 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS1108

## Single Lamp Driver IC

This ASIC provides up to 350 mA of drive current for powering bulbs. The typical application for this part is for use in airbag systems using a type 194 bulb. On-chip diagnostics provide open circuit and short circuit detection in the output on mode. In addition, the output driver will turn on (sink current) when $\mathrm{V}_{\mathrm{CC}}$ is low. $\overline{\text { Fault }}$ is an active-low output which reports in the output-on mode. Internal pull-up circuitry is provided to ensure the output pin turns on when the Control pin is floating.

## Features

- Fault Detection
- Open Circuit
- Short Circuit
- Overtemperature
- $\mathrm{V}_{\mathrm{CC}}$ Sense: Output Turns On with Loss of $\mathrm{V}_{\mathrm{CC}}$
- Low Standby Current
- Internally Fused Leads in SO-8 Package


Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Storage Temperature | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {CC }}$, Fault, Control | $\left(26 \mathrm{~V}\right.$ Load Dump @ $\left.14 \mathrm{~V} \mathrm{~V}_{\mathrm{BAT}}\right)$ | -0.5 to 6.0 |
| ESD Capability (Human Body Model) | V |  |
| Peak Transient Voltage (output off mode, output pin only) | Reflow: (SMD styles only) (Note 1) | 2.0 |
| Lead Temperature Soldering: |  | kV |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(4.75 \leq \mathrm{V}_{\mathrm{CC}} \leq 5.25 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 150^{\circ} \mathrm{C}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Requirements |  |  |  |  |  |
| $\mathrm{V}_{\text {CC }}$ Quiescent Current | Output ON | - | 3.0 | 6.0 | mA |
| $V_{C C}$ Quiescent Current | Output OFF | - | 100 | 250 | $\mu \mathrm{A}$ |

## Output

| Leakage Current | $\mathrm{V}_{\text {BAT }}=14 \mathrm{~V}$ | - | 16 | 100 | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Saturation Voltage | IOUTPUT $=350 \mathrm{~mA}$ | - | 1.1 | 1.5 | V |
|  | IOUTPUT $=180 \mathrm{~mA}$ | - | 0.9 | 1.3 | V |
| $\mathrm{V}_{\text {OUTPUT }}$ (self-bias) | $\mathrm{V}_{\mathrm{CC}}<4.5 \mathrm{~V}$, IOUTPUT $<200 \mathrm{~mA}$ | - | - | 3.5 | V |

## Current Sense

| Short Circuit Current | - | 350 | 500 | 650 | mA |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Open Circuit Current | Output in the ON state | 20 | 40 | 60 | mA |


| Control-Input |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Voltage | $\begin{aligned} & \text { Logic }=\text { High } \\ & \text { Logic }=\text { Low } \end{aligned}$ | 2.0 - | - | ${ }_{0}^{-}$ | V |
| Input Current | $\begin{aligned} & \text { Logic }=V_{C C} \\ & \text { Logic }=0 \mathrm{~V} \end{aligned}$ | $-\overline{-50}$ | $\begin{gathered} 20 \\ -20 \end{gathered}$ | 40 | $\begin{aligned} & \mu \mathrm{A} \\ & \mu \mathrm{~A} \end{aligned}$ |

Fault Output - (Open Collector)

| Output Low Voltage | $\mathrm{I}_{\text {FAULT }}=250 \mu \mathrm{~A}$ (sink) | - | 0.24 | 0.40 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |

## Overtemperature Shutdown

| $T_{J}$ Output Disable Threshold | (Guaranteed by Design) | 150 | 180 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $T_{J}$ Hysteresis | (Guaranteed by Design) | 5.0 | - | - | ${ }^{\circ} \mathrm{C}$ |

Note: A fault signal will be shown (at the fault pin) during inrush as the short circuit threshold is exceeded.

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| 8 Lead SO Narrow | PIN SYMBOL |  |
| 1 | Output | Open collector output. |
| 2 | VCC $_{\text {CC }}$ | Fault |
| 3 | Control | Open collector diagnostic output low during open load, short <br> circuit and overtemperature conditions. |
| 4 | Ground | TTL compatible input. |
| $5,6,7,8$ | Signal ground. |  |

## CIRCUIT DESCRIPTION

The CS1108 lamp driver IC provides up to 350 mA of drive current in a low-side configuration. The Output driver pin is controlled through the TTL compatible Control input pin. A high condition on the Control pin turns the output pin on.

The Fault pin reports short circuit, open circuit, and overtemperature conditions on the IC. If a fault is present, the open collector output $\overline{\text { Fault }}$ pin will be low. Typical numbers for faults are: exceeding 500 mA of drive current will report a short circuit. Less than 40 mA (typical) will report an open circuit. A temperature fault will be reported when the die temperature exceeds $180^{\circ} \mathrm{C}$ (typical). Faults are only reported when the Control pin is high, due to the low quiescent current when the Control pin is low and the output device is turned off.

The CS1108 is designed to provide overcurrent protection by duty cycle control. When the lamp current exceeds the internally programmed current limit threshold (typically 500 mA ), the output enters duty cycle mode to reduce power dissipation of the IC to a safe level.

Typical lamps have a low resistance when off and the current will exceed the current limit threshold during the initial inrush period. During this inrush time, the IC will be operating in the duty cycle mode. Due to characteristics of lamps in this mode, they may appear dimly lit. This condition will persist for a breif time until the lamp resistance has increased enough to reduce it's current below the threshold. Once this occurs the lamp will appear at full brightness. During the inrush period the Fault pin will be forced low indicating that duty cycle mode is in operation.

Thermal protection has been designed into this IC. Should duty cycle mode operate for an extended amount of time and the power limitations of the IC are exceeded the IC die temperature will rise. Once the die temperature reaches the thermal temperature limit, the internal cicuitry will shutoff the output and the lamp will turn off. Once the die temperature lowers below the thermal threshold, the output will be allowed to turn back on.


Figure 2. Applications Diagram

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | Unit |
| :--- | :--- | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 25 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 110 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS299

## Darlington Lamp Driver

This integrated circuit is a flip chip lamp driver for use in an automotive alternator system. The circuit drives an indicator lamp located on the dashboard. Reverse battery protection is provided with internal diode, D1, and external resistance on $\mathrm{B}, \mathrm{C} 1, \mathrm{C} 2$.

## Features

- DC Current Gain 1000
- 80 V Breakdown Voltage




## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com

PIN CONNECTIONS

Flip Chip


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS299H | Flip Chip | Contact Sales |

## MAXIMUM RATINGS*

|  | Rating | Value |
| :--- | :---: | :---: |
| Unit |  |  |
| Storage Temperature Range, $T_{S}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Ambient Operating Temperature | -40 to 140 | ${ }^{\circ} \mathrm{C}$ |
| Collector Breakdown Voltage | 80 | V |

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Supply Requirements

| Saturation Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{B} 1}=0.6 \mathrm{~mA}, \mathrm{I}_{\mathrm{C} 2}=350 \mathrm{~mA} \\ & \mathrm{~T}_{\mathrm{J}}=-30^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{J}}=150^{\circ} \mathrm{C} \end{aligned}$ | - | - | $\begin{aligned} & 0.60 \\ & 0.55 \\ & 0.65 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \\ & \text { V } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Collector Breakdown Voltage | $\mathrm{I}_{\mathrm{C} 1}=\mathrm{I}_{\mathrm{C} 2}=1.0 \mathrm{~mA}, \mathrm{R}_{\mathrm{BE}}=200, \mathrm{~V}_{\mathrm{C} 1}=\mathrm{V}_{\mathrm{C} 2}$ | 80 | - | - | V |
| Collector Cut Off Current (lceo) | $\mathrm{V}_{\mathrm{CE} 1}=\mathrm{V}_{\mathrm{CE} 2}=60 \mathrm{~V}, \mathrm{R}_{\mathrm{BE}}=200$ | - | - | 10 | $\mu \mathrm{A}$ |
| DC Current Gain (HFE) | $\mathrm{V}_{\mathrm{C} 1}=\mathrm{V}_{\mathrm{C} 2}=1.0 \mathrm{~V}, \mathrm{I}_{\mathrm{B} 1}=100 \mu \mathrm{~A}$ | 1000 | - | - | $\left(I_{C 1}+I_{C 2}\right) I_{\text {B }}$ |
| NPN $\beta$ (Q1) | $\mathrm{I}_{\mathrm{B} 1}=1.0 \mu \mathrm{~A}, \mathrm{~V}_{\text {CE2 }}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE} 1}=1.5 \mathrm{~V}$ | 50 | - | - | $\mathrm{IC}_{\mathrm{C}} / \mathrm{I}_{\mathrm{B} 1}$ |
| $\mathrm{V}_{\mathrm{BE}}$ (in saturation) | $\mathrm{I}_{\mathrm{B} 1}=0.6 \mathrm{~mA}, \mathrm{I}_{\mathrm{C} 1}=50 \mathrm{~mA}, \mathrm{I}_{\mathrm{C} 2}=350 \mathrm{~mA}$ | - | - | 2.0 | V |
| Diode Forward Voltage (D1) | $\mathrm{I}_{\mathrm{D} 1}=25 \mathrm{~mA}$ | 0.5 | - | 1.5 | V |

## PACKAGE PIN DESCRIPTION

| PIN SYMBOL | FUNCTION |
| :---: | :--- |
| B | Base of input darlington. |
| C1 | Collector of darlington input device. |
| C2 | Collector of darlington output driver. |
| GND | Ground. Emitter of dartlington driver. Base/Emitter resistor and substrate are also connected here. |



Figure 2. Typical Application Dlagram


Note: All dimensions are in inches.

Figure 3. Flip Chip Dimensions and Solder Bump Locations, Bump Side Up

## CS8240

## 500 mA High Side (PNP) Driver with On-Chip Flyback Diode

The CS8240 is a fast, PNP high side driver capable of delivering up to 500 mA into a resistive or inductive load in harsh automotive or industrial environments. An internal flyback diode clamp is incorporated for inductive loads. The input ( $\mathrm{V}_{\mathrm{IN}}$ ) is TTL and CMOS compatible and has hysteresis to minimize the effects of noise. When the input is high, the output is on. When the input is low, the output is off and the supply voltage quiescent current is very low ( $<1.0 \mu \mathrm{~A}$, typ). For device protection, the CS8240 incorporates thermal shutdown, short circuit current limiting, overvoltage shutdown, and reverse battery protection. The CS8240 can withstand supply voltage transients of $60 \mathrm{~V}(\mathrm{~min})$ and -50 V .

The CS8240 is available in an overmolded 5 lead TO-220 package and is a competitive replacement for the LM-1921, LM-1951, LM-1952, MC-3399, and L-9350.

## Features

- Low Output Saturation Voltage
-0.22 V at $\mathrm{I}_{\text {OUT }}=125 \mathrm{~mA}$
-0.33 V at $\mathrm{I}_{\text {OUT }}=225 \mathrm{~mA}$
- Overmolded Package
- On-Chip Flyback Diode
- Fault Protection
- Over Voltage Shutdown (32 V, typ)
- Thermal Shutdown ( $165^{\circ} \mathrm{C}$, typ)
- Short Circuit Limiting (1.1 A typ)
- -50 V Reverse Transient Protection
- 60 V Load Dump Protection
- Reverse Battery
- Low Quiescent Current (Off State)
- ESD Protected


Figure 1. Block Diagram

ON Semiconductor ${ }^{\text {w }}$
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MARKING DIAGRAM


A
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS8240YTQ5 | TO-220 <br> FIVE LEAD <br> STRAIGHT | 50 Units/Rail |
| CS8240YTQVA5 | TO-220 <br> FIVE LEAD <br> VERTICAL | 50 Units/Rail |

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage |  | 6.0 to 26 | V |
| Overvoltage Protection |  | 60 | V |
| Reverse Voltage: | DC <br> Transient | $\begin{aligned} & -16 \\ & -50 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Internal Power Dissipation |  | Internally limited | - |
| Logic Input Voltage |  | -0.3 to +7.0 | V |
| Junction Temperature Range, $\mathrm{T}_{J}$ |  | -40 to150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\text {S }}$ |  | -55 to +165 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) | 260 peak | ${ }^{\circ} \mathrm{C}$ |
| Electrostatic Discharge (Human Body Model) |  | 2.0 | kV |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq T_{A} \leq 125^{\circ} \mathrm{C} ;-40^{\circ} \mathrm{C} \leq \mathrm{T}_{J} \leq 150^{\circ} \mathrm{C}\right.$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| General Characteristics |  |  |  |  |  |
| Operating Supply Voltage | - | 6.0 | - | - | V |
| Quiescent Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}} \leq \mathrm{V}_{\operatorname{IN}(\mathrm{LOW})} \\ & \mathrm{V}_{\mathrm{IN}} \geq \mathrm{V}_{\mathrm{IN}(\mathrm{HI}),}, \mathrm{R}_{\mathrm{LOAD}}=50 \Omega, \\ & 6.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 20 \mathrm{~V} \\ & 20 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 24 \mathrm{~V} \end{aligned}$ | - | $\begin{aligned} & 1.0 \\ & 16 \\ & 25 \end{aligned}$ | $\begin{aligned} & 100 \\ & 30 \\ & 50 \end{aligned}$ | $\mu \mathrm{A}$ <br> mA <br> mA |

## Output Stage

| Output Saturation Voltage | $\mathrm{V}_{\mathrm{IN}} \leq \mathrm{V}_{\mathrm{IN}(\mathrm{HII}}, \mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=125 \mathrm{~mA}$ <br> $\mathrm{~V}_{\mathrm{CC}}=14 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=225 \mathrm{~mA}$ | - | 0.22 | 0.5 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Leakage Current | $\mathrm{Input} \leq \mathrm{V}_{\mathrm{IN}(\mathrm{L})}, \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}}=0 \mathrm{~V}$ | - | 1.0 | 150 | $\mu \mathrm{~A}$ |
| Negative Output Clamp | $\mathrm{I}_{\mathrm{CLAMP}}=100 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=12 \mathrm{~V}$ | -18 | -15.5 | -12 | V |
| Turn On Delay Time | $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{I}_{\text {LOAD }}=150 \mathrm{~mA}$ | - | 5.0 | 20 | $\mu \mathrm{~s}$ |
| Turn Off Delay Time | $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{I}_{\mathrm{LOAD}}=150 \mathrm{~mA}$ | - | 5.0 | 20 | $\mu \mathrm{~s}$ |

Input Stage

| Input Voltage | Logic $=$ High, $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ Turn ON | 0.8 | 1.45 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
|  | Logic $=$ Low, $\mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}$ Turn OFF | - | 1.2 | 2.0 | V |
| Input Current | $\mathrm{V}_{\mathrm{IN}}=5.5 \mathrm{~V}$ | - | 100 | 200 | $\mu \mathrm{~A}$ |
|  | $\mathrm{~V}_{\mathrm{IN}}=0.8 \mathrm{~V}$ | - | 15 | 50 | $\mu \mathrm{~A}$ |

## Protection Circuitry

| Overvoltage Shutdown | $\mathrm{V}_{\mathrm{IN}} \geq \mathrm{V}_{\operatorname{IN}(\mathrm{HI})}$ | 26 | 32 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Short Circuit Current | $\mathrm{V}_{\operatorname{IN}} \geq \mathrm{V}_{\operatorname{IN}(\mathrm{HI})}, \mathrm{V}_{\mathrm{CC}}=12 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=0 \mathrm{~V}$ | 0.55 | 1.1 | 2.5 | A |
| Thermal Shutdown | - | 150 | 165 | - | ${ }^{\circ} \mathrm{C}$ |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| 5 Lead TO-220 | PIN SYMBOL | FUNCTION |
| 1 | $\mathrm{V}_{\mathrm{CC}}$ | Supply Voltage to the IC. Supplies load current through PNP. |
| 2 | OUT | Collector of output PNP, current to load is sourced from this lead. |
| 3 | NC | No connection. |
| 4 | GND | Ground. |
| 5 | $\mathrm{V}_{\mathrm{IN}}$ | Input voltage to control output. Logic high turns output on. Logic low turns output off. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Quiescent Current vs. IOUT


Figure 4. Turn Off Delay Time


Figure 3. Turn-On Delay Time


Figure 5. Output Saturation Voltage vs. Iout


Figure 6. Flyback Clamp Characteristics


Figure 7. $\mathrm{I}_{\mathrm{IN}}$ vs. $\mathrm{V}_{\mathrm{IN}}$

## CIRCUIT DESCRIPTION

## Input Stage

The input stage is a self biased band gap based circuit with a positive going trip point of 1.45 V (typ) and a negative going trip point of 1.20 V (typ) ( 250 mV of hysteresis). When the input voltage is below the positive trip point, the quiescent current of the supply voltage line is less than $1.0 \mu \mathrm{~A}$, (typ). When the input voltage exceeds the positive trip point ( 1.45 V , typ), the input stage "wakes up" the rest of the CS8240 circuitry and turns on the output stage.

## Output Stage

The output stage is built around a high current PNP output transistor. A control amplifier monitors the saturation voltage of the output PNP and maintains a balance of low saturation voltage and minimum base drive to the PNP for
the given output current. The base drive of the PNP is the dominant component of the quiescent current of the CS8240 and is dependent on the level of output current.

Short circuit protection ( 1.1 A, typ) is also incorporated in the output stage.

## Protection Circuitry

In addition to the short circuit protection mentioned above, the CS8240 also incorporates a thermal shutdown circuit ( $165^{\circ} \mathrm{C}$, typ) and a high voltage shutdown circuit ( 33 V , typ), both of which cut off the drive to the PNP output transistor when excessive current is drawn. Inherent in the design of the CS8240 is transient protection to +60 V and -50 V on the supply line. The CS8240 is ESD protected in excess of 2.0 kV (Human Body Model).

TYPICAL APPLICATION CIRCUITS


Figure 8. Solenoid Driver

[^42]

Figure 9. Lamp Driver


Figure 10. Controlled High Side Switch

PACKAGE THERMAL DATA

| Parameter |  | TO-220, Five Lead | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 4.0 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## NCV7601

## Quad Driver

This automotive grade product provides a versatile interface between control logic and many types of loads. The inputs accept a wide range of control signal levels while the open-collector outputs feature independent thermal and current limiting. Integral transient suppression diodes are provided at all inputs and outputs.


## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCV7601P | DIP-16 | 25 Units/Rail |



Figure 1. Typical Driver Applications

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
| :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | -0.3 to 7.0 | V |
| Logic Input Voltage (INA, INB, INC, IND, ENABLE) | -0.3 to 15 | V |
| Power Output (OUTA, OUTB, OUTC, OUTD) | -0.3 to 60 | V |
| Junction Temperature Range, $\mathrm{T}_{J}$ | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) | 2.0 | kV |
| $\begin{aligned} & \text { Package Thermal Resistance } \\ & \text { Junction-to-Case, R } \begin{array}{l} \text { ӨJC } \\ \text { Junction-to-Ambient, } \text { R }_{\text {QJA }} \end{array} \end{aligned}$ | $\begin{aligned} & 15 \\ & 50 \end{aligned}$ | $\begin{aligned} & \circ \\ & \\ & \\ & \\ & \\ & \mathrm{C} / \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Lead Temperature Soldering: Wave Solder (through hole styles only)(Note 1) | 260 peak | ${ }^{\circ} \mathrm{C}$ |

1. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS ( $4.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 5.5 \mathrm{~V},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 125^{\circ} \mathrm{C}$, unless otherwise specified.) Note 2

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| General |  |  |  |  |  |
| $\mathrm{V}_{\text {CC }}$ Supply Current | ```Outputs Off, \(\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}\) Note \(3 \mathrm{l}_{\text {OUT }}=600 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{IN}}=5.5 \mathrm{~V}\) (four outputs on) (one output on)``` | - | - - - | $\begin{aligned} & 5.0 \\ & 65 \\ & 20 \end{aligned}$ | mA <br> mA <br> mA |

## Output Drivers

| Saturation Voltage | $\mathrm{I}_{\mathrm{OUT}}=600 \mathrm{~mA}, \mathrm{~V}_{\mathrm{IN}}=2.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=4.0 \mathrm{~V}$ | - | - | 650 | mV |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Leakage Current | $\mathrm{V}_{\mathrm{OUT}}=60 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0.8 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | - | - | 50 | $\mu \mathrm{~A}$ |
| Current Limit | $4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{OUT}}<16 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | 0.6 | - | 1.8 | A |
| Thermal Shutdown | - | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| Sustaining Voltage, $\mathrm{V}_{\mathrm{CE} \text { (SUS) }}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | 40 | - | - | V |

Clamp Diodes

| Forward Voltage | $\mathrm{I}_{\mathrm{F}}=1.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | - | - | 2.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Leakage Current | $\mathrm{V}_{\mathrm{R}}=60 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | - | - | 100 | $\mu \mathrm{~A}$ |

Input

| Input Current | $0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq \mathrm{V}_{\mathrm{CC}}$ | -2.0 | - | 10 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input High Voltage | $\mathrm{I}_{\text {OUT }}=600 \mathrm{~mA}$ | 2.0 | - | - | V |
| Input Low Voltage | $\mathrm{I}_{\text {OUT }}=600 \mathrm{~mA}$ | - | - | 0.8 | V |

## AC Characteristics, Note 4

| Turn-On Delay, Turn-Off Delay | IOUT $=500 \mathrm{~mA}$ | - | - | 10 | $\mu \mathrm{~s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |

2. Designed to meet these characteristics over the stated temperature range, though may not be $100 \%$ parametrically tested in production.
3. Pulse test.
4. Input rise time $\leq 10 \mathrm{~ns}$, falltime $\leq 10 \mathrm{~ns}$, measured at $50 \%$ points.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :---: |
| DIP-16 | PIN SYMBOL | FUNCTION |
| 1 | OUTA | Driver A Output. |
| 2 | CLAMPAB | Diode Clamp to Driver A and Driver B. |
| 3 | OUTB | Driver B Output. |
| 4 | GND | Ground. |
| 5 | GND | Ground. |
| 6 | OUTC | Driver C Output. |
| 7 | CLAMPCD | Diode Clamp to Driver C and Driver D. |
| 8 | OUTD | Driver D Output. |
| 9 | IND | Driver D Input. |
| 10 | INC | Driver C Input. |
| 11 | $\mathrm{V}_{\mathrm{CC}}$ | 5.0 V Input Supply Voltage. |
| 12 | GND | Ground. |
| 13 | GND | Ground. |
| 14 | ENABLE | ENABLE Input to all Drivers. |
| 15 | INB | Driver B Input. |
| 16 | INA | Driver A Input. |



Figure 2. Simplified Block Diagram - Each Driver

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Typical $\mathrm{V}_{\mathrm{CE}(\mathrm{SUS})}$


Figure 5. Typical Output Current Limit, $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$


Figure 7. Typical $\mathrm{V}_{\mathrm{Cc}}$ Current - No Outputs On, $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$


Figure 4. Typical Output On Voltage, $\mathrm{V}_{\mathrm{Cc}}=4.0 \mathrm{~V}$


Figure 6. Typical Clamp Diode Forward Voltage


Figure 8. Typical $\mathrm{V}_{\mathrm{CC}}$ Current - All Outputs On, $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, $\mathrm{I}_{\text {OUT }}=600 \mathrm{~mA}$ (Each Output)

## TYPICAL PERFORMANCE CHARACTERISTICS



Figure 9. Typical Input Threshold Voltage, $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$

## DETAILED OPERATING DESCRIPTION

The NCV7601 Quad Driver consists of four identical driver sections with output clamp diodes and a common bias generator.

Each driver input (Figure 2) is buffered by a PNP emitter follower for reduced input bias current and features a nominal 18 V Zener input clamp for transient protection. Each input is compared to a separate temperature-compensated reference, which provides a nominal 1.35 V comparison threshold. With the addition of an external series resistor, the inputs can be interfaced directly to +14 V automotive system voltages. Floating inputs are interpreted as high.

Each driver output NPN is supplied with a substantially fixed base current from the $+5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ pin by a pre-driver.

Each pre-driver multiplies a temperature-compensated reference current when its control input and the common enable input is high. Current limit and thermal limit circuits act independently within the pre-driver to reduce base drive to the output NPN. The independent limit operation allows the driver to handle inrush current from lamp loads while protecting the driver from fault conditions that exist long enough to raise the temperature at that driver to its thermal limit threshold. Each driver has its own temperature-sensing device located in close proximity to the output NPN. The separate sensing devices are strategically placed at the corners of the die to reduce interaction between them.

## APPLICATIONS INFORMATION

The NCV7601 Quad Driver interfaces high power loads to low power control signals. The four open-collector NAND drivers with common ENABLE are TTL, DTL and CMOS compatible. Any number of drivers may be parallel connected to drive loads greater than each driver's nominal capability. Power for the Quad's control logic and output pre-drive is supplied from the $+5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ pin, and is proportional to the number of active inputs. Minimum standby power is consumed when the ENABLE input is low. Each driver is individually protected with current limit and thermal limit circuitry. Drivers with fault loads are protected while drivers with normal loads continue to operate, provided that sufficient heat sinking maintains a good thermal gradient between all drivers.

Clamp diodes at each driver output provide a means for managing inductive load transients. The common cathode pin for each driver pair can be connected to the load supply voltage for suppression of minor transients resulting from
wiring harness inductances. The use of an external Zener diode or TVS (Transient Voltage Suppressor) device such as the ON Semiconductor 1.5 SMCXXXAT3 series is strongly recommended when driving large inductive loads or when load supply transients can be expected to exceed the Quad Driver's VCE (SUS) rating. The use of a TVS device provides an additional benefit by reducing the decay time of inductive loads. More information on safeguarding the Quad's output NPN's and about transient suppression methods and device selection is available in ON Semiconductor application notes "Understanding Power Transistors Breakdown Parameters", document number AN1628/D, "A Review of Transients and their Means Of Suppression", document number AN843/D and "Transient Power Capability of Zener Diodes", document number AN784/D. All application notes are available through the Literature Distribution Center or via our website at http://www.onsemi.com.

## CS2082

## Dual Airbag <br> Deployment ASIC

The CS2082 controls and monitors two airbag firing loops. The independent firing loops are low- and high-side controlled. Device communication is through a Serial Peripheral Interface (SPI) port, and includes frame error detection circuitry for data reliability.

Diagnostics include squib resistance measurement and continuous monitoring for shorts to ground, shorts to battery, and for open loops. The high- and low-side drivers can be individually activated to guarantee function and to identify shorts between firing loops. Additional features include power on reset, overtemperature protection, a charge pump, high-side safing sensor closure detection, an analog multiplexer, a monitor to ensure battery potential, and a programmable monitor to ensure firing potential.

## Features

- Serial Input Bus
- Two Squib Outputs
- Low- and High-Side Control
- Monitors
- Squib Resistance
- Short to Ground or Battery
- Battery Potential
- Firing Potential
- Safing Sensor Detection
- 60 V Peak Transient Voltage

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SO-20L DW SUFFIX
CASE 751D

PIN CONNECTIONS AND MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS2082EDW20 | SO-20L | 37 Units/Rail |
| CS2082EDWR20 | SO-20L | 1000 Tape \& Reel |



Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Storage Temperature | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {BAT }}$ | -0.3 to 24 | V |
| $\mathrm{~V}_{\text {RES }}$ | -0.3 to 30 | V |
| $\mathrm{~V}_{\text {CC }}$ | -0.3 to 6.0 | V |
| ESD Susceptibility (Human Body Model) | 500 | V |
| Power Dissipation (Non-Firing) | 0.15 | W |
| Power Dissipation (Both Firing Loops With Squibs Shorted) | 140 | W |
| Power Dissipation (Squib Resistance Measurement) | 1.6 | W |
| Peak Transient Voltage (46 V Load Dump @ 14 V V ${ }_{\text {BAT }}$ ) | Reflow: (SMD styles only) (Note 1) | 230 peak |
| Lead Temperature Soldering: | ${ }^{\circ} \mathrm{C}$ |  |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (4.75 V $<\mathrm{V}_{\mathrm{CC}}<5.25 \mathrm{~V}, 8.0 \mathrm{~V}<\mathrm{V}_{\text {RES }}<30 \mathrm{~V}, 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{BAT}}<18 \mathrm{~V}$, $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+85^{\circ} \mathrm{C}$; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Requirements |  |  |  |  |  |
| $\mathrm{V}_{\text {CC }}$ Quiescent Current | $\mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}$ | - | 2.0 | 4.0 | mA |
| $V_{\text {BAT }}$ Quiescent Current | $\mathrm{V}_{\text {BAT }}=18 \mathrm{~V}$ | - | 2.5 | 5.0 | mA |
| $\mathrm{V}_{\text {BAT }}$ Measurement Current | $\mathrm{V}_{\text {BAT }}=18 \mathrm{~V}, \mathrm{R}_{\text {SQUIB }}=1.0 \Omega$ | - | - | 80 | mA |
| $\mathrm{V}_{\text {RES }}$ Quiescent Current | $\mathrm{V}_{\text {RES }}=30 \mathrm{~V}$ | - | - | 1.0 | mA |
| $V_{\text {RES }}$ Firing Current | $\mathrm{V}_{\text {RES }}=30 \mathrm{~V}$ | - | - | 3.0 | mA |

## Power on Reset $\quad \mathrm{V}_{\mathrm{BAT}}=9.0 \mathrm{~V}, \mathrm{~V}_{\text {RES }}=10 \mathrm{~V}$

| Power Reset Active Voltage | $\mathrm{V}_{\mathrm{CC}}$ Falling | 3.50 | 4.00 | 4.25 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Power Reset Off Voltage | $\mathrm{V}_{\mathrm{CC}}$ Rising | 3.65 | 4.20 | 4.50 | V |
| Hysteresis |  | 50 | - | - | mV |

Low Side Driver $\quad \mathrm{V}_{\text {RES }}=8.0 \mathrm{~V}=\mathrm{V}_{\mathrm{RX}}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=8.0 \mathrm{~V}$

| Saturation Voltage | $\mathrm{I}=1.2 \mathrm{~A}$ | - | - | 1.8 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Current Limit (ILIMIT) | $\mathrm{V}_{\text {SLX }}-\mathrm{V}_{\mathrm{FGX}}=5.0 \mathrm{~V}$ | 1.2 | 1.6 | 2.0 | A |
| Turn-on Delay Time | From CS falling Edge, $\mathrm{I}_{\mathrm{D}}=0.9 \times \mathrm{I}_{\mathrm{LIMIT}(\mathrm{MIN})}$ | - | - | 75 | $\mu \mathrm{~s}$ |
| Turn-off Delay Time | From CS falling Edge, $\mathrm{I}_{\mathrm{D}}=0.1 \times \mathrm{I}_{\mathrm{LIMIT}(\mathrm{MIN})}$ | - | - | 25 | $\mu \mathrm{~s}$ |

High Side Driver $\quad \mathrm{V}_{\text {RES }}=8.0 \mathrm{~V}=\mathrm{V}_{\mathrm{RX}}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=8.0 \mathrm{~V}$

| Saturation Voltage | $\mathrm{I}=1.2 \mathrm{~A}$ | - | - | 1.8 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Current Limit (LIMIT) | $\mathrm{V}_{\mathrm{RX}}-\mathrm{V}_{\mathrm{SHX}}=5.0 \mathrm{~V}$ | 1.2 | 2.0 | 2.5 | A |
| $\mathrm{~V}_{\mathrm{R} 1}$ Quiescent Current Drivers off | $\mathrm{V}_{\mathrm{RX}}=\mathrm{V}_{\mathrm{RES}}=30 \mathrm{~V}$ | - | - | 1.0 | mA |
| $\mathrm{~V}_{\mathrm{R} 2}$ Quiescent Current Drivers off | $\mathrm{V}_{\mathrm{RX}}=\mathrm{V}_{\mathrm{RES}}=30 \mathrm{~V}$ | - | - | 100 | $\mu \mathrm{~A}$ |
| Turn-on Delay Time | From CS falling Edge, $\mathrm{I}_{\mathrm{D}}=0.9 \times \mathrm{I}_{\mathrm{LIMIT}(\mathrm{MIN})}$ | - | - | 100 | $\mu \mathrm{~s}$ |
| Turn-off Delay Time | From CS falling Edge, $\mathrm{I}_{\mathrm{D}}=0.1 \times \operatorname{IIIMIT(MIN)}$ | - | - | 25 | $\mu \mathrm{~s}$ |

## Thermal Shut Down

| Thermal Shutdown Temp | Guaranteed by Design | 150 | 180 | 210 | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Thermal Hysteresis | Guaranteed by Design | 30 | 40 | 60 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS (continued) (4.75 V $<\mathrm{V}_{\mathrm{CC}}<5.25 \mathrm{~V}, 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{RES}}<30 \mathrm{~V}, 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{BAT}}<18 \mathrm{~V}$, $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+85^{\circ} \mathrm{C}$; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Thermal Shut Down |  |  |  |  |  |
| Time to Thermal Shutdown | RSQUIB $=0, V_{\mathrm{RX}}=30 \mathrm{~V}, \mathrm{~T}=85^{\circ} \mathrm{C}$, <br> Guaranteed by Design | 7.0 | - | - | ms |

Squib Resistive Measurements $\quad \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{MR}}=49.9 \Omega, \mathrm{~V}_{\text {RES }}=30 \mathrm{~V}$

| Squib Differential Voltage | $\mathrm{V}_{\text {DIFF }}=\mathrm{SHx}-\mathrm{SLx}, \mathrm{R}_{\text {SQUIB }}=1.0 \Omega$ to $10 \Omega$ | 46 | 53 | 60 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Difference Between SHx \& MR <br> current - SHx reference | $\mathrm{I}_{\text {SQUIB }}=50 \mathrm{~mA}$ | -1.0 | - | 1.0 | \% |
| SHx Current Limit | $\mathrm{R}_{\text {SQUIB }}=0$ | 67 | 100 | 133 | mA |
| SLx Current Limit | $\mathrm{R}_{\mathrm{MR}}=0$ | 77 | 115 | 153 | mA |
| MR Voltage Clamp | - | $\mathrm{V}_{C C}-0.3$ | - | $\mathrm{V}_{C C}+0.3$ | V |
| Turn On Delay Time excluding external Capacitors | - | - | - | 100 | $\mu \mathrm{S}$ |
| Turn off Delay Time | - | - | - | 50 | $\mu \mathrm{s}$ |

Short Measurements $\quad V_{\text {CC }}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {RES }} \geq \mathrm{V}_{\mathrm{BAT}}, \mathrm{V}_{\mathrm{RX}} \geq \mathrm{V}_{\text {BAT }}$

| SHx pull-up resistance to $\mathrm{V}_{\mathrm{BAT}}$ SLx pull-down resistance | $\mathrm{V}_{\text {BAT }}=18 \mathrm{~V}$ | $\begin{aligned} & 4.0 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 10 \end{aligned}$ | $\begin{aligned} & 17 \\ & 17 \end{aligned}$ | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Pull-up resistor matching | - | -5.0 | - | 5.0 | \% |
| Pull-down resistor matching | - | -5.0 | - | 5.0 | \% |
| Short to $\mathrm{V}_{\text {BAT }}$ Trip | SHx short to Battery SLx bit set to 1 | $0.73 \times \mathrm{V}_{\text {BAT }}$ | $0.75 \times \mathrm{V}_{\text {BAT }}$ | $0.77 \times \mathrm{V}_{\text {BAT }}$ | V |
| Short to GND Trip | SHx short to GND SGx bit set to 1 | $0.23 \times \mathrm{V}_{\text {BAT }}$ | $0.25 \times \mathrm{V}_{\text {BAT }}$ | $0.27 \times \mathrm{V}_{\text {BAT }}$ | V |

$\mathrm{V}_{\mathrm{BAT}}$ Monitoring $\quad \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$, External $\mathrm{V}_{\mathrm{BAT}}$ Diode not included, $\mathrm{V}_{\mathrm{RES}}=30 \mathrm{~V}$

| $V_{\text {BAT }}$ Low Trip | BL bit set to 1 when below trip | 7.5 | 8.5 | 9.5 | V |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~V}_{\mathrm{BAT}}$ High Trip | BL bit set to 0 when above trip | 8.0 | 9.0 | 10 | V |

$\mathrm{V}_{\text {RES }}$ Monitoring $\quad \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=18 \mathrm{~V}$

| $V_{\text {RES }}$ Low Trip | \$6d AUX register b0 $=0$ | 15.7 | 17.5 | 19.3 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $V_{\text {RES }}$ High Trip | \$6d AUX register b0 $=0$ | 16.5 | 18.5 | 20.5 | V |
| $\mathrm{~V}_{\text {RES }}$ Low Trip | \$6d AUX register b0 $=1$ | 21.5 | 24.0 | 26.5 | V |
| $\mathrm{~V}_{\text {RES }}$ High Trip | \$6d AUX register b0 $=1$ | 22.5 | 25 | 27.5 | V |

## Safing Sensor Monitor

| External Resistance Trip Range | SSC bit set when resistance is less | 30 | 400 | 600 | $\Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Charge Pump and Monitor $\quad \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\text {BAT }}=10 \mathrm{~V}$ |  |  |  |  |  |
| Oscillator Frequency | $\mathrm{V}_{\text {RES }}=10 \mathrm{~V}$ | 200 | - | 800 | kHz |
| Charge Pump charge time | $\begin{gathered} \mathrm{C}_{\mathrm{CHG}}=0.1 \mu \mathrm{~F}, \mathrm{~V}_{\mathrm{RES}}=8.0 \mathrm{~V}, \\ \text { Chrg from } 8.0 \mathrm{~V} \text { to } 14 \mathrm{~V} \end{gathered}$ | - | - | 20 | ms |
| Charge Pump Low Voltage | CL bit set to 1 when below trip | 14.5 | 16.0 | 17.5 | V |
| Charge Pump High Voltage | CL bit set to 0 when above trip | 15.0 | 17.5 | 18.0 | V |

Analog MUX

$$
\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}
$$

| A OUT Output Range | - | 0.1 | - | $V_{\text {CC }}-0.1$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~A}_{\text {IN }}$ Input Range | - | 0 | - | $\mathrm{V}_{\text {CC }}$ | V |

ELECTRICAL CHARACTERISTICS (continued) (4.75 V $<\mathrm{V}_{\mathrm{CC}}<5.25 \mathrm{~V}, 8.0 \mathrm{~V}<\mathrm{V}_{\mathrm{RES}}<30 \mathrm{~V}, 9.0 \mathrm{~V}<\mathrm{V}_{\mathrm{BAT}}<18 \mathrm{~V}$, $-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+85^{\circ} \mathrm{C}$; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Analog MUX | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  |  |  |  |
| MUX internal voltage drop | lout $=100 \mu \mathrm{~A}$ | - | - | 100 | mV |
| Proportion of $\mathrm{V}_{\mathrm{BAT}}$ on $A_{\text {OUT }}$ with $\mathrm{V}_{\text {BAT }}$ selected | - | 23 | 25 | 27 | \% |
| AOUT Impedance with $V_{\text {BAT }}$ selected | - | 6.0 | 15.0 | 35 | k $\Omega$ |
| Proportion of $\mathrm{V}_{\text {RES }}$ on $\mathrm{A}_{\text {OUT }}$ with $\mathrm{V}_{\text {RES }}$ selected | - | 15 | 17 | 19 | \% |
| AOUT Impedance with $\mathrm{V}_{\text {RES }}$ selected | - | 6.0 | 12.5 | 25.5 | k $\Omega$ |

Digital Inputs - $\mathrm{D}_{\mathrm{IN}}, \mathrm{CLK}, \mathrm{CS} \quad \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=18 \mathrm{~V}, \mathrm{~V}_{\text {RES }}=30 \mathrm{~V}$

| Input Low Voltage ( $\mathrm{V}_{\mathrm{IL}}$ ) | - | 0 | - | $0.3 \times \mathrm{V}_{\mathrm{CC}}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input High Voltage $\left(\mathrm{V}_{\mathrm{IH}}\right)$ | - | $0.7 \times \mathrm{V}_{\mathrm{CC}}$ | - | $\mathrm{V}_{\mathrm{CC}}$ | V |
| Input Voltage Hysteresis | - | 100 | - | - | mV |
| Input Pull Down Current $\left(\mathrm{l}_{\mathrm{IH}}\right)$ | - | 50 | 100 | 200 | $\mu \mathrm{~A}$ |

Digital Outputs - Dout $\quad \mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=18 \mathrm{~V}, \mathrm{~V}_{\text {RES }}=30 \mathrm{~V}$

| Output Low Voltage $\left(\mathrm{V}_{\mathrm{OL}}\right)$ | $\mathrm{I}_{\text {SINK }}=1.0 \mathrm{~mA}$ | - | - | 0.4 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output High Voltage $\left(\mathrm{V}_{\mathrm{OH}}\right)$ | $\mathrm{I}_{\text {SOURCE }}=1.0 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{CC}}-0.75$ | - | - | V |
| Tri-State Pull-up Current | $\mathrm{CS}=0, \mathrm{D}_{\text {OUT }}=0$ | 50 | 100 | 200 | $\mu \mathrm{~A}$ |
| Rise \| Fall Time | $\mathrm{C}_{\text {LOAD }}=200 \mathrm{pF}$ | - | - | 50 | ns |

## PACKAGE PIN DESCRIPTION

| Package Lead Number |  |  |
| :---: | :---: | :---: |
| SO-20L | Pin Symbol | Function |
| 1 | $V_{\text {BAT }}$ | Battery Supply Voltage. |
| 2 | CHRG | Charge pump Storage. |
| 3 | $V_{\text {RES }}$ | Reserve Supply Voltage. |
| 4 | VR1 | Loop 1 Supply. |
| 5 | SH1 | Squib 1 High Side. |
| 6 | SL1 | Squib 1 Low Side. |
| 7 | FG1 | Loop 1 Return. |
| 8 | Dout | Serial Port output. |
| 9 | CLK | Serial Port Clock. |
| 10 | MR | Squib Resistance Output Current. |
| 11 | CS | Serial Port Chip Select. |
| 12 | A OUT | Analog MUX Output. |
| 13 | $\mathrm{A}_{\text {IN }}$ | Analog MUX Input. |
| 14 | FG2 | Loop 2 Return. |
| 15 | SL2 | Squib 2 Low Side. |
| 16 | SH2 | Squib 2 High Side. |
| 17 | VR2 | Loop 2 Supply. |

PACKAGE PIN DESCRIPTION (continued)

| Package Lead Number |  |  |
| :---: | :---: | :--- |
| SO-20L | Pin Symbol |  |
| 18 | $\mathrm{D}_{\mathrm{IN}}$ | Function |
| 19 | $\mathrm{~V}_{\mathrm{CC}}$ | 5.0 V Regulated Supply. |
| 20 | GND | Signal Ground. |

## FUNCTIONAL DESCRIPTION

The CS2082 is an automotive air bag deployment and diagnostic system for up to two independent firing loops. Communication with the ASIC is through a synchronous serial port using Serial Peripheral Interface (SPI) protocol, at CLK rates up to 2.0 MHz .

Data is simultaneously sent from the DOUT pin and received at the $\mathrm{D}_{\text {IN }}$ pin under the control of the CS and CLK pins. Error detection logic is included in the SPI to guard against glitches on either the CS or CLK logic signal inputs. A valid CS frame must contain exactly 8 CLK cycles for each CS low-high-low transition. Detection of a frame error will cause input data for that frame to be ignored and an error code ( $\$ \mathrm{FE}$ ) to be sent during the next valid CS frame.

The data at $\mathrm{D}_{\text {OUT }}$ is sent MSB first and is guaranteed valid before the rising edge of CLK. The 8 bits sent from $\mathrm{D}_{\text {OUT }}$ after CS goes high will be the previous data received, data from either the status register or the fault register, or the CS frame error code (\$FE).

The data at $\mathrm{D}_{\text {IN }}$ is received MSB first and must be valid before the rising edge of CLK. The 8 bits received at $\mathrm{D}_{\mathrm{IN}}$ before CS goes low will be the current command. Table 1 defines the legal 8-bit SPI commands, where $\mathrm{d}=$ four data bits and $\mathrm{x}=$ don't care. All other inputs will be ignored

Table 1. Valid CS2082 SPI Commands

| COMMAND | FUNCTION |
| :---: | :--- |
| $\$ 1 \mathrm{x}$ | Read Staus Register |
| $\$ 2 \mathrm{x}$ | Read Fault Register |
| $\$ 3 \mathrm{~d}$ | Squib Resistance Measurements |
| $\$ 4 \mathrm{~d}$ | Analog MUX Select |
| $\$ 5 \mathrm{~d}$ | Low Side Switch Control |
| $\$ 6 \mathrm{~d}$ | Auxiliary Control Register |
| $\$$ Ad | High Side Switch Control |

## Read Status Register - \$1x

The $\$ 1 x$ command causes the data contained in the status register to be sent from $\mathrm{D}_{\text {OUT }}$ during the next valid CS frame. The status register reports the condition of the firing paths, closure detection of an external safing switch between
the $\mathrm{V}_{\text {RES }}$ and VR1 pins, the state of the internal charge pump, and the state of external $\mathrm{V}_{\text {BAT }}$ and $\mathrm{V}_{\text {RES }}$ power supplies. The status register is an 8 -bit active-high register with bit definition as shown in Table 2.

Table 2. Status Register Bit Definition

| BIT | VALUE | DESCRIPTION |
| :---: | :---: | :--- |
| D7 | 0 | Always Logic zero |
| D6 | 0 | Always Logic zero |
| D5 | F1 | SH1 and SL1 switches active |
| D4 | F2 | SH2 and SL2 switches active |
| D3 | SSC | Safing Sensor is closed |
| D2 | RL | V REs voltage is below trip $^{\text {D1 }}$ |
| BL | V $_{\text {BAT }}$ voltage is below trip |  |
| D0 | CL | CHRG voltage is below trip |

## Read Fault Register - \$2x

The $\$ 2 x$ command causes the data contained in the fault register to be sent from $\mathrm{D}_{\text {OUT }}$ during the next valid CS frame. The register reports fire path faults by continuously comparing each path to a portion of the voltage at the $\mathrm{V}_{\text {BAT }}$ pin. The fault register is an 8-bit active-high register with bit definition as shown in Table 3.

Table 3. Fault Register Bit Definition

| BIT | VALUE | DESCRIPTION |
| :---: | :---: | :--- |
| D7 | 0 | Always Logic zero |
| D6 | 0 | Always Logic zero |
| D5 | 0 | Always Logic zero |
| D4 | 0 | Always Logic zero |
| D3 | SB2 | High Side of Sqib 2 above <br> $75 \% ~ V_{\text {BAT }}$ trip threshold |
| D2 | SB1 | High Side of Sqib 1 above <br> $75 \% V_{\text {BAT trip threshold }}$ |
| D1 | SG2 | Low Side of Sqib 2 below <br> $25 \% ~ V_{\text {BAT }}$ trip threshold |
| D0 | SG1 | Low Side of Sqib 1 below <br> $25 \% ~ V_{\text {BAT }}$ trip threshold |

Each SHx pin is pulled up to $\mathrm{V}_{\text {BAT }}$ while each SLx pin is pulled down to GND through separate nominal $10 \mathrm{k} \Omega$ resistors, thus biasing each normal fire path to about $1 / 2$ $\mathrm{V}_{\text {BAT }}$. An open fire path has been detected if both the SBx and SGx bits are set for that path. To detect faults between fire paths and to test driver function, each driver should be activated individually. The activated driver should cause its respective fault bit to be set. If an activated driver does not set its respective fault bit, a driver fault has been detected. If an activated driver causes the fault bit of an inactivated driver to be set, a fault between fire paths has been detected. Table 4 defines the implied ranges over which the various types of faults can be detected.

Table 4. Implied Resistive Fault Detection Ranges

| Fault | Min | Nom | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Short to Ground | 1 | 5 | 10 | $\mathrm{k} \Omega$ |
| Short to Battery | 1 | 5 | 10 | $\mathrm{k} \Omega$ |
| Open | 5 | 20 | 40 | $\mathrm{k} \Omega$ |
| Driver Open | 1 | 5 | 10 | $\mathrm{k} \Omega$ |
| Driver Shorted | 1 | 5 | 10 | $\mathrm{k} \Omega$ |
| Squib to Squib | 1 | 5 | 10 | $\mathrm{k} \Omega$ |

## Squib Resistance Measurement - \$3d

The \$3d command activates squib resistance measurement for the selected firing path. The respective active-high bit definitions are shown in Table 5. At power-up, the default path is 'None.'

Table 5. Squib Resistance Path Select

| D3 | D2 | D1 | D0 | Path |
| :---: | :---: | :---: | :---: | :--- |
| $x$ | $x$ | 0 | 0 | NONE |
| $x$ | $x$ | 0 | 1 | SQUIB 1 |
| $x$ | $x$ | 1 | 0 | SQUIB 2 |
| $x$ | $x$ | 1 | 1 | NONE |

Squib resistance is measured by forcing 50 mV nominal (proportional to $\mathrm{V}_{\mathrm{CC}}$ ) across the squib. The resulting squib current is passed to an external load resistor at the MR pin, converting the current back into a voltage. This voltage may be read directly at the MR pin, or passed through the analog multiplexer to be read at the AOUT pin. The known values of the squib differential voltage ( $\mathrm{V}_{\text {DIFF }}$ ) and the MR resistance $\left(\mathrm{R}_{\mathrm{MR}}\right)$, and the measured MR voltage $\left(\mathrm{V}_{\mathrm{MR}}\right)$ indicate squib resistance such that:

$$
\text { RSQUIB }=\frac{\mathrm{R}_{\mathrm{MR}} \times \mathrm{V}_{\text {DIFF }}}{\mathrm{V}_{\mathrm{MR}}}
$$

Typical MR voltage response for $\mathrm{R}_{\mathrm{MR}}=50 \Omega$ over a squib resistance range of $0.6 \Omega$ to $6.0 \Omega$ is illustrated in Figure 2.


Figure 2. Typical MR Voltage Response
Measurement accuracy of the CS2082 with combined tolerances and with and external $1 \%$ load resistor at the MR pin can be defined by the equation:

$$
\begin{aligned}
& =\operatorname{RSQ}(\mathrm{A})+12.5 \% /-15.94 \%
\end{aligned}
$$

where $\mathrm{V}_{\text {DIFF(IDEAL) }}$ and $\mathrm{R}_{\mathrm{MR} \text { (IDEAL) }}$ are the assumed values for the squib resistance solution algorithm, $\mathrm{R}_{\mathrm{SQ}(\mathrm{A})}$ is the actual squib resistance, and $\mathrm{R}_{\mathrm{SQ}(\mathrm{E})}$ is the result of the solution algorithm. An additional error may be added if the MR voltage is measured through the analog multiplexer.

In operation, current is sourced from $\mathrm{V}_{\mathrm{BAT}}$ to the SHx pin, through the squib to the SLx pin, and returned to ground through the MR load resistor. Current clamps are provided for both the SHx and SLx pins and a voltage clamp is provided for the MR pin. These clamps along with the resolution of the ADC are the constraining factors for the minimum and maximum measurable squib resistance values.
The minimum measurable squib resistance can be defined as:

$$
\frac{V_{\operatorname{DIFF}(\mathrm{MIN})}}{\operatorname{IIIM}(\mathrm{MAX})} \leq \mathrm{R}_{\text {SQUIB }(\mathrm{MIN})} \leq \frac{\mathrm{V}_{\mathrm{DIFF}}(\mathrm{MIN}) \times \mathrm{R}_{\mathrm{MR}(\mathrm{MIN})}}{\mathrm{V}_{\mathrm{CLAMP}}(\mathrm{MAX})}
$$

The maximum measurable squib resistance can be defined as:
$R_{\text {SQUIB }}(\mathrm{MAX})=\frac{\mathrm{V}_{\text {DIFF }}(\mathrm{MAX}) \times \mathrm{R}_{\text {MR(MAX }} \times\left(2^{\mathrm{n}}-1\right)}{\mathrm{V}_{\mathrm{CC}}(\mathrm{MIN})}$
In the above equations, $V_{\text {DIFF }}$ is the $\mathrm{SHx}-\mathrm{SLx}$ forced differential voltage, $\mathrm{I}_{\text {LIM }}$ is the SHx resistive measure current limit, $\mathrm{V}_{\text {CLAMP }}$ is the MR clamp voltage, $\mathrm{R}_{\mathrm{MR}}$ is the toleranced MR load resistor value and $n$ is the number of bits of resolution of the ADC.

It should be noted that during resistive measurements, faults to GND or BAT (dependent on $\mathrm{V}_{\text {BAT }}$ voltage and
squib resistance) may be reported by the fault register and should be ignored.

Power Dissipation during resistive measurement can be calculated as:

$$
P=I_{\text {SQUIB }}\left(V_{\text {BAT }}-V_{\text {DIFF }}\right)-\left(I_{\text {SQUIB }} \times R_{M R}\right)
$$

where $\mathrm{V}_{\text {BAT }}$ is the voltage at the CS2082 $\mathrm{V}_{\text {BAT }}$ pin and $\mathrm{I}_{\text {SQUIB }}$ is the measurement current through the squib. A typical value for P is 300 mW when $\mathrm{V}_{\mathrm{BAT}}=13.5$,
$\mathrm{V}_{\mathrm{DIFF}}=50 \mathrm{mV}, \mathrm{R}_{\text {SQUIB }}=2.0 \Omega$ and $\mathrm{R}_{\mathrm{MR}}=49.9 \Omega$
The resultant increase in power dissipation will cause a corresponding increase in die temperature which will cause a corresponding decrease in time to thermal shutdown of the CS2082. To minimize the impact of squib resistive measurements on time to thermal shutdown a 5\% duty cycle is recommended.

## Analog MUX - \$4d

The $\$ 4 \mathrm{~d}$ command selects one of five states at the AOUT pin. The states are: High-Z; MR voltage; A $\mathrm{A}_{\text {IN }}$ voltage; proportion of $\mathrm{V}_{\mathrm{BAT}}$; proportion of $\mathrm{V}_{\text {RES }}$. The active-high Analog Mux select register bit definitions are shown in Table 6. All other states will be interpreted as High-Z. At power-up, the default state is 'High-Z.'

Table 6. Analog MUX Output Select

| D3 | D2 | D1 | D0 | State |
| :---: | :---: | :---: | :---: | :--- |
| 0 | 0 | 0 | 0 | High-Z |
| 0 | 0 | 0 | 1 | MR |
| 0 | 0 | 1 | 0 | AIN |
| 0 | 1 | 0 | 0 | BAT |
| 1 | 0 | 0 | 0 | RES |

## Low Side Switch Control - \$5d

The \$5d command activates the low side switches. When a data bit is low that switch is turned on. More than one switch can be activated at a time. Bit assignment is shown in Table 7. At power-up, no switches are active.

Table 7. Low Side Switch Select

| D3 | D2 | D1 | D0 | Active |
| :---: | :---: | :---: | :---: | :--- |
| $x$ | $x$ | 0 | 0 | BOTH |
| $x$ | $x$ | 0 | 1 | SL2 |
| $x$ | $x$ | 1 | 0 | SL1 |
| $x$ | $x$ | 1 | 1 | NONE |

## Auxiliary Control Register - \$6d

The $\$ 6 \mathrm{~d}$ command selects the $\mathrm{V}_{\text {RES }}$ Monitoring trip threshold. The threshold determines when the \$1x Status Register reports $\mathrm{V}_{\text {RES }}=1$. Bit assignment is shown in Table 8. At power-up, default trip is 17 V .

Table 8. VRES Monitor Trip Select

| D3 | D2 | D1 | D0 | Trip |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $x$ | $x$ | $x$ | 0 | 17 V |  |
| $x$ | x | x | 1 | 23 V |  |

## High Side Switch Control - \$Ad

The \$Ad command activates the high side switches. When a data bit is high, that switch is turned on. More than one switch can be activated at a time. Bit assignment is shown in Table 9. Note that the $\$ 5 \mathrm{~d}$ and $\$$ Ad commands are binary complements, i.e., by sending 1010xx11, both high side switches are activated, and by sending the complement 0101xx00, both low side switches are activated. At power-up, no switches are active.

Table 9. High Side Switch Select

| D3 | D2 | D1 | D0 | Active |
| :---: | :---: | :---: | :---: | :--- |
| $x$ | $x$ | 0 | 0 | NONE |
| $x$ | $x$ | 0 | 1 | SH1 |
| $x$ | $x$ | 1 | 0 | SH2 |
| $x$ | $x$ | 1 | 1 | BOTH |



Figure 3. Application Diagram

PACKAGE THERMAL DATA

| Parameter |  | SO-20L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 17 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 90 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC1489, MC1489A

## Quad Line EIA-232D Receivers

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

- Input Resistance - 3.0 k to $7.0 \mathrm{k} \Omega$
- Input Signal Range - $\pm 30 \mathrm{~V}$
- Input Threshold Hysteresis Built In
- Response Control
a) Logic Threshold Shifting
b) Input Noise Filtering


Figure 1. Simplified Application


PIN CONNECTIONS


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 2973 of this data sheet.

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 2974 of this data sheet.

MC1489, MC1489A


Figure 2. Representative Schematic Diagram (1/4 of Circuit Shown)

MAXIMUM RATINGS $\left(T_{A}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 10 | Vdc |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | $\pm 30$ | Vdc |
| Output Load Current | IL | 20 | mA |
| Power Dissipation (Package Limitation, SO-14 and Plastic Dual In-Line Package) Derate above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | $\begin{gathered} \mathrm{P}_{\mathrm{D}} \\ 1 / \mathrm{\theta JA}^{2} \end{gathered}$ | $\begin{gathered} 1000 \\ 6.7 \end{gathered}$ | $\begin{gathered} \mathrm{mW} \\ \mathrm{~mW} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | 0 to +75 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +175 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS (Response control pin is open.) $\left(\mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{Vdc} \pm 10 \%, \mathrm{~T}_{\mathrm{A}}=0\right.$ to $+75^{\circ} \mathrm{C}$, unless otherwise noted)

| Characteristics |  | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Positive Input Current | $\begin{aligned} & \left(\mathrm{V}_{1 \mathrm{H}}=+25 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{1 \mathrm{H}}=+3.0 \mathrm{Vdc}\right) \end{aligned}$ | IIH | $\begin{gathered} \hline 3.6 \\ 0.43 \end{gathered}$ | - | 8.3 - | mA |
| Negative Input Current | $\begin{aligned} & \left(\mathrm{V}_{\mathrm{IH}}=-25 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{IH}}=-3.0 \mathrm{Vdc}\right) \end{aligned}$ | IIL | $\begin{gathered} \hline-3.6 \\ -0.43 \end{gathered}$ | - | $-8.3$ | mA |
| Input Turn-On Threshold Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{OL}} \leqslant 0.45 \mathrm{~V}\right)$ | $\begin{aligned} & \text { MC1489 } \\ & \text { MC1489A } \end{aligned}$ | $\mathrm{V}_{\mathrm{IH}}$ | $\begin{gathered} 1.0 \\ 1.75 \end{gathered}$ | $\stackrel{-}{1.95}$ | $\begin{gathered} 1.5 \\ 2.25 \end{gathered}$ | Vdc |
| Input Turn-Off Threshold Voltage $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{~V}_{\mathrm{OH}} \geqslant 2.5 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=-0.5 \mathrm{~mA}\right)$ | MC1489 <br> MC1489A | $\mathrm{V}_{\mathrm{IL}}$ | $\begin{aligned} & 0.75 \\ & 0.75 \\ & \hline \end{aligned}$ | $\overline{0.8}$ | $\begin{aligned} & 1.25 \\ & 1.25 \end{aligned}$ | Vdc |
| $\begin{array}{ll}\text { Output Voltage High } & \begin{array}{l}\left(\mathrm{V}_{\mathrm{IH}}=0.75\right. \\ \text { (Input Ope }\end{array}\end{array}$ | $\begin{aligned} & \left(\mathrm{V}_{\mathrm{IH}}=0.75 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=-0.5 \mathrm{~mA}\right) \\ & \text { (Input Open Circuit, } \mathrm{I}_{\mathrm{L}}=-0.5 \mathrm{~mA} \text { ) } \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 2.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \hline 4.0 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & \hline 5.0 \\ & 5.0 \end{aligned}$ | Vdc |
| Output Voltage Low $\quad\left(\mathrm{V}_{\mathrm{IL}}=3.0 \mathrm{~V}\right.$ | $\left(\mathrm{V}_{\mathrm{IL}}=3.0 \mathrm{~V}, \mathrm{I}_{\mathrm{L}}=10 \mathrm{~mA}\right)$ | $\mathrm{V}_{\text {OL }}$ | - | 0.2 | 0.45 | Vdc |
| Output Short-Circuit Current |  | Ios | - | -3.0 | -4.0 | mA |
| Power Supply Current (All Gates "on," $\mathrm{l}_{\text {out }}=0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{IH}}=+5.0 \mathrm{Vdc}$ ) |  | ICC | - | 16 | 26 | mA |
| Power Consumption | $\left(\mathrm{V}_{\mathrm{IH}}=+5.0 \mathrm{Vdc}\right)$ | $\mathrm{P}_{\mathrm{C}}$ | - | 80 | 130 | mW |

SWITCHING CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{Vdc} \pm 1 \%, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, See Figure 3.)

| Propagation Delay Time | $\left(R_{L}=3.9 \mathrm{k} \Omega\right)$ | $\mathrm{t}_{\text {PLH }}$ | - | 25 | 85 | ns |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Rise Time | $\left(\mathrm{R}_{\mathrm{L}}=3.9 \mathrm{k} \Omega\right)$ | $\mathrm{t}_{\mathrm{TLH}}$ | - | 120 | 175 | ns |
| Propagation Delay Time | $\left(R_{\mathrm{L}}=390 \mathrm{k} \Omega\right)$ | $\mathrm{t}_{\text {PHL }}$ | - | 25 | 50 | ns |
| Fall Time | $\left(R_{\mathrm{L}}=390 \mathrm{k} \Omega\right)$ | $\mathrm{t}_{\text {THL }}$ | - | 10 | 20 | ns |

## MC1489, MC1489A

## TEST CIRCUITS


$C_{L}=15 \mathrm{pF}=$ total parasitic capacitance which includes probe and wiring capacitances

Figure 3. Switching Response


C, capacitor is for noise filtering
$R$, resistor is for threshold shifting.

Figure 4. Response Control Node

## MC1489, MC1489A

TYPICAL CHARACTERISTICS
$\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$, unless otherwise noted $)$


Figure 5. Input Current


Figure 7. MC1489A Input Threshold Voltage Adjustment


Figure 6. MC1489 Input Threshold Voltage Adjustment


Figure 8. Input Threshold Voltage versus Temperature


Figure 9. Input Threshold versus
Power Supply Voltage

## APPLICATIONS INFORMATION

## General Information

The Electronic Industries Association (EIA) has released the EIA-232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between $3000 \Omega$ and $7000 \Omega$ for input voltages between 3.0 and 25 V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one $\mathrm{V}_{\mathrm{BE}}$.

The receiver shall detect a voltage between - 3.0 and -25 V as a Logic " 1 " and inputs between 3.0 and 25 V as a Logic " 0 ." On some interchange leads, an open circuit of power "OFF" condition ( $300 \Omega$ or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic " 1 " input.

## Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical
turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV . The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 4, 6 and 7 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high frequency, high energy noise pulses. Figures 10 and 11 show typical noise pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels (see Figure 12).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 13 where two receivers are slaved to the same line that must still meet the EIA-232D impedance requirement.


Figure 11. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND


Figure 12. Typical Translator Application - MOS to DTL or TTL


Figure 13. Typical Paralleling of Two MC1489, A Receivers to Meet EIA-232D

MC1489, MC1489A
ORDERING INFORMATION

| Device | Package | Operating Temperature Range | Shipping |
| :---: | :---: | :---: | :---: |
| MC1489D | SO-14 | $\mathrm{T}_{\mathrm{A}}=0$ to $+75^{\circ} \mathrm{C}$ | 55 Units/Rail |
| MC1489DR2 |  |  | 2500 Tape \& Reel |
| MC1489AD |  |  | 55 Units/Rail |
| MC1489ADR2 |  |  | 2500 Tape \& Reel |
| MC1489P | PDIP-14 |  | 25 Units/Rail |
| MC1489AP | PDIP-14 |  | 25 Units/Rail |
| MC1489M | SOEIAJ-14 |  | 50 Units/Rail |
| MC1489MEL |  |  | 2000 Tape \& Reel |
| MC1489AM |  |  | 50 Units/Rail |
| MC1489AMEL |  |  | 2000 Tape \& Reel |

## MC1489, MC1489A

## MARKING DIAGRAMS

$$
\begin{gathered}
\text { SO-14 } \\
\text { D SUFFIX } \\
\text { CASE 751A }
\end{gathered}
$$

$$
\begin{aligned}
& \text { PDIP-14 } \\
& \text { P SUFFIX } \\
& \text { CASE } 646
\end{aligned}
$$



SOEIAJ-14
M SUFFIX
CASE 965


A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

## Quad Line EIA-232D Driver

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

## Features:

- Current Limited Output
$\pm 10 \mathrm{~mA}$ typical
- Power-Off Source Impedance
$300 \Omega$ minimum
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All ON Semiconductor MDTL and MTTL Logic Families

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| MC 1488 P | $\mathrm{T}_{\mathrm{A}}=0$ to $+75^{\circ} \mathrm{C}$ | Plastic |
| MC1488D |  | $\mathrm{SO}-14$ |

Simplified Application


## QUAD MDTL LINE DRIVER

EIA-232D

## SEMICONDUCTOR TECHNICAL DATA

PIN CONNECTIONS


Circuit Schematic
(1/4 of Circuit Shown)


MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ <br> $\mathrm{V}_{\mathrm{EE}}$ | +15 <br> -15 | Vdc |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IR}}$ | $-15 \leqslant \mathrm{~V}_{\mathrm{IR}} \leqslant$ | Vdc |
| 7.0 |  |  |  |

ELECTRICAL CHARACTERISTICS ( $\mathrm{V}_{\mathrm{CC}}=+9.0 \pm 1 \% \mathrm{Vdc}, \mathrm{V}_{\mathrm{EE}}=-9.0 \pm 1 \% \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=0$ to $75^{\circ} \mathrm{C}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Current - Low Logic State ( $\mathrm{V}_{\mathrm{IL}}=0$ ) | ILL | - | 1.0 | 1.6 | mA |
| Input Current - High Logic State ( $\mathrm{V}_{\mathrm{IH}}=5.0 \mathrm{~V}$ ) | $\mathrm{IIH}^{\text {H }}$ | - | - | 10 | $\mu \mathrm{A}$ |
| Output Voltage - High Logic State $\begin{aligned} & \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=+9.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-9.0 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=+13.2 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-13.2 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & +6.0 \\ & +9.0 \end{aligned}$ | $\begin{gathered} +7.0 \\ +10.5 \end{gathered}$ | - | Vdc |
| $\begin{aligned} & \text { Output Voltage - Low Logic State } \\ & \left(\mathrm{V}_{I H}=1.9 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=+9.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-9.0 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{I H}=1.9 \mathrm{Vdc}, \mathrm{R}_{\mathrm{L}}=3.0 \mathrm{k} \Omega, \mathrm{~V}_{\mathrm{CC}}=+13.2 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-13.2 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{OL}}$ | $\begin{aligned} & -6.0 \\ & -9.0 \end{aligned}$ | $\begin{gathered} -7.0 \\ -10.5 \end{gathered}$ | - | Vdc |
| Positive Output Short-Circuit Current, Note 1 | los+ | +6.0 | + 10 | + 12 | mA |
| Negative Output Short-Circuit Current, Note 1 | los- | -6.0 | - 10 | -12 | mA |
| Output Resistance ( $\left.\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{EE}}=0,\left\|\mathrm{~V}_{\mathrm{O}}\right\|= \pm 2.0 \mathrm{~V}\right)$ | $\mathrm{r}_{0}$ | 300 | - | - | Ohms |
| $\begin{aligned} & \text { Positive Supply Current }\left(\mathrm{R}_{\mathrm{I}}=\infty\right) \\ & \left(\mathrm{V}_{\mathrm{IH}}=1.9 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{CC}}=+9.0 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{CC}}=+9.0 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{IH}}=1.9 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{CC}}=+12 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{CC}}=+12 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{IH}}=1.9 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{CC}}=+15 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{I}_{\mathrm{Cc}}$ | $\begin{aligned} & - \\ & - \\ & - \\ & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & +15 \\ & +4.5 \\ & +19 \\ & +5.5 \end{aligned}$ | $\begin{aligned} & +20 \\ & +6.0 \\ & +25 \\ & +7.0 \\ & +34 \\ & +12 \end{aligned}$ | mA |
| $\begin{gathered} \text { Negative Supply Current }\left(R_{L}=\infty\right) \\ \left(V_{I H}=1.9 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-9.0 \mathrm{Vdc}\right) \\ \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-9.0 \mathrm{Vdc}\right) \\ \left(\mathrm{V}_{\mathrm{IH}}=1.9 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-12 \mathrm{Vdc}\right) \\ \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-12 \mathrm{Vdc}\right) \\ \left(\mathrm{V}_{\mathrm{IH}}=1.9 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{Vdc}\right) \\ \left(\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-15 \mathrm{Vdc}\right) \end{gathered}$ | $\mathrm{I}_{\text {EE }}$ | $\begin{aligned} & - \\ & \text { - } \\ & \text { - } \\ & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{gathered} -13 \\ - \\ -18 \\ - \\ - \end{gathered}$ | $\begin{gathered} -17 \\ -500 \\ -23 \\ -500 \\ -34 \\ -2.5 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \\ & \mathrm{~mA} \\ & \mu \mathrm{~A} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Power Consumption $\begin{aligned} & \left(\mathrm{V}_{\mathrm{CC}}=9.0 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-9.0 \mathrm{Vdc}\right) \\ & \left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{EE}}=-12 \mathrm{Vdc}\right) \end{aligned}$ | $\mathrm{P}_{\mathrm{C}}$ | - | - | $\begin{aligned} & 333 \\ & 576 \end{aligned}$ | mW |

SWITCHING CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=+9.0 \pm 1 \% \mathrm{Vdc}, \mathrm{V}_{\mathrm{EE}}=-9.0 \pm 1 \% \mathrm{Vdc}, \mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}\right.$. $)$

| Propagation Delay Time $\left(z_{l}=3.0 \mathrm{k}\right.$ and 15 pF$)$ | $\mathrm{t}_{\text {PLH }}$ | - | 275 | 350 | ns |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Fall Time | $\left(z_{l}=3.0 \mathrm{k}\right.$ and 15 pF$)$ | $\mathrm{t}_{\text {THL }}$ | - | 45 | 75 |
| Propagation Delay Time | $\left(z_{l}=3.0 \mathrm{k}\right.$ and 15 pF$)$ | $\mathrm{t}_{\text {PHL }}$ | - | 110 | 175 |
| Rise Time | $\left(z_{l}=3.0 \mathrm{k}\right.$ and 15 pF$)$ | $\mathrm{t}_{\text {TLH }}$ | - | 55 | 100 |

NOTE: 1. Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

## CHARACTERISTIC DEFINITIONS



Figure 1. Input Current

Figure 3. Output Short-Circuit Current



Figure 2. Output Voltage


Figure 4. Output Resistance (Power Off)


Figure 5. Power Supply Currents


Figure 6. Switching Response

MC1488

TYPICAL CHARACTERISTICS
( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)


Figure 7. Transfer Characteristics versus Power Supply Voltage


Figure 9. Output Slew Rate versus Load Capacitance


Figure 8. Short Circuit Output Current versus Temperature


Figure 10. Output Voltage and Current-Limiting Characteristics


Figure 11. Maximum Operating Temperature versus Power Supply Voltage

## APPLICATIONS INFORMATION

The Electronic Industries Association EIA-232D specification details the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5.0 and 15 V in magnitude and are positive for a Logic " 0 " and negative for a Logic " 1 ." These voltages are so defined when the drivers are terminated with a 3000 to $7000 \Omega$ resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into EIA-232D levels with one stage of inversion.

The EIA-232D specification further requires that during transitions, the driver output slew rate must not exceed 30 V per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $\mathrm{C}=\mathrm{I}_{\mathrm{OS}} \times \Delta \mathrm{T} / \Delta \mathrm{V}$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per microsecond.


Figure 12. Slew Rate versus Capacitance for $\mathrm{I}_{\mathrm{SC}}=10 \mathrm{~mA}$

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus $15 \mathrm{~V}, 500 \mathrm{~mA}$ source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power supply voltages are greater than 9.0 V (i.e., $\mathrm{V}_{\mathrm{CC}} \geqslant 9.0 \mathrm{~V}$; $\mathrm{V}_{\mathrm{EE}} \leqslant-9.0 \mathrm{~V}$ ). In some
power supply designs, a loss of system power causes a low impedance on the power supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the $300 \Omega$ output resistors to ground. If all four outputs were then shorted to plus or minus 15 V , the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power supplies of the drivers, a diode should be placed in each power supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the $\pm 25$ V limits specified in the earlier Standard EIA-232B.) The addition of the diodes also permits the MC1488 to withstand faults with power supplies of less than the 9.0 V stated above.


Figure 13. Power Supply Protection to Meet Power Off Fault Conditions

The maximum short circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

## Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting - this enables the circuit designer to define the output voltage levels independent of power supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.
2. Power Supply Range - as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power supplies. In fact, the positive supply can vary from a minimum 7.0 V (required for driving the negative pulldown section) to the maximum specified 15 V . The negative supply can vary from approximately -2.5 V to the minimum specified -15 V . The


Figure 14. MDTL/MTTL-to-MOS Translator

MC1488 will drive the output to within 2.0 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current limiting and supply voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving EIA-232D lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.


Figure 15. Logic Translator Applications

## Dual EIA-423/EIA-232D Line Driver

The MC3488A dual is single-ended line driver has been designed to satisfy the requirements of EIA standards EIA-423 and EIA-232D, as well as CCITT X.26, X. 28 and Federal Standard FIDS1030. It is suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from $1.0 \mu$ s to $100 \mu$ s by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility.

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for $V_{E E}$ Supply
- Second Source $\mu$ A9636A

MC3488A

## DUAL <br> EIA-423/EIA-232D <br> DRIVER

SEMICONDUCTOR TECHNICAL DATA


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS


Simplified Application


MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltages | $\mathrm{V}_{\mathrm{CC}}$ | +15 | V |
| Output Current <br> Source <br> Sink | $\mathrm{V}_{\mathrm{EE}}$ | -15 |  |
| Operating Ambient Temperature | $\mathrm{I}_{\mathrm{O}}$ | mA |  |
| Junction Temperature Range | $\mathrm{I}_{-}$ | -150 |  |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | 0 to +70 |  |

RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltages | $\mathrm{V}_{\mathrm{CC}}$ | 10.8 | 12 | 13.2 | V |
|  | $\mathrm{~V}_{\mathrm{EE}}$ | -13.2 | -12 | -10.8 |  |
| Operating Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | 0 | 25 | 70 | ${ }^{\circ} \mathrm{C}$ |
| Wave Shaping Resistor | $\mathrm{R}_{\mathrm{WS}}$ | 10 | - | 1000 | $\mathrm{k} \Omega$ |

TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply over recommended operating conditions)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Voltage - Low Logic State | $\mathrm{V}_{\text {IL }}$ | - | - | 0.8 | V |
| Input Voltage - High Logic State | $\mathrm{V}_{\mathrm{IH}}$ | 2.0 | - | - | V |
| Input Current - Low Logic State $\left(\mathrm{V}_{\mathrm{IL}}=0.4 \mathrm{~V}\right)$ | IIL | -80 | - | - | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Input Current - High Logic State } \\ & \left(\mathrm{V}_{\mathrm{IH}}=2.4 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\mathrm{IH}}=5.5 \mathrm{~V}\right) \end{aligned}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{IH} 1} \\ & \mathrm{I}_{\mathrm{IH}} \end{aligned}$ | - | - | $\begin{gathered} 10 \\ 100 \end{gathered}$ | $\mu \mathrm{A}$ |
| Input Clamp Diode Voltage $\left(\mathrm{I}_{\mathrm{IK}}=-15 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{IK}}$ | -1.5 | - | - | V |
| $\begin{array}{ll} \text { Output Voltage }- \text { Low Logic State } \\ \left(R_{L}=\infty\right) & \text { EIA-423 } \\ \left(R_{L}=3.0 \mathrm{k} \Omega\right) & \text { EIA-232D } \\ \left(R_{L}=450 \Omega\right) & \text { EIA-423 } \end{array}$ | $\mathrm{V}_{\text {OL }}$ | $\begin{aligned} & -6.0 \\ & -6.0 \\ & -6.0 \end{aligned}$ | $\begin{aligned} & - \\ & - \\ & - \end{aligned}$ | $\begin{aligned} & -5.0 \\ & -5.0 \\ & -4.0 \end{aligned}$ | V |
| $$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & 5.0 \\ & 5.0 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 6.0 \\ & 6.0 \end{aligned}$ | V |
| Output Resistance $\left(R_{L} \geqslant 450 \Omega\right)$ | $\mathrm{R}_{\mathrm{O}}$ | - | 25 | 50 | $\Omega$ |
| $\begin{aligned} & \text { Output Short-Circuit Current (Note 2) } \\ & \left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {out }}=0 \mathrm{~V}\right) \\ & \left(\mathrm{V}_{\text {in }}=\mathrm{V}_{\text {IH }}(\text { Min }), V_{\text {out }}=0 \mathrm{~V}\right) \end{aligned}$ | $\begin{aligned} & \text { losh } \\ & \text { losL } \end{aligned}$ | $\begin{aligned} & -150 \\ & +15 \end{aligned}$ | - | $\begin{gathered} -15 \\ +150 \end{gathered}$ | mA |
| Output Leakage Current (Note 3) $\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{EE}}=0 \mathrm{~V},-6.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{O}} \leqslant 6.0 \mathrm{~V}\right)$ | $\mathrm{l}_{\text {ox }}$ | -100 | - | 100 | $\mu \mathrm{A}$ |
| Power Supply Currents $\left(\mathrm{R}_{\mathrm{W}}=100 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{L}}=\infty, \mathrm{V}_{\mathrm{IL}} \leqslant \mathrm{~V}_{\text {in }} \leqslant \mathrm{V}_{\mathrm{IH}}\right)$ | $\begin{aligned} & \mathrm{I}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{EE}} \end{aligned}$ | $-18$ | - | $+18$ | mA |

NOTES: 1. Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation. 2. One output shorted at a time.
3. No $V_{E E}$ diode required.

TRANSITION TIMES (Unless otherwise noted, $C_{L}=30 \mathrm{pF}, \mathrm{f}=1.0 \mathrm{kHz}, \mathrm{V}_{\mathrm{CC}}=-\mathrm{V}_{\mathrm{EE}}=12.0 \mathrm{~V} \pm 10 \%, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{R}_{\mathrm{L}}=450 \Omega$.
Transition times measured $10 \%$ to $90 \%$ and $90 \%$ to $10 \%$ )

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Transition Time, Low-to-High State Output | $\mathrm{t}_{\mathrm{TL}}$ |  |  |  | $\mu \mathrm{s}$ |
| $\left(R_{W}=10 \mathrm{k} \Omega\right)$ |  | 0.8 | - | 1.4 |  |
| $\left(R_{W}=100 \mathrm{k} \Omega\right)$ |  | 8.0 | - | 14 |  |
| $\left(R_{W}=500 \mathrm{k} \Omega\right)$ |  | - | 70 |  |  |
| $\left(R_{W}=1000 \mathrm{k} \Omega\right)$ |  | 80 | - | 140 |  |
| Transition Time, High-to-Low State Output | $\mathrm{t}_{T H L}$ |  |  |  |  |
| $\left(R_{W}=10 \mathrm{k} \Omega\right)$ |  | 0.8 | - | 1.4 |  |
| $\left(R_{W}=100 \mathrm{k} \Omega\right)$ |  | 8.0 | - | 14 |  |
| $\left(R_{W}=500 \mathrm{k} \Omega\right)$ | 40 | - | 70 |  |  |
| $\left(R_{W}=1000 \mathrm{k} \Omega\right)$ |  | 80 | - | 140 |  |



Figure 1. Test Circuit and Waveforms for Transition Times


Figure 2. Output Transition Times versus Wave Shape Resistor Value


Figure 3. Input/Output Characteristics versus Temperature


Figure 4. Output Current versus Output Voltage


Figure 5. Supply Current versus Temperature


Figure 6. Rise/Fall Time versus $\mathrm{R}_{\text {Ws }}$

## MC26LS30

## Dual Differential

## (EIA-422-A)/ <br> Quad Single-Ended

 (EIA-423-A) Line DriversThe MC26LS30 is a low power Schottky set of line drivers which can be configured as two differential drivers which comply with EIA-422-A standards, or as four single-ended drivers which comply with EIA-423-A standards. A mode select pin and appropriate choice of power supplies determine the mode. Each driver can source and sink currents in excess of 50 mA .

In the differential mode (EIA-422-A), the drivers can be used up to 10 Mbaud. A disable pin for each driver permits setting the outputs into a high impedance mode within $\mathrm{a}+10 \mathrm{~V}$ common mode range.

In the single-ended mode (EIA-423-A), each driver has a slew rate control pin which permits setting the slew rate of the output signal so as to comply with EIA-423-A and FCC requirements and to reduce crosstalk. When operated from symmetrical supplies (+5.0 V), the outputs exhibit zero imbalance

The MC26LS30 is available in a $16-$ pin surface mount package. Operating temperature range is $-40^{\circ}$ to $+85^{\circ} \mathrm{C}$.

- Operates as Two Differential EIA-422-A Drivers, or Four Single-Ended EIA-423-A Drivers
- High Impedance Outputs in Differential Mode
- Short Circuit Current Limit In Both Source and Sink Modes
- $\pm 10$ V Common Mode Range on High Impedance Outputs
- $\pm 15$ V Range on Inputs
- Low Current PNP Inputs Compatible with TTL, CMOS, and MOS Outputs
- Individual Output Slew Rate Control in Single-Ended Mode
- Replacement for the AMD AM26LS30 and National Semiconductor DS3691


## Representative Block Diagrams

## Single-Ended Mode

 EIA-423-A




Differential Mode
EIA-422-A


Enable CD

$$
\begin{array}{ll}
V_{\mathrm{CC}}-1 & \text { Gnd-5 } \\
\mathrm{V}_{\mathrm{EE}-8} & \text { Mode-4 }
\end{array}
$$



## ON Semiconductor

http://onsemi.com

## MARKING

DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| MC26LS30D | SO-16 | 48 Units/Rail |
| MC26LS30DR2 | SO-16 | 2500 Tape \& Reel |

## MC26LS30

MAXIMUM OPERATING CONDITIONS (Pin numbers refer to SO-16 package only.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | $-0.5,+7.0$ | Vdc |
| Input Voltage (All Inputs) | $\mathrm{V}_{\mathrm{EE}}$ | $-7.0,+0.5$ |  |
| Applied Output Voltage when in High Impedance Mode <br> $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right.$, Pin 4 = Logic 0, Pins 3, 6 = Logic 1) <br> Output Voltage with $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{EE}}=0 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{in}}$ | $-0.5,+20$ | Vdc |
| Output Current | $\mathrm{V}_{\mathrm{za}}$ | $\pm 15$ | Vdc |
| Junction Temperature | $\mathrm{V}_{\mathrm{zb}}$ | $\pm 15$ |  |

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides conditions for actual device operation.

## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltage (Differential Mode) <br> Power Supply Voltage (Single-Ended Mode) | $V_{C C}$ <br> $V_{E E}$ <br> $V_{C C}$ <br> $\mathrm{V}_{\mathrm{EE}}$ | $\begin{gathered} +4.75 \\ -0.5 \\ +4.75 \\ -5.25 \end{gathered}$ | $\begin{gathered} 5.0 \\ 0 \\ +5.0 \\ -5.0 \end{gathered}$ | $\begin{gathered} +5.25 \\ +0.3 \\ +5.25 \\ -4.75 \end{gathered}$ | Vdc |
| Input Voltage (All Inputs) <br> Applied Output Voltage (when in High Impedance Mode) <br> Applied Output Voltage, $\mathrm{V}_{\mathrm{CC}}=0$ | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{in}} \\ & \mathrm{~V}_{\mathrm{za}} \\ & \mathrm{~V}_{\mathrm{zb}} \end{aligned}$ | $\begin{gathered} 0 \\ -10 \\ -10 \end{gathered}$ |  | $\begin{aligned} & +15 \\ & +10 \\ & +10 \end{aligned}$ | Vdc |
| Output Current | 10 | -65 | - | +65 | mA |
| Operating Ambient Temperature (See text) | $\mathrm{T}_{\text {A }}$ | -40 | - | +85 | ${ }^{\circ} \mathrm{C}$ |

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (EIA-422-A differential mode, Pin $4 \leqslant 0.8 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}, 4.75 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{CC}} \leqslant 5.25 \mathrm{~V}$, $\mathrm{V}_{\mathrm{EE}}=$ Gnd, unless otherwise noted. Pin numbers refer to SO-16 package only.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage (see Figure 1) <br> Differential, $\mathrm{R}_{\mathrm{L}}=\infty, \mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}$ <br> Differential, $R_{L}=100 \Omega, V_{C C}=4.75 \mathrm{~V}$ <br> Change in Differential Voltage, $\mathrm{R}_{\mathrm{L}}=100 \Omega$ (Note 4) <br> Offset Voltage, $\mathrm{R}_{\mathrm{L}}=100 \Omega$ <br> Change in Offset Voltage*, $\mathrm{R}_{\mathrm{L}}=100 \Omega$ | $\left\|V_{O D 1}\right\|$ <br> $\mid V_{\mathrm{OD} 2}$ <br> $\left\|\Delta \mathrm{V}_{\mathrm{OD} 2}\right\|$ <br> $\mathrm{V}_{\mathrm{OS}}$ <br> $\left\|\Delta V_{\text {OS }}\right\|$ | $2.0$ | $\begin{aligned} & 4.2 \\ & 2.6 \\ & 10 \\ & 2.5 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{gathered} 6.0 \\ - \\ 400 \\ 3.0 \\ 400 \end{gathered}$ | Vdc <br> Vdc <br> mVdc <br> Vdc <br> mVdc |
| Output Current (each output) <br> Power Off Leakage, $\mathrm{V}_{\mathrm{CC}}=0,-10 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{O}} \leqslant+10 \mathrm{~V}$ <br> High Impedance Mode, $\mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V},-10 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{O}} \leqslant+10 \mathrm{~V}$ <br> Short Circuit Current (Note 2) <br> High Output Shorted to Pin $5\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ <br> High Output Shorted to Pin $5\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+85^{\circ} \mathrm{C}\right)$ <br> Low Output Shorted to $+6.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$ <br> Low Output Shorted to $+6.0 \mathrm{~V}\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+85^{\circ} \mathrm{C}\right)$ | $\begin{gathered} \mathrm{l}_{\mathrm{OLK}} \\ \mathrm{I}_{\mathrm{OZ}} \\ \mathrm{I}_{\mathrm{SC}-} \\ \mathrm{I}_{\mathrm{SC}-} \\ \mathrm{ISC}_{+} \\ \mathrm{I}_{\mathrm{SC}+} \\ \hline \end{gathered}$ | $\begin{gathered} -100 \\ -100 \\ \\ -150 \\ -150 \\ 60 \\ 50 \end{gathered}$ | 0 0 -95 - 75 | $\begin{array}{r} +100 \\ +100 \\ \\ -60 \\ -50 \\ 150 \\ 150 \end{array}$ | $\mu \mathrm{A}$ <br> mA |
| Inputs <br> Low Level Voltage <br> High Level Voltage <br> Current @ $\mathrm{V}_{\text {in }}=2.4 \mathrm{~V}$ <br> Current @ $\mathrm{V}_{\text {in }}=15 \mathrm{~V}$ <br> Current @ $\mathrm{V}_{\text {in }}=0.4 \mathrm{~V}$ <br> Current, $0 \leqslant \mathrm{~V}_{\text {in }} \leqslant 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=0$ <br> Clamp Voltage ( $\mathrm{l}_{\text {in }}=-12 \mathrm{~mA}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{IL}} \\ & \mathrm{~V}_{\mathrm{IH}} \\ & I_{\mathrm{IH}} \\ & I_{\mathrm{HH}} \\ & \mathrm{I}_{\mathrm{IL}} \\ & \mathrm{I}_{\mathrm{IX}} \\ & \mathrm{~V} \end{aligned}$ | $\begin{gathered} - \\ 2.0 \\ - \\ - \\ -200 \\ - \\ -1.5 \end{gathered}$ | $\begin{gathered} 0 \\ 0 \\ -8.0 \\ 0 \end{gathered}$ | $\begin{gathered} 0.8 \\ - \\ 40 \\ 100 \end{gathered}$ | Vdc <br> Vdc <br> $\mu \mathrm{A}$ <br> Vdc |
| Power Supply Current ( $\mathrm{V}_{\mathrm{CC}}=+5.25 \mathrm{~V}$, Outputs Open) ( $0 \leqslant$ Enable $\leqslant \mathrm{V}_{\mathrm{CC}}$ ) | $\mathrm{I}_{\mathrm{CC}}$ | - | 16 | 30 | mA |

TIMING CHARACTERISTICS (EIA-422-A differential mode, Pin $4 \leqslant 0.8 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=\mathrm{Gnd}$, (Notes 1 and 3) unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Differential Output Rise Time (Figure 3) | $\mathrm{tr}_{r}$ | - | 70 | 200 | ns |
| Differential Output Fall Time (Figure 3) | $\mathrm{t}_{\mathrm{f}}$ | - | 70 | 200 | ns |
| Propagation Delay Time - Input to Differential Output Input Low to High (Figure 3) Input High to Low (Figure 3) | $t_{\text {PDH }}$ tpDL |  | 90 90 | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | ns |
| Skew Timing (Figure 3) <br> \| $t_{\text {PDH }}$ to $t_{\text {PDL }} \mid$ for Each Driver Max to Min tPDH Within a Package Max to Min tpDL Within a Package | ${ }^{\text {tsK1 }}$ <br> ${ }^{\text {tsK2 }}$ <br> ${ }^{\text {tsK3 }}$ | - | 9.0 2.0 2.0 |  | ns |
| Enable Timing (Figure 4) <br> Enable to Active High Differential Output Enable to Active Low Differential Output Enable to 3-State Output From Active High Enable to 3-State Output From Active Low | $\begin{aligned} & \text { tpZH } \\ & \text { tpPL } \\ & \text { tpHZ }^{\prime} \\ & t_{\text {PLZ }} \end{aligned}$ | - | $\begin{gathered} 150 \\ 190 \\ 80 \\ 110 \end{gathered}$ | $\begin{aligned} & 300 \\ & 350 \\ & 350 \\ & 300 \end{aligned}$ | ns |

1. All voltages measured with respect to Pin 5 .
2. Only one output shorted at a time, for not more than 1 second.
3. Typical values established at $+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}$.
4. $\mathrm{V}_{\text {in }}$ switched from 0.8 to 2.0 V .
5. Imbalance is the difference between $\left|\mathrm{V}_{\mathrm{O} 2}\right|$ with $\mathrm{V}_{\text {in }}<0.8 \mathrm{~V}$ and $\left|\mathrm{V}_{\mathrm{O} 2}\right|$ with $\mathrm{V}_{\text {in }}>2.0 \mathrm{~V}$.

ELECTRICAL CHARACTERISTICS (EIA-423-A single-ended mode, Pin $4 \geqslant 2.0 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<85^{\circ} \mathrm{C}, 4.75 \mathrm{~V} \leqslant\left|\mathrm{~V}_{\mathrm{CC}}\right|$, $\left|\mathrm{V}_{\mathrm{EE}}\right| \leqslant 5.25 \mathrm{~V}$, (Notes 1 and 3 ) unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage ( $\mathrm{V}_{\mathrm{CC}}=\left\|\mathrm{V}_{\mathrm{EE}}\right\|=4.75 \mathrm{~V}$ ) <br> Single-Ended Voltage, $\mathrm{R}_{\mathrm{L}}=\infty$ (Figure 2) <br> Single-Ended Voltage, $\mathrm{R}_{\mathrm{L}}=450 \Omega$, (Figure 2) <br> Voltage Imbalance (Note 5), $\mathrm{R}_{\mathrm{L}}=450 \Omega$ | $\left\|\mathrm{V}_{\mathrm{O} 1}\right\|$ $\left\|\mathrm{V}_{\mathrm{O}}\right\|$ $\left\|\Delta \mathrm{V}_{\mathrm{O} 2}\right\|$ | $\begin{aligned} & 4.0 \\ & 3.6 \end{aligned}$ | $\begin{gathered} 4.2 \\ 3.95 \\ 0.05 \end{gathered}$ | $\begin{aligned} & 6.0 \\ & 6.0 \\ & 0.4 \end{aligned}$ | Vdc |
| Slew Control Current (Pins 16, 13, 12, 9) | ISLEW | - | $\pm 120$ | - | $\mu \mathrm{A}$ |
| Output Current (Each Output) <br> Power Off Leakage, $\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{EE}}=0,-6.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{O}} \leqslant+6.0 \mathrm{~V}$ Short Circuit Current (Output Short to Ground, Note 2) $\begin{aligned} & \mathrm{V}_{\text {in }} \leqslant 0.8 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \mathrm{V}_{\text {in }} \leqslant 0.8 \mathrm{~V}\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+85^{\circ} \mathrm{C}\right) \\ & \mathrm{V}_{\text {in }} \geq 2.0 \mathrm{~V}\left(\mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right) \\ & \mathrm{V}_{\text {in }} \geq 2.0 \mathrm{~V}\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<+85^{\circ} \mathrm{C}\right) \end{aligned}$ | lolk <br> $I_{\mathrm{SC}+}$ <br> ${ }^{\mathrm{ISC}}+$ <br> Isc- <br> $\mathrm{I}_{\mathrm{SC}}$ | $\begin{gathered} -100 \\ 60 \\ 50 \\ -150 \\ -150 \\ \hline \end{gathered}$ | $\begin{gathered} 0 \\ 80 \\ - \\ -95 \end{gathered}$ | $\begin{array}{r} +100 \\ 150 \\ 150 \\ -60 \\ -50 \end{array}$ | $\begin{aligned} & \mu \mathrm{A} \\ & \mathrm{~mA} \end{aligned}$ |
| Inputs <br> Low Level Voltage <br> High Level Voltage <br> Current @ $\mathrm{V}_{\text {in }}=2.4 \mathrm{~V}$ <br> Current @ $\mathrm{V}_{\text {in }}=15 \mathrm{~V}$ <br> Current @ $\mathrm{V}_{\text {in }}=0.4 \mathrm{~V}$ <br> Current, $0 \leqslant \mathrm{~V}_{\text {in }} \leqslant 15 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=0$ <br> Clamp Voltage ( $\mathrm{l}_{\text {in }}=-12 \mathrm{~mA}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{IL}} \\ & \mathrm{~V}_{\mathrm{IH}} \\ & I_{I H} \\ & I_{\mathrm{IH}} \\ & I_{\mathrm{IL}} \\ & I_{I X} \\ & V_{I K} \end{aligned}$ | $\begin{gathered} - \\ 2.0 \\ - \\ - \\ -200 \\ - \\ -1.5 \end{gathered}$ | $\begin{gathered} - \\ 0 \\ 0 \\ -8.0 \\ 0 \end{gathered}$ | $\begin{gathered} 0.8 \\ - \\ 40 \\ 100 \\ - \end{gathered}$ | Vdc <br> Vdc <br> $\mu \mathrm{A}$ <br> Vdc |
| Power Supply Current (Outputs Open) $\mathrm{V}_{\mathrm{CC}}=+5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{in}}=0.4 \mathrm{~V}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{EE}} \\ & \hline \end{aligned}$ | $-22$ | $\begin{gathered} 17 \\ -8.0 \end{gathered}$ | $30$ | mA |

TIMING CHARACTERISTICS (EIA-423-A single-ended mode, Pin $4 \geqslant 2.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}$, (Notes 1 and 3) unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Timing (Figure 5) |  |  |  |  |  |
| Output Rise Time, $\mathrm{C}_{\mathrm{C}}=0$ | $\mathrm{t}_{\mathrm{r}}$ | - | 65 | 300 | ns |
| Output Fall Time, $\mathrm{C}_{\mathrm{C}}=0$ | $t_{f}$ | - | 65 | 300 |  |
| Output Rise Time, $\mathrm{C}_{\mathrm{C}}=50 \mathrm{pF}$ | $\mathrm{t}_{\mathrm{r}}$ | - | 3.0 | - | $\mu \mathrm{s}$ |
| Output Fall Time, $\mathrm{C}_{\mathrm{C}}=50 \mathrm{pF}$ | $t_{f}$ | - | 3.0 | - |  |
| Rise Time Coefficient (Figure 16) | $\mathrm{Cr}_{\text {rt }}$ | - | 0.06 | - | $\mu \mathrm{s} / \mathrm{pF}$ |
| Propagation Delay Time, Input to Single Ended Output (Figure 5) |  |  |  |  | ns |
| Input Low to High, $\mathrm{C}_{\mathrm{C}}=0$ | $t_{\text {PD }}$ | - | 100 | 300 |  |
| Input High to Low, $\mathrm{C}_{\mathrm{C}}=0$ | tpDL | - | 100 | 300 |  |
| Skew Timing, $\mathrm{C}_{\mathrm{C}}=0$ (Figure 5) |  |  |  |  | ns |
| $\mid t_{\text {PDH }}$ to tPDL ${ }^{\text {l }}$ for Each Driver | $t_{\text {SK4 }}$ | - | 15 | - |  |
| Max to Min tPDH Within a Package | $\mathrm{t}_{\text {SK5 }}$ | - | 2.0 | - |  |
| Max to Min tpDL Within a Package | $\mathrm{t}_{\text {SK6 }}$ | - | 5.0 | - |  |

1. All voltages measured with respect to Pin 5.
2. Only one output shorted at a time, for not more than 1 second.
3. Typical values established at $+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}$.
4. $V_{\text {in }}$ switched from 0.8 to 2.0 V .
5. Imbalance is the difference between $\left|\mathrm{V}_{\mathrm{O} 2}\right|$ with $\mathrm{V}_{\text {in }}<0.8 \mathrm{~V}$ and $\left|\mathrm{V}_{\mathrm{O} 2}\right|$ with $\mathrm{V}_{\text {in }}>2.0 \mathrm{~V}$.

## MC26LS30

Table 1

| Operation | $\mathrm{V}_{\mathrm{cc}}$ | $\mathrm{V}_{\mathrm{EE}}$ | Inputs |  |  |  |  | Outputs |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Mode | A | B | C | D | A | B | C | D |
| Differential (EIA-422-A) | +5.0 | Gnd | $\begin{aligned} & \hline 0 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 1 \\ & X \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 1 \\ & 1 \\ & 0 \\ & 1 \\ & x \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 1 \\ & Z \\ & 1 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & \hline 1 \\ & 0 \\ & z \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 1 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \\ & \text { Z } \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 1 \\ & 1 \\ & 0 \\ & 1 \\ & z \end{aligned}$ |
| Single-Ended <br> (EIA-423-A) | +5.0 | -5.0 | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | 0 1 0 0 0 | $\begin{aligned} & \hline 0 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ |
| X | 0 | X | X | X | X | X | X | Z | Z | Z | Z |

$X=$ Don't Care
$Z=$ High Impedance (Off)


Figure 1. Differential Output Test


NOTES:

1. S.G. set to: $\mathrm{f} \leqslant 1.0 \mathrm{MHz}$; duty cycle $=50 \%$; $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}, \leqslant 10 \mathrm{~ns}$.
2. $\mathrm{t}_{\mathrm{SK} 1}=\left|\mathrm{t}_{\mathrm{PD}} \mathrm{H}^{-\mathrm{t}_{\text {PDL }}}\right|$ for each driver.
3. $\mathrm{t}_{\text {SK2 }}$ computed by subtracting the shortest $\mathrm{t}_{\text {PDH }}$ from the longest $\mathrm{t}_{\text {PDH }}$ of the 2 drivers within a package.
4. $\mathrm{t}_{\text {SK3 }}$ computed by subtracting the shortest $\mathrm{t}_{\text {PDL }}$ from the longest $\mathrm{t}_{\text {PDL }}$ of the 2 drivers within a package.

Figure 3. Differential Mode Rise/Fall Time and Data Propagation Delay

## MC26LS30



NOTES:

1. S.G. set to: $f \leqslant 1.0 \mathrm{MHz}$; duty cycle $=50 \% ; \mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}, \leqslant 10 \mathrm{~ns}$.
2. Above tests conducted by monitoring output current levels.

Figure 4. Differential Mode Enable Timing


NOTES:

1. S.G. set to: $\mathrm{f} \leqslant 100 \mathrm{kHz}$; duty cycle $=50 \%$; $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}, \leqslant 10 \mathrm{~ns}$.
2. $\mathrm{t}_{\mathrm{SK} 4}=\left|\mathrm{t}_{\mathrm{PDH}}-\mathrm{t}_{\text {PDL }}\right|$ for each driver.
3. $\mathrm{I}_{\text {SK } 5}$ computed by subtracting the shortest $\mathrm{tPDH}^{\text {from }}$ the longest $\mathrm{t}_{\text {PDH }}$ of the 4 drivers within a package
4. $\mathrm{I}_{\text {SK6 }}$ computed by subtracting the shortest $t_{\text {PDL }}$ from the longest $t_{P D L}$ of the 4 drivers within a package.

Figure 5. Single-Ended Mode Rise/Fall Time and Data Propagation Delay


Figure 6. Differential Output Voltage versus Load Current


Figure 8. Short Circuit Current versus Output Voltage


Figure 10. Output Voltage versus Output Source Current


Figure 7. Internal Bias Current versus Load Current

(Pin numbers refer to SO-16 package only.)
Figure 9. Input Current versus Input Voltage


Figure 11. Output Voltage versus Output Sink Current

## MC26LS30



Figure 12. Internal Positive Bias Current versus Load Current


Figure 14. Short Circuit Current versus Output Voltage


Figure 13. Internal Negative Bias Current versus Load Current


Figure 15. Short Circuit Current versus Temperature


Figure 16. Rise/Fall Time versus Capacitance

## APPLICATIONS INFORMATION

(Pin numbers refer to SO-16 package only.)

## Description

The MC26LS30 is a dual function line driver - it can be configured as two differential output drivers which comply with EIA-422-A Standard, or as four single-ended drivers which comply with EIA-423-A Standard. The mode of operation is selected with the Mode pin (Pin 4) and appropriate power supplies (see Table 1). Each of the four outputs is capable of sourcing and sinking 60 to 70 mA while providing sufficient voltage to ensure proper data transmission.

As differential drivers, data rates to 10 Mbaud can be transmitted over a twisted pair for a distance determined by the cable characteristics. EIA-422-A Standard provides guidelines for cable length versus data rate. The advantage of a differential (balanced) system over a single-ended system is greater noise immunity, common mode rejection, and higher data rates.

Where extraneous noise sources are not a problem, the MC26LS30 may be configured as four single-ended drivers transmitting data rates to 100 Kbaud . Crosstalk among wires within a cable is controlled by the use of the slew rate control pins on the MC26LS30.

## Mode Selection (Differential Mode)

In this mode (Pins 4 and 8 at ground), only a +5.0 V supply $\pm 5 \%$ is required at $\mathrm{V}_{\mathrm{CC}}$. Pins 2 and 7 are the driver inputs, while Pins $10,11,14$ and 15 are the outputs (see Block Diagram on page 1). The two outputs of a driver are always complementary and the differential voltage available at each pair of outputs is shown in Figure 6 for $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$. The differential output voltage will vary directly with $\mathrm{V}_{\mathrm{CC}}$. A "high" output can only source current, while a "low" output can only sink current (except for short circuit current - see Figure 8).

The two outputs will be in a high impedance mode when the respective Enable input (Pin 3 or 6) is high, or if $\mathrm{V}_{\mathrm{CC}} \leqslant$ 1.1 V . Output leakage current over a common mode range of $\pm 10 \mathrm{~V}$ is typically less than $1.0 \mu \mathrm{~A}$.

The outputs have short circuit current limiting, typically, less than 100 mA over a voltage range of 0 to +6.0 V (see Figure 8). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Pins $9,12,13$ and 16 are not normally used when in this mode, and should be left open.

## (Single-Ended Mode)

In this mode (Pin $4 \geq 2.0 \mathrm{~V}$ ) $\mathrm{V}_{\mathrm{CC}}$ requires +5.0 V , and $\mathrm{V}_{\mathrm{EE}}$ requires -5.0 V , both $\pm 5.0 \%$. Pins $2,3,6$, and 7 are inputs for the four drivers, and Pins 15, 14, 11, and 10 (respectively) are the outputs. The four drivers are independent of each other, and each output will be at a positive or a negative voltage depending on its input state, the load current, and the supply voltage. Figures $10 \& 11$ indicate the high and low output voltages for $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{EE}}=-5.0 \mathrm{~V}$. The graph
of Figure 10 will vary directly with $\mathrm{V}_{\mathrm{CC}}$, and the graph of Figure 11 will vary directly with $\mathrm{V}_{\mathrm{EE}}$. A "high" output can only source current, while a "low" output can only sink current (except short circuit current - see Figure 14).
The outputs will be in a high impedance mode only if $\mathrm{V}_{\mathrm{CC}} \leqslant 1.1 \mathrm{~V}$. Changing $\mathrm{V}_{\mathrm{EE}}$ to 0 V does not set the outputs to a high impedance mode. Leakage current over a common mode range of $\pm 10 \mathrm{~V}$ is typically less than $1.0 \mu \mathrm{~A}$.
The outputs have short circuit current limiting, typically less than 100 mA over a voltage range of $\pm 6.0 \mathrm{~V}$ (see Figure 14). Short circuits should not be allowed to last indefinitely as the IC may be damaged.
Capacitors connected between Pins 9, 12, 13, and 16 and their respective outputs will provide slew rate limiting of the output transition. Figure 16 indicates the required capacitor value to obtain a desired rise or fall time (measured between the $10 \%$ and $90 \%$ points). The positive and negative transition times will be within $\approx \pm 5 \%$ of each other. Each output may be set to a different slew rate if desired.

## Inputs

The five inputs determine the state of the outputs in accordance with Table 1. All inputs (regardless of the operating mode) have a nominal threshold of +1.3 V , and their voltage must be kept within a range of 0 V to +15 V for proper operation. If an input is taken more than 0.3 V below ground, excessive currents will flow, and the proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. Unused inputs should be connected to ground. The characteristics of the inputs are shown in Figure 9.

## Power Supplies

$\mathrm{V}_{\mathrm{CC}}$ requires $+5.0 \mathrm{~V}, \pm 5 \%$, regardless of the mode of operation. The supply current is determined by the IC's internal bias requirements and the total load current. The internally required current is a function of the load current and is shown in Figure 7 for the differential mode.
In the single-ended mode, $\mathrm{V}_{\text {EE }}$ must be $-5.0 \mathrm{~V}, \pm 5 \%$ in order to comply with EIA-423-A standards. Figures 12 and 13 indicate the internally required bias currents as a function of total load current (the sum of the four output loads). The discontinuity at 0 load current exists due to a change in bias current when the inputs are switched. The supply currents vary $\approx \pm 2.0 \mathrm{~mA}$ as $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{V}_{\mathrm{EE}}$ are varied from $4.75 \mathrm{~V} \mid$ to $|5.25 \mathrm{~V}|$.
Sequencing of the supplies during power-up/ power-down is not required.
Bypass capacitors ( $0.1 \mu \mathrm{~F}$ minimum on each supply pin) are recommended to ensure proper operation. Capacitors reduce noise induced onto the supply lines by the switching action of the drivers, particularly where long P.C. board tracks are involved. Additionally, the capacitors help absorb
transients induced onto the drivers' outputs from the external cable (from ESD, motor noise, nearby computers, etc.).

## Operating Temperature Range

The maximum ambient operating temperature, listed as $+85^{\circ} \mathrm{C}$, is actually a function of the system use (i.e., specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$
P_{D \max }=\frac{T_{J \max }-T_{A}}{R_{\theta J A}}
$$

where $\mathrm{R}_{\theta \mathrm{JA}}=$ package thermal resistance which is typically:
$120^{\circ} \mathrm{C} / \mathrm{W}$ for the SOIC (D) package,
$\mathrm{T}_{\text {Jmax }}=$ max. allowable junction temperature $\left(150^{\circ} \mathrm{C}\right)$
$\mathrm{T}_{\mathrm{A}}=$ ambient air temperature near the IC package.

1) Differential Mode Power Dissipation

For the differential mode, the power dissipated within the package is calculated from:

$$
\mathrm{P}_{\mathrm{D}}=\left[\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{OD}}\right) \times \mathrm{IO}_{\mathrm{O}}\right](\text { each driver })+\left(\mathrm{V}_{\mathrm{CC}} \times \mathrm{I}_{\mathrm{B}}\right)
$$

where: $\quad \mathrm{V}_{\mathrm{CC}}=$ the supply voltage

$$
\begin{aligned}
\mathrm{V}_{\mathrm{OD}}= & \text { is taken from Figure } 6 \text { for the known } \\
& \text { value of } \mathrm{I}_{\mathrm{O}}
\end{aligned}
$$

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the two drivers, while the last term is common to the entire package. Note that the term $\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{OD}}\right)$ is constant for a given value of $\mathrm{I}_{\mathrm{O}}$ and does not vary with $\mathrm{V}_{\mathrm{CC}}$. For an application involving the following conditions:
$\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=-60 \mathrm{~mA}$ (each driver), $\mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}$, the suitability of the package types is calculated as follows.

The power dissipated is:

$$
\begin{aligned}
& \mathrm{PD}=[3.0 \mathrm{~V} \times 60 \mathrm{~mA} \times 2]+(5.25 \mathrm{~V} \times 18 \mathrm{~mA}) \\
& \mathrm{PD}=454 \mathrm{~mW}
\end{aligned}
$$

The junction temperature calculates to:

$$
\begin{aligned}
\mathrm{T} \mathrm{~J}= & 85^{\circ} \mathrm{C}+\left(0.454 \mathrm{~W} \times 120^{\circ} \mathrm{C} / \mathrm{W}\right)=139^{\circ} \mathrm{C} \text { for the } \\
& \text { SOIC package. }
\end{aligned}
$$

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.
2) Single-Ended Mode Power Dissipation

For the single-ended mode, the power dissipated within the package is calculated from:

$$
\begin{aligned}
& \mathrm{PD}_{\mathrm{D}}=\left(\mathrm{I}_{\mathrm{B}}+\times \mathrm{V}_{\mathrm{CC}}\right)+\left(\mathrm{I}_{\mathrm{B}}-\times \mathrm{V}_{\mathrm{EE}}\right)+ \\
& {\left[\left(\mathrm{I}_{\mathrm{O}} \times\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{OH}}\right)\right](\text { each driver })\right.}
\end{aligned}
$$

The above equation assumes $I_{O}$ has the same magnitude for both output states, and makes use of the fact that the absolute value of the graphs of Figures 10 and 11 are nearly identical. $\mathrm{I}_{\mathrm{B}}+$ and $\mathrm{I}_{\mathrm{B}}-$ are obtained from the right half of Figures 12 and 13 , and $\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{OH}}\right)$ can be obtained from Figure 10. Note that the term $\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{OH}}\right)$ is constant for a given value of $\mathrm{I}_{\mathrm{O}}$ and does not vary with $\mathrm{V}_{\mathrm{CC}}$. For an application involving the following conditions:
$\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{O}}=-60 \mathrm{~mA}$ (each driver), $\mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}$, $\mathrm{V}_{\mathrm{EE}}=-5.25 \mathrm{~V}$, the suitability of the package types is calculated as follows.

The power dissipated is:

$$
\begin{aligned}
\mathrm{PD}= & (24 \mathrm{~mA} \times 5.25 \mathrm{~V})+(-3.0 \mathrm{~mA} \times-5.25 \mathrm{~V})+ \\
& {[60 \mathrm{~mA} \times 1.45 \mathrm{~V} \times 4.0] } \\
\mathrm{PD}= & 490 \mathrm{~mW}
\end{aligned}
$$

The junction temperature calculates to:

$$
\begin{aligned}
\mathrm{TJ}= & 85^{\circ} \mathrm{C}+\left(0.490 \mathrm{~W} \times 120^{\circ} \mathrm{C} / \mathrm{W}\right)=144^{\circ} \mathrm{C} \text { for the } \\
& \text { SOIC package. }
\end{aligned}
$$

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.

## SYSTEM EXAMPLES

(Pin numbers refer to SO-16 package only.)

## Differential System

An example of a typical EIA-422-A system is shown in Figure 17. Although EIA-422-A does not specifically address multiple driver situations, the MC26LS30 can be used in this manner since the outputs can be put into a high impedance mode. It is, however, the system designer's responsibility to ensure the Enable pins are properly controlled so as to prevent two drivers on the same cable from being "on" at the same time.

The limit on the number of receivers and drivers which may be connected on one system is determined by the input current of each receiver, the maximum leakage current of each "off" driver, and the DC current through each terminating resistor. The sum of these currents must not exceed the capability of the "on" driver ( $\approx 60 \mathrm{~mA}$ ). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV .

The ground terminals of each driver and receiver in Figure 17 must be connected together by a dedicated wire (or the shield) in the cable to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

## Single-Ended System

An example of a typical EIA-423-A system is shown in Figure 18. Multiple drivers on a single data line are not possible since the drivers cannot be put into a high impedance mode. Although each driver is shown connected to a single receiver, multiple receivers can be driven from a single driver as long as the total load current of the receivers and the terminating resistor does not exceed the capability of the driver $(\approx 60 \mathrm{~mA})$. If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the
minimum voltage across any receiver inputs is never less than 200 mV .
The ground terminals of each driver and receiver in Figure 18 must be connected together by a dedicated wire (or the shield) in the cable so as to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

## Additional Modes of Operation

If compliance with EIA-422-A or EIA-423-A Standard is not required in a particular application, the MC26LS30 can be operated in two other modes.

1) The device may be operated in the differential mode ( Pin $4=0$ ) with $\mathrm{V}_{\text {EE }}$ connected to any voltage between ground and -5.25 V . Outputs in the low state will be referenced to $\mathrm{V}_{\mathrm{EE}}$, resulting in a differential output voltage greater than that shown in Figure 6. The Enable pins will operate the same as previously described.
2) The device may be operated in the single-ended mode (Pin $4=1$ ) with $\mathrm{V}_{\mathrm{EE}}$ connected to any voltage between ground and -5.25 V . Outputs in the high state will be at a voltage as shown in Figure 10, while outputs in a low state will be referenced to $\mathrm{V}_{\mathrm{EE}}$.

## Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 17, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs leading to each receiver and driver should be as short as possible.
In a system such as that depicted in Figure 18, in which data normally travels in one direction only, a terminator is theoretically required only at the receiving end of the cable. However, if the cable is in a location where noise spikes of several volts can be induced onto it, then a terminator (preferably a series resistor) should be placed at the driver end to prevent damage to the driver.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above $\mathrm{V}_{\mathrm{CC}}$ or several volts below ground or $\mathrm{V}_{\mathrm{EE}}$. These overshoots/undershoots can disrupt the driver and/or receiver, create false data, and in some cases, damage components on the bus.

## MC26LS30



1. Terminating resistors $\mathrm{R}_{\mathrm{T}}$ should be located at the physical ends of the cable.
2. Stubs should be as short as possible.
3. Receivers = AM26LS32, MC3486, SN75173 or SN75175.
4. Circuit grounds must be connected together through a dedicated wire.

Figure 17. EIA-422-A Example


Figure 18. EIA-423-A Example

## Quad EIA-485 Line Drivers with Three-State Outputs

The ON Semiconductor MC75172B/174B Quad Line drivers are differential high speed drivers designed to comply with the EIA-485 Standard. Features include three-state outputs, thermal shutdown, and output current limiting in both directions. These devices also comply with EIA-422-A, and CCITT Recommendations V. 11 and X. 27 .

The MC75172B/174B are optimized for balanced multipoint bus transmission at rates in excess of 10 MBPS . The outputs feature wide common mode voltage range, making them suitable for party line applications in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions. These devices offer optimum performance when used with the MC75173 and MC75175 line receivers.

Both devices are available in 16-pin plastic DIP and 20-pin wide body surface mount packages.

- Meets EIA-485 Standard for Party Line Operation
- Meets EIA-422-A and CCITT Recommendations V. 11 and X. 27
- Operating Ambient Temperature: $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
- High Impedance Outputs
- Common Mode Output Voltage Range: -7 to 12 V
- Positive and Negative Current Limiting
- Transmission Rates in Excess of 10 MBPS
- Thermal Shutdown at $150^{\circ} \mathrm{C}$ Junction Temperature, $\left( \pm 20^{\circ} \mathrm{C}\right)$
- Single 5.0 V Supply
- Pin Compatible with TI SN75172/4 and NS $\mu$ A96172/4
- Interchangeable with MC3487 and AM26LS31 for EIA-422-A Applications


## QUAD EIA-485 LINE DRIVERS

SEMICONDUCTOR TECHNICAL DATA


P SUFFIX
PLASTIC PACKAGE
CASE 648

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)


ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| MC75172BDW |  | SO-20L |
| MC75174BDW | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-20L |
| MC75174BP |  | Plastic DIP |

PIN CONNECTIONS


MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | $-0.5,+7.0$ | Vdc |
| Input Voltage (Data, Enable) | $\mathrm{V}_{\text {in }}$ | +7.0 | Vdc |
| Input Current (Data, Enable) | $\mathrm{I}_{\text {in }}$ | -24 | mA |
| Applied Output Voltage, when in 3-State Condition (V $\mathrm{CC}=5.0 \mathrm{~V})$ | $\mathrm{V}_{\mathrm{za}}$ | $-10,+14$ | Vdc |
| Applied Output Voltage, when $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{zb}}$ | $\pm 14$ |  |
| Output Current | $\mathrm{I}_{\mathrm{O}}$ | Self-Limiting | - |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | $-65,+150$ | ${ }^{\circ} \mathrm{C}$ |

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | +4.75 | +5.0 | +5.25 | Vdc |
| Input Voltage (All Inputs) | $\mathrm{V}_{\text {in }}$ | 0 | - | $\mathrm{V}_{\mathrm{CC}}$ | Vdc |
| Output Voltage in 3-State Condition, or when $\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{cm}}$ | -7.0 | - | +12 | Vdc |
| Output Current (Normal data transmission) | $\mathrm{I}_{\mathrm{O}}$ | -65 | - | +65 | mA |
| Operating Ambient Temperature (see text) <br> EIA-485 <br> EIA-422 | $\mathrm{T}_{\mathrm{A}}$ |  |  |  | ${ }^{\circ} \mathrm{C}$ |

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leqslant \mathrm{T}_{\mathrm{A}} \leqslant 85^{\circ} \mathrm{C}, 4.75 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{CC}} \leqslant 5.25 \mathrm{~V}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Voltage <br> Single-Ended Voltage $10=0$ <br> High @ $\mathrm{l}_{\mathrm{O}}=-33 \mathrm{~mA}$ <br> Low @ $\mathrm{I}_{\mathrm{O}}=+33 \mathrm{~mA}$ <br> Differential Voltage <br> Open Circuit ( $\mathrm{l}=0$ ) <br> $\mathrm{R}_{\mathrm{L}}=54 \Omega$ (Figure 1) | $V_{0}$ <br> $\mathrm{V}_{\mathrm{OH}}$ <br> VoL <br> $\left\|V_{O D 1}\right\|$ <br> $\left\|V_{\mathrm{OD} 2}\right\|$ | $\begin{gathered} 0 \\ - \\ - \\ 1.5 \\ 1.5 \end{gathered}$ | $\begin{aligned} & - \\ & 4.0 \\ & 1.6 \\ & \\ & 3.4 \\ & 2.3 \end{aligned}$ | $\begin{gathered} 6.0 \\ - \\ - \\ 6.0 \\ 5.0 \end{gathered}$ | Vdc |
| Change in Differential ${ }^{*}$, $\mathrm{R}_{\mathrm{L}}=54 \Omega$ (Figure 1) <br> Differential Voltage, $\mathrm{R}_{\mathrm{L}}=100 \Omega$ (Figure 1) <br> Change in Differential*, $\mathrm{R}_{\mathrm{L}}=100 \Omega$ (Figure 1) <br> Differential Voltage, $-7.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{cm}} \leqslant 12 \mathrm{~V}$ (Figure 2) <br> Change in Differential ${ }^{*},-7.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{cm}} \leqslant 12 \mathrm{~V}$ (Figure 2) <br> Offset Voltage, $\mathrm{R}_{\mathrm{L}}=54 \Omega$ (Figure 1) <br> Change in Offset ${ }^{*}, R_{L}=54 \Omega$ (Figure 1) | $\left\|\Delta V_{\text {OD2 }}\right\|$ $\left\|\mathrm{V}_{\text {OD2A }}\right\|$ $\left\|\Delta \mathrm{V}_{\text {OD2A }}\right\|$ $\left\|\mathrm{V}_{\mathrm{OD}}\right\|$ $\left\|\Delta \mathrm{V}_{\mathrm{OD} 3}\right\|$ VOS $\left\|\Delta \mathrm{V}_{\text {OS }}\right\|$ | $\begin{gathered} - \\ 1.5 \\ - \\ - \end{gathered}$ | $\begin{gathered} 5.0 \\ 2.2 \\ 5.0 \\ - \\ 5.0 \\ 2.9 \\ 5.0 \end{gathered}$ | $\begin{gathered} 200 \\ - \\ 200 \\ 5.0 \\ 200 \\ - \\ 200 \end{gathered}$ | mVdc Vdc mVdc Vdc mVdc Vdc mVdc |
| Output Current (Each Output) <br> Power Off Leakage, $\mathrm{V}_{\mathrm{CC}}=0,-7.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{O}} \leqslant 12 \mathrm{~V}$ Leakage in 3 -State Mode, $-7.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{O}} \leqslant 12 \mathrm{~V}$ | $\begin{gathered} \mathrm{I}_{\mathrm{O}(\text { off })} \\ \mathrm{I}_{\mathrm{Oz}} \end{gathered}$ | $\begin{aligned} & -50 \\ & -50 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & +50 \\ & +50 \end{aligned}$ | $\mu \mathrm{A}$ |
| Short Circuit Current to Ground <br> Short Circuit Current, $-7.0 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{O}} \leqslant 12 \mathrm{~V}$ | $\begin{aligned} & \mathrm{losR} \\ & \mathrm{los} \end{aligned}$ | $\begin{aligned} & -150 \\ & -250 \end{aligned}$ | - | $\begin{aligned} & +150 \\ & +250 \end{aligned}$ | mA |

[^43]ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leqslant \mathrm{T}_{\mathrm{A}} \leqslant 85^{\circ} \mathrm{C}, 4.75 \mathrm{~V} \leqslant \mathrm{~V}_{\mathrm{CC}} \leqslant 5.25 \mathrm{~V}\right.$, unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ```Inputs Low Level Voltage (Pins 4 & 12, MC75174B only) Low Level Voltage (All Other Pins) High Level Voltage (All Inputs)``` | $\begin{gathered} \mathrm{V}_{\mathrm{IL}(\mathrm{~A})} \\ \mathrm{V}_{\mathrm{IL}(\mathrm{~B})} \\ \mathrm{V}_{\mathrm{IH}} \end{gathered}$ | $\begin{gathered} 0 \\ 0 \\ 2.0 \end{gathered}$ | - | $\begin{gathered} 0.7 \\ 0.8 \\ V_{C C} \end{gathered}$ | Vdc |
| Current @ Vin $=2.7 \mathrm{~V}$ (All Inputs) <br> Current @ $\mathrm{V}_{\text {in }}=0.5 \mathrm{~V}$ (All Inputs) | $\begin{aligned} & \mathrm{I}_{\mathrm{H}} \\ & \mathrm{I}_{\mathrm{IL}} \end{aligned}$ | $-\overline{-100}$ | $\begin{array}{r} 0.2 \\ -15 \end{array}$ | $20$ | $\mu \mathrm{A}$ |
| Clamp Voltage (All Inputs, $\mathrm{I}_{\text {in }}=-18 \mathrm{~mA}$ ) | $\mathrm{V}_{\mathrm{IK}}$ | -1.5 | - | - | Vdc |
| Thermal Shutdown Junction Temperature | $\mathrm{T}_{\mathrm{jts}}$ | - | +150 | - | ${ }^{\circ} \mathrm{C}$ |
| Power Supply Current (Outputs Open, $\mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}$ ) Outputs Enable Outputs Disabled | Icc | - | $\begin{aligned} & 60 \\ & 30 \end{aligned}$ | $\begin{aligned} & 70 \\ & 40 \end{aligned}$ | mA |

TIMING CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right)$

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation Delay - Input to Single-ended Output (Figure 3) Output Low-to-High Output High-to-Low | $\begin{aligned} & \text { tpLH } \\ & \text { tppL }^{2} \end{aligned}$ |  | $\begin{aligned} & 23 \\ & 18 \end{aligned}$ | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ | ns |
| Propagation Delay - Input to Differential Output (Figure 4) Input Low-to-High Input High-to-Low | $\begin{aligned} & \mathrm{tPLH}^{(\mathrm{D})} \\ & \mathrm{t}_{\mathrm{PH}(\mathrm{D})} \end{aligned}$ |  | $\begin{aligned} & 15 \\ & 17 \end{aligned}$ | $\begin{aligned} & 25 \\ & 25 \end{aligned}$ | ns |
| Differential Output Transition Time (Figure 4) | $\mathrm{t}_{\mathrm{dr}}$, $\mathrm{d}_{\mathrm{df}}$ | - | 19 | 25 | ns |
| Skew Timing <br> \| tPLHD - tPHLD $^{\prime}$ for Each Driver Max - Min tpLhD Within a Package Max - Min tphLD Within a Package | tsk1 <br> ${ }^{\text {tsk2 }}$ <br> tsk3 |  | $\begin{aligned} & 0.2 \\ & 1.5 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \text { - } \\ & \text { - } \end{aligned}$ | ns |
| Enable Timing <br> Single-ended Outputs (Figure 5) <br> Enable to Active High Output <br> Enable to Active Low Output <br> Active High to Disable (using Enable) <br> Active Low to Disable (using Enable) <br> Enable to Active High Output (MC75172B only) <br> Enable to Active Low Output (MC75172B only) <br> Active High to Disable (using Enable, MC75172B only) <br> Active Low to Disable (using Enable, MC75172B only) | tpzh(E) $^{\text {(E) }}$ <br> tpzL(E) <br> tphz(E) <br> tpLZ(E) <br> $\mathrm{t}_{\mathrm{PZH}(\mathrm{E})}$ <br> tpzL(E) <br> tpHz(E) <br> tpLZ(E) |  | $\begin{aligned} & 48 \\ & 20 \\ & 35 \\ & 30 \\ & 58 \\ & 28 \\ & 38 \\ & 36 \end{aligned}$ | $\begin{aligned} & 60 \\ & 30 \\ & 45 \\ & 50 \\ & 70 \\ & 35 \\ & 50 \\ & 50 \end{aligned}$ | ns |
| Differential Outputs (Figure 6) <br> Enable to Active Output <br> Enable to Active Output (MC75172B only) <br> Enable to 3-State Output <br> Enable to 3-State Output (MC75172B only) | tpzD(E) <br> tpzD(E) <br> tpDZ(E) <br> tpDZ(E) | - | $\begin{aligned} & 47 \\ & 56 \\ & 32 \\ & 40 \end{aligned}$ | - - - | ns |

## MC75172B MC75174B



Figure 1. $V_{D D}$ Measurement


Figure 2. Common Mode Test


Figure 3. Propagation Delay, Single-Ended Outputs


NOTES: 1. S.G. set to: $\mathrm{f} \leqslant 1.0 \mathrm{MHz}$; duty cycle $=50 \%$; $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}, \leqslant 5.0 \mathrm{~ns}$.
2. $\mathrm{t}_{\text {SK } 1}=$ t $_{\text {PLHD }}-$ t $_{\text {PHLD }} \mid$ for each driver.
3. $\mathrm{t}_{\text {SK2 }}$ computed by subtracting the shortest $t_{\text {PLHD }}$ from the longest $t_{\text {PLHD }}$ of the 4 drivers within a package.

Figure 4. Propagation Delay, Differential Outputs

## MC75172B MC75174B



Figure 5. Enable Timing, Single-Ended Outputs


NOTES: 1. S.G. set to: $\mathrm{f} \leqslant 1.0 \mathrm{MHz}$; duty cycle $=50 \%$; $\mathrm{t}_{\mathrm{f}}, \mathrm{t}_{\mathrm{f}}, \leqslant 5.0 \mathrm{~ns}$.
2. $\mathrm{V}_{\text {in }}$ is inverted for Enable measurements.

Figure 6. Enable Timing, Differential Outputs


Figure 7. Single-Ended Output Voltage versus Output Sink Current


Figure 9. Single-Ended Output Voltage versus Output Source Current


Figure 11. Output Differential Voltage versus Load Current


Figure 8. Single-Ended Output Voltage versus Temperature


Figure 10. Single-Ended Output Voltage versus Temperature


Figure 12. Output Differential Voltage versus Temperature


Figure 13. Output Leakage Current versus Output Voltage


Figure 14. Output Leakage Current versus Temperature


Figure 15. Input Current versus Input Voltage


Figure 16. Short Circuit Current versus Common Mode Voltage

## APPLICATIONS INFORMATION

## Description

The MC75172B and MC75174B are differential line drivers designed to comply with EIA-485 Standard (April 1983) for use in balanced digital multipoint systems containing multiple drivers. The drivers also comply with EIA-422-A and CCITT Recommendations V. 11 and X.27. The drivers meet the EIA-485 requirement for protection from damage in the event that two or more drivers attempt to transmit data simultaneously on the same cable. Data rates in excess of 10 MBPS are possible, depending on the cable length and cable characteristics. A single power supply, $5.0 \mathrm{~V}, \pm 5 \%$, is required at a nominal current of 60 mA , plus load currents.

## Outputs

Each output (when active) will be a low or a high voltage, which depends on the input state and the load current (see Table 1, 2 and Figures 7 to 10). The graphs apply to each driver, regardless of how many other drivers within the package are supplying load current.

Table 1. MC75172B Truth Table

|  | Enables |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: |
| Data Input | EN | EN | Y | Z |
| H | H | X | H | L |
| L | H | X | L | H |
| H | X | L | H | L |
| L | X | L | L | H |
| X | L | H | Z | Z |

Table 2. MC75174B Truth Table

|  |  | Outputs |  |
| :---: | :---: | :---: | :---: |
| Data Input | Enable | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

$\mathrm{H}=$ Logic high, $\mathrm{L}=$ Logic low, $\mathrm{X}=$ Irrelevant, $\mathrm{Z}=$ High impedance
The two outputs of a driver are always complementary. A "high" output can only source current out, while a "low" output can only sink current (except for short circuit current - see Figure 16).

The outputs will be in the high impedance mode when:
a) the Enable inputs are set according to Table 1 or 2;
b) $\mathrm{V}_{\mathrm{CC}}$ is less than 1.5 V ;
c) the junction temperature exceeds the trip point of the thermal shutdown circuit (see below). When in this condition, the output's source and sink capability are shut off, and only leakage currents will flow (see Figures 13, 14). Disabled outputs may be taken to any voltage between -7.0 V and 12 V without damage.

The drivers are protected from short circuits by two methods:
a) Current limiting is provided at each output, in both the source and sink direction, for shorts to any voltage within the range of 12 V to -7.0 V , with respect to circuit ground (see Figure 16). The short circuit current will flow until the fault is removed, or until the thermal shutdown circuit activates (see below). The current limiting circuit has a negative temperature coefficient and requires no resetting upon removal of the fault condition.
b) A thermal shutdown circuit disables the outputs when the junction temperature reaches $150^{\circ} \mathrm{C}$, $\pm 20^{\circ} \mathrm{C}$. The thermal shutdown circuit has a hysteresis of $\approx 12^{\circ} \mathrm{C}$ to prevent oscillations. When this circuit activates, the output stage of each driver is put into the high impedance mode, thereby shutting off the output currents. The remainder of the internal circuitry remains biased. The outputs will become active once again as the IC cools down.

## Driver Inputs

The driver inputs determine the state of the outputs in accordance with Tables 1 and 2. The driver inputs have a nominal threshold of 1.2 V , and their voltage must be kept within the range of 0 V to $\mathrm{V}_{\mathrm{CC}}$ for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The characteristics of the driver inputs are shown in Figure 15. This graph is not affected by the state of the Enable pins.

## Enable Logic

Each driver's outputs are active when the Enable inputs (Pins 4 and 12) are true according to Tables 1 and 2.

The Enable inputs have a nominal threshold of 1.2 V and their voltage must be kept within the range of 0 V to $\mathrm{V}_{\mathrm{CC}}$ for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The Enable input characteristics are shown in Figure 15.

## Operating Temperature Range

The minimum ambient operating temperature is listed as $-40^{\circ} \mathrm{C}$ to meet EIA- 485 specifications, and $0^{\circ} \mathrm{C}$ to meet EIA-422-A specifications. The higher $\mathrm{V}_{\mathrm{OD}}$ required by EIA-422-A is the reason for the narrower temperature range.

The maximum ambient operating temperature (applicable to both EIA-485 and EIA-422-A) is listed as $85^{\circ} \mathrm{C}$. However, a lower ambient may be required depending on system use (i.e. specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$
P D_{\max }=\frac{\mathrm{T}_{\mathrm{Jmax}}{ }^{-\mathrm{T}_{\mathrm{A}}}}{\mathrm{R}_{\theta J A}}
$$

where: $\quad \mathrm{R}_{\theta J \mathrm{~A}}=$ package thermal resistance (typical $70^{\circ} \mathrm{C} / \mathrm{W}$ for the DIP package, $85^{\circ} \mathrm{C} / \mathrm{W}$ for SOIC package);
$\mathrm{T}_{\mathrm{Jmax}}=$ max. operating junction
temperature, and
$\mathrm{T}_{\mathrm{A}}=$ ambient temperature.
Since the thermal shutdown feature has a trip point of $150^{\circ} \mathrm{C}, \pm 20^{\circ} \mathrm{C}, \mathrm{T}_{\text {Jmax }}$ is selected to be $130^{\circ} \mathrm{C}$. The power dissipated within the package is calculated from:
PD

$$
\left.=\left\{\left[\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{OH}}\right) \bullet \mathrm{I}_{\mathrm{OH}}\right]+\mathrm{V}_{\mathrm{OL}} \bullet \mathrm{I}_{\mathrm{OL}}\right)\right\} \text { each }
$$

$$
\text { driver }+\left(\mathrm{V}_{\mathrm{CC}} \bullet \mathrm{I}_{\mathrm{CC}}\right)
$$

where: $\quad \mathrm{V}_{\mathrm{CC}}=$ the supply voltage;
$\mathrm{V}_{\mathrm{OH}}, \mathrm{V}_{\mathrm{OL}}$ are measured or estimated from
Figures 7 to 10;
$\mathrm{I}_{\mathrm{CC}}=$ the quiescent power supply current (typical 60 mA ).
As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last term is common to the entire package.

Example 1: $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{OL}}=\mathrm{I}_{\mathrm{OH}}=55 \mathrm{~mA}$ for each driver, $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$, DIP package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$
\mathrm{PD}_{\max }=\frac{130^{\circ} \mathrm{C}-25^{\circ} \mathrm{C}}{70^{\circ} \mathrm{C} / \mathrm{W}}=1.5 \mathrm{~W}
$$

Since the power supply current of 60 mA dissipates 300 mW , that leaves $1.2 \mathrm{~W}(1.5 \mathrm{~W}-0.3 \mathrm{~W})$ for the drivers. From Figures 7 and $9, \mathrm{~V}_{\mathrm{OL}} \approx 1.75 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{OH}} \approx 3.85 \mathrm{~V}$. The power dissipated in each driver is:
$\{(5.0-3.85) \bullet 0.055\}+(1.75 \bullet 0.055)=160 \mathrm{~mW}$.
Since each driver dissipates 160 mW , the four drivers per package could be used in this application.

Example 2: $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}, \mathrm{I}_{\mathrm{OL}}=27.8 \mathrm{~mA}, \mathrm{I}_{\mathrm{OH}}=20 \mathrm{~mA}$ for each driver, $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$, SOIC package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$
\mathrm{PD}_{\max }=\frac{130^{\circ} \mathrm{C}-85^{\circ} \mathrm{C}}{85^{\circ} \mathrm{C} / \mathrm{W}}=0.53 \mathrm{~W}
$$

Since the power supply current of 60 mA dissipates 300 mW , that leaves $230 \mathrm{~mW}(530 \mathrm{~mW}-300 \mathrm{~mW})$ for the
drivers. From Figures 8 and 10 (adjusted for $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ ), $\mathrm{V}_{\mathrm{OL}} \approx 1.38 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{OH}} \approx 4.27 \mathrm{~V}$. The power dissipated in each driver is:

$$
\{(5.0-4.27) \bullet 0.020\}+(1.38 \bullet 0.0278)=53 \mathrm{~mW}
$$

Since each driver dissipates 53 mW , the use of all four drivers in a package would be marginal. Options include reducing the load current, reducing the ambient temperature, and/or providing a heat sink.

## System Requirements

EIA-485 requires each driver to be capable of transmitting data differentially to at least 32 unit loads, plus an equivalent DC termination resistance of $60 \Omega$, over a common mode voltage of -7.0 to 12 V . A unit load (U.L.), as defined by EIA-485, is shown in Figure 17.


Reprinted from EIA-485, Electronic Industries Association, Washington,DC.

Figure 17. Unit Load Definition

A load current within the shaded regions represents an impedance of less than one U.L., while a load current of a magnitude outside the shaded area is greater than one U.L. A system's total load is the sum of the unit load equivalents of each receiver's input current, and each disabled driver's output leakage current. The $60 \Omega$ termination resistance mentioned above allows for two $120 \Omega$ terminating resistors.
Using the EIA-485 requirements (worst case limits), and the graphs of Figures 7 and 9, it can be determined that the maximum current an MC75172B or MC75174B driver will source or sink is $\approx 65 \mathrm{~mA}$.

## System Example

An example of a typical EIA-485 system is shown in Figure 18. In this example, it is assumed each receiver's input characteristics correspond to 1.0 U.L. as defined in Figure 17. Each "off" driver, with a maximum leakage of $\pm 50 \mu \mathrm{~A}$ over the common mode range, presents a load of $\approx 0.06$ U.L. The total load for the active driver is therefore 8.3 unit loads, plus the parallel combination of the two terminating resistors ( $60 \Omega$ ). It is up to the system software to control the driver Enable pins to ensure that only one driver is active at any time.

## MC75172B MC75174B

## Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 18, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs, leading to each receiver and driver, should be as short as possible.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above $\mathrm{V}_{\mathrm{CC}}$ or below ground. These overshoots and undershoots can disrupt the driver and/or receiver operation, create false data, and in some cases damage components on the bus.


Figure 18. Typical EIA-485 System

Comparing System Requirements

| Characteristic | Symbol | EIA-485 | EIA-422-A | V. 11 and X.27 |
| :---: | :---: | :---: | :---: | :---: | GENERATOR (DRIVER)


| Output Impedance (Note 1) | $\mathrm{Z}_{\text {out }}$ | Not Specified | <100 $\Omega$ | $5010100 \Omega$ |
| :---: | :---: | :---: | :---: | :---: |
| Open Circuit Voltage Differential Single-Ended | $V_{\text {OCD }}$ <br> Vocs | $\begin{aligned} & 1.5 \text { to } 6.0 \mathrm{~V} \\ & <6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \leqslant 6.0 \mathrm{~V} \\ & \leqslant 6.0 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \leqslant 6.0 \mathrm{~V}, \mathrm{w} / 3.9 \mathrm{k} \Omega \text {, Load } \\ & \leqslant 6.0 \mathrm{~V}, \mathrm{w} / 3.9 \mathrm{k} \Omega \text {, Load } \end{aligned}$ |
| Loaded Differential Voltage | $\mathrm{V}_{\text {OD }}$ | 1.5 to $5.0 \mathrm{~V}, \mathrm{w} / 54 \Omega$ load | $\begin{aligned} & \geqslant 2.0 \mathrm{~V} \text { or } \geqslant 0.5 \\ & \mathrm{~V}_{\mathrm{OCD}}, \mathrm{w} / 100 \Omega \text { load } \end{aligned}$ | $\begin{aligned} & \geqslant 2.0 \mathrm{~V} \text { or } \geqslant 0.5 \mathrm{~V}_{\mathrm{OCD}}, \\ & \mathrm{w} / 100 \Omega \text { load } \end{aligned}$ |
| Differential Voltage Balance | $\Delta \mathrm{V}_{\text {OD }}$ | <200 mV | $\leqslant 400 \mathrm{mV}$ | < 400 mV |
| Output Common Mode Range | $V_{\text {CM }}$ | -7.0 to +12 V | Not Specified | Not Specified |
| Offset Voltage | $\mathrm{V}_{\text {OS }}$ | $-1.0<\mathrm{V}_{\mathrm{OS}}<3.0 \mathrm{~V}$ | $\leqslant 3.0 \mathrm{~V}$ | $\leqslant 3.0 \mathrm{~V}$ |
| Offset Voltage Balance | $\Delta \mathrm{V}_{\text {OS }}$ | $<200 \mathrm{mV}$ | $\leqslant 400 \mathrm{mV}$ | $<400 \mathrm{mV}$ |
| Short Circuit Current | los | $\begin{aligned} & \leqslant 250 \mathrm{~mA} \text { for }-7.0 \text { to } \\ & 12 \mathrm{~V} \end{aligned}$ | $\leqslant 150 \mathrm{~mA}$ to ground | $\leqslant 150 \mathrm{~mA}$ to ground |
| Leakage Current ( $\mathrm{V}_{\mathrm{CC}}=0$ ) | loLk | Not Specified | $\begin{aligned} & \leqslant 100 \mu \mathrm{~A} \text { to }-0.25 \mathrm{~V} \\ & \text { thru } 6.0 \mathrm{~V} \end{aligned}$ | $\leqslant 100 \mu \mathrm{~A}$ to $\pm 0.25 \mathrm{~V}$ |
| Output Rise/Fall Time (Note 2) | $\mathrm{tr}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | $\leqslant 0.3 \mathrm{~T}_{\mathrm{B}}, \mathrm{w} / 54 \Omega / 1150 \mathrm{pF}$ load | $\begin{aligned} & \leqslant 0.1 \mathrm{~T}_{\mathrm{B}} \text { or } \leqslant 20 \mathrm{~ns}, \\ & \mathrm{w} / 100 \Omega \text { load } \end{aligned}$ | $\begin{aligned} & \leqslant 0.1 \mathrm{~T}_{\mathrm{B} \text { or }} \leqslant 20 \mathrm{~ns}, \\ & \mathrm{w} / 100 \Omega \text { load } \end{aligned}$ |

## RECEIVER

| Input Sensitivity | $\mathrm{V}_{\text {th }}$ | $\pm 200 \mathrm{mV}$ | $\pm 200 \mathrm{mV}$ | $\pm 300 \mathrm{mV}$ |
| :--- | :---: | :--- | :--- | :--- |
| Input Bias Voltage | $\mathrm{V}_{\text {bias }}$ | $\leqslant 3.0 \mathrm{~V}$ | $\leqslant 3.0 \mathrm{~V}$ | $\leqslant 3.0 \mathrm{~V}$ |
| Input Common Mode Range | $\mathrm{V}_{\mathrm{cm}}$ | -7.0 to 12 V | -7.0 to 7.0 V | -7.0 to 7.0 V |
| Dynamic Input Impedance | $\mathrm{R}_{\text {in }}$ | Spec number of U.L. | $\geqslant 4 \mathrm{k} \Omega$ | $\geqslant 4 \mathrm{k} \Omega$ |

NOTES: 1. Compliance with V. 11 and X. 27 (Blue book) output impedance requires external resistors in series with the outputs of the MC75172B and MC75174B. 2. $\mathrm{T}_{\mathrm{B}}=$ Bit time.

## Additional Information

Copies of the EIA Recommendations (EIA-485 and EIA-422-A) can be obtained from the Electronics Industries Association, Washington, D.C. (202-457-4966). Copies of the CCITT Recommendations (V. 11 and X.27) can be obtained from the United States Department of Commerce, Springfield, VA (703-487-4600).

## Timers

The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode, time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555 Timers
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of $0.005 \%$ per ${ }^{\circ} \mathrm{C}$
- Normally ON or Normally OFF Output
 changing $R$ and $C$ (see Figure 16).

Figure 1. 22 Second Solid State Time Delay Relay Circuit


Figure 2. Representative Block Diagram

## MC1455, MC1455B

## TIMING CIRCUIT

## SEMICONDUCTOR TECHNICAL DATA

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
PSUSFIX
CASE 751
(SO-8)
ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :--- | :---: | :---: |
| MC1455P1 | $T_{A}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | Plastic DIP |
| MC1455D |  | SO-8 |
| MC1455BD | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-8 |
| MC1455BP1 |  |  |
|  |  | Plastic DIP |  |



Test circuit for measuring DC parameters (to set output and measure parameters):
a) When $V_{S} \geq 2 / 3 V_{C C}, V_{O}$ is low.
b) When $\mathrm{V}_{S} \leq 1 / 3 \mathrm{~V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{O}}$ is high.
c) When $\mathrm{V}_{\mathrm{O}}$ is low, Pin 7 sinks current. To test for Reset, set $\mathrm{V}_{\mathrm{O}}$ high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to $\mathrm{V}_{\mathrm{Cc}}$.

Figure 3. General Test Circuit

MAXIMUM RATINGS ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | +18 | Vdc |
| Discharge Current (Pin 7) | $\mathrm{I}_{7}$ | 200 | mA |
| Power Dissipation (Package Limitation) |  |  |  |
| P1 Suffix, Plastic Package | $\mathrm{P}_{\mathrm{D}}$ | 625 | mW |
| Derate above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | 5.0 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| $\mathrm{D} \mathrm{Suffix} Plastic Package$, | 625 | mW |  |
| Derate above $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ |  | 160 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature Range (Ambient) | $\mathrm{T}_{\mathrm{A}}$ |  | ${ }^{\circ} \mathrm{C}$ |
| MC1455B |  | -40 to +85 |  |
| MC1455 |  | 0 to +70 |  |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=+5.0 \mathrm{~V}\right.$ to +15 V , unless otherwise noted.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Supply Voltage Range | $\mathrm{V}_{\mathrm{CC}}$ | 4.5 | - | 16 | V |
| Supply Current $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty \\ & \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=\infty, \text { Low State (Note 1) } \end{aligned}$ | Icc | - | $\begin{aligned} & 3.0 \\ & 10 \end{aligned}$ | $\begin{aligned} & 6.0 \\ & 15 \end{aligned}$ | mA |
| ```Timing Error (R=1.0 k\Omega to 100 k\Omega) (Note 2) Initial Accuracy C = 0.1 \muF Drift with Temperature Drift with Supply Voltage``` |  |  | $\begin{aligned} & 1.0 \\ & 50 \\ & 0.1 \end{aligned}$ | - | $\begin{gathered} \% \\ \text { PPM } /{ }^{\circ} \mathrm{C} \end{gathered}$ $\% / V$ |
| Threshold Voltage/Supply Voltage | $\mathrm{V}_{\text {th }} / \mathrm{V}_{\text {cc }}$ | - | 2/3 | - |  |
| $\begin{gathered} \text { Trigger Voltage } \\ \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \end{gathered}$ | $\mathrm{V}_{\mathrm{T}}$ | - | $\begin{gathered} 5.0 \\ 1.67 \end{gathered}$ | - | V |
| Trigger Current | $\mathrm{I}_{\mathrm{T}}$ | - | 0.5 | - | $\mu \mathrm{A}$ |
| Reset Voltage | $\mathrm{V}_{\text {R }}$ | 0.4 | 0.7 | 1.0 | V |
| Reset Current | $\mathrm{I}_{\mathrm{R}}$ | - | 0.1 | - | mA |
| Threshold Current (Note 3) | $\mathrm{Ith}^{\text {then }}$ | - | 0.1 | 0.25 | $\mu \mathrm{A}$ |
| Discharge Leakage Current (Pin 7) | $\mathrm{I}_{\text {dischg }}$ | - | - | 100 | nA |
| $\begin{aligned} & \text { Control Voltage Level } \\ & \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{CL}}$ | $\begin{aligned} & 9.0 \\ & 2.6 \end{aligned}$ | $\begin{gathered} 10 \\ 3.33 \end{gathered}$ | $\begin{aligned} & 11 \\ & 4.0 \end{aligned}$ | V |
| $\begin{aligned} & \text { Output Voltage Low } \\ & I_{\text {Sink }}=10 \mathrm{~mA}\left(\mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ & I_{\text {Sink }}=50 \mathrm{~mA}\left(\mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ & I_{\text {Sink }}=100 \mathrm{~mA}\left(\mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ & I_{\text {Sink }}=200 \mathrm{~mA}\left(\mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}\right) \\ & I_{\text {Sink }}=8.0 \mathrm{~mA}\left(\mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right) \\ & I_{\text {Sink }}=5.0 \mathrm{~mA}\left(\mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{OL}}$ | $\begin{aligned} & \text { - } \\ & \text { - } \\ & \text { - } \end{aligned}$ | $\begin{gathered} 0.1 \\ 0.4 \\ 2.0 \\ 2.5 \\ - \\ 0.25 \end{gathered}$ | $\begin{gathered} 0.25 \\ 0.75 \\ 2.5 \\ - \\ - \\ 0.35 \end{gathered}$ | V |
| $\begin{aligned} & \text { Output Voltage High } \\ & \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\left(\text { I Source }^{2}=200 \mathrm{~mA}\right) \\ & \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\left(I_{\text {Source }}=100 \mathrm{~mA}\right) \\ & \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}(\text { I Source }=100 \mathrm{~mA}) \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{gathered} - \\ 12.75 \\ 2.75 \end{gathered}$ | $\begin{gathered} 12.5 \\ 13.3 \\ 3.3 \end{gathered}$ | - | V |
| Rise Time Differential Output | $\mathrm{t}_{\mathrm{r}}$ | - | 100 | - | ns |
| Fall Time Differential Output | $\mathrm{t}_{\mathrm{f}}$ | - | 100 | - | ns |

NOTES: 1 . Supply current when output is high is typically 1.0 mA less.
2. Tested at $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}$ Monostable mode.
3. This will determine the maximum value of $R_{A}+R_{B}$ for 15 V operation. The maximum total $R=20 M \Omega$.

## MC1455, MC1455B



Figure 4. Trigger Pulse Width


Figure 5. Supply Current


Figure 6. High Output Voltage


Figure 8. Low Output Voltage @ $\mathrm{V}_{\mathrm{cc}}=10 \mathrm{Vdc}$


Figure 7. Low Output Voltage @ $\mathrm{V}_{\mathrm{Cc}}=5.0 \mathrm{Vdc}$


Figure 9. Low Output Voltage
@ $V_{c c}=15$ Vdc

## MC1455, MC1455B



Figure 10. Delay Time versus Supply Voltage


Figure 11. Delay Time versus Temperature


Figure 12. Propagation Delay versus Trigger Voltage


Figure 13. Representative Circuit Schematic

## GENERAL OPERATION

The MC1455 is a monolithic timing circuit which uses an external resistor - capacitor network as its timing element. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

## Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode (refer to circuit in Figure 14). When the input voltage to the trigger comparator falls below $1 / 3 \mathrm{~V}_{\mathrm{CC}}$, the comparator output triggers the flip-flop so that its output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches $2 / 3 \mathrm{~V}_{\mathrm{CC}}$, the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop
has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t=1.1 \mathrm{R}_{\mathrm{A}} \mathrm{C}$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor, thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.


Figure 14. Monostable Circuit


Figure 15. Monostable Waveforms


Figure 17. Astable Circuit

## Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between $1 / 3 V_{C C}$ and $2 / 3 V_{C C}$. See Figure 17.

The external capacitor changes to $2 / 3 \mathrm{~V}_{\mathrm{CC}}$ through $\mathrm{R}_{\mathrm{A}}$ and $R_{B}$ and discharges to $1 / 3 V_{C C}$ through $R_{B}$. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.
The charge time (output high) is given by:

$$
t_{1}=0.695\left(R_{A}+R_{B}\right) C
$$

The discharge time (output low) is given by:

$$
t_{2}=0.695\left(R_{B}\right) C
$$

Thus the total period is given by:

$$
T=t_{1}+t_{2}=0.695\left(R_{A}+2 R_{B}\right) C
$$

The frequency of oscillation is then: $f=\frac{1}{T}=\frac{1.44}{\left(R_{A}+2 R_{B}\right) C}$ and may be easily found as shown in Figure 19.
The duty cycle is given by: $D C=\frac{R_{B}}{R_{A}+2 R_{B}}$
To obtain the maximum duty cycle $\mathrm{R}_{\mathrm{A}}$ must be as small as possible; but it must also be large enough to limit the


Figure 16. Time Delay

$\mathrm{t}=20 \mu \mathrm{~s} / \mathrm{cm}$
$\left(R_{A}=5.1 \mathrm{k} \Omega, C=0.01 \mu \mathrm{~F}, \mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k} \Omega ; \mathrm{R}_{\mathrm{B}}=3.9 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{CC}}=15 \mathrm{~V}\right)$
Figure 18. Astable Waveforms
discharge current (Pin 7 current) within the maximum rating of the discharge transistor ( 200 mA ).

The minimum value of $\mathrm{R}_{\mathrm{A}}$ is given by:

$$
\mathrm{R}_{\mathrm{A}} \geq \frac{\mathrm{V}_{\mathrm{Cc}}(\mathrm{Vdc})}{17(\mathrm{~A})} \geq \frac{\mathrm{V}_{\mathrm{CC}}(\mathrm{Vdc})}{0.2}
$$



Figure 19. Free Running Frequency

## MC1455, MC1455B

## APPLICATIONS INFORMATION

## Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from $0 \mathrm{~V}_{\mathrm{CC}}$ to $2 / 3 \mathrm{~V}_{\mathrm{CC}}$. The linear ramp time is given by:

$$
t=\frac{2}{3} \frac{V_{C C}}{1} \text {, where } I=\frac{V_{C C}-V_{B}-V_{B E}}{R_{E}}
$$

If $V_{B}$ is much larger than $V_{B E}$, then $t$ can be made independent of $\mathrm{V}_{\mathrm{CC}}$.


Figure 20. Linear Voltage Sweep Circuit

$\mathrm{t}=100 \mu \mathrm{~s} / \mathrm{cm}$
$\left(R_{E}=10 \mathrm{k} \Omega, \mathrm{R} 2=100 \mathrm{k} \Omega, \mathrm{R} 1=39 \mathrm{k} \Omega, \mathrm{C}=0.01 \mu \mathrm{~F}, \mathrm{~V} \mathrm{CC}=15 \mathrm{~V}\right)$
Figure 22. Linear Voltage Ramp Waveforms

## Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.


Figure 21. Missing Pulse Detector

$\mathrm{t}=500 \mu \mathrm{~s} / \mathrm{cm}$
$\left(R_{A}=2.0 \mathrm{k} \Omega, R_{L}=1.0 \mathrm{k} \Omega, \mathrm{C}=0.01 \mu \mathrm{~F}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}\right)$
Figure 23. Missing Pulse Detector Waveforms

## Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monstable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.


Figure 24. Pulse Width Modulator

$\mathrm{t}=0.5 \mathrm{~ms} / \mathrm{cm}$
$\left(\mathrm{R}_{\mathrm{A}}=10 \mathrm{k} \Omega, \mathrm{C}=0.02 \mu \mathrm{~F}, \mathrm{~V}_{\mathrm{CC}}=15 \mathrm{~V}\right)$
Figure 25. Pulse Width Modulation Waveforms

## Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms . The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.


Figure 26. Sequential Timer

## MC1496, MC1496B

## Balanced Modulators/ Demodulators

These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See ON Semiconductor Application Note AN531 for additional design information.

- Excellent Carrier Suppression -65 dB typ @ 0.5 MHz

$$
-50 \mathrm{~dB} \text { typ @ } 10 \mathrm{MHz}
$$

- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection -85 dB typical

This device contains 8 active transistors.


Figure 1. Suppressed Carrier Output Waveform


Figure 3. Amplitude Modulation Output Waveform


## ON Semiconductor ${ }^{\text {T }}$

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SO-14
DSUFFIX
CASE 751A

PIN CONNECTIONS


ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 3026 of this data sheet.

## DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 3026 of this data sheet.


Figure 4. Amplitude-Modulation Spectrum

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Applied Voltage <br> (V6-V8, V10-V1, V12-V8, V12-V10, V8-V4, V8-V1, V10-V4, V6-V10, V2-V5, V3-V5) | $\Delta \mathrm{V}$ | 30 | Vdc |
| Differential Input Signal | $\begin{aligned} & \mathrm{V} 8-\mathrm{V} 10 \\ & \mathrm{~V} 4-\mathrm{V} 1 \end{aligned}$ | $\begin{gathered} +5.0 \\ \pm\left(5+15 R_{e}\right) \end{gathered}$ | Vdc |
| Maximum Bias Current | $\mathrm{I}_{5}$ | 10 | mA |
| Thermal Resistance, Junction-to-Air Plastic Dual In-Line Package | $\mathrm{R}_{\theta \mathrm{JA}}$ | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\begin{array}{ll}\text { Operating Ambient Temperature Range } & \text { MC1496 } \\ & \text { MC1496B }\end{array}$ | $\mathrm{T}_{\text {A }}$ | $\begin{gathered} 0 \text { to }+70 \\ -40 \text { to }+125 \end{gathered}$ | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

NOTE: ESD data available upon request.
ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=12 \mathrm{Vdc}, \mathrm{V}_{\mathrm{EE}}=-8.0 \mathrm{Vdc}, 15=1.0 \mathrm{mAdc}, \mathrm{R}_{\mathrm{L}}=3.9 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{e}}=1.0 \mathrm{k} \Omega, \mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$, all input and output characteristics are single-ended, unless otherwise noted.) (Note 1)

| Characteristic | Fig. | Note | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Carrier Feedthrough <br> $\mathrm{V}_{\mathrm{C}}=60 \mathrm{mVrms}$ sine wave and offset adjusted to zero <br> $\mathrm{V}_{\mathrm{C}}=300 \mathrm{mVpp}$ square wave: $\begin{aligned} & \mathrm{f}_{\mathrm{C}}=1.0 \mathrm{kHz} \\ & \mathrm{f}_{\mathrm{C}}=10 \mathrm{MHz} \end{aligned}$ <br> offset adjusted to zero <br> $\mathrm{f}_{\mathrm{C}}=1.0 \mathrm{kHz}$ <br> offset not adjusted <br> $\mathrm{f}_{\mathrm{C}}=1.0 \mathrm{kHz}$ | 5 | 1 | $\mathrm{V}_{\text {CFT }}$ | _ | $\begin{gathered} 40 \\ 140 \\ 0.04 \\ 20 \end{gathered}$ | $\begin{gathered} 0.4 \\ .00 \end{gathered}$ | $\mu \mathrm{Vrms}$ <br> mVrms |
| Carrier Suppression $\mathrm{f}_{\mathrm{S}}=10 \mathrm{kHz}, 300 \mathrm{mVrms}$ $\mathrm{f}_{\mathrm{C}}=500 \mathrm{kHz}, 60 \mathrm{mVrms}$ sine wave $\mathrm{f}_{\mathrm{C}}=10 \mathrm{MHz}, 60 \mathrm{mVrms}$ sine wave | 5 | 2 | $\mathrm{V}_{\mathrm{CS}}$ | 40 | $\begin{aligned} & 65 \\ & 50 \end{aligned}$ | - | dB <br> k |
| Transadmittance Bandwidth (Magnitude) ( $\mathrm{R}_{\mathrm{L}}=50 \Omega$ ) Carrier Input Port, $\mathrm{V}_{\mathrm{C}}=60 \mathrm{mVrms}$ sine wave $\mathrm{f}_{\mathrm{S}}=1.0 \mathrm{kHz}, 300 \mathrm{mVrms}$ sine wave Signal Input Port, $\mathrm{V}_{\mathrm{S}}=300 \mathrm{mVrms}$ sine wave $\left\|\mathrm{V}_{\mathrm{C}}\right\|=0.5 \mathrm{Vdc}$ | 8 | 8 | $\mathrm{BW}_{3 \mathrm{~dB}}$ | - | $\begin{gathered} 300 \\ 80 \end{gathered}$ |  | MHz |
| Signal Gain ( $\mathrm{V}_{\mathrm{S}}=100 \mathrm{mVrms}, \mathrm{f}=1.0 \mathrm{kHz} ;\left\|\mathrm{V}_{\mathrm{C}}\right\|=0.5 \mathrm{Vdc}$ ) | 10 | 3 | Avs | 2.5 | 3.5 | - | V/V |
| Single-Ended Input Impedance, Signal Port, $f=5.0 \mathrm{MHz}$ Parallel Input Resistance Parallel Input Capacitance | 6 | - | $\begin{aligned} & r_{i p} \\ & \mathrm{c}_{\mathrm{ip}} \end{aligned}$ | - | $\begin{aligned} & 200 \\ & 2.0 \end{aligned}$ | - | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \end{aligned}$ |
| Single-Ended Output Impedance, $\mathrm{f}=10 \mathrm{MHz}$ Parallel Output Resistance Parallel Output Capacitance | 6 | - | $\begin{aligned} & r_{o p} \\ & c_{00} \end{aligned}$ | - | $\begin{aligned} & 40 \\ & 5.0 \end{aligned}$ | - | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{pF} \end{aligned}$ |
| Input Bias Current $I_{b S}=\frac{I 1+14}{2} ; I_{b c}=\frac{18+110}{2}$ | 7 | - | $\begin{aligned} & \mathrm{l}_{\mathrm{bS}} \\ & \mathrm{l}_{\mathrm{cc}} \end{aligned}$ | - | $\begin{aligned} & 12 \\ & 12 \end{aligned}$ | $\begin{aligned} & 30 \\ & 30 \end{aligned}$ | $\mu \mathrm{A}$ |
| Input Offset Current $\mathrm{I}_{\mathrm{ioS}}=11-\mathrm{I} 4 ; \mathrm{I}_{\mathrm{iOC}}=18-\mathrm{I} 10$ | 7 | - | $\begin{array}{\|l\|} \left\lvert\, \begin{array}{l} \|\mathrm{lios}\| \\ \mathrm{I}_{\mathrm{ioC}} \mid \end{array}\right. \end{array}$ | - | $\begin{aligned} & 0.7 \\ & 0.7 \end{aligned}$ | $\begin{aligned} & 7.0 \\ & 7.0 \end{aligned}$ | $\mu \mathrm{A}$ |
| Average Temperature Coefficient of Input Offset Current $\left(\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}\right)$ | 7 | - | $\left\|T C_{\text {lio }}\right\|$ | - | 2.0 | - | $n \mathrm{~A} /{ }^{\circ} \mathrm{C}$ |
| Output Offset Current (16-19) | 7 | - | $\left\|\mathrm{log}_{0}\right\|$ | - | 14 | 80 | $\mu \mathrm{A}$ |
| Average Temperature Coefficient of Output Offset Current $\left(\mathrm{T}_{\mathrm{A}}=-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C}\right)$ | 7 | - | $\left\|T C_{\text {loo }}\right\|$ | - | 90 | - | $n \mathrm{~A} /{ }^{\circ} \mathrm{C}$ |
| Common-Mode Input Swing, Signal Port, $\mathrm{f}_{\mathrm{S}}=1.0 \mathrm{kHz}$ | 9 | 4 | CMV | - | 5.0 | - | Vpp |
| Common-Mode Gain, Signal Port, $\mathrm{f}_{\mathrm{S}}=1.0 \mathrm{kHz},\left\|\mathrm{V}_{\mathrm{C}}\right\|=0.5 \mathrm{Vdc}$ | 9 | - | ACM | - | -85 | - | dB |
| Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9) | 10 | - | $V_{\text {out }}$ | - | 8.0 | - | Vpp |
| Differential Output Voltage Swing Capability | 10 | - | $V_{\text {out }}$ | - | 8.0 | - | Vpp |
| $\begin{array}{ll}\text { Power Supply Current } & \begin{array}{l}16+112 \\ \mathrm{I}\end{array} 14\end{array}$ | 7 | 6 | $\begin{aligned} & \hline \mathrm{I}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{FF}} \end{aligned}$ | - | $\begin{aligned} & \hline 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 4.0 \\ & 5.0 \end{aligned}$ | mAdc |
| DC Power Dissipation | 7 | 5 | $\mathrm{P}_{\mathrm{D}}$ | - | 33 | - | mW |

[^44]
## GENERAL OPERATING INFORMATION

## Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage $=0$ ).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

## Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz , and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, $\mathrm{V}_{\mathrm{S}}$. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair - or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

## Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$
A_{V S}=\frac{V_{0}}{V_{S}}=\frac{R_{L}}{R_{e}+2 r_{e}} \text { where } r_{e}=\frac{26 \mathrm{mV}}{15(\mathrm{~mA})}
$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" ( $\left.\mathrm{V}_{\mathrm{C}}=0.5 \mathrm{Vdc}\right)$. This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by $\mathrm{R}_{\mathrm{E}}$ and the bias current I5.

$$
V_{S} \leqslant 15 R_{E}(\text { Volts peak })
$$

Note that in the test circuit of Figure $10, \mathrm{~V}_{\mathrm{S}}$ corresponds to a maximum value of 1.0 V peak.

## Common Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

## Power Dissipation

Power dissipation, $\mathrm{P}_{\mathrm{D}}$, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $\mathrm{V} 12=\mathrm{V} 6, \mathrm{I} 5=\mathrm{I} 6=\mathrm{I} 12$ and ignoring base current, $\left.\mathrm{P}_{\mathrm{D}}=2 \mathrm{I} 5(\mathrm{~V} 6-\mathrm{V} 14)+\mathrm{I} 5\right) \mathrm{V} 5-\mathrm{V} 14$ where subscripts refer to pin numbers.

## Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

## A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

$$
\begin{aligned}
& \mathrm{I} 5=\mathrm{I} 6=\mathrm{I} 12, \\
& \mathrm{I}_{\mathrm{B}} \ll \mathrm{I}_{\mathrm{C}} \text { for all transistors }
\end{aligned}
$$

then :

$$
R 5=\frac{V--\phi}{I 5}-500 \Omega \begin{aligned}
& \text { where: } \begin{array}{l}
\text { R5 is the resistor between } \\
\text { Pin } 5 \text { and ground } \\
\phi=0.75 \text { at } T_{A}=+25^{\circ} \mathrm{C}
\end{array}
\end{aligned}
$$

The MC1496 has been characterized for the condition $\mathrm{I}_{5}=1.0 \mathrm{~mA}$ and is the generally recommended value.
B. Common-Mode Quiescent Output Voltage

$$
\mathrm{V} 6=\mathrm{V} 12=\mathrm{V}+-\mathrm{I} 5 \mathrm{R}_{\mathrm{L}}
$$

## Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$
\begin{aligned}
& 30 \mathrm{Vdc} \geq[(\mathrm{V} 6, \mathrm{~V} 12)-(\mathrm{V} 8, \mathrm{~V} 10)] \geq 2 \mathrm{Vdc} \\
& 30 \mathrm{Vdc} \geq[(\mathrm{V} 8, \mathrm{~V} 10)-(\mathrm{V} 1, \mathrm{~V} 4)] \geq 2.7 \mathrm{Vdc} \\
& 30 \mathrm{Vdc} \geq[(\mathrm{V} 1, \mathrm{~V} 4)-(\mathrm{V} 5)] \geq 2.7 \mathrm{Vdc}
\end{aligned}
$$

The foregoing conditions are based on the following approximations:

$$
\mathrm{V} 6=\mathrm{V} 12, \mathrm{~V} 8=\mathrm{V} 10, \mathrm{~V} 1=\mathrm{V} 4
$$

## MC1496, MC1496B

Bias currents flowing into Pins $1,4,8$ and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

## Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$
\left.\gamma 21 \mathrm{C}=\frac{\mathrm{i}_{\mathrm{O}}(\text { each sideband })}{\mathrm{v}_{\mathrm{S}}(\text { signal })} \right\rvert\, \mathrm{V}_{\mathrm{O}}=0
$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$
\left.\gamma 21 \mathrm{~S}=\frac{\mathrm{i}_{\mathrm{O}}(\text { signal })}{\mathrm{v}_{\mathrm{S}}(\text { signal })} \right\rvert\, \mathrm{V}_{\mathrm{c}}=0.5 \mathrm{Vdc}, \mathrm{~V}_{\mathrm{O}}=0
$$

## Coupling and Bypass Capacitors

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than $5.0 \Omega$ at the carrier frequency.

## Output Signal

The output signal is taken from Pins 6 and 12 either balanced or single-ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations
in both the carrier and modulating signal inputs with a single-ended output connection.

## Negative Supply

$\mathrm{V}_{\mathrm{EE}}$ should be dc only. The insertion of an RF choke in series with $\mathrm{V}_{\mathrm{EE}}$ can enhance the stability of the internal current sources.

## Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.


An alternate method for low-frequency applications is to insert a $1.0 \mathrm{k} \Omega$ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

## TEST CIRCUITS



Figure 5. Carrier Rejection and Suppression


Figure 7. Bias and Offset Currents


NOTE: Shielding of input and output leads may be needed to properly perform these tests.
Figure 6. Input-Output Impedance


Figure 8. Transconductance Bandwidth

# MC1496, MC1496B 



Figure 9. Common Mode Gain


Figure 10. Signal Gain and Output Swing

## TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure $5, \mathrm{f}_{\mathrm{C}}=500 \mathrm{kHz}$ (sine wave),


Figure 11. Sideband Output versus Carrier Levels


Figure 12. Signal-Port Parallel-Equivalent Input Resistance versus Frequency


Figure 13. Signal-Port Parallel-Equivalent Input Capacitance versus Frequency


Figure 14. Single-Ended Output Impedance versus Frequency

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TYPICAL CHARACTERISTICS (continued)
Typical characteristics were obtained with circuit shown in Figure $5, \mathrm{f}_{\mathrm{C}}=500 \mathrm{kHz}$ (sine wave), $\mathrm{V}_{\mathrm{C}}=60 \mathrm{mVrms}, \mathrm{f}_{\mathrm{S}}=1.0 \mathrm{kHz}, \mathrm{V}_{\mathrm{S}}=300 \mathrm{mVrms}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.


Figure 15. Sideband and Signal Port Transadmittances versus Frequency


Figure 17. Signal-Port Frequency Response


Figure 16. Carrier Suppression versus Temperature


Figure 18. Carrier Suppression versus Frequency


Figure 19. Carrier Feedthrough versus Frequency


Figure 20. Sideband Harmonic Suppression versus Input Signal Level


Figure 21. Suppression of Carrier Harmonic Sidebands versus Carrier Frequency


Figure 22. Carrier Suppression versus Carrier Input Level

## OPERATIONS INFORMATION

The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

## Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency
components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$
\mathrm{V}=(\mathrm{I} 5)\left(\mathrm{R}_{\mathrm{E}}\right) \text { volts peak. }
$$

This expression may be used to compute the minimum value of $\mathrm{R}_{\mathrm{E}}$ for a given input voltage amplitude.


Figure 24. Typical Modulator Circuit

| Carrier Input Signal ( $\mathrm{V}_{\mathrm{C}}$ ) | Approximate Voltage Gain | Output Signal Frequency(s) |
| :---: | :---: | :---: |
| Low-level dc | $\frac{R_{L} V_{C}}{2\left(R_{E}+2 r_{e}\right)\left(\frac{K T}{q}\right)}$ | $f_{M}$ |
| High-level dc | $\frac{R_{L}}{R_{E}+2 r_{e}}$ | $f_{M}$ |
| Low-level ac | $\frac{R_{L} V_{C}(r m s)}{2 \sqrt{2}\left(\frac{K T}{q}\right)\left(R_{E}+2 r_{e}\right)}$ | $f_{C} \pm f_{M}$ |
| High-level ac | $\frac{0.637 R_{L}}{R_{E}+2 r_{e}}$ | $f_{C} \pm f_{M}, 3 f_{C} \pm f_{M}, 5 f_{C} \pm f_{M}, \ldots$ |

2. Low-level Modulating Signal, $\mathrm{V}_{\mathrm{M}}$, assumed in all cases. $\mathrm{V}_{\mathrm{C}}$ is Carrier Input Voltage.
3. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude ofeach of the two desired outputs, $f_{C}+f_{M}$ and $f_{C}-f_{M}$.
4. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
5. $R_{L}=$ Load resistance.
6. $\mathrm{R}_{\mathrm{E}}=$ Emitter resistance between Pins 2 and 3 .
7. $r_{e}=$ Transistor dynamic emitter resistance, at $25^{\circ} \mathrm{C}$;

$$
\mathrm{re} \approx \frac{26 \mathrm{mV}}{15(\mathrm{~mA})}
$$

8. $\mathrm{K}=$ Boltzmann's Constant, $\mathrm{T}=$ temperature in degrees Kelvin, $\mathrm{q}=$ the charge on an electron.
$\frac{K T}{q} \approx 26 \mathrm{mV}$ at room temperature
Figure 25. Voltage Gain and Output Frequencies

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Figure NO TAG, along with the frequency components contained in the output signal.

## APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

## AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.
However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

## Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz .

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the $0.1 \mu \mathrm{~F}$ capacitors on Pins 8 and 10 should be increased to $1.0 \mu \mathrm{~F}$. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.
The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level

## MC1496, MC1496B

is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

## Doubly Balanced Mixer

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms .

Figure 30 shows a mixer with a broadband input and a tuned output.

## Frequency Doubler

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

## Phase Detection and FM Detection

The MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.
An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.

## TYPICAL APPLICATIONS



Figure 26. Balanced Modulator (12 Vdc Single Supply)


Figure 28. AM Modulator Circuit

Figure 29. Product Detector (12 Vdc Single Supply)


L1 = 44 Turns AWG No. 28 Enameled Wire, Wound on Micrometals Type 44-6 Toroid Core.

Figure 30. Doubly Balanced Mixer (Broadband Inputs, 9.0 MHz Tuned Output)


Figure 31. Low-Frequency Doubler


Figure 32. 150 to $\mathbf{3 0 0} \mathbf{~ M H z}$ Doubler


## MC1496，MC1496B

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC1496D | SO－14 | 55 Units／Rail |
| MC1496DR2 | SO－14 | 2500 Tape \＆Reel |
| MC1496P | PDIP－14 | 25 Units／Rail |
| MC1496P1 | PDIP－14 | 25 Units／Rail |
| MC1496BD | SO－14 | 55 Units／Rail |
| MC1496BDR2 | SO－14 | 2500 Tape \＆Reel |
| MC1496BP | PDIP－14 | 25 Units／Rail |

## MARKING DIAGRAMS

| SO－14 | PDIP－14 |
| :---: | :---: |
| D SUFFIX | P SUFFIX |
| CASE 751A | CASE 646 |


| 14 | $14$ |  | 14 ） |
| :---: | :---: | :---: | :---: |
| M－MC1496D |  | 囚 | 囚 |
| AWLYWW | AWLYWW | O AWLYYWW | O AWLYYWW |
|  | 园 |  |  |
| 1 | 1 | 1 | 1 |

> A $=$ Assembly Location
> WL $=$ Wafer Lot
> YY, Y $=$ Year
> WW $=$ Work Week

## Brushless DC Motor Controller

The MC33033 is a high performance second generation, limited feature, monolithic brushless dc motor controller which has evolved from ON Semiconductor's full featured MC33034 and MC33035 controllers. It contains all of the active functions required for the implementation of open loop, three or four phase motor control. The device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs. Unlike its predecessors, it does not feature separate drive circuit supply and ground pins, brake input, or fault output signal.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open loop speed, forward or reverse direction, and run enable. The MC33033 is designed to operate brushless motors with electrical sensor phasings of $60^{\circ} / 300^{\circ}$ or $120^{\circ} / 240^{\circ}$, and can also efficiently control brush dc motors.

- 10 to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed Loop Servo Applications
- High Current Drivers Can Control External 3-Phase MOSFET Bridge
- Cycle-By-Cycle Current Limiting
- Internal Thermal Shutdown
- Selectable $60^{\circ} / 300^{\circ}$ or $120^{\circ} / 240^{\circ}$ Sensor Phasings
- Also Efficiently Control Brush DC Motors with External MOSFET H-Bridge


## MC33033

## BRUSHLESS DC MOTOR CONTROLLER

## SEMICONDUCTOR TECHNICAL DATA



PIN CONNECTIONS


ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :--- | :---: | :---: |
| MC33033DW | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-20L |
| MC33033P |  | Plastic DIP |

## MC33033

Representative Schematic Diagram


This device contains 266 active transistors.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 30 | V |
| Digital Inputs (Pins 3, 4, 5, 6, 18, 19) | - | $\mathrm{V}_{\text {ref }}$ | V |
| Oscillator Input Current (Source or Sink) | losc | 30 | mA |
| Error Amp Input Voltage Range (Pins 9, 10, Note 1) | $\mathrm{V}_{\mathrm{IR}}$ | -0.3 to $\mathrm{V}_{\text {ref }}$ | V |
| Error Amp Output Current (Source or Sink, Note 2) | lout | 10 | mA |
| Current Sense Input Voltage Range | $V_{\text {Sense }}$ | -0.3 to 5.0 | V |
| Top Drive Voltage (Pins 1, 2, 20) | $\mathrm{V}_{\text {CE(top) }}$ | 40 | V |
| Top Drive Sink Current (Pins 1, 2, 20) | $\mathrm{I}_{\text {Sink(top) }}$ | 50 | mA |
| Bottom Drive Output Current (Source or Sink, Pins 15,16, 17) | IDRV | 100 | mA |
| Power Dissipation and Thermal Characteristics P Suffix, Dual-In-Line, Case 738 <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air <br> DW Suffix, Surface Mount, Case 751D Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\theta \mathrm{JA}}$ | $\begin{gathered} 867 \\ 75 \\ 619 \\ 105 \end{gathered}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\text {A }}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=4.7 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=10 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| REFERENCE SECTION |  |  |  |  |  |
| $\begin{aligned} & \text { Reference Output Voltage ( } I_{\text {ref }}=1.0 \mathrm{~mA} \text { ) } \\ & \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \text { to }+85^{\circ} \mathrm{C} \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{gathered} 5.9 \\ 5.82 \end{gathered}$ | $6.24$ | $\begin{gathered} 6.5 \\ 6.57 \end{gathered}$ | V |
| Line Regulation ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to $30 \mathrm{~V}, \mathrm{I}_{\text {ref }}=1.0 \mathrm{~mA}$ ) | Regline | - | 1.5 | 30 | mV |
| Load Regulation ( $\mathrm{I}_{\text {ref }}=1.0 \mathrm{~mA}$ to 20 mA ) | Regioad | - | 16 | 30 | mV |
| Output Short-Circuit Current (Note 3) | $\mathrm{I}_{\text {SC }}$ | 40 | 75 | - | mA |
| Reference Under Voltage Lockout Threshold | $\mathrm{V}_{\text {th }}$ | 4.0 | 4.5 | 5.0 | V |

## ERROR AMPLIFIER

| Input Offset Voltage ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ ) | $\mathrm{V}_{10}$ | - | 0.4 | 10 | mV |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Current ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ ) | 10 | - | 8.0 | 500 | nA |
| Input Bias Current ( $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ ) | $\mathrm{I}_{\mathrm{B}}$ | - | -46 | -1000 | nA |
| Input Common Mode Voltage Range | $V_{\text {ICR }}$ | ( 0 V to $\mathrm{V}_{\text {ref }}$ ) |  |  | V |
| Open Loop Voltage Gain ( $\mathrm{V}_{\mathrm{O}}=3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=15 \mathrm{k}$ ) | $A_{\text {VOL }}$ | 70 | 80 | - | dB |
| Input Common Mode Rejection Ratio | CMRR | 55 | 86 | - | dB |
| Power Supply Rejection Ratio ( $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}$ to 30 V ) | PSRR | 65 | 105 | - | dB |
| $\begin{aligned} & \text { Output Voltage Swing } \\ & \text { High State }\left(R_{L}=15 \mathrm{k} \text { to } \mathrm{Gnd}\right) \\ & \text { Low State }\left(R_{L}=17 \mathrm{k} \text { to } \mathrm{V}_{\text {ref }}\right) \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ <br> $\mathrm{V}_{\mathrm{OL}}$ | 4.6 | $\begin{aligned} & 5.3 \\ & 0.5 \\ & \hline \end{aligned}$ | $\begin{gathered} - \\ 1.0 \end{gathered}$ | V |

NOTES: 1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V .
2. The compliance voltage must not exceed the range of -0.3 to $\mathrm{V}_{\text {ref }}$.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=4.7 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=10 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| OSCILLATOR SECTION | $\mathrm{fosc}^{\prime}$ | 22 | 25 | 28 | kHz |
| Oscillator Frequency | $\Delta \mathrm{f}_{\mathrm{OSC}} / \Delta \mathrm{V}$ | - | 0.01 | 5.0 | $\%$ |
| Frequency Change with Voltage $\left(\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}\right.$ to 30 V$)$ | $\mathrm{V}_{\mathrm{OSC}(\mathrm{P})}$ | - | 4.1 | 4.5 | V |
| Sawtooth Peak Voltage | $\mathrm{V}_{\mathrm{OSC}(\mathrm{V})}$ | 1.2 | 1.5 | - | V |
| Sawtooth Valley Voltage |  |  |  |  |  |

## LOGIC INPUTS

| Input Threshold Voltage (Pins 3, 4, 5, 6, 18, 19) <br> High State <br> Low State | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | 3.0 | $\begin{aligned} & 2.2 \\ & 1.7 \end{aligned}$ | $\overline{0.8}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Sensor Inputs (Pins 4, 5, 6) <br> High State Input Current $\left(\mathrm{V}_{\mathrm{IH}}=5.0 \mathrm{~V}\right)$ <br> Low State Input Current ( $\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}$ ) | $\begin{aligned} & I_{\mathrm{IH}} \\ & I_{\mathrm{IL}} \end{aligned}$ | $\begin{aligned} & -150 \\ & -600 \end{aligned}$ | $\begin{gathered} -70 \\ -337 \end{gathered}$ | $\begin{gathered} -20 \\ -150 \end{gathered}$ | $\mu \mathrm{A}$ |
| Forward/Reverse, $60^{\circ} / \overline{120^{\circ}}$ Select and Output Enable (Pins 3, 18, 19) <br> High State Input Current $\left(\mathrm{V}_{\mathrm{IH}}=5.0 \mathrm{~V}\right)$ <br> Low State Input Current ( $\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}$ ) | $\begin{aligned} & I_{I H} \\ & I_{I L} \end{aligned}$ | $\begin{gathered} -75 \\ -300 \end{gathered}$ | $\begin{gathered} -36 \\ -175 \end{gathered}$ | $\begin{aligned} & -10 \\ & -75 \end{aligned}$ | $\mu \mathrm{A}$ |

## CURRENT-LIMIT COMPARATOR

| Threshold Voltage | $\mathrm{V}_{\mathrm{th}}$ | 85 | 101 | 115 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Common Mode Voltage Range | $\mathrm{V}_{\mathrm{ICR}}$ | - | 3.0 | - | V |
| Input Bias Current | $\mathrm{I}_{\mathrm{IB}}$ | - | -0.9 | -5.0 | $\mu \mathrm{~A}$ |

## OUTPUTS AND POWER SECTIONS

| Top Drive Output Sink Saturation ( $\mathrm{I}_{\text {Sink }}=25 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {CE(sat) }}$ | - | 0.5 | 1.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Top Drive Output Off-State Leakage ( $\mathrm{V}_{\mathrm{CE}}=30 \mathrm{~V}$ ) | I DRV(leak) | - | 0.06 | 100 | $\mu \mathrm{A}$ |
| Top Drive Output Switching Time ( $\mathrm{C}_{\mathrm{L}}=47 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k}$ ) Rise Time Fall Time | $\begin{aligned} & t_{r} \\ & t_{f} \end{aligned}$ | - | $\begin{aligned} & 107 \\ & 26 \end{aligned}$ | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | ns |
| $\begin{aligned} & \text { Bottom Drive Output Voltage } \\ & \text { High State }\left(\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, I_{\text {source }}=50 \mathrm{~mA}\right) \\ & \text { Low State }\left(\mathrm{V}_{\mathrm{CC}}=30 \mathrm{~V}, I_{\text {sink }}=50 \mathrm{~mA}\right) \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $\left(\mathrm{V}_{\mathrm{CC}}-2.0\right)$ | $\begin{gathered} \left(\mathrm{V}_{\mathrm{CC}}-1.1\right) \\ 1.5 \\ \hline \end{gathered}$ | $\overline{2.0}$ | V |
| Bottom Drive Output Switching Time ( $\mathrm{C}_{\mathrm{L}}=1000 \mathrm{pF}$ ) Rise Time Fall Time | $\begin{aligned} & \mathrm{t}_{\mathrm{r}} \\ & \mathrm{t}_{\mathrm{f}} \end{aligned}$ | - | $\begin{aligned} & 38 \\ & 30 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | ns |
| Under Voltage Lockout Drive Output Enabled (VCC Increasing) Hysteresis | $\begin{gathered} \mathrm{V}_{\mathrm{th}(\text { on })} \\ \mathrm{V}_{\mathrm{H}} \end{gathered}$ | $\begin{aligned} & 8.2 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 8.9 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & 10 \\ & 0.3 \end{aligned}$ | V |
| Power Supply Current | $I_{\text {cc }}$ | - | 15 | 22 | mA |

## MC33033



Figure 1. Oscillator Frequency versus Timing Resistor


Figure 2. Oscillator Frequency Change versus Temperature


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 5. Error Amp Small-Signal Transient Response

$5.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 6. Error Amp Large-Signal Transient Response


Figure 7. Reference Output Voltage Change versus Output Source Current


Figure 9. Reference Output Voltage versus Temperature


Figure 11. Bottom Drive Response Time versus Current Sense Input Voltage


Figure 8. Reference Output Voltage versus Supply Voltage


Figure 10. Output Duty Cycle versus
PWM Input Voltage


Figure 12. Top Drive Output Saturation Voltage versus Sink Current


Figure 13. Top Drive Output Waveform


Figure 15. Bottom Drive Output Waveform

$50 \mathrm{~ns} / \mathrm{DIV}$
Figure 14. Bottom Drive Output Waveform


Figure 16. Bottom Drive Output Saturation Voltage versus Load Current


Figure 17. Supply Current versus Voltage

PIN FUNCTION DESCRIPTION

| Pin | Symbol |  |
| :---: | :--- | :--- |
| $1,2,20$ | $\mathrm{~B}_{\mathrm{T}}, \mathrm{A}_{\mathrm{T}}, \mathrm{C}_{\mathrm{T}}$ | These three open collector Top Drive Outputs are designed to drive the external upper <br> power switch transistors. |
| 3 | Fwd/Rev | The Forward/Reverse Input is used to change the direction of motor rotation. |
| $4,5,6$ | $\mathrm{~S}_{\mathrm{A}}, \mathrm{S}_{\mathrm{B}}, \mathrm{S}_{\mathrm{C}}$ | These three Sensor Inputs control the commutation sequence. |
| 7 | Reference Output | This output provides charging current for the oscillator timing capacitor $\mathrm{C}_{\mathrm{T}}$ and a <br> reference for the Error Amplifier. It may also serve to furnish sensor power. |
| 8 | Oscillator | The Oscillator frequency is programmed by the values selected for the timing <br> components, $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. |
| 9 | Error Amp Noninverting Input | This input is normally connected to the speed set potentiometer. |
| 10 | Error Amp Inverting Input | This input is normally connected to the Error Amp Output in open loop applications. |
| 11 | Error Amp Out/PWM Input | This pin is available for compensation in closed loop applications. |
| 12 | Current Sense Noninverting Input | A 100 mV signal, with respect to Pin 13, at this input terminates output switch <br> conduction during a given oscillator cycle. This pin normally connects to the top side <br> of the current sense resistor. |
| 13 | Gnd $^{14}$ | $\mathrm{~V}_{\mathrm{CC}}$ |
| This pin supplies a separate ground return for the control circuit and should be <br> referenced back to the power source ground. |  |  |
| $15,16,17$ | $\mathrm{C}_{\mathrm{B}}, \mathrm{B}_{\mathrm{B}}, \mathrm{A}_{\mathrm{B}}$ | This pin is the positive supply of the control IC. The controller is functional over a $\mathrm{V}_{\mathrm{CC}}$ <br> range of 10 to 30 V. |
| 18 | $60^{\circ} / 120^{\circ}$ Select | These three totem pole Bottom Drive Outputs are designed for direct drive of the <br> external bottom power switch transistors. |
| 19 | The electrical state of this pin configures the control circuit operation for either $60^{\circ}$ <br> (high state) or $120^{\circ}$ (low state) sensor electrical phasing inputs. |  |
|  | A logic high at this input causes the motor to run, while a low causes it to coast. |  |

## INTRODUCTION

The MC33033 is one of a series of high performance monolithic dc brushless motor controllers produced by ON Semiconductor. It contains all of the functions required to implement a limited-feature, open loop, three or four phase motor control system. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33033 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open loop speed control, forward or reverse rotation, and run enable. In addition, the MC33033 has a $60^{\circ} / \overline{120^{\circ}}$ select pin which configures the rotor position decoder for either $60^{\circ}$ or $120^{\circ}$ sensor electrical phasing inputs.

## FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 18, with various applications shown in Figures 34, $36,37,41,43$, and 44 . A discussion of the features and function of each of the internal blocks given below and referenced to Figures 18 and 36.

## Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins $4,5,6$ ) to provide the proper sequencing of the top and bottom drive outputs. The Sensor Inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 V . The MC33033 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A $60^{\circ} / 120^{\circ}$ Select (Pin 18) is conveniently provided which affords the MC33033 to configure itself to control motors having either $60^{\circ}, 120^{\circ}, 240^{\circ}$ or $300^{\circ}$ electrical sensor phasing. With three Sensor Inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The Forward/Reverse input ( $\operatorname{Pin} 3$ ) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged ( $A_{T}$ to $A_{B}, B_{T}$ to $B_{B}, C_{T}$ to $C_{B}$ ). In effect the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the Output Enable (Pin19). When left disconnected, an internal pull-up resistor to a positive source enables sequencing of the top and bottom drive outputs. When grounded, the Top Drive Outputs turn off and the bottom drives are forced low, causing the motor to coast.
The commutation logic truth table is shown in Figure 19. In half wave motor drive applications, the Top Drive Outputs are not required and are typically left disconnected.

## Error Amplifier

A high performance, fully compensated Error Amplifier with access to both inputs and output (Pins 9, 10, 11) is provided to facilitate the implementation of closed loop motor speed control. The amplifier features a typical dc voltage gain of $80 \mathrm{~dB}, 0.6 \mathrm{MHz}$ gain bandwidth, and a wide input common mode voltage range that extends from ground to $\mathrm{V}_{\text {ref. }}$. In most open loop speed control applications, the amplifier is configured as a unity gain voltage follower with the Noninverting Input connected to the speed set voltage source. Additional configurations are shown in Figures 29 through 33.

## Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged from the Reference Output (Pin 7) through resistor $\mathrm{R}_{\mathrm{T}}$ and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 to 30 kHz is recommended. Refer to Figure 1 for component selection.

## Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As $\mathrm{C}_{\mathrm{T}}$ discharges, the oscillator sets both latches, allowing conduction of the Top and Bottom Drive Outputs. The PWM comparator resets the upper latch, terminating the Bottom Drive Output conduction when the positive-going ramp of $\mathrm{C}_{\mathrm{T}}$ becomes greater than the Error Amplifier output. The pulse width modulator timing diagram is shown in Figure 20. Pulse width modulation for speed control appears only at the Bottom Drive Outputs.


Figure 18. Representative Block Diagram

| Inputs (Note 2) |  |  |  |  |  |  |  |  | Outputs (Note 3) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sensor Electrical Phasing (Note 4) |  |  |  |  |  | F/R | Enable | Current <br> Sense | Top Drives |  |  | Bottom Drives |  |  |  |
| $\mathrm{S}_{\mathrm{A}}$ | $\begin{aligned} & 60^{\circ} \\ & \mathrm{S}_{\mathrm{B}} \end{aligned}$ | $\mathrm{S}_{\mathrm{c}}$ | $\mathrm{S}_{\text {A }}$ | $\begin{gathered} 120^{\circ} \\ \mathrm{S}_{\mathrm{B}} \end{gathered}$ | $\mathrm{S}_{\mathrm{c}}$ |  |  |  | $\mathrm{A}_{\mathbf{T}}$ | $\mathrm{B}_{\text {T }}$ | $\mathrm{C}_{\text {T }}$ | $A_{B}$ | $\mathrm{B}_{\mathrm{B}}$ | $\mathrm{C}_{\mathrm{B}}$ |  |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | (Note 5) |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | $\mathrm{F} / \mathrm{R}=1$ |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |  |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |  |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |  |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | (Note 5) |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | F/R = 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |  |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |  |
| 1 | 0 | 1 | 1 | 1 | 1 | X | X | X | 1 | 1 | 1 | 0 | 0 | 0 | (Note 6) |
| 0 | 1 | 0 | 0 | 0 | 0 | X | X | X | 1 | 1 | 1 | 0 | 0 | 0 |  |
| V | V | V | V | V | V | X | 0 | X | 1 | 1 | 1 | 0 | 0 | 0 | (Note 7) |
| V | V | V | V | V | V | X | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | (Note 8) |

NOTES: 1. $V=$ Any one of six valid sensor or drive combinations.
$X=$ Don't care.
2. The digital inputs (Pins $3,4,5,6,18,19$ ) are all TTL compatible. The current sense input (Pin 12) has a 100 mV threshold with respect to Pin 13. A logic 0 for this input is defined as $<85 \mathrm{mV}$, and a logic 1 is $>115 \mathrm{mV}$.
3. The top drive outputs are open collector design and active in the low ( 0 ) state.
4. With $60^{\circ} / 120^{\circ}$ (Pin 18) in the high (1) state, configuration is for $60^{\circ}$ sensor electrical phasing inputs. With Pin 18 in the low (0) state, configuration is for $120^{\circ}$ sensor electrical phasing inputs.
5. Valid $60^{\circ}$ or $120^{\circ}$ sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs; All top and bottom drives are off.
7. Valid sensor inputs with enable $=0$; All top and bottom drives are off.
8. Valid sensor inputs with enable and current sense $=1$; All top and bottom drives are off.

Figure 19. Three Phase, Six Step Commutation Truth Table (Note 1)

## Current Limit

Continuous operation of a motor that is severely over-loaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate event. Cycle-by-cycle current limiting is accomplished by monitoring the stator current build-up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ (Figure 34) in series with the three bottom switch transistors $\left(\mathrm{Q}_{4}, \mathrm{Q}_{5}, \mathrm{Q}_{6}\right)$. The voltage developed across the sense resistor is monitored by the current sense input (Pin 12), and compared to the internal 100 mV reference. If the current sense threshold is exceeded, the comparator resets the lower latch and terminates output switch conduction. The value for the sense resistor is:

$$
R_{S}=\frac{0.1}{I_{\text {stator(max) }}}
$$

The dual-latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the Error Amplifier or the current limit comparator.

## Reference

The on-chip 6.25 V regulator (Pin 7) provides charging current for the oscillator timing capacitor, a reference for the Error Amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 21. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{\text {ref }}-V_{\text {BE }}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to one amp of load current can be obtained.

## Undervoltage Lockout

A dual Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient Bottom Drive Output voltage. The positive power supply to the IC $\left(\mathrm{V}_{\mathrm{CC}}\right)$ is monitored to a threshold of 8.9 V . This level ensures sufficient gate drive necessary to attain low $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ when interfacing with standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor
operation can result if the reference output voltage should fall below 4.5 V . If one or both of the comparators detects an undervoltage condition, the top drives are turned off and the


Figure 20. PWM Timing Diagram


Transistor $Q_{1}$ is a common base stage used to level shift from $V_{C C}$ to the high motor voltage, $\mathrm{V}_{\mathrm{M}}$. The collector diode is required if $\mathrm{V}_{\mathrm{CC}}$ is present while $\mathrm{V}_{\mathrm{M}}$ is low.

Figure 22. High Voltage Interface with NPN Power Transistors

Bottom Drive Outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.


The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but also more accurate. Neither circuit has current limiting.

Figure 21. Reference Output Buffers


Figure 23. High Voltage Interface with N-Channel Power MOSFETs


The addition of the RC filter will eliminate current-limit instability caused by the leading edge spike on the current waveform. Resistor $\mathrm{R}_{\mathrm{S}}$ should be a low inductance type.

Figure 24. Current Waveform Spike Suppression


Series gate resistor $R_{g}$ will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate-source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA .

Figure 25. MOSFET Drive Precautions


The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C .

Figure 26. Bipolar Transistor Drive


Figure 28. High Voltage Boost Supply


Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

Figure 27. Current Sensing Power MOSFETs


Figure 29. Differential Input Speed Controller


Resistor $R_{1}$ with capacitor $C$ sets the acceleration time constant while $R_{2}$ controls the deceleration. The values of $R_{1}$ and $R_{2}$ should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

Figure 30. Controlled Acceleration/Deceleration


The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

Figure 32. Closed Loop Speed Control

## Drive Outputs

The three Top Drive Outputs (Pins 1, 2, 20) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 V . Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 22 and 23.

The three totem pole Bottom Drive Outputs (Pins 15, 16, 17) are particularly suited for direct drive of N -Channel MOSFETs or NPN bipolar transistors (Figures 24, 25, 26, and 27). Each output is capable of sourcing and sinking up to 100 mA .

## Thermal Shutdown

Internal thermal shutdown circuity is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at $170^{\circ} \mathrm{C}$, the IC acts as though the regulator was disabled, in turn shutting down the IC.


The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately $10 \%$ from 0 to $90 \%$ on-time. Input codes 1010 through 1111 will produce $100 \%$ on-time or full motor speed.

Figure 31. Digital Speed Controller


This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of $R_{1}$ and $R_{2}$.

Figure 33. Closed Loop Temperature Control

## SYSTEM APPLICATIONS

## Three Phase Motor Commutation

The three phase application shown in Figure 34 is an open loop motor controller with full wave, six step drive. The upper power switch transistors are Darlington PNPs while the lower switches are N-Channel power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit error. The spike can be eliminated by adding
an RC filter in series with the Current Sense Input. Using a low inductance type resistor for $\mathrm{R}_{\mathrm{S}}$ will also aid in spike reduction. Figure 35 shows the commutation waveforms over two electrical cycles. The first cycle ( $0^{\circ}$ to $360^{\circ}$ ) depicts motor operation at full speed while the second cycle ( $360^{\circ}$
to $720^{\circ}$ ) shows a reduced speed with about $50 \%$ pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.


Figure 34. Three Phase, Six Step, Full Wave Motor Controller

Rotor Electrical Position (Degrees)


Figure 35. Three Phase, Six Step, Full Wave Commutation Waveforms

## MC33033

Figure 36 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automobile and other low voltage applications since there is only one power switch voltage drop in series with a given
stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. The stator flyback voltage is clamped by a single zener and three diodes.


Figure 36. Three Phase, Three Step, Half Wave Motor Controller

## Three Phase Closed Loop Controller

The MC33033, by itself, is capable of open loop motor speed control. For closed loop speed control, the MC33033 requires an input voltage proportional to the motor speed. Traditionally this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 37 shows an application whereby an MC33039, powered from the 6.25 V reference (Pin 7) of the MC33033, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33033 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor $R_{1}$ and capacitor $C_{1}$. The resulting output train of
pulses present at Pin 5 of the MC33039 are integrated by the Error Amplifier of the MC33033 configured as an integrator, to produce a dc voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 11 of the MC33033 motor controller and completes or closes the feedback loop. The MC33033 outputs drive a TMOS power MOSFET 3-phase bridge. High current can be expected during conditions of start-up and when changing direction of the motor.

The system shown in Figure 37 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate $60 / 300$ degree Hall sensor electrical phasing by removing the jumper $\left(\mathrm{J}_{1}\right)$ at Pin 18 of the MC33033.


Figure 37. Closed Loop Brushless DC Motor Control With the MC33033 Using the MC33039

## Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 38. From the sensor phasing table (Figure 39), note that the order of input codes for $60^{\circ}$ phasing is the reverse of $300^{\circ}$. This means the MC33033, when the $60^{\circ} / \overline{120^{\circ}}$ select (Pin 18) and the FWD/REV (Pin 3) both in the high state (open), is configured to operate a $60^{\circ}$ sensor phasing motor in the forward direction. Under the same conditions a $300^{\circ}$ sensor phasing motor would operate equally well but in the reverse direction. One would simply have to reverse the FWD/REV switch (FWD/REV closed) in order to cause the $300^{\circ}$ motor to also operate in the same direction. The same difference exists between the $120^{\circ}$ and $240^{\circ}$ conventions.


Figure 38. Sensor Phasing Comparison

| Sensor Electrical Phasing (Degrees) |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $60^{\circ}$ |  |  | $120^{\circ}$ |  |  | $240^{\circ}$ |  |  | $300^{\circ}$ |  |  |
| $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ | $\mathrm{S}_{\mathrm{C}}$ | $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ | $\mathrm{S}_{\mathrm{C}}$ | $\mathrm{S}_{\mathrm{A}}$ | $\mathrm{S}_{B}$ | $\mathrm{S}_{\mathrm{C}}$ | $\mathrm{S}_{\mathrm{A}}$ | $\mathrm{S}_{\mathrm{B}}$ | $\mathrm{S}_{\mathrm{C}}$ |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | $17$ | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

In this data sheet, the rotor position has always been given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:
Electrical Degrees $=$ Mechanical Degrees $\left(\frac{\text { \#Rotor Poles }}{2}\right)$
An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

## Two and Four Phase Motor Commutation

The MC33033 configured for $60^{\circ}$ sensor inputs is capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 40 shows that by connecting sensor inputs $\mathrm{S}_{\mathrm{B}}$ and $\mathrm{S}_{\mathrm{C}}$ together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to $\mathrm{B}_{\mathrm{T}}, \mathrm{C}_{\mathrm{T}}, \mathrm{B}_{\mathrm{B}}$, and $\mathrm{C}_{\mathrm{B}}$. Figure 41 shows a four phase, four step, full wave motor control application. Power switch transistors $\mathrm{Q}_{1}$ through $\mathrm{Q}_{8}$ are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 42.
Figure 43 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 36, except for the deletion of speed adjust.

| MC33033 (60\% ${ }^{120}{ }^{\circ}$ Select Pin Open) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Inputs |  |  | Outputs |  |  |  |
| Sensor Electrical$\begin{array}{cc} \text { Spacing }^{*} & =90^{\circ} \\ \mathrm{S}_{\mathrm{A}} & \mathrm{~S}_{\mathrm{B}} \end{array}$ |  | F/R | Top Drives |  | Bottom Drives |  |
|  |  | $B_{\text {T }}$ | $\mathrm{C}_{\text {T }}$ | $B_{B}$ | $\mathrm{C}_{\mathrm{B}}$ |
| 1 | 0 |  | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |

*With MC33033 sensor input $S_{B}$ connected to $S_{C}$
Figure 40. Two and Four Phase, Four Step, Commutation Truth Table

Figure 39. Sensor Phasing Table


Rotor Electrical Position (Degrees)


Figure 42. Four Phase, Four Step, Full Wave Commutation Waveforms


## Brush Motor Control

Though the MC33033 was designed to control brushless dc motors, it may also be used to control dc brush-type motors. Figure 44 shows an application of the MC33033 driving a H-bridge affording minimal parts count to operate a brush-type motor. Key to the operation is the input sensor code [100] which produces a top-left $\left(\mathrm{Q}_{1}\right)$ and a bottom-right $\left(\mathrm{Q}_{3}\right)$ drive when the controller's Forward/Reverse pin is at logic [1]; top-right $\left(\mathrm{Q}_{4}\right)$, bottom-left $\left(\mathrm{Q}_{2}\right)$ drive is realized when the Forward/Reverse pin is at logic [0]. This code supports the requirements necessary for H -bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse width modulated frequency of approximately 25 kHz . Motor speed is controlled by adjusting the voltage presented to the noninverting input of the Error Amplifier establishing the PWM's slice or reference level. Cycle-by-cycle current limiting of the motor current is accomplished by sensing the voltage ( 100 mV threshold) across the $\mathrm{R}_{\mathrm{S}}$ resistor to ground of the H -bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, on the
fly, using the normal Forward/Reverse switch, and not have to completely stop before reversing.

## LAYOUT CONSIDERATIONS

Do not attempt to construct any of the motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor $\mathrm{V}_{\mathrm{M}}$. Ceramic bypass capacitors $(0.01 \mu \mathrm{~F})$ connected close to the integrated circuit at $\mathrm{V}_{\mathrm{CC}}$, $\mathrm{V}_{\text {ref }}$ and error amplifier noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.


Figure 44. H-Bridge Brush-Type Controller

## Brushless DC Motor Controller

The MC33035 is a high performance second generation monolithic brushless DC motor controller containing all of the active functions required to implement a full featured open loop, three or four phase motor control system. This device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open loop speed, forward or reverse direction, run enable, and dynamic braking. The MC33035 is designed to operate with electrical sensor phasings of $60^{\circ} / 300^{\circ}$ or $120^{\circ} / 240^{\circ}$, and can also efficiently control brush DC motors.

- 10 to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed Loop Servo Applications
- High Current Drivers Can Control External 3-Phase MOSFET Bridge
- Cycle-By-Cycle Current Limiting
- Pinned-Out Current Sense Reference
- Internal Thermal Shutdown
- Selectable $60^{\circ} / 300^{\circ}$ or $120^{\circ} / 240^{\circ}$ Sensor Phasings
- Can Efficiently Control Brush DC Motors with External MOSFET H-Bridge


## ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :--- | :---: | :---: |
| MC33035DW | $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | SO-24L |
| MC33035P |  | Plastic DIP |

## BRUSHLESS DC MOTOR CONTROLLER

## SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE CASE 724


## DW SUFFIX

PLASTIC PACKAGE CASE 751E
(SO-24L)


PIN CONNECTIONS

(Top View)

## MC33035

Representative Schematic Diagram


This device contains 285 active transistors.

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 40 | V |
| Digital Inputs (Pins 3, 4, 5, 6, 22, 23) | - | $\mathrm{V}_{\text {ref }}$ | V |
| Oscillator Input Current (Source or Sink) | losc | 30 | mA |
| Error Amp Input Voltage Range (Pins 11, 12, Note 1) | $\mathrm{V}_{\mathrm{IR}}$ | -0.3 to $\mathrm{V}_{\text {ref }}$ | V |
| Error Amp Output Current (Source or Sink, Note 2) | lout | 10 | mA |
| Current Sense Input Voltage Range (Pins 9, 15) | $\mathrm{V}_{\text {Sense }}$ | -0.3 to 5.0 | V |
| Fault Output Voltage | $\mathrm{V}_{\text {CE }} \overline{\text { (Fault) }}$ | 20 | V |
| Fault Output Sink Current | ISink( $\overline{\text { Fault }}$ ) | 20 | mA |
| Top Drive Voltage (Pins 1, 2, 24) | $\mathrm{V}_{\mathrm{CE} \text { (top) }}$ | 40 | V |
| Top Drive Sink Current (Pins 1, 2, 24) | I ${ }_{\text {Sink(top) }}$ | 50 | mA |
| Bottom Drive Supply Voltage (Pin 18) | $\mathrm{V}_{\mathrm{C}}$ | 30 | V |
| Bottom Drive Output Current (Source or Sink, Pins 19, 20, 21) | IDRV | 100 | mA |
| Power Dissipation and Thermal Characteristics P Suffix, Dual In Line, Case 724 Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air DW Suffix, Surface Mount, Case 751E Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ Thermal Resistance, Junction-to-Air | $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ <br> $P_{D}$ <br> $\mathrm{R}_{\text {өJA }}$ | $\begin{gathered} 867 \\ 75 \\ 650 \\ 100 \end{gathered}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=4.7 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=10 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted. $)$

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## REFERENCE SECTION

| Reference Output Voltage ( $\left.\mathrm{I}_{\text {ref }}=1.0 \mathrm{~mA}\right)$ <br> $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ <br> $\mathrm{T}_{\mathrm{A}}=-40^{\circ}$ to $+85^{\circ} \mathrm{C}$ | $\mathrm{V}_{\text {ref }}$ |  |  |  | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Line Regulation $\left(\mathrm{V}_{\mathrm{CC}}=10\right.$ to $\left.30 \mathrm{~V}, \mathrm{I}_{\text {ref }}=1.0 \mathrm{~mA}\right)$ |  | 5.9 <br> 5.82 | 6.24 <br> - | 6.57 |  |
| Load Regulation $\left(\mathrm{I}_{\text {ref }}=1.0\right.$ to 20 mA$)$ | Reg $_{\text {line }}$ | - | 1.5 | 30 | mV |
| Output Short Circuit Current (Note 3) | Reg $_{\text {load }}$ | - | 16 | 30 | mV |
| Reference Under Voltage Lockout Threshold | $\mathrm{I}_{\mathrm{SC}}$ | 40 | 75 | - | mA |

ERROR AMPLIFIER

| Input Offset Voltage $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{IO}}$ | - | 0.4 | 10 | mV |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Offset Current $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{IO}}$ | - | 8.0 | 500 | nA |  |  |  |
| Input Bias Current $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ | $\mathrm{I}_{\mathrm{IB}}$ | - | -46 | -1000 | nA |  |  |  |
| Input Common Mode Voltage Range | $\mathrm{V}_{\mathrm{ICR}}$ | $\left(0 \mathrm{~V}\right.$ to $\left.\mathrm{V}_{\text {ref }}\right)$ |  |  |  |  |  | V |
| Open Loop Voltage Gain $\left(\mathrm{V}_{\mathrm{O}}=3.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=15 \mathrm{k}\right)$ | $\mathrm{A}_{\mathrm{VOL}}$ | 70 | 80 | - | dB |  |  |  |
| Input Common Mode Rejection Ratio | CMRR | 55 | 86 | - | dB |  |  |  |
| Power Supply Rejection Ratio $\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{C}}=10\right.$ to 30 V$)$ | PSRR | 65 | 105 | - | dB |  |  |  |

NOTES: 1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V .
2. The compliance voltage must not exceed the range of -0.3 to $\mathrm{V}_{\text {ref }}$.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=4.7 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=10 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMPLIFIER |  |  |  |  |  |
| Output Voltage Swing <br> High State ( $\mathrm{R}_{\mathrm{L}}=15 \mathrm{k}$ to Gnd) <br> Low State ( $\mathrm{R}_{\mathrm{L}}=15 \mathrm{k}$ to $\mathrm{V}_{\text {ref }}$ ) | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $4.6$ | $\begin{aligned} & 5.3 \\ & 0.5 \end{aligned}$ | $\begin{gathered} - \\ 1.0 \end{gathered}$ | V |

OSCILLATOR SECTION

| Oscillator Frequency | fOsc | 22 | 25 | 28 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Frequency Change with Voltage $\left(\mathrm{V}_{\mathrm{CC}}=10\right.$ to 30 V$)$ | $\Delta \mathrm{f}_{\mathrm{OSC}} / \Delta \mathrm{V}$ | - | 0.01 | 5.0 | $\%$ |
| Sawtooth Peak Voltage | $\mathrm{V}_{\mathrm{OSC}(\mathrm{P})}$ | - | 4.1 | 4.5 | V |
| Sawtooth Valley Voltage | $\mathrm{V}_{\mathrm{OSC}(\mathrm{V})}$ | 1.2 | 1.5 | - | V |

LOGIC INPUTS

| Input Threshold Voltage (Pins 3, 4, 5, 6, 7, 22, 23) <br> High State <br> Low State | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | $3.0$ | $\begin{aligned} & 2.2 \\ & 1.7 \end{aligned}$ | $\overline{-}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Sensor Inputs (Pins 4, 5, 6) <br> High State Input Current $\left(\mathrm{V}_{\mathrm{IH}}=5.0 \mathrm{~V}\right)$ <br> Low State Input Current ( $\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}$ ) | $\begin{aligned} & I_{\mathrm{IH}} \\ & I_{I L} \end{aligned}$ | $\begin{aligned} & -150 \\ & -600 \end{aligned}$ | $\begin{gathered} -70 \\ -337 \end{gathered}$ | $\begin{gathered} -20 \\ -150 \end{gathered}$ | $\mu \mathrm{A}$ |
| Forward/Reverse, $60^{\circ} / \overline{120^{\circ}}$ Select (Pins 3, 22, 23) <br> High State Input Current $\left(\mathrm{V}_{\mathrm{IH}}=5.0 \mathrm{~V}\right)$ <br> Low State Input Current ( $\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}$ ) | $\begin{aligned} & I_{\mathrm{IH}} \\ & I_{\mathrm{IL}} \end{aligned}$ | $\begin{gathered} -75 \\ -300 \end{gathered}$ | $\begin{gathered} -36 \\ -175 \end{gathered}$ | $\begin{aligned} & -10 \\ & -75 \end{aligned}$ | $\mu \mathrm{A}$ |
| Output Enable <br> High State Input Current $\left(\mathrm{V}_{\mathrm{IH}}=5.0 \mathrm{~V}\right)$ <br> Low State Input Current ( $\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}$ ) | $\begin{aligned} & I_{I H} \\ & I_{I L} \end{aligned}$ | $\begin{aligned} & -60 \\ & -60 \end{aligned}$ | $\begin{aligned} & -29 \\ & -29 \end{aligned}$ | $\begin{aligned} & -10 \\ & -10 \end{aligned}$ | $\mu \mathrm{A}$ |

CURRENT-LIMIT COMPARATOR

| Threshold Voltage | $\mathrm{V}_{\mathrm{th}}$ | 85 | 101 | 115 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Input Common Mode Voltage Range | $\mathrm{V}_{\mathrm{ICR}}$ | - | 3.0 | - | V |
| Input Bias Current | $\mathrm{I}_{\mathrm{IB}}$ | - | -0.9 | -5.0 | $\mu \mathrm{~A}$ |

## OUTPUTS AND POWER SECTIONS

| Top Drive Output Sink Saturation ( $1_{\text {sink }}=25 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {CE(sat) }}$ | - | 0.5 | 1.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Top Drive Output Off-State Leakage ( $\mathrm{V}_{\mathrm{CE}}=30 \mathrm{~V}$ ) | $\mathrm{I}_{\text {DRV(leak) }}$ | - | 0.06 | 100 | $\mu \mathrm{A}$ |
| Top Drive Output Switching Time ( $C_{L}=47 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=1.0 \mathrm{k}$ ) <br> Rise Time <br> Fall Time | $\begin{aligned} & \mathrm{t}_{\mathrm{r}} \\ & \mathrm{t}_{\mathrm{f}} \end{aligned}$ | - | $\begin{gathered} 107 \\ 26 \end{gathered}$ | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | ns |
| Bottom Drive Output Voltage <br> High State $\left(\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=30 \mathrm{~V}\right.$, $\left.\mathrm{I}_{\text {source }}=50 \mathrm{~mA}\right)$ <br> Low State ( $\left.\mathrm{V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=30 \mathrm{~V}, \mathrm{I}_{\text {sink }}=50 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{OH}}$ <br> $\mathrm{V}_{\mathrm{OL}}$ | $\left(\mathrm{V}_{\mathrm{CC}}-2.0\right)$ | $\begin{gathered} \left(\mathrm{V}_{\mathrm{CC}}-1.1\right) \\ 1.5 \end{gathered}$ | $\overline{2.0}$ | V |
| Bottom Drive Output Switching Time ( $\mathrm{C}_{\mathrm{L}}=1000 \mathrm{pF}$ ) <br> Rise Time <br> Fall Time | $\begin{aligned} & \mathrm{t}_{\mathrm{r}} \\ & \mathrm{t}_{\mathrm{f}} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 38 \\ & 30 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \\ & \hline \end{aligned}$ | ns |
| Fault Output Sink Saturation ( $I_{\text {sink }}=16 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {CE(sat) }}$ | - | 225 | 500 | mV |
| Fault Output Off-State Leakage ( $\mathrm{V}_{\mathrm{CE}}=20 \mathrm{~V}$ ) | $\mathrm{I}_{\text {FLT (leak) }}$ | - | 1.0 | 100 | $\mu \mathrm{A}$ |
| Under Voltage Lockout Drive Output Enabled ( $\mathrm{V}_{\mathrm{CC}}$ or $\mathrm{V}_{\mathrm{C}}$ Increasing) Hysteresis | $\begin{gathered} \mathrm{V}_{\mathrm{th} \text { (on) }} \\ \mathrm{V}_{\mathrm{H}} \end{gathered}$ | $\begin{aligned} & 8.2 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 8.9 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & 10 \\ & 0.3 \end{aligned}$ | V |
| $\begin{aligned} & \text { Power Supply Current } \\ & \text { Pin } 17\left(\mathrm{~V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}\right) \\ & \text { Pin } 17\left(\mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=30 \mathrm{~V}\right) \\ & \text { Pin } 18\left(\mathrm{~V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{C}}=20 \mathrm{~V}\right) \\ & \text { Pin } 18\left(\mathrm{~V}_{\mathrm{CC}}=20 \mathrm{~V}, \mathrm{~V}_{\mathrm{C}}=30 \mathrm{~V}\right) \end{aligned}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{C}} \end{aligned}$ | - | $\begin{aligned} & 12 \\ & 14 \\ & 3.5 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 16 \\ & 20 \\ & 6.0 \\ & 10 \end{aligned}$ | mA |


$\mathrm{R}_{\mathrm{T}}$, TIMING RESISTOR $(\mathrm{k} \Omega)$
Figure 1. Oscillator Frequency versus Timing Resistor


Figure 2. Oscillator Frequency Change versus Temperature


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

$1.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 5. Error Amp Small-Signal Transient Response

$5.0 \mu \mathrm{~s} / \mathrm{DIV}$
Figure 6. Error Amp Large-Signal Transient Response


Figure 7. Reference Output Voltage Change versus Output Source Current


Figure 9. Reference Output Voltage versus Temperature

Figure 11. Bottom Drive Response Time versus Current Sense Input Voltage


Figure 8. Reference Output Voltage versus Supply Voltage


Figure 10. Output Duty Cycle versus PWM Input Voltage


Figure 12. Fault Output Saturation versus Sink Current


Figure 13. Top Drive Output Saturation Voltage versus Sink Current

$50 \mathrm{~ns} / \mathrm{DIV}$
Figure 15. Bottom Drive Output Waveform


Figure 17. Bottom Drive Output Saturation Voltage versus Load Current


Figure 14. Top Drive Output Waveform

$50 \mathrm{~ns} /$ DIV
Figure 16. Bottom Drive Output Waveform


Figure 18. Power and Bottom Drive Supply Current versus Supply Voltage

## PIN FUNCTION DESCRIPTION

| Pin | Symbol | Description |
| :---: | :---: | :---: |
| 1, 2, 24 | $\mathrm{B}_{\mathrm{T}}, \mathrm{A}_{\mathrm{T}}, \mathrm{C}_{T}$ | These three open collector Top Drive outputs are designed to drive the external upper power switch transistors. |
| 3 | Fwd/Rev | The Forward/Reverse Input is used to change the direction of motor rotation. |
| 4, 5, 6 | $\mathrm{S}_{\mathrm{A}}, \mathrm{S}_{\mathrm{B}}, \mathrm{S}_{\mathrm{C}}$ | These three Sensor Inputs control the commutation sequence. |
| 7 | Output Enable | A logic high at this input causes the motor to run, while a low causes it to coast. |
| 8 | Reference Output | This output provides charging current for the oscillator timing capacitor $\mathrm{C}_{\boldsymbol{T}}$ and a reference for the error amplifier. It may also serve to furnish sensor power. |
| 9 | Current Sense Noninverting Input | A 100 mV signal, with respect to Pin 15, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor. |
| 10 | Oscillator | The Oscillator frequency is programmed by the values selected for the timing components, $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. |
| 11 | Error Amp Noninverting Input | This input is normally connected to the speed set potentiometer. |
| 12 | Error Amp Inverting Input | This input is normally connected to the Error Amp Output in open loop applications. |
| 13 | Error Amp Out/PWM Input | This pin is available for compensation in closed loop applications. |
| 14 | Fault Output | This open collector output is active low during one or more of the following conditions: Invalid Sensor Input code, Enable Input at logic 0, Current Sense Input greater than 100 mV (Pin 9 with respect to Pin 15), Undervoltage Lockout activation, and Thermal Shutdown. |
| 15 | Current Sense Inverting Input | Reference pin for internal 100 mV threshold. This pin is normally connected to the bottom side of the current sense resistor. |
| 16 | Gnd | This pin supplies a ground for the control circuit and should be referenced back to the power source ground. |
| 17 | $\mathrm{V}_{\text {CC }}$ | This pin is the positive supply of the control IC. The controller is functional over a minimum $\mathrm{V}_{\mathrm{CC}}$ range of 10 to 30 V . |
| 18 | $\mathrm{V}_{\mathrm{C}}$ | The high state $\left(\mathrm{V}_{\mathrm{OH}}\right)$ of the Bottom Drive Outputs is set by the voltage applied to this pin. The controller is operational over a minimum $\mathrm{V}_{\mathrm{C}}$ range of 10 to 30 V . |
| 19, 20, 21 | $\mathrm{C}_{\mathrm{B}}, \mathrm{B}_{\mathrm{B}}, \mathrm{A}_{\mathrm{B}}$ | These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors. |
| 22 | $60 \% 120^{\circ}$ Select | The electrical state of this pin configures the control circuit operation for either $60^{\circ}$ (high state) or $120^{\circ}$ (low state) sensor electrical phasing inputs. |
| 23 | Brake | A logic low state at this input allows the motor to run, while a high state does not allow motor operation and if operating causes rapid deceleration. |

## INTRODUCTION

The MC33035 is one of a series of high performance monolithic DC brushless motor controllers produced by Motorola. It contains all of the functions required to implement a full-featured, open loop, three or four phase motor control system. In addition, the controller can be made to operate DC brush motors. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33035 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying a sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33035 are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can easily be interfaced to a microprocessor controller.

Typical motor control functions include open loop speed control, forward or reverse rotation, run enable, and dynamic braking. In addition, the MC33035 has a $60^{\circ} / \overline{120^{\circ}}$ select pin which configures the rotor position decoder for either $60^{\circ}$ or $120^{\circ}$ sensor electrical phasing inputs.

## FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 19 with various applications shown in Figures 36, 38, $39,43,45$, and 46 . A discussion of the features and function of each of the internal blocks given below is referenced to Figures 19 and 36.

## Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 V . The MC33035 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A $60^{\circ} \overline{120}^{\circ}$ Select (Pin 22) is conveniently provided and affords the MC33035 to configure itself to control motors having either $60^{\circ}, 120^{\circ}, 240^{\circ}$ or $300^{\circ}$ electrical sensor phasing. With three sensor inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The Forward/Reverse input ( $\operatorname{Pin} 3$ ) is used to change the direction of motor rotation by reversing the voltage across
the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged $\left(\mathrm{A}_{\mathrm{T}}\right.$ to $\mathrm{A}_{\mathrm{B}}, \mathrm{B}_{\mathrm{T}}$ to $\mathrm{B}_{\mathrm{B}}, \mathrm{C}_{\mathrm{T}}$ to $\left.\mathrm{C}_{\mathrm{B}}\right)$. In effect, the commutation sequence is reversed and the motor changes directional rotation.
Motor on/off control is accomplished by the Output Enable (Pin 7). When left disconnected, an internal $25 \mu \mathrm{~A}$ current source enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast and the $\overline{\text { Fault }}$ output to activate.

Dynamic motor braking allows an additional margin of safety to be designed into the final product. Braking is accomplished by placing the Brake Input (Pin 23) in a high state. This causes the top drive outputs to turn off and the bottom drives to turn on, shorting the motor-generated back EMF. The brake input has unconditional priority over all other inputs. The internal $40 \mathrm{k} \Omega$ pull-up resistor simplifies interfacing with the system safety-switch by insuring brake activation if opened or disconnected. The commutation logic truth table is shown in Figure 20. A four input NOR gate is used to monitor the brake input and the inputs to the three top drive output transistors. Its purpose is to disable braking until the top drive outputs attain a high state. This helps to prevent simultaneous conduction of the the top and bottom power switches. In half wave motor drive applications, the top drive outputs are not required and are normally left disconnected. Under these conditions braking will still be accomplished since the NOR gate senses the base voltage to the top drive output transistors.

## Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 11, 12, 13) is provided to facilitate the implementation of closed loop motor speed control. The amplifier features a typical DC voltage gain of $80 \mathrm{~dB}, 0.6 \mathrm{MHz}$ gain bandwidth, and a wide input common mode voltage range that extends from ground to $\mathrm{V}_{\text {ref }}$. In most open loop speed control applications, the amplifier is configured as a unity gain voltage follower with the noninverting input connected to the speed set voltage source. Additional configurations are shown in Figures 31 through 35.

## Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$. Capacitor $\mathrm{C}_{\mathrm{T}}$ is charged from the Reference Output (Pin 8) through resistor $\mathrm{R}_{\mathrm{T}}$ and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 to 30 kHz is recommended. Refer to Figure 1 for component selection.


Figure 19. Representative Block Diagram

| Inputs (Note 2) |  |  |  |  |  |  |  |  |  | Outputs (Note 3) |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sensor Electrical Phasing (Note 4) |  |  |  |  |  | F/R | Enable | Brake | Current Sense | Top Drives |  |  | Bottom Drives |  |  | Fault |  |
| $\mathrm{S}_{\mathrm{A}}$ | $\begin{aligned} & 60^{\circ} \\ & S_{B} \end{aligned}$ | $\mathrm{S}_{\mathrm{C}}$ | $\mathrm{S}_{\text {A }}$ | $\begin{gathered} 120^{\circ} \\ S_{B} \end{gathered}$ | $\mathrm{S}_{\mathrm{C}}$ |  |  |  |  | $A_{T}$ | $B_{T}$ | $\mathrm{C}_{\text {T }}$ | $A_{B}$ | $B_{B}$ | $\mathrm{C}_{\mathrm{B}}$ |  |  |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | (Note 5) |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | F/R $=1$ |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |  |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | (Note 5) |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | F/R = 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 1 | 1 | 1 | X | X | 0 | X | 1 | 1 | 1 | 0 | 0 | 0 | 0 | (Note 6) |
| 0 | 1 | 0 | 0 | 0 | 0 | X | X | 0 | X | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Brake $=0$ |
| 1 | 0 | 1 | 1 | 1 | 1 | X | X | 1 | X | 1 | 1 | 1 | 1 | 1 | 1 | 0 | (Note 7) |
| 0 | 1 | 0 | 0 | 0 | 0 | X | X | 1 | X | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Brake = 1 |
| V | V | V | V | V | V | X | 1 | 1 | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (Note 8) |
| V | V | V | V | V | V | X | 0 | 1 | X | 1 | 1 | 1 | 1 | 1 | 1 | 0 | (Note 9) |
| V | V | V | V | V | V | X | 0 | 0 | X | 1 | 1 | 1 | 0 | 0 | 0 | 0 | (Note 10) |
| V | V | V | V | V | V | X | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | (Note 11) |

NOTES: 1. $V=$ Any one of six valid sensor or drive combinations $\quad X=$ Don't care.
2. The digital inputs (Pins $3,4,5,6,7,22,23$ ) are all TTL compatible. The current sense input (Pin 9 ) has a 100 mV threshold with respect to Pin 15. A logic 0 for this input is defined as $<85 \mathrm{mV}$, and a logic 1 is $>115 \mathrm{mV}$.
3. The fault and top drive outputs are open collector design and active in the low (0) state.
4. With $60^{\circ} / 120^{\circ}$ select (Pin 22) in the high (1) state, configuration is for $60^{\circ}$ sensor electrical phasing inputs. With Pin 22 in low (0) state, configuration is for $120^{\circ}$ sensor electrical phasing inputs.
5. Valid $60^{\circ}$ or $120^{\circ}$ sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs with brake $=0$; All top and bottom drives off, Fault low.
7. Invalid sensor inputs with brake $=1$; All top drives off, all bottom drives on, Fault low.
8. Valid $60^{\circ}$ or $120^{\circ}$ sensor inputs with brake $=1$; All top drives off, all bottom drives on, Fault high.
9. Valid sensor inputs with brake $=1$ and enable $=0$; All top drives off, all bottom drives on, Fault low.
10. Valid sensor inputs with brake $=0$ and enable $=0$; All top and bottom drives off, Fault low.
11. All bottom drives off, Fault low.

Figure 20. Three Phase, Six Step Commutation Truth Table (Note 1)

## Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As $\mathrm{C}_{\mathrm{T}}$ discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating the bottom drive output conduction when the positive-going ramp of $\mathrm{C}_{\mathrm{T}}$ becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 21. Pulse width modulation for speed control appears only at the bottom drive outputs.

## Current Limit

Continuous operation of a motor that is severely over-loaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate event. Cycle-by-cycle current limiting is accomplished by monitoring the stator current build-up each time an output switch conducts, and upon
sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor $\mathrm{R}_{\mathrm{S}}$ (Figure 36) in series with the three bottom switch transistors $\left(\mathrm{Q}_{4}, \mathrm{Q}_{5}, \mathrm{Q}_{6}\right)$. The voltage developed across the sense resistor is monitored by the Current Sense Input (Pins 9 and 15), and compared to the internal 100 mV reference. The current sense comparator inputs have an input common mode range of approximately 3.0 V . If the 100 mV current sense threshold is exceeded, the comparator resets the lower sense latch and terminates output switch conduction. The value for the current sense resistor is:

$$
R_{S}=\frac{0.1}{I_{\text {stator(max) }}}
$$

The $\overline{\text { Fault }}$ output activates during an over current condition. The dual-latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the error amp or the current limit comparator.


Figure 21. Pulse Width Modulator Timing Diagram Reference

The on-chip 6.25 V regulator (Pin 8) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications, it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 22. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $\mathrm{V}_{\text {ref }}-\mathrm{V}_{\mathrm{BE}}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection and adequate heatsinking, up to one amp of load current can be obtained.


The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but is also more accurate over temperature. Neither circuit has current limiting.

## Undervoltage Lockout

A triple Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supplies to the IC $\left(\mathrm{V}_{\mathrm{CC}}\right)$ and the bottom drives $\left(\mathrm{V}_{\mathrm{C}}\right)$ are each monitored by separate comparators that have their thresholds at 9.1 V . This level ensures sufficient gate drive necessary to attain low $\mathrm{R}_{\mathrm{DS}(\mathrm{on})}$ when driving standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result if the reference output voltage falls below 4.5 V . A third comparator is used to detect this condition. If one or more of the comparators detects an undervoltage condition, the Fault Output is activated, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

## Fault Output

The open collector Fault Output (Pin 14) was designed to provide diagnostic information in the event of a system malfunction. It has a sink current capability of 16 mA and can directly drive a light emitting diode for visual indication. Additionally, it is easily interfaced with TTL/CMOS logic for use in a microprocessor controlled system. The Fault Output is active low when one or more of the following conditions occur:

1) Invalid Sensor Input code
2) Output Enable at logic [0]
3) Current Sense Input greater than 100 mV
4) Undervoltage Lockout, activation of one or more of the comparators
5) Thermal Shutdown, maximum junction temperature being exceeded
This unique output can also be used to distinguish between motor start-up or sustained operation in an overloaded condition. With the addition of an RC network between the Fault Output and the enable input, it is possible to create a time-delayed latched shutdown for overcurrent. The added circuitry shown in Figure 23 makes easy starting of motor systems which have high inertial loads by providing additional starting torque, while still preserving overcurrent protection. This task is accomplished by setting the current limit to a higher than nominal value for a predetermined time. During an excessively long overcurrent condition, capacitor $\mathrm{C}_{\text {DLY }}$ will charge, causing the enable input to cross its threshold to a low state. A latch is then formed by the positive feedback loop from the Fault Output to the Output Enable. Once set, by the Current Sense Input, it can only be reset by shorting CDLY or cycling the power supplies.

Figure 22. Reference Output Buffers

## Drive Outputs

The three top drive outputs (Pins 1, 2, 24) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 V . Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 24 and 25.

The three totem pole bottom drive outputs (Pins 19, 20, 21) are particularly suited for direct drive of $\mathrm{N}-$ Channel MOSFETs or NPN bipolar transistors (Figures 26, 27, 28 and 29). Each output is capable of sourcing and sinking up to 100 mA . Power for the bottom drives is supplied from $\mathrm{V}_{\mathrm{C}}$ (Pin 18). This separate supply input allows the designer added flexibility in tailoring the drive voltage, independent
of $\mathrm{V}_{\mathrm{CC}}$. A zener clamp should be connected to this input when driving power MOSFETs in systems where $\mathrm{V}_{\mathrm{CC}}$ is greater than 20 V so as to prevent rupture of the MOSFET gates.

The control circuitry ground (Pin 16) and current sense inverting input (Pin 15) must return on separate paths to the central input source ground.

## Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at $170^{\circ} \mathrm{C}$, the IC acts as though the Output Enable was grounded.


Figure 23. Timed Delayed Latched Over Current Shutdown


Transistor $Q_{1}$ is a common base stage used to level shift from $V_{C c}$ to the high motor voltage, $\mathrm{V}_{\mathrm{M}}$. The collector diode is required if $\mathrm{V}_{\mathrm{CC}}$ is present while $\mathrm{V}_{\mathrm{M}}$ is low.

Figure 24. High Voltage Interface with NPN Power Transistors


Figure 25. High Voltage Interface with N-Channel Power MOSFETs


Series gate resistor $R_{g}$ will dampen any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate-source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA .

Figure 27. MOSFET Drive Precautions


The addition of the RC filter will eliminate current-limit instability caused by the leading edge spike on the current waveform. Resistor $R_{S}$ should be a low inductance type.

Figure 26. Current Waveform Spike Suppression


The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C .

Figure 28. Bipolar Transistor Drive


Control Circuitry Ground (Pin 16) and Current Sense Inverting Input (Pin 15) must return on separate paths to the Central Input Source Ground.

Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches

Figure 29. Current Sensing Power MOSFETs


Figure 31. Differential Input Speed Controller


This circuit generates $\mathrm{V}_{\text {Boost }}$ for Figure 25.
Figure 30. High Voltage Boost Supply


Resistor $R_{1}$ with capacitor $C$ sets the acceleration time constant while $R_{2}$ controls the deceleration. The values of $R_{1}$ and $R_{2}$ should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

Figure 32. Controlled Acceleration/Deceleration


The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately $10 \%$ from 0 to $90 \%$ on-time. Input codes 1010 through 1111 will produce $100 \%$ on-time or full motor speed.


The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

Figure 34. Closed Loop Speed Control


This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$.

Figure 35. Closed Loop Temperature Control

## SYSTEM APPLICATIONS

## Three Phase Motor Commutation

The three phase application shown in Figure 36 is a full-featured open loop motor controller with full wave, six step drive. The upper power switch transistors are Darlingtons while the lower devices are power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit instability. The spike can be eliminated by adding an RC filter in series with the Current Sense Input. Using a low inductance type resistor for $\mathrm{R}_{\mathrm{S}}$ will also aid in
spike reduction. Care must be taken in the selection of the bottom power switch transistors so that the current during braking does not exceed the device rating. During braking, the peak current generated is limited only by the series resistance of the conducting bottom switch and winding.

$$
I_{\text {peak }}=\frac{V_{M}+E M F}{R_{\text {switch }}+R_{\text {winding }}}
$$

If the motor is running at maximum speed with no load, the generated back EMF can be as high as the supply voltage, and at the onset of braking, the peak current may approach twice the motor stall current. Figure 37 shows the commutation waveforms over two electrical cycles. The first cycle ( $0^{\circ}$ to $360^{\circ}$ ) depicts motor operation at full speed while the second cycle $\left(360^{\circ}\right.$ to $\left.720^{\circ}\right)$ shows a reduced speed with about $50 \%$ pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.


Figure 36. Three Phase, Six Step, Full Wave Motor Controller


Figure 37. Three Phase, Six Step, Full Wave Commutation Waveforms

Figure 38 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automotive and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. Continuous braking with the typical half wave arrangement presents a motor overheating problem since stator current is limited only by the winding resistance. This is due to the lack of upper power switch transistors, as in the full wave circuit, used to disconnect the windings from the supply voltage
$\mathrm{V}_{\mathrm{M}}$. A unique solution is to provide braking until the motor stops and then turn off the bottom drives. This can be accomplished by using the Fault Output in conjunction with the Output Enable as an over current timer. Components $R_{\text {DLY }}$ and $C_{\text {DLY }}$ are selected to give the motor sufficient time to stop before latching the Output Enable and the top drive AND gates low. When enabling the motor, the brake switch is closed and the PNP transistor (along with resistors $\mathrm{R}_{1}$ and $\mathrm{R}_{\mathrm{DLY}}$ ) are used to reset the latch by discharging $\mathrm{C}_{\text {DLY }}$. The stator flyback voltage is clamped by a single zener and three diodes.


Figure 38. Three Phase, Three Step, Half Wave Motor Controller

## Three Phase Closed Loop Controller

The MC33035, by itself, is only capable of open loop motor speed control. For closed loop motor speed control, the MC33035 requires an input voltage proportional to the motor speed. Traditionally, this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 39 shows an application whereby an MC33039, powered from the 6.25 V reference (Pin 8) of the MC33035, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33035 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor $\mathrm{R}_{1}$ and capacitor $\mathrm{C}_{1}$. The output train
of pulses at Pin 5 of the MC33039 are integrated by the error amplifier of the MC33035 configured as an integrator to produce a DC voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 13 of the MC33035 motor controller and closes the feedback loop. The MC33035 outputs drive a TMOS power MOSFET 3-phase bridge. High currents can be expected during conditions of start-up, breaking, and change of direction of the motor.

The system shown in Figure 39 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate $60 / 300$ degree Hall sensor electrical phasing by removing the jumper $\left(\mathrm{J}_{2}\right)$ at Pin 22 of the MC33035.


Figure 39. Closed Loop Brushless DC Motor Control Using The MC33035 and MC33039

## Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees; however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 40. From the sensor phasing table in Figure 41, note that the order of input codes for $60^{\circ}$ phasing is the reverse of $300^{\circ}$. This means the MC33035, when configured for $60^{\circ}$ sensor electrical phasing, will operate a motor with either $60^{\circ}$ or $300^{\circ}$ sensor electrical phasing, but resulting in opposite directions of rotation. The same is true for the part when it is configured for $120^{\circ}$ sensor electrical phasing; the motor will operate equally, but will result in opposite directions of rotation for $120^{\circ}$ for $240^{\circ}$ conventions.


Figure 40. Sensor Phasing Comparison

| Sensor Electrical Phasing (Degrees) |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $60^{\circ}$ |  |  | $120^{\circ}$ |  |  | $240^{\circ}$ |  |  | $300^{\circ}$ |  |  |
| $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ | $\mathrm{S}_{\mathrm{C}}$ | $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ | $\mathrm{S}_{\mathrm{C}}$ | $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ | $\mathrm{S}_{\mathrm{C}}$ | $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ | $\mathrm{S}_{\mathrm{C}}$ |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | $1$ | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

Figure 41. Sensor Phasing Table

In this data sheet, the rotor position is always given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$
\text { Electrical Degrees }=\text { Mechanical Degrees }\left(\frac{\# \text { Rotor Poles }}{2}\right)
$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

## Two and Four Phase Motor Commutation

The MC33035 is also capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 42 shows that by connecting sensor inputs $S_{B}$ and $S_{C}$ together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to $\mathrm{B}_{\mathrm{T}}, \mathrm{C}_{\mathrm{T}}, \mathrm{B}_{\mathrm{B}}$, and $\mathrm{C}_{\mathrm{B}}$. Figure 43 shows a four phase, four step, full wave motor control application. Power switch transistors $\mathrm{Q}_{1}$ through $\mathrm{Q}_{8}$ are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 44.
Figure 45 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 38, except for the deletion of speed control and braking.

| MC33035 ( $60^{\circ} /{ }^{120^{\circ}}$ Select Pin Open) |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Inputs |  |  | Outputs |  |  |  |
| Sensor Electrical Spacing ${ }^{*}=90^{\circ}$ |  | F/R | Top Drives |  | Bottom Drives |  |
| $\mathrm{S}_{\text {A }}$ | $\mathrm{S}_{\mathrm{B}}$ |  | $\mathrm{B}_{\mathrm{T}}$ | $\mathrm{C}_{\text {T }}$ | $B_{B}$ | $\mathrm{C}_{\mathrm{B}}$ |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |

*With MC33035 sensor input $\mathrm{S}_{\mathrm{B}}$ connected to $\mathrm{S}_{\mathrm{C}}$.
Figure 42. Two and Four Phase, Four Step, Commutation Truth Table


## MC33035

Rotor Electrical Position (Degrees)


Figure 44. Four Phase, Four Step, Full Wave Motor Controller


## Brush Motor Control

Though the MC33035 was designed to control brushless DC motors, it may also be used to control DC brush type motors. Figure 46 shows an application of the MC33035 driving a MOSFET H-bridge affording minimal parts count to operate a brush-type motor. Key to the operation is the input sensor code [100] which produces a top-left $\left(\mathrm{Q}_{1}\right)$ and a bottom-right $\left(\mathrm{Q}_{3}\right)$ drive when the controller's forward/reverse pin is at logic [1]; top-right $\left(\mathrm{Q}_{4}\right)$, bottom-left $\left(\mathrm{Q}_{2}\right)$ drive is realized when the Forward/Reverse pin is at logic [0]. This code supports the requirements necessary for H -bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse width modulated frequency of approximately 25 kHz . Motor speed is controlled by adjusting the voltage presented to the noninverting input of the error amplifier establishing the PWM's slice or reference level. Cycle-by-cycle current limiting of the motor current is accomplished by sensing the voltage ( 100 mV ) across the $\mathrm{R}_{\mathrm{S}}$ resistor to ground of the H -bridge motor current. The over current sense circuit
makes it possible to reverse the direction of the motor, using the normal forward/reverse switch, on the fly and not have to completely stop before reversing.

## LAYOUT CONSIDERATIONS

Do not attempt to construct any of the brushless motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor $\mathrm{V}_{\mathrm{M}}$. Ceramic bypass capacitors $(0.1 \mu \mathrm{~F})$ connected close to the integrated circuit at $\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{C}}, \mathrm{V}_{\text {ref }}$ and the error amp noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.


Figure 46. H-Bridge Brush-Type Controller

## Closed Loop Brushless Motor Adapter

The MC33039 is a high performance closed-loop speed control adapter specifically designed for use in brushless DC motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33035 brushless motor controller, it can be used cost effectively in many other closed-loop speed control applications.

- Digital Detection of Each Input Transition for Improved Low Speed Motor Operation
- TTL Compatible Inputs With Hysteresis
- Operation Down to 5.5 V for Direct Powering from MC33035 Reference
- Internal Shunt Regulator Allows Operation from a Non-Regulated Voltage Source
- Inverter Output for Easy Conversion between $60^{\circ} / 300^{\circ}$ and $120^{\circ} / 240^{\circ}$ Sensor Phasing Conventions



## PIN CONNECTIONS



Representative Block Diagram

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ Zener Current | $\mathrm{I}_{\mathrm{Z}\left(\mathrm{V}_{\mathrm{CC}}\right)}$ | 30 | mA |
| Logic Input Current (Pins 1, 2, 3) | $\mathrm{I}_{\mathrm{IH}}$ | 5.0 | mA |
| Output Current (Pins 4, 5), Sink or Source | $\mathrm{I}_{\mathrm{DRV}}$ | 20 | mA |
| Power Dissipation and Thermal Characteristics <br> Maximum Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction-to-Air | $\mathrm{P}_{\mathrm{D}}$ <br> $\mathrm{R}_{\theta \mathrm{JA}}$ | 650 <br> 100 | mW |
| ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |  |  |  |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to + | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=6.25 \mathrm{~V}, \mathrm{R}_{\mathrm{T}}=10 \mathrm{k}, \mathrm{C}_{\mathrm{T}}=22 \mathrm{nF}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LOGIC INPUTS |  |  |  |  |  |
| Input Threshold Voltage High State Low State Hysteresis | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \\ & \mathrm{~V}_{\mathrm{H}} \end{aligned}$ | $\frac{2.4}{-.4}$ | $\begin{aligned} & 2.1 \\ & 1.4 \\ & 0.7 \end{aligned}$ | $\begin{aligned} & \overline{1.0} \\ & 0.9 \end{aligned}$ | V |
| ```Input Current High State \(\left(\mathrm{V}_{\mathrm{IH}}=5.0 \mathrm{~V}\right)\) \(\phi_{A}\) \(\phi_{B}, \phi_{C}\) Low State \(\left(\mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}\right)\) \(\phi_{A}\) \(\phi_{\mathrm{B}}, \phi_{\mathrm{C}}\)``` | $\begin{aligned} & \mathrm{I}_{\mathrm{H}} \\ & \mathrm{I}_{\mathrm{IL}} \end{aligned}$ | $\begin{gathered} -40 \\ - \\ -190 \end{gathered}$ | $\begin{array}{r} -60 \\ -0.3 \\ -300 \\ -0.3 \end{array}$ | $\begin{aligned} & -80 \\ & -5.0 \\ & -380 \\ & -5.0 \end{aligned}$ | $\mu \mathrm{A}$ |

MONOSTABLE AND OUTPUT SECTIONS

| ```Output Voltage High State \(\mathrm{f}_{\text {out }}\left(\mathrm{I}_{\text {source }}=5.0 \mathrm{~mA}\right)\) \(\phi_{\mathrm{A}}^{\overline{-}}\left(\mathrm{I}_{\text {source }}=2.0 \mathrm{~mA}\right)\) Low State \(\mathrm{f}_{\text {out }}\left(\mathrm{I}_{\text {sink }}=10 \mathrm{~mA}\right)\) \(\phi_{A}^{-}\left(l_{\text {sink }}=10 \mathrm{~mA}\right)\)``` | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $\begin{aligned} & 3.60 \\ & 4.20 \end{aligned}$ | $\begin{aligned} & 3.95 \\ & 4.75 \\ & \\ & 0.25 \\ & 0.25 \end{aligned}$ | $\begin{gathered} 4.20 \\ - \\ 0.50 \\ 0.50 \end{gathered}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Capacitor $\mathrm{C}_{T}$ Discharge Current | $\mathrm{I}_{\text {dischg }}$ | 20 | 35 | 60 | mA |
| Output Pulse Width (Pin 5) | tpw | 205 | 225 | 245 | $\mu \mathrm{s}$ |

POWER SUPPLY SECTION

| Power Supply Operating Voltage Range $\left(\mathrm{T}_{\mathrm{A}}=-40^{\circ}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{CC}}$ | 5.5 | - | $\mathrm{V}_{\mathrm{Z}}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ | 1.8 | 3.9 | 5.0 | mA |
| Zener Voltage $\left(\mathrm{I}_{\mathrm{Z}}=10 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{Z}}$ | 7.5 | 8.25 | 9.0 | V |
| Zener Dynamic Impedance $\left(\Delta \mathrm{I}_{\mathrm{Z}}=10 \mathrm{~mA}\right.$ to $\left.20 \mathrm{~mA}, \mathrm{f} \leqslant 1.0 \mathrm{kHz}\right)$ | $\left\|\mathrm{Z}_{\mathrm{ka}}\right\|$ | - | 2.0 | 5.0 | $\Omega$ |



Figure 1. Typical Three Phase, Six Step Motor Application

## OPERATING DESCRIPTION

The MC33039 provides an economical method of implementing closed-loop speed control of brushless DC motors by eliminating the need for a magnetic or optical tachometer. Shown in the timing diagram of Figure 1, the three inputs (Pins 1, 2, 3) monitor the brushless motor rotor position sensors. Each sensor signal transition is digitally detected, OR'ed at the Latch 'Set' Input, and causes $\mathrm{C}_{\mathrm{T}}$ to discharge. A corresponding output pulse is generated at $f_{\text {out }}$ (Pin 5) of a defined amplitude, and programmable width determined by the values selected for $\mathrm{R}_{\mathrm{T}}$ and $\mathrm{C}_{\mathrm{T}}$ (Pin 6). The average voltage of the output pulse train increases with motor speed. When fed through a low pass filter or integrator, a DC voltage proportional to speed is generated. Figure 2 shows the proper connections for a typical closed
loop application using the MC33035 brushless motor controller. Constant speed operation down to 100 RPM is possible with economical three phase four pole motors.

The $\phi_{\mathrm{A}}$ inverter output (Pin 4) is used in systems where the controller and motor sensor phasing conventions are not compatible. A method of converting from either convention to the other is shown in Figure 3. For a more detailed explanation of this subject, refer to the text above Figure 39 on the MC33035 data sheet.

The output pulse amplitude $\mathrm{V}_{\mathrm{OH}}$ is constant with temperature and controlled by the supply voltage on $\mathrm{V}_{\mathrm{CC}}$ (Pin 8). Operation down to 5.5 V is guaranteed over temperature. For systems without a regulated power supply, an internal 8.25 V shunt regulator is provided.


MC33039


Figure 3. $\mathrm{f}_{\text {out }}$, Pulse Width versus Timing Resistor


Figure 5. $\mathrm{f}_{\text {out }}$, Pulse Width Change versus Supply Voltage


Figure 4. $f_{\text {out }}$, Pulse Width Change versus Temperature


Figure 6. Supply Current versus Supply Voltage


Figure 7. $\mathrm{f}_{\text {out }}$, Saturation versus Load Current


Figure 8. $\mathrm{f}_{\text {out }}$, Saturation Change versus Temperature

## MC33030

## DC Servo Motor Controller/Driver

The MC33030 is a monolithic DC servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, Power $\mathrm{H}-$ Switch driver capable of 1.0 A , independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

Although this device is primarily intended for servo applications, it can be used as a switchmode motor controller.

- On-Chip Error Amp for Feedback Monitoring
- Window Detector with Deadband and Self Centering

Reference Input

- Drive/Brake Logic with Direction Memory
- 1.0 A Power H-Switch
- Programmable Over-Current Detector
- Programmable Over-Current Shutdown Delay
- Over-Voltage Shutdown


This device contains 119 active transistors.


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PIN CONNECTIONS


Pins 4, 5, 12 and 13 are electrical ground and heat sink pins for IC.

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33030DW | SO-16W | 47 Units/Rail |
| MC33030DWR2 | SO-16W | 1000 Tape \& Reel |
| MC33030P | PDIP-16 | 25 Units/Rail |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 36 | V |
| Input Voltage Range Op Amp, Comparator, Current Limit (Pins 1, 2, 3, 6, 7, 8, 9, 15) | $\mathrm{V}_{\mathrm{IR}}$ | -0.3 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Input Differential Voltage Range Op Amp, Comparator (Pins 1, 2, 3, 6, 7, 8, 9) | $\mathrm{V}_{\text {IDR }}$ | -0.3 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Delay Pin Sink Current (Pin 16) | $\mathrm{I}_{\text {DLY(sink) }}$ | 20 | mA |
| Output Source Current (Op Amp) | $I_{\text {source }}$ | 10 | mA |
| Drive Output Voltage Range (Note 1) | $\mathrm{V}_{\text {DRV }}$ | -0.3 to ( $\left.\mathrm{V}_{\mathrm{CC}}+\mathrm{V}_{\mathrm{F}}\right)$ | V |
| Drive Output Source Current (Note 2) | $\mathrm{I}_{\text {DRV(source) }}$ | 1.0 | A |
| Drive Output Sink Current (Note 2) | $\mathrm{I}_{\mathrm{DRV} \text { (sink) }}$ | 1.0 | A |
| Brake Diode Forward Current (Note 2) | $\mathrm{I}_{\mathrm{F}}$ | 1.0 | A |
| Power Dissipation and Thermal Characteristics <br> P Suffix, Dual In Line Case 648C <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> (Pins 4, 5, 12, 13) <br> DW Suffix, Dual In Line Case 751G <br> Thermal Resistance, Junction-to-Air <br> Thermal Resistance, Junction-to-Case <br> (Pins 4, 5, 12, 13) | $R_{\text {日JA }}$ $\mathrm{R}_{\text {өJC }}$ <br> $\mathrm{R}_{\text {өJA }}$ $\mathrm{R}_{\text {өJC }}$ | $\begin{aligned} & 80 \\ & 15 \\ & \\ & 94 \\ & 18 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ERROR AMP |  |  |  |  |  |
| $\begin{aligned} & \text { Input Offset Voltage }\left(-40^{\circ} \mathrm{C} \leqslant \mathrm{~T}_{\mathrm{A}} \leqslant 85^{\circ} \mathrm{C}\right) \\ & \mathrm{V}_{\text {Pin } 6}=7.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=100 \mathrm{k} \end{aligned}$ | $\mathrm{V}_{10}$ | - | 1.5 | 10 | mV |
| Input Offset Current ( $\mathrm{V}_{\text {Pin } 6}=1.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=100 \mathrm{k}$ ) | $1{ }_{10}$ | - | 0.7 | - | nA |
| Input Bias Current ( $\mathrm{V}_{\text {Pin } 6}=7.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=100 \mathrm{k}$ ) | $\mathrm{IIB}^{\text {I }}$ | - | 7.0 | - | nA |
| Input Common-Mode Voltage Range $\Delta V_{I O}=20 \mathrm{mV}, \mathrm{R}_{\mathrm{L}}=100 \mathrm{k}$ | $V_{\text {ICR }}$ | - | 0 to ( $\left.\mathrm{V}_{\mathrm{CC}}-1.2\right)$ | - | V |
| Slew Rate, Open Loop ( $\mathrm{V}_{\text {ID }}=0.5 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ ) | SR | - | 0.40 | - | V/us |
| Unity-Gain Crossover Frequency | $\mathrm{f}_{\mathrm{c}}$ | - | 550 | - | kHz |
| Unity-Gain Phase Margin | ¢m | - | 63 | - | deg. |
| Common-Mode Rejection Ratio ( $\mathrm{V}_{\text {Pin } 6}=7.0 \mathrm{~V}, \mathrm{R}_{\mathrm{L}}=100 \mathrm{k}$ ) | CMRR | 50 | 82 | - | dB |
| Power Supply Rejection Ratio $V_{C C}=9.0 \text { to } 16 \mathrm{~V}, \mathrm{~V}_{\text {Pin } 6}=7.0 \mathrm{~V}, R_{\mathrm{L}}=100 \mathrm{k}$ | PSRR | - | 89 | - | dB |
| Output Source Current ( $\mathrm{V}_{\text {Pin } 6}=12 \mathrm{~V}$ ) | $10+$ | - | 1.8 | - | mA |
| Output Sink Current ( $\mathrm{V}_{\text {Pin } 6}=1.0 \mathrm{~V}$ ) | $10-$ | - | 250 | - | $\mu \mathrm{A}$ |
| Output Voltage Swing ( $\mathrm{R}_{\mathrm{L}}=17 \mathrm{k}$ to Ground) | $\begin{aligned} & \mathrm{V}_{\mathrm{OH}} \\ & \mathrm{~V}_{\mathrm{OL}} \end{aligned}$ | $12.5$ | $\begin{aligned} & 13.1 \\ & 0.02 \end{aligned}$ | - | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |

1. The upper voltage level is clamped by the forward drop, $\mathrm{V}_{\mathrm{F}}$, of the brake diode.
2. These values are for continuous DC current. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) $\left(\mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| WINDOW DETECTOR |  |  |  |  |  |
| Input Hysteresis Voltage ( $\mathrm{V}_{1}-\mathrm{V}_{4}, \mathrm{~V}_{2}-\mathrm{V}_{3}$, Figure 18) | $\mathrm{V}_{\mathrm{H}}$ | 25 | 35 | 45 | mV |
| Input Dead Zone Range ( $\mathrm{V}_{2}-\mathrm{V}_{4}$, Figure 18) | $\mathrm{V}_{\text {IDZ }}$ | 166 | 210 | 254 | mV |
| Input OffsetVoltage ( $\left[\mathrm{V}_{2}-\mathrm{V}_{\text {Pin 2 }}\right]-\left[\mathrm{V}_{\text {Pin } 2}-\mathrm{V}_{4}\right]$ IFigure 18) | $\mathrm{V}_{10}$ | - | 25 | - | mV |
| Input Functional Common-Mode Range (Note 3) <br> Upper Threshold <br> Lower Threshold | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | - | $\begin{gathered} \left(\mathrm{V}_{\mathrm{CC}}-1.05\right) \\ 0.24 \end{gathered}$ | - | V |
| Reference Input Self Centering Voltage Pins 1 and 2 Open | $\mathrm{V}_{\text {RSC }}$ | - | $\left(1 / 2 \mathrm{~V}_{\mathrm{CC}}\right)$ | - | V |
| Window Detector Propagation Delay Comparator Input, Pin 3, to Drive Outputs $\mathrm{V}_{\mathrm{ID}}=0.5 \mathrm{~V}, \mathrm{R}_{\mathrm{L}(\mathrm{DRV})}=390 \Omega$ | $\mathrm{t}_{\mathrm{p} \text { (IN/DRV) }}$ | - | 2.0 | - | $\mu \mathrm{s}$ |

OVER-CURRENT MONITOR

| Over-Current Reference Resistor Voltage (Pin 15) | Roc | 3.9 | 4.3 | 4.7 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Delay Pin Source Current $\mathrm{V}_{\mathrm{DLY}}=0 \mathrm{~V}, \mathrm{R}_{\mathrm{OC}}=27 \mathrm{k}, \mathrm{I}_{\mathrm{DRV}}=0 \mathrm{~mA}$ | ${ }^{\text {DLY }}$ (source) | - | 5.5 | 6.9 | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Delay Pin Sink Current }\left(\mathrm{R}_{\mathrm{OC}}=27 \mathrm{k}, \mathrm{I}_{\mathrm{DRV}}=0 \mathrm{~mA}\right) \\ & \mathrm{V}_{\mathrm{DLY}}=5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{DLY}}=8.3 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{DLY}}=14 \mathrm{~V} \end{aligned}$ | $\mathrm{I}_{\text {DLY( }}$ Sink) | - | $\begin{gathered} 0.1 \\ 0.7 \\ 16.5 \end{gathered}$ |  | mA |
| Delay Pin Voltage, Low State ( $\mathrm{I}_{\mathrm{DLY}}=0 \mathrm{~mA}$ ) | $\mathrm{V}_{\text {OL(DLY }}$ | - | 0.3 | 0.4 | V |
| Over-Current Shutdown Threshold $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=14 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=8.0 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\text {th( }}(\mathrm{OC})$ | $\begin{aligned} & 6.8 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 6.0 \end{aligned}$ | $\begin{aligned} & 8.2 \\ & 6.5 \end{aligned}$ | V |
| Over-Current Shutdown Propagation Delay Delay Capacitor Input, Pin 16, to Drive Outputs, $\mathrm{V}_{\mathrm{ID}}=0.5 \mathrm{~V}$ | $\mathrm{t}_{\mathrm{p} \text { (DLY/DRV) }}$ | - | 1.8 | - | $\mu \mathrm{S}$ |

## POWER H-SWITCH

| $\begin{array}{ll} \text { Drive-Output Saturation }\left(-40^{\circ} \mathrm{C} \leqslant \mathrm{~T}_{\mathrm{A}} \leqslant+85^{\circ} \mathrm{C}\right. \text {, Note 4) } \\ \text { High-State } & \left(I_{\text {source }}=100 \mathrm{~mA}\right) \\ \text { Low-State } & \left(I_{\text {sink }}=100 \mathrm{~mA}\right) \end{array}$ | $\mathrm{V}_{\mathrm{OH}(\mathrm{DRV})}$ <br> $\mathrm{V}_{\text {OL(DRV) }}$ | $\left(\mathrm{V}_{\mathrm{Cc}}-2\right)$ | $\begin{gathered} \left(\mathrm{V}_{\mathrm{CC}}-0.85\right) \\ 0.12 \end{gathered}$ | $\overline{-}$ | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Drive-Output Voltage Switching Time ( $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ ) Rise Time Fall Time | $\begin{aligned} & t_{r} \\ & t_{f} \end{aligned}$ |  | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ |  | ns |
| Brake Diode Forward Voltage Drop ( $\mathrm{I}_{\mathrm{F}}=200 \mathrm{~mA}$, Note 4) | $\mathrm{V}_{\mathrm{F}}$ | - | 1.04 | 2.5 | V |

TOTAL DEVICE

| Standby Supply Current | $\mathrm{I}_{\mathrm{CC}}$ | - | 14 | 25 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Over-Voltage Shutdown Threshold <br> $\left(-40^{\circ} \mathrm{C} \leqslant \mathrm{T}_{\mathrm{A}} \leqslant+85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{th}(\mathrm{OV})}$ | 16.5 | 18 | 20.5 | V |
| Over-Voltage Shutdown Hysteresis (Device "off" to "on") | $\mathrm{V}_{\mathrm{H}(\mathrm{OV})}$ | 0.3 | 0.6 | 1.0 | V |
| Operating Voltage Lower Threshold <br> $\left(-40^{\circ} \mathrm{C} \leqslant \mathrm{T}_{\mathrm{A}} \leqslant+85^{\circ} \mathrm{C}\right)$ | $\mathrm{V}_{\mathrm{CC}}$ | - | 7.5 | 8.0 | V |

3. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.


Figure 1. Error Amp Input Common-Mode Voltage Range versus Temperature


Figure 3. Open Loop Voltage Gain and Phase versus Frequency


Figure 5. Window Detector Feedback-Input Thresholds versus Temperature


Figure 2. Error Amp Output Saturation versus Load Current


Figure 4. Window Detector Reference-Input Common-Mode Voltage Range versus Temperature


Figure 6. Output Driver Saturation versus Load Current


Figure 7. Brake Diode Forward Current versus Forward Voltage


Figure 9. Output Source Current-Limit versus Temperature


Figure 11. Normalized Over-Current Delay Threshold Voltage versus Temperature


Figure 8. Output Source Current-Limit versus Over-Current Reference Resistance


Figure 10. Normalized Delay Pin Source Current versus Temperature


Figure 12. Supply Current versus Supply Voltage


Figure 13. Normalized Over-Voltage Shutdown Threshold versus Temperature


Figure 14. Normalized Over-Voltage Shutdown Hysteresis versus Temperature


Figure 15. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length


Figure 16. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

## OPERATING DESCRIPTION

The MC33030 was designed to drive fractional horsepower DC motors and sense actuator position by voltage feedback. A typical servo application and representative internal block diagram are shown in Figure 17. The system operates by setting a voltage on the reference input of the Window Detector (Pin 1) which appears on (Pin 2). A DC motor then drives a position sensor, usually a potentiometer driven by a gear box, in a corrective fashion so that a voltage proportional to position is present at Pin 3. The servo motor will continue to run until the voltage at Pin 3 falls within the dead zone, which is centered about the reference voltage.

The Window Detector is composed of two comparators, A and B, each containing hysteresis. The reference input, common to both comparators, is pre-biased at $1 / 2 \mathrm{~V}_{\mathrm{CC}}$ for simple two position servo systems and can easily be overridden by an external voltage divider. The feedback voltage present at Pin 3 is connected to the center of two resistors that are driven by an equal magnitude current source and sink. This generates an offset voltage at the input of each comparator which is centered about Pin 3 that can float virtually from $\mathrm{V}_{\mathrm{CC}}$ to ground. The sum of the upper and lower offset voltages is defined as the window detector input dead zone range.

To increase system flexibility, an on-chip Error Amp is provided. It can be used to buffer and/or gain-up the actuator position voltage which has the effect of narrowing the dead zone range. A PNP differential input stage is provided so that the input common-mode voltage range will include ground. The main design goal of the error amp output stage was to be able to drive the window detector input. It typically can source 1.8 mA and sink $250 \mu \mathrm{~A}$. Special design considerations must be made if it is to be used for other applications.

The Power H-Switch provides a direct means for motor drive and braking with a maximum source, sink, and brake current of 1.0 A continuous. Maximum package power dissipation limits must be observed. Refer to Figure 15 for thermal information. For greater drive current requirements, a method for buffering that maintains all the system features is shown in Figure 30.

The Over-Current Monitor is designed to distinguish between motor start-up or locked rotor conditions that can occur when the actuator has reached its travel limit. A fraction of the Power H-Switch source current is internally fed into one of the two inverting inputs of the current comparator, while the non-inverting input is driven by a programmable current reference. This reference level is controlled by the resistance value selected for $\mathrm{R}_{\mathrm{OC}}$, and must be greater than the required motor run-current with its
mechanical load over temperature; refer to Figure 8. During an over-current condition, the comparator will turn off and allow the current source to charge the delay capacitor, $\mathrm{C}_{\text {DLY }}$. When C DLY charges to a level of 7.5 V , the set input of the over-current latch will go high, disabling the drive and brake functions of the Power H -Switch. The programmable time delay is determined by the capacitance value-selected for C CLY .


This system allows the Power H-Switch to supply motor start-up current for a predetermined amount of time. If the rotor is locked, the system will time-out and shut-down. This feature eliminates the need for servo end-of-travel or limit switches. Care must be taken so as not to select too large of a capacitance value for $C_{D L Y}$. An over-current condition for an excessively long time-out period can cause the integrated circuit to overheat and eventually fail. Again, the maximum package power dissipation limits must be observed. The over-current latch is reset upon power-up or by readjusting $\mathrm{V}_{\text {Pin } 2}$ as to cause $\mathrm{V}_{\text {Pin }} 3$ to enter or pass through the dead zone. This can be achieved by requesting the motor to reverse direction.

An Over-Voltage Monitor circuit provides protection for the integrated circuit and motor by disabling the Power H -Switch functions if $\mathrm{V}_{\mathrm{CC}}$ should exceed 18 V . Resumption of normal operation will commence when $\mathrm{V}_{\mathrm{CC}}$ falls below 17.4 V .

A timing diagram that depicts the operation of the Drive/Brake Logic section is shown in Figure 18. The waveforms grouped in [1] show a reference voltage that was preset, appearing on Pin 2, which corresponds to the desired actuator position. The true actuator position is represented by the voltage on Pin 3. The points $\mathrm{V}_{1}$ through $\mathrm{V}_{4}$ represent the input voltage thresholds of comparators A and B that cause a change in their respective output state. They are defined as follows:
$\mathrm{V}_{1}=$ Comparator B turn-off threshold
$\mathrm{V}_{2}=$ Comparator A turn-on threshold
$\mathrm{V}_{3}=$ Comparator A turn-off threshold
$\mathrm{V}_{4}=$ Comparator B turn-on threshold
$\mathrm{V}_{1}-\mathrm{V}_{4}=$ Comparator B input hysteresis voltage
$\mathrm{V}_{2}-\mathrm{V}_{3}=$ Comparator A input hysteresis voltage
$\mathrm{V}_{2}-\mathrm{V}_{4}=$ Window detector input dead zone range
$\left|\left(\mathrm{V}_{2}-\mathrm{V}_{\text {Pin2 }}\right)-\left(\mathrm{V}_{\text {Pin2 }}-\mathrm{V}_{4}\right)\right|=$ Window detector input voltage

It must be remembered that points $\mathrm{V}_{1}$ through $\mathrm{V}_{4}$ always try to follow and center about the reference voltage setting if it is within the input common-mode voltage range of Pin 3 ; Figures 4 and 5 . Initially consider that the feedback input voltage level is somewhere on the dashed line between $\mathrm{V}_{2}$ and $\mathrm{V}_{4}$ in [1]. This is within the dead zone range as defined above and the motor will be off. Now if the reference voltage is raised so that $V_{\text {Pin } 3}$ is less than $V_{4}$, comparator $B$ will turn-on [3] enabling $\bar{Q}$ Drive, causing Drive Output A to sink and B to source motor current [8]. The actuator will move in Direction $B$ until $V_{\text {Pin }} 3$ becomes greater than $V_{1}$. Comparator B will turn-off, activating the brake enable [4]
and $\bar{Q}$ Brake [6] causing Drive Output A to go high and B to go into a high impedance state. The inertia of the mechanical system will drive the motor as a generator creating a positive voltage on Pin 10 with respect to Pin 14 . The servo system can be stopped quickly, so as not to over-shoot through the dead zone range, by braking. This is accomplished by shorting the motor/generator terminals together. Brake current will flow into the diode at Drive Output B, through the internal $\mathrm{V}_{\mathrm{CC}}$ rail, and out the emitter of the sourcing transistor at Drive Output A. The end of the solid line and beginning of the dashed for $\mathrm{V}_{\operatorname{Pin} 3}$ [1] indicates the possible resting position of the actuator after braking.


Figure 17. Representative Block Diagram and Typical Servo Application

If $\mathrm{V}_{\text {Pin } 3}$ should continue to rise and become greater than $\mathrm{V}_{2}$, the actuator will have over shot the dead zone range and cause the motor to run in Direction A until $\mathrm{V}_{\text {Pin } 3}$ is equal to $\mathrm{V}_{3}$. The Drive/Brake behavior for Direction A is identical to that of B . Overshooting the dead zone range in both directions can cause the servo system to continuously hunt or oscillate. Notice that the last motor run-direction is stored in the direction latch. This information is needed to determine whether Q or $\overline{\mathrm{Q}}$ Brake is to be enabled when $\mathrm{V}_{\text {Pin }}$ 3 enters the dead zone range. The dashed lines in [8,9] indicate the resulting waveforms of an over-current condition that has exceeded the programmed time delay. Notice that both Drive Outputs go into a high impedance state until $\mathrm{V}_{\text {Pin } 2}$ is readjusted so that $\mathrm{V}_{\text {Pin } 3}$ enters or crosses through the dead zone [7, 4].

The inputs of the Error Amp and Window Detector can be susceptible to the noise created by the brushes of the DC motor and cause the servo to hunt. Therefore, each of these inputs are provided with an internal series resistor and are pinned out for an external bypass capacitor. It has been found that placing a capacitor with short leads directly across the brushes will significantly reduce noise problems. Good quality RF bypass capacitors in the range of 0.001 to $0.1 \mu \mathrm{~F}$ may be required. Many of the more economical motors will generate significant levels of RF energy over a spectrum that extends from DC to beyond 200 MHz . The capacitance value and method of noise filtering must be determined on a system by system basis.

Thus far, the operating description has been limited to servo systems in which the motor mechanically drives a potentiometer for position sensing. Figures 19, 20, 27, and 31 show examples that use light, magnetic flux, temperature, and pressure as a means to drive the feedback element. Figures 21, 22 and 23 are examples of two position, open loop servo systems. In these systems, the motor runs the actuator to each end of its travel limit where the Over-Current Monitor detects a locked rotor condition and shuts down the drive. Figures 32 and 33 show two possible methods of using the MC33030 as a switching motor controller. In each example a fixed reference voltage is applied to Pin 2. This causes $\mathrm{V}_{\text {pin }} 3$ to be less than $\mathrm{V}_{4}$ and Drive Output A, Pin 14, to be in a low state saturating the TIP42 transistor. In Figure 32, the motor drives a tachometer that generates an ac voltage proportional to RPM. This voltage is rectified, filtered, divided down by the speed set potentiometer, and applied to Pin. 8. The motor will accelerate until $\mathrm{V}_{\text {Pin } 3}$ is equal to $\mathrm{V}_{1}$ at which time Pin 14 will go to a high state and terminate the motor drive. The motor will now coast until $\mathrm{V}_{\text {Pin }} 3$ is less than $\mathrm{V}_{4}$ where upon drive is then reapplied. The system operation of Figure 31 is identical to that of 32 except the signal at Pin 3 is an amplified average of the motors drive and back EMF voltages. Both systems exhibit excellent control of RPM with variations of $\mathrm{V}_{\mathrm{CC}}$; however, Figure 32 has somewhat better torque characteristics at low RPM.


Figure 18. Timing Diagram


Figure 19. Solar Tracking Servo System


Over-current monitor (not shown) shuts down servo when end stop is reached.

Figure 21. Infrared Latched Two Position Servo System


Figure 23. 0.25 Hz Square-Wave Servo Agitator


Typical sensitivity with gain set at 3.9 k is $1.5 \mathrm{mV} /$ gauss Servo motor controls magnetic field about sensor.

Figure 20. Magnetic Sensing Servo System


Over-current monitor (not shown) shuts down servo when end stop is reached.

Figure 22. Digital Two Position Servo System


Figure 24. Second Order Low-Pass Active Filter

$f_{\text {notch }}=\frac{1}{2 \pi R C}$
For $60 \mathrm{~Hz} \mathrm{R}=53.6 \mathrm{k}, \mathrm{C}=0.05$

Figure 25. Notch Filter


In this application the servo motor drives the heat/air conditioner modulator door in a duct system.

Figure 27. Temperature Sensing Servo System


A direction change signal is required at Pins 2 or 3 to reset the over-current latch.

Figure 29. Remote Latched Shutdown


Figure 26. Differential Input Amplifier

$V_{A}-V_{B}=V_{\text {Ref }}\left(\frac{\Delta R}{4 R+2 \Delta R}\right)$
$R_{1}=R_{3}, R_{2}=R_{4}, R_{1} \gg R$
$V_{\text {Pin } 6}=\frac{R_{4}}{R_{3}}\left(V_{A}-V_{B}\right)$

Figure 28. Bridge Amplifier


This circuit maintains the brake and over-current features of the MC33030. Set ROC to 15 k for $I_{D R V(\text { max })} \approx 0.5 \mathrm{~A}$.

Figure 30. Power H-Switch Buffer


Figure 31. Adjustable Pressure Differential Regulator


Figure 32. Switching Motor Controller With Buffered Output and Tach Feedback


Figure 33. Switching Motor Controller With Buffered Output and Back EMF Sensing

## Stepper Motor Driver

The MC3479 is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver-stages for the motor coils, and an output to indicate the $\overline{\text { Phase A }}$ drive state.

- Single Supply Operation: 7.2 to 16.5 V
- $350 \mathrm{~mA} /$ Coil Drive Capability
- Clamp Diodes Provided for Back-EMF Suppression
- Selectable $\overline{\mathrm{CW}} / \mathrm{CCW}$ and $\overline{\text { Full }} /$ Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis: 400 mV Minimum
- Phase Logic Can Be Initialized to $\overline{\text { Phase A }}$
- Phase A Output Drive State Indication (Open-Collector)


Figure 1. Representative Block Diagram

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| MC3479P | $\mathrm{T}_{\mathrm{A}}=0^{\circ}$ to $+70^{\circ} \mathrm{C}$ | Plastic |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{M}}$ | +18 | Vdc |
| Clamp Diode Cathode Voltage (Pin 1) | $\mathrm{V}_{\mathrm{D}}$ | $\mathrm{V}_{\mathrm{M}}+5.0$ | Vdc |
| Driver Output Voltage | $\mathrm{V}_{\mathrm{OD}}$ | $\mathrm{V}_{\mathrm{M}}+6.0$ | Vdc |
| Drive Output Current/Coil | $\mathrm{I}_{\mathrm{OD}}$ | $\pm 500$ | mA |
| Input Voltage (Logic Controls) | $\mathrm{V}_{\text {in }}$ | -0.5 to +7.0 | Vdc |
| Bias/Set Current | $\mathrm{I}_{\mathrm{BS}}$ | -10 | mA |
| Phase A Output Voltage | $\mathrm{V}_{\mathrm{OA}}$ | +18 | Vdc |
| Phase A Sink Current | $\mathrm{I}_{\mathrm{OA}}$ | 20 | mA |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\mathrm{stg}}$ | $-65 \mathrm{to}+150$ | ${ }^{\circ} \mathrm{C}$ |

RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Supply Voltage | $\mathrm{V}_{\mathrm{M}}$ | +7.2 | +16.5 | Vdc |
| Clamp Diode Cathode Voltage | $\mathrm{V}_{\mathrm{D}}$ | $\mathrm{V}_{\mathrm{M}}$ | $\mathrm{V}_{\mathrm{M}}+4.5$ | Vdc |
| Driver Output Current (Per Coil) (Note 1) | $\mathrm{I}_{\mathrm{OD}}$ | - | 350 | mA |
| Input Voltage (Logic Controls) | $\mathrm{V}_{\mathrm{in}}$ | 0 | +5.5 | Vdc |
| Bias/Set Current (Outputs Active) | $\mathrm{I}_{\mathrm{BS}}$ | -300 | -75 | $\mu \mathrm{~A}$ |
| Phase A Output Voltage | $\mathrm{V}_{\mathrm{OA}}$ | - | $\mathrm{V}_{\mathrm{M}}$ | Vdc |
| Phase A Sink Current | $\mathrm{I}_{\mathrm{OA}}$ | 0 | 8.0 | mA |
| Operating Ambient Temperature | $\mathrm{T}_{\mathrm{A}}$ | 0 | +70 | ${ }^{\circ} \mathrm{C}$ |

NOTE: 1. See section on Power Dissipation in Application Information.
DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

| Characteristic | Pins | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| INPUT LOGIC LEVELS |  |  |  |  |  |  |
| Threshold Voltage (Low-to-High) | $\begin{aligned} & 7,8 \\ & 9,10 \end{aligned}$ | $\mathrm{V}_{\text {TLH }}$ | - | - | 2.0 | Vdc |
| Threshold Voltage (High-to-Low) |  | $\mathrm{V}_{\text {THL }}$ | 0.8 | - | - | Vdc |
| Hysteresis |  | $\mathrm{V}_{\mathrm{HYS}}$ | 0.4 | - | - | Vdc |
| $\begin{aligned} \hline \text { Current: } \begin{aligned} \left(\mathrm{V}_{1}\right. & =0.4 \mathrm{~V}) \\ \left(\mathrm{V}_{1}\right. & =5.5 \mathrm{~V}) \\ \left(\mathrm{V}_{1}\right. & =2.7 \mathrm{~V}) \end{aligned} \text { ) } \end{aligned}$ |  | IIL | -100 | - | $\begin{aligned} & - \\ & +100 \\ & +20 \end{aligned}$ | $\mu \mathrm{A}$ |

## DRIVER OUTPUT LEVELS

| Output High Voltage $\left.\begin{array}{rl} \left(\mathrm{I}_{\mathrm{BS}}=-300 \mu \mathrm{~A}\right): & \left(\mathrm{l}_{\mathrm{OD}}\right. \end{array}=-350 \mathrm{~mA}\right)$ | $\begin{gathered} 2,3, \\ 14,15 \end{gathered}$ | $\mathrm{V}_{\text {OHD }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{M}}-2.0 \\ & \mathrm{~V}_{\mathrm{M}}-1.2 \end{aligned}$ | - | - | Vdc |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output Low Voltage ( $\mathrm{I}_{\mathrm{BS}}=-300 \mu \mathrm{~A}, \mathrm{I}_{\mathrm{OD}}=350 \mathrm{~mA}$ ) |  | $\mathrm{V}_{\text {OLD }}$ | - | - | 0.8 | Vdc |
| Differential Mode Output Voltage Difference (Note 4) $\left(\mathrm{I}_{\mathrm{BS}}=-300 \mu \mathrm{~A}, \mathrm{I}_{\mathrm{OD}}=350 \mathrm{~mA}\right)$ |  | DV OD | - | - | 0.15 | Vdc |
| Common Mode Output Voltage Difference (Note 5) $\left(I_{\mathrm{BS}}=-300 \mu \mathrm{~A}, \mathrm{I}_{\mathrm{OD}}=-0.1 \mathrm{~mA}\right)$ |  | CV ${ }_{\text {OD }}$ | - | - | 0.15 | Vdc |
| $\begin{aligned} & \text { Output Leakage, } \mathrm{Hi} \text { Z State } \\ & \qquad\left(0 \leqslant \mathrm{~V}_{\mathrm{OD}} \leqslant \mathrm{~V}_{\mathrm{M}}, \mathrm{I}_{\mathrm{BS}}=-5.0 \mu \mathrm{~A}\right) \\ & \left(0 \leqslant \mathrm{~V}_{\mathrm{OD}} \leqslant \mathrm{~V}_{\mathrm{M}}, \mathrm{I}_{\mathrm{BS}}=-300 \mu \mathrm{~A}, \mathrm{~F} / \mathrm{H}=2.0 \mathrm{~V}, \mathrm{OIC}=0.8 \mathrm{~V}\right) \end{aligned}$ |  | $\begin{aligned} & \mathrm{l}_{\mathrm{OZ1}} \\ & \mathrm{l} \mathrm{loz2} \end{aligned}$ | $\begin{aligned} & -100 \\ & -100 \end{aligned}$ | - | $\begin{aligned} & +100 \\ & +100 \end{aligned}$ | $\mu \mathrm{A}$ |

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.

$$
\begin{aligned}
& \text { 3. Current into a pin is designated as positive. Current out of a pin is designated as negative. } \\
& \text { 4. } D \mathrm{~V}_{\mathrm{OD}}=\left|\mathrm{V}_{\mathrm{OD1,2}}-\mathrm{V}_{\mathrm{OD} 3,4}\right| \text { where: } \quad \mathrm{V}_{\mathrm{OD} 1,2}=\left(\mathrm{V}_{\mathrm{OHD1}}-\mathrm{V}_{\mathrm{OLD} 2}\right) \text { or }\left(\mathrm{V}_{\mathrm{OHD} 2}-\mathrm{V}_{\mathrm{OLD1}}\right) \text {, and } \mathrm{V}_{\mathrm{OD} 3,4}=\left(\mathrm{V}_{\mathrm{OHD}}-\mathrm{V}_{\mathrm{OLD4}}\right) \text { or }\left(\mathrm{V}_{\mathrm{OHD4}}-\mathrm{V}_{\mathrm{OLD}}\right) \text {. } \\
& \text { 5. } C V_{O D}=\left|\mathrm{V}_{\mathrm{OHD1}}-\mathrm{V}_{\mathrm{OHD2}}\right| \text { or }\left|\mathrm{V}_{\mathrm{OHD}}-\mathrm{V}_{\mathrm{OHD}}\right| \text {. }
\end{aligned}
$$

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

| Characteristic | Pins | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLAMP DIODES |  |  |  |  |  |  |
| Forward Voltage $\left(\mathrm{l}_{\mathrm{D}}=350 \mathrm{~mA}\right)$ | $\begin{aligned} & 1,2,3, \\ & 14,15 \end{aligned}$ | $\mathrm{V}_{\mathrm{DF}}$ | - | 2.5 | 3.0 | Vdc |
| Leakage Current (Per Diode) <br> (Pin $1=21 \mathrm{~V}$; Outputs $=0 \mathrm{~V}$; $\mathrm{I}_{\mathrm{BS}}=0 \mu \mathrm{~A}$ ) |  | IDR | - | - | 100 | $\mu \mathrm{A}$ |

PHASE A OUTPUT

| Output Low Voltage $\left(\mathrm{l}_{\mathrm{OA}}=8.0 \mathrm{~mA}\right)$ | 11 | $\mathrm{V}_{\text {OLA }}$ | - | - | 0.4 | Vdc |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Off State Leakage Current $\left(\mathrm{V}_{\mathrm{OHA}}=16.5 \mathrm{~V}\right)$ |  | $\mathrm{I}_{\text {OHA }}$ | - | - | 100 | $\mu \mathrm{A}$ |
| POWER SUPPLY |  |  |  |  |  |  |
| Power Supply Current $\begin{aligned} & \left(\mathrm{I}_{\mathrm{OD}}=0 \mu \mathrm{~A}, \mathrm{I}_{\mathrm{BS}}=-300 \mu \mathrm{~A}\right) \\ & \left(\mathrm{L} 1=\mathrm{V}_{\mathrm{OHD}}, \mathrm{~L} 2=\mathrm{V}_{\mathrm{OLD}}, \mathrm{~L} 3=\mathrm{V}_{\mathrm{OHD}}, \mathrm{~L} 4=\mathrm{V}_{\mathrm{OLD}}\right) \\ & \left(\mathrm{L1}=\mathrm{V}_{\mathrm{OHD}}, \mathrm{~L} 2=\mathrm{V}_{\mathrm{OLD}}, \mathrm{~L} 3=\mathrm{Hi} \mathrm{Z}, \mathrm{~L} 4=H i \mathrm{Z}\right) \\ & \left(\mathrm{L1}=\mathrm{V}_{\mathrm{OHD}}, \mathrm{~L} 2=\mathrm{V}_{\mathrm{OLD}}, \mathrm{~L} 3=\mathrm{V}_{\mathrm{OHD}}, \mathrm{~L} 4=\mathrm{V}_{\mathrm{OHD}}\right) \end{aligned}$ | 16 | $\begin{aligned} & \mathrm{I}_{\mathrm{MW}} \\ & \mathrm{I}_{\mathrm{MZ}} \\ & \mathrm{I}_{\mathrm{MN}} \end{aligned}$ | - | - | 70 40 75 | mA |

## BIAS/SET CURRENT

| To Set Phase A | 6 | $\mathrm{I}_{\mathrm{BS}}$ | -5.0 | - | - | $\mu \mathrm{A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |

## PACKAGE THERMAL CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Thermal Resistance, Junction-to-Ambient (No Heatsink) | $R_{\text {өJA }}$ | - | 45 | - | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

AC SWITCHING CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{M}}=12 \mathrm{~V}\right)$ (See Figures 2, 3, 4)

| Characteristic | Pins | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Clock Frequency | 7 | $\mathrm{f}_{\mathrm{CK}}$ | 0 | - | 50 | kHz |
| Clock Pulse Width (High) | 7 | $\mathrm{PW}_{\mathrm{CKH}}$ | 10 | - | - | $\mu \mathrm{s}$ |
| Clock Pulse Width (Low) | 7 | $\mathrm{PW}_{\mathrm{CKL}}$ | 10 | - | - | $\mu \mathrm{s}$ |
| Bias/Set Pulse Width | 6 | $\mathrm{PW}_{\mathrm{BS}}$ | 10 | - | - | $\mu \mathrm{s}$ |
| Setup Time (CW/CCW and F/HS) | $10-7$ <br> $9-7$ | $\mathrm{t}_{\mathrm{su}}$ | 5.0 | - | - | $\mu \mathrm{s}$ |
| Hold Time (CW/CCW and F/HS) | $10-7$ <br> $9-7$ | $\mathrm{t}_{\mathrm{h}}$ | 10 | - | - | $\mu \mathrm{s}$ |
| Propagation Delay (Clk-to-Driver Output) |  | $\mathrm{t}_{\text {PCD }}$ | - | 8.0 | - | $\mu \mathrm{s}$ |
| Propagation Delay (Bias/Set-to-Driver Output) |  | $\mathrm{t}_{\text {PBSD }}$ | - | 1.0 | - | $\mu \mathrm{s}$ |
| Propagation Delay (CIk-to-Phase A Low) | $7-11$ | $\mathrm{t}_{\text {PHLA }}$ | - | 12 | - | $\mu \mathrm{s}$ |
| Propagation Delay (Clk-to-Phase A High) | $7-11$ | $\mathrm{t}_{\text {PLHA }}$ | - | 5.0 | - | $\mu \mathrm{s}$ |

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.
3. Current into a pin is designated as positive. Current out of a pin is designated as negative.


Figure 2. AC Test Circuit


Note: $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}(10 \%$ to $90 \%)$ for input signals are $\leqslant 25 \mathrm{~ns}$.

Figure 3. Bias/Set Timing (Refer to Figure 2)

| Pin No. |  | Function | Symbol | Description |
| :---: | :---: | :---: | :---: | :---: |
| 20-Pin | 16-Pin |  |  |  |
| 20 | 16 | Power Supply | $\mathrm{V}_{\mathrm{M}}$ | Power supply pin for both the logic circuit and the motor coil current. Voltage range is +7.2 to +16.5 volts. |
| $\begin{gathered} \hline 4,5,6,7 \\ 14,15,16 \\ 17 \end{gathered}$ | $\begin{gathered} 4,5, \\ 12.13 \end{gathered}$ | Ground | Gnd | Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package. |
| 1 | 1 | Clamp Diode Voltage | $\mathrm{V}_{\mathrm{D}}$ | This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11. |
| $\begin{gathered} 2,3, \\ 18,19 \end{gathered}$ | $\begin{gathered} 2,3, \\ 14,15 \end{gathered}$ | Driver Outputs | $\begin{aligned} & \mathrm{L} 1, \mathrm{~L} 2 \\ & \mathrm{~L} 3, \mathrm{~L} 4 \end{aligned}$ | High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil. |
| 8 | 6 | Bias/Set | $\overline{\mathrm{B}} / \mathrm{S}$ | This pin is typically 0.7 volts below $\mathrm{V}_{\mathrm{M}}$. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened ( $l_{\mathrm{BS}}<5.0 \mu \mathrm{~A}$ ) the outputs assume a high impedance condition, while the internal logic presets to a Phase A condition. |
| 9 | 7 | Clock | Clk | The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open. |
| 11 | 9 | Full/Half Step | F/HS | When low (Logic "0"), each clock input pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. See Figure 7 for sequence. |
| 12 | 10 | Clockwise/ Counterclockwise | CW/CCW | This input allows reversing the rotation of the motor. See Figure 7 for sequence. |
| 10 | 8 | Output Impedance Control | OIC | This input is relevant only in the half step mode (Pin $9>2.0 \mathrm{~V}$ ). When low (Logic "0"), the two driver outputs of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to $\mathrm{V}_{\mathrm{M}}$. See Figure 7. |
| 13 | 11 | Phase A | Ph A | This open-collector output indicates (when low) that the driver outputs are in the Phase A condition ( $\mathrm{L} 1=\mathrm{L} 3=\mathrm{V}_{\mathrm{OHD}}, \mathrm{L} 2=\mathrm{L} 4=\mathrm{V}_{\mathrm{OLD}}$ ). |

## APPLICATION INFORMATION

## General

The MC3479 integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two-phase motor. The outputs change state with each low-to-high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions at the logic controls.

## Outputs

The outputs (L1-L4) are high current outputs (see Figure 5), which when connected to a two-phase motor, provide two full-bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor $\left(\mathrm{Q}_{\mathrm{H}}\right.$ or $\left.\mathrm{Q}_{\mathrm{L}}\right)$ of each output is on, which in turn depends on the inputs and the decoding circuitry.


Figure 4. Clock Timing (Refer to Figure 2)


Figure 5. Output Stages

The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on $\overline{\mathrm{Bias}} /$ Set operation). Whenever the outputs are to be in a high impedance state, both transistors $\left(\mathrm{Q}_{\mathrm{H}}\right.$ and $\mathrm{Q}_{\mathrm{L}}$ of Figure 5) of each output are off.

## $V_{D}$

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back-EMF voltage spikes. $\mathrm{V}_{\mathrm{D}}$ is normally connected to $\mathrm{V}_{\mathrm{M}}$ (Pin 16) through a diode (zener or regular), a resistor, or directly. The peaks instantaneous voltage at the outputs must not exceed $\mathrm{V}_{\mathrm{M}}$ by more than 6.0 V . The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each $\mathrm{Q}_{\mathrm{L}}$ of each output provide for a complete circuit path for the switched current.


Figure 6. Clamp Diode Characteristics

## Full/Half Step

When this input is at a Logic " 0 " ( $<0.8 \mathrm{~V}$ ), the outputs change a full step with each clock cycle, with the sequence direction depending on the $\overline{\mathrm{CW}} / \mathrm{CCW}$ input. There are four steps ( $\overline{\text { Phase } \mathrm{A}}, \overline{\mathrm{B}}, \overline{\mathrm{C}}, \overline{\mathrm{D}}$ ) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step, as shown in Figure 7.

When taken to a Logic " 1 " (>2.0 V), the outputs change a half step with each clock cycle, with the sequence direction depending on the $\overline{\mathrm{CW}} / \mathrm{CCW}$ input. Eight steps ( $\overline{\text { Phase A }}$ to $\overline{\mathrm{H}})$ result for each complete cycle of the sequencing logic. $\overline{\text { Phase } A}, \overline{\mathrm{C}}, \overline{\mathrm{E}}$ and $\overline{\mathrm{G}}$ correspond (in polarity) to $\overline{\text { Phase } \mathrm{A}}, \overline{\mathrm{B}}$, $\overline{\mathrm{C}}$, and $\overline{\mathrm{D}}$, respectively, of the full step sequence. $\overline{\text { Phase } \mathrm{B}}, \overline{\mathrm{D}}$, $\overline{\mathrm{F}}$ and $\overline{\mathrm{H}}$ provide current to one motor coil, while de-energizing the other coil. The condition of the outputs of the de-energized coil depends on the OIC input, see Figure 7 timing diagram.

## OIC

The output impedance control input determines the output impedance to the de-energized coil when operating in the half-step mode. When the outputs are in $\overline{\text { Phase } B}, \overline{\mathrm{D}}, \overline{\mathrm{F}}$ or $\overline{\mathrm{H}}$
(Figure 7) and this input is at a Logic " 0 " ( $<0.8 \mathrm{~V}$ ), the two outputs to the de-energized coil are in a high impedance condition - $\mathrm{Q}_{\mathrm{L}}$ and $\mathrm{Q}_{\mathrm{H}}$ of both outputs (Figure 5) are off. When this input is at a Logic " 1 " (>2.0 V), a low impedance output is provided to the de-energized coil as both outputs have $\mathrm{Q}_{\mathrm{H}}$ on $\left(\mathrm{Q}_{\mathrm{L}}\right.$ off $)$. To complete the low impedance path requires connecting $\mathrm{V}_{\mathrm{D}}$ to $\mathrm{V}_{\mathrm{M}}$ as described elsewhere in this data sheet.

## $\overline{B i a s} /$ Set

This pin can be used for three functions: a) determining the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.
a) The maximum output sink current is determined by the base drive current supplied to the lower transistors $\left(\mathrm{Q}_{\mathrm{LS}}\right.$ of Figure 5) of each output, which in turn, is a function of $\mathrm{I}_{\mathrm{BS}}$. The appropriate value of $\mathrm{I}_{\mathrm{BS}}$ is determined by:

$$
I_{B S}=I_{O D} \times 0.86
$$

where $\mathrm{I}_{\mathrm{BS}}$ is in microamps, and $\mathrm{I}_{\mathrm{OD}}$ is the motor current/coil in milliamps.


Figure 7. Output Sequence

The value of $R_{B}$ (between this pin and ground) is then determined by:

$$
R_{B}=\frac{V_{M}-0.7 V}{I_{B S}}
$$

b) When this pin is opened (raised to $V_{M}$ ) such that $I_{B S}$ is $<5.0 \mu \mathrm{~A}$, the internal logic is set to the Phase A condition, and the four driver outputs are put into a high impedance state. The $\overline{\text { Phase A }}$ output (Pin 11) goes active (low), and input signals at the controls are ignored during this time. Upon re-establishing $\mathrm{I}_{\mathrm{BS}}$, the driver outputs become active, and will be in the Phase $\overline{\mathrm{A}}$ position $\left(\mathrm{L} 1=\mathrm{L} 3=\mathrm{V}_{\mathrm{OHD}}, \mathrm{L} 2=\mathrm{L} 4=\mathrm{V}_{\mathrm{OLD}}\right)$. The circuit will then respond to the inputs at the controls.

The Set function (opening this pin) can be used as a power-up reset while supply voltages are settling. A CMOS logic gate (powered by $\mathrm{V}_{\mathrm{M}}$ ) can be used to control this pin as shown in Figure 11.
c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing $\mathrm{I}_{\mathrm{BS}}$, so as to reduce the output (motor) current. Setting $\mathrm{I}_{\mathrm{BS}}$ to $75 \mu \mathrm{~A}$ will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

## Power Dissipation

The power dissipated by the MC3479 must be such that the junction temperature $\left(\mathrm{T}_{\mathrm{J}}\right)$ does not exceed $150^{\circ} \mathrm{C}$. The power dissipated can be expressed as:

$$
\mathrm{P}=\left(\mathrm{V}_{\mathrm{M}} \times \mathrm{I}_{\mathrm{M}}\right)+\left(2 \times \mathrm{I}_{\mathrm{OD}}\right)\left[\left(\mathrm{V}_{\mathrm{M}}-\mathrm{V}_{\mathrm{OHD}}\right)+\mathrm{V}_{\mathrm{OLD}}\right]
$$

where $\quad V_{M}=$ Supply voltage;
$\mathrm{I}_{\mathrm{M}}=$ Supply current other than $\mathrm{I}_{\mathrm{OD}}$;
$\mathrm{I}_{\mathrm{OD}}=$ Output current to each motor coil;
$\mathrm{V}_{\mathrm{OHD}}=$ Driver output high voltage;
$\mathrm{V}_{\text {OLD }}=$ Driver output low voltage .
The power supply current $\left(\mathrm{I}_{\mathrm{M}}\right)$ is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$
T_{J}=\left(P \times R_{\theta J A}\right)+T_{A}
$$

where $\mathrm{R}_{\theta \mathrm{JA}}=$ Junction-to-ambient thermal resistance ( $52^{\circ} \mathrm{C} / \mathrm{W}$ for the DIP, $72^{\circ} \mathrm{C} / \mathrm{W}$ for the FN Package);

$$
\mathrm{T}_{\mathrm{A}}=\text { Ambient Temperature }
$$



Figure 8. Power Supply Current

For example, assume an application where $\mathrm{V}_{\mathrm{M}}=12 \mathrm{~V}$, the motor requires $200 \mathrm{~mA} /$ coil, operating at room temperature with no heatsink on the IC. $\mathrm{I}_{\mathrm{BS}}$ is calculated:

$$
\begin{aligned}
& \mathrm{I}_{\mathrm{BS}}=200 \times 0.86 \\
& \mathrm{I}_{\mathrm{BS}}=172 \mu \mathrm{~A}
\end{aligned}
$$

$\mathrm{R}_{\mathrm{B}}$ is calculated:

$$
\begin{aligned}
& \mathrm{R}_{\mathrm{B}}=(12-0.7) \mathrm{V} / 172 \mu \mathrm{~A} \\
& \mathrm{R}_{\mathrm{B}}=65.7 \mathrm{k} \Omega
\end{aligned}
$$

From Figure $8, \mathrm{I}_{\mathrm{M}}$ (max) is determined to be 40 mA . From Figure $9, \mathrm{~V}_{\mathrm{OLD}}$ is 0.46 volts, and from Figure $10,\left(\mathrm{~V}_{\mathrm{M}}-\right.$ $\left.\mathrm{V}_{\mathrm{OHD}}\right)$ is 1.4 volts.

$$
\begin{aligned}
& \mathrm{P}=(12 \times 0.040)+(2 \times 0.2)(1.4+0.46) \\
& \mathrm{P}=1.22 \mathrm{~W} \\
& \mathrm{~T}_{\mathrm{J}}=\left(1.22 \mathrm{~W} \times 52^{\circ} \mathrm{C} / \mathrm{W}\right)+25^{\circ} \mathrm{C} \\
& \mathrm{~T}_{\mathrm{J}}=88^{\circ} \mathrm{C}
\end{aligned}
$$

This temperature is well below the maximum limit. If the calculated $\mathrm{T}_{\mathrm{J}}$ had been higher than $150^{\circ} \mathrm{C}$, a heatsink such as the Staver Co. V-7 Series, Aavid \#5802, or Thermalloy \#6012 could be used to reduce $\mathrm{R}_{\theta \mathrm{JJA}}$. In extreme cases, forced air cooling should be considered.

The above calculation, and $\mathrm{R}_{\theta \mathrm{JA}}$, assumes that a ground plane is provided under the MC3479 (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase $\mathrm{T}_{\mathrm{J}}$, as well as provide potentially disruptive ground noise and $\mathrm{I}_{\mathrm{R}}$ drops when switching the motor current.


Figure 9. Maximum Saturation Voltage Driver Output Low


Figure 10. Maximum Saturation Voltage Driver Output High


Figure 11. Typical Applications Circuit


- Suggested value for $\mathrm{R}_{\mathrm{B} 1}\left(\mathrm{~V}_{\mathrm{M}}=12 \mathrm{~V}\right)$ is $150 \mathrm{k} \Omega$.
- $\mathrm{R}_{\mathrm{B}}$ calculation (see text) must take into account
the current through $\mathrm{R}_{\mathrm{B} 1}$.

Figure 12. Power Reduction

## CS8441

## Stepper Motor Driver with Divide by Select

The CS8441 is a Stepper Motor Driver that implements an H -Bridge design in order to drive two coils in an eight step sequence per revolution in the divide by 1 mode; 16 step sequence in the divide by 2 mode. The H -Bridge is capable of delivering 85 mA to the load.

The sequencer insures that the odometer is monotonic. This sequencer is configured such that simultaneous conduction does not occur. Before each successive output sequence the part is taken through a state where both outputs are turned off individually. This tends to minimize the inductive kick back energy that the part must absorb. On-chip clamp diodes are across each output to protect the part from the kick back energy that it must absorb.

Additional part protection is provided by two functions. The first being "short circuit protection." This function will protect the part in the case of a shorted or partially shorted load. The second protection function is the "overvoltage function." This function monitors the level of the supply voltage. In transient conditions such as load dump, the part will shut down, protecting itself.

## Features

- No Cross-Conduction in Either H-Bridge
- Divide by 1 and Divide by 2 Modes
- Guaranteed Monotonic
- On-Chip Flyback Diodes
- Fault Protection
- Overvoltage
- Load Dump Protection to 60 V


Figure 1. Block Diagram
ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


## PIN CONNECTIONS AND MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, $\mathrm{Y}=$ Year
WW, W = Work Week

## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS8441YN8 | DIP-8 | 50 Units/Rail |

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) (Note 1): | Continuous 100 ms Pulse Transient | $\begin{aligned} & -0.5 \text { to } 24 \\ & -0.5 \text { to } 60 \end{aligned}$ | V |
| Input Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ) |  | -0.3 to $\mathrm{V}_{\mathrm{CC}}+0.3$ | V |
| Storage Temperature Range ( $\mathrm{T}_{\text {STG }}$ ) |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature Range |  | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering: | Wave Solder: (through hole styles only) (Note 2) | 260 peak | ${ }^{\circ} \mathrm{C}$ |

1. $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
2. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}, 6.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 15.5 \mathrm{~V}\right.$; unless otherwise stated. All voltage shall be referenced to GND unless otherwise noted. Overvoltage shutdown of coils occurs when $\mathrm{V}_{\mathrm{CC}}>16 \mathrm{~V}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply, $\mathrm{V}_{\text {CC }}$ |  |  |  |  |  |
| Supply Voltage Range | $\begin{aligned} & -40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C} \\ & -40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C} \\ & \text { Transient Pulse, } 100 \mathrm{~ms} \end{aligned}$ | $\begin{aligned} & 6.5 \\ & 6.5 \end{aligned}$ | - | $\begin{aligned} & 15.5 \\ & 24 \\ & 35 \end{aligned}$ | $V_{D C}$ <br> $V_{D C}$ <br> $V_{D C}$ |
| Supply Current | $\mathrm{V}_{\mathrm{CC}}=15.5 \mathrm{~V}_{\mathrm{DC}}$, Outputs not loaded. | - | 24 | 35 | mA |
| Overvoltage Shutdown | - | 16 | - | 23 | V |

Speed Sensor Input, SENSOR

| Input Frequency Range | - | - | 0.2 | 1.0 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Switching Threshold | - | 1.2 | - | 2.4 | $\mathrm{~V}_{\mathrm{DC}}$ |
| Hysteresis | - | 300 | 500 | - | $\mathrm{m} \mathrm{V}_{\mathrm{DC}}$ |
| Input Bias Current | $0.8 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{IN}} \leq \mathrm{V}_{\mathrm{CC}}$ | - | 0.1 | $\pm 1.0$ | $\mu \mathrm{~A}$ |
| Input Voltage Range | - | 0 | - | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{DC}}$ |
| Operating Input Voltage | $10 \mathrm{k} \Omega$ Resistor in Series | - | - | -15 to $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{DC}}$ |
| Input Clamp Current | I Clamp at $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}_{\mathrm{DC}}$ | - | -0.4 | -5.0 | mA |

## Divider Select Input, SELECT

| Logic 0 Input Voltage | - | - | - | 100 | $\mathrm{mV} \mathrm{V}_{\mathrm{DC}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Logic 1 Input Voltage | - | 3.0 | - | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{DC}}$ |
| Logic 0 Input Current | $0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 100 \mathrm{mV}$ | - | -1.0 | -100 | $\mu \mathrm{~A}$ |
| Logic 1 Input Current | $3.0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 15.5 \mathrm{~V}_{\mathrm{DC}}$ | - | 0.75 | 2.0 | mA |

## Coil Output Drivers

| Coil Load | $+25^{\circ} \mathrm{C}$ | 198 | 210 | 222 | $\Omega$ |  |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Coil Inductance | - |  |  |  |  |  | - | 80 | - | mH |
| Coil Resistance Temperature | Coefficient | - | - | 0.35 | $\% /{ }^{\circ} \mathrm{C}$ |  |  |  |  |  |
| Energized Coil Voltage (Note 3) | $\mathrm{V}_{\mathrm{CC}}=6.5 \mathrm{~V}_{\mathrm{DC}}$ | $\mathrm{V}_{\mathrm{CC}}-1.5 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-0.9 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |  |  |  |  |  |
| (Both Polarities) A and B | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}_{\mathrm{DC}}$ | $\mathrm{V}_{\mathrm{CC}}-1.6 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-1.0 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |  |  |  |  |  |
|  | $\mathrm{V}_{\mathrm{CC}}=15.5 \mathrm{~V}_{\mathrm{DC}},-20^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{CC}}-1.75 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-1.1 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |  |  |  |  |  |
|  | $\mathrm{V}_{\mathrm{CC}}=15.5 \mathrm{~V}_{\mathrm{DC}},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq-20^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{CC}}-2.0 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-1.2 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |  |  |  |  |  |
| De-energized Coil Leakage Current | - | - | - | $\pm 100$ | $\mu \mathrm{~A}$ |  |  |  |  |  |

3. Voltage across the coils shall be measured at the specific voltages, but shall also be within linearly interpolated limits.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}, 6.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 15.5 \mathrm{~V}\right.$; unless otherwise stated. All voltage shall be referenced to GND unless otherwise noted. Overvoltage shutdown of coils occurs when $\mathrm{V}_{\mathrm{CC}}>16 \mathrm{~V}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Short Circuit Protection |  |  |  |  |  |
| Short Circuit Threshold I Coil A + I Coil B | - | - | 275 | 400 | mA |
| Short Circuit Turn-Off Delay | - | - | 5.0 | - | $\mu \mathrm{s}$ |

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| DIP-8 | PIN SYMBOL |  |
| 1 | GND | FUNCTION |
| 2 | COILA + | Output stage, when active, this pin supplies current to COIL A. |
| 3 | COILA- | Output stage, when active, this pin supplies current to COIL A. |
| 4 | SENSOR | Input signal from wheel speed or engine rpm. |
| 5 | SELECT | Selects divide by 1 or divide by 2 mode. |
| 6 | COILB- | Output stage, when active, this pin supplies current to COIL B. |
| 7 | COILB+ | Output stage, when active, this pin supplies current to COIL B. |
| 8 | $\mathrm{~V}_{\text {CC }}$ | Supply voltage. |

## CIRCUIT OPERATION

## SPEED SENSOR INPUT

SENSOR is a PNP comparator input which accepts a sine wave or a square wave input. This input is protected from excursions above $\mathrm{V}_{\mathrm{CC}}$ as well as any below ground, as long as the current is limited to 1.5 mA . It has an active clamp set to zero volts to prevent negative input voltages from disrupting normal operation. The sensor input can withstand $150 \mathrm{~V}_{\mathrm{DC}}$ as long as the input current is limited to 1.5 mA max. using a series resistor of $100 \mathrm{k} \Omega$.

## COIL DRIVER OUTPUTS

Simultaneously energizing the source and sink on either leg is not permitted, i.e. Q1 \& Q2 or Q3 \& Q4 cannot be energized simultaneously.

Circuit function is not affected by inductive transients due to coil loads as specified in the Transition States section.

The transition states occur as indicated in Table 1 without any intermediate states permitted.

Table 1. Transition States

| State | Coil A | Coil B |
| :---: | :---: | :---: |
| 0 | + | + |
| 1 | OFF | + |
| 2 | - | + |
| 3 | - | OFF |
| 4 | - | - |
| 5 | OFF | - |
| 6 | + | - |
| 7 | + | OFF |

The polarity definition for the coil driver outputs is as follows:

| Polarity | Connect Coil + | Connect Coil - |
| :---: | :---: | :---: |
| Positive (+) | V $_{\text {CC }}$ | GND |
| Negative ( - ) | GND | $\mathrm{V}_{\mathrm{CC}}$ |

## DIVIDER SELECT INPUT

The speed sensor input frequency is divided by one or divided by two by connecting the divider select input, (Pin 5) as follows:

Logic $0=$ divide by 2 .
Logic $1=$ divide by 1 .


Figure 2. Coil Driver Output


Figure 3. Divide by 1 (8 Step Mode), SELECT = 1


Figure 4. Divide by 2 (16 Step Mode), SELECT = 0

## CS8441



Figure 5. Odometer Application Diagram

PACKAGE THERMAL DATA

| Parameter |  | DIP-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 52 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS4161

## 85 mA Dual H-Bridge Odometer Driver with Divide by Select and UVLO

The CS4161 is a Stepper Motor Driver that implements an H -Bridge design in order to drive two coils in an eight step sequence per revolution in the divide by 1 mode; 16 step sequence in the divide by 2 mode. The H -Bridge is capable of delivering 85 mA to the load.

The sequencer insures that the odometer is monotonic. This sequencer is configured such that simultaneous conduction does not occur. Before each successive output sequence the part is taken through a state where both outputs are turned off individually. This tends to minimize the inductive kick back energy that the part must absorb. On chip clamp diodes are across each output to protect the part from the kick back energy that it must absorb.

The CS4161 includes overvoltage and short circuit protection circuitry. It is lead for lead compatible with the CS8441. The CS4161 includes an additional undervoltage lockout (UVLO) function which disables the output stage until the supply voltage rises above 5.6 V , typically. The UVLO has hysteresis to prevent any power up glitching.

## Features

- Undervoltage Lockout
- Cross-Conduction Prevention Logic
- Divide by 1 and Divide by 2 Modes
- Guaranteed Monotonic
- On-Chip Flyback Diodes
- Fault Protection
- Overvoltage
- Load Dump Protection to 60 V


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) (Note 1): | Continuous 100 ms Pulse Transient | $\begin{aligned} & -0.5 \text { to } 24 \\ & -0.5 \text { to } 60 \end{aligned}$ | V |
| Input Voltage ( $\mathrm{V}_{\mathrm{IN}}$ ) |  | -0.3 to $\mathrm{V}_{\mathrm{CC}}+0.3$ | V |
| Operating Temperature Range |  | -40 to 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range (TSTG) |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature Range |  | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering: | Wave Solder: (through hole styles only) (Note 2) | 260 peak | ${ }^{\circ} \mathrm{C}$ |

1. $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.
2. 10 second maximum.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}, 6.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 15.5 \mathrm{~V}\right.$; unless otherwise stated. All voltage shall be referenced to GND unless otherwise noted. Overvoltage shutdown of coils occurs when $\mathrm{V}_{\mathrm{CC}}>16 \mathrm{~V}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply, $\mathrm{V}_{\text {cc }}$ |  |  |  |  |  |
| Supply Voltage Range | $\begin{aligned} & -40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C} \\ & -40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C} \\ & \text { Transient Pulse, } 100 \mathrm{~ms} \end{aligned}$ | $\begin{aligned} & 6.5 \\ & 6.5 \\ & - \end{aligned}$ | - | $\begin{gathered} 15.5 \\ 24 \\ 35 \end{gathered}$ | $V_{D C}$ <br> $V_{D C}$ <br> $V_{D C}$ |
| Supply Current | $\mathrm{V}_{\mathrm{CC}}=15.5 \mathrm{~V}_{\mathrm{DC}}$, Outputs not loaded. | - | 24 | 35 | mA |
| Overvoltage Shutdown | - | 16 | - | 23 | V |
| Undervoltage Lockout Voltage | $\mathrm{V}_{\mathrm{CC}}$ Initial Power Up UVLO Hysteresis | $\begin{aligned} & 5.1 \\ & 200 \end{aligned}$ | $\begin{aligned} & 5.6 \\ & 600 \end{aligned}$ | $\begin{gathered} 6.1 \\ 1000 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{mV} \end{gathered}$ |

## Speed Sensor Input, SENSOR

| Input Frequency Range | - | - | 0.2 | 1.0 | kHz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Switching Threshold | - | 1.2 | - | 2.6 | $\mathrm{~V}_{\mathrm{DC}}$ |
| Hysteresis | - | 300 | 500 | - | $\mathrm{m} \mathrm{V}_{\mathrm{DC}}$ |
| Input Bias Current | $0.8 \mathrm{~V}_{\mathrm{DC}} \leq \mathrm{V}_{\mathrm{IN}} \leq \mathrm{V}_{\mathrm{CC}}$ | - | - | 0.1 | $\pm 1.0$ |
| Input Voltage Range |  | - |  |  |  |
| Operating Input Voltage | $10 \mathrm{k} \Omega$ Resistor in Series | - | - | -15 to $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{DC}}$ |
| Input Clamp Current | I Clamp at $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}_{\mathrm{DC}}$ | - | -0.4 | -5.0 | mA |

## Divider Select Input, SELECT

| Logic 0 Input Voltage | - | - | - | 100 | $\mathrm{~m} \mathrm{~V}_{\mathrm{DC}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Logic 1 Input Voltage | - | 3.0 | - | $\mathrm{V}_{\mathrm{CC}}$ | $\mathrm{V}_{\mathrm{DC}}$ |
| Logic 0 Input Current | $0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 100 \mathrm{mV}$ | - | -1.0 | -100 | $\mu \mathrm{~A}$ |
| Logic 1 Input Current | $3.0 \mathrm{~V} \leq \mathrm{V}_{\mathbb{I N}} \leq 15.5 \mathrm{~V}_{\mathrm{DC}}$ | - | 0.75 | 2.0 | mA |

## Coil Output Drivers

| Coil Load | $+25^{\circ} \mathrm{C}$ | 198 | 210 | 222 | $\Omega$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Coil Inductance | - | - | 80 | - | mH |
| Coil Resistance Temperature | Coefficient | - | - | 0.35 | $\% /{ }^{\circ} \mathrm{C}$ |
| Energized Coil Voltage (Note 3) | $\mathrm{V}_{\mathrm{CC}}=6.5 \mathrm{~V}_{\mathrm{DC}}$ | $\mathrm{V}_{\mathrm{CC}}-1.5 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-0.9 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |
| (Both Polarities) A and B | $\mathrm{V}_{\mathrm{CC}}=10 \mathrm{~V}_{\mathrm{DC}}$ | $\mathrm{V}_{\mathrm{CC}}-1.6 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-1.0 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |
|  | $\mathrm{V}_{\mathrm{CC}}=15.5 \mathrm{~V}_{\mathrm{DC}},-20^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{CC}}-1.75 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-1.1 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |
|  | $\mathrm{V}_{\mathrm{CC}}=15.5 \mathrm{~V}_{\mathrm{DC}},-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq-20^{\circ} \mathrm{C}$ | $\mathrm{V}_{\mathrm{CC}}-2.0 \mathrm{~V}$ | $\mathrm{~V}_{\mathrm{CC}}-1.2 \mathrm{~V}$ | - | $\mathrm{V}_{\mathrm{DC}}$ |

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ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 125^{\circ} \mathrm{C}, 6.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 15.5 \mathrm{~V}\right.$; unless otherwise stated. All voltage shall be referenced to GND unless otherwise noted. Overvoltage shutdown of coils occurs when $\mathrm{V}_{\mathrm{CC}}>16 \mathrm{~V}$.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Coil Output Drivers (continued)

| De-energized Coil Leakage Current | - | - | $\pm 100$ | - | $\mu \mathrm{A}$ |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |


| Short Circuit Protection |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| Short Circuit Threshold <br> I Coil A + I Coil B | - | - | 275 | 400 |
| Short Circuit Turn-Off Delay | - | - | $5 A$ |  |

3. Voltage across the coils shall be measured at the specific voltages, but shall also be within linearly interpolated limits.

PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# | FIN SYMBOL |  |
| :---: | :---: | :--- |
| DIP-8 |  | Ground connection. |
| 1 | COILA + | Output stage, when active, this lead supplies current to COIL A. |
| 2 | COILA- | Output stage, when active, this lead supplies current to COIL A. |
| 3 | SENSOR | Input signal from wheel speed or engine rpm. |
| 4 | SELECT | Selects divide by 1 or divide by 2 mode. |
| 5 | COILB- | Output stage, when active, this lead supplies current to COIL B. |
| 6 | COILB+ | Output stage, when active, this lead supplies current to COIL B. |
| 7 | $\mathrm{~V}_{\text {CC }}$ | Supply voltage. |
| 8 |  |  |

## CIRCUIT OPERATION

## SPEED SENSOR INPUT

SENSOR is a PNP comparator input which accepts either a sine wave or a square wave input. This input is protected from excursions above $\mathrm{V}_{\mathrm{CC}}$ as well as any below ground as long as the current is limited to 1.5 mA . It has an active clamp set to zero volts to prevent negative input voltages from disrupting normal operation. The sensor input can withstand $150 \mathrm{~V}_{\mathrm{DC}}$ as long as the input current is limited to 1.5 mA max. using a series resistor of $100 \mathrm{k} \Omega$.

## COIL DRIVER OUTPUTS

Simultaneously energizing the source and sink on either leg is not permitted, i.e. Q1 \& Q2 or Q3 \& Q4 cannot be energized simultaneously.

Circuit function is not affected by inductive transients due to coil loads as specified in the Transition States section.

The transition states occur as indicated in Table 1 without any intermediate states permitted.

Table 1. Transition States

| State | Coil A | Coil B |
| :---: | :---: | :---: |
| 0 | + | + |
| 1 | OFF | + |
| 2 | - | + |
| 3 | - | OFF |
| 4 | - | - |
| 5 | OFF | - |
| 6 | + | - |
| 7 | + | OFF |

The polarity definition for the coil driver outputs is as follows:

| Polarity | Connect Coil + | Connect Coil - |
| :---: | :---: | :---: |
| Positive (+) | $\mathrm{V}_{\mathrm{CC}}$ | GND |
| Negative (-) | GND | $\mathrm{V}_{\mathrm{CC}}$ |

## DIVIDER SELECT INPUT

The speed sensor input frequency is either divided by one or divided by two depending on the state of the SELECT input as follows:

Logic $0=$ divide by 2 .
Logic $1=$ divide by 1 .


Figure 2. Coil Driver Output


Figure 3. Divide by 1 (8 Step Mode), SELECT = 1


Figure 4. Divide by 2 (16 Step Mode), SELECT = 0


Figure 5. Odometer Application Diagram

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PACKAGE THERMAL DATA

| Parameter |  | DIP-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 52 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## Universal Motor Speed Controller

The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramp possibilities.

- On-Chip Frequency to Voltage Converter
- On-Chip Ramps Generator
- Soft-Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Performed by Monitor


## TDA1085C

## UNIVERSAL MOTOR <br> SPEED CONTROLLER

SEMICONDUCTOR
TECHNICAL DATA
PLASTIC PACKAGE
CASE 648
PLASTIC PACKAGE
CASE 751B
(SO-16)

ORDERING INFORMATION

| Device | Operating <br> Temperature Range | Package |
| :---: | :---: | :---: |
| TDA1085CD | $T_{J}=-10^{\circ}$ to $+120^{\circ} \mathrm{C}$ | SO- 16 |
| TDA1085C |  |  |



Figure 1. Representative Block Diagram and Pin Connections

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, voltages are referenced to Pin 8 , ground)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply, when externally regulated, $\mathrm{V}_{\text {Pin }} 9$ | $\mathrm{V}_{\mathrm{CC}}$ | 15 | V |
| Maximum Voltage per listed pin <br> Pin 3 <br> Pin 4-5-6-7-13-14-16 <br> Pin 10 | $V_{\text {Pin }}$ | $\begin{gathered} +5.0 \\ 0 \text { to }+\mathrm{V}_{\mathrm{CC}} \\ 0 \text { to }+17 \end{gathered}$ | V |
| Maximum Current per listed pin Pin 1 and 2 <br> Pin 3 <br> Pin $9\left(V_{C C}\right)$ <br> Pin 10 shunt regulator <br> Pin 12 <br> Pin 13 | $1{ }_{\text {Pin }}$ | $\begin{gathered} -3.0 \text { to }+3.0 \\ -1.0 \text { to }+0 \\ 15 \\ 35 \\ -1.0 \text { to }+1.0 \\ -200 \end{gathered}$ | mA |
| Maximum Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | 1.0 | W |
| Thermal Resistance, Junction-to-Air | $\mathrm{R}_{\text {өJA }}$ | 65 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Junction Temperature | $\mathrm{T}_{J}$ | -10 to +120 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to + 150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}\right)$

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VOLTAGE REGULATOR |  |  |  |  |  |
| Internally Regulated Voltage ( $\mathrm{V}_{\text {Pin } 9}$ ) $\left(I_{\text {Pin } 7}=0, I_{\text {Pin } 9}+I_{\text {Pin } 10}=15 \mathrm{~mA}, I_{\text {Pin } 13}=0\right)$ | $\mathrm{V}_{\mathrm{CC}}$ | 15 | 15.3 | 15.6 | V |
| $\mathrm{V}_{\text {CC }}$ Temperature Factor | TF | - | - 100 | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| Current Consumption ( IPin 9 ) $\left(\mathrm{V}_{9}=15 \mathrm{~V}, \mathrm{~V}_{12}=\mathrm{V}_{8}=0, \mathrm{I}_{1}=\mathrm{I}_{2}=100 \mu \mathrm{~A},\right.$ <br> all other pins not connected) | $I_{\text {cc }}$ | - | 4.5 | 6.0 | mA |
| $\mathrm{V}_{\mathrm{CC}}$ Monitoring Enable Level Disable Level | $\mathrm{V}_{\mathrm{CC}} \mathrm{EN}$ <br> $V_{C C}$ DIS | - | $\begin{aligned} & \mathrm{V}_{C C}-0.4 \\ & \mathrm{~V}_{\mathrm{CC}}-1.0 \end{aligned}$ | - | V |

RAMP GENERATOR

| Reference Speed Input Voltage Range | $V_{\text {Pin } 5}$ | 0.08 | - | 13.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Reference Input Bias Current | - IPin 5 | 0 | 0.8 | 1.0 | $\mu \mathrm{A}$ |
| Ramp Selection Input Bias Current | - $\mathrm{I}_{\text {Pin } 6}$ | 0 | - | 1.0 | $\mu \mathrm{A}$ |
| Distribution Starting Level Range | $V_{\text {DS }}$ | 0 | - | 2.0 | V |
| Distribution Final Level $V_{\text {Pin } 6}=0.75 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{DF}} / \mathrm{V}_{\mathrm{DS}}$ | 2.0 | 2.09 | 2.2 |  |
| High Acceleration Charging Current $\begin{aligned} & V_{\text {Pin } 7}=0 \mathrm{~V} \\ & V_{\text {Pin } 7}=10 \mathrm{~V} \end{aligned}$ | - IPin 7 | $\begin{aligned} & 1.0 \\ & 1.0 \end{aligned}$ | $\overline{1.2}$ | $\begin{aligned} & 1.7 \\ & 1.4 \end{aligned}$ | mA |
| Distribution Charging Current $\mathrm{V}_{\text {Pin } 7}=2.0 \mathrm{~V}$ | $-\mathrm{I}_{\text {Pin } 7}$ | 4.0 | 5.0 | 6.0 | $\mu \mathrm{A}$ |

ELECTRICAL CHARACTERISTICS (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CURRENT LIMITER |  |  |  |  |  |
| $\begin{aligned} & \text { Limiter Current Gain — } l_{\text {Pin } 7} / I_{\text {Pin } 3} \\ & \left(I_{\text {Pin3 }}=-300 \mu \mathrm{~A}\right) \end{aligned}$ | $\mathrm{C}_{\text {g }}$ | 130 | 180 | 250 |  |
| Detection Threshold Voltage $I_{\text {Pin } 3}=-10 \mu \mathrm{~A}$ | $\mathrm{V}_{\text {Pin } 3 \text { TH }}$ | 50 | 65 | 80 | mV |

FREQUENCY TO VOLTAGE CONVERTER

| Input Signal "Low Voltage" Input Signal "High Voltage" Monitoring Reset Voltage | $\begin{aligned} & V_{12 \mathrm{~L}} \\ & \mathrm{~V}_{122} \mathrm{H} \\ & \mathrm{~V}_{12} \mathrm{R} \end{aligned}$ | $\begin{gathered} -100 \\ +100 \\ 5.0 \end{gathered}$ | - | - | $\begin{gathered} \mathrm{mV} \\ \mathrm{mV} \\ \mathrm{~V} \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Negative Clamping Voltage $I_{\text {Pin } 12}=-200 \mu \mathrm{~A}$ | - $\mathrm{V}_{12 \mathrm{CL}}$ | - | 0.6 | - | V |
| Input Bias Current | - I ${ }_{\text {Pin12 }}$ | - | 25 | - | $\mu \mathrm{A}$ |
| Internal Current Source Gain $\mathrm{G}=\frac{\mathrm{I}_{\operatorname{Pin} 4}}{\mathrm{I}_{\operatorname{Pin} 11}}, \mathrm{~V}_{\operatorname{Pin} 4}=\mathrm{V}_{\operatorname{Pin} 11}=0$ | G. 0 | 9.5 | - | 11 |  |
| $\begin{aligned} & \text { Gain Linearity versus Voltage on Pin } 4 \\ & \left(\mathrm{G}_{8.6}=\text { Gain for } \mathrm{V}_{\text {Pin } 4}=8.6 \mathrm{~V}\right) \\ & \mathrm{V}_{4}=0 \mathrm{~V} \\ & \mathrm{~V}_{4}=4.3 \mathrm{~V} \\ & \mathrm{~V}_{4}=12 \mathrm{~V} \end{aligned}$ | $\mathrm{G} / \mathrm{G}_{8.6}$ | $\begin{aligned} & 1.04 \\ & 1.015 \\ & 0.965 \end{aligned}$ | $\begin{gathered} 1.05 \\ 1.025 \\ 0.975 \end{gathered}$ | $\begin{gathered} 1.06 \\ 1.035 \\ 0.985 \end{gathered}$ |  |
| Gain Temperature Effect ( $\mathrm{V}_{\text {Pin } 4}=0$ ) | TF | - | 350 | - | ppm $/{ }^{\circ} \mathrm{C}$ |
| Output Leakage Current ( $\left.\mathrm{I}_{\text {Pin } 11}=0\right)$ | $-I_{\text {Pin } 4}$ | 0 | - | 100 | nA |

CONTROL AMPLIFIER

| Actual Speed Input Voltage Range | $V_{\text {Pin }} 4$ | 0 | - | 13.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Input Offset Voltage } V_{\text {Pin } 5}-V_{\text {Pin } 4} \\ & \quad\left(I_{\text {Pin } 16}=0, V_{\text {Pin } 16}=3.0 \text { and } 8.0 \mathrm{~V}\right. \text { ) } \end{aligned}$ | $\mathrm{V}_{\text {off }}$ | 0 | - | 50 | mV |
| Amplifier Transconductance <br> $\left(I_{\text {Pin }} 16 / \Delta\left(V_{5}-V_{4}\right)\right.$ <br> ( $\mathrm{I}_{\text {Pin } 16}=+$ and $-50 \mu \mathrm{~A}, \mathrm{~V}_{\text {Pin } 16}=3.0 \mathrm{~V}$ ) | T | 270 | 340 | 400 | $\mu \mathrm{A} / \mathrm{V}$ |
| Output Current Swing Capability <br> Source <br> Sink | $\mathrm{I}_{\text {Pin } 16}$ | $\begin{gathered} -200 \\ 50 \end{gathered}$ | $\begin{gathered} -100 \\ 100 \end{gathered}$ | $\begin{array}{r} -50 \\ 200 \end{array}$ | $\mu \mathrm{A}$ |
| Output Saturation Voltage | $\mathrm{V}_{16 \text { sat }}$ | - | - | 0.8 | V |

TRIGGER PULSE GENERATOR

| Synchronization Level Currents Voltage Line Sensing Triac Sensing | $\begin{aligned} & I_{\text {Pin } 2} \\ & I_{\text {Pin } 1} \end{aligned}$ |  | $\begin{aligned} & \pm 50 \\ & \pm 50 \end{aligned}$ | $\begin{aligned} & \pm 100 \\ & \pm 100 \end{aligned}$ | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Trigger Pulse Duration ( $\mathrm{C}_{\text {Pin } 14}=47 \mathrm{nF}, \mathrm{R}_{\text {Pin } 15}=270 \mathrm{k} \Omega$ ) | $\mathrm{T}_{\mathrm{p}}$ | - | 55 | - | $\mu \mathrm{s}$ |
| Trigger Pulse Repetition Period, conditions as a.m. | $\mathrm{T}_{\mathrm{R}}$ | - | 220 | - | $\mu \mathrm{s}$ |
| Output Pulse Current $\mathrm{V}_{\text {Pin } 13}=\mathrm{V}_{\text {CC }}-4.0 \mathrm{~V}$ | $-\mathrm{I}_{\text {Pin } 13}$ | 180 | 192 | - | mA |
| Output Leakage Current $\mathrm{V}_{\text {Pin } 13}=-3.0 \mathrm{~V}$ | $\mathrm{I}_{13 \mathrm{~L}}$ | - | - | 30 | $\mu \mathrm{A}$ |
| Full Angle Conduction Input Voltage | $\mathrm{V}_{14}$ | - | 11.7 | - | V |
| Saw Tooth "High" Level Voltage | $\mathrm{V}_{14 \mathrm{H}}$ | 12 | - | 12.7 | V |
| Saw Tooth Discharge Current, $\mathrm{I}_{\text {Pin15 }}=100 \mu \mathrm{~A}$ | $l_{\text {Pin } 14}$ | 95 | - | 105 | $\mu \mathrm{A}$ |

## GENERAL DESCRIPTION

The TDA 1085C triggers a triac accordingly to the speed regulation requirements. Motor speed is digitally sensed by a tachogenerator and then converted into an analog voltage.

The speed set is externally fixed and is applied to the internal linear regulation input after having been submitted to programmable acceleration ramps. The overall result
consists in a full motor speed range with two acceleration ramps which allow efficient washing machine control (Distribute function).
Additionally, the TDA 1085C protects the whole system against AC line stop or variations, overcurrent in the motor and tachogenerator failure.

## INPUT/OUTPUT FUNCTIONS

(Refer to Figures 1 and 8)

Voltage Regulator - (Pins 9 and 10) This is a parallel type regulator able to sink a large amount of current and offering good characteristics. Current flow is provided from AC line by external dropping resistors R1, R2, and rectifier: This half wave current is used to feed a smothering capacitor, the voltage of which is checked by the IC.

When $\mathrm{V}_{\mathrm{CC}}$ is reached, the excess of current is derived by another dropping resistor R10 and by Pin 10 . These three resistors must be determined in order:

- To let 1.0 mA flow through Pin 10 when AC line is minimum and $\mathrm{V}_{\mathrm{CC}}$ consumption is maximum (fast ramps and pulses present).
- To let $\mathrm{V}_{10}$ reach 3.0 V when AC line provides maximum current and $\mathrm{V}_{\mathrm{CC}}$ consumption is minimum (no ramps and no pulses).
- All along the main line cycle, the Pin 10 dynamic range must not be exceeded unless loss of regulation.
An AC line supply failure would cause shut down.
The double capacitive filter built with R1 and R2 gives an efficient $\mathrm{V}_{\mathrm{CC}}$ smoothing and helps to remove noise from set speeds.

Speed Sensing - (Pins 4, 11, 12) The IC is compatible with an external analog speed sensing: its output must be applied to Pin 4, and Pin 12 connected to Pin 8.

In most of the applications it is more convenient to use a digital speed sensing with an inexpensive tachogenerator which doesn't need any tuning. During every positive cycle at Pin 12, the capacitor $C_{P i n} 11$ is charged to almost $\mathrm{V}_{\mathrm{CC}}$ and during this time, Pin 4 delivers a current which is 10 times the one charging $\mathrm{C}_{\text {Pin }}$ 11. The current source gain is called $G$ and is tightly specified, but nevertheless requires an adjustment on $\mathrm{R}_{\mathrm{Pin} 4}$. The current into this resistor is proportional to $\mathrm{C}_{\text {Pin }} 11$ and to the motor speed; being filtered by a capacitor, $V_{\text {Pin } 4}$ becomes smothered and represents the "true actual motor speed".

To maintain linearity into the high speed range, it is important to verify that $\mathrm{C}_{\mathrm{Pin} 11}$ is fully charged: the internal source on Pin 11 has $100 \mathrm{~K} \Omega$ impedance. Nevertheless $\mathrm{C}_{\text {Pin } 11}$ has to be as high as possible as it has a large influence on FV/C temperature factor. A $470 \mathrm{~K} \Omega$ resistor between Pins 11 and 9 reduces leakage currents and temperature factor as well, down to neglectable effects.

Pin 12 also has a monitoring function: when its voltage is above 5.0 V , the trigger pulses are inhibited and the IC is
reset. It also senses the tachogenerator continuity, and in case of any circuit aperture, it inhibits pulse, avoiding the motor to run out of control. In the TDA 1085C, Pin 12 is negatively clamped by an internal diode which removes the necessity of the external one used in the former circuit.
Ramp Generator - (Pins 5, 6, 7) The true Set Speed value taken in consideration by the regulation is the output of the ramp generator ( $\operatorname{Pin} 7$ ). With a given value of speed set input (Pin 5), the ramp generator charges an external capacitor $C_{\text {Pin } 7}$ up to the moment $V_{\text {Pin } 5}$ (set speed) equals $\mathrm{V}_{\text {Pin }} 4$ (true speed), see Figure 2. The IC has an internal charging current source of 1.2 mA and delivers it from 0 to 12 V at Pin 7. It is the high acceleration ramp ( 5.0 s typical) which allows rapid motor speed changes without excessive strains on the mechanics. In addition, the TDA 1085C offers the possibility to break this high acceleration with the introduction of a low acceleration ramp (called Distribution) by reducing the Pin 7 source current down to $5.0 \mu \mathrm{~A}$ under Pin 6 full control, as shown by following conditions:

- Presence of high acceleration ramp $V_{\text {Pin } 5}>V_{\text {Pin } 4}$
- Distribution occurs in the $V_{\text {Pin }} 4$ range (true motor speed) defined by $\mathrm{V}_{\text {Pin } 6} \leqq \mathrm{~V}_{\text {Pin } 4} \leqq 2.0 \mathrm{~V}_{\text {Pin } 6}$
For two fixed values of $V_{\text {Pin }} 5$ and $V_{\text {Pin 6 }}$, the motor speed will have high acceleration, excluding the time for $\mathrm{V}_{\text {Pin } 4}$ to go from $\mathrm{V}_{\text {Pin }} 6$ to two times this value, high acceleration again, up to the moment the motor has reached the set speed value, at which it will stay, see Figure 3.
Should a reset happen (whatever the cause would be), the above mentioned successive ramps will be fully reprocessed from 0 to the maximum speed. If $\mathrm{V}_{\operatorname{Pin} 6}=0$, only the high acceleration ramp occurs.
To get a real zero speed position, Pin 5 has been designed in such a way that its voltage from 0 to 80 mV is interpreted as a true zero. As a consequence, when changing the speed set position, the designer must be sure that any transient zero would not occur: if any, the entire circuit will be reset.
As the voltages applied by Pins 5 and 6 are derived from the internal voltage regulator supply and Pin 4 voltage is also derived from the same source, motor speed (which is determined by the ratios between above mentioned voltages) is totally independent from $\mathrm{V}_{\mathrm{CC}}$ variations and temperature factor.

Control Amplifier - (Pin 16) It amplifies the difference between true speed (Pin 4) and set speed (Pin 5), through the
ramp generator. Its output available at Pin 16 is a double sense current source with a maximum capability of $\pm 100 \mu \mathrm{~A}$ and a specified transconductance ( $340 \mu \mathrm{~A} / \mathrm{V}$ typical). Pin 16 drives directly the trigger pulse generator, and must be loaded by an electrical network which compensates the mechanical characteristics of the motor and its load, in order to provide stability in any condition and shortest transient response; see Figure 4.

This network must be adjusted experimentally.
In case of a periodic torque variations, Pin 16 directly provides the phase angle oscillations.

Trigger Pulse Generator - (Pins 1, 2, 5, 13, 14, 15) This circuit performs four functions:

- The conversion of the control amplifier DC output level to a proportional firing angle at every main line half cycle.
- The calibration of pulse duration.
- The repetition of the pulse if the triac fails to latch on if the current has been interrupted by brush bounce.
- The delay of firing pulse until the current crosses zero at wide firing angles and inductive loads.
$R_{\text {Pin }} 15$ programs the Pin 14 discharging current. Saw tooth signal is then fully determined by R15 and C14 (usually 47 nF ). Firing pulse duration and repetition period are in inverse ratio to the saw tooth slope.

Pin 13 is the pulse output and an external limiting resistor is mandatory. Maximum current capability is 200 mA .
Current Limiter - (Pin 3) Safe operation of the motor and triac under all conditions is ensured by limiting the peak current. The motor current develops an alternative voltage in the shunt resistor ( $0.05 \Omega$ in Figure 4). The negative half waves are transferred to Pin 3 which is positively preset at a voltage determined by resistors R3 and R4. As motor current increases, the dynamical voltage range of Pin 3 increases and when Pin 3 becomes slightly negative in respect to Pin 8, a current starts to circulate in it. This current, amplified typically 180 times, is then used to discharge Pin 7 capacitor and, as a result, reduces firing angle down to a value where an equilibrium is reached. The choice of resistors R3, R4 and shunt determines the magnitude of the discharge current signals on $C_{\text {Pin }} 7$.

Notice that the current limiter acts only on peak triac current.

## APPLICATION NOTES

## (Refer to Figure 4)

## Printed Circuit Layout Rules

In the common applications, where TDA 1085C is used, there is on the same board, presence of high voltage, high currents as well as low voltage signals where millivolts count. It is of first magnitude importance to separate them from each other and to respect the following rules:

- Capacitor decoupling pins, which are the inputs of the same comparator, must be physically close to the IC, close to each other and grounded in the same point.
- Ground connection for tachogenerator must be directly connected to Pin 8 and should ground only the tacho. In effect, the latter is a first magnitude noise generator due to its proximity to the motor which induces high $\mathrm{d} \phi / \mathrm{dt}$ signals.
- The ground pattern must be in the "star style" in order to fully eliminate power currents flowing in the ground network devoted to capacitors decoupling sensitive Pins: 4, 5, 7, 11, 12, 14, 16.
As an example, Figure 5 presents a PC board pattern which concerns the group of sensitive Pins and their associated capacitors into which the a.m. rules have been implemented. Notice the full separation of "Signal World" from "Power", one by line AB and their communication by a unique strip.

These rules will lead to much satisfactory volume production in the sense that speed adjustment will stay valid in the entire speed range.

## Power Supply

As dropping resistor dissipates noticeable power, it is necessary to reduce the $\mathrm{I}_{\mathrm{CC}}$ needs down to a minimum.

Triggering pulses, if a certain number of repetitions are kept in reserve to cope with motor brush wearing at the end of its life, are the largest $\mathrm{I}_{\mathrm{CC}}$ user. Classical worst case configuration has to be considered to select dropping resistor. In addition, the parallel regulator must be always into its dynamic range, i.e., $\mathrm{I}_{\text {Pin } 10}$ over 1.0 mA and $\mathrm{V}_{\text {Pin }} 10$ over 3.0 V in any extreme configuration. The double filtering cell is mandatory.

## Tachogenerator Circuit

The tacho signal voltage is proportional to the motor speed. Stability considerations, in addition, require an RC filter, the pole of which must be looked at. The combination of both elements yield a constant amplitude signal on Pin 12 in most of the speed range. It is recommended to verify this maximum amplitude to be within 1.0 V peak in order to have the largest signal/noise ratio without resetting the integrated circuit (which occurs if $\mathrm{V}_{\text {Pin }} 12$ reaches 5.5 V ). It must be also verified that the Pin 12 signal is approximately balanced between "high" (over 300 mV ) and "low". An 8-poles tacho is a minimum for low speed stability and a 16 -poles is even better.

The RC pole of the tacho circuit should be chosen within 30 Hz in order to be as far as possible from the 150 Hz which corresponds to the AC line 3rd harmonic generated by the motor during starting procedure. In addition, a high value resistor coming from $\mathrm{V}_{\mathrm{CC}}$ introduces a positive offset at Pin 12, removes noise to be interpreted as a tacho signal. This offset should be designed in order to let Pin 12 reach at least - 200 mV (negative voltage) at the lowest motor speed. We remember the necessity of an individual tacho ground connection.

## Frequency to Voltage Converter - F V/C

$\mathrm{C}_{\text {Pin }} 11$ has a recommended value of 820 pF for 8-poles tachos and maximum motor rpm of 15000 , and $\mathrm{R}_{\text {Pin }} 11$ must be always 470 K .
$\mathrm{R}_{\text {Pin } 4}$ should be choosen to deliver within 12 V at maximum motor speed in order to maximize signal/noise ratio. As the $\mathrm{FV} / \mathrm{C}$ ratio as well as the $\mathrm{C}_{\text {Pin } 11}$ value are dispersed, $R_{\text {Pin } 4}$ must be adjustable and should be made of a fixed resistor in service with a trimmer representing 25\% of the total. Adjustment would become easier.

Once adjusted, for instance at maximum motor speed, the FV/C presents a residual non linearity; the conversion factor ( mV per RPM) increases by within $7.7 \%$ as speed draws to zero. The guaranteed dispersion of the latter being very narrow, a maximum $1 \%$ speed error is guaranteed if during Pin 5 network design the small set values are modified, once forever, according this increase.

The following formulas give $V_{\text {Pin } 4 \text { : }}$

$$
\begin{aligned}
& V_{\text {Pin } 4}=G .0 \cdot\left(V_{C C}-V_{a}\right) \cdot C_{\text {Pin } 11} \cdot R_{4} \cdot f \cdot{ }_{\left(1+\frac{120 k}{} \frac{1}{R_{\text {Pin } 11}}\right)}{ }^{\text {In volts. }} \\
& G .0 \cdot\left(V_{C C}-V_{a}\right) \simeq 140 \\
& V_{a}=2 . V_{B E} \\
& 120 \mathrm{k}=R_{\text {int }}, \text { on Pin } 11
\end{aligned}
$$

Speed Set - (Pin 5) Upon designer choice, a set of external resistors apply a series of various voltages corresponding to the various motor speeds. When switching external resistors, verify that no voltage below 80 mV is ever applied to Pin 5. If so, a full circuit reset will occur.

Ramps Generator - (Pin 6) If only a high acceleration ramp is needed, connect Pin 6 to ground.

When a Distribute ramp should occur, preset a voltage on Pin 6 which corresponds to the motor speed starting ramp point. Distribution (or low ramp) will continue up to the moment the motor speed would have reached twice the starting value.

The ratio of two is imposed by the IC. Nevertheless, it could be externally changed downwards (Figure 6) or upwards (Figure 7).

The distribution ramp can be shortened by an external resistor from $\mathrm{V}_{\mathrm{CC}}$ charging $\mathrm{C}_{\text {Pin 7 }}$, adding its current to the internal $5.0 \mu \mathrm{~A}$ generator.


Figure 2. Acceleration Ramp

## Power Circuits

Triac Triggering pulse amplitude must be determined by Pin 13 resistor according to the needs in Quadrant IV. Trigger pulse duration can be disturbed by noise signals generated by the triac itself, which interfere within Pins 14 and 16 , precisely those which determine it. While easily visible, this effect is harmless.

The triac must be protected from high AC line $\mathrm{dV} / \mathrm{dt}$ during external disturbances by $100 \mathrm{nF} \times 100 \Omega$ network.

Shunt resistor must be as non-inductive as possible. It can be made locally by using constantan alloy wire.

When the load is a DC fed universal motor through a rectifier bridge, the triac must be protected from commutating dV/dt by a 1.0 to 2.0 mH coil in series with $\mathrm{MT}_{2}$.

Synchronization functions are performed by resistors sensing AC line and triac conduction. 820 k values are normal but could be reduced down to 330 k in order to detect the "zeros" with accuracy and to reduce the residual DC line component below 20 mA .

## Current Limitation

The current limiter starts to discharge Pin 7 capacitor (reference speed) as the motor current reaches the designed threshold level. The loop gain is determined by the resistor connecting Pin 3 to the series shunt. Experience has shown that its optimal value for a 10 Arms limitation is within $2.0 \mathrm{k} \Omega$ Pin 3 input has a sensitivity in current which is limited to reasonable values and should not react to spikes.
If not used, Pin 3 must be connected to a maximum positive voltage of 5.0 V rather than be left open.

## Loop Stability

The Pin 16 network is predominant and must be adjusted experimentally during module development. The values indicated in Figure 4 are typical for washing machine applications but accept large modifications from one model to another. R16 (the sole restriction) should not go below 33 k , otherwise slew rate limitation will cause large transient errors for load steps.


Figure 3. Programmable Double Acceleration Ramp



TDA1085C

## TDA1085C

For $k=1.6, \quad R_{3}=0.6(R 1+R 2)$,
$\mathrm{R}_{3} \mathrm{C}$ within 4 seconds


Figure 6. Distribution Speed $\mathbf{k}<2$


Figure 7. Distribution Speed k > 2

${ }^{*}($ P12 connected $)$ and ( $\mathrm{V}_{\mathrm{CC}} \mathrm{OK}$ ) and (VP5>80 mV)
Then
(I1 OFF),(I2 OFF), (I4 OFF) and (I5 OFF)

## CS4121

## Low Voltage Precision Air-Core Tach/Speedo Driver

The CS4121 is specifically designed for use with air-core meter movements. The IC provides all the functions necessary for an analog tachometer or speedometer. The CS4121 takes a speed sensor input and generates sine and cosine related output signals to differentially drive an air-core meter.

Many enhancements have been added over industry standard tachometer drivers such as the CS289 or LM1819. The output utilizes differential drivers which eliminates the need for a zener reference and offers more torque. The device withstands 60 V transients which decreases the protection circuitry required. The device is also more precise than existing devices allowing for fewer trims and for use in a speedometer.

The CS4121 is compatible with the CS8190, and provides higher accuracy at a lower supply voltage ( 8.0 V min. as opposed to 8.5 V ). It is functionally operational to 6.5 V .

## Features

- Direct Sensor Input
- High Torque Output
- Low Pointer Flutter
- High Input Impedance
- Overvoltage Protection
- Accurate to 8.0 V Functional to 6.5 V (typ)
- Internally Fused Leads in SO-20 Package and DIP-16

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONNECTIONS AND
MARKING DIAGRAM


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS4121EDWF20 | SO-20L | 37 Units/Rail |
| CS4121EDWFR20 | SO-20L | 1000 Tape \& Reel |
| CS4121ENF16 | DIP-16 | 25 Units/Rail |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*
$\left.\begin{array}{|l|c|c|c|}\hline & \text { Rating } & \text { Value } \\ \hline \text { Supply Voltage, } \mathrm{V}_{\mathrm{CC}} & <100 \mathrm{~ms} \mathrm{Pulse} \mathrm{Transient} \\ \text { Continuous }\end{array}\right)$

1. 10 seconds maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, 8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}\right.$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage Section |  |  |  |  |  |
| ICC Supply Current | $\mathrm{V}_{C C}=16 \mathrm{~V},-40^{\circ} \mathrm{C}$, No Load | - | 50 | 125 | mA |
| $\mathrm{V}_{\text {CC }}$ Normal Operation Range | - | 8.0 | 13.1 | 16 | V |

Input Comparator Section

| Positive Input Threshold | - | 1.0 | 2.0 | 3.0 | V |  |  |  |  |  |  |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Hysteresis | - | 200 | 500 | - | mV |  |  |  |  |  |  |  |
| Input Bias Current (Note 3) | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 8.0 \mathrm{~V}$ | - | -10 | -80 | $\mu \mathrm{~A}$ |  |  |  |  |  |  |  |
| Input Frequency Range |  |  |  |  |  |  |  | - | 0 | - | 20 | kHz |
| Input Voltage Range | in series with $1.0 \mathrm{k} \Omega$ | -1.0 | - | $\mathrm{V}_{\mathrm{CC}}$ | V |  |  |  |  |  |  |  |
| Output $\mathrm{V}_{\text {SAT }}$ | $\mathrm{I}_{\mathrm{CC}}=10 \mathrm{~mA}$ | 0 | 0.15 | 0.40 | V |  |  |  |  |  |  |  |
| Output Leakage | $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ | - | - | 10 | $\mu \mathrm{~A}$ |  |  |  |  |  |  |  |
| Logic 0 Input Voltage |  | 1.0 | - | - | V |  |  |  |  |  |  |  |

Voltage Regulator Section

| Output Voltage | - | 6.25 | 7.00 | 7.50 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Load Current | - | - | - | 10 | mA |
| Output Load Regulation | 0 to 10 mA | - | 10 | 50 | mV |
| Output Line Regulation | $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | - | 20 | 150 | mV |
| Power Supply Rejection | $\mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}, 1.0 \mathrm{~V}_{\mathrm{P} / \mathrm{P}} 1.0 \mathrm{kHz}$ | 34 | 46 | - | dB |

## Charge Pump Section

| Inverting Input Voltage | - | 1.5 | 2.0 | 2.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | - | - | 40 | 150 | nA |
| $V_{\text {BIAS }}$ Input Voltage | - | 1.5 | 2.0 | 2.5 | V |
| Non Invert. Input Voltage | $\mathrm{I}_{\mathrm{N}}=1.0 \mathrm{~mA}$ | - | 0.7 | 1.1 | V |
| Linearity (Note 4) | @ 0, 87.5, 175, 262.5, + 350 Hz | -0.10 | 0.28 | +0.70 | \% |
| F/Vout Gain | $\begin{aligned} & @ 350 \mathrm{~Hz}, \mathrm{C}_{\mathrm{CP}}=0.0033 \mu \mathrm{~F}, \\ & \mathrm{R}_{\mathrm{T}}=243 \mathrm{k} \Omega \end{aligned}$ | 7.0 | 10 | 13 | $\mathrm{mV} / \mathrm{Hz}$ |
| Norton Gain, Positive | $\mathrm{I}_{\mathrm{IN}}=15 \mu \mathrm{~A}$ | 0.9 | 1.0 | 1.1 | I/I |
| Norton Gain, Negative | $\mathrm{I}_{\mathrm{IN}}=15 \mu \mathrm{~A}$ | 0.9 | 1.0 | 1.1 | 1/1 |

Function Generator Section: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}$ unless otherwise noted.
$\left.\begin{array}{|l|l|c|c|c|c|}\left.\hline \begin{array}{l}\text { Differential Drive Voltage } \\ \left(\mathrm{V}_{\mathrm{COS}}^{+}\right.\end{array}-\mathrm{V}_{\text {COS- }-}\right)\end{array}, \begin{array}{l}8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V} \\ \Theta=0^{\circ}\end{array}\right)$
3. Input is clamped by an internal 12 V Zener.
4. Applies to $\%$ of full scale $\left(270^{\circ}\right)$.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, 8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}\right.$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Function Generator Section: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}$ unless otherwise noted. (continued) |  |  |  |  |  |
| Differential Drive Current | $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | - | 33 | 42 | mA |
| Zero Hertz Output Angle | - | -1.5 | 0 | 1.5 | deg |
| Function Generator Error (Note 5) Reference Figures 2, 3, 4, 5 | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \Theta=0^{\circ} \text { to } 305^{\circ} \end{aligned}$ | -2.0 | 0 | +2.0 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | -2.5 | 0 | +2.5 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 11 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | -1.0 | 0 | +1.0 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 8.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | -3.0 | 0 | +3.0 | deg |
| Function Generator Error | $25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$ | -3.0 | 0 | +3.0 | deg |
| Function Generator Error | $25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}$ | -5.5 | 0 | +5.5 | deg |
| Function Generator Error | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C}$ | -3.0 | 0 | +3.0 | deg |
| Function Generator Gain | $\Theta$ vs $\mathrm{F} / \mathrm{V}_{\text {OUT, }}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 60 | 77 | 95 | \% V |

5. Deviation from nominal per Table 1 after calibration at $0^{\circ}$ and $270^{\circ}$.

## PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| DIP-16 | SO-20L |  |  |
| 1 | 1 | CP+ | Positive input to charge pump. |
| 2 | 2 | SQout | Buffered square wave output signal. |
| 3 | 3 | FREQ ${ }_{\text {IN }}$ | Speed or RPM input signal. |
| 4, 5, 12, 13 | 4-7, 14-17 | GND | Ground Connections. |
| 6 | 8 | COS+ | Positive cosine output signal. |
| 7 | 9 | cos- | Negative cosine output signal. |
| 8 | 10 | $\mathrm{V}_{\mathrm{CC}}$ | Ignition or battery supply voltage. |
| 9 | 11 | BIAS | Test point or zero adjustment. |
| 10 | 12 | SIN- | Negative sine output signal. |
| 11 | 13 | SIN+ | Positive sine output signal. |
| 14 | 18 | $\mathrm{V}_{\text {REG }}$ | Voltage regulator output. |
| 15 | 19 | F/VOUT | Output voltage proportional to input signal frequency. |
| 16 | 20 | CP- | Negative input to charge pump. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Function Generator Output Voltage vs. Degrees of Deflection


Figure 4. Output Angle in Polar Form


Figure 3. Charge Pump Output Voltage vs. Output Angle


Figure 5. Nominal Output Deviation


Figure 6. Nominal Angle vs. Ideal Angle (After Calibrating at $\mathbf{1 8 0}^{\boldsymbol{\circ}}$ )

Table 1. Function Generator Output Nominal Angle vs. Ideal Angle (After Calibrating at 270)

| Ideal $\Theta$ Degrees | Nominal <br> $\Theta$ <br> Degrees | Ideal $\Theta$ Degrees | Nominal <br> $\Theta$ <br> Degrees | Ideal $\Theta$ Degrees | Nominal <br> $\Theta$ <br> Degrees | Ideal $\Theta$ Degrees | Nominal <br> $\Theta$ <br> Degrees | Ideal $\Theta$ Degrees | Nominal <br> $\Theta$ <br> Degrees | Ideal $\Theta$ Degrees | Nominal <br> $\Theta$ Degrees |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 17 | 17.98 | 34 | 33.04 | 75 | 74.00 | 160 | 159.14 | 245 | 244.63 |
| 1 | 1.09 | 18 | 18.96 | 35 | 34.00 | 80 | 79.16 | 165 | 164.00 | 250 | 249.14 |
| 2 | 2.19 | 19 | 19.92 | 36 | 35.00 | 85 | 84.53 | 170 | 169.16 | 255 | 254.00 |
| 3 | 3.29 | 20 | 20.86 | 37 | 36.04 | 90 | 90.00 | 175 | 174.33 | 260 | 259.16 |
| 4 | 4.38 | 21 | 21.79 | 38 | 37.11 | 95 | 95.47 | 180 | 180.00 | 265 | 264.53 |
| 5 | 5.47 | 22 | 22.71 | 39 | 38.21 | 100 | 100.84 | 185 | 185.47 | 270 | 270.00 |
| 6 | 6.56 | 23 | 23.61 | 40 | 39.32 | 105 | 106.00 | 190 | 190.84 | 275 | 275.47 |
| 7 | 7.64 | 24 | 24.50 | 41 | 40.45 | 110 | 110.86 | 195 | 196.00 | 280 | 280.84 |
| 8 | 8.72 | 25 | 25.37 | 42 | 41.59 | 115 | 115.37 | 200 | 200.86 | 285 | 286.00 |
| 9 | 9.78 | 26 | 26.23 | 43 | 42.73 | 120 | 119.56 | 205 | 205.37 | 290 | 290.86 |
| 10 | 10.84 | 27 | 27.07 | 44 | 43.88 | 125 | 124.00 | 210 | 209.56 | 295 | 295.37 |
| 11 | 11.90 | 28 | 27.79 | 45 | 45.00 | 130 | 129.32 | 215 | 214.00 | 300 | 299.21 |
| 12 | 12.94 | 29 | 28.73 | 50 | 50.68 | 135 | 135.00 | 220 | 219.32 | 305 | 303.02 |
| 13 | 13.97 | 30 | 29.56 | 55 | 56.00 | 140 | 140.68 | 225 | 225.00 |  |  |
| 14 | 14.99 | 31 | 30.39 | 60 | 60.44 | 145 | 146.00 | 230 | 230.58 |  |  |
| 15 | 16.00 | 32 | 31.24 | 65 | 64.63 | 150 | 150.44 | 235 | 236.00 |  |  |
| 16 | 17.00 | 33 | 32.12 | 70 | 69.14 | 155 | 154.63 | 240 | 240.44 |  |  |

Note: Temperature, voltage and nonlinearity not included.

## CIRCUIT DESCRIPTION and APPLICATION NOTES

The CS4121 is specifically designed for use with air-core meter movements. It includes an input comparator for sensing an input signal from an ignition pulse or speed sensor, a charge pump for frequency to voltage conversion, a bandgap voltage regulator for stable operation, and a function generator with sine and cosine amplifiers to differentially drive the meter coils.

From the partial schematic of Figure 7, the input signal is applied to the $\mathrm{FREQ}_{\text {IN }}$ lead, this is the input to a high impedance comparator with a typical positive input threshold of 2.0 V and typical hysteresis of 0.5 V . The output of the comparator, SQout, is applied to the charge pump input $\mathrm{CP}+$ through an external capacitor $\mathrm{C}_{\mathrm{CP}}$. When the input signal changes state, $\mathrm{C}_{\mathrm{CP}}$ is charged or discharged through R3 and R4. The charge accumulated on $\mathrm{C}_{\mathrm{CP}}$ is mirrored to C4 by the Norton Amplifier circuit comprising of Q1, Q2 and Q3. The charge pump output voltage, F/V ${ }_{\text {OUT }}$, ranges from 2.0 V to 6.3 V depending on the input signal frequency and the gain of the charge pump according to the formula:

```
\(\mathrm{F} / \mathrm{V}_{\text {OUT }}=2.0 \mathrm{~V}+2.0 \times \mathrm{FREQ} \times \mathrm{C}_{\mathrm{CP}} \times \mathrm{R}_{\mathrm{T}} \times\left(\mathrm{V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right)\)
```

$\mathrm{R}_{\mathrm{T}}$ is a potentiometer used to adjust the gain of the $\mathrm{F} / \mathrm{V}$ output stage and give the correct meter deflection. The F/V output voltage is applied to the function generator which generates the sine and cosine output voltages. The output voltage of the sine and cosine amplifiers are derived from the on-chip amplifier and function generator circuitry. The various trip points for the circuit (i.e., $0^{\circ}, 90^{\circ}, 180^{\circ}, 270^{\circ}$ ) are determined by an internal resistor divider and the bandgap voltage reference. The coils are differentially driven, allowing bidirectional current flow in the outputs, thus providing up to $305^{\circ}$ range of meter deflection. Driving the coils differentially offers faster response time, higher current capability, higher output voltage swings, and reduced external component count. The key advantage is a higher torque output for the pointer.

The output angle, $\Theta$, is equal to the $\mathrm{F} / \mathrm{V}$ gain multiplied by the function generator gain:

$$
\Theta=A_{F} / V \times A_{F G}
$$

where:

$$
\mathrm{AFG}=77^{\circ} / \mathrm{V}(\mathrm{typ})
$$

The relationship between input frequency and output angle is:

$$
\begin{aligned}
& \Theta=A_{F G} \times 2.0 \times \mathrm{FREQ} \times \mathrm{CCP} \times \mathrm{RT} \times\left(\mathrm{V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right) \\
& \Theta=970 \times \mathrm{FREQ} \times \mathrm{C}_{\mathrm{CP}} \times \mathrm{RT}
\end{aligned}
$$

The ripple voltage at the F/V converter's output is determined by the ratio of $\mathrm{C}_{\mathrm{CP}}$ and C 4 in the formula:

$$
\Delta \mathrm{V}=\frac{\mathrm{C}_{\mathrm{CP}}\left(\mathrm{~V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right)}{\mathrm{C} 4}
$$

Ripple voltage on the F/V output causes pointer or needle flutter especially at low input frequencies.

The response time of the F/V is determined by the time constant formed by $\mathrm{R}_{\mathrm{T}}$ and C 4 . Increasing the value of C 4 will reduce the ripple on the $\mathrm{F} / \mathrm{V}$ output but will also increase the response time. An increase in response time causes a very slow meter movement and may be unacceptable for many applications.

## Design Example

Maximum meter Deflection $=270^{\circ}$
Maximum Input Frequency $=350 \mathrm{~Hz}$
10. Select $R_{T}$ and $C_{C P}$

$$
\Theta=970 \times \mathrm{FREQ} \times \mathrm{C}_{\mathrm{CP}} \times \mathrm{RT}=270^{\circ}
$$

Let $\mathrm{C}_{\mathrm{T}}=0.0033 \mu \mathrm{~F}$, find $\mathrm{R}_{\mathrm{T}}$

$$
\begin{gathered}
\mathrm{RT}=\frac{270^{\circ}}{970 \times 350 \mathrm{~Hz} \times 0.0033 \mu \mathrm{~F}} \\
\mathrm{RT}=243 \mathrm{k} \Omega
\end{gathered}
$$

$\mathrm{R}_{\mathrm{T}}$ should be a $250 \mathrm{k} \Omega$ potentiometer to trim out any inaccuracies due to IC tolerances or meter movement pointer placement.

## 11. Select R3 and R4

Resistor R3 sets the output current from the voltage regulator. The maximum output current from the voltage regulator is 10 mA . R3 must ensure that the current does not exceed this limit.

Choose R3 $=3.3 \mathrm{k} \Omega$
The charge current for $\mathrm{C}_{\mathrm{CP}}$ is

$$
\frac{\mathrm{V}_{\mathrm{REG}}-0.7 \mathrm{~V}}{3.3 \mathrm{k} \Omega}=1.90 \mathrm{~mA}
$$

$\mathrm{C}_{\mathrm{CP}}$ must charge and discharge fully during each cycle of the input signal. Time for one cycle at maximum frequency is 2.85 ms . To ensure that $\mathrm{C}_{\mathrm{CP}}$ is charged, assume that the $(\mathrm{R} 3+\mathrm{R} 4) \mathrm{C}_{\mathrm{CP}}$ time constant is less than $10 \%$ of the minimum input period.

$$
\mathrm{T}=10 \% \times \frac{1}{350 \mathrm{~Hz}}=285 \mu \mathrm{~s}
$$

$$
\begin{aligned}
& \text { Choose } 4=1.0 \mathrm{k} \Omega \\
& \text { Discharge time: } \begin{aligned}
\mathrm{t}_{\mathrm{DCHG}} & =\mathrm{R} 3 \times \mathrm{C}_{\mathrm{CP}}=3.3 \mathrm{k} \Omega \times 0.0033 \mu \mathrm{~F} \\
& =10.9 \mu \mathrm{~s}
\end{aligned} \\
& \begin{aligned}
\text { Charge time: } \mathrm{t}_{\mathrm{CHG}} & =(\mathrm{R} 3+\mathrm{R} 4) \mathrm{C}_{\mathrm{CP}}=4.3 \mathrm{k} \Omega \times 0.0033 \mu \mathrm{~F} \\
& =14.2 \mu \mathrm{~s}
\end{aligned}
\end{aligned}
$$

## 12. Determine C4

C 4 is selected to satisfy both the maximum allowable ripple voltage and response time of the meter movement.

$$
\mathrm{C} 4=\frac{\mathrm{C}_{\mathrm{CP}}\left(\mathrm{~V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right)}{\Delta \mathrm{V}_{\mathrm{MAX}}}
$$

With $\mathrm{C} 4=0.47 \mu \mathrm{~F}$, the $\mathrm{F} / \mathrm{V}$ ripple voltage is 44 mV .


Figure 7. Partial Schematic of Input and Charge Pump


Figure 8. Timing Diagram of RREQ $_{\text {IN }}$ and $I_{C P}$


Notes:

1. For $58 \%$ Speed Input $\mathrm{T}_{\text {MAX }} \leq 5.0 / \mathrm{f}_{\mathrm{MAX}}$ where $\mathrm{T}_{\mathrm{MAX}}=\mathrm{C}_{\mathrm{CP}}(\mathrm{R} 3+\mathrm{R} 4)$ $f_{M A X}=$ maximum speed input frequency
2. The product of C 4 and $\mathrm{R}_{\mathrm{T}}$ have a direct effect on gain and therefore directly affect temperature compensation.
3. $\mathrm{C}_{\mathrm{CP}}$ Range; 20 pF to $0.2 \mu \mathrm{~F}$.
4. $\mathrm{R}_{\mathrm{T}}$ Range; $100 \mathrm{k} \Omega$ to $500 \mathrm{k} \Omega$.
5. The Ic must be protected from transients above 60 V and reverse battery conditions.
6. Additional filtering on $\mathrm{FREQ}_{I N}$ lead may be required.
7. Gauge coil connections to the IC must be kept as short as possible ( $\leq 3.0$ inch) for best pointer stability.

Figure 9. Speedometer or Tachometer Application


Notes:

1. The product of $C 4$ and $R_{T}$ have a direct effect on gain and therefore directly affect temperature compensation.
2. $\mathrm{C}_{\mathrm{CP}}$ Range; 20 pF to $0.2 \mu \mathrm{~F}$.
3. $R_{T}$ Range; $100 \mathrm{k} \Omega$ to $500 \mathrm{k} \Omega$.
4. The Ic must be protected from transients above 60 V and reverse battery conditions.
5. Additional filtering on $F_{R E Q}{ }_{I N}$ lead may be required.
6. Gauge coil connections to the IC must be kept as short as possible ( $\leq 3.0$ inch) for best pointer stability.

Figure 10. Speedometer With Odometer or Tachometer Application

PACKAGE THERMAL DATA

| Parameter |  | DIP-16 | SO-20L | Unit |
| :---: | :---: | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 15 | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\Theta \mathrm{JA}}$ | Typical | 50 | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS4122

## Triple Air-Core Gauge Driver with Serial Input Bus

The CS4122 converts digital data from a microprocessor to complementary DC outputs and drives air-core meter movements for vehicle instrument panels. It is optimized for one $360^{\circ}$ gauge and two $112^{\circ}$ gauges. The digital data controls the voltage applied to the quadrature coils of the meters with a $0.35^{\circ}$ resolution for the major $\left(360^{\circ}\right)$ gauge and $0.44^{\circ}$ resolution for the minor $\left(112^{\circ}\right)$ gauges. The accuracy is $\pm 0.75^{\circ}$ for the major and $\pm 1.00^{\circ}$ for the minors. The interface from the microcontroller is by a SPI compatible serial connection using up to a 2.0 MHz shift clock rate.

The digital code is shifted into the appropriate DAC and multiplexer. These two blocks provide a tangential conversion function to change the digital data into the appropriate DC coil voltage. The major gauge driver can position a pointer anywhere within a $360^{\circ}$ circle while the minor gauge drivers are limited to an arc of $112.2^{\circ}$.

The output buffers are capable of supplying up to 70 mA per coil and are protected against output short circuit conditions. A thermal protection circuit limits the junction temperature to approximately $160^{\circ} \mathrm{C}$.

A fault output lead goes low when any of the outputs are shorted or the device is in a thermal shutdown state. This ASIC is designed on POWERSENSE ${ }^{\text {TM }} 3.0$.

## Features

- Serial Input Bus
- 2.0 MHz Operating Frequency
- Independently Addressable Gauges
- Tangential Drive Algorithm
- 70 mA Drive Circuits
- $0.75^{\circ}$ Major Accuracy
- Power-On-Reset
- Protection Features
- Short Circuit
- Overtemperature
- Internally Fused Leads in SO-24L Package

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## PIN CONNECTIONS



ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS4122XDWF24 | SO-24L | 31 Units/Rail |
| CS4122XDWFR24 | SO-24L | 1000 Tape \& Reel |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{BB}} \\ & \mathrm{~V}_{\mathrm{CC}} \end{aligned}$ | $\begin{gathered} -1.0 \text { to } 16.5 \\ -1.0 \text { to } 6.0 \end{gathered}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Digital Inputs |  | -1.0 to 6.0 | V |
| Steady State Output Current |  | $\pm 100$ | mA |
| Forced Injection Current (Inputs and Supply) |  | $\pm 10$ | mA |
| Operating Junction Temperature ( $\mathrm{T}_{\mathrm{J}}$ ) |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range ( $\mathrm{T}_{\text {STG }}$ ) |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| $\Theta_{\mathrm{JA}}$ (Thermal Resistance Junction to Ambient) |  | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\Theta_{\mathrm{JC}}$ (Thermal Resistance Junction to Case) |  | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}, 7.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}} \leq 14 \mathrm{~V}, 4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 5.5 \mathrm{~V}\right.$;
unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

## Supply Voltages and Currents

| Analog Supply Current | $\begin{aligned} & V_{\mathrm{BB}}=14 \mathrm{~V} \text {, no coil loads, } \\ & \mathrm{R}_{\text {COS }} \mathrm{R}_{\text {SIN }}=\mathrm{R}_{\mathrm{L}(\mathrm{MIN})} \\ & \text { Major } @ 45^{\circ}\left(\text { code }=080_{16}\right), \\ & \text { Both Minors @ } 0^{\circ}\left(\text { codes }=00_{16}\right) \\ & \text { Major @ } 0^{\circ}\left(\text { code }=000_{16}\right) \text {, } \\ & \text { Both Minors @ } 56^{\circ}\left(\text { codes }=80_{16}\right) \end{aligned}$ |  | - | $\begin{gathered} 25 \\ 340 \\ 100 \end{gathered}$ | mA <br> mA <br> mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Logic Supply Current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \\ & \mathrm{SCLK}=2.0 \mathrm{MHz} \\ & \mathrm{SCLK}=0 \mathrm{MHz}, \mathrm{~V}_{\mathrm{BB}}=0 \mathrm{~V} \end{aligned}$ | - | - | $\begin{aligned} & 2.0 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

## Digital Inputs and Outputs

| Output High Voltage | $\mathrm{SO}=\mathrm{I}_{\mathrm{OUT}(\mathrm{HIGH})}=0.8 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{CC}}-0.8$ | - | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Low Voltage | $\mathrm{SO}=\mathrm{I}_{\mathrm{OUT}(\mathrm{LOW})}=1.5 \mathrm{~mA}$ |  |  |  |  |
|  | FAULT, $\mathrm{I}_{\mathrm{OUT}(\mathrm{LOW})}=2.8 \mathrm{~mA}$ | - | - | 0.4 | V |
| Output High Current | $\mathrm{FAULT}, \mathrm{V} \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{OUT}(\mathrm{HIGH})}=\mathrm{V}_{\mathrm{CC}}$ | - | - | 0.8 | V |
| Input High Voltage | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}$ | - | 25 | $\mu \mathrm{~A}$ |  |
| Input Low Voltage | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}$ | $-7 \times \mathrm{V}_{\mathrm{CC}}$ | - | - | V |
| Input High Current | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}, \mathrm{V}_{\mathrm{IN}}=0.7 \times \mathrm{V}_{\mathrm{CC}}$ | - | - | $0.3 \times \mathrm{V}_{\mathrm{CC}}$ | V |
| Input Low Current | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}, \mathrm{V}_{\mathrm{IN}}=0.3 \times \mathrm{V}_{\mathrm{CC}}$ | - | - | 1.0 | $\mu \mathrm{~A}$ |

Analog Outputs

| Output Function Accuracy | Major Accuracy <br> Minor Accuracy | - | - | $\begin{aligned} & \pm 0.75 \\ & \pm 1.00 \end{aligned}$ | $\begin{aligned} & \text { deg } \\ & \text { deg } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Shutdown Current, Source and Sink | $\begin{aligned} & \mathrm{V}_{\mathrm{BB}}=\operatorname{Max} \\ & \mathrm{V}_{\mathrm{BB}}=\operatorname{Min} \end{aligned}$ | $\begin{aligned} & 70 \\ & 43 \end{aligned}$ | - | - | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Major Coil Drive Output Voltage | - | - | $0.748 \times V_{B B}$ | - | V |
| Minor Coil Drive Output Voltage | - | - | $0.744 \times V_{B B}$ | - | V |
| $\mathrm{V}_{\mathrm{BB}} / 2$ | $\mathrm{I}_{\mathrm{DR}(\mathrm{VBB} / 2)}= \pm 50 \mathrm{~mA}$ | $\left(0.5 \times \mathrm{V}_{\mathrm{BB}}\right)-0.1$ | - | $\left(0.5 \times \mathrm{V}_{\mathrm{BB}}\right)+0.1$ | V |
| Minimum Load Resistance | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=105^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \end{aligned}$ | $\begin{aligned} & 229 \\ & 171 \\ & 150 \end{aligned}$ | - | - | $\Omega$ $\Omega$ $\Omega$ |
| SCLK Frequency | - | - | - | 2.0 | MHz |
| SCLK High Time | - | 175 | - | - | ns |
| SCLK Low Time | - | 175 | - | - | ns |
| SO Rise Time | 0.75 V to $\mathrm{V}_{\mathrm{CC}}-1.2 \mathrm{~V} ; \mathrm{C}_{\mathrm{L}}=90 \mathrm{pF}$ | - | - | 100 | ns |
| SO Fall Time | $\mathrm{V}_{\mathrm{CC}}-1.2 \mathrm{~V}$ to $0.75 \mathrm{~V} ; \mathrm{C}_{\mathrm{L}}=90 \mathrm{pF}$ | - | - | 100 | ns |
| SO Delay Time | $\mathrm{C}_{\mathrm{L}}=90 \mathrm{pF}$ | - | - | 150 | ns |
| SI Setup Time | - | 75 | - | - | ns |
| SI Hold Time | - | 75 | - | - | ns |
| CS Setup Time | - | 0 | - | - | ns |
| CS Hold Time | - | 75 | - | - | ns |

PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| SO-24L |  |  |
| 1 |  | PIN SYMBOL |

## APPLICATIONS INFORMATION

THEORY OF OPERATION
The CS4122 is for interfacing between a microcontroller or microprocessor and air-core meters commonly used in automotive vehicles for speedometers, tachometers and auxiliary gauges. These meters are built using 2 coils placed at $90^{\circ}$ orientation to each other. A magnetized disc floats in the middle of the coils and responds to the magnetic field generated by each coil. The disc has a shaft attached to it that protrudes out of the assembly. A pointer indicator is attached to this shaft and in conjunction with a separate printed scale displays the vehicle's speed, engine's speed or other information such as fuel quantity or battery voltage.

The disc (and pointer) respond to the vector sum of the voltages applied to the coils. Ideally, this relationship follows a sine/cosine equation. Since this is a transcendental and non-linear function, devices of this type use an approximation for this relationship. The CS4122 uses a tangential algorithm as shown in Figure 2 for the major $\left(360^{\circ}\right)$ gauge. Only one output varies in any $45^{\circ}$ range.

Note: The actual slopes are segmented but are shown here as straight lines for simplicity.




Figure 2. Major Gauge Outputs

## Quadrant I

$$
\theta=\operatorname{Tan}^{-1}\left[\frac{\left(\mathrm{~V}_{\mathrm{SIN}+}\right)-\left(\mathrm{V}_{\mathrm{SIN}-}\right)}{\left(\mathrm{V}_{\mathrm{COS}}+\right)-\left(\mathrm{V}_{\mathrm{COS}}-\right)}\right]
$$

For $\theta=0.176^{\circ}$ to $44.824^{\circ}$ :

$$
\mathrm{V}_{\mathrm{SIN}}=\operatorname{Tan} \theta \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

$$
V_{\mathrm{COS}}=0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

For $\theta=45.176^{\circ}$ to $89.824^{\circ}$ :
$\mathrm{V}_{\mathrm{SIN}}=0.748 \times \mathrm{V}_{\mathrm{BB}}$
$\mathrm{V}_{\mathrm{COS}}=\operatorname{Tan}\left(90^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}$

## Quadrant II

$$
\begin{aligned}
& \theta=180^{\circ}-\operatorname{Tan}^{-1}\left[\frac{\left(\mathrm{~V}_{\mathrm{SIN}+}\right)-\left(\mathrm{V}_{\mathrm{SIN}-}\right)}{\left(\mathrm{V}_{\mathrm{COS}+}\right)-\left(\mathrm{V}_{\mathrm{COS}}-\right)}\right] \\
& \text { For } \theta=90.176^{\circ} \text { to } 134.824^{\circ}: \\
& \quad \mathrm{V}_{\mathrm{SIN}}=0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \quad \mathrm{~V}_{\mathrm{COS}}=-\operatorname{Tan}\left(\theta-90^{\circ}\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

For $\theta=135.176^{\circ}$ to $179.824^{\circ}$ :

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{SIN}}=\operatorname{Tan}\left(180^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \mathrm{~V}_{\mathrm{COS}}=-0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

## Quadrant III

$$
\theta=180^{\circ}+\operatorname{Tan}^{-1}\left[\frac{(\mathrm{~V} \mathrm{SIN}+)-\left(\mathrm{V}_{\mathrm{SIN}-}\right)}{\left(\mathrm{V}_{\mathrm{COS}}+\right)-\left(\mathrm{V}_{\mathrm{COS}}-\right)}\right]
$$

For $\theta=180.176^{\circ}$ to $224.824^{\circ}$ :

$$
\mathrm{V}_{\mathrm{SIN}}=-\operatorname{Tan}\left(\theta-180^{\circ}\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

$$
V_{\mathrm{COS}}=-0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

For $\theta=225.176^{\circ}$ to $269.824^{\circ}$ :

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{SIN}}=-0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \mathrm{~V}_{\mathrm{COS}}=-\operatorname{Tan}\left(270^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

## Quadrant IV

$$
\theta=360^{\circ}-\operatorname{Tan}^{-1}\left[\frac{(\mathrm{~V} \mathrm{SIN}+)-\left(\mathrm{V}_{\mathrm{SIN}-}\right)}{\left(\mathrm{V}_{\mathrm{COS}+}\right)-\left(\mathrm{V}_{\mathrm{COS}}-\right)}\right]
$$

For $\theta=270.176^{\circ}$ to $314.824^{\circ}$ :

$$
\mathrm{V}_{\mathrm{SIN}}=-0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

$$
V_{\mathrm{COS}}=\operatorname{Tan}\left(\theta-270^{\circ}\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

For $\theta=315.176^{\circ}-359.824^{\circ}$ :

$$
\mathrm{V}_{\mathrm{SIN}}=-\operatorname{Tan}\left(360^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

$$
V_{\mathrm{COS}}=0.748 \times \mathrm{V}_{\mathrm{BB}}
$$



Figure 3. Major Gauge Response

The minor gauge coil outputs differ in that only one of the coils in each movement is driven by the IC. The other is driven directly by the analog supply voltage, specifically one-half of this voltage. The common output assures that this is true. By varying the voltage across the other coil to a greater voltage, the pointer can be deflected more than $45^{\circ}$ to each side of the externally driven coil. This relationship is shown in Figure 4.

Note: There are actually 8 segments, but only 3 are shown here for simplicity.


Figure 4. Minor Gauge Outputs

## Quadrant I, II

$$
\begin{aligned}
& \theta=56.1^{\circ}-\operatorname{Tan}^{-1}\left[\frac{\left(\mathrm{~V}_{\mathrm{C}+}\right)-\left(\mathrm{V}_{\mathrm{C}-}\right)}{\mathrm{V}_{\mathrm{BB}}-\mathrm{V}_{(\mathrm{VBB} / 2)}}\right] \\
& \mathrm{V}_{\mathrm{COIL}}=\mathrm{V}_{(\mathrm{VBB} / 2)} \times \operatorname{Tan}\left(56.1^{\circ}-\theta\right)
\end{aligned}
$$



Figure 5. Minor Gauge Outputs
To drive a gauge's pointer to a particular angle, the microcontroller sends a 12 bit digital word to the CS4122. These 12 bits are divided as shown in Figure 6. However, from a software programmer's viewpoint, a $360^{\circ}$ circle is divided into 1024 equal parts of $.35^{\circ}$ each and a $112.2^{\circ}$ arc is divided into 256 parts of $.44^{\circ}$ each. Table 1 shows the data associated with the $45^{\circ}$ divisions of the $360^{\circ}$ driver. Table 2 shows the data for the center and end points of the $112.2^{\circ}$ drivers. Setting the address to " 11 " disables all outputs.


| Minor | D11 D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\left\|\begin{array}{c} \text { Gauge } \\ \text { Address } \\ =\text { "01" } \end{array}\right\|$ |  |  |  |  | $\begin{aligned} & \text { hiev } \\ & \text { Co } \end{aligned}$ | an | $\begin{aligned} & 44^{\circ} r \\ & -255 \end{aligned}$ | $\begin{aligned} & -112 \\ & \text { esol } \\ & j_{10} \end{aligned}$ |  |  |


| Minor | D11 D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \#2 | \|cc|c $\begin{gathered}\text { Gauge } \\ \text { Address } \\ =\text { "10" }\end{gathered}$ | Set to "00" |  |  | Deflection angle 0-112.2 ${ }^{\circ}$, to achieve a $0.44^{\circ}$ resolution Code $0-255_{10}$ |  |  |  |  |  |  |



Figure 6. Definition of Serial Word

Table 1. Nominal Output for Major Gauge ( $\mathrm{V}_{\mathrm{BB}}=14 \mathrm{~V}$ )

| Input Code <br> (Decimal) | Ideal <br> Degrees | Nominal <br> Degrees | $\mathbf{V}_{\text {SIN }}$ <br> (V) | $\mathbf{V}_{\text {cos }}$ <br> (V) |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0.176 | 0.032 | 10.472 |
| 128 | 45 | 45.176 | 10.472 | 10.412 |
| 256 | 90 | 90.176 | 10.472 | -0.032 |
| 384 | 135 | 135.176 | 10.412 | -10.472 |
| 512 | 180 | 180.176 | -0.032 | -10.472 |
| 640 | 225 | 225.176 | -10.472 | -10.412 |
| 768 | 270 | 270.176 | -10.472 | 0.032 |
| 896 | 315 | 315.176 | -10.476 | 10.412 |
| 1023 | 359.65 | 359.826 | -0.032 | 10.472 |

Table 2. Nominal Output for Minor Gauges ( $\mathrm{V}_{\mathrm{BB}}=14 \mathrm{~V}$ )

| Input Code <br> (Decimal) | Scale <br> Degrees | Degrees <br> from Center | $\mathbf{V}_{\text {coIL }}$ |
| :---: | :---: | :---: | :---: |
| 0 | 0 | -56.1 | 10.417 |
| 127 | 55.88 | -0.22 | 0.027 |
| 128 | 56.32 | 0.22 | -0.027 |
| 255 | 112.2 | 56.1 | -10.417 |

The 12 bits are shifted into the device's shift register MSB first using a SPI compatible scheme. This method is shown in Figures 6 and 7. The first 2 bits select the output driver for which the data is intended. The CS must be high and remain high for SCLK to be enabled. Data on SI is shifted in on the
rising edge of the synchronous clock signal. Data in the shift register is shifted to SO on the falling edge of SCLK. This arrangement allows the cascading of devices. SO is always enabled. Data shifts through without affecting the outputs until CS is brought low. At this time, the internal DAC is updated and the outputs change accordingly.


Figure 7. Serial Data Timing Diagram
The DAC for the major gauge driver outputs 128 discrete levels selected by bits D6 - D0. These bits are XOR'd with D7 to invert them when choosing the 2nd half of each quadrant (each odd octant). This reduces the number of
resistors and switches required. The MUX chooses which signals to send to the output amplifiers based upon D9 - D7. There are three choices for each amplifier: high, low or the DAC output.

The DAC's for the minor gauge drivers similarly output 128 discrete levels selected by bits D6 - D0. These bits are also XOR'd with D7 to invert them when choosing the 2nd half of the output range. The MUX chooses which signals to send to the output amplifiers based upon D7. There are two choices for each amplifier; high or the DAC output. Bits D8 and D9 are not used, but should be set to " 00 " to ensure that the minor gauge outputs are enabled.

The output buffers are unity gain amplifiers. Each of the 8 outputs is designed to swing close to the supply rails to maximize the voltage across the coils to produce maximum torque. Additionally, this lowers the power dissipation. The current for each output is also monitored. If any of the major gauge outputs exceed the maximum value, all of the major outputs are disabled. If any of the minor gauge outputs exceed the maximum value, all of the minor outputs are disabled. The falling edge of the CS re-enables the outputs with the fault condition but they remain on only if the overcurrent situation has been eliminated.


Figure 8. Application Diagram

PACKAGE THERMAL DATA

| Parameter |  | SO-24L | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8190

## Precision Air-Core <br> Tach/Speedo Driver with Return to Zero

The CS8190 is specifically designed for use with air-core meter movements. The IC provides all the functions necessary for an analog tachometer or speedometer. The CS8190 takes a speed sensor input and generates sine and cosine related output signals to differentially drive an air-core meter.

Many enhancements have been added over industry standard tachometer drivers such as the CS289 or LM1819. The output utilizes differential drivers which eliminates the need for a zener reference and offers more torque. The device withstands 60 V transients which decreases the protection circuitry required. The device is also more precise than existing devices allowing for fewer trims and for use in a speedometer.

## Features

- Direct Sensor Input
- High Output Torque
- Low Pointer Flutter
- High Input Impedance
- Overvoltage Protection
- Return to Zero
- Internally Fused Leads in DIP-16 and SO-20L Packages

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PIN CONNECTIONS AND
MARKING DIAGRAM

$\begin{array}{ll}\text { A } & =\text { Assembly Location } \\ \text { WL, L } & =\text { Wafer Lot } \\ \text { YY, Y } & =\text { Year } \\ \text { WW, W } & =\text { Work Week }\end{array}$
ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8190ENF16 | DIP-16 | 25 Units/Rail |
| CS8190EDWF20 | SO-20L | 37 Units/Rail |
| CS8190EDWFR20 | SO-20L | 1000 Tape \& Reee |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {CC }}$ | < 100 ms Pulse Transient Continuous | $\begin{aligned} & 60 \\ & 24 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Operating Temperature |  | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature |  | -40 to +165 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| ESD (Human Body Model) |  | 4.0 | kV |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow: (SMD styles only) (Note 2) | 260 peak 230 peak | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\mathrm{C}} \end{aligned}$ |

1. 10 seconds maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, 8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 15 \mathrm{~V}\right.$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage Section |  |  |  |  |  |
| ICC Supply Current | $\mathrm{V}_{\mathrm{CC}}=16 \mathrm{~V},-40^{\circ} \mathrm{C}$, No Load | - | 50 | 125 | mA |
| $\mathrm{V}_{\text {CC }}$ Normal Operation Range | - | 8.5 | 13.1 | 16 | V |

Input Comparator Section

| Positive Input Threshold | - | 1.0 | 2.0 | 3.0 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Hysteresis | - | 200 | 500 | - | mV |
| Input Bias Current (Note 3) | $0 \mathrm{~V} \leq \mathrm{V}_{\text {IN }} \leq 8.0 \mathrm{~V}$ | - | -10 | -80 | $\mu \mathrm{A}$ |
| Input Frequency Range | - | 0 | - | 20 | kHz |
| Input Voltage Range | in series with $1.0 \mathrm{k} \Omega$ | -1.0 | - | $\mathrm{V}_{\mathrm{CC}}$ | V |
| Output $\mathrm{V}_{\text {SAT }}$ | $\mathrm{I}_{\mathrm{CC}}=10 \mathrm{~mA}$ | - | 0.15 | 0.40 | V |
| Output Leakage | $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ | - | - | 10 | $\mu \mathrm{A}$ |
| Low V ${ }_{\text {CC }}$ Disable Threshold | - | 7.0 | 8.0 | 8.5 | V |
| Logic 0 Input Voltage | - | 1.0 | - | - | V |

Voltage Regulator Section

| Output Voltage | - | 6.25 | 7.00 | 7.50 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Load Current | - | - | - | 10 | mA |
| Output Load Regulation | 0 to 10 mA | - | 10 | 50 | mV |
| Output Line Regulation | $8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | - | 20 | 150 | mV |
| Power Supply Rejection | $\mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}, 1.0 \mathrm{~V}_{\mathrm{P} / \mathrm{P}} 1.0 \mathrm{kHz}$ | 34 | 46 | - | dB |

Charge Pump Section

| Inverting Input Voltage | - | 1.5 | 2.0 | 2.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | - | - | 40 | 150 | nA |
| $V_{\text {BIAS }}$ Input Voltage | - | 1.5 | 2.0 | 2.5 | V |
| Non Invert. Input Voltage | $\mathrm{I}_{\mathrm{IN}}=1.0 \mathrm{~mA}$ | - | 0.7 | 1.1 | V |
| Linearity (Note 4) | @ 0, 87.5, 175, 262.5, + 350 Hz | -0.10 | 0.28 | +0.70 | \% |
| F/Vout Gain | $\begin{gathered} @ 350 \mathrm{~Hz}, \mathrm{C}_{\mathrm{CP}}=0.0033 \mu \mathrm{~F}, \\ \mathrm{R}_{\mathrm{T}}=243 \mathrm{k} \Omega \end{gathered}$ | 7.0 | 10 | 13 | $\mathrm{mV} / \mathrm{Hz}$ |
| Norton Gain, Positive | $\mathrm{I}_{\mathrm{N}}=15 \mu \mathrm{~A}$ | 0.9 | 1.0 | 1.1 | 1/1 |
| Norton Gain, Negative | $\mathrm{I}_{\mathrm{N}}=15 \mu \mathrm{~A}$ | 0.9 | 1.0 | 1.1 | 1/1 |

Function Generator Section: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}$ unless otherwise noted.

| Return to Zero Threshold | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 5.2 | 6.0 | 7.0 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Differential Drive Voltage | $8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ <br> $\left(\mathrm{~V}_{\text {COS }+}-\mathrm{V}_{\text {COS- }}\right)$ | 5.5 | 6.5 | 7.5 | V |
| Differential Drive Voltage | $8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ <br> $\left(\mathrm{~V}_{\text {SIN+ }}-\mathrm{V}_{\text {SIN- }}\right)$ | 5.5 | 6.5 | 7.5 | V |
| Differential Drive Voltage <br> $\left(\mathrm{V}_{\text {COS }+}-\mathrm{V}_{\text {COS- }}\right)$ | $8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ <br> $\Theta=180^{\circ}$ | -7.5 | -6.5 | -5.5 | V |
| Differential Drive Voltage <br> $\left(\mathrm{V}_{\text {SIN+ }}-\mathrm{V}_{\text {SIN- }}\right)$ | $8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ <br> $\Theta=270^{\circ}$ | -7.5 | -6.5 | -5.5 | V |

3. Input is clamped by an internal 12 V Zener.
4. Applies to $\%$ of full scale $\left(270^{\circ}\right)$.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, 8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 15 \mathrm{~V}\right.$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Function Generator Section: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}$ unless otherwise noted. (continued) |  |  |  |  |  |
| Differential Drive Current | $8.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | - | 33 | 42 | mA |
| Zero Hertz Output Angle | - | -1.5 | 0 | 1.5 | deg |
| Function Generator Error (Note 5) Reference Figures 2, 3, 4, 5 | $\begin{aligned} & V_{C C}=13.1 \mathrm{~V} \\ & \Theta=0^{\circ} \text { to } 305^{\circ} \end{aligned}$ | -2.0 | 0 | +2.0 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | -2.5 | 0 | +2.5 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 11 \mathrm{~V}$ | -1.0 | 0 | +1.0 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 9.0 \mathrm{~V}$ | -3.0 | 0 | +3.0 | deg |
| Function Generator Error | $25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 80^{\circ} \mathrm{C}$ | -3.0 | 0 | +3.0 | deg |
| Function Generator Error | $25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}$ | -5.5 | 0 | +5.5 | deg |
| Function Generator Error | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C}$ | -3.0 | 0 | +3.0 | deg |
| Function Generator Gain | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \Theta$ vs $\mathrm{F} / \mathrm{V}_{\text {OUT }}$, | 60 | 77 | 95 | ${ }^{\circ} \mathrm{V}$ |

5. Deviation from nominal per Table 1 after calibration at $0^{\circ}$ and $270^{\circ}$.

## PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| DIP-16 | SO-20L |  |  |
| 1 | 1 | CP+ | Positive input to charge pump. |
| 2 | 2 | SQout | Buffered square wave output signal. |
| 3 | 3 | FREQ ${ }_{\text {IN }}$ | Speed or RPM input signal. |
| 4, 5, 12, 13 | 4-7, 14-17 | GND | Ground Connections. |
| 6 | 8 | COS+ | Positive cosine output signal. |
| 7 | 9 | cos- | Negative cosine output signal. |
| 8 | 10 | $\mathrm{V}_{\mathrm{CC}}$ | Ignition or battery supply voltage. |
| 9 | 11 | BIAS | Test point or zero adjustment. |
| 10 | 12 | SIN- | Negative sine output signal. |
| 11 | 13 | SIN+ | Positive sine output signal. |
| 14 | 18 | $\mathrm{V}_{\text {REG }}$ | Voltage regulator output. |
| 15 | 19 | F/VOUT | Output voltage proportional to input signal frequency. |
| 16 | 20 | CP- | Negative input to charge pump. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Function Generator Output Voltage vs. Degrees of Deflection


Figure 3. Charge Pump Output Voltage vs. Output Angle


Figure 5. Nominal Output Deviation


Figure 6. Nominal Angle vs. Ideal Angle (After Calibrating at $\mathbf{1 8 0}^{\mathbf{\circ}}$ )

Table 1. Function Generator Output Nominal Angle vs. Ideal Angle (After Calibrating at $\mathbf{2 7 0}^{\circ}$ )

| Ideal $\Theta$ Degrees | Nominal $\Theta$ Degrees | Ideal $\Theta$ Degrees | Nominal $\Theta$ Degrees | Ideal $\Theta$ Degrees | Nominal $\Theta$ Degrees | Ideal $\Theta$ Degrees | Nominal <br> $\Theta$ <br> Degrees | Ideal $\Theta$ Degrees | Nominal $\Theta$ Degrees | Ideal $\Theta$ Degrees | Nominal $\Theta$ <br> Degrees |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 17 | 17.98 | 34 | 33.04 | 75 | 74.00 | 160 | 159.14 | 245 | 244.63 |
| 1 | 1.09 | 18 | 18.96 | 35 | 34.00 | 80 | 79.16 | 165 | 164.00 | 250 | 249.14 |
| 2 | 2.19 | 19 | 19.92 | 36 | 35.00 | 85 | 84.53 | 170 | 169.16 | 255 | 254.00 |
| 3 | 3.29 | 20 | 20.86 | 37 | 36.04 | 90 | 90.00 | 175 | 174.33 | 260 | 259.16 |
| 4 | 4.38 | 21 | 21.79 | 38 | 37.11 | 95 | 95.47 | 180 | 180.00 | 265 | 264.53 |
| 5 | 5.47 | 22 | 22.71 | 39 | 38.21 | 100 | 100.84 | 185 | 185.47 | 270 | 270.00 |
| 6 | 6.56 | 23 | 23.61 | 40 | 39.32 | 105 | 106.00 | 190 | 190.84 | 275 | 275.47 |
| 7 | 7.64 | 24 | 24.50 | 41 | 40.45 | 110 | 110.86 | 195 | 196.00 | 280 | 280.84 |
| 8 | 8.72 | 25 | 25.37 | 42 | 41.59 | 115 | 115.37 | 200 | 200.86 | 285 | 286.00 |
| 9 | 9.78 | 26 | 26.23 | 43 | 42.73 | 120 | 119.56 | 205 | 205.37 | 290 | 290.86 |
| 10 | 10.84 | 27 | 27.07 | 44 | 43.88 | 125 | 124.00 | 210 | 209.56 | 295 | 295.37 |
| 11 | 11.90 | 28 | 27.79 | 45 | 45.00 | 130 | 129.32 | 215 | 214.00 | 300 | 299.21 |
| 12 | 12.94 | 29 | 28.73 | 50 | 50.68 | 135 | 135.00 | 220 | 219.32 | 305 | 303.02 |
| 13 | 13.97 | 30 | 29.56 | 55 | 56.00 | 140 | 140.68 | 225 | 225.00 |  |  |
| 14 | 14.99 | 31 | 30.39 | 60 | 60.44 | 145 | 146.00 | 230 | 230.58 |  |  |
| 15 | 16.00 | 32 | 31.24 | 65 | 64.63 | 150 | 150.44 | 235 | 236.00 |  |  |
| 16 | 17.00 | 33 | 32.12 | 70 | 69.14 | 155 | 154.63 | 240 | 240.44 |  |  |

Note: Temperature, voltage and nonlinearity not included.

## CIRCUIT DESCRIPTION and APPLICATION NOTES

The CS8190 is specifically designed for use with air-core meter movements. It includes an input comparator for sensing an input signal from an ignition pulse or speed sensor, a charge pump for frequency to voltage conversion, a bandgap voltage regulator for stable operation, and a function generator with sine and cosine amplifiers to differentially drive the meter coils.

From the partial schematic of Figure 7, the input signal is applied to the $\mathrm{FREQ}_{\text {IN }}$ lead, this is the input to a high impedance comparator with a typical positive input threshold of 2.0 V and typical hysteresis of 0.5 V . The output of the comparator, SQout, is applied to the charge pump input CP+ through an external capacitor $\mathrm{C}_{\mathrm{CP}}$. When the input signal changes state, $\mathrm{C}_{\mathrm{CP}}$ is charged or discharged through R3 and R4. The charge accumulated on $\mathrm{C}_{\mathrm{CP}}$ is mirrored to C4 by the Norton Amplifier circuit comprising of Q1, Q2 and Q3. The charge pump output voltage, F/V OUT, ranges from 2.0 V to 6.3 V depending on the input signal frequency and the gain of the charge pump according to the formula:

$$
\mathrm{F} / \mathrm{VOUT}_{\mathrm{O}}=2.0 \mathrm{~V}+2.0 \times \mathrm{FREQ} \times \mathrm{C} C P \times \mathrm{RT} \times(\mathrm{VREG}-0.7 \mathrm{~V})
$$

$\mathrm{R}_{\mathrm{T}}$ is a potentiometer used to adjust the gain of the $\mathrm{F} / \mathrm{V}$ output stage and give the correct meter deflection. The F/V output voltage is applied to the function generator which generates the sine and cosine output voltages. The output voltage of the sine and cosine amplifiers are derived from the
on-chip amplifier and function generator circuitry. The various trip points for the circuit (i.e., $0^{\circ}, 90^{\circ}, 180^{\circ}, 270^{\circ}$ ) are determined by an internal resistor divider and the bandgap voltage reference. The coils are differentially driven, allowing bidirectional current flow in the outputs, thus providing up to $305^{\circ}$ range of meter deflection. Driving the coils differentially offers faster response time, higher current capability, higher output voltage swings, and reduced external component count. The key advantage is a higher torque output for the pointer.

The output angle, $\Theta$, is equal to the $\mathrm{F} / \mathrm{V}$ gain multiplied by the function generator gain:

$$
\Theta=A_{F} / V \times A_{F G}
$$

where:

$$
\mathrm{AFG}=77^{\circ} / \mathrm{V}(\mathrm{typ})
$$

The relationship between input frequency and output angle is:

$$
\begin{aligned}
& \Theta=A_{F G} \times 2.0 \times \mathrm{FREQ} \times \mathrm{C}_{\mathrm{CP}} \times \mathrm{RT} \times\left(\mathrm{V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right) \\
& \quad \text { or, } \\
& \Theta=970 \times \mathrm{FREQ} \times \mathrm{C}_{\mathrm{CP}} \times \mathrm{RT}
\end{aligned}
$$

The ripple voltage at the $\mathrm{F} / \mathrm{V}$ converter's output is determined by the ratio of $\mathrm{C}_{\mathrm{CP}}$ and C 4 in the formula:

$$
\Delta \mathrm{V}=\frac{\mathrm{C} \mathrm{CP}\left(\mathrm{~V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right)}{\mathrm{C} 4}
$$



Figure 7. Partial Schematic of Input and Charge Pump


Figure 8. Timing Diagram of FREQ $_{\text {IN }}$ and $\mathrm{I}_{\mathrm{CP}}$

Ripple voltage on the F/V output causes pointer or needle flutter especially at low input frequencies.

The response time of the F/V is determined by the time constant formed by RT and C4. Increasing the value of C4 will reduce the ripple on the $\mathrm{F} / \mathrm{V}$ output but will also increase the response time. An increase in response time causes a very slow meter movement and may be unacceptable for many applications.

The CS8190 has an undervoltage detect circuit that disables the input comparator when $\mathrm{V}_{\mathrm{CC}}$ falls below 8.0 V (typical). With no input signal the F/V output voltage decreases and the needle moves towards zero. A second undervoltage detect circuit at 6.0 V (typical) causes the function generator to
generate a differential SIN drive voltage of zero volts and the differential COS drive voltage to go as high as possible. This combination of voltages (Figure 2) across the meter coil moves the needle to the $0^{\circ}$ position. Connecting a large capacitor(> $2000 \mu \mathrm{~F}$ ) to the $\mathrm{V}_{\mathrm{CC}}$ lead ( C 2 in Figure 9) increases the time between these undervoltage points since the capacitor discharges slowly and ensures that the needle moves towards $0^{\circ}$ as opposed to $360^{\circ}$. The exact value of the capacitor depends on the response time of the system, the maximum meter deflection and the current consumption of the circuit. It should be selected by breadboarding the design in the lab.


Figure 9. Speedometer or Tachometer Application

## Design Example

Maximum meter Deflection $=270^{\circ}$
Maximum Input Frequency $=350 \mathrm{~Hz}$

1. Select $\mathbf{R}_{\mathbf{T}}$ and $\mathbf{C}_{\mathbf{C P}}$

$$
\Theta=970 \times \mathrm{FREQ} \times \mathrm{C}_{\mathrm{CP}} \times \mathrm{R}_{\mathrm{T}}=270^{\circ}
$$

Let $\mathrm{C}_{\mathrm{CP}}=0.0033 \mu \mathrm{~F}$, find $\mathrm{R}_{\mathrm{T}}$

$$
\begin{gathered}
\mathrm{R} \mathrm{~T}=\frac{270^{\circ}}{970 \times 350 \mathrm{~Hz} \times 0.0033 \mu \mathrm{~F}} \\
\mathrm{RT}=243 \mathrm{k} \Omega
\end{gathered}
$$

RT should be a $250 \mathrm{k} \Omega$ potentiometer to trim out any inaccuracies due to IC tolerances or meter movement pointer placement.

## 2. Select R3 and R4

Resistor R3 sets the output current from the voltage regulator. The maximum output current from the voltage regulator is 10 mA . R3 must ensure that the current does not exceed this limit.

Choose R3 $=3.3 \mathrm{k} \Omega$
The charge current for $\mathrm{C}_{\mathrm{CP}}$ is

$$
\frac{\mathrm{V}_{\mathrm{REG}}-0.7 \mathrm{~V}}{3.3 \mathrm{k} \Omega}=1.90 \mathrm{~mA}
$$

$\mathrm{C}_{\mathrm{CP}}$ must charge and discharge fully during each cycle of the input signal. Time for one cycle at maximum frequency is 2.85 ms . To ensure that $\mathrm{C}_{\mathrm{CP}}$ is charged, assume that the
$(\mathrm{R} 3+\mathrm{R} 4) \mathrm{C}_{\mathrm{CP}}$ time constant is less than $10 \%$ of the minimum input period.

$$
\mathrm{T}=10 \% \times \frac{1}{350 \mathrm{~Hz}}=285 \mu \mathrm{~s}
$$

Choose R4 $=1.0 \mathrm{k} \Omega$.
Discharge time: ${ }_{\mathrm{DCHG}}=\mathrm{R} 3 \times \mathrm{C}_{\mathrm{CP}}=3.3 \mathrm{k} \Omega \times 0.0033 \mu \mathrm{~F}$

$$
=10.9 \mu \mathrm{~s}
$$

Charge time: $\mathrm{t}_{\mathrm{CHG}}=(\mathrm{R} 3+\mathrm{R} 4) \mathrm{C}_{\mathrm{CP}}=4.3 \mathrm{k} \Omega \times 0.0033 \mu \mathrm{~F}$

$$
=14.2 \mu \mathrm{~s}
$$

## 3. Determine C4

C 4 is selected to satisfy both the maximum allowable ripple voltage and response time of the meter movement.

$$
\mathrm{C} 4=\frac{\mathrm{C}_{\mathrm{CP}}(\mathrm{VREG}-0.7 \mathrm{~V})}{\Delta \mathrm{V}_{\mathrm{MAX}}}
$$

With $\mathrm{C} 4=0.47 \mu \mathrm{~F}$, the $\mathrm{F} / \mathrm{V}$ ripple voltage is 44 mV .
The last component to be selected is the return to zero capacitor C 2 . This is selected by increasing the input signal frequency to its maximum so the pointer is at its maximum deflection, then removing the power from the circuit. C2 should be large enough to ensure that the pointer always returns to the $0^{\circ}$ position rather than $360^{\circ}$ under all operating conditions.

Figure 10 shows how the CS8190 and the CS8441 are used to produce a Speedometer and Odometer circuit.


Notes:

1. $\mathrm{C} 2=10 \mu \mathrm{~F}$ with CS8441 application.
2. The product of C 4 and $\mathrm{R}_{\mathrm{T}}$ have a direct effect on gain and therefore directly affect temperature compensation.
3. C 4 Range; 20 pF to $0.2 \mu \mathrm{~F}$.
4. R4 Range; $100 \mathrm{k} \Omega$ to $500 \mathrm{k} \Omega$.
5. The IC must be protected from transients above 60 V and reverse battery conditions.
6. Additional filtering on the $\mathrm{FREQ}_{I \mathrm{~N}}$ lead may be required.
7. Gauge coil connections to the IC must be kept as short as possible ( $\leq 3.0$ inch) for best pointer stability.

Figure 10. Speedometer With Odometer or Tachometer Application

In some cases a designer may wish to use the CS8190 only as a driver for an air-core meter having performed the F/V conversion elsewhere in the circuit.

Figure 11 shows how to drive the CS8190 with a DC voltage ranging from 2.0 V to 6.0 V . This is accomplished by forcing a voltage on the $\mathrm{F} / \mathrm{V}_{\text {OUT }}$ lead. The alternative scheme shown in Figure 12 uses an external op amp as a buffer and operates over an input voltage range of 0 V to 4.0 V .


Figures 11 and 12 are not temperature compensated.


Figure 12. Driving the CS8190 from an External DC Voltage Using an Op Amp Buffer

Figure 11. Driving the CS8190 from an External DC Voltage

PACKAGE THERMAL DATA

| Parameter |  | DIP-16 | SO-20L | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $R_{\text {®JC }}$ | Typical | 15 | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS8191

## Precision Air-Core <br> Tach/Speedo Driver with Short Circuit Protection

The CS8191 is specifically designed for use with 4 quadrant air-core meter movements. The IC includes an input comparator for sensing input frequency such as vehicle speed or engine RPM, a charge pump for frequency to voltage conversion, a bandgap reference for stable operation and a function generator with sine and cosine amplifiers that differentially drive the meter coils.

The CS8191 has a higher torque output and better output signal symmetry than other competitive parts (CS289, and LM1819). It is protected against short circuit and overvoltage ( 60 V ) fault conditions. Enhanced circuitry permits functional operation down to 8.0 V .

## Features

- Direct Sensor Input
- High Output Torque
- Wide Output Voltage Range
- High Impedance Inputs
- Accurate Down to $10 \mathrm{~V}_{\mathrm{CC}}$
- Fault Protection
- Overvoltage
- Short Circuit
- Low Voltage Operation
- Internally Fused Leads in DIP-16 and SO-20L Packages

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


PIN CONNECTIONS AND
MARKING DIAGRAM


$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS8191XNF16 | DIP-16 | 25 Units/Rail |
| CS8191XDWF20 | SO-20L | 37 Units/Rail |
| CS8191XDWFR20 | SO-20L | 1000 Tape \& Reel |



Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage, $\mathrm{V}_{\text {CC }}$ | < 100 ms Pulse Transient Continuous | $\begin{aligned} & 60 \\ & 24 \end{aligned}$ | $\begin{aligned} & \text { V } \\ & \text { V } \end{aligned}$ |
| Operating Temperature Range |  | -40 to +105 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature Range |  | -40 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -55 to +165 | ${ }^{\circ} \mathrm{C}$ |
| Elecrostatic Discharge (Human Body Model) |  | 4.0 | kV |
| Lead Temperature Soldering: | Wave Solder (through hole styles only) (Note 1) Reflow: (SMD styles only) (Note 2) | 260 peak 230 peak | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |

1. 10 seconds maximum.
2. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}, 8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}\right.$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltage Section |  |  |  |  |  |
| ICC Supply Current | $\mathrm{V}_{\mathrm{CC}}=16 \mathrm{~V},-40^{\circ} \mathrm{C}$, No Load | - | 70 | 125 | mA |
| $\mathrm{V}_{\text {CC }}$ Normal Operation Range | - | 8.0 | 13.1 | 16 | V |

Input Comparator Section

| Positive Input Threshold | - | 2.4 | 2.7 | 3.0 | V |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Negative Input Threshold | - | 2.0 | 2.3 | - | V |  |
| Input Hysteresis | - | 200 | 400 | 1000 | mV |  |
| Input Bias Current (Note 3) | $0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{IN}} \leq 8.0 \mathrm{~V}$ | - | -2.0 | $\pm 10$ | $\mu \mathrm{~A}$ |  |
| Input Frequency Range |  | - | 0 | - | 20 | kHz |
| Input Voltage Range | in series with $1.0 \mathrm{k} \Omega$ | -1.0 | - | $\mathrm{V}_{\mathrm{CC}}$ | V |  |
| Output $\mathrm{V}_{\text {SAT }}$ | I CC $=10 \mathrm{~mA}$ | - | 0.15 | 0.40 | V |  |
| Output Leakage | $\mathrm{V}_{\mathrm{CC}}=7.0 \mathrm{~V}$ | - | - | 10 | $\mu \mathrm{~A}$ |  |
| Logic 0 Input Voltage |  | 2.0 | - | - | V |  |

Voltage Regulator Section

| Output Voltage | - | 6.50 | 7.00 | 7.50 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Load Current | - | - | - | 10 | mA |
| Output Load Regulation | 0 to 10 mA | - | 10 | 50 | mV |
| Output Line Regulation | $8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | - | 20 | 150 | mV |
| Power Supply Rejection | $\mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}, 1.0 \mathrm{~V}_{\mathrm{P} / \mathrm{P}} 1.0 \mathrm{kHz}$ | 34 | 46 | - | dB |

Charge Pump Section

| Inverting Input Voltage | - | 1.5 | 2.0 | 2.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current | - | - | 40 | 150 | nA |
| $V_{\text {BIAS }}$ Input Voltage | - | 1.5 | 2.0 | 2.5 | V |
| Non Invert. Input Voltage | $\mathrm{I}_{\mathrm{IN}}=1.0 \mathrm{~mA}$ | - | 0.7 | 1.1 | V |
| Linearity (Note 4) | @ 0, 87.5, 175, 262.5, + 350 Hz | -0.10 | 0.28 | +0.70 | \% |
| F/Vout Gain | $\begin{gathered} @ 350 \mathrm{~Hz}, \mathrm{C}_{\mathrm{CP}}=0.0033 \mu \mathrm{~F}, \\ \mathrm{R}_{\mathrm{T}}=243 \mathrm{k} \Omega \end{gathered}$ | 7.0 | 10 | 13 | $\mathrm{mV} / \mathrm{Hz}$ |
| Norton Gain, Positive | $\mathrm{I}_{\mathrm{N}}=15 \mu \mathrm{~A}$ | 0.9 | 1.0 | 1.1 | 1/1 |
| Norton Gain, Negative | $\mathrm{I}_{\mathrm{N}}=15 \mu \mathrm{~A}$ | 0.9 | 1.0 | 1.1 | 1/1 |

Function Generator Section: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}$ unless otherwise noted.

| Differential Drive Voltage ( $\mathrm{V}_{\text {COS }+}-\mathrm{V}_{\text {COS- }}$ ) | $\begin{aligned} & 10 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V} \\ & \Theta=0^{\circ} \end{aligned}$ | 7.5 | 8.0 | 8.5 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Differential Drive Voltage $\left(\mathrm{V}_{\mathrm{SIN}_{+}}-\mathrm{V}_{\mathrm{SIN}-}\right)$ | $\begin{aligned} & 10 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V} \\ & \Theta=90^{\circ} \end{aligned}$ | 7.5 | 8.0 | 8.5 | V |
| Differential Drive Voltage ( $\mathrm{V}_{\mathrm{COS}+}-\mathrm{V}_{\mathrm{COS}-}$ ) | $\begin{aligned} & 10 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V} \\ & \Theta=180^{\circ} \end{aligned}$ | -8.5 | -8.0 | -7.5 | V |
| Differential Drive Voltage $\left(\mathrm{V}_{\mathrm{SIN}_{+}}-\mathrm{V}_{\mathrm{SIN}-}\right)$ | $\begin{aligned} & 10 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V} \\ & \Theta=270^{\circ} \end{aligned}$ | -8.5 | -8.0 | -7.5 | V |

3. Input is clamped by an internal 12 V Zener.
4. Applies to $\%$ of full scale $\left(270^{\circ}\right)$.

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}, 8.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}\right.$, unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Function Generator Section: $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=13.1 \mathrm{~V}$ unless otherwise noted. (continued) |  |  |  |  |  |
| Differential Drive Load | $\begin{array}{r} 10 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V},-40^{\circ} \mathrm{C} \\ 25^{\circ} \mathrm{C} \\ 105^{\circ} \mathrm{C} \end{array}$ | $\begin{aligned} & 178 \\ & 239 \\ & 314 \end{aligned}$ | - | - | $\begin{aligned} & \Omega \\ & \Omega \\ & \Omega \end{aligned}$ |
| Zero Hertz Output Voltage | - | -0.08 | 0 | +0.08 | V |
| Function Generator Error (Note 5) Reference Figures 2, 3, 4, 5 | $\begin{aligned} & \Theta=0^{\circ} \text { to } 225^{\circ} \\ & \Theta=226^{\circ} \text { to } 305^{\circ} \end{aligned}$ | $\begin{aligned} & -2.0 \\ & -3.0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & +2.0 \\ & +3.0 \end{aligned}$ | deg <br> deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 16 \mathrm{~V}$ | -1.0 | 0 | +1.0 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 10 \mathrm{~V}$ | -1.0 | 0 | +1.0 | deg |
| Function Generator Error | $13.1 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 8.0 \mathrm{~V}$ | -7.0 | 0 | +7.0 | deg |
| Function Generator Error | $25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 80^{\circ} \mathrm{C}$ | -2.0 | 0 | +2.0 | deg |
| Function Generator Error | $25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 105^{\circ} \mathrm{C}$ | -4.0 | 0 | +4.0 | deg |
| Function Generator Error | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 25^{\circ} \mathrm{C}$ | -2.0 | 0 | +2.0 | deg |
| Function Generator Gain | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \Theta$ vs F/V ${ }_{\text {OUT }}$, | 60 | 77 | 95 | \%/V |

5. Deviation from nominal per Table 1 after calibration at $0^{\circ}$ and $270^{\circ}$.

PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# |  | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: | :---: |
| DIP-16 | SO-20L |  |  |
| 1 | 1 | $\mathrm{V}_{\mathrm{CC}}$ | Ignition or battery supply voltage. |
| 2 | 2 | $V_{\text {REG }}$ | Voltage regulator output. |
| 3 | 3 | BIAS | Test point or zero adjustment. |
| 4, 5, 12, 13 | 5, 6, 15, 16 | GND | Ground Connections. |
| 6 | 8 | COS- | Negative cosine output signal. |
| 7 | 9 | SIN- | Negative sine output signal. |
| 8 | 10 | $\mathrm{FREQ}_{\text {IN }}$ | Speed or RPM input signal. |
| 9 | 11 | SQout | Buffered square wave output signal. |
| 10 | 12 | $\mathrm{SIN}+$ | Positive sine output signal. |
| 11 | 13 | COS+ | Positive cosine output signal. |
| 14 | 18 | CP- | Negative input to charge pump. |
| 15 | 19 | CP+ | Positive input to charge pump. |
| 16 | 20 | F/V ${ }_{\text {OUT }}$ | Output voltage proportional to input signal frequency. |
| - | 4, 7, 14, 17 | NC | No connection. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Function Generator Output Voltage vs. Degrees of Deflection


Figure 4. Output Angle in Polar Form
$\mathrm{F} / \mathrm{V}_{\mathrm{OUT}}=2.0 \mathrm{~V}+2.0 \times \mathrm{FREQ} \times \mathrm{CCP} \times \mathrm{RT} \times\left(\mathrm{V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right)$


Figure 3. Charge Pump Output Voltage vs. Output Angle


Figure 5. Nominal Output Deviation


Figure 6. Nominal Angle vs. Ideal Angle (After Calibrating at $\mathbf{1 8 0}^{\boldsymbol{}}$ )

Table 1. Function Generator Output Nominal Angle vs. Ideal Angle (After Calibrating at $\mathbf{2 7 0}^{\mathbf{\circ}}$ )

| Ideal $\Theta$ Degrees | $\begin{gathered} \text { Nominal } \\ \Theta \\ \text { Degrees } \end{gathered}$ | Ideal $\Theta$ Degrees | $\begin{gathered} \text { Nominal } \\ \Theta \\ \text { Degrees } \end{gathered}$ | Ideal $\Theta$ Degrees | $\begin{gathered} \hline \text { Nominal } \\ \Theta \\ \text { Degrees } \end{gathered}$ | Ideal $\Theta$ Degrees | $\begin{gathered} \text { Nominal } \\ \Theta \\ \text { Degrees } \end{gathered}$ | Ideal $\Theta$ Degrees | $\begin{gathered} \hline \text { Nominal } \\ \Theta \\ \text { Degrees } \end{gathered}$ | Ideal $\Theta$ Degrees | $\begin{array}{c\|} \hline \text { Nominal } \\ \Theta \\ \text { Degrees } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 17 | 17.98 | 34 | 33.04 | 75 | 74.00 | 160 | 159.14 | 245 | 244.63 |
| 1 | 1.09 | 18 | 18.96 | 35 | 34.00 | 80 | 79.16 | 165 | 164.00 | 250 | 249.14 |
| 2 | 2.19 | 19 | 19.92 | 36 | 35.00 | 85 | 84.53 | 170 | 169.16 | 255 | 254.00 |
| 3 | 3.29 | 20 | 20.86 | 37 | 36.04 | 90 | 90.00 | 175 | 174.33 | 260 | 259.16 |
| 4 | 4.38 | 21 | 21.79 | 38 | 37.11 | 95 | 95.47 | 180 | 180.00 | 265 | 264.53 |
| 5 | 5.47 | 22 | 22.71 | 39 | 38.21 | 100 | 100.84 | 185 | 185.47 | 270 | 270.00 |
| 6 | 6.56 | 23 | 23.61 | 40 | 39.32 | 105 | 106.00 | 190 | 190.84 | 275 | 275.47 |
| 7 | 7.64 | 24 | 24.50 | 41 | 40.45 | 110 | 110.86 | 195 | 196.00 | 280 | 280.84 |
| 8 | 8.72 | 25 | 25.37 | 42 | 41.59 | 115 | 115.37 | 200 | 200.86 | 285 | 286.00 |
| 9 | 9.78 | 26 | 26.23 | 43 | 42.73 | 120 | 119.56 | 205 | 205.37 | 290 | 290.86 |
| 10 | 10.84 | 27 | 27.07 | 44 | 43.88 | 125 | 124.00 | 210 | 209.56 | 295 | 295.37 |
| 11 | 11.90 | 28 | 27.79 | 45 | 45.00 | 130 | 129.32 | 215 | 214.00 | 300 | 299.21 |
| 12 | 12.94 | 29 | 28.73 | 50 | 50.68 | 135 | 135.00 | 220 | 219.32 | 305 | 303.02 |
| 13 | 13.97 | 30 | 29.56 | 55 | 56.00 | 140 | 140.68 | 225 | 225.00 |  |  |
| 14 | 14.99 | 31 | 30.39 | 60 | 60.44 | 145 | 146.00 | 230 | 230.58 |  |  |
| 15 | 16.00 | 32 | 31.24 | 65 | 64.63 | 150 | 150.44 | 235 | 236.00 |  |  |
| 16 | 17.00 | 33 | 32.12 | 70 | 69.14 | 155 | 154.63 | 240 | 240.44 |  |  |

Note: Temperature, voltage and nonlinearity not included.

## CIRCUIT DESCRIPTION and APPLICATION NOTES

The CS8191 is specifically designed for use with air-core meter movements. It includes an input comparator for sensing an input signal from an ignition pulse or speed sensor, a charge pump for frequency to voltage conversion, a bandgap voltage regulator for stable operation, and a function generator with sine and cosine amplifiers to differentially drive the meter coils.

From the partial schematic of Figure 7, the input signal is applied to the $\mathrm{FREQ}_{\text {IN }}$ lead, this is the input to a high impedance comparator with a typical positive input threshold of 2.7 V and typical hysteresis of 0.4 V . The output of the comparator, SQout, is applied to the charge pump input $\mathrm{CP}+$ through an external capacitor $\mathrm{C}_{\mathrm{CP}}$. When the input signal changes state, $\mathrm{C}_{\mathrm{CP}}$ is charged or discharged through R3 and R4. The charge accumulated on $\mathrm{C}_{\mathrm{CP}}$ is mirrored to C4 by the Norton Amplifier circuit comprising of Q1, Q2 and Q3. The charge pump output voltage, F/V ranges from 2.0 V to 6.3 V depending on the input signal frequency and the gain of the charge pump according to the formula:
$\mathrm{F} / \mathrm{V}_{\text {OUT }}=2.0 \mathrm{~V}+2.0 \times \mathrm{FREQ} \times \mathrm{C} \mathbf{C P} \times \mathrm{RT} \times(\mathrm{VREG}-0.7 \mathrm{~V})$
$\mathrm{R}_{\mathrm{T}}$ is a potentiometer used to adjust the gain of the F/V output stage and give the correct meter deflection. The F/V output voltage is applied to the function generator which generates the sine and cosine output voltages. The output voltage of the sine and cosine amplifiers are derived from the
on-chip amplifier and function generator circuitry. The various trip points for the circuit (i.e., $0^{\circ}, 90^{\circ}, 180^{\circ}, 270^{\circ}$ ) are determined by an internal resistor divider and the bandgap voltage reference. The coils are differentially driven, allowing bidirectional current flow in the outputs, thus providing up to $305^{\circ}$ range of meter deflection. Driving the coils differentially offers faster response time, higher current capability, higher output voltage swings, and reduced external component count. The key advantage is a higher torque output for the pointer.
The output angle, $\Theta$, is equal to the $\mathrm{F} / \mathrm{V}$ gain multiplied by the function generator gain:

$$
\Theta=A_{F} / V \times A_{F G},
$$

where:

$$
\mathrm{AFG}=77^{\circ} / \mathrm{V}(\mathrm{typ})
$$

The relationship between input frequency and output angle is:

or,
$\Theta=970 \times \mathrm{FREQ} \times \mathrm{C}_{\mathrm{CP}} \times \mathrm{RT}$
The ripple voltage at the F/V converter's output is determined by the ratio of $\mathrm{C}_{\mathrm{CP}}$ and C 4 in the formula:

$$
\Delta \mathrm{V}=\frac{\mathrm{CCP}\left(\mathrm{~V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right)}{\mathrm{C} 4}
$$

Ripple voltage on the F/V output causes pointer or needle flutter especially at low input frequencies.

The response time of the $\mathrm{F} / \mathrm{V}$ is determined by the time constant formed by $\mathrm{R}_{\mathrm{T}}$ and C 4 . Increasing the value of C 4
will reduce the ripple on the F/V output but will also increase the response time. An increase in response time causes a very slow meter movement and may be unacceptable for many applications.


Figure 7. Partial Schematic of Input and Charge Pump


Figure 8. Timing Diagram of FREQ $_{\text {IN }}$ and $\mathrm{I}_{\mathbf{C P}}$


Notes:

1. The product of $C 4$ and $R_{T}$ have a direct effect on gain and therefore directly affect temperature compensation.
2. C 4 Range; 20 pF to $0.2 \mu \mathrm{~F}$.
3. R4 Range; $100 \mathrm{k} \Omega$ to $500 \mathrm{k} \Omega$.
4. The IC must be protected from transients above 60 V and reverse battery conditions.
5. Additional filtering on the $\mathrm{FREQ}_{\mathrm{IN}}$ lead may be required.
6. Gauge coil connections to the IC must be kept as short as possible ( $\leq 3.0$ inch) for best pointer stability.

Figure 9. Speedometer or Tachometer Application

## Design Example

Maximum meter Deflection $=270^{\circ}$
Maximum Input Frequency $=350 \mathrm{~Hz}$

1. Select $\mathbf{R}_{\mathbf{T}}$ and $\mathbf{C}_{\mathbf{C P}}$

$$
\Theta=970 \times \mathrm{FREQ} \times \mathrm{C} C P \times \mathrm{R}_{\mathrm{T}}
$$

Let $\mathrm{C}_{\mathrm{CP}}=0.0033 \mu \mathrm{~F}$, find $\mathrm{R}_{\mathrm{T}}$

$$
\begin{gathered}
\mathrm{RT}=\frac{270^{\circ}}{970 \times 350 \mathrm{~Hz} \times 0.0033 \mu \mathrm{~F}} \\
\mathrm{RT}=243 \mathrm{k} \Omega
\end{gathered}
$$

RT should be a $250 \mathrm{k} \Omega$ potentiometer to trim out any inaccuracies due to IC tolerances or meter movement pointer placement.

## 2. Select R3 and R4

Resistor R3 sets the output current from the voltage regulator. The maximum output current from the voltage regulator is 10 mA . R3 must ensure that the current does not exceed this limit.

Choose R3 $=3.3 \mathrm{k} \Omega$
The charge current for $\mathrm{C}_{\mathrm{CP}}$ is

$$
\frac{\mathrm{V}_{\mathrm{REG}}-0.7 \mathrm{~V}}{3.3 \mathrm{k} \Omega}=1.90 \mathrm{~mA}
$$

$\mathrm{C}_{\mathrm{CP}}$ must charge and discharge fully during each cycle of the input signal. Time for one cycle at maximum frequency is 2.85 ms . To ensure that $\mathrm{C}_{\mathrm{CP}}$ is charged, assume that the $(\mathrm{R} 3+\mathrm{R} 4) \mathrm{C}_{\mathrm{CP}}$ time constant is less than $10 \%$ of the minimum input period.

$$
\mathrm{T}=10 \% \times \frac{1}{350 \mathrm{~Hz}}=285 \mu \mathrm{~s}
$$

Choose R4 $=1.0 \mathrm{k} \Omega$.
Discharge time: $\mathrm{t}_{\mathrm{DCHG}}=\mathrm{R} 3 \times \mathrm{C}_{\mathrm{CP}}=3.3 \mathrm{k} \Omega \times 0.0033 \mu \mathrm{~F}$

$$
=10.9 \mu \mathrm{~s}
$$

Charge time: $\mathrm{t}_{\mathrm{CHG}}=(\mathrm{R} 3+\mathrm{R} 4) \mathrm{C}_{\mathrm{CP}}=4.3 \mathrm{k} \Omega \times 0.0033 \mu \mathrm{~F}$

$$
=14.2 \mu \mathrm{~s}
$$

## 3. Determine C4

C 4 is selected to satisfy both the maximum allowable ripple voltage and response time of the meter movement.

$$
\mathrm{C} 4=\frac{\mathrm{C}_{\mathrm{CP}}\left(\mathrm{~V}_{\mathrm{REG}}-0.7 \mathrm{~V}\right)}{\Delta \mathrm{V}_{\mathrm{MAX}}}
$$

With $\mathrm{C} 4=0.47 \mu \mathrm{~F}$, the $\mathrm{F} / \mathrm{V}$ ripple voltage is 44 mV .
Figure 10 shows how the CS8191 and the CS8441 are used to produce a Speedometer and Odometer circuit.


Figure 10. Speedometer With Odometer or Tachometer Application

In some cases a designer may wish to use the CS8191 only as a driver for an air-core meter having performed the F/V conversion elsewhere in the circuit.

Figure 11 shows how to drive the CS8191 with a DC voltage ranging from 2.0 V to 6.0 V . This is accomplished by forcing a voltage on the $\mathrm{F} / \mathrm{V}_{\text {OUT }}$ lead. The alternative scheme shown in Figure 12 uses an external op amp as a buffer and operates over an input voltage range of 0 V to 4.0 V .


Figures 11 and 12 are not temperature compensated.


Figure 12. Driving the CS8191 from an External DC Voltage Using an Op Amp Buffer

Figure 11. Driving the CS8191 from an External DC Voltage

PACKAGE THERMAL DATA

| Parameter |  | DIP-16 | SO-20L | Unit |
| :--- | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {©JC }}$ | Typical | 15 | 9 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $\mathrm{R}_{\text {©JA }}$ | Typical | 50 | 55 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS4192

## Single Air-Core Gauge Driver

The CS4192 is a monolithic BiCMOS integrated circuit used to translate a digital 10-bit word from a microprocessor/microcontroller to complementary DC outputs. The DC outputs drive an air-core meter commonly used in vehicle instrument panels. The 10 bits of data are used to linearly control the quadrature coils of the meter directly with a $0.35^{\circ}$ resolution and $\pm 1.2^{\circ}$ accuracy over the full $360^{\circ}$ range of the gauge. The interface from the microcontroller is by a Serial Peripheral Interface (SPI) compatible serial connection using up to a 2.0 MHz shift clock rate.

The digital code, which is directly proportional to the desired gauge pointer deflection, is shifted into a DAC and multiplexer. These two blocks provide a tangential conversion function to change the digital data into the appropriate DC coil voltage for the angle demanded. The tangential algorithm creates approximately $40 \%$ more torque in the meter movement than does a sin-cos algorithm at $45^{\circ}, 135^{\circ}, 225^{\circ}$, and $315^{\circ}$ angles. This increased torque reduces the error due to pointer droop at these critical angles.

Each output buffer is capable of supplying up to 70 mA per coil and the buffers are controlled by a common OE enable pin. The output buffers are turned off when OE is brought low, while the logic portion of the chip remains powered and continues to operate normally. OE must be high before the falling edge of CS to enable the output buffers. The status pin (ST) reflects the state of the outputs and is low whenever the outputs are disabled.

The Serial Gauge Driver is self-protected against fault conditions. Each driver is protected for 125 mA (typ.) overcurrent while a global thermal protection circuit limits junction temperature to $170^{\circ} \mathrm{C}$ (typ.). The output drivers are disabled anytime the IC protection circuitry detects an overcurrent or overtemperature fault. The drivers remain disabled until a falling edge is presented on CS. If the fault is still present, the output drivers automatically disable themselves again.

## Features

- Serial Input Bus
- 2.0 MHz Operating Frequency
- Tangential Drive Algorithm
- 70 mA Drive Circuits
- $0.5^{\circ}$ Accuracy (Typ.)
- Power-On-Reset
- Protection Features
- Output Short Circuit
- Overtemperature
- Internally Fused Leads in SO-16L Package

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com


SO-16L DWF SUFFIX CASE 751G

## PIN CONNECTION AND

 MARKING DIAGRAM

$$
\begin{array}{ll}
\text { A } & =\text { Assembly Location } \\
\text { WL, L } & =\text { Wafer Lot } \\
\text { YY, Y } & =\text { Year } \\
\text { WW, W } & =\text { Work Week }
\end{array}
$$

## ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| CS4192XDWF16 | SO-16L | 46 Units/Rail |
| CS4192XDWFR16 | SO-16L | 1000 Tape \& Reel |



Figure 1. Block Diagram

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Voltage | $V_{B B}$ $V_{C C}$ | $\begin{gathered} -1.0 \text { to } 16.5 \\ -1.0 \text { to } 6.0 \end{gathered}$ | V |
| Digital Inputs |  | -1.0 to 6.0 | V |
| Steady State Output Current |  | $\pm 100$ | mA |
| Forced Injection Current (Inputs and Supply) |  | $\pm 10$ | mA |
| Operating Junction Temperature, ( $\mathrm{T}_{\mathrm{J}}$ ) |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature Soldering | Reflow (SMD styles only) Note 1 | 230 peak | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Package Thermal Resistance, SO-16L Junction-to-Case, R ®Jc Junction-to-Ambient, R RJJA |  | $\begin{aligned} & 18 \\ & 75 \end{aligned}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |

1. 60 seconds max above $183^{\circ}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{J}} \leq 105^{\circ} \mathrm{C} ; 7.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BB}} \leq 14 \mathrm{~V}, 4.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 5.5 \mathrm{~V}\right.$;
unless otherwise specified. Note 2.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Voltages and Currents |  |  |  |  |  |
| $V_{\text {BB }}$ Quiescent Current | Output disabled ( $\mathrm{OE}=0 \mathrm{~V}$ ) <br> $\left[R_{\text {COS }}, R_{\text {SIN }}=R_{\text {L(MIN) }}\right]$ @ $45^{\circ}$ (code $=X^{\prime} 080$ ) $\mathrm{V}_{\mathrm{BB}}=14 \mathrm{~V}$ | - | $1.0$ | $\begin{aligned} & 5.0 \\ & 175 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |
| $\mathrm{V}_{\text {CC }}$ Quiescent Current | $\mathrm{OE}, \mathrm{CS}, \mathrm{DI}=$ high, $\mathrm{V}_{\mathrm{BB}}=0 \mathrm{~V}, \mathrm{SCLK}=2.0 \mathrm{MHz}$ | - | - | 1.15 | mA |

Digital Inputs and Outputs

| Output High Voltage | $\mathrm{SO}, \mathrm{IOH}_{\mathrm{OH}}=0.8 \mathrm{~mA}$ | $\mathrm{~V}_{\mathrm{CC}}-0.8$ | - | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Low Voltage | $\mathrm{SO}, \mathrm{I}_{\mathrm{OL}}=0.8 \mathrm{~mA}$ | - | - | 0.4 | V |
|  | $\mathrm{ST}, \mathrm{IOL}=2.5 \mathrm{~mA}$ | - | - | 0.8 | V |
| Output Off Leakage | $\mathrm{ST}, \mathrm{V}$ CC $=5.0 \mathrm{~V}$ | - | - | 25 | $\mu \mathrm{~A}$ |
| Input High Voltage | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}, \mathrm{OE}$ | $0.7 \times \mathrm{V}_{\mathrm{CC}}$ | - | - | V |
| Input Low Voltage | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}, \mathrm{OE}$ | - | - | $0.3 \times$ | V |
|  |  |  |  | - | 1.0 |
| Input High Current | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}, \mathrm{OE} ; \mathrm{V}_{\mathrm{CC}}=0.7 \times \mathrm{V}_{\mathrm{CC}}$ | $\mu \mathrm{A}$ |  |  |  |
| Input Low Current | $\mathrm{CS}, \mathrm{SCLK}, \mathrm{SI}, \mathrm{OE} ; \mathrm{V}_{\mathrm{IN}}=0.3 \times \mathrm{V}_{\mathrm{CC}}$ | - | - | 1.0 | $\mu \mathrm{~A}$ |

## Analog Outputs

| Output Function Accuracy | - | -1.2 | $\pm 0.5$ | +1.2 | deg |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Shutdown Current, Source | $\mathrm{V}_{\mathrm{BB}}=14 \mathrm{~V}$ | 70 | 125 | 250 | mA |
| Output Shutdown Current, Sink | $\mathrm{V}_{\mathrm{BB}}=14 \mathrm{~V}$ | 70 | 125 | 250 | mA |
| Output Shutdown Current, Source | $\mathrm{V}_{\mathrm{BB}}=7.5 \mathrm{~V}$ | 43 | 125 | 250 | mA |
| Output Shutdown Current, Sink | $\mathrm{V}_{\mathrm{BB}}=7.5 \mathrm{~V}$ | 43 | 125 | 250 | mA |
| Thermal Shutdown | - | - | 170 | - | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysteresis | - | - | 20 | - | ${ }^{\circ} \mathrm{C}$ |
| Coil Drive Output Voltage | - | - | $0.748 \times \mathrm{V}_{\mathrm{BB}}$ | - | V |
| Minimum Load Resistance | $\begin{aligned} & \mathrm{T}_{\mathrm{A}}=105^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \end{aligned}$ | - | $\begin{aligned} & 229 \\ & 171 \\ & 150 \end{aligned}$ | - | $\begin{aligned} & \Omega \\ & \Omega \\ & \Omega \end{aligned}$ |
| Shift Clock Frequency | - | - | - | 2.0 | MHz |
| SCLK High Time | - | 175 | - | - | ns |
| SCLK Low Time | - | 175 | - | - | ns |
| SO Rise Time | 0.75 V to $\mathrm{V}_{\mathrm{CC}}-1.2 \mathrm{~V} ; \mathrm{C}_{\mathrm{L}}=90 \mathrm{pF}$ | - | - | 150 | ns |
| SO Fall Time | 0.75 V to $\mathrm{V}_{\mathrm{CC}}-1.2 \mathrm{~V} ; \mathrm{C}_{\mathrm{L}}=90 \mathrm{pF}$ | - | - | 150 | ns |
| SO Delay Time | $\mathrm{C}_{\mathrm{L}}=90 \mathrm{pF}$ | - | - | 150 | ns |
| SI Setup Time | - | 75 | - | - | ns |
| SI Hold Time | - | 75 | - | - | ns |
| CS Setup Time | Note 3. | 0 | - | - | ns |
| CS Hold Time | - | 75 | - | - | ns |

2. Designed to meet these characteristics over the stated voltage and temperature ranges, though may not be $100 \%$ parametrically tested in production.
3. OE must be high at falling edge of CS. This condition ensures valid output for any given input.

PIN FUNCTION DESCRIPTION

| PACKAGE PIN \# | PIN SYMBOL | FUNCTION |
| :---: | :---: | :---: |
| 16 Lead SO Wide |  |  |
| 1 | SIN- | Negative output for SINE coil. |
| 2 | SIN+ | Positive output SINE coil. |
| 3 | $\mathrm{V}_{\mathrm{BB}}$ | Analog supply. Nominally 13.5 V . |
| 4, 5, 12, 13 | GND | Ground. |
| 6 | SI | Serial data input. Data present at the rising edge of the clock signal is shifted into the internal shift register. |
| 7 | $\mathrm{V}_{\mathrm{CC}}$ | 5.0 V logic supply. The internal registers and latches are reset by a POR generated by the rising edge of the voltage on this pin. |
| 8 | OE | Controls the state of the output buffers. A logic low on this pin turns them off. |
| 9 | SCLK | Serial clock for shifting in/out of data. Rising edge shifts data on SI into the shift register and the falling edge changes the data on SO. |
| 10 | CS | When high allows data at SI to be shifted into part with the rising edges of SCLK. The falling edge transfers the shift register contents into the DAC and multiplexer to update the output buffers. The falling edge also reenables the output drivers if they have been disabled by a fault. |
| 11 | ST | STATUS reflects the state of the outputs and is low anytime the outputs are disabled, either by OE or the internal protection circuitry. Requires external pull-up resistor. |
| 14 | SO | Serial data output. Existing 10-bit data is shifted out when new data is shifted in. Allows cascading of multiple devices on common serial port. |
| 15 | COS- | Negative output for COSINE coil. |
| 16 | COS+ | Positive output for COSINE coil. |

## APPLICATIONS INFORMATION

THEORY OF OPERATION
The SACD is for interfacing between a microcontroller or microprocessor and air-core meter movements commonly used in automotive vehicles for speedometers and tachometers. These movements are built using two coils placed at a $90^{\circ}$ orientation to each other. A magnetized disc floats in the middle of the coils and responds to the magnetic field generated by each coil. The disc has a shaft attached to it that protrudes out of the assembly. A pointer indicator is attached to this shaft and in conjunction with a separate printed scale displays the vehicle's speed or the engine's speed.

The disc (and pointer) respond to the vector sum of the voltages applied to the coils. Ideally, this relationship follows a sine/cosine equation. Since this is a transcendental and non-linear function, devices of this type use an approximation for this relationship. The SACD uses a tangential algorithm as shown in Figure 2. Only one output varies in any 45 degree range.


Figure 2. SIN, COS Outputs

## Quadrant I

$$
\theta=\operatorname{Tan}^{-1}\left[\frac{\mathrm{~V}_{\mathrm{SIN}+}-\mathrm{V}_{\mathrm{SIN}-}}{\mathrm{V}_{\mathrm{COS}+}-\mathrm{V}_{\mathrm{COS}}-}\right]
$$

For $\theta=0.176^{\circ}$ to $44.824^{\circ}$ :

$$
\mathrm{V}_{\mathrm{SIN}}=\operatorname{Tan} \theta \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

$$
V_{\mathrm{COS}}=0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

For $\theta=45.176^{\circ}$ to $89.824^{\circ}$ :

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{SIN}}=0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \mathrm{~V}_{\mathrm{COS}}=\operatorname{Tan}\left(90^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

## Quadrant II

$$
\theta=180^{\circ}-\operatorname{Tan}^{-1}\left[\frac{\mathrm{~V}_{\mathrm{SIN}+}-\mathrm{V}_{\mathrm{SIN}-}}{\mathrm{V}_{\mathrm{COS}+}-\mathrm{V}_{\mathrm{COS}}-}\right]
$$

For $\theta=90.176^{\circ}$ to $134.824^{\circ}$ :

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{SIN}}=0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \mathrm{~V}_{\mathrm{COS}}=-\operatorname{Tan}\left(\theta-90^{\circ}\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

$$
\begin{aligned}
& \text { For } \theta=135.176^{\circ} \text { to } 179.824^{\circ}: \\
& \quad V_{\mathrm{SIN}}=\operatorname{Tan}\left(180^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \mathrm{~V}_{\mathrm{COS}}=-0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

## Quadrant III

$$
\theta=180^{\circ}+\operatorname{Tan}^{-1}\left[\frac{\mathrm{~V}_{\mathrm{SIN}}+-\mathrm{V}_{\mathrm{SIN}-}}{\mathrm{V}_{\mathrm{COS}+}-\mathrm{V}_{\mathrm{COS}}-}\right]
$$

For $\theta=180.176^{\circ}$ to $224.824^{\circ}$ :

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{SIN}}=-\operatorname{Tan}\left(\theta-180^{\circ}\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \mathrm{~V}_{\mathrm{COS}}=-0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

For $\theta=225.176^{\circ}$ to $269.824^{\circ}$ :

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{SIN}}=-0.748 \times \mathrm{V}_{\mathrm{BB}} \\
& \mathrm{~V}_{\mathrm{COS}}=-\operatorname{Tan}\left(270^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
\end{aligned}
$$

## Quadrant IV

$$
\theta=360^{\circ}-\operatorname{Tan}^{-1}\left[\frac{\mathrm{~V}_{\mathrm{SIN}+}-\mathrm{V}_{\mathrm{SIN}-}}{\mathrm{V}_{\mathrm{COS}+}-\mathrm{V}_{\mathrm{COS}}-}\right]
$$

For $\theta=270.176^{\circ}$ to $314.824^{\circ}$ :

$$
\mathrm{V}_{\mathrm{SIN}}=-0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

$$
\mathrm{V}_{\mathrm{COS}}=\operatorname{Tan}\left(\theta-270^{\circ}\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}
$$

For $\theta=315.176^{\circ}-359.824^{\circ}$ :
$\mathrm{V}_{\mathrm{SIN}}=-\operatorname{Tan}\left(360^{\circ}-\theta\right) \times 0.748 \times \mathrm{V}_{\mathrm{BB}}$
$\mathrm{V}_{\mathrm{COS}}=0.748 \times \mathrm{V}_{\mathrm{BB}}$


Figure 3. Gauge Response
To drive the gauge's pointer to a particular angle, the microcontroller sends a 10 -bit digital word into the serial port. These 10 bits are divided as shown in Figure 4.


Figure 4. Definition of Serial Word

However, from a software programmers viewpoint, a $360^{\circ}$ circle is divided into 1024 equal parts of $0.35^{\circ}$ each. Table 1 shows the data associated with the $45^{\circ}$ divisions of the $360^{\circ}$ driver.

Table1. Nominal Output ( $\mathrm{V}_{\mathrm{BB}}=14 \mathrm{~V}$ )

| Input Code <br> (Decimal) | Ideal <br> Degrees | Nominal <br> Degrees | $\mathbf{V}_{\text {SIN }}$ <br> $(\mathrm{V})$ | $\mathbf{V}_{\text {Cos }}$ <br> $(\mathrm{V})$ |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0.176 | 0.032 | 10.476 |
| 128 | 45 | 45.176 | 10.476 | 10.412 |
| 256 | 90 | 90.176 | 10.476 | -0.032 |
| 384 | 135 | 135.176 | 10.412 | -10.476 |
| 512 | 180 | 180.176 | -0.032 | -10.476 |
| 640 | 225 | 225.176 | -10.476 | -10.412 |
| 768 | 270 | 270.176 | -10.476 | 0.032 |
| 896 | 315 | 315.176 | -10.476 | 10.476 |
| 1023 | 359.65 | 359.826 | -0.032 | 10.476 |

The 10 bits are shifted into the device's shift register MSB first using an SPI compatible scheme. This method is shown in Figure 5. The CS must be high and remain high for SCLK to be enabled. Data on SI is shifted in on the rising edge of the synchronous clock signal. Data in the shift register changes at SO on the falling edge of SCLK. This arrangement allows the cascading of devices. SO is always enabled. Data shifts through without affecting the outputs until CS is brought low. At this time the internal DAC is updated and the outputs change accordingly.


Figure 5. Serial Data Timing Diagram
Figure 6 shows the power-up sequence for the CS4192. Note the IC requires a pulse on the Chip Select (CS) pin to clear the Status Fault (ST) after power up. OE must be high before the falling edge of CS to enable the output buffers.


Figure 6. Power Up Sequence

CS4192


Figure 7. Application Diagram

## Zero Voltage Switch Power Controller

The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI-free power regulation of resistive loads. Operating directly on the AC power line, its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built-in digital sawtooth waveform permits proportional temperature regulation action over $\mathrm{a} \pm 1^{\circ} \mathrm{C}$ band around the set point. For energy savings there is a programmable temperature reduction function, and for security a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e. defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to $5^{\circ} \mathrm{C}$ around the set point. All these features are implemented with a very low external component count.

- Zero Voltage Switch for Triacs, up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proportional Regulation of Temperature over a $1^{\circ} \mathrm{C}$ Band
- Programmable Temperature Reduction
- Preset Temperature (i.e. Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count

ZERO VOLTAGE SWITCH POWER CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE CASE 626


D SUFFIX PLASTIC PACKAGE CASE 751
(SO-8)


PIN CONNECTIONS


MAXIMUM RATINGS (Voltages referenced to Pin 7)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Supply Current ( $\mathrm{I}_{\text {Pin } 5}$ ) | $\mathrm{I}_{\mathrm{CC}}$ | 15 | mA |
| Non-Repetitive Supply Current (Pulse Width $=1.0 \mu \mathrm{~s}$ ) | $I_{\text {CCP }}$ | 200 | mA |
| AC Synchronization Current | $\mathrm{l}_{\text {sync }}$ | 3.0 | mA |
| Pin Voltages | $V_{\text {Pin } 2}$ <br> $V_{\text {Pin } 3}$ <br> $V_{\text {Pin } 4}$ <br> $V_{\text {Pin } 6}$ | $\begin{aligned} & 0 ; \mathrm{V}_{\text {ref }} \\ & 0 ; \mathrm{V}_{\text {ref }} \\ & 0 ; \mathrm{V}_{\text {ref }} \\ & 0 ; \mathrm{V}_{\mathrm{EE}} \end{aligned}$ | V |
| $\mathrm{V}_{\text {ref }}$ Current Sink | $l_{\text {Pin } 1}$ | 1.0 | mA |
| $\begin{aligned} & \text { Output Current (Pin 6) } \\ & \text { (Pulse Width }<400 \mu \mathrm{~s} \text { ) } \end{aligned}$ | 10 | 150 | mA |
| Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | 625 | mW |
| Thermal Resistance, Junction-to-Air | $\mathrm{R}_{\text {өJA }}$ | 100 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Operating Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -20 to +85 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{EE}}=-7.0 \mathrm{~V}\right.$, voltages referred to Pin 7 , unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply Current (Pins 6, 8 not connected) $\left(\mathrm{T}_{\mathrm{A}}=-20^{\circ} \text { to }+85^{\circ} \mathrm{C}\right)$ | ICC | - | 0.9 | 1.5 | mA |
| Stabilized Supply Voltage (Pin 5) ( $\mathrm{ICC}^{\text {a }}$ 2.0 mA) | $\mathrm{V}_{\mathrm{EE}}$ | -10 | -9.0 | -8.0 | V |
| Reference Voltage (Pin 1) | $\mathrm{V}_{\text {ref }}$ | -6.5 | -5.5 | -4.5 | V |
| $\begin{aligned} & \text { Output Pulse Current }\left(T_{A}=-20^{\circ} \text { to }+85^{\circ} \mathrm{C}\right) \\ & \left(R_{\text {out }}=60 \mathrm{~W}, \mathrm{~V}_{\mathrm{EE}}=-8.0 \mathrm{~V}\right) \end{aligned}$ | 10 | 90 | 100 | 130 | mA |
| Output Leakage Current ( $\mathrm{V}_{\text {out }}=0 \mathrm{~V}$ ) | lOL | - | - | 10 | $\mu \mathrm{A}$ |
| Output Pulse Width ( $\mathrm{T}_{\mathrm{A}}=-20^{\circ}$ to $+85^{\circ} \mathrm{C}$ ) (Note 1) <br> (Mains = $220 \mathrm{Vrms}, \mathrm{R}_{\text {sync }}=220 \mathrm{k} \Omega$ ) | $\mathrm{T}_{\mathrm{P}}$ | 50 | - | 100 | $\mu \mathrm{s}$ |
| Comparator Offset (Note 5) | $\mathrm{V}_{\text {off }}$ | -10 | - | +10 | mV |
| Sensor Input Bias Current | $I_{\text {IB }}$ | - | - | 0.1 | $\mu \mathrm{A}$ |
| Sawtooth Period (Note 2) | $\mathrm{T}_{\mathrm{S}}$ | - | 40.96 | - | sec |
| Sawtooth Amplitude (Note 6) | $\mathrm{A}_{S}$ | 50 | 70 | 90 | mV |
| Temperature Reduction Voltage (Note 3) (Pin 4 Connected to $\mathrm{V}_{\mathrm{CC}}$ ) | $\mathrm{V}_{\text {TR }}$ | 280 | 350 | 420 | mV |
| Internal Hysteresis Voltage (Pin 2 Not Connected) | $\mathrm{V}_{\mathrm{IH}}$ | - | 10 | - | mV |
| Additional Hysteresis (Note 4) (Pin 2 Connected to $\mathrm{V}_{\mathrm{CC}}$ ) | $\mathrm{V}_{\mathrm{H}}$ | 280 | 350 | 420 | mV |
| Failsafe Threshold ( $\mathrm{T}_{\mathrm{A}}=-20^{\circ}$ to $+85^{\circ} \mathrm{C}$ ) (Note 7) | $\mathrm{V}_{\mathrm{FSth}}$ | 180 | - | 300 | mV |

NOTES: 1. Output pulses are centered with respect to zero crossing point. Pulse width is adjusted by the value of $R_{\text {sync }}$. Refer to application curves.
2. The actual sawtooth period depends on the AC power line frequency. It is exactly 2048 times the corresponding period. For the 50 Hz case it is 40.96 sec . For the 60 Hz case it is 34.13 sec . This is to comply with the European standard, namely that 2.0 kW loads cannot be connected or removed from the line more than once every 30 sec .
3.350 mV corresponds to $5^{\circ} \mathrm{C}$ temperature reduction. This is tested at probe using internal test pad. Smaller temperature reduction can be obtained by adding an external resistor between Pin 4 and $\mathrm{V}_{\mathrm{CC}}$. Refer to application curves.
4.350 mV corresponds to a hysteresis of $5^{\circ} \mathrm{C}$. This is tested at probe using internal test pad. Smaller additional hysteresis can be obtained by adding an external resistor between Pin 2 and $\mathrm{V}_{\mathrm{cc}}$. Refer to application curves
5. Parameter guaranteed but not tested. Worst case 10 mV corresponds to $0.15^{\circ} \mathrm{C}$ shift on set point.
6. Measured at probe by internal test pad. 70 mV corresponds to $1^{\circ} \mathrm{C}$. Note that the proportional band is independent of the NTC value.
7. At very low temperature the NTC resistor increases quickly. This can cause the sensor input voltage to reach the failsafe threshold, thus inhibiting output pulses; refer to application schematics. The corresponding temperature is the limit at which the circuit works in the typical application. By setting this threshold at $0.05 \mathrm{~V}_{\text {ref }}$, the NTC value can increase up to 20 times its nominal value, thus the application works below $-20^{\circ} \mathrm{C}$.


Figure 1. Application Schematic

## APPLICATION INFORMATION

(For simplicity, the LED in series with $R_{\text {out }}$ is omitted in the following calculations.)

## Triac Choice and $\mathbf{R}_{\text {out }}$ Determination

Depending on the power in the load, choose the triac that has the lowest peak gate trigger current. This will limit the output current of the UAA2016 and thus its power consumption. Use Figure 4 to determine $\mathrm{R}_{\text {out }}$ according to the triac maximum gate current $\left(\mathrm{I}_{\mathrm{GT}}\right)$ and the application low temperature limit. For a 2.0 kW load at 220 Vrms , a good triac choice is the ON Semiconductor MAC212A8. Its maximum peak gate trigger current at $25^{\circ} \mathrm{C}$ is 50 mA .

For an application to work down to $-20^{\circ} \mathrm{C}, \mathrm{R}_{\text {out }}$ should be $60 \Omega$. It is assumed that: $\mathrm{I}_{\mathrm{GT}}(\mathrm{T})=\mathrm{I}_{\mathrm{GT}}\left(25^{\circ} \mathrm{C}\right) \times \exp (-\mathrm{T} / 125)$ with T in ${ }^{\circ} \mathrm{C}$, which applies to the MAC212A8.

## Output Pulse Width, $\mathbf{R}_{\text {sync }}$

The pulse with $\mathrm{T}_{\mathrm{P}}$ is determined by the triac's $\mathrm{I}_{\text {Hold }}, \mathrm{I}_{\text {Latch }}$ together with the load value and working conditions (frequency and voltage):

Given the RMS AC voltage and the load power, the load value is:

$$
\mathrm{R}_{\mathrm{L}}=\mathrm{V}^{2} \mathrm{rms} / \mathrm{POWER}
$$

The load current is then:

$$
\mathrm{I}_{\text {Load }}=\left(\mathrm{Vrms} \times \sqrt{2} \times \sin (2 \pi \mathrm{ft})-\mathrm{V}_{\mathrm{TM}}\right) / \mathrm{R}_{\mathrm{L}}
$$

where $\mathrm{V}_{\mathrm{TM}}$ is the maximum on state voltage of the triac, f is the line frequency.

$$
\text { Set } I_{\text {Load }}=I_{\text {Latch }} \text { for } t=T_{P} / 2 \text { to calculate } T_{P} \text {. }
$$

Figures 6 and 7 give the value of $T_{P}$ which corresponds to the higher of the values of $\mathrm{I}_{\text {Hold }}$ and $\mathrm{I}_{\text {Latch }}$, assuming that $\mathrm{V}_{\mathrm{TM}}=1.6 \mathrm{~V}$. Figure 8 gives the $\mathrm{R}_{\text {sync }}$ that produces the corresponding $\mathrm{T}_{\mathrm{P}}$.

## $\mathbf{R}_{\text {Supply }}$ and Filter Capacitor

With the output current and the pulse width determined as above, use Figures 9 and 10 to determine R $_{\text {Supply }}$, assuming that the sinking current at $\mathrm{V}_{\text {ref }}$ pin (including NTC bridge current) is less than 0.5 mA . Then use Figure 11 and 12 to determine the filter capacitor $\left(\mathrm{C}_{\mathrm{F}}\right)$ according to the ripple desired on supply voltage. The maximum ripple allowed is 1.0 V .

Temperature Reduction Determined by $\mathbf{R}_{\mathbf{1}}$
(Refer to Figures 13 and 14.)


Figure 2. Comparison Between Proportional Control and ON/OFF Control


Figure 3. Zero Voltage Technique

## CIRCUIT FUNCTIONAL DESCRIPTION

## Power Supply (Pin 5 and Pin 7)

The application uses a current source supplied by a single high voltage rectifier in series with a power dropping resistor. An integrated shunt regulator delivers a $\mathrm{V}_{\mathrm{EE}}$ voltage of -8.6 V with respect to $\operatorname{Pin} 7$. The current used by the total regulating system can be shared in four functional blocks: IC supply, sensing bridge, triac gate firing pulses and zener current. The integrated zener, as in any shunt regulator, absorbs the excess supply current. The 50 Hz pulsed supply current is smoothed by the large value capacitor connected between Pins 5 and 7.

## Temperature Sensing (Pin 3)

The actual temperature is sensed by a negative temperature coefficient element connected in a resistor divider fashion. This two element network is connected between the ground terminal Pin 5 and the reference voltage -5.5 V available on Pin 1. The resulting voltage, a function of the measured temperature, is applied to Pin 3 and internally compared to a control voltage whose value depends on several elements: Sawtooth, Temperature Reduction and Hysteresis Adjust. (Refer to Application Information.)

## Temperature Reduction

For energy saving, a remotely programmable temperature reduction is available on Pin 4. The choice of resistor $\mathrm{R}_{1}$ connected between Pin 4 and $\mathrm{V}_{\mathrm{CC}}$ sets the temperature reduction level.

## Comparator

When the positive input ( $\operatorname{Pin} 3$ ) receives a voltage greater than the internal reference value, the comparator allows the triggering logic to deliver pulses to the triac gate. To improve the noise immunity, the comparator has an adjustable hysteresis. The external resistor $\mathrm{R}_{3}$ connected to Pin 2 sets the hysteresis level. Setting Pin 2 open makes a 10 mV hysteresis level, corresponding to $0.15^{\circ} \mathrm{C}$. Maximum


Figure 4. Output Resistor versus Triac Gate Current
hysteresis is obtained by connecting Pin 2 to $\mathrm{V}_{\mathrm{CC}}$. In that case the level is set at $5^{\circ} \mathrm{C}$. This configuration can be useful for low temperature inertia systems.

## Sawtooth Generator

In order to comply with European norms, the ON/OFF period on the load must exceed 30 seconds. This is achieved by an internal digital sawtooth which performs the proportional regulation without any additional component. The sawtooth signal is added to the reference applied to the comparator negative input. Figure 2 shows the regulation improvement using the proportional band action.

## Noise Immunity

The noisy environment requires good immunity. Both the voltage reference and the comparator hysteresis minimize the noise effect on the comparator input. In addition the effective triac triggering is enabled every $1 / 3 \mathrm{sec}$.

## Failsafe

Output pulses are inhibited by the "failsafe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit is open.

## Sampling Full Wave Logic

Two consecutive zero-crossing trigger pulses are generated at every positive mains half-cycle. This ensures that the number of delivered pulses is even in every case. The pulse length is selectable by $\mathrm{R}_{\text {sync }}$ connected on Pin 8 . The pulse is centered on the zero-crossing mains waveform.

## Pulse Amplifier

The pulse amplifier circuit sinks current pulses from Pin 6 to $\mathrm{V}_{\mathrm{EE}}$. The minimum amplitude is 70 mA . The triac is then triggered in quadrants II and III. The effective output current amplitude is given by the external resistor $\mathrm{R}_{\text {out }}$. Eventually, an LED can be inserted in series with the Triac gate (see Figure 1).


Figure 5. Minimum Output Current versus Output Resistor


Figure 6. Output Pulse Width versus Maximum Triac Latch Current


Figure 8. Synchronization Resistor versus Output Pulse Width


Figure 10. Maximum Supply Resistor versus Output Current


Figure 7. Output Pulse Width versus Maximum Triac Latch Current


Figure 9. Maximum Supply Resistor versus Output Current


Figure 11. Minimum Filter Capacitor versus Output Current


Figure 12. Minimum Filter Capacitor versus Output Current


Figure 14. Temperature Reduction versus Temperature Setpoint


Figure 16. $\mathbf{R}_{\mathbf{S}} \mathbf{+} \mathbf{R}_{\mathbf{2}}$ versus Preset Setpoint


Figure 13. Temperature Reduction versus $\mathbf{R}_{1}$


Figure 15. R DeF versus Preset Temperature


Figure 17. Comparator Hysteresis versus $\mathbf{R}_{\mathbf{3}}$

## CS3341, CS3351, CS387

## Alternator Voltage Regulator Darlington Driver

The CS3341/3351/387 integral alternator regulator integrated circuit provides the voltage regulation for automotive, 3-phase alternators.

It drives an external power Darlington for control of the alternator field current. In the event of a charge fault, a lamp output pin is provided to drive an external darlington transistor capable of switching on a fault indicator lamp. An overvoltage or no STATOR signal condition activates the lamp output.

The CS3341 and CS3351 are available in SO-14 packages. The CS387 is available as a Flip Chip.

## Features

- Drives NPN Darlington
- Short Circuit Protection
- 80 V Load Dump
- Temperature Compensated Regulation Voltage
- Shorted Field Protection Duty Cycle, Self Clearing



## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com
MARKING
DIAGRAM

PIN CONNECTIONS


Flip Chip, Bump Side Up


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS3341YD14 | SO-14 | 55 Units/Rail |
| CS3341YDR14 | SO-14 | 2500 Tape \& Reel |
| CS3351YD14 | SO-14 | 55 Units/Rail |
| CS3351YDR14 | SO-14 | 2500 Tape \& Reel |
| CS387H | Flip Chip | Contact Sales |

CS3341, CS3351, CS387


Figure 1. Block Diagram

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ |  | -55 to +165 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature Range |  | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Continuous Supply |  | 27 | V |
| ICC Load Dump |  | 400 | mA |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}, 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 17 \mathrm{~V}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply |  |  |  |  |  |
| Supply Current Enabled | - | - | 12 | 25 | mA |
| Supply Current Disabled | - | - | - | 50 | $\mu \mathrm{A}$ |

Driver Stage

| Output High Current | $\mathrm{V}_{\mathrm{DD}}=1.2 \mathrm{~V}$ | -10 | -6.0 | -4.0 | mA |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Output Low Voltage | $\mathrm{I}_{\mathrm{OL}}=25 \mu \mathrm{~A}$ | - | - | 0.35 | V |  |
| Minimum ON Time |  | - | 200 | - | - | $\mu \mathrm{s}$ |
| Minimum Duty Cycle |  | - | - | 6.0 | 10 | $\%$ |
| Short Circuit Duty Cycle | - | 1.0 | - | 5.0 | $\%$ |  |
| Field Switch Turn On <br> Rise Time | - | 30 | - | 90 | $\mu \mathrm{~s}$ |  |
| Field Switch Turn On <br> Fall Time |  | - | 30 | - | 90 | $\mu \mathrm{~s}$ |

## Stator

| Input High Voltage | - | 10 | - | - | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Low Voltage | - | - | - | 6.0 | V |
| Stator Time Out | High to Low | 6.0 | 100 | 600 | ms |
| Stator Power-Up Input High | CS3351 only | 10 | - | - | V |
| Stator Power-Up Input Low | CS3351 only | - | - | 6.0 | V |

Lamp

| Output High Current | $\mathrm{V}_{\text {LAMP }} @ 3.0 \mathrm{~V}$ | - | - | 50 | $\mu \mathrm{~A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Low Voltage | $\mathrm{I}_{\text {LAMP }} @ 30 \mathrm{~mA}$ | - | - | 0.35 | V |

Ignition

| Input High Voltage | $\mathrm{I}_{\mathrm{CC}}>1.0 \mathrm{~mA}$ | 1.8 | - | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Low Voltage | $\mathrm{I}_{\mathrm{CC}}<100 \mu \mathrm{~A}$ | - | - | 0.5 | V |

## Oscillator

| Oscillator Frequency | $\mathrm{C}_{\text {OSC }}=0.22 \mu \mathrm{~F}$ | 65 | - | 325 | Hz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Rise Time/Fall Time | $\mathrm{C}_{\text {OsC }}=0.22 \mu \mathrm{~F}$ | - | 17 | - | - |
| Oscillator High Threshold | $\mathrm{C}_{\text {OSC }}=0.22 \mu \mathrm{~F}$ | - | - | 6.0 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}, 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 17 \mathrm{~V}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Battery Sense |  |  |  |  |  |
| Input Current | - | -10 | - | +10 | $\mu \mathrm{A}$ |
| Regulation Voltage | $@ 25^{\circ} \mathrm{C}, \mathrm{R}_{1}=100 \mathrm{k} \Omega, \mathrm{R}_{2}=50 \mathrm{k} \Omega$ | 13.5 | - | 16 | V |
| Proportional Control | - | 0.050 | - | 0.400 | V |
| High Voltage Threshold Ratio | $\frac{\text { VHigh Voltage @ LampOn }}{\text { VRegulation @ 50\%Duty Cycle }}$ | 1.083 | - | 1.190 | - |
| High Voltage Hysteresis | - | 0.020 | - | 0.600 | V |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |  |
| :---: | :---: | :---: | :--- |
| SO-14 | Flip Chip | PIN SYMBOL |  |
| 1 | 1 |  | Output driver for external power switch-Darlington. |
| 2 | 2 | GND | Ground. |
| $3,6,7,9,13$ | 3 | NC | No Connection. |
| 4 | 4 | OSC | Timing capacitor for oscillator. |
| 5 | 5 | Lamp | Base driver for lamp driver indicates no stator signal or overvoltage condition. |
| 8 | 6 | IGN | Switched ignition power up. |
| 10 | 7 | Stator | Stator signal input for stator timer (CS3351 also power up). |
| 11 | 8 | Sense | Battery sense voltage regulator comparator input and protection. |
| 12 | 9 | VCC | Supply for IC. |
| 14 | 10 | SC | Short circuit sensing. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. Battery Voltage vs. Temperature ( ${ }^{\circ} \mathrm{C}$ ) Over Process Variation

## APPLICATIONS INFORMATION

The CS3341 and CS3351 IC's are designed for use in an alternator charging system. The circuit is also available in flip-chip form as the CS387.

In a standard alternator design (Figure 3), the rotor carries the field winding. An alternator rotor usually has several N and $S$ poles. The magnetic field for the rotor is produced by forcing current through a field or rotor winding. The Stator windings are formed into a number of coils spaced around a cylindrical core. The number of coils equals the number of pairs of N and S poles on the rotor. The alternating current in the Stator windings is rectified by the diodes and applied to the regulator. By controlling the amount of field current, the magnetic field strength is controlled and hence the output voltage of the alternator.

Referring to Figure 4, a typical application diagram, the oscillator frequency is set by an external capacitor connected between OSC and ground. The sawtooth waveform ramps between 1.0 V and 3.0 V and provides the timing for the system. For the circuit shown the oscillator frequency is approximately 140 Hz . The alternator voltage is sensed at Terminal A via the resistor divider network R1/R2 on the Sense pin of the IC. The voltage at the sense pin determines the duty cycle for the regulator. The voltage is adjusted by potentiometer R2. A relatively low voltage on the sense pin causes a long duty cycle that increases the Field current. A high voltage results in a short duty cycle.

The ignition Terminal (I) switches power to the IC through the $\mathrm{V}_{\mathrm{CC}}$ pin. In the CS3351 the Stator pin senses the voltage from the stator. This will keep the device powered while the voltage is high, and it also senses a stopped engine condition and drives the Lamp pin high after the stator
timeout expires. The Lamp pin also goes high when an overvoltage condition is detected on the sense pin. This causes the darlington lamp drive transistor to switch on and pull current through the lamp. If the system voltage continues to increase, the field and lamp output turn off as in an overvoltage or load dump condition.

The SC or Short Circuit pin monitors the field voltage. If the drive output and the SC voltage are simultaneously high for a predetermined period, a short circuit condition is assumed and the output is disabled. The regulator is forced to a minimum short circuit duty cycle.


Figure 3. IAR System Block Diagram


Figure 4. Typical Application Dlagram


Figure 5. Flip Chip Dimensions and Solder Bump Locations, Bump Side Up

## CS3341, CS3351, CS387

PACKAGE THERMAL DATA

| Parameter |  | SO-14 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 30 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 125 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## CS1124

## Dual Variable-Reluctance Sensor Interface IC

The CS1124 is a monolithic integrated circuit designed primarily to condition signals used to monitor rotating parts.

The CS1124 is a dual channel device. Each channel interfaces to a Variable Reluctance Sensor, and monitors the signal produced when a metal object is moved past that sensor. An output is generated that is a comparison of the input voltage and the voltage produced at the $\mathrm{IN}_{\text {Adj }}$ lead. The resulting square-wave is available at the OUT pin.

When the DIAG pin is high, the reference voltage at $\mathrm{IN}_{\text {Adj }}$ is increased. This then requires a larger signal at the input to trip the comparator, and provides for a procedure to test for an open sensor.

## Features

- Dual Channel Capability
- Built-In Test Mode
- On-Chip Input Voltage Clamping
- Works from 5.0 V Supply
- Accurate Built-In Hysteresis


Figure 1. Block Diagram


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```
SO-8 D SUFFIX CASE 751
```


## PIN CONNECTIONS AND

 MARKING DIAGRAM

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS1124YD8 | SO-8 | 95 Units/Rail |
| CS1124YDR8 | SO-8 | 2500 Tape \& Reel |

## MAXIMUM RATINGS*

| Rating | Value |  |
| :--- | :---: | :---: |
| Storage Temperature Range | -65 to 150 |  |
| Ambient Operating Temperature | -40 to 125 |  |
| Supply Voltage Range (continuous) | ${ }^{\circ} \mathrm{C}$ |  |
| Input Voltage Range (at any input, R1 = R2 = 22 k) | -0.3 to 7.0 |  |
| Maximum Junction Temperature | ${ }^{\circ} \mathrm{C}$ |  |
| ESD Susceptibility (Human Body Model) | -250 to 250 |  |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1$)$ | V |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (4.5 V $<\mathrm{V}_{C C}<5.5 \mathrm{~V},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<125^{\circ} \mathrm{C}, \mathrm{V}_{\text {DIAG }}=0$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ SUPPLY | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | - | - | 5.0 | mA |
| Operating Current Supply |  |  |  |  |  |

## Sensor Inputs

| Input Threshold - Positive | $\begin{aligned} & V_{\text {DIAG }}=\text { Low } \\ & V_{\text {DIAG }}=H i g h \end{aligned}$ | $\begin{aligned} & 135 \\ & 135 \end{aligned}$ | $\begin{aligned} & 160 \\ & 160 \end{aligned}$ | $\begin{aligned} & 185 \\ & 185 \end{aligned}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Threshold - Negative | $\begin{aligned} & V_{\text {DIAG }}=\text { Low } \\ & V_{\text {DIAG }}=H i g h \end{aligned}$ | $\begin{gathered} -185 \\ 135 \end{gathered}$ | $\begin{gathered} -160 \\ 160 \end{gathered}$ | $\begin{gathered} -135 \\ 185 \end{gathered}$ | $\begin{aligned} & \mathrm{mV} \\ & \mathrm{mV} \end{aligned}$ |
| Input Bias Current (INP1, INP2) | $\mathrm{V}_{\text {IN }}=0.336 \mathrm{~V}$ | -16 | -11 | -6.0 | $\mu \mathrm{A}$ |
| Input Bias Current (DIAG) | $\mathrm{V}_{\text {DIAG }}=0 \mathrm{~V}$ | - | - | 1.0 | $\mu \mathrm{A}$ |
| Input Bias Current Factor ( $\mathrm{K}_{\mathrm{l}}$ ) $\left(\mathbb{N}_{\text {Adj }}=\mathrm{INP} \times \mathrm{K}_{\mathrm{l}}\right)$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=0.336 \mathrm{~V}, \mathrm{~V}_{\text {DIAG }}=\text { Low } \\ & \mathrm{V}_{\mathrm{IN}}=0.336 \mathrm{~V}, \mathrm{~V}_{\text {DIAG }}=\text { High } \end{aligned}$ | $152$ | $\begin{aligned} & 100 \\ & 155 \end{aligned}$ | $157$ | \%INP <br> \%INP |
| Bias Current Matching | INP1 or INP2 to $\mathrm{IN}_{\text {Adj }}, \mathrm{V}_{\text {IN }}=0.336 \mathrm{~V}$ | -1.0 | 0 | 1.0 | $\mu \mathrm{A}$ |
| Input Clamp - Negative | $\begin{aligned} & \mathrm{I}_{\mathrm{N}}=-50 \mu \mathrm{~A} \\ & \mathrm{I}_{\mathrm{N}}=-12 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & -0.5 \\ & -0.5 \end{aligned}$ | $\begin{aligned} & -0.25 \\ & -0.30 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \end{aligned}$ |
| Input Clamp - Positive | $\mathrm{I}_{\mathrm{IN}}=+12 \mathrm{~mA}$ | 5.0 | 7.0 | 9.0 | V |
| Output Low Voltage | IOUT $=1.6 \mathrm{~mA}$ | - | 0.2 | 0.4 | V |
| Output High Voltage | $\mathrm{l}_{\text {OUT }}=-1.6 \mathrm{~mA}$ | $\mathrm{V}_{C C}-0.5$ | $\mathrm{V}_{C C}-0.2$ | - | V |
| Mode Change Time Delay | - | 0 | - | 20 | $\mu \mathrm{s}$ |
| Input to Output Delay | IOUT $=1.0 \mathrm{~mA}$ | - | 1.0 | 20 | $\mu \mathrm{s}$ |
| Output Rise Time | $\mathrm{C}_{\text {LOAD }}=30 \mathrm{pF}$ | - | 0.5 | 2.0 | $\mu \mathrm{s}$ |
| Output Fall Time | $\mathrm{C}_{\text {LOAD }}=30 \mathrm{pF}$ | - | 0.05 | 2.0 | $\mu \mathrm{s}$ |
| Open-Sensor Positive Threshold | $\mathrm{V}_{\text {DIAG }}=$ High, $\mathrm{R}_{\text {IN(Adj) }}=40 \mathrm{k}$. Note 2 | 29.4 | 54 | 86.9 | $\mathrm{k} \Omega$ |

## Logic Inputs

| DIAG Input Low Threshold | - | - | - | $0.2 \times \mathrm{V}_{\mathrm{CC}}$ | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| DIAG Input High Threshold | - | $0.7 \times \mathrm{V}_{\mathrm{CC}}$ | - | - | V |
| DIAG Input Resistance | $\mathrm{V}_{\mathrm{IN}}=0.3 \times \mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | 8.0 | 22 | 70 | $\mathrm{k} \Omega$ |
|  | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | 8.0 | 22 | 70 | $\mathrm{k} \Omega$ |

2. This parameter is guaranteed by design, but not parametrically tested in production.

## PACKAGE PIN DESCRIPTION*

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| SO-8 | PIN SYMBOL |  |
| 1 | IN $_{\text {Adj }}$ | FUNCTION |
| 2 | IN1 | External resistor to ground that sets the trip levels of both channels. <br> Functions for both diagnostic and normal mode. |
| 3 | IN2 | Input to channel 1. |
| 4 | GND | Input to channel 2. |
| 5 | DIAG | Ground. |
| 6 | OUT2 | Diagnostic mode switch. Normal mode is low. |
| 7 | OUT1 | Output of channel 2. |
| 8 | $V_{\text {CC }}$ | Output of channel 1. |
|  |  | Positive 5.0 volt supply input. |



Figure 2. Application Diagram

## THEORY OF OPERATION

## NORMAL OPERATION

Figure 2 shows one channel of the CS1124 along with the necessary external components. Both channels share the $\mathrm{IN}_{\text {Adj }}$ pin as the negative input to a comparator. A brief description of the components is as follows:
$\mathbf{V}_{\mathbf{R S}}$ - Ideal sinusoidal, ground referenced, sensor output - amplitude usually increases with frequency, depending on loading.
$\mathbf{R}_{\mathbf{R S}}$ - Source impedance of sensor.
$\mathbf{R 1} / \mathbf{R}_{\text {Adj }}$ - External resistors for current limiting and biasing.

INP1/IN $\mathbf{N d j}$ - Internal current sources that determine trip points via R1/R ${ }_{\text {Adj }}$.

COMP1 - Internal comparator with built-in hysteresis set at 160 mV .
OUT1 - Output $0 \mathrm{~V}-5.0 \mathrm{~V}$ square wave with the same frequency as $\mathrm{V}_{\mathrm{RS}}$.
By inspection, the voltage at the ( + ) and (-) terminals of COMP1 with $\mathrm{V}_{\mathrm{RS}}=0 \mathrm{~V}$ are:

$$
\begin{equation*}
\mathrm{V}^{+}=\operatorname{INP} 1(\mathrm{R} 1+\mathrm{RRS}) \tag{1}
\end{equation*}
$$

$$
\begin{equation*}
\mathrm{V}^{-}=\mathrm{IN}_{\mathrm{Adj}} \times \mathrm{R}_{\mathrm{Adj}} \tag{2}
\end{equation*}
$$

As $V_{R S}$ begins to rise and fall, it will be superimposed on the DC biased voltage at $\mathrm{V}^{+}$.

$$
\begin{equation*}
\mathrm{V}+=\operatorname{INP} 1\left(\mathrm{R} 1+\mathrm{R}_{\mathrm{RS}}\right)+\mathrm{V}_{\mathrm{RS}} \tag{3}
\end{equation*}
$$

To get comparator COMP1 to trip, the following condition is needed when crossing in the positive direction,

$$
\begin{equation*}
\mathrm{V}+>\mathrm{V}^{-}+\mathrm{V}_{\mathrm{HYS}} \tag{4}
\end{equation*}
$$

( $\mathrm{V}_{\text {HYS }}$ is the built-in hysteresis set to 160 mV ), or when crossing in the negative direction,

$$
\begin{equation*}
\mathrm{V}+<\mathrm{V}^{-}-\mathrm{V}_{\mathrm{HYS}} \tag{5}
\end{equation*}
$$

Combining equations 2,3 , and 4 , we get:

$$
\begin{equation*}
\operatorname{INP} 1\left(R 1+R_{R S}\right)+V_{R S}>I_{A d j} \times R_{A d j}+V_{H Y S} \tag{6}
\end{equation*}
$$

therefore,

$$
\begin{equation*}
V_{R S}(+T R P)<\operatorname{IN}_{\text {Adj }} \times R_{\text {Adj }}-\operatorname{INP} 1\left(R 1+R_{R S}\right)+V_{H Y S} \tag{7}
\end{equation*}
$$

It should be evident that tripping on the negative side is:

$$
\begin{equation*}
V_{R S}(-T R P)<I_{A d j} \times R_{A d j}-\operatorname{INP} 1\left(R 1+R_{R S}\right)-V_{H Y S} \tag{8}
\end{equation*}
$$

In normal mode,

$$
\begin{equation*}
\mathrm{INP} 1=\mathrm{IN}_{\mathrm{Adj}} \tag{9}
\end{equation*}
$$

We can now re-write equation (7) as:

$$
\begin{equation*}
\mathrm{V}_{\mathrm{RS}(+\mathrm{TR})}>\operatorname{INP1}\left(\mathrm{R}_{\mathrm{Adj}}-\mathrm{R} 1-\mathrm{R}_{\mathrm{RS}}\right)+\mathrm{V}_{\mathrm{HYS}} \tag{10}
\end{equation*}
$$

By making

$$
\begin{equation*}
R_{\text {Adj }}=R 1+R_{R S} \tag{11}
\end{equation*}
$$

you can detect signals with as little amplitude as $\mathrm{V}_{\text {HYS }}$.
A design example is given in the applications section.

## OPEN SENSOR PROTECTION

The CS1124 has a DIAG pin that when pulled high (5.0 V), will increase the $\mathrm{IN}_{\text {Adj }}$ current source by roughly $50 \%$.

Equation (7) shows that a larger $\mathrm{V}_{\mathrm{RS}(+\mathrm{TRP})}$ voltage will be needed to trip comparator COMP1. However, if no $\mathrm{V}_{\mathrm{RS}}$ signal is present, then we can use equations 1,2 , and 4 (equation 5 does not apply in this mode) to get:

$$
\begin{equation*}
\text { INP1 } \left.\mathrm{R} 1+\mathrm{R}_{\mathrm{RS}}\right)>\operatorname{INP} 1 \times \mathrm{K}_{\mathrm{I}} \times \mathrm{R}_{\text {Adj }}+\mathrm{V}_{\mathrm{HYS}} \tag{12}
\end{equation*}
$$

Since $R_{R S}$ is the only unknown variable we can solve for $\mathrm{R}_{\mathrm{RS}}$,

$$
\begin{equation*}
\mathrm{R}_{\mathrm{RS}}=\frac{\mathrm{INP} 1 \times \mathrm{K}_{\mathrm{I}} \times \mathrm{R}_{\mathrm{Adj}}+\mathrm{V}_{\mathrm{HYS}}}{\mathrm{INP} 1}-\mathrm{R} 1 \tag{13}
\end{equation*}
$$

Equation (13) shows that if the output switches states when entering the diag mode with $\mathrm{V}_{\mathrm{RS}}=0$, the sensor impedance must be greater than the above calculated value. This can be very useful in diagnosing intermittent sensor.

## INPUT PROTECTION

As shown in Figure 2, an active clamp is provided on each input to limit the voltage on the input pin and prevent substrate current injection. The clamp is specified to handle $\pm 12 \mathrm{~mA}$. This puts an upper limit on the amplitude of the sensor output. For example, if R1 $=20 \mathrm{k}$, then

$$
\mathrm{V}_{\mathrm{RS}(\mathrm{MAX})}=20 \mathrm{k} \times 12 \mathrm{~mA}=240 \mathrm{~V}
$$

Therefore, the $\mathrm{V}_{\mathrm{RS}(\mathrm{pk}-\mathrm{pk})}$ voltage can be as high as 480 V . The CS1124 will typically run at a frequency up to 1.8 MHz if the input signal does not activate the positive or negative input clamps. Frequency performance will be lower when the positive or negative clamps are active. Typical performance will be up to a frequency of 680 kHz with the clamps active.

## CIRCUIT DESCRIPTION

Figure 3 shows the part operating near the minimum input thresholds. As the sin wave input threshold is increased, the low side clamps become active (Figure 4). Increasing the amplitude further (Figure 5), the high-side clamp becomes active. These internal clamps allow for voltages up to -250 V and 250 V on the sensor side of the setup (with $\mathrm{R} 1=\mathrm{R} 2=$ 22 k ) (reference the diagram page 3183).

Figure 6 shows the effect using the diagnostic (DIAG) function has on the circuit. The input threshold (negative) is switched from a threshold of -160 mV to +160 mV when DIAG goes from a low to a high. There is no hysteresis when DIAG is high.


Figure 3. Minimum Threshold Operation


Figure 4. Low-Side Clamp


Figure 5. Low- and High-Side Clamps


Figure 6. Diagnostic Operation

## CS1124

## APPLICATION INFORMATION

Referring to Figure 2, the following will be a design example given these system requirements:

$$
\begin{gathered}
\mathrm{R}_{\mathrm{RS}}=1.5 \mathrm{k} \Omega(>12 \mathrm{k} \Omega \text { is considered open }) \\
\mathrm{V}_{\mathrm{RS}}(\mathrm{MAX})=120 \mathrm{~V}_{\mathrm{pk}} \\
\mathrm{~V}_{\mathrm{RS}}(\mathrm{MIN})=250 \mathrm{mV}_{\mathrm{pk}} \\
\mathrm{FVRS}_{\mathrm{V}}=10 \mathrm{kHz} @ \mathrm{~V}_{\mathrm{RS}}(\mathrm{MIN})=40 \mathrm{~V}_{\mathrm{pk}-\mathrm{pk}}
\end{gathered}
$$

## 1. Determine tradeoff between R1 value and power

 rating. (use $1 / 2$ watt package)$$
\mathrm{PD}=\frac{\left(\frac{120}{\sqrt{2}}\right)^{2}}{\mathrm{R} 1}<1 / 2 \mathrm{~W}
$$

Set R1 $=15 \mathrm{k}$. (The clamp current will then be $120 / 15 \mathrm{k}$ $=8.0 \mathrm{~mA}$, which is less than the 12 mA limit.)

## 2. Determine $\mathbf{R}_{\text {Adj }}$

Set $R_{\text {Adj }}$ as close to $\mathrm{R} 1+\mathrm{R}_{\mathrm{RS}}$ as possible.
Therefore, $\mathrm{R}_{\mathrm{Adj}}=17 \mathrm{k}$.

## 3. Determine $\mathrm{V}_{\mathrm{RS}(+\mathrm{TRP})}$ using equation (7).

$$
\begin{aligned}
V_{R S}(+T R P)= & 11 \mu \mathrm{~A} \times 17 \mathrm{k}-11 \mu \mathrm{~A}(15 \mathrm{k}+1.5 \mathrm{k})+160 \mathrm{mV} \\
& V_{R S}(+ \text { TRP })=166 \mathrm{mV} \text { typical } \\
& \text { (easily meets } 250 \mathrm{mV} \text { minimum })
\end{aligned}
$$

## 4. Calculate worst case $\mathrm{V}_{\mathrm{RS}(+ \text { TRP) }}$

Examination of equation (7) and the spec reveals the worst case trip voltage will occur when:

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{HYS}}=180 \mathrm{mV} \\
& \mathrm{IN}_{\text {Adj }}=16 \mu \mathrm{~A} \\
& \text { INP1 }=15 \mu \mathrm{~A} \\
& \text { R1 }=14.25 \mathrm{k} \text { (5\% low) } \\
& \mathrm{R}_{\text {Adj }}=17.85 \mathrm{k}(5 \% \text { High }) \\
& \mathrm{V}_{\mathrm{RS}(+) \mathrm{MAX}}=16 \mu \mathrm{~A}(17.85 \mathrm{k}) \\
& -15 \mu \mathrm{~A}(14.25 \mathrm{k}+1.5 \mathrm{k})+180 \mathrm{mV} \\
& =229 \mathrm{mV}
\end{aligned}
$$

which is still less than the 250 mV minimum amplitude of the input.
5. Calculate $\mathbf{C 1}$ for low pass filtering

Since the sensor guarantees $40 \mathrm{~V}_{\mathrm{pk}-\mathrm{pk}} @ 10 \mathrm{kHz}$, a low pass filter using R1 and C1 can be used to eliminate high frequency noise without affecting system performance.

$$
\text { Gain Reduction }=\frac{0.29 \mathrm{~V}}{20 \mathrm{~V}}=0.0145=-36.7 \mathrm{~dB}
$$

Therefore, a cut-off frequency, $\mathrm{f}_{\mathrm{C}}$, of 145 Hz could be used.

$$
\mathrm{C} 1 \leq \frac{1}{2 \pi f \mathrm{CR} 1} \leq 0.07 \mu \mathrm{~F}
$$

Set $\mathrm{C} 1=0.047 \mu \mathrm{~F}$.
6. Calculate the minimum $R_{\text {RS }}$ that will be indicated as an open circuit. (DIAG = 5.0 V)

Rearranging equation (7) gives

$$
\mathrm{R}_{\mathrm{RS}}=\frac{\left[\begin{array}{l}
\mathrm{V}_{\mathrm{HYS}}+\left[\mathrm{INP} 1 \times \mathrm{K}_{\mathrm{I}} \times \mathrm{R}_{\text {Adj }}\right] \\
-\mathrm{V}_{\mathrm{RS}}(+\mathrm{TRP})
\end{array}\right]}{\mathrm{INP} 1}-\mathrm{R} 1
$$

But, $\mathrm{V}_{\mathrm{RS}}=0$ during this test, so it drops out.
Using the following as worst case Low and High:

|  | Worst Case Low ( $\mathbf{R}_{\text {RS }}$ ) | Worst Case High ( $\mathbf{R}_{\mathbf{R S}}$ ) |
| :---: | :---: | :---: |
| $\mathrm{IN}_{\text {Adj }}$ | $23.6 \mu \mathrm{~A}=15 \mu \mathrm{~A} \times 1.57$ | $10.7 \mu \mathrm{~A}=7.0 \mu \mathrm{~A} \times 1.53$ |
| $\mathrm{R}_{\text {Adj }}$ | 16.15 k | 17.85 k |
| $\mathrm{V}_{\mathrm{HYS}}$ | 135 mV | 185 mV |
| INP1 | $16 \mu \mathrm{~A}$ | $6.0 \mu \mathrm{~A}$ |
| R1 | 15.75 k | 14.25 k |
| K | 1.57 | 1.53 |

$$
\begin{aligned}
\mathrm{R}_{\mathrm{RS}} & =\frac{135 \mathrm{mV}+23.6 \mu \mathrm{~A} \times 16.15 \mathrm{k}}{16 \mu \mathrm{~A}}-15.75 \mathrm{k} \\
& =16.5 \mathrm{k}
\end{aligned}
$$

Therefore,

$$
\operatorname{RRS}(\mathrm{MIN})=16.5 \mathrm{k} \text { (meets } 12 \mathrm{k} \text { system spec) }
$$

and,

$$
\begin{aligned}
\operatorname{RRS}(\mathrm{MAX}) & =\frac{185 \mathrm{mV}+10.7 \mu \mathrm{~A} \times 17.85 \mathrm{k}}{6.0 \mu \mathrm{~A}}-14.25 \mathrm{k} \\
& =48.4 \mathrm{k}
\end{aligned}
$$

PACKAGE THERMAL DATA

| Parameter |  | SO-8 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 45 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 165 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## NCP5351

## Product Preview

## Synchronous Power MOSFET Driver

The NCP5351 is a dual MOSFET gate driver optimized to drive the gates of both high and low side Power MOSFETs in a Synchronous Buck converter. The NCP5351 is an excellent companion to multiphase controllers that do not have integrated gate drivers, such as ON Semiconductor's CS5323, CS5305 or CS5307. This architecture provides a power supply designer great flexibility by being able to locate the gate drivers close to the MOSFETs.

4 Amp drive capability makes the NCP5351 ideal for minimizing switching losses in MOSFETs with large input capacitance. Optimized internal, adaptive non-overlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate MOSFET drain voltages as high as 25 V . Both gate outputs can be driven low, and supply current reduced to less than $10 \mu \mathrm{~A}$, by applying a low logic level to the Enable (EN) pin. An Undervoltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with overtemperature protection.

The NCP5351 is pin-to-pin compatible with the SC1205 and is available in a standard SO-8 package.

## Features

- 4 A Peak Drive Current
- Rise and Fall Times Typically < 15 ns
- Propagation Delay from Inputs to Outputs < 20 ns Maximum
- Adaptive Non-Overlap Time Optimized for Power MOSFETs Switching > 20 A/Phase
- Floating Top Driver Accommodates Applications Up to 25 V
- Undervoltage Lockout to Prevent Switching When the Power Supply Is Unreliable
- Thermal Shutdown Protection Against Overtemperature
- <1 mA Quiescent Current - Enable (EN) Asserted (No Switching)
- <10 $\mu \mathrm{A}$ Quiescent Current - Enable (EN) Deasserted (Disables Switching)

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http://onsemi.com


PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| NCP5351D | SO-8 | 95 Units/Rail |
| NCP5351DR2 | SO-8 | 2500 Tape \& Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.


Figure 1. Block Diagram

Table 2. Input-Output Truth Table

| EN | CO | DRN | TG | BG |
| :---: | :---: | :---: | :---: | :---: |
| L | X | X | L | L |
| $H$ | L | $<0.5 \mathrm{~V}$ | L | H |
| $H$ | $H$ | $<0.5 \mathrm{~V}$ | $H$ | L |
| $H$ | L | $<0.5 \mathrm{~V}$ | L | H |
| $H$ | $H$ | $<0.5 \mathrm{~V}$ | H | L |
| $H$ | L | $>1.5 \mathrm{~V}$ | L | L |
| $H$ | $H$ | $>1.5 \mathrm{~V}$ | $H$ | L |
| $H$ | L | $>1.5 \mathrm{~V}$ | L | L |
| $H$ | $H$ | $>1.5 \mathrm{~V}$ | $H$ | L |

MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Operating Junction Temperature, $\mathrm{T}_{J}$ |  | Internally Limited | ${ }^{\circ} \mathrm{C}$ |
| Package Thermal Resistance: Junction to Case, R QJc Junction to Ambient, R धJA |  | $\begin{gathered} 45 \\ 165 \end{gathered}$ | $\begin{aligned} & \circ{ }^{\circ} \mathrm{C} / \mathrm{W} \\ & { }^{\circ} \mathrm{C} / \mathrm{W} \end{aligned}$ |
| Storage Temperature Range, $\mathrm{T}_{S}$ |  | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| ESD Susceptibility (Human Body Model) |  | 2.0 | kV |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 3) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

3. 60 seconds maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

## MAXIMUM RATINGS

| Pin Symbol | Pin Name | $\mathrm{V}_{\text {MAX }}$ | $\mathrm{V}_{\text {MIN }}$ | Isource | ISINK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{S}$ | Main Supply Voltage Input | 7.0 V | -0.3 V | NA | $\begin{gathered} \text { 4.0 A Peak }(<100 \mu \mathrm{~s}) \\ 250 \mathrm{~mA} \mathrm{DC} \end{gathered}$ |
| BST | Bootstrap Supply Voltage Input | 30 V wrt/PGND 7.0 V wrt/DRN | -0.3 V wrt/DRN | NA | $\begin{gathered} \text { 4.0 A Peak (< } 100 \mu \mathrm{~s}) \\ 250 \mathrm{~mA} \text { DC } \end{gathered}$ |
| DRN | Switching Node (Bootstrap Supply Return) | 25 V | $\begin{gathered} -1.0 \text { V DC } \\ -5.0 \mathrm{~V} \text { for } 100 \mathrm{~ns} \end{gathered}$ | $\begin{gathered} \text { 4.0 A Peak (< } 100 \mu \mathrm{~s}) \\ 250 \mathrm{~mA} \mathrm{DC} \end{gathered}$ | NA |
| TG | High Side Driver Output (Top Gate) | 30 V wrt/PGND 7.0 V wrt/DRN | -0.3 V wrt/DRN | $\begin{gathered} \text { 4.0 A Peak (<100 } \mu \mathrm{s}) \\ 250 \mathrm{~mA} \mathrm{DC} \end{gathered}$ | $\begin{gathered} \text { 4.0 A Peak (< } 100 \mu \mathrm{~s}) \\ 250 \mathrm{~mA} \text { DC } \end{gathered}$ |
| BG | Low Side Driver Output (Bottom Gate) | 7.0 V | -0.3 V | $\begin{gathered} \text { 4.0 A Peak (< } 100 \mu \mathrm{~s}) \\ 250 \mathrm{~mA} \text { DC } \end{gathered}$ | $\begin{gathered} \text { 4.0 A Peak (< } 100 \mu \mathrm{~s}) \\ 250 \mathrm{~mA} \text { DC } \end{gathered}$ |
| CO | TG \& BG Control Input | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| EN | Enable Input | 7.0 V | -0.3 V | 1.0 mA | 1.0 mA |
| PGND | Ground | 0 V | 0 V | $\begin{gathered} \text { 4.0 A Peak }(<100 \mu \mathrm{~s}) \\ 250 \mathrm{~mA} \mathrm{DC} \end{gathered}$ | NA |

NOTE: All voltages are with respect to PGND except where noted.

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{S}}<5.5 \mathrm{~V} ; 4.0 \mathrm{~V}<\mathrm{V}_{\mathrm{BST}}<26 \mathrm{~V} ; \mathrm{V}_{\mathrm{EN}}=\mathrm{V}_{\mathrm{S}}\right.$; unless otherwise noted.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DC OPERATING SPECIFICATIONS Power Supply |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{S}}$ Quiescent Current, Operating | $\mathrm{V}_{\mathrm{CO}}=0 \mathrm{~V}, 4.5 \mathrm{~V}$; No output switching | - | 1.0 | - | mA |
| $\mathrm{V}_{\text {BST }}$ Quiescent Current, Operating | $\mathrm{V}_{\mathrm{CO}}=0 \mathrm{~V}, 4.5 \mathrm{~V}$; No output switching | - | 50 | - | $\mu \mathrm{A}$ |
| Quiescent Current, Non-Operating | $\mathrm{V}_{\mathrm{EN}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{CO}}=0 \mathrm{~V}, 4.5 \mathrm{~V}$ | - | - | 10 | $\mu \mathrm{A}$ |

## Undervoltage Lockout

| Start Threshold | $\mathrm{CO}=0 \mathrm{~V}$ | 4.2 | 4.35 | 4.5 | V |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Stop Threshold | $\mathrm{CO}=0 \mathrm{~V}$ | 4.1 | 4.28 | 4.45 | V |
| Hysteresis | $\mathrm{CO}=0 \mathrm{~V}$ | 0.05 | 0.07 | 0.1 | V |

## CO Input Characteristics

| High Threshold | - | 2.0 | - | - | V |  |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| Low Threshold |  | - | - | - | 0.8 | V |
| Input Bias Current | $0<\mathrm{V}_{\mathrm{CO}}<\mathrm{V}_{\mathrm{S}}$ | - | 0 | 10 | $\mu \mathrm{~A}$ |  |

## EN Input Characteristics

| High Threshold | Both drivers respond to CO | 2.0 | - | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Low Threshold | Both drivers are low independent of CO | - | - | 0.8 | V |
| Input Bias Current | $0<\mathrm{V}_{\mathrm{EN}}<\mathrm{V}_{\mathrm{S}}$ | - | 0 | 10 | $\mu \mathrm{~A}$ |

## Thermal Shutdown

| Overtemperature Trip Point | Note 4. | - | 170 | - | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Recovery Temperature | Note 4. | 125 | - | - | ${ }^{\circ} \mathrm{C}$ |
| Hysteresis | Note 4. | - | 30 | - | ${ }^{\circ} \mathrm{C}$ |

High Side Driver

| Peak Output Current | Note 4. | - | 4.0 | - | A |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Resistance (Sourcing) (Note 4) | $\begin{aligned} & \text { Duty Cycle }<2.0 \%, \text { Pulse Width }<100 \mu \mathrm{~s}, \\ & T_{J}=125^{\circ} \mathrm{C}, \mathrm{~V}_{\text {BST }}-\mathrm{V}_{\text {DRN }}=4.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{TG}}=4.0 \mathrm{~V}+\mathrm{V}_{\text {DRN }} \end{aligned}$ | - | 0.5 | - | $\Omega$ |
| Output Resistance (Sinking) (Note 4) | $\begin{aligned} & \text { Duty Cycle }<2.0 \%, \text { Pulse Width }<100 \mu \mathrm{~s}, \\ & T_{J}=125^{\circ} \mathrm{C}, \mathrm{~V}_{\text {BST }}-\mathrm{V}_{\text {DRN }}=4.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{TG}}=0.5 \mathrm{~V}+\mathrm{V}_{\text {DRN }} \end{aligned}$ | - | 0.35 | - | $\Omega$ |

## Low Side Driver

| Peak Output Current | Note 4. | - | 4.0 | - | A |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Output Resistance (Sourcing) <br> (Note 4) | Duty Cycle $<2.0 \%$, Pulse Width $<100 \mu \mathrm{~s}$, <br> $\mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{BG}}=4.0 \mathrm{~V}$ | - | 0.6 | - | $\Omega$ |
| Output Resistance (Sinking) <br> (Note 4) | Duty $\mathrm{Cycle}<2.0 \%$, Pulse Width $<100 \mu \mathrm{~s}$, <br> $\mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{S}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{BG}}=0.5 \mathrm{~V}$ | - | 0.5 | - | $\Omega$ |

4. Guaranteed by design, not $100 \%$ tested in production.

ELECTRICAL CHARACTERISTICS $\left(0^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<125^{\circ} \mathrm{C} ; 4.5 \mathrm{~V}<\mathrm{V}_{\mathrm{S}}<5.5 \mathrm{~V} ; 4.0 \mathrm{~V}<\mathrm{V}_{\mathrm{BST}}<26 \mathrm{~V} ; \mathrm{V}_{\mathrm{EN}}=\mathrm{V}_{\mathrm{S}}, \mathrm{C}_{\mathrm{LOAD}}=6.0 \mathrm{nF}\right.$; unless otherwise noted.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

AC OPERATING SPECIFICATIONS
High Side Driver

| Rise Time | $\operatorname{tr}_{T G}$ | $\mathrm{~V}_{\mathrm{BST}}-\mathrm{V}_{\mathrm{DRN}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}=5.0 \mathrm{~V}$ | - | 8.0 | 16 | ns |
| :--- | :---: | :--- | :---: | :---: | :---: | :---: |
| Fall Time | $\mathrm{tf}_{\mathrm{TG}}$ | $\mathrm{V}_{\mathrm{BST}}-\mathrm{V}_{\mathrm{DRN}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}=5.0 \mathrm{~V}$ | - | 14 | 21 | ns |
| Propagation Delay Time, <br> TG Going High <br> (Non-Overlap Time) | $\operatorname{tpdh}_{\mathrm{TG}}$ | $\mathrm{V}_{\mathrm{BST}}-\mathrm{V}_{\text {DRN }}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}=5.0 \mathrm{~V}$ | 30 | 55 | 100 | ns |
| Propagation Delay Time, <br> TG Going Low | tpdl $_{\mathrm{TG}}$ | $\mathrm{V}_{\mathrm{BST}}-\mathrm{V}_{\mathrm{DRN}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{S}}=5.0 \mathrm{~V}$ | - | 18 | 37 | ns |

## Low Side Driver

| Rise Time | $\operatorname{tr}_{\mathrm{BG}}$ | $\mathrm{V}_{\mathrm{S}}=4.5 \mathrm{~V}$ | - | 10 | 15 | ns |
| :--- | :---: | :--- | :---: | :---: | :---: | :---: |
| Fall Time | $\mathrm{tf}_{\mathrm{BG}}$ | $\mathrm{V}_{\mathrm{S}}=4.5 \mathrm{~V}$ | - | 12 | 20 | ns |
| Propagation Delay Time, <br> BG Going High <br> (Non-Overlap Time) | $\operatorname{tpdh}_{\mathrm{BG}}$ | $\mathrm{V}_{\mathrm{S}}=4.5 \mathrm{~V}$ | 30 | 55 | 100 | ns |
| Propagation Delay Time, <br> BG Going Low | tpdl $_{\mathrm{BG}}$ | $\mathrm{V}_{\mathrm{S}}=4.5 \mathrm{~V}$ | - | 10 | 18 | ns |

Undervoltage Lockout

| $\mathrm{V}_{\mathrm{S}}$ Rising | tpdh UVLO | $\mathrm{EN}=\mathrm{V}_{\mathrm{S}}, \mathrm{CO}=0 \mathrm{~V}, \mathrm{dV} / \mathrm{dt}>1.0 \mathrm{~V} / \mu \mathrm{s}$, <br> from 4.0 V to 4.5 V, time to $\mathrm{BG}>1.0 \mathrm{~V}$ | - | 10 | - | $\mu \mathrm{s}$ |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{S}}$ Falling | tpdl UVLO | $\mathrm{EN}=\mathrm{V}_{\mathrm{S}}, \mathrm{CO}=0 \mathrm{~V}, \mathrm{dV} / \mathrm{dt}<-1.0 \mathrm{~V} / \mu \mathrm{s}$, <br> from 4.5 V to 4.0 V, time to $\mathrm{BG}<1.0 \mathrm{~V}$ | - | 10 | - | $\mu \mathrm{s}$ |



Figure 2. Timing Diagram

## PACKAGE PIN DESCRIPTION

| Pin Number | Pin Symbol | Description |
| :---: | :---: | :---: |
| 1 | DRN | The switching node common to the high and low-side FETs. The high-side (TG) driver and supply (BST) are referenced to this pin. |
| 2 | TG | Driver output to the high-side MOSFET gate. |
| 3 | BST | Bootstrap supply voltage input. In conjunction with a Schottky diode to $\mathrm{V}_{\mathrm{S}}$, a $0.1 \mu \mathrm{~F}$ to $1.0 \mu \mathrm{~F}$ ceramic capacitor connected between BST and DRN develops supply voltage for the high-side driver (TG). |
| 4 | CO | Logic level control input produces complementary output states - no inversion at TG; inversion at BG. |
| 5 | EN | Logic level enable input forces TG and BG low, and supply current to less than $10 \mu \mathrm{~A}$ when EN is low. |
| 6 | $\mathrm{V}_{\text {S }}$ | Power supply input. A $0.1 \mu \mathrm{~F}$ to $1.0 \mu \mathrm{~F}$ ceramic capacitor should be connected from this pin to PGND. |
| 7 | BG | Driver output to the low-side (synchronous rectifier) MOSFET gate. |
| 8 | PGND | Ground. |



Figure 3. Application Diagram

## CS3361

## Alternator Voltage Regulator FET Driver

The CS3361 integral alternator regulator integrated circuit provides the voltage regulation for automotive, 3-phase alternators.

It drives an external logic level N channel enhancement power FET for control of the alternator field current. In the event of a charge fault, a lamp output pin is provided to drive an external darlington transistor capable of switching on a fault indicator lamp. An overvoltage or no Stator signal condition activates the lamp output.

A STATOR Power Up feature is incorporated for systems which require power up activation by sensing the crank cycle of the starter at the stator. This eliminates unnecessary current drain when the ignition is turned on, but the car is not running. The CS3361 is available in an SO-14 package.

## Features

- Drives Logic Level Power NFET
- 80 V Load Dump
- Temperature Compensated Regulation Voltage
- Shorted Field Protection Duty Cycle, Self Clearing
- STATOR Power Up


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PIN CONNECTIONS AND
MARKING DIAGRAM


A
= Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| CS3361YD14 | SO-14 | 55 Units/Rail |
| CS3361YDR14 | SO-14 | 2500 Tape \& Reel |

CS3361


Figure 1. Block Diagram

## MAXIMUM RATINGS*

| Rating |  | Value | Unit |
| :---: | :---: | :---: | :---: |
| Storage Temperature Range, $\mathrm{T}_{\mathrm{S}}$ |  | -55 to +165 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature Range |  | -40 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Continuous Supply |  | 27 | V |
| ICC Load Dump (@ $\mathrm{V}_{\text {CC }}=80 \mathrm{~V}_{\text {peak }}$ ) |  | 400 | mA |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | ${ }^{\circ} \mathrm{C}$ |

1. 60 second maximum above $183^{\circ} \mathrm{C}$.
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}, 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 17 \mathrm{~V}\right.$;
unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Supply |  |  |  |  |  |
| Supply Current Enabled | - | - | - | 10 | mA |
| Supply Current Disabled | - | - | - | 50 | $\mu \mathrm{A}$ |

## Driver Stage

| Output High Voltage | - | 5.5 | - | 12 | V |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Low Voltage | $\mathrm{l} \mathrm{OL}=25 \mu \mathrm{~A}$ | - | - | 0.35 | V |
| Output High Current | $V_{D D}=1.2 \mathrm{~V}$ | -10 | -6.0 | -4.0 | mA |
| Minimum ON Time | $\mathrm{C}_{\text {OSC }}=0.022 \mu \mathrm{~F}$ | 200 | - | - | $\mu \mathrm{s}$ |
| Minimum Duty Cycle | - | - | 6.0 | 10 | \% |
| Short Circuit Duty Cycle | - | 1.0 | - | 5.0 | \% |
| Field Switch Turn On Rise Time | - | 15 | - | 75 | $\mu \mathrm{s}$ |
| Field Switch Turn On Fall Time | - | 15 | - | 75 | $\mu \mathrm{s}$ |

## Stator

| Input High Voltage | - | 10 | - | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Low Voltage | - | - | - | 6.0 | V |
| Stator Time Out | High to Low | 6.0 | 100 | 600 | ms |

## Lamp

| Output High Current | $V_{\text {LAMP }} @ 3.0 \mathrm{~V}$ | - | - | 50 | $\mu \mathrm{~A}$ |
| :--- | :--- | :--- | :--- | :---: | :---: |
| Output Low Voltage | ILAMP @ 30 mA | - | - | 0.35 | V |

## Ignition

| Input High Voltage | $\mathrm{I}_{\mathrm{CC}}>1.0 \mathrm{~mA}$ | 1.8 | - | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Low Voltage | $\mathrm{I}_{\mathrm{CC}}<100 \mu \mathrm{~A}$ | - | - | 0.5 | V |

## Oscillator

| Oscillator Frequency | C OSC $=0.022 \mu \mathrm{~F}$ | 90 | - | 210 | Hz |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Rise Time/Fall Time | $\mathrm{C}_{\text {OSC }}=0.022 \mu \mathrm{~F}$ | - | 17 | - | - |
| Oscillator High Threshold | C OSC $=0.022 \mu \mathrm{~F}$ | - | - | 4.5 | V |

ELECTRICAL CHARACTERISTICS (continued) $\left(-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<125^{\circ} \mathrm{C},-40^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{J}}<150^{\circ} \mathrm{C}, 9.0 \mathrm{~V} \leq \mathrm{V}_{\mathrm{CC}} \leq 17 \mathrm{~V}\right.$; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

Battery Sense

| Input Current | - | -10 | - | +10 | $\mu \mathrm{~A}$ |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Regulation Voltage | $@ 25^{\circ} \mathrm{C}, \mathrm{R}_{1}=100 \mathrm{k} \Omega, \mathrm{R}_{2}=50 \mathrm{k} \Omega$ | 13.8 | - | 15.8 | V |
| Proportional Control | - | 0.10 | - | 0.25 | V |
| High Voltage Threshold Ratio | $\frac{\text { VHigh Voltage@LampOn }}{} \mathrm{V}$ Regulation@50\%Duty Cycle | 1.083 | - | 1.190 | $\mathrm{~V} / \mathrm{V}$ |
| High Voltage Hysteresis | - | 0.020 | - | 0.600 | V |

## PACKAGE PIN DESCRIPTION

| PACKAGE PIN \# |  |  |
| :---: | :---: | :--- |
| SO-14 | PIN SYMBOL |  |
| 1 | Driver | Output driver for external power switch. |
| 2 | GND | Ground. |
| $3,6,7,9,13$ | NC | No Connection. |
| 4 | OSC | Timing capacitor for oscillator. |
| 5 | Lamp | Base driver for lamp driver indicates no stator signal or overvoltage condition. |
| 8 | IGN | Switched ignition power up. |
| 10 | Stator | Stator signal input for stator timer. |
| 11 | Sense | Battery sense voltage regulator comparator input and protection. |
| 12 | SC | Supply for IC. |
| 14 |  | Short circuit sensing. |

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 2. CS3361 Battery Voltage vs. Temperature
$\left({ }^{\circ} \mathrm{C}\right)$ Over Process Variation

## APPLICATIONS INFORMATION

The CS3361 is designed for use in an alternator charging system.

In a standard alternator design (Figure 3), the rotor carries the field winding. An alternator rotor usually has several N and $S$ poles. The magnetic field for the rotor is produced by forcing current through a field or rotor winding. The Stator windings are formed into a number of coils spaced around a cylindrical core. The number of coils equals the number of pairs of N and S poles on the rotor. The alternating current in the Stator windings is rectified by the diodes and applied to the regulator. By controlling the amount of field current, the magnetic field strength is controlled and hence the output voltage of the alternator.

Referring to Figure 4, a typical application diagram, the oscillator frequency is set by an external capacitor connected between OSC and ground. The sawtooth waveform ramps between 1.0 V and 3.0 V and provides the timing for the system. For the circuit shown the oscillator frequency is approximately 140 Hz . The alternator voltage is sensed at Terminal A via the resistor divider network R1/R2 on the Sense pin of the IC. The voltage at the sense pin determines the duty cycle for the regulator. The voltage is adjusted by potentiometer R2. A relatively low voltage on the sense pin causes a long duty cycle that increases the Field current. A high voltage results in a short duty cycle.

The ignition Terminal (I) switches power to the IC through the $\mathrm{V}_{\mathrm{CC}}$ pin. The Stator pin monitors the voltage from the stator and senses a stopped engine condition. It drives the Lamp pin high after the stator timeout expires. The Lamp pin also goes high when an overvoltage condition
is detected on the sense pin. This causes the darlington lamp drive transistor to switch on and pull current through the lamp. If the system voltage continues to increase, the field and lamp output turn off as in an overvoltage or load dump condition.
The SC or Short Circuit pin monitors the field voltage. If the drive output and the SC voltage are simultaneously high for a predetermined period, a short circuit condition is assumed and the output is disabled. The regulator is forced to a minimum short circuit duty cycle.


Figure 3. IAR System Block Diagram


Figure 4. Typical Application Dlagram

PACKAGE THERMAL DATA

| Parameter |  | SO-14 | Unit |
| :--- | :---: | :---: | :---: |
| $R_{\text {©JC }}$ | Typical | 30 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| $R_{\text {©JA }}$ | Typical | 125 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## MC34280

## Power Supply \&

Management IC for Handheld Electronic Products

The MC34280 is a power supply integrated circuit which provides two boost regulated outputs and some power management supervisory functions. Both regulators apply Pulse-Frequency-Modulation (PFM). The main step-up regulator output can be externally adjusted from 2.7 V to 5 V . An internal synchronous rectifier is used to ensure high efficiency (achieve 87\%). The auxiliary regulator with a built-in power transistor can be configured to produce a wide range of positive voltage (can be used for LCD contrast voltage). This voltage can be adjusted from +5 V to +25 V by an external potentiometer; or by a microprocessor, digitally through a 6 -bit internal DAC.

The MC34280 has been designed for battery powered hand-held products. With the low start-up voltage from 1 V and the low quiescent current (typical $35 \mu \mathrm{~A}$ ); the MC34280 is best suited to operate from 1 to 2 AA/ AAA cell. Moreover, supervisory functions such as low battery detection, CPU power-on reset, and back-up battery control, are also included in the chip. It makes the MC34280 the best one-chip power management solution for applications such as electronic organizers and PDAs.

## FEATURES:

- Low Input Voltage, 1V up
- Low Quiescent Current in Standby Mode: $35 \mu$ A typical
- PFM and Synchronous Rectification to ensure high efficiency ( $87 \%$ @ 200 mA Load)
- Adjustable Main Output: nominal 3.3V @ 200mA max, with 1.8 V input
- Auxiliary Output Voltage can be digitally controlled by microprocessor
- Auxiliary Output Voltage: $+5 \mathrm{~V} @ 25 \mathrm{~mA}$ max, with 1.8 V input +25 V @ 15 mA max, with 1.8 V input
- Current Limit Protection
- Power-ON Reset Signal with Programmable Delay
- Battery Low Detection
- Lithium Battery Back-up
- 32-Pin LQFP Package


## APPLICATIONS:

- Digital Organizer and Dictionary
- Personal Digital Assistance (PDA)
- Dual Output Power Supply (For MPU, Logic, Memory, LCD)
- Handheld Battery Powered Device (1-2 AA/AAA cell)


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PIN CONNECTIONS


## ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC34280FTB | LQFP | 250 Units/Tray |
| MC34280FTBR2 | LQFP | 1800 Tape \& Reel |



Figure 1. Typical Application Block Diagram

TIMING DIAGRAMS


Figure 2. Startup Timing


Figure 3. Power Down Timing

## TIMING DIAGRAMS (Con't)



Figure 4. Auxiliary Regulator Voltage Control


Figure 5. Auxiliary Regulator Voltage Control Timing

MC34280

PIN FUNCTION DESCRIPTION

| Pin <br> No. | Function | Type/Direction | Description |
| :---: | :---: | :---: | :---: |
| 1 | VMAINFB | Analog / Input | Feedback pin for VMAIN |
| 2 | VBAT | Power | Main battery supply |
| 3 | ENABLE | CMOS / Input | Chip enable, Active high, ENABLE activates VMAIN after battery plug in, ENABLE is inactive after VMAIN is on |
| 4 | VDD | Analog / Output | Connect to decoupling capacitor for internal logic supply |
| 5 | PDELAY | Analog / Input | Capacitor connection for defining Power-On signal delay |
| 6 | VREF | Analog / Output | Bandgap Reference output voltage. Nominal voltage is 1.25 V |
| 7 | AGND | Analog Ground |  |
| 8 | IREF | Analog / Input | Resistor connection for defining internal current bias and PDELAY current |
| 9 | LOWBATSEN | Analog / Input | Resistive network connection for defining low battery detect threshold |
| 10 | DGND | Digital Ground |  |
| 11 | PORB | CMOS / Output | Active LOW Power-On reset signal |
| 12 | LOWBATB | CMOS / Output | Active LOW low battery detect output |
| 13 | LIBATON | CMOS / Input | microprocessor control signal for Lithium battery backup switch, the switch is ON when LIBATON=HIGH and LIBATCL=HIGH |
| 14 | LIBATCL | CMOS / Input | microprocessor control signal for Lithium battery backup switch, if it is HIGH, the switch is controlled by LIBATON, otherwise, controlled by internal logic |
| 15 | VAUXADJ | CMOS / Input | microprocessor control signal for VAUX voltage control |
| 16 | VAUXCON | CMOS / Input | microprocessor control signal for VAUX voltage control |
| 17 | VAUXEN | CMOS / Input | VAUX enable, Active high |
| 18 | VAUXFBP | Analog / Input | Feedback pin for VAUX |
| 19 | VAUXREF | Analog / Output | Reference Voltage for VAUX voltage level |
| 20 | VAUXFBN | Analog / Input | Feedback pin for VAUX |
| 21 | VAUXBDV | Power | VAUX BJT base drive circuit power supply |
| 22 | VAUXCHG | Analog / Output | test pin |
| 23 | VAUXBASE | Analog / Output | test pin |
| 24 | NC |  | no connection |
| 25 | VAUXSW | Analog / Output | Collector output of the VAUX power BJT |
| 26 | VAUXEMR | Analog / Output | Emitter output of the VAUX power BJT |
| 27 | LIBATIN | Analog / Input | Lithium battery input for backup purposes |
| 28 | LIBATOUT | Analog / Output | Lithium battery output |
| 29 | NC |  | no connection |
| 30 | VMAINGND | Power Ground | Ground for VMAIN Iow side switch |
| 31 | VMAINSW | Analog / Input | VMAIN inductor connection |
| 32 | VMAIN | Analog / Output | VMAIN output |

ABSOLUTE MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Parameter | Symbol | Min | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\text {BAT }}$ | -0.3 | 7.0 | Vdc |
| Digital Pin Voltage | $\mathrm{V}_{\text {digital }}$ | -0.3 | 7.0 | Vdc |
| General Analog Pin Voltage | $\mathrm{V}_{\text {analog }}$ | -0.3 | 7.0 | Vdc |
| Pin VAUXSW to Pin VAUXEMR Voltage (Continuous) | $\mathrm{V}_{\text {AUXCE }}$ | -0.3 | 30 | Vdc |
| Pin VMAINSW to Pin VMAIN Voltage (Continuous) | $\mathrm{V}_{\text {syn }}$ |  | 0.3 | Vdc |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{j}(\max )}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Ambient Operating Temperature | $\mathrm{T}_{\mathrm{a}}$ | 0 | 70 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -50 | 150 | ${ }^{\circ} \mathrm{C}$ |

STATIC ELECTRICAL CHARACTERISTICS (Circuit of Figure 1, $\mathrm{VP}=1.8 \mathrm{~V}, \mathrm{l}_{\mathrm{load}}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise noted.)

| Rating | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Supply Voltage ${ }^{1}$ | $\mathrm{V}_{\text {BAT }}$ | 1.0 |  |  | V |
| VMAIN output voltage | $V_{\text {main }}$ | 3.13 | 3.3 | 3.47 | V |
| VMAIN output voltage range ${ }^{2}$ | $\mathrm{V}_{\text {main_range }}$ | 2.7 |  | 5.0 | V |
| VMAIN output current ${ }^{3}$ | $\mathrm{I}_{3.3} 1.8$ |  |  | 200 | mA |
| VMAIN maximum switching frequency ${ }^{4}$ | Freqmax_VM |  |  | 100 | kHz |
| VMAIN peak coil static current limit | lıIM_Vm | 0.85 | 1.0 | 1.15 | A |
| VAUX output voltage range | VAUX_range | 5.0 |  | 25 | V |
| VAUXREF lower level voltage | VAUX ${ }_{\text {REF_L }}$ | 1.0 | 1.1 | 1.2 | V |
| VAUXREF upper level voltage | VAUX ${ }_{\text {REF_H }}$ | 2.0 | 2.2 | 2.4 | V |
| VAUXREF step size | VAUX ${ }_{\text {REF_S }}$ |  | 17 |  | mV |
| VAUX maximum switching frequency | Freqmax_VL $^{\text {a }}$ |  |  | 120 | kHz |
| VAUX peak coil static current limit | ILIM_VL |  | 1.0 |  | A |
| Quiescent Supply Current at Standby Mode ${ }^{5}$ | $1 \mathrm{I}_{\text {standby }}$ |  | 35 | 60 | $\mu \mathrm{A}$ |
| Reference Voltage @ no load | Vref ${ }_{\text {no_load }}$ | 1.16 | 1.22 | 1.28 | V |
| Battery Low Detect lower hysteresis threshold ${ }^{6}$ | V Lobat_L | 0.8 | 0.85 | 0.9 | V |
| Battery Low Detect upper hysteresis threshold | V Lobat_h | 1.05 | 1.1 | 1.15 | V |
| PDELAY Pin output charging current | Ichgrdelay | 0.8 | 1.0 | 1.2 | $\mu \mathrm{A}$ |
| PDELAY Pin voltage threshold | Vth ${ }_{\text {PDELAY }}$ | 1.16 | 1.22 | 1.28 | V |

NOTE: 1. Output current capability is reduced with supply voltage due to decreased energy transfer. The supply voltage must not be higher than VMAIN +0.6 V to ensure boost operation. Max Start-up loading is typically 1 V at $400 \mu \mathrm{~A}, 1.8 \mathrm{~V}$ at 4.4 mA , and 2.2 V at 88 mA .
NOTE: 2. Output voltage can be adjusted by external resistor to the VMAINFB pin.
NOTE: 3. At VBAT $=1.8 \mathrm{~V}$, output current capability increases with VBAT.
NOTE: 4. Only when current limit is not reached.
NOTE: 5. This is average current consumed by the IC from VDD, which is low-pass filtered from VMAIN, when only VMAIN is enabled and at no loading.
NOTE: 6. This is the minimum of "LOWBATB" threshold for battery voltage, the threshold can be increased by external resistor divider from "VBAT" to "LOWBATSEN".

DYNAMIC ELECTRICAL CHARACTERISTICS (Refer to TIMING DIAGRAMS, $T_{A}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise noted.)

| Rating | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum PORB to Control delay | $\mathrm{t}_{\text {PORC }}$ |  |  | 500 | nS |
| Minimum VAUXCON pulse HIGH width | $\mathrm{t}_{\mathrm{CW}}$ |  |  | 5.0 | $\mu \mathrm{~S}$ |
| Minimum VAUXCON pulse LOW width | $\mathrm{t}_{\mathrm{CC}}$ |  |  | 8.0 | $\mu \mathrm{~S}$ |
| Minimum VAUXADJ to VAUXCON delay | $\mathrm{t}_{\mathrm{CL}}$ |  |  | 1.0 | $\mu \mathrm{~S}$ |
| Minimum VAUXADJ pulse HIGH width | $\mathrm{t}_{\mathrm{JW}}$ |  |  | 1.0 | $\mu \mathrm{~S}$ |
| Minimum VAUXADJ pulse LOW width | $\mathrm{t}_{\mathrm{JC}}$ |  |  | 1.0 | $\mu \mathrm{~S}$ |
| Minimum VAUXCON LOW to VAUXADJ pulse delay ${ }^{1}$ | $\mathrm{t}_{\mathrm{JL}}$ |  |  | 1.0 | $\mu \mathrm{~S}$ |
| Minimum hold time of VAUXADJ for Reset VAUXREF | $\mathrm{t}_{\text {RJL }}$ |  |  | 500 | nS |
| Minimum VAUXADJ pulse HIGH width for Reset VAUXREF | $\mathrm{t}_{\text {RW }}$ |  |  | 1.0 | $\mu \mathrm{~S}$ |
| Minimum hold time of VAUXADJ for Decrement VAUXREF | $\mathrm{t}_{\mathrm{DL}}$ |  |  | 500 | nS |
| Minimum VAUXADJ pulse HIGH width for Decrement VAUXREF | $\mathrm{t}_{\mathrm{DW}}$ |  |  | 1.0 | $\mu \mathrm{~S}$ |

NOTE: 1. For not resetting VAUXREF.
TYPICAL ELECTRICAL CHARACTERISTICS


Figure 6. Efficiency of VMAIN versus Output Current (VMAIN $=3.3 \mathrm{~V}, \mathrm{~L}=33 \mathrm{uH}$, Various $\mathrm{V}_{\mathrm{IN}}$ )


Figure 8. Efficiency of VAUX versus Output Current (VAUX = 25 V, L2 = 33 uH , Various $\mathrm{V}_{\mathrm{IN}}$ )


Figure 7. Efficiency of VMAIN versus Input Voltage (VMAIN = 3.3 V, L1 = 33 uH , Various lout)


Figure 9. Efficiency of VAUX versus Input Voltage (VAUX = 25 V , L2 = 33 uH , Various IOUT)

TYPICAL ELECTRICAL CHARACTERISTICS (Cont'd)


Figure 10. Efficiency of VAUX versus Output Current (VAUX = 20 V, L2 = $\mathbf{3 3} \mathbf{u H}$, Various VIN)


Figure 12. Efficiency of VAUX versus Output Current (VAUX = 5 V, L2 = 82 uH , Various VIN)


Figure 11. Efficiency of VAUX versus Input Voltage (VAUX = $20 \mathrm{~V}, \mathrm{~L} 2=33 \mathrm{uH}$, Various IOUT)


Figure 13. Efficiency of VAUX versus Input Voltage (VAUX = 5 V, L2 = 82 uH , Various IOUT)


20 uS / div
1: VMAIN $=3.3 \mathrm{~V}(50 \mathrm{mV} / \mathrm{div}, \mathrm{AC}$ COUPLED $)$
2: Voltage at VMAINSW (1 V/div)
Figure 14. VMAIN Output Ripple (Medium Load)


Figure 16. VAUX Output Ripple (Medium Load)


Figure 18. VMAIN Startup and Power-On Reset


10 uS / div
1: VMAIN $=3.3 \mathrm{~V}(50 \mathrm{mV} /$ div, AC COUPLED $)$
2: Voltage at VMAINSW (1 V/div)
Figure 15. VMAIN Output Ripple (Heavy Load)


Figure 17. VAUX Output Ripple (Heavy Load)


## DETAILED OPERATING DESCRIPTION

## General

The MC34280 is a power supply integrated circuit which provides two boost regulated outputs and some power management supervisory functions. Both regulators apply Pulse-Frequency-Modulation (PFM). The main boost regulator output can be externally adjusted from 2.7 V to 5 V . An internal synchronous rectifier is used to ensure high efficiency (achieve $87 \%$ ). The auxiliary regulator with a built-in power transistor can be configured to produce a wide range of positive voltage (can be used to supply a LCD contrast voltage). This voltage can be adjusted from +5 V to +25 V by an external potentiometer; or by a microprocessor, digitally through a 6-bit internal DAC.

The MC34280 has been designed for battery powered hand-held products. With the low start-up voltage from 1V and the low quiescent current (typical $35 \mu \mathrm{~A}$ ); the MC34280 is best suited to operate from 1 to $2 \mathrm{AA} / \mathrm{AAA}$ cell. Moreover, supervisory functions such as low battery detection, CPU power-on reset, and back-up battery control, are also included in the chip. It makes the MC34280 the best one-chip power management solution for applications such as electronic organizers and PDAs.

## Pulse Frequency Modulation (PFM)

Both regulators apply PFM. With this switching scheme, every cycle is started as the feedback voltage is lower than the internal reference. This is normally performed by internal comparator. As cycle starts, Low-Side switch (i.e. M1 in Figure 1) is turned ON for a fixed ON time duration (namely, $\mathrm{T}_{\mathrm{on}}$ ) unless current limit comparator senses coil current reaches its preset limit. In the latter case, M1 is OFF instantly. So $\mathrm{T}_{\mathrm{on}}$ is defined as the maximum ON time of M1. When M1 is ON, coil current ramps up so energy is being stored inside the coil. At the moment just after M1 is OFF, the Synchronous Rectifier (i.e. M2 in Figure 1) or any rectification device (such as Schottky Diode of Auxiliary Regulator) is turned ON to direct coil current to charge up the output bulk capacitor. Provided that coil current is not reached, every switching cycle delivers fixed amount of energy to the bulk capacitor. So for higher loading, larger amount of energy (Charge) is withdrawn from the bulk capacitor, and as output voltage is needed to regulated, larger amount of Charge is needed to be supplied to the bulk capacitor, that means switching frequency is needed to be increased; and vice-versa.

## Main Regulator

Figure 20 shows the simplified block diagram of Main Regulator. Notice that precise bias current Iref is generated by a VI converter and external resistor RIref, where

$$
\text { Iref }=\frac{0.5}{\text { RIref }}(\mathrm{A})
$$

This bias current is used for all internal current bias as well as setting VMAIN value. For the latter application, Iref is doubled and fed as current sink at Pin 1. With external resistor RMAINb tied from Pin1 to Pin32, a constant level shift is generated in between the two pins. In close-loop operation, voltage at Pin 1 (i.e. Output feedback voltage) is needed to be regulated at the internal reference voltage level, 1.22 V . Therefore, the delta voltage across Pin 1 and Pin 32 which can be adjusted by RMAINb determines the Main Output voltage. If the feedback voltage drops below 1.22 V , internal comparator sets switching cycle to start. So, VMAIN can be calculated as follows.


From the above equation, although VMAIN can be adjusted by RMAINb and RIref ratio, for setting VMAIN, it is suggested, by changing RMAINb value with RIref kept at 480K. Since changing RIref will alter internal bias current which will affect timing functions of Max ON time ( $T_{O N 1}$ ) and Min OFF time ( $T_{O F F 1}$ ). Their relationships are as follows;

$$
\begin{aligned}
& T_{O N 1}=1.7 \times 10^{-11} \times \text { RIref }(\mathrm{S}) \\
& T_{O F F 1}=6.4 \times 10^{-12} \times \text { RIref }(\mathrm{S})
\end{aligned}
$$

## Continuous Conduction Mode and Discontinuous Conduction Mode

In Figure 21, regulator is operating at Continuous Conduction Mode. A switching cycle is started as the output feedback voltage drops below internal voltage reference VREF. At that instant, the coil current does not drop to zero yet, and it starts to ramp up for the next cycle. As the coil current ramps up, loading makes the output voltage to decrease as the energy supply path to the output bulk capacitor is disconnected. And after Ton elapsed, M1 is OFF, M2 becomes ON, energy is dumped to the bulk capacitor. Output voltage is increased as excessive charge is pumped in, then it is decreased after the coil current drops below the loading. Notice the abrupt spike of output voltage is due to ESR of the bulk capacitor. Feedback voltage can be resistor-divided down or level-shift down from the output voltage. As this feedback voltage drops below VREF, next switching cycle starts.

## DETAILED OPERATING DESCRIPTION (Cont'd)



Figure 20. Simplified Block Diagram of Main Regulator

In Figure 22, regulator is operating at Discontinuous Conduction Mode, waveforms are similar to those of Figure 21. However, coil current drops to zero before next switching cycle starts.

To estimate conduction mode, below equation can be used.

$$
\text { Iroom }=\frac{\eta \times T_{O N} \times V_{i n}{ }^{2}}{2 \times L \times V o u t}-I_{\text {LOAD }}
$$

where, $\eta$ is efficiency, refer to Figure 6
if $I_{\text {room }}>0$, the regulator is at Discontinuous Conduction mode
if $I_{\text {room }}=0$, the regulator is at Critical Conduction mode where coil current just drops to zero and next cycle starts.
if $I_{\text {room }}<0$, the regulator is at Continuous Conduction mode

$$
\begin{align*}
& T_{S W}=\frac{T_{O N}}{1-\eta\left(\frac{\text { Vin }}{\text { Vout }}\right)}(\mathrm{S}) ; \\
& { }^{I_{p k}}=\frac{I_{L O A D}}{1-\left(\frac{T_{O N}}{T_{S W}}\right)}+\frac{\operatorname{Vin} \times T_{O N}}{2 \times L} \tag{A}
\end{align*}
$$

For Discontinuous Conduction mode, provided that current limit is not reached,

$$
\begin{aligned}
T_{S W} & =\frac{V i n \cdot T_{O N}^{2}}{2 \cdot L \cdot I_{L O A D} \cdot\left(\frac{\text { Vout }}{\eta \cdot V i n}-1\right)} \\
I_{p k} & =\frac{V i n}{L} \cdot T_{O N} \quad \text { (A) }
\end{aligned}
$$

For Continuous Conduction mode, provided that current limit is not reached,


Figure 21. Waveforms of Continuous Conduction Mode


Figure 22. Waveforms of Discontinuous Conduction Mode

## DETAILED OPERATING DESCRIPTION (Cont'd)

## Synchronous Rectification

A Synchronous Rectifier is used in the main regulator to enhance efficiency. Synchronous rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns. In Figure 20, as main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M 2 is being turned ON , this timing is indicated as $\mathrm{t}_{\mathrm{dh}}$ in Figure 21.

When the main regulator is operating in continuous mode, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completed OFF, the above mentioned situation will occur. So dead time is introduced to make sure M2 is completed OFF before M1 is being turned ON, this is indicated as $\mathrm{t}_{\mathrm{dl}}$ in Figure 21.

When the main regulator is operating in discontinuous mode, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So M2-voltage-drop sensing comparator (COMP3 of Figure 20) comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is
switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.

## Auxiliary Regulator

The Auxiliary Regulator is a boost regulator, applies PFM scheme to enhance high efficiency and reduce quiescent current. An internal voltage comparator (COMP1 of Figure 23) detects when the voltage of Pin VAUXFBN drops below that of Pin VAUXFBP. The internal power BJT is then switched ON for a fixed-ON-time (or until the internal current limit is reached), and coil current is allowed to build up. As the BJT is switched OFF, coil current will flow through the external Schottky diode to charge up the bulk capacitor. After a fixed-mimimum-OFF time elapses, next switching cycle will start if the output of the voltage comparator is HIGH. Refer to Figure 23, the VAUX regulation level is determined by the equation as follows,

$$
V_{A U X}=V A U X F B P \cdot\left(1+\frac{R_{A U X b}}{R_{A U X a}}\right)(\mathrm{V})
$$

Where Max ON Time, TON2, and Min OFF Time, TOFF2 can be determined by the following equations.

$$
\begin{aligned}
& T_{O N 2}=1.7 \times 10^{-11} \times \text { RIref }(\mathrm{S}) \\
& T_{\text {OFF2 }}=2.1 \times 10^{-12} \times \text { RIref }(\mathrm{S})
\end{aligned}
$$



Figure 23. Simplified Block Diagram of Auxiliary Regulator

## DETAILED OPERATING DESCRIPTION (Cont'd)

## Auxiliary Regulator (Cont'd)

As the Auxiliary Regulator control scheme is the same as the Main Regulator, equations for conduction mode, Tsw and Ipk can also be applied, However, $\eta$ to be used for caculation is refered to Figure 8, 10, or 12.

If external potentiometer is used for voltage level adjustment, internal 1.22 V reference voltage can be used as shown in the application diagram of Figure 24.

## Current Limit for Both regulators

From Figure 20 and Figure 23, sense devices (senseFET or senseBJT) are applied to sample coil current as the low-side switch is ON. With that sample current flowing through a sense resistor, sense-voltage is developed. Threshold detector (COMP2 in both figures) detects whether the sense-voltage is higher than preset level. If it happens, detector output reset the flip-flop to switch OFF low-side switch, and the switch can only be ON as next cycle starts.


Figure 24. Application Diagram with External Potentiometer for VAUX Adjustment

## DETAILED OPERATING DESCRIPTION (Cont'd)

## Auxiliary voltage adjustment

The VAUX voltage can be adjusted by the microprocessor control signals, namely, VAUXCON and VAUXADJ. The control signal pattern is shown in Figure 4. The input truth table is shown in Figure 25.

When VAUXEN is LOW, the Auxiliary Regulator is shut down, only the counter content is retained. The initial counter content is mid-range of 6 -bit.

At the rising edge of VAUXCON, if VAUXADJ is LOW (/ HIGH), each following VAUXADJ pulse enclosed by the VAUXCON pulse packet increments (/ decrements) the 6-bit counter. At the falling edge of VAUXCON, the counter content is then latched to a 6-bit DAC and is converted to a voltage level of VAUXREF between 1.1 V and 2.2 V .

At the falling edge of VAUXCON, if VAUXADJ is HIGH, the counter content will be reset to mid-range (1.65V). This is also the default setting just after power-ON reset is removed.

The 6-bit DAC converts the counter content to voltage level ranging from 1.1 to 2.2 V , so there are altogether 64 levels, and each voltage step is 17 mV . When the counter content reaches its maximum or minimum, further pulse of VAUXADJ will be disregarded, until counting direction is changed.

## Power-ON Reset

The Power-ON Reset block accepts external active HIGH ENABLE signal to activate the IC after battery is plugged in. During the startup period (see Figure 2), the internal startup circuitry is enabled to pump up VMAIN to a certain voltage level, which is the user-defined VMAIN output level minus an offset of 0.15 V . The internal power-on reset signal is then disabled to activate the main regulator and conditionally the
auxiliary regulator. Meanwhile, the startup circuitry will be shut down. The Power-ON Reset block also starts to charge up the external capacitor tied from Pin PDELAY to ground with precise constant current. As the Pin PDELAY's voltage reaches an internal set threshold, Pin PORB will go HIGH to awake the microprocessor. And,

$$
T_{P O R}=\left(\frac{1.22}{0.5}\right) \times C_{p o r} \times R / r e f(S)
$$

From Figure 3, if, by any chance, VMAIN is dropped below the user-defined VMAIN output level minus 0.5 V , PORB will go LOW to indicate the OUTPUT LOW situation. And, the IC will continue to function until the VMAIN is dropped below 2 V .

## Low-Battery-Detect

The Low-Battery-Detect block is actually a voltage comparator. Pin LOWBAT is LOW, if the voltage of external Pin LOWBATSEN is lower than 0.85 V internal reference. The IC will neglect this warning signal. Pin LOWBAT will become HIGH, if the voltage of external Pin LOWBATSEN is recovered to more than 1.1V. From Figure 1, with external resistors RLBa and RLBb, thresholds of Low-Battery-Detect can be adjusted based on the equations below.

$$
\begin{aligned}
& v_{\text {LOBAThigh }}=1.1 \times\left(1+\frac{R_{\text {LBa }}}{R_{\text {LBb }}}\right)(\mathrm{V}) \\
& v_{\text {LOBATIOW }}=0.85 \times\left(1+\frac{R_{L B a}}{R_{\text {LBb }}}\right)(\mathrm{V})
\end{aligned}
$$

| VAUXEN | VAUXCON | VAUXADJ | RESULT |
| :---: | :---: | :---: | :--- |
| 0 | X | X | Hold the counter content |
| 1 | 0 | X | Hold the counter content |
| 1 | - | 0 | Set "countup" flag HIGH |
| 1 | - | 1 | Set "countup" flag LOW |
| 1 | - | 0 | Increment (/ Decrement) the counter if "countup" flag is HIGH (/ LOW) |
| 1 |  | 1 | DAC the counter content to VAUXREF voltage level (1.1 - 2.2 V) <br> Reset the counter to mid-range, then convert the counter content to <br> VAUXREF voltage level (1.65V) |
| 1 |  |  |  |

Figure 25. Auxiliary Voltage Control Input Truth Table

## DETAILED OPERATING DESCRIPTION (Cont'd)

## Lithium-Battery backup

The backup conduction path which is provided by an internal power switch (typ. 13 Ohm ) can be controlled by internal logic or microprocessor.

If LIBATCL is LOW, the switch, which is then controlled by internal logic, is ON when the battery is removed and VMAIN is dropped below LIBATIN by more than 100 mV , and returns OFF when the battery is plugged back in.

If LIBATCL is HIGH, the switch is controlled by microprocessor through LIBATON. The truth table is shown in Figure 26.

## Efficiency and Output Ripple

For both regulators, when large values are used for feedback resistors (>50kOhm), stray capacitance of pin 1 (VMAINFB) and pin 20 (VAUXFBN) can add "lag" to the
feedback response, destabilizing the regulator and creating a larger ripple at the output. From Figure 1, ripple of Main and AUX regulator can be reduced by CMAINb, CAUXa and CAUXb ranging from 100 pF to 100 nF respectively. Reducing the ripple is also with improving efficiency, system designers are recommended to do experiments on capacitance values based on the PCB design.

## Bypass Capacitors

If the metal leads from battery to coils are long, its stray resistance can put additional power loss to the system as AC current is being conducted. In that case, bypass capacitors (CMAINbp and CAUXbp of Figure 1) are recommended to remove AC components of coil currents to minimize that power loss to optimize efficiency.

| LIBATCL | LIBATON | Action |
| :---: | :---: | :--- |
| 0 | $X$ | The switch is ON when the battery is removed and VMAIN is dropped below LIBATIN <br> by more than 100 mV ; The switch is OFF when the battery is plugged in. |
| 1 | 0 | The switch is OFF |
| 1 | 1 | The switch is ON |

Figure 26. Lithium Battery Backup Control Truth Table

## MC33680

## Dual DC-DC Regulator for Electronic Organizer

The MC33680 is a dual DC-DC regulator designed for electronic organizer applications. Both regulators apply Pulse-Frequency-Modulation (PFM). The main step-up regulator output can be externally adjusted from 2.7 V to 5 V . An internal synchronous rectifier is used to ensure high efficiency (achieve 87\%). The auxiliary regulator with a built-in power transistor can be configured to produce a wide range of positive voltage (can be used for LCD contrast voltage). This voltage can be adjusted from +5 V to +25 V by an external potentiometer.

The MC33680 has been designed for battery powered hand-held products. With the low start-up voltage from 1 V and the low quiescent current (typical $35 \mu \mathrm{~A}$ ); the MC33680 is best suited to operate from 1 to 2 AA/ AAA cell. Moreover, supervisory functions such as low battery detection, CPU Power-Good signal, and back-up battery control, for lithium battery or supercap are also included in the chip.

## FEATURES:

- Low Input Voltage, 1V up
- Low Quiescent Current in Standby Mode: $35 \mu$ A typical
- PFM and Synchronous Rectification to ensure high efficiency ( $87 \%$ @ 60mA Load)
- Adjustable Main Output: +2.7 V to +5 V nominal 3.3V @ 100mA max, with 1.8 V input
- Auxiliary Output Voltage: +5 V to +25 V
$+5 \mathrm{~V} @ 25 \mathrm{~mA}$ max, with 1.8 V input $+25 \mathrm{~V} @ 15 \mathrm{~mA}$ max, with 1.8 V input
- Current Limit Protection
- Power-Good Signal with Programmable Delay
- Battery Low Detection
- Lithium Battery or Supercap Back-up
- 32-Pin LQFP Package


## APPLICATIONS:

- Digital Organizer and Dictionary
- Dual Output Power Supply (For MPU, Logic, Memory, LCD)
- Handheld Battery Powered Device (1-2 AA/AAA cell)

ON Semiconductor ${ }^{\text {T }}$ http://onsemi.com


32-LEAD LQFP
FTB SUFFIX
CASE 873A

PIN CONNECTIONS \& DEVICE MARKING


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33680FTB | LQFP | 1250 Tray / Drypack |
| MC33680FTBR2 | LQFP | $1800 /$ Tape \& Reel |



Figure 1. Detailed Application Block Diagram

## MC33680

## TIMING DIAGRAMS



Figure 2. Startup Timing


Figure 3. Power Down Timing

## MC33680

PIN FUNCTION DESCRIPTION

| Pin <br> No. | Function | Type/Direction | Description |
| :---: | :---: | :---: | :---: |
| 1 | VMAINFB | Analog / Input | Feedback pin for VMAIN |
| 2 | VBAT | Power | Main battery supply |
| 3 | VBAT | Power | Main battery supply |
| 4 | VDD | Analog / Output | Connect to decoupling capacitor for internal logic supply |
| 5 | PDELAY | Analog / Input | Capacitor connection for defining Power-On signal delay |
| 6 | VREF | Analog / Output | Bandgap Reference output voltage. Nominal voltage is 1.25 V |
| 7 | AGND | Analog Ground |  |
| 8 | IREF | Analog / Input | Resistor connection for defining internal current bias and PDELAY current |
| 9 | LOWBATSEN | Analog / Input | Resistive network connection for defining low battery detect threshold |
| 10 | DGND | Digital Ground |  |
| 11 | PORB | CMOS / Output | Active LOW Power-On reset signal |
| 12 | LOWBATB | CMOS / Output | Active LOW low battery detect output |
| 13 | LIBATON | CMOS / Input | microprocessor control signal for Lithium battery backup switch, the switch is ON when LIBATON=HIGH and LIBATCL=HIGH |
| 14 | LIBATCL | CMOS / Input | microprocessor control signal for Lithium battery backup switch, if it is HIGH, the switch is controlled by LIBATON, otherwise, controlled by internal logic |
| 15 | DGND | Digital Ground |  |
| 16 | NC |  | no connection |
| 17 | VAUXEN | CMOS / Input | VAUX enable, Active high |
| 18 | VAUXFBP | Analog / Input | Feedback pin for VAUX |
| 19 | NC |  | no connection |
| 20 | VAUXFBN | Analog / Input | Feedback pin for VAUX |
| 21 | VAUXBDV | Power | VAUX BJT base drive circuit power supply |
| 22 | VAUXCHG | Analog / Output | test pin |
| 23 | VAUXBASE | Analog / Output | test pin |
| 24 | NC |  | no connection |
| 25 | VAUXSW | Analog / Output | Collector output of the VAUX power BJT |
| 26 | VAUXEMR | Analog / Output | Emitter output of the VAUX power BJT |
| 27 | LIBATIN | Analog / Input | Lithium battery input for backup purposes |
| 28 | LIBATOUT | Analog / Output | Lithium battery output |
| 29 | NC |  | no connection |
| 30 | VMAINGND | Power Ground | Ground for VMAIN low side switch |
| 31 | VMAINSW | Analog / Input | VMAIN inductor connection |
| 32 | VMAIN | Analog / Output | VMAIN output |

ABSOLUTE MAXIMUM RATINGS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Parameter | Symbol | Min | Max | Unit |
| :--- | :---: | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\text {BAT }}$ | -0.3 | 7.0 | Vdc |
| Digital Pin Voltage | $\mathrm{V}_{\text {digital }}$ | -0.3 | 7.0 | Vdc |
| General Analog Pin Voltage | $\mathrm{V}_{\text {analog }}$ | -0.3 | 7.0 | Vdc |
| Pin VAUXSW to Pin VAUXEMR Voltage (Continuous) | $\mathrm{V}_{\text {AUXCE }}$ | -0.3 | 30 | Vdc |
| Pin VMAINSW to Pin VMAIN Voltage (Continuous) | $\mathrm{V}_{\text {syn }}$ |  | 0.3 | Vdc |
| Operating Junction Temperature | $\mathrm{T}_{\mathrm{j}(\max )}$ |  | 150 | ${ }^{\circ} \mathrm{C}$ |
| Ambient Operating Temperature | $\mathrm{T}_{\mathrm{a}}$ | 0 | 70 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ | -50 | 150 | ${ }^{\circ} \mathrm{C}$ |

STATIC ELECTRICAL CHARACTERISTICS (Circuit of Figure 1, $\mathrm{VP}=1.8 \mathrm{~V}, \mathrm{l}_{\mathrm{load}}=0 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise noted.)

| Rating | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Supply Voltage ${ }^{1}$ | $V_{\text {BAT }}$ | 1.0 |  |  | V |
| VMAIN output voltage | $V_{\text {main }}$ | 3.1 | 3.3 | 3.5 | V |
| VMAIN output voltage range ${ }^{2}$ | $\mathrm{V}_{\text {main_range }}$ | 2.7 |  | 5.0 | V |
| VMAIN output current ${ }^{3}$ | $\mathrm{I}_{3.3}$ _1.8 |  |  | 200 | mA |
| VMAIN maximum switching frequency ${ }^{4}$ | Freqmax_VM |  |  | 100 | kHz |
| VMAIN peak coil static current limit | ILIM_VM | 0.85 | 1.0 | 1.15 | A |
| VAUX output voltage range | VAUX_range | 5.0 |  | 25 | V |
| VAUX maximum switching frequency | Freq $_{\text {max_VL }}$ |  |  | 120 | kHz |
| VAUX peak coil static current limit | ILIM_VL |  | 1.0 |  | A |
| Quiescent Supply Current at Standby Mode ${ }^{5}$ | $1 \mathrm{I}_{\text {standby }}$ |  | 35 | 60 | $\mu \mathrm{A}$ |
| Reference Voltage @ no load | Vref ${ }_{\text {no_load }}$ | 1.16 | 1.22 | 1.28 | V |
| Battery Low Detect lower hysteresis threshold ${ }^{6}$ | V Lobat_L | 0.8 | 0.85 | 0.9 | V |
| Battery Low Detect upper hysteresis threshold | V Lobat_h | 1.05 | 1.1 | 1.15 | V |
| PDELAY Pin output charging current | Ichgrdelay | 0.8 | 1.0 | 1.2 | $\mu \mathrm{A}$ |
| PDELAY Pin voltage threshold | Vth ${ }_{\text {PDELAY }}$ | 1.16 | 1.22 | 1.28 | V |

NOTE: 1. Output current capability is reduced with supply voltage due to decreased energy transfer. The supply voltage must not be higher than VMAIN +0.6 V to ensure boost operation. Max Start-up loading is typically 1 V at $400 \mu \mathrm{~A}, 1.8 \mathrm{~V}$ at 4.4 mA , and 2.2 V at 88 mA .
NOTE: 2. Output voltage can be adjusted by external resistor to the VMAINFB pin.
NOTE: 3. At VBAT $=1.8 \mathrm{~V}$, output current capability increases with VBAT.
NOTE: 4. Only when current limit is not reached.
NOTE: 5. This is average current consumed by the IC from VDD, which is low-pass filtered from VMAIN, when only VMAIN is enabled and at no loading. NOTE: 6. This is the minimum of "LOWBATB" threshold for battery voltage, the threshold can be increased by external resistor divider from "VBAT" to "LOWBATSEN".

DYNAMIC ELECTRICAL CHARACTERISTICS (Refer to TIMING DIAGRAMS, $\mathrm{T}_{\mathrm{A}}=0$ to $70^{\circ} \mathrm{C}$ unless otherwise noted.)

| Rating | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Minimum PORB to Control delay | tporc $^{y}$ |  |  | 500 | nS |



Figure 4. Efficiency of VMAIN versus Output Current (VMAIN = 3.3 V, L = 33 uH , Various VIN)


Figure 5. Efficiency of VMAIN versus Input Voltage (VMAIN $=3.3 \mathrm{~V}, \mathrm{~L} 1=33 \mathrm{uH}$, Various $\mathrm{I}_{\text {OUT }}$ )


Figure 7. Efficiency of VAUX versus Input Voltage (VAUX $=25 \mathrm{~V}, \mathrm{~L} 2=33 \mathrm{uH}$, Various IOUT)


Figure 8. Efficiency of VAUX versus Output Current (VAUX = 20 V, L2 = $\mathbf{3 3} \mathbf{u H}$, Various $\mathrm{V}_{\text {IN }}$ )


Figure 10. Efficiency of VAUX versus Output Current (VAUX = 5 V, L2 = 82 uH , Various VIN)


Figure 9. Efficiency of VAUX versus Input Voltage (VAUX = $20 \mathrm{~V}, \mathrm{~L} 2=33 \mathrm{uH}$, Various $\mathrm{I}_{\mathrm{OUT}}$ )


Figure 11. Efficiency of VAUX versus Input Voltage (VAUX = 5 V, L2 = 82 uH , Various I $\mathrm{l}_{\text {OUT }}$ )


Figure 12. VMAIN Output Ripple (Medium Load)


Figure 14. VAUX Output Ripple (Medium Load)


Figure 16. VMAIN Startup and Power-Good Signal


Figure 13. VMAIN Output Ripple (Heavy Load)


Figure 15. VAUX Output Ripple (Heavy Load)


1: VAUX from 1.8 V to 20 V ( $5 \mathrm{~V} /$ div)
2: VAUXEN (2 V/div)

Figure 17. VAUX Startup

## DETAILED OPERATING DESCRIPTION General

The MC33680 is a dual DC-DC regulator designed for electronic organizer applications. Both regulators apply Pulse-Frequency-Modulation (PFM). The main boost regulator output can be externally adjusted from 2.7 V to 5 V . An internal synchronous rectifier is used to ensure high efficiency (achieve $87 \%$ ). The auxiliary regulator with a built-in power transistor can be configured to produce a wide range of positive voltage (can be used for LCD contrast voltage). This voltage can be adjusted from +5 V to +25 V by an external potentiometer.
The MC33680 has been designed for battery powered hand-held products. With the low start-up voltage from 1V and the low quiescent current (typical $35 \mu \mathrm{~A}$ ), the MC33680 is best suited to operate from 1 to $2 \mathrm{AA} / \mathrm{AAA}$ cell. Moreover, supervisory functions such as low battery detection, CPU Power-Good signal, and back-up battery control, are also included in the chip. It makes the MC33680 the best one-chip power management solution for applications such as electronic organizers and PDAs.

## Pulse Frequency Modulation (PFM)

Both regulators apply PFM. With this switching scheme, every cycle is started as the feedback voltage is lower than the internal reference. This is normally performed by internal comparator. As cycle starts, Low-Side switch (i.e. M1 in Figure 1) is turned ON for a fixed ON time duration (namely, $\mathrm{T}_{\text {on }}$ ) unless current limit comparator senses coil current has reached its preset limit. In the latter case, M1 is OFF instantly. So $\mathrm{T}_{\text {on }}$ is defined as the maximum ON time of M1. When M1 is ON, coil current ramps up, so energy is being stored inside the coil. At the moment just after M1 is OFF, the Synchronous Rectifier (i.e. M2 in Figure 1) or any rectification device (such as Schottky Diode of Auxiliary Regulator) is turned ON to direct coil current to charge up the output bulk capacitor. Provided that coil current limit is not reached, every switching cycle delivers fixed amount of energy to the bulk capacitor. For higher loading, a larger amount of energy (Charge) is withdrawn from the bulk capacitor, and a larger amount of Charge is then supplied to the bulk capacitor to regulate output voltage. This implies switching frequency is increased; and vice-versa.

## Main Regulator

Figure 18 shows the simplified block diagram of Main Regulator. Notice that precise bias current Iref is generated by a VI converter and external resistor RIref, where

$$
\text { Iref }=\frac{0.5}{\text { RIref }}(\mathrm{A})
$$

This bias current is used for all internal current bias as well as setting VMAIN value. For the latter application, Iref is doubled and fed as current sink at Pin 1. With external resistor RMAINb tied from Pin1 to Pin32, a constant voltage level shift is generated in between the two pins. In close-loop operation, voltage at Pin 1 (i.e. Output feedback voltage) is needed to be regulated at the internal reference voltage level, 1.22 V . Therefore, the delta voltage across Pin 1 and Pin 32 which can be adjusted by RMAINb determines the Main Output voltage. If the feedback voltage drops below 1.22 V , internal comparator sets switching cycle to start. So, VMAIN can be calculated as follows.

$$
V M A I N=1.22+\frac{R M A I N b}{R / r e f}(\mathrm{~V})
$$

From the above equation, although VMAIN can be adjusted by RMAINb and RIref ratio, for setting VMAIN, it is suggested, by changing RMAINb value with RIref kept at 480K. Since changing RIref will alter internal bias current which will affect timing functions of Max ON time ( $T_{O N 1}$ ) and Min OFF time ( $T_{\text {OFFl }}$ ). Their relationships are as follows;

$$
\begin{aligned}
& T_{O N 1}=1.7 \times 10^{-11} \times \text { RIref }(\mathrm{S}) \\
& T_{O F F 1}=6.4 \times 10^{-12} \times \text { RIref }(\mathrm{S}) \\
& \text { Continuous Conduction Mode and Discontinuous } \\
& \text { Conduction Mode }
\end{aligned}
$$

In Figure 19, regulator is operating at Continuous Conduction Mode. A switching cycle is started as the output feedback voltage drops below internal voltage reference VREF. At that instant, the coil current is not yet zero, and it starts to ramp up for the next cycle. As the coil current ramps up, loading makes the output voltage to decrease as the energy supply path to the output bulk capacitor is disconnected. After Ton elapses, M1 is OFF, M2 is ON, energy is pumped to the bulk capacitor. Output voltage is increased as excessive charge is pumped in, then it is decreased after the coil current drops below the loading. Notice the abrupt spike of output voltage is due to ESR of the bulk capacitor. Feedback voltage can be resistor-divided down or level-shift down from the output voltage. As this feedback voltage drops below VREF, next switching cycle starts.

## MC33680

## DETAILED OPERATING DESCRIPTION (Cont'd)



Figure 18. Simplified Block Diagram of Main Regulator

In Figure 20, regulator is operating at Discontinuous Conduction Mode, waveforms are similar to those of Figure 19. However, coil current drops to zero before next switching cycle starts.

To estimate conduction mode, below equation can be used.

$$
\text { Iroom }=\frac{\eta \times T_{\text {ON }} \times \text { Vin }^{2}}{2 \times L \times \text { Vout }}-I_{L O A D}
$$

where, $\eta$ is efficiency, refer to Figure 4
if $I_{\text {room }}>0$, the regulator is at Discontinuous Conduction mode
if $I_{\text {room }}=0$, the regulator is at Critical Conduction mode where coil current just drops to zero and next cycle starts.
if $I_{\text {room }}<0$, the regulator is at Continuous Conduction mode

For Continuous Conduction mode, provided that current limit is not reached,

$$
\begin{aligned}
& T_{S W}=\frac{T_{O N}}{1-\eta\left(\frac{\text { Vin }}{\text { Vout }}\right)}(\mathrm{S}) ; \\
& I_{p k}=\frac{I_{L O A D}}{1-\left(\frac{T_{O N}}{T_{S W}}\right)}+\frac{\operatorname{Vin} \times T_{O N}}{2 \times L}(\mathrm{~A})
\end{aligned}
$$

For Discontinuous Conduction mode, provided that current limit is not reached,

$$
\begin{align*}
T_{S W} & =\frac{V i n \cdot T_{O N}^{2}}{2 \cdot L \cdot I_{L O A D} \cdot\left(\frac{\text { Vout }}{\eta \cdot \text { Vin }}-1\right)}  \tag{S}\\
I_{p k} & =\frac{V i n}{L} \cdot T_{O N} \quad(\mathrm{~A})
\end{align*}
$$



Figure 19. Waveforms of Continuous Conduction Mode


Figure 20. Waveforms of Discontinuous Conduction Mode

## DETAILED OPERATING DESCRIPTION (Cont'd) Synchronous Rectification

A Synchronous Rectifier is used in the main regulator to enhance efficiency. Synchronous rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns. In Figure 19, as main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completely turned OFF, current will be shunted from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M2 is being turned ON , this timing is indicated as $\mathrm{t}_{\mathrm{dh}}$ in Figure 20.

When the main regulator is operating in continuous mode, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completed OFF, the above mentioned situation will occur. So dead time is introduced to make sure M2 is completed OFF before M1 is being turned ON, this is indicated as $\mathrm{t}_{\mathrm{dl}}$ in Figure 20.

When the main regulator is operating in discontinuous mode, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So M2-voltage-drop sensing comparator (COMP3 of Figure 18) comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss.

Therefore, determination on the offset voltage is essential for optimum performance.

## Auxiliary Regulator

The Auxiliary Regulator is a boost regulator, applies PFM scheme to enhance high efficiency and reduce quiescent current. An internal voltage comparator (COMP1 of Figure 21) detects when the voltage of Pin VAUXFBN drops below that of Pin VAUXFBP. The internal power BJT is then switched ON for a fixed-ON-time (or until the internal current limit is reached), and coil current is allowed to build up. As the BJT is switched OFF, coil current will flow through the external Schottky diode to charge up the bulk capacitor. After a fixed-mimimum-OFF time elapses, next switching cycle will start if the output of the voltage comparator is HIGH. Refer to Figure 21, the VAUX regulation level is determined by the equation as follows,

$$
\begin{equation*}
V_{A U X}=V A U X F B P \cdot\left(1+\frac{R_{A U X b}}{R_{A U X a}}\right) \tag{V}
\end{equation*}
$$

Where Max ON Time, TON2, and Min OFF Time, TOFF2 can be determined by the following equations.

$$
\begin{aligned}
& T_{O N 2}=1.7 \times 10^{-11} \times \text { RIref }(\mathrm{S}) \\
& T_{O F F 2}=2.1 \times 10^{-12} \times \text { RIref }(\mathrm{S})
\end{aligned}
$$

As the Auxiliary Regulator control scheme is the same as the Main Regulator, equations for conduction mode, Tsw and Ipk can also be applied, However, $\eta$ to be used for calculation is referred to Figures 6, 8, or 10.


Figure 21. Simplified Block Diagram of Auxiliary Regulator

## DETAILED OPERATING DESCRIPTION (Cont'd) Current Limit for Both regulators

From Figure 18 and Figure 21, sense devices (senseFET or senseBJT) are applied to sample coil current as the low-side switch is ON. With that sample current flowing through a sense resistor, sense-voltage is developed. Threshold detector (COMP2 in both Figures) detects whether the sense-voltage is higher than preset level. If it happens, detector output reset the flip-flop to switch OFF low-side switch, and the switch can only be ON as next cycle starts.

## Power-Good Signal

During the startup period (see Figure 2), the internal startup circuitry is enabled to pump up VMAIN to a certain voltage level, which is the user-defined VMAIN output level minus an offset of 0.15 V . The internal Power-Good signal is then enabled to activate the main regulator and conditionally the auxiliary regulator. Meanwhile, the startup circuitry will be shut down. The Power-Good signal block also starts to charge up the external capacitor tied from Pin PDELAY to ground with precise constant current. As the Pin PDELAY's voltage reaches an internal set threshold, Pin PORB will go HIGH to awake the microprocessor. This delay is stated as follows;

$$
T_{P O R}=\left(\frac{1.22}{0.5}\right) \times C_{p o r} \times R / r e f(\mathrm{~S})
$$

From Figure 3, if, by any chance, VMAIN is dropped below the user-defined VMAIN output level minus 0.5 V , PORB will go LOW to indicate the OUTPUT LOW situation. And, the IC will continue to function until the VMAIN is dropped below 2 V .

## Low-Battery-Detect

The Low-Battery-Detect block is actually a voltage comparator. Pin LOWBAT is LOW, if the voltage of external Pin LOWBATSEN is lower than 0.85 V . The IC will neglect this warning signal. Pin LOWBAT will become HIGH, if the voltage of external Pin LOWBATSEN is recovered to more than 1.1V. From Figure 1, with external resistors RLBa and RLBb, thresholds of Low-Battery-Detect can be adjusted based on the equations below.

$$
\begin{aligned}
& v_{\text {LOBAThigh }}=1.1 \times\left(1+\frac{R_{\text {LBa }}}{R_{\text {LBb }}}\right)(\mathrm{V}) \\
& v_{\text {LOBATIow }}=0.85 \times\left(1+\frac{R_{\text {LBa }}}{R_{\text {LBb }}}\right)(\mathrm{V})
\end{aligned}
$$

## Lithium-Battery backup

The backup conduction path which is provided by an internal power switch (typ. 13 Ohm ) can be controlled by internal logic or microprocessor.
If LIBATCL is LOW, the switch, which is then controlled by internal logic, is ON when the battery is removed and VMAIN is dropped below LIBATIN by more than 100 mV , and returns OFF when the battery is plugged back in.
If LIBATCL is HIGH, the switch is controlled by microprocessor through LIBATON. The truth table is shown in Figure 22.

## Efficiency and Output Ripple

For both regulators, when large values are used for feedback resistors (>50kOhm), stray capacitance of pin 1 (VMAINFB) and pin 20 (VAUXFBN) can add "lag" to the feedback response, destabilizing the regulator and creating a larger ripple at the output. From Figure 1, ripple of Main and AUX regulator can be reduced by capacitors in parallel with RMAINb, RAUXa and RAUXb ranging from 100 pF to 100 nF respectively. Reducing the ripple is also with improving efficiency, system designers are recommended to do experiments on capacitance values based on the PCB design.

## Bypass Capacitors

If the metal lead from battery to coils are long, its stray resistance can put additional power loss to the system as AC current is being conducted. In that case, bypass capacitors should be placed closely to the coil, and connected from $\mathrm{V}_{\text {BAT }}$ to ground. This reduces AC component of coil current passing through the long metal lead, thus minimizing that portion of power loss.

| LIBATCL | LIBATON | Action |
| :---: | :---: | :--- |
| 0 | X | The switch is ON when the battery is removed and VMAIN is dropped below LIBATIN by <br> more than $100 \mathrm{mV} ;$ <br> The switch is OFF when the battery is plugged in. |
| 1 | 0 | The switch is OFF |
| 1 | 1 | The switch is ON |

Figure 22. Lithium Battery Backup Control Truth Table

## MC33560

## Power Management and Interface IC for Smartcard Readers and Couplers

The MC33560 is an interface IC for smartcard reader/writer applications. It enables the management of any type of smart or memory card through a simple and flexible microcontroller interface. Moreover, several couplers can be coupled in parallel, thanks to the chip select input pin (pin \#5). The MC33560 is particularly suited to low power and portable applications because of its power saving features and the minimum of external parts required. Battery life is extended by the wide operating range and the low quiescent current in stand by mode. A highly sophisticated protection system guarantees timely and controlled shutdown upon error conditions.

- $100 \%$ Compatible with ISO 7816-3 Standard
- Wide Battery Supply Voltage Range: $1.8 \mathrm{~V}<\mathrm{V}_{\mathrm{BAT}}<6.6 \mathrm{~V}$
- Programmable $\mathrm{V}_{\mathrm{CC}}$ Supply for 3.0 V or 5.0 V Card Operation
- Power Management for Very Low Quiescent Current in Stand By Mode ( $30 \mu \mathrm{~A}$ max)
- Microprocessor Wake-up Signal Generated Upon Card Insertion
- Self Contained DC/DC Converter to Generate $\mathrm{V}_{\mathrm{CC}}$ using a Minimum of Passive Components
- Controlled Power Up/Down Sequence for High Signal Integrity on the Card I/O and Signal Lines
- Programmable Card Clock Generator
- Chip Select Capability for Parallel Coupler Operation
- High ESD Protection on Card Pins (4.0 kV, Human Body Model)
- Fault Monitoring $\mathrm{V}_{\text {BATlow }}, \mathrm{V}_{\mathrm{CClow}}$ and $\mathrm{I}_{\mathrm{CClim}}$
- All Card Outputs Current Limited and Short Circuit Protected
- Tested Operating Temperature Range: $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$


Figure 1. Simplified Functional Block Diagram


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SO-24W DW SUFFIX CASE 751E

TSSOP-24
DTB SUFFIX
CASE 948K


PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33560DTB | TSSOP-24 | 62 Units/Rail |
| MC33560DTBR2 | TSSOP-24 | 2500 Tape \& Reel |
| MC33560DW | SO-24W | 30 Units/Rail |
| MC33560DWR2 | SO-24W | 1000 Tape \& Reel |

DEVICE MARKING INFORMATION
See general marking information in the device marking section on page 3253 of this data sheet.

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Battery Supply Voltage | $\mathrm{V}_{\text {BAT }}$ | 7.0 | V |
| Battery Supply Current | $\mathrm{I}_{\text {BAT }}$ | $\pm 200$ | mA |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 6.0 | V |
| Power Supply Current | $\mathrm{I}_{\mathrm{CC}}$ | $\pm 150$ | mA |
| Digital Input Pins $(2,4,5,6,7,9,10,17,18,20,21)$ | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{IN}} \\ & \mathrm{I}_{\mathrm{N}} \end{aligned}$ | $\begin{gathered} \hline-0.5 \text { to VBAT }+0.5 \text { but }<7.0 \\ \pm 5.0 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Output Pins (3, 4, 8) | $\mathrm{V}_{\text {OUT }}$ Iout | $\begin{gathered} \hline-0.5 \text { to VBAT }+0.5 \text { but }<7.0 \\ \pm 10 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Card Interface Pins (11, 13, 14, 15, 16, 19) | $V_{\text {Card }}$ $I_{\text {Card }}$ | $\begin{gathered} -0.5 \text { to } \text { VCC }+0.5 \\ \pm 25 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Coil Driver Pin (22), ILIM (pin 24) Power Ground (pin 1) | IL | $\begin{aligned} & \pm 200 \\ & \pm 100 \end{aligned}$ | mA |
| ESD Capability: (Note 2) <br> Standard Pins (2, 3, 4, 5, 6, 7, 8, 9, 10, 17, 18, 20, 21, 22, 23, 24) <br> Card Interface Pins (11, 13, 14, 15, 16, 19) | $\mathrm{V}_{\text {ESD }}$ | $\begin{aligned} & 2.0 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & \mathrm{kV} \\ & \mathrm{kV} \end{aligned}$ |
| SO-24WB Package: <br> Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ <br> Thermal Resistance Junction to Air | $P_{\text {Ds }}$ $\mathrm{R}_{\text {өJAs }}$ | $\begin{aligned} & 285 \\ & 140 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| TSSOP-24 Package: <br> Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=85^{\circ} \mathrm{C}$ <br> Thermal Resistance Junction to Air | $P_{D t}$ <br> $\mathrm{R}_{\theta \mathrm{JAt}}$ | $\begin{aligned} & 220 \\ & 180 \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{J}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Max. Junction Temperature (Note 3) | $\mathrm{T}_{\text {Jmax }}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to + 150 | ${ }^{\circ} \mathrm{C}$ |

ELECTRICAL CHARACTERISTICS These specifications are written in the same style as common for standard integrated circuits. The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: $\mathrm{V}_{\mathrm{BAT}}=4.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ nom, $\mathrm{PWRON}=\mathrm{V}_{\mathrm{BAT}}$, operating mode, $-\mathrm{l}_{\mathrm{CC}}=10 \mathrm{~mA},-25^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 85^{\circ} \mathrm{C}$, $\mathrm{L}_{1}=47 \mu \mathrm{H}, \mathrm{R}_{\mathrm{LIM}}=0 \Omega$, CRDVCC capacitor $=10 \mu \mathrm{~F}$, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BATTERY POWER SUPPLY SECTION |  |  |  |  |  |
| Supply Voltage Range Normal operating range extended operating range (Note 4) | $\mathrm{V}_{\text {BAT }}$ | $\begin{aligned} & 2.2 \\ & 1.8 \end{aligned}$ | - | $\begin{aligned} & \hline 6.0 \\ & 6.6 \end{aligned}$ | V |
| MC33560 Stand By Quiescent Current PWRON $=$ GND, $\mathrm{CRDCON}=\mathrm{GND}, \mathrm{ASYCLKIN}=\mathrm{GND}, \mathrm{V}_{\mathrm{BAT}}=6.0 \mathrm{~V}$, All other logic inputs and outputs open | $\mathrm{l}_{\text {OBAT }}$ | - | - | 30 | us |
| DC Operating Current $\mathrm{I}_{\mathrm{CC}}=10 \mathrm{~mA} ; \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=6.0 \mathrm{~V}$ | $\mathrm{I}_{\text {BATop }}$ | - | - | 12.5 | mA |
| $\mathrm{V}_{\mathrm{BAT}}$ undervoltage detection: <br> Upper Threshold <br> Lower Threshold <br> Hysteresis | - | - | $\begin{aligned} & 1.6 \\ & 1.4 \\ & 0.2 \end{aligned}$ | - | V |

1. Maximum electrical ratings are those values beyond which damage to the device may occur. $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
2. Human body model, $\mathrm{R}=1500 \Omega, \mathrm{C}=100 \mathrm{pF}$.
3. Maximum thermal rating beyond which damage to the device may occur.
4. See Figures 2 and 3.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, input and output voltages should be constrained to the ranges indicated in the recommended operating conditions.
$\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ NOMINAL POWER SUPPLY SECTION

| Characteristic | Test Conditions | Symbol | Guaranteed Limits |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Output Voltage | $\begin{aligned} & 2.2 \mathrm{~V} \leq \mathrm{V}_{\text {BAT }} \leq 6.0 \mathrm{~V} \\ & 1.0 \mathrm{~mA} \leq-\mathrm{I}_{\mathrm{CC}} \leq 25 \mathrm{~mA} \\ & 3.0 \mathrm{~V} \leq \mathrm{V}_{\text {BAT }} \leq 6.0 \mathrm{~V} \\ & 1.0 \mathrm{~mA} \leq-\mathrm{I}_{\mathrm{CC}} \leq 60 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{CC}}$ | $\begin{aligned} & 4.75 \\ & 4.60 \end{aligned}$ | $\begin{array}{r} 5.0 \\ 5.0 \\ \hline \end{array}$ | $\begin{aligned} & 5.25 \\ & 5.40 \end{aligned}$ | V |
| Card $\mathrm{V}_{\mathrm{CC}}$ Undervoltage Detection: <br> Upper Threshold <br> Lower Threshold <br> Switching Hysteresis | (RDYMOD output) (See Table 4) | $\mathrm{V}_{\mathrm{T} 5 \mathrm{H}}$ <br> $V_{\text {T5L }}$ <br> $\mathrm{V}_{\mathrm{HYS} 5}$ | $\begin{aligned} & 4.2 \\ & 120 \end{aligned}$ | $\begin{aligned} & 4.5 \\ & 180 \end{aligned}$ | $\mathrm{V}_{\mathrm{CC}}-0.14$ | V <br> mV |
| Peak Output Current | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V} \text {, internally limited } \\ & \text { (RDYMOD }=\mathrm{L} \text { ) } \end{aligned}$ | ${ }^{-1} \mathrm{ICClim}$ | 80 | - | - | mA |
| Current limit time-out | $\mathrm{V}_{\mathrm{CC}}=4.0 \mathrm{~V}$ | $\mathrm{t}_{\mathrm{d}}$ | - | 160 | - | ms |
| Start-up Current | $\begin{aligned} \mathrm{V}_{\mathrm{CC}}= & 2.0 \mathrm{~V} ; 0^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\ & -40^{\circ} \mathrm{C} \text { to } 0^{\circ} \mathrm{C} \end{aligned}$ | ${ }^{-} \mathrm{CCCst}$ | $\begin{aligned} & 80 \\ & 50 \end{aligned}$ | - | - | mA |
| Low Side Switch Saturation Voltage | $\mathrm{I}_{\mathrm{L}}=50 \mathrm{~mA}, \operatorname{pin} 22$ | $\mathrm{V}_{\text {sat22 }}$ | - | 100 | 160 | mV |
| Rectifier on Saturation Voltage | $\mathrm{I}_{\mathrm{L}}=50 \mathrm{~mA}$, pin 22 to pin 13 | $\mathrm{V}_{\text {Fsat22 }}$ | - | 400 | 520 | mV |
| Converter Switching Frequency | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | $\mathrm{f}_{\text {sw }}$ | - | 120 | - | kHz |
| Shut Down Current (Card access deactivated) | PWRON = GND, $\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}$ | $I_{\text {SD }}$ | 80 | - | - | mA |

$\mathrm{V}_{\mathrm{CC}}=$ 3.0 V NOMINAL POWER SUPPLY SECTION $\left(\mathrm{V}_{\mathrm{BAT}}=2.5 \mathrm{~V},-\mathrm{I}_{\mathrm{CC}}=5.0 \mathrm{~mA}\right)$

| Characteristic | Test Conditions | Symbol | Guaranteed Limits |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Output Voltage | $\begin{aligned} & 2.2 \mathrm{~V} \leq \mathrm{V}_{\text {BAT }} \leq 6.0 \mathrm{~V} \\ & 1.0 \mathrm{~mA} \leq-\mathrm{I}_{\mathrm{CC}} \leq 10 \mathrm{~mA} \\ & 2.5 \mathrm{~V} \leq \mathrm{V}_{\mathrm{BAT}} \leq 6.0 \mathrm{~V} \\ & 1.0 \mathrm{~mA} \leq-\mathrm{I}_{\mathrm{CC}} \leq 50 \mathrm{~mA} \end{aligned}$ | $\mathrm{V}_{\mathrm{CC}}$ | $\begin{aligned} & 2.75 \\ & 2.60 \end{aligned}$ | 3.0 3.0 | $\begin{aligned} & 3.25 \\ & 3.40 \end{aligned}$ | V |
| Card $\mathrm{V}_{\mathrm{CC}}$ Undervoltage Detection: Upper Threshold Lower Threshold Switching Hysteresis | (RDYMOD output) <br> (See Table 4) | $\mathrm{V}_{\mathrm{T} 3 \mathrm{H}}$ <br> $\mathrm{V}_{\text {T3L }}$ <br> $\mathrm{V}_{\mathrm{HYS}}$ | $\begin{aligned} & 2.4 \\ & 80 \end{aligned}$ | $\begin{aligned} & 2.7 \\ & 110 \end{aligned}$ | $\mathrm{V}_{\mathrm{CC}}-0.1$ | $\begin{gathered} \mathrm{V} \\ \mathrm{mV} \end{gathered}$ |
| Start-up Current Shut Down Current (Card access deactivated) | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V} \\ & \mathrm{PWRON}=\mathrm{GND}, \mathrm{~V}_{\mathrm{CC}}=2.0 \mathrm{~V} \end{aligned}$ | $\begin{gathered} -\mathrm{I}_{\mathrm{CCst}} \\ \mathrm{I}_{\mathrm{SD}} \end{gathered}$ | $\begin{aligned} & \hline 50 \\ & 50 \end{aligned}$ | - | - | mA |

APPLICATION INTERFACE DC SECTION (VBAT $=5.0 \mathrm{~V}$ )

| Characteristic | Test Conditions | Symbol | Guaranteed Limits |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Input High Threshold Voltage (increasing) | pins 2, 4, 5, 6, 10, 17 | $\mathrm{V}_{\mathrm{IH}}$ | $0.55{ }^{*} \mathrm{~V}_{\text {BAT }}$ | - | $0.65{ }^{*} \mathrm{~V}_{\text {BAT }}$ | V |
| Input Low Threshold Voltage (decreasing) | $\begin{aligned} & \text { pins 2, 5, 6, } 10 \\ & \text { pin 17 } \\ & \text { pin } 4 \end{aligned}$ | $\mathrm{V}_{\text {IL }}$ | $\begin{aligned} & 0.3^{*} V_{B A T} \\ & 0.2^{*} V_{B A T} \\ & 0.3^{*} V_{B A T} \end{aligned}$ | - | $\begin{aligned} & \hline 0.45^{*} V_{B A T} \\ & 0.40^{*} V_{B A T} \\ & 0.5^{*} V_{B A T} \end{aligned}$ | V |
| Switching Hysteresis | pins 2, 4, 5, 6, 10, 17 | $\mathrm{V}_{\text {HYST }}$ | $0.06{ }^{*} V_{\text {BAT }}$ | - | $0.3^{*} V_{\text {BAT }}$ | V |
| Threshold Voltage | $\begin{aligned} & \hline \text { pin } 9 \\ & \text { pin18 } \end{aligned}$ | $\mathrm{V}_{\text {TH }}$ | $\begin{aligned} & 0.5^{*} V_{B A T} \\ & 0.4^{*} V_{B A T} \end{aligned}$ | - | $\begin{aligned} & 0.6^{*} V_{B A T} \\ & 0.6^{*} V_{B A T} \end{aligned}$ | V |
| Pull-down resistance | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {BAT }}-1.0 \mathrm{~V}$, pin 2, 6, 7, 10 | $\mathrm{R}_{\text {down }}$ | 120 | 240 | 500 | $\mathrm{k} \Omega$ |
| Pull-up resistance | $\mathrm{V}_{\mathrm{IN}}=0.5 \mathrm{~V}$, pin 3, 4, 5 | $\mathrm{R}_{\text {up }}$ | 120 | 240 | 500 | $\mathrm{k} \Omega$ |
| Output High Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{OH}}=-2.5 \mu \mathrm{~A}, \operatorname{pin} 3, \text { pin } 4 \text { for } \overline{\mathrm{CS}}=\mathrm{H} \\ & \mathrm{I}_{\mathrm{OH}}=-50 \mu \mathrm{~A}, \text { pins } 7,20,21 \\ & \mathrm{I}_{\mathrm{OH}}=-0.2 \mathrm{~mA}, \text { pin } 8 \\ & \text { pin } 4 \text { (in output mode }) \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{BAT}}$-1 | - | - | V |
| Output Low Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{OL}}=1.0 \mathrm{~mA}, \text { pins } 7,20,21 \\ & \mathrm{I}_{\mathrm{OL}}=0.2 \mathrm{~mA} \text {, pins } 3,4,8 \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | - | 0.4 | V |
| Input Leakage Current | $\begin{aligned} & \mathrm{V}_{\mathbb{I N}}=2.5 \mathrm{~V}, \overline{\mathrm{CS}}=\mathrm{H}, \text { pins } 9,17,18, \\ & 20,21 \end{aligned}$ | +/-Ileak | - | - | 2.0 | $\mu \mathrm{A}$ |

CARD INTERFACE DC SECTION (V $\mathrm{V}_{\mathrm{BAT}}=5.0 \mathrm{~V}$ )

| Characteristic | Test Conditions | Symbol | Guaranteed Limits |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Output High Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{OH}}=-20 \mu \mathrm{~A}, \operatorname{pin} 11,16,19 \\ & \mathrm{I}_{\mathrm{OL}}=0.2 \mathrm{~mA}, \text { pins } 14,15 \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}$ | $\mathrm{V}_{\text {CC }}-0.9$ | - | - | V |
| Output Low Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{OL}}=1.0 \mathrm{~mA}, \text { pins } 11,16,19 \\ & \mathrm{I}_{\mathrm{LL}}=0.2 \mathrm{~mA}, \text { pins } 14,15 \end{aligned}$ | $\mathrm{V}_{\text {OL }}$ | - | - | 0.4 | V |
| I/O Pull-up resistance, operating mode, $\overline{C S}=\mathrm{L}, \mathrm{PWRON}=\mathrm{H}$ | $\mathrm{V}_{\mathrm{OL}}=0.5 \mathrm{~V}, \operatorname{pin} 11,16,19$ | - | - | 18 | - | k $\Omega$ |
| Card pins security voltage (Card access deactivated) | PWRON = GND, lin=10 mA, pin 11, 14, 15, 16, 19 | $\mathrm{V}_{\text {security }}$ | - | - | 2.0 | V |

DIGITAL DYNAMIC SECTION (VBAT $=5.0 \mathrm{~V}$, normal operating mode) (Note 6)

| Characteristic | Test Conditions | Symbol | Guaranteed Limits |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Input Clock Frequency | pin 9 , duty cycle $=50 \%$ | $f_{\text {asyclk }}$ | - | - | 20 | MHz |
| Card Clock Frequency | pin 15 | $\mathrm{f}_{\text {craclk }}$ | - | - | 20 | MHz |
| Card Clock Duty Cycle (Note 7) | $\begin{aligned} & \operatorname{pin}^{\operatorname{pin}} 15,50 \% \text { to } 50 \% \mathrm{~V}_{\mathrm{CC}}, \\ & \mathrm{f}_{\text {io }}=16 \mathrm{MHz} \end{aligned}$ | $\mathrm{r}_{\text {clk }}$ | 45 | - | 55 | \% |
| Card Clock Rise and Fall Time | pin15, $10 \% \leftrightarrow 90 \% \mathrm{~V}_{\text {cc }}$ | $\mathrm{t}_{\text {clk }}, \mathrm{t}_{\text {flik }}$ | - | - | 10 | ns |
| I/O Data Transfer Frequency | pin [7, 11], [21, 16], [20, 19] (Note 8) | $\mathrm{f}_{\mathrm{io}}$ | - | 1.0 | - | MHz |
| I/O Duty Cycle | $\begin{aligned} & \operatorname{pin}[7,11],[21,16],[20,19] \text { (Note } 8) \\ & 50 \% \text { to } 50 \% \mathrm{~V}_{\mathrm{CC}} \end{aligned}$ | $\mathrm{r}_{\text {io }}$ | 45 | - | 55 | \% |
| I/O Rise and Fall Time | $\begin{aligned} & \operatorname{pin}[7,11],[21,16],[20,19] \text { (Note 8) } \\ & 10 \% \leftrightarrow 90 \% \text { V }_{C C} \end{aligned}$ | $\mathrm{trio}_{\text {rio }} \mathrm{t}_{\text {fio }}$ | - | - | 150 | ns |
| I/O Transfer Time | $\operatorname{pin}[7,11],[21,16],[20,19] \text { (Note 8) }$ <br> $50 \%$ to $50 \% \mathrm{~V}_{\mathrm{CC}}, \mathrm{L} \rightarrow \mathrm{H}, \mathrm{H} \rightarrow \mathrm{L}$ | $\mathrm{t}_{\mathrm{tr}}$ | - | - | 100 | ns |
| Card Signal Sequence Interval | pin 11, 14, 15, 16, 19, $V_{\text {CC }}$ power up/down | ${ }^{\text {dseq }}$ | - | 0.2 | 1.0 | $\mu \mathrm{S}$ |
| Card Detection Filter Time: Card insertion Card extraction |  | $t_{\text {fltin }}$ <br> $t_{\text {fftout }}$ | $\begin{aligned} & 50 \\ & 50 \end{aligned}$ | - | $\begin{aligned} & 150 \\ & 150 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{S} \\ & \mu \mathrm{~S} \end{aligned}$ |
| Internal Reset Delay | $\overline{\mathrm{RES}}, \mathrm{V}_{\text {CC }}$ power up/down | $\mathrm{t}_{\text {dres }}$ | - | 20 | - | $\mu \mathrm{S}$ |
| Ready Delay Time | pin 4 | $\mathrm{t}_{\text {drdy }}$ | - | - | 2.0 | $\mu \mathrm{S}$ |
| PWRON low Pulse Width | $\overline{\mathrm{CS}}=\mathrm{L}, \mathrm{pin} 2$ | $\mathrm{t}_{\text {won }}$ | 2.0 | - | - | $\mu \mathrm{s}$ |

DIGITAL DYNAMIC SECTION ( $\mathrm{V}_{\mathrm{BAT}}=5.0 \mathrm{~V}$, programming mode) (Note 6)

| Characteristic | Test Conditions | Symbol | Guaranteed Limits |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |
| Data Setup Time RDYMOD, PWRON, RESET, IO | pin 2, 4, 6, 7 | $\mathrm{t}_{\text {smod }}$ | 1.0 | - | - | us |
| Data Hold Time RDYMOD, PWRON, RESET, IO | pin 2, 4, 6, 7 | $t_{\text {hmod }}$ | 1.0 | - | - | $\mu \mathrm{S}$ |
| $\overline{\text { CS low Pulse Width }}$ | pin 5 | $\mathrm{t}_{\text {wcs }}$ | 2.0 | - | - | us |

5. The transistors T1 on lines IO, C4 and C8 (see Figure 24) have a max Rdson of $250 \Omega$.
6. Pin loading $=30 \mathrm{pF}$, except INVOUT $=15 \mathrm{pF}$.
7. As the clock buffer is optimized for low power consumption and hence not symmetrical, clock signal duty cycle is guaranteed for divide by 2 and divide by 4 ratio.
8. In either direction.


Figure 2. Maximum Battery and Card Supply Current vs. $\mathrm{V}_{\mathrm{BAT}}\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right)$


Figure 4. Battery Current vs. Input Clock Frequency $\left(\mathrm{I}_{\mathrm{CC}}=0, \mathrm{~V}_{\mathrm{BAT}}=4.0 \mathrm{~V}\right)$


Figure 6. Maximum Battery Current vs. R LIM $\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=4.0 \mathrm{~V}\right)$


Figure 3. Maximum Battery and Card Supply Current vs. $\mathrm{V}_{\mathrm{BAT}}\left(\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}\right)$


Figure 5. Battery Current vs. Input Clock Frequency $\left(\mathrm{I}_{\mathrm{CC}}=0, \mathrm{~V}_{\mathrm{BAT}}=2.5 \mathrm{~V}\right)$


Figure 7. Maximum Battery Current vs. R $_{\text {LIM }}$ $\left(\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=2.5 \mathrm{~V}\right)$


Figure 8. Maximum Card Supply Current
vs. $\mathrm{R}_{\mathrm{LIM}}\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=4.0 \mathrm{~V}\right)$


Figure 10. Low Side Switch Saturation Voltage ( $\mathrm{l}_{\mathrm{L}}=50 \mathrm{~mA}$ ) vs. Temperature


Figure 12. Card Detection (Insertion) Filter Time vs. Temperature


Figure 9. Maximum Card Supply Current
vs. $\mathrm{R}_{\mathrm{LIM}}\left(\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}, \mathrm{~V}_{\mathrm{BAT}}=2.5 \mathrm{~V}\right)$


Figure 11. Rectifier On Saturation Voltage ( $\mathrm{L}_{\mathrm{L}}=50 \mathrm{~mA}$ ) vs. Temperature


Figure 13. Card Detection (Extraction) Filter Time vs. Temperature


Figure 14. Pull Down Resistance vs. Temperature


Figure 15. Transition from 5.0 V to 3.0 V Card Supply


Figure 16. Transition from 3.0 V to 5.0 V Card Supply


Figure 18. Undervoltage Shutoff $\left(\mathrm{V}_{\mathrm{T} 5 \mathrm{~L}}=4.6 \mathrm{~V}\right)$


Figure 19. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

| Pin | Symbol | Type | Name/Function |
| :--- | :---: | :---: | :---: |

## CONTROLLER INTERFACE

| 2 | PWRON | INPUT pull down | This pin is used to start operation of the internal DC/DC converter. In programming mode, this pin is used to set the "Output Voltage" switch. (See Table 2). |
| :---: | :---: | :---: | :---: |
| 3 | INT | OUTPUT pull up | This open collector pin indicates a change in the card presence circuit status. When a card is inserted or extracted, the pin goes to logic level " 0 ". The signal is reset to logic level " 1 " upon the rising edge of $\overline{C S}$ or upon the rising edge of PWRON. In the case of a multislot application, two or more INT outputs are connected together and the microcontroller has to poll all the MC33560s to identify which slot was detected. |
| 4 | RDYMOD | I/O \& pull up | This bidirectional pin has tri-state output and schmitt trigger input. <br> * When RDYMOD is forced to 0 , the MC33560 can be set to programming mode by a negative transition on $\overline{C S}$. <br> * When RDYMOD is connected to a high impedance, the MC33560 is in normal operating mode, and RDYMOD is in output mode (See Tables 2 and 4): <br> - With $\overline{C S}=L$ and PWRON=H, RDYMOD indicates the status of the DC/DC converter. <br> - With $\overline{C S}=L$ and PWRON $=L$, RDYMOD indicates the status of the card detector. |
| 5 | $\overline{\text { CS }}$ | INPUT pull up | This is the MC33560 chip select signal. Pins 2, 6, 7, 10, 20, 21 are disabled when $\overline{C S}=H$. When RDYMOD=L, the MC33560 enters programming mode upon the falling edge of CS. <br> (See Figure 20) |
| 6 | RESET | INPUT pull down | The signal present at this input pin is translated to pin 14 (the card reset signal) when $\overline{\mathrm{CS}}=\mathrm{L}$. The signal on this pin is latched when $\overline{\mathrm{CS}}=\mathrm{H}$. This pin is also used in programming mode. (See Table 2) |
| 7 | 10 | I/O | This pin connects to the Serial I/O port of a microcontroller. A bi-directional level translator adapts the serial I/O signal between the smartcard and the microcontroller. The level translator is enabled when $\overline{C S}=\mathrm{L}$. The signal on thispin is latched when $\overline{C S}=\mathrm{H}$. This pin is also used in programming mode. (See Table 2) |
| 8 | INVOUT | CLK OUTPUT | The ASYCLKIN (pin 9) signal is buffered and inverted to generate the output signal INVOUT. This output is used for multislot applications, where the ASYCLKIN inputs and INVOUT outputs are daisy-chained. (See the multislot application example in Figure 31) |
| 9 | ASYCLKIN | CLK INPUT high impedance | This pin can be connected to the microcontroller master clock or any clock signal for asynchronous cards. The signal is fed to the internal clock selector circuit, and is translated to CRDCLK at the same frequency, or divided by 2 or 4 , depending on programming. (See Table 3) |
| 10 | SYNCLK | CLK INPUT pull down | This function is used for communication with synchronous cards, and the pin is generally connected to the controller serial interface clock signal. The signal is fed to the internal clock selector circuit, and is translated to CRDCLK upon appropriate programming of the MC33560 (See Table 3). When selected at programming, the signal on this pin is latched when $\overline{C S}=\mathrm{H}$. |
| 20 | C8 | I/O | General purpose input/output. It has the same behavior as I/O, except for programming. It can be connected to a bidirectional port of the microcontroller. The level translator is enabled when CS=L, and the signal is latched whenCS=H. (Compare with pin 19) |
| 21 | C4 | I/O | General purpose input/output. It has the same behaviour as I/O, except for programming. It can be connected to a bidirectional port of the microcontroller. The level translator is enabled when $\overline{C S}=L$, and the signal is latched when $\overline{C S}=H$. (Compare with pin 16) |

CARD INTERFACE

| 11 | CRDIO | I/O | This pin connects to the serial I/O pin of the card connector. A bidirectional level translator <br> adapts the serial I/O signal between the card and the microcontroller. (Compare with pin 7) |
| :---: | :--- | :--- | :--- |
| 14 | CRDRST | OUTPUT | This pin connects to the RESET pin of the card connector. A level translator adapts the <br> RESET signal driven by the microcontroller. (Compare with pin 6 ) |
| 15 | CRDCLK | OUTPUT | This pin connects to the CLK pin of the card connector. The CRDCLK signal is the output of <br> the clock selector circuit. The clock selection is programmed using pins 2,6 and 7 with <br> RDYMOD forced to "0". |
| 16 | CRDC4 | I/O | General purpose input/output. It has the same behavior as CRDIO. It can be connected to the <br> C4 pin of the card connector. |
| 17 | CRDDET | INPUT high <br> impedance | This pin connects to the card detection switch of the card connector. Card detection phase is <br> determined with pin 18. This pin needs an external pull-up or pull-down resistor to operate <br> properly. |


| Pin | Symbol | Type | Name/Function |
| :---: | :--- | :--- | :--- |
| CARD INTERFACE |  |  |  |
| 18 | CRDCON | INPUT high <br> impedance | This pin connects to PGND or VBAT, or possibly to an output port of the microcontroller. With <br> this pin set to a logic "0", the presence of a card is signalled with a logic "1" on pin 17. With <br> this pin set to a logic "1", the presence of a card is signalled with a logic "0" on pin 17. |
| 19 | CRDC8 | I/O | General purpose input/output. It has the same behavior as CRDIO. It can be connected to the <br> C8 pin of the card connector. |

CURRENT LIMIT AND THERMAL PROTECTION

| 1 | PGND | POWER | This pin is the return path for the current flowing into pin 22 (L1). It must be connected to <br> CRDGND using appropriate grounding techniques. |
| :---: | :--- | :--- | :--- |
| 12 | CRDGND | POWER | This pin is the signal ground. It must be connected to the ground pin of the card connector. It <br> is the reference level for all analog and digital signals. |
| 13 | CRDVCC | POWER | This pin connects to the $V_{C C}$ pin of the card connector. It is the reference level for a logic "1" <br> of pins 11, 14, 15, 16 and 19. |
| 22 | L1 | POWER | This pin connects to an external inductance for the DC/DC converter. Please refer to the <br> description of the DC/DC converter functional block. |
| 23 | VBAT | POWER | This pin is connected to the supply voltage. Logic level "1" of pins 2 to 10, 17, 18, 20 and 21 is <br> referenced to $V_{\text {BAT. Operation of the MC33560 is inhibited when V } V_{\text {BAT }} \text { is lower than the }}$ <br> minimum value. |
| 24 | ILIM | POWER | This pin can be connected to the PGND pin, or to a resistor connected to PGND, or left open, <br> depending on the peak coil current needed to supply the card. |

## PROGRAMMING AND STATUS FUNCTIONS

The MC33560 features a programming interface and a status interface. Figure 20 shows how to enter and exit programming mode; Table 2 shows which pins are used to access the various functions.


Figure 20. MC33560 Programming Sequence

Table 2. PIN USE FOR PROGRAMMING AND STATUS FUNCTIONS

|  | Programs <br> CRDVCC <br> TO 3V/5V | Select VCC <br> ON/OFF | Select <br> Clock Input | Program ASYCLKIN <br> Divide Ratio | Poll Card <br> Status | Poll CRDVCC <br> Status |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RDYMOD <br> (in/out) | Force to 0 | READ | Force to 0 | Force to 0 | READ | READ |
| $\overline{\text { CS } \text { (in) }}$ | rising edge | 0 | rising edge | rising edge | 0 | 0 |
| PWRON | $0 / 1$ | $0 / 1$ | Programs CRDVCC | Programs CRDVCC | 0 or Hi-z | 1 |
| RESET (in) | Programs CLK <br> input/divide ratio | NOT USED | $0 / 1$ | $0 / 1$ | NOT USED | NOT USED |
| IO (in) | Programs CLK <br> input/divide ratio | NOT USED | $0 / 1$ | $0 / 1$ | NOT USED | NOT USED |

## MC33560

## CARD VCC AND CARD CLOCK PROGRAMMING

The CRDV $_{\text {CC }}$ and ASYCLK programming options allow the system clock frequency to be matched to the card clock frequency and to select 3.0 V or $5.0 \mathrm{~V} \mathrm{CRDV}_{\mathrm{CC}}$ supply. Table 3 shows the values of PWRON, RESET and IO for the possible options. The default power reset condition is state 4 (synchronous clock and $\mathrm{CRDV}_{\mathrm{CC}}=5.0 \mathrm{~V}$ ). All states are latched for each output variable in programming mode at the positive transition of $\overline{\mathbf{C S}}$ (see Figure 20).

Table 3. CARD VCC AND CARD CLOCK TRUTH TABLE

| STATE\# | PWRON | RESET | IO | CRDVCc | CRDCLK |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | L | L | L | 3 V | SYNCLK |
| 1 | L | L | H | 3 V | ASYCLKIN/4 |
| 2 | L | H | H | 3 V | ASYCLKIN/2 |
| 3 | L | H | L | 3 V | ASYCLKIN |
| 4 | H | L | L | 5 V | SYNCLK |
| 5 | H | L | H | 5 V | ASYCLKIN/4 |
| 6 | H | H | H | 5 V | ASYCLKIN/2 |
| 7 | H | H | L | 5 V | ASYCLKIN |

Note: Card clock integrity is maintained during all frequency commutations (no spikes).
State 4 is the default state at power on.

## DC/DC CONVERTER AND CARD DETECTOR STATUS

The MC33560 status can be polled when $\overline{\mathbf{C S}}=\mathbf{L}$. Please consult Table 2 for a description of input and output signals. The significance of the status message is described in Table 4.

Table 4. RDYMOD STATUS MESSAGES

| PWRON <br> (input) | RDYMOD <br> (output) | Message |
| :--- | :--- | :---: |
| LOW | LOW | No card |
| LOW | HIGH | Card present |
| HIGH | LOW | DC/DC converter overload |
| HIGH | HIGH | DC/DC converter OK |

## DETAILED OPERATING DESCRIPTION

## INTRODUCTION

The MC33560 smartcard interface IC has been designed to provide all necessary functions for safe data transfers between a microcontroller and a smartcard or memory card.

A card detector scans for the presence of a card and generates a debounced wake-up signal to the microcontroller.

Communication and control signal levels are translated between the digital interface and the card interface by the voltage level translator, and the card clock is matched to the system clock frequency by the programmable card clock
generator. The power management unit enables the DC/DC converter for card power supply, supervises the power up/down sequence of the card's I/O and signal lines, and keeps the power consumption very low in stand by mode.

All card interface pins have adequate ESD protection, and fault monitoring ( $\mathrm{V}_{\text {BATlow, }}, \mathrm{V}_{\mathrm{CClow}}, \mathrm{I}_{\mathrm{CClim}}$ ) guarantees hazard-free card reader operation.

Several MC33560s can be operated in parallel, using the same control and data bus, through the use of the chip select signal CS.


Figure 21. MC33560 Operating Modes

## OPERATING MODES

The MC33560 has five operating modes:

- stand by
- programming
- active
- transaction
- idle

The transitions between these different states are shown in Figure 21 above.

## STAND BY MODE

Stand by mode allows the MC33560 to detect card insertion and monitor the power supply while keeping the power consumption at a minimum. It is obtained with $\overline{\mathbf{C S}}=\mathbf{H}$ and $\mathbf{P W R O N}=\mathbf{L}$.

When the MC33560 detects a card, $\overline{\mathbf{I N T}}$ is asserted low to wake up the Microcontroller.

## PROGRAMMING MODE

The programming mode allows the user to configure the card $\mathrm{V}_{\mathrm{cc}}$ and the card clock signal for his specific application. The card supply, $\mathrm{CRDV}_{\mathrm{cc}}$, can be programmed to 3 V or 5 V , and the card clock signal can be defined to be either synchronous, or asynchronous divided by 1,2 or 4.

Programming mode is obtained with RDYMOD=L followed by a negative transition on $\overline{\mathbf{C S}}$. The programming options are shown in Table 3. Programmed values are latched on a positive transition of $\overline{\mathbf{C S}}$ with RDYMOD=L.

## ACTIVE MODE

In active mode, the MC33560 is selected, the RDYMOD pin becomes an output, and the MC33560 status can be polled. Power is not applied to the card.

The microcontroller polls the MC33560 by asserting $\overline{\mathbf{C S}}=\mathbf{L}$ and reading the RDYMOD pin.

If a card is present, the microcontroller starts the DC/DC converter by asserting $\mathbf{P W R O N}=\mathbf{H}$. This starts the automatic power on sequence: when $\mathrm{CRDV}_{\mathrm{cc}}$ reaches the undervoltage level $\left(\mathrm{V}_{\mathrm{T} 5 \mathrm{H}}\right.$ or $\mathrm{V}_{\mathrm{T} 3 \mathrm{H}}$, depending on programming), the card sequencer validates CRDIO, CRDRST, CRDCLK, CRDC4, CRDC8 pins according to the ISO7816-3 sequence (see Figure 26). The MC33560 is now in transaction mode, and the system is ready for data exchange via the three I/O lines and the RESET line.

## TRANSACTION MODE

In transaction mode, the MC33560 maintains power and the selected clock signal applied to the card, and the levels of the IO, RESET, C4 and C8 signals between the microcontroller and the card are translated depending on the supply voltages $\mathrm{V}_{\mathrm{BAT}}$ and $\mathrm{V}_{\mathrm{CC}}$.

The DC/DC converter status can be monitored on the RDYMOD pin.

## IDLE MODE

Idle mode is used when maintaining a card powered up without communicating with it. When an asynchronous clock is used, the selected clock signal is applied to the card.

## POWER DOWN OPERATION

Power-down can be initiated by the controlling microprocessor, by stopping the DC/DC converter with $\mathbf{P W R O N}=\mathbf{L}$ while $\overline{\mathbf{C S}}=\mathbf{L}$, or by the MC33560 itself when an error condition has been detected $\left(\mathrm{CRDV}_{\mathrm{cc}}\right.$ undervoltage, overcurrent longer than 160 ms typ., overtemperature, "hot"
card extraction). The communication session is terminated in a given sequence defined in ISO7816-3.

The MC33560 then goes into active mode, in which its status can be polled.

Stand by mode is reached by deselecting the MC33560 ( $\overline{\mathrm{CS}}=\mathbf{H}$ ).

## FUNCTIONAL BLOCKS

## CARD DETECTOR

This block monitors the card contact CRDDET (during insertion and extraction), filters the incoming waveform and generates an interrupt signal $\overline{\mathbf{I N T}}$ after each change. In order to identify which coupler activated the $\overline{\text { INT }}$ line (multicoupler application) the microcontroller scans both circuits via $\overline{\mathbf{C S}}$ and reads the RDYMOD pin.

The programming input CRDCON tells the level detector which type of mechanical contact is implemented (normally open or normally closed). Special care is taken to hold the current consumption very low on this part of the circuit which is continuously powered by the VBAT supply.

The CRDDET pin has high impedance input, and an external resistor must be connected to pull-up or pull- down, depending on CRDCON. This resistor is chosen according to the maximum leakage current of the card connector and the PCB.

The card detector has an internal $50 \mu$ s debouncing delay. The micro controller has to insert an additional delay (in the ms range) to allow the card contacts to stabilize in the card connector before setting $\mathbf{P W R O N}=\mathbf{H}$.

When the card detector circuit detects a card extraction, it activates the power-down sequence and stops the converter, regardless of the PWRON signal. The $50 \mu$ s delay of the debouncer is enough to ensure that all card signals have reached a safe value before communication with the card takes place.

## CARD STATUS

The controlling microprocessor is informed of the MC33560 status by interrupt and by polling. When a card is extracted or inserted, the $\overline{\mathbf{I N T}}$ line is asserted low. The interrupt is cleared upon the rising edge of $\overline{\mathbf{C S}}$ or upon the rising edge of PWRON $(\overline{\mathbf{I N T}}$ line set to high state).

The microprocessor can poll the status at any time by reading the RDYMOD pin with proper PWRON setting (see Tables 2 and 4).

Since $\overline{\text { INT }}$ and RDYMOD have a high value pull-up resistor ( $240 \mathrm{k} \Omega$ typ.), their rise time can be as long as $10 \mu \mathrm{~s}$ if parasitic capacitance is high and no other pull-up circuitry is connected.

## POWER MANAGER

The task of the power manager is to activate only those circuit functions which are needed for a determined operating mode in order to minimize power consumption (see Figure 19).

In stand by mode ( $\mathbf{P W R O N}=\mathbf{L}$ ) the power manager keeps only the "card present" detector alive. All card interface pins are forced to ground potential.

In the event of a power-up request from the microcontroller (PWRON L to $\mathbf{H}$ transition, $\overline{\mathbf{C S}}=\mathbf{L}$ ) the power manager starts the DC/DC converter. As soon as the CRDVCC supply reaches the operating voltage range, the circuit activates the card signals in the following sequence:

CRDVCC, CRDIO, CRDCLK, CRDC4/C8, CRDRST
At the end of the transaction (PWRON reset to $\mathbf{L}, \overline{\mathbf{C S}}=\mathbf{L}$ ) or forced card extraction, the CRDVCC supply powers down and the card signal deactivation sequence takes place:

CRDRST, CRDC4/C8, CRDCLK, CRDIO, CRDVCC
When $\overline{\mathbf{C S}}=\mathbf{L}$, the bi-directional signal lines (IO, C4 and C8) are put into high impedance state to avoid signal collision with the microcontroller in transmission mode.

## BATTERY UNDERVOLTAGE DETECTOR

The task of this block is to monitor the supply voltage, and to allow operation of the DC/DC converter only with valid voltage (typically 1.5 V ). The comparator has been designed to have stability better than 20 mV in the temperature range.

## DC/DC CONVERTER

Upon request from the power manager, the DC/DC converter generates the CRDVCC supply for the smartcard. The output voltage is programmable for 3.0 V or 5.0 V (see Table 3) to guarantee full cross compatibility of the reader for 5.0 V and 3.0 V smartcards. The wide voltage supply range, $1.8 \mathrm{~V}<\mathrm{V}_{\mathrm{BAT}}<6.6 \mathrm{~V}$, accommodates a broad range of coupler applications with different battery configurations (single cell or multiple cells, serial or parallel connections).

The CRDVCC is current-limited and short-circuit-proof. To avoid excessive battery loading during a card short-circuit, a current integration function forces the power-down sequence (see Figure 28). To retry the session, the microprocessor works through the power on sequence as defined in the power manager section.

## DC/DC Converter operating principles

The DC/DC converter architecture used in the MC33560 allows step-up and step-down voltage conversion to be done. The unique regulation architecture permits an automatic transition from step-up to step-down, and from zero to full load, without affecting the output characteristics.

DC/DC Converter Description: The converter architecture is very similar to the boost architecture, with an active rectifier in place of the diode. The switching transistor is connected to ground through a resistor network in order to adjust the maximum peak current (see Figure 22). A transistor connected to the converter output (CRDVCC) forces this pin to a low voltage when the converter is not operating. This prevents erratic voltage supply to the smartcard when not in use.

The MC33560 has a built in oscillator; the DC/DC converter requires only one inductor and the output filtering capacitor to operate.

Step-Up Operation: When the card supply voltage is lower than the battery voltage, the converter operates like a boost converter; the active rectifier behavior is similar to that of a diode.

Step-Down Operation: When the card supply voltage is higher than the battery voltage, the rectifier control circuit puts the power rectifying transistor in conduction when the $\mathrm{L}_{1}$ voltage reaches $\mathrm{V}_{\mathrm{BAT}}+\mathrm{V}_{\text {FSAT22 }}$. The voltage across the rectifying transistor is higher than in step-up operation. The efficiency is lower, and similar to a linear regulator.

Fault Detection: The DC/DC converter has several features that help to avoid electrical overstress of the MC33560 and of the smartcard, and help to ensure that data transmission with the smartcard occurs only when its supply voltage is within predetermined limits. These functions are:

- overtemperature detection,
- current limitation, and
- card supply undervoltage detection.

The level at which current will be limited is defined by the maximum card supply current programmed with the external components L1 and RLIM.
The undervoltage detection levels for 3.0 V and 5.0 V card supply are preset internally to the MC33560.


Figure 22. DC/DC Converter Functional Block

The overcurrent and undervoltage protection features are complementary, and will shut the circuit off either if the overcurrent is high enough to bring the CRDVCC output below the preset threshold, either after 160 ms (typ.)

In addition, the DC/DC converter will be allowed to start only if the battery supply voltage is high enough to allow normal operation (1.8 V).

The undervoltage comparator has a hysteresis and a delay of typically 20 ms to ensure stable operation. The current detector is a comparator associated with two resistors: one $2.0 \Omega$ attached to PGND and usually connected to analog ground, and a $0.5 \Omega$ attached to ILIM, usually connected to ground through an external resistor to adjust the maximum peak current. The voltage developed across this resistor network is then compared to a 120 mV (typical) reference voltage, and the comparator output performs a cycle-by-cycle peak current limitation by switching off the low side transistor when the voltage exceeds 120 mV .

The internal ILIMCOMP signal is monitored to stop the converter if current limitation is continuously detected
during 160 ms (typical). This allows normal operation with high filtering capacitance and low peak current, even at converter start-up. As a result, a short circuit to ground on the card connector or a continuous overcurrent is reported by RDYMOD 160 ms (typical) after power up.

Unexpected card extraction: The MC33560 detects card extraction and runs a power down sequence if card power is still on when extraction occurs. An active pull-down switch clamps CRDVCC to GND within $150 \mu \mathrm{~s}$ (max) after extraction is detected. The external capacitors will then be discharged. With typical capacitor values of $10 \mu \mathrm{~F}$ and 47 nF as indicated in the application schematic, the time needed to discharge CRDVCC to a voltage below 0.4 V can be estimated to less than $750 \mu \mathrm{~s}$. The total time aftercard extraction detection until CRDVCC reaches 0.4 V is then estimated to $900 \mu \mathrm{~s}$ (max). All smartcard connector contacts will be deactivated before CRDVCC deactivation. This ensures that no electrical damage will be caused to the smartcard under abnormal extraction conditions.
3.0 V/5.0 V programming: It is possible to set the card supply voltage to 3.0 V or 5.0 V at any time, before DC/DC converter start, or during converter operation. When switching from 3.0 V to 5.0 V , a 160 ms (typical) delay blanks the undervoltage fault detection to allow filter capacitor charging.

PWM: The free-running integrated oscillator has two working modes:

- variable on-state and fixed frequency (typically 120 KHz ) for average to heavy loads.
- variable on-state and variable frequency for light loads.

The frequency can be as low as a few kHz if no load is connected to CRDVCC.

The charging current of the timing capacitor is related to the $\mathrm{V}_{\text {BAT }}$ supply voltage, to allow better line regulation, and to increase stability.

Filtering Capacitor: A high value allows efficient filtering of card current spikes. Low values allow low start-up charging current. Care must be taken not to combine low capacitor value with high current limiting, as this can generate high ripple. Usual values range from $4.7 \mu \mathrm{~F}$ to $47 \mu \mathrm{~F}$, depending on current limiting.

Selecting the external components L1 and RLIM: The choice of inductor L1 and resistor R4 is made by using Figure 8 ( 5.0 V card) and/or Figure $9(3.0 \mathrm{~V}$ card) on page 8:

First, determine the maximum current that the application requires to supply to the card (ICCmax, on the y-axis)

Then, select one curve that crosses the selected ICCmax level. The curve is associated with an inductance value $(22 \mu \mathrm{H}, 47 \mu \mathrm{H}$, or $100 \mu \mathrm{H})$.

Finally, use the intersection of the curve and the ICCmax level to find the Rlim value on the x -axis.

Good starting values are : $\mathrm{L} 1=47 \mu \mathrm{H} ; \mathrm{R}_{\mathrm{lim}}=0.5 \Omega$
Note also that, for a high inductance value $(100 \mu \mathrm{H})$, the filtering capacitor is generally charged before inductance current reaches current limitation, while for alow inductance value, the current limitation is activated after a few converter cycles.

Battery requirements: Having determined the $L_{1}$ and $\mathrm{R}_{\mathrm{lim}}$ values, the maximum current drawn from the battery supply is shown by the curves in Figures 6 and 7 .

When the application is powered by a single 3.0 V battery, special care has to be taken to extend its lifetime. When lithium batteries approach the end-of-life, their internal resistance increases, while voltage decreases. This phenomenon can prevent the start-up of the DC/DC converter if the current limiting is set too high, because of the filtering capacitor charging current.

## CLOCK GENERATOR

The primary purpose of the clock generator module is to match the smartcard operating frequency to the system frequency. The source frequency can be provided to ASYCLKIN by the microcontroller itself or from an external oscillator circuit.

In programming mode (RDYMOD=L and $\overline{\mathbf{C S}}$ asserted low) the three input variables PWRON, IO and RESET are used to configure the two output variables CRDVCC and CRDCLK as described in Table 3. This circuit setup is latched during the positive transition of $\overline{\mathbf{C S}}$.

Furthermore, in asynchronous mode the system clock frequency ASYCLKIN can be divided by a factor of 1,2 or 4. The circuit controls the frequency commutation to guarantee that the card clock signal remains free from spikes and glitches. In addition, this circuit ensures that CRDCLK signal pulses will not be shorter than the shortest and/or longer than the longest of the clock signals present before and after programming changes.

The INVOUT output is provided to drive other circuits without additional load to the microprocessor quartz oscillator. It can also be used to build a local RC oscillator. This driver has been optimized for low consumption; it has no hysteresis, and input levels are not symmetrical. If the ASYCLKIN pin is connected to a sine wave, the duty cycle will not always be $50 \%$ at INVOUT.

## Clock generator operating principles

Synchronous Clock: This clock is used mainly for memory cards. It can also be used for asynchronous (microprocessor) cards, allowing the use of two different clock sources. The status of SYNCLK is latched at CRDCLK when $\overline{\mathbf{C S}}$ goes high, so that data (the $\mathbf{I O}$ pin) and clock are always consistent at the card connector, whatever the $\overline{\mathbf{C S}}$ status is. When using the synchronous clock, the clock output becomes active only when the MC33560 is selected with $\overline{\mathbf{C S}}$.

Asynchronous Clock: This clock is used mainly for microprocessor cards. When applied, the clock output remains active even when the MC33560 is not selected with $\overline{\mathbf{C S}}$, in order to keep the microprocessor running and avoid an unwanted reset. The ASYCLKINsignal is buffered at the INVOUT pin, so that several MC33560 systems can use the same clock with one load only.

Depending on programming, the frequency is fed directly, or divided by 2 or by 4 to the CRDCLK pin. If the duty cycle of the applied clock signal is not exactly symmetrical, it is recommended that the clock signal be divided by two or four to guarantee $50 \%$ duty cycle.

Clock Signal Synchronization and Consistency (see Figure 29). The clock divider includes synchronization logic that controls the switch from synchronous clock to asynchronous (and vice-versa), from any division ratio to any other ratio, during $\overline{\mathbf{C S}}$ changes and at power up. The synchronization logic guarantees that each clock cycle on the CRDCLK pin is finished before changing clock selection (and has always the adequate duration), regardless of the moment the programming is changed.

At power-up, when ASYCLKIN is selected, the clock signal at the CRDCLK pin has an entire length, according to the selected divide ratio, whatever the ASYCLKIN signal is versus the internal sequencer timing.


Figure 23. Clock Generator Functional Block

## BIDIRECTIONAL LEVEL TRANSLATOR

This module (used on IO/CRDIO, C4/CRDC4, C8/CRDC8, see Figure 24) adapts the signal voltage levels of the I/O and control lines between the micro controller (supplied by $\mathrm{V}_{\mathrm{BAT}}$ ) and the smartcard (supplied by $\mathrm{CRDV}_{\mathrm{CC}}$ )

When $\overline{\mathbf{C S}}$ is low, with CRDVCC on, and start sequencing completed, this module is transparent for the data, and acts as if the card was directly connected to the reader microcontroller. The core of the level shifter circuit defined for the bidirectional CRDIO, CRDC4 and CRDC8 lines consists of a NMOS switch which can be driven to the logic low state from either side (microcontroller or card). If both sides work in transmission mode with opposite phase, then signal collision on the line is not avoidable. In this case, the peak current is limited to a safe value for the integrated circuit and the smartcard.

During high-to-low transitions, the NMOS transistor impedance ( $\mathrm{T} 1=250 \Omega$ max.) is low enough to charge parasitic capacitance, and have a high enough dv/dt. On low to high transition, the NMOS transistor is not active above a certain voltage, and an acceleration circuit is activated to ensure a high dv/dt.

When the chip is disabled $(\overline{\mathbf{C S}}=\mathbf{H})$ with the voltage supply CRDVCC still active, the IO, C4 and $\mathbf{C 8}$ lines keep their last logic state.

When the converter is off, a transistor forces the CRDIO, CRDC4 and CRDC8 lines to a low state, thus preventing any unwanted voltage level to be applied to the data lines when the card is not in use.


Figure 24. Bidirectional Translator Functional Block

## SECURITY FEATURES

The MC33560 has a number of unique security functions to guarantee that no electrical damage will be caused to the smartcard:

- Battery supply minimum voltage threshold
- Card supply undervoltage and overcurrent detection with automatic shutdown
- Card pin overvoltage clamp to CRDVCC
- Card presence detector for "clean" and fast shut-down
- Consistent card signal sequencing at start-up and power-down, according to ISO7816, even on error conditions
- Consistent clock signal, even when division ratio or synchronization clock signal are changed "on the fly" during a card session (see Figure 29)

Active pull-down on all card pins, including CRDVCC, when not in normal operating mode.

A current limiting function and an overtemperature detector are limiting power dissipation.

## ESD PROTECTION

Due to the nature of smartcards, the card interface pins must absorb high ESD (Electro Static Discharge) energy during card insertion. In addition, the control circuits attached to these pins must safely withstand short circuits and voltage transients during forced card extraction.

Therefore, the MC33560 features enhanced ESD protection, current limitation and short circuit protection on all smartcard interface pins, including C4 and C8.

## PARALLEL OPERATION

For applications where two or more MC33560 are used, the digital control and data bus lines are common to all MC33560. Only the chip select signal, $\overline{\mathbf{C S}}$, requires a separate line for each interface.
While deselected, all communication pins except CRDCLK will keep their logical state on the card side, and will go to high impedance mode on the microprocessor side.
Figure 31 shows a typical application of a dual card reader. This arrangement was chosen only to illustrate the parallel operation of two card interfaces in the same module. The discrete capacitor components are necessary to provide low
impedance on the supply lines VBAT and CRDVCC and to suppress the high frequency noise due to the $\mathrm{DC} / \mathrm{DC}$ converter. The load resistors are external in order to adapt the sense current of the "cardpresent" switches.

## MINIMUM POWER CONSUMPTION CONSIDERATIONS

All analog blocks except the $\mathrm{V}_{\text {BAT }}$ comparator and the card presence detector are disabled in stand by mode ( $\overline{\mathbf{C S}}=\mathbf{H}: \mathrm{DC} / \mathrm{DC}$ converter stopped).

In order to maintain stand by current at a minimum value, all pins with pull-up resistance ( $\overline{\mathbf{C S}}, \overline{\overline{I N T}}, \mathbf{R D Y M O D}$ ) have to be kept in the high state or left open, and pins with pull-down resistance (RESET, SYNCLK, PWRON) have to be kept in the low state or left open. ASYCLKIN should not be connected to an active clock signal during stand by to avoid dynamic currents. This is valid also for SYNCLK, except that it can be left open.


Figure 25. Example of Single Sided PCB Layout for MC33560


Figure 26. Card Signal Sequence During $\mathrm{V}_{\mathrm{cc}}$ Power Up/Down


Figure 27. Interrupt Servicing and Polling


Figure 28. Card Signal Sequence During $\mathrm{V}_{\mathrm{CC}}$ Overload and Unexpected Card Extraction


Figure 29. "On-the-Fly" Card Clock Selection Examples



## MC33560

## MARKING DIAGRAMS

| $\begin{aligned} & \text { SO-24W } \\ & \text { DW SUFFIX } \\ & \text { CASE 751E } \end{aligned}$ | TSSOP-24 DTB SUFFIX CASE 948K |
| :---: | :---: |
| 24 | 24 |
|  | AН-A |
| MC33560DW | MC335 |
| - AWLYYWW | 60 |
|  | - ALYW |
| 1 |  |
|  | 1 |

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

## NCN6000

## Compact Smart Card Interface IC

The NCN6000 is an integrated circuit dedicated to the smart card interface applications. The device handles any type of smart card through a simple and flexible microcontroller interface. On top of that, thanks to the built-in chip select pin, several couplers can be connected in parallel. The device is particularly suited for low cost, low power applications, with high extended battery life coming from extremely low quiescent current.

## Features

- 100\% Compatible with ISO7816-3 and EMV Standard
- Wide Battery Supply Voltage Range: $2.7 \leq$ Vbat $\leq 6.0 \mathrm{~V}$
- Programmable CRD_VCC Supply to Cope with either 3.0 V or 5.0 V Card Operation
- Built-in DC/DC Converter Generates the CRD_VCC Supply with a Single External Low Cost Inductor only, providing a High Efficiency Power Conversion
- Full Control of the Power Up/Down Sequence Yields High Signal Integrity on both the Card I/O and the Signal Lines
- Programmable Card Clock Generator
- Built-in Chip Select Logic allows Parallel Coupling Operation
- ESD Protection on Card Pins ( 8.0 kV, Human Body Model)
- Fault Monitoring includes $\mathrm{Vbat}_{\text {low }}$ and $\mathrm{Vcc}_{\text {low, }}$, providing Logic Feedback to External CPU
- Card Detection Programmable to Handle Positive or Negative Going Input
- Built-in Programmable CRD_CLK Stop Function Handles both High or Low State

Typical Application

- E-Commerce Interface
- ATM Smart Card
- Pay TV System


Figure 1. Simplified Application

ON Semiconductor ${ }^{\text {w }}$
http://onsemi.com
MARKING

## PIN CONNECTIONS


(Top View)
ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| NCN6000DTB | TSSOP-20 | 75 Units/Rail |
| NCN6000DBTR2 | TSSOP-20 | 2500/Tape \& Reel |



Figure 2. Typical Application


Figure 3. Block Diagram
STATUS PGM

| - | RESET | A1 | A0 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| - | L |  |  |  |  |
| - | L | L | L | L | L |
| - | L | L | L | H | L |
| - | L | L | L | H | H |
| - | L | L | H | L | L |
| - | L | L | H | L | H |
| - | L | L | H | H | L |
| - | L | L | H | H | H |
| - | L | H | L | L | L |
| - | L | H | L | L | H |
| - | L | H | L | H | L |
| - | L | H | L | H | H |
| - | L | H | H | L | L |
| - | L | H | H | L | H |
| - | L | H | H | H | L |
| - | L | H | H | H | H |
| H/L | H | Z | L | L | Z |
| H/L | H | Z | L | H | Z |
| L/H | H | Z | H | L | Z |
| H/L | H | Z | H | H | Z |



Figure 4. Programming and Normal Operation Basic Timing

The programming can be achieved with the card powered ON or OFF. The identification of the interrupt is carried out by polling the STATUS pin, the Vbat voltage and the DC/DC results being provided on the same pin as depicted by the
table in Figure 4. During the programming mode, the $\overline{\text { PGM }}$ pin can be released to High since the mode is internally latched by the Negative going transition presents on the Chip Select pin.


Figure 5. Interrupt Servicing and Card Polling

When a card is either inserted or extracted, the CRD_DET pin signal is debounced internally prior to pull the INT pin to Low. The built-in logic circuit automatically accommodates positive or negative input signal slope, on both insertion and extraction state, depending upon the polarity defined during the initialization sequence. The default condition is Normally Open switch, negative going card detection. The external CPU shall acknowledge the request by forcing $\overline{\mathrm{CS}}=\mathrm{L}$ which, in turn, releases the $\overline{\mathrm{INT}}$ pin to High upon positive going of Chip Select (Table 4). Polling the STATUS pin as depicted in Table 3 identifies the active card. If a card is present, the STATUS returns High,
otherwise a Low is presented pin 5 . The $50 \mu$ s digital filter is activated during both Insertion and Extraction of the card. The MPU shall clear the INT line when the card has been extracted, making the interrupt function available for other purposes. However, neither the NCN6000 operation nor the smart card I/O line or commands are affected by the state of the $\overline{\mathrm{INT}} \mathrm{pin}$.

On the other hand, clearing the $\overline{\mathrm{INT}}$ and reading the STATUS register can be performed by a single read by the MPU: states S1 and S2 can be combined in a single instruction, the same for S3 and S4.

## ABBREVIATIONS

| Lout_H | DC/DC External Inductor |
| :--- | :--- |
| Lout_L | DC/DC External Inductor |
| Cout | Output Capacitor |
| VCC | Card Power Supply Input |
| Icc | Current at CRD_VCC Pin |
| Class A | 5.0 V Smart Card |
| Class B | 3.0 V Smart Card |
| CS | Chip Select (from MPU) |
| Z | High Impedance Logic State <br> (according to ISO7816) |
| CRD_VCC | Interface IC Card Power Supply Output |
| CRD_CLK | Interface IC Card Clock Output |
| CRD_RST | Interface IC Card Reset Output |
| CRD_IO | Interface IC Card I/O Signal Line |
| CRD_DET | Interface IC Card Detection |
| ATR | Answer to Reset |
| $\overline{\text { PGM }}$ | Select Programming or Normal Operation |
| INT | Interrupt (to MPU) |
| tr | Rise Time |
| tf | Fall Time |
| td | Delay Time |
| ts | Storage Time |

PIN FUNCTIONS AND DESCRIPTION

| Pin | Name | Type | Description |
| :---: | :---: | :---: | :---: |
| 1 | A0 | INPUT | This pin is combined with A1, PGM, RESET and I/O to program the chip mode of operation and to read the data provided by STATUS. <br> (Figures 4 and 5 and Tables 2 and 3) |
| 2 | A1 | INPUT | This pin is combined with A0, PGM, RESET and I/O to program the chip mode of operation and to read the data provided by STATUS. <br> (Figures 4 and 5 and Tables 2 and 3) |
| 3 | PGM | INPUT | This pin is combined with A0, A1, RESET and I/O to program the chip mode of operation and to read the data provided by STATUS. <br> (Figures 4 and 5 and Tables 2 and 3) |
| 4 | PWR_ON | INPUT Pull Down | This pin validates the operation of the internal DC/DC converter: <br> $\overline{C S}=L+P W R \_O N=$ Negative going: $D C / D C$ is OFF <br> $\overline{C S}=L+$ PWR_ON = Positive going: $D C / D C$ is ON <br> Note: The PWR_ON bit must be combined with a Low state $\overline{C S}$ signal to activate the function. (Table 2) |
| 5 | STATUS | OUTPUT | This pin provides logic state related to the card and NCN6000 status. According to the A0, A1 and PGM logic state, this pin carries either the Card present status or the Vbat or the DC/DC operation state. When PGM $=\mathrm{L}$, STATUS is not affected, see Table 2. |
| 6 | CS | INPUT Pull Up | This pin provides the NCN6000 chip select function. The PWR_ON, RESET, I/O, A0, <br>  device jumps to the programming mode (Figure 4 and Tables 1, 2 and 3). The Chip Select pin must be a unique physical address when more than one card are controlled by a single MPU. The data presented by the MPU are latched upon positive going edge of the Chip Select pin. |

PIN FUNCTIONS AND DESCRIPTION (continued)

| Pin | Name | Type |  |
| :---: | :---: | :---: | :--- |
| 7 | RESET | INPUT <br> Pull Down | This pin provides two modes of operation depending upon the logic state of PGM <br> pin 3: <br> PGM = 1: The signal present at this pin is translated to pin 12 (card reset <br> signal) when CS = L and PWR_ON = H. It is latched when CS = H. |
| PGM = 0: The signal present on this pin is used as a logic input to program the |  |  |  |
| internal functions (Figure 5 and Tables 2 and 3). |  |  |  |

## NCN6000

PIN FUNCTIONS AND DESCRIPTION (continued)

| Pin | Name | Type | Description |
| :---: | :---: | :---: | :--- |
| 16 | GROUND | SIGNAL | The logic and low level analog signals shall be connected to this ground pin. This pin <br> must be externally connected to the PWR_GND pin 17. The designer must make <br> sure no high current transients are shared with the low signal currents flowing into <br> this pin. |
| 17 | PWR_GND | POWER | This pin is the Power Ground associated with the built-in DC/DC converter and must <br> be connected to the system ground together with GROUND pin 11. Using good <br> quality ground plane is recommended to avoid spikes on the logic signal lines. |
| 18 | Lout_L | POWER | The High Side of the external inductor is connected between this pin and Lout_H to <br> provide the DC/DC function. The built-in MOS devices provide the switching function <br> together with the CRD_VCC voltage rectification. |
| 19 | Lout_H | POWER | The High Side of the external inductor is connected between this pin and Lout_L to <br> provide the DC/DC function. The current flowing into this inductor is limited by a <br> sense resistor internally connected from Vbat/pin 20 and pin 19. Typically, Lout $=$ <br> 22 $\mu \mathrm{H}$, with ESR < 2.0 $\Omega$, for a nominal 55 mA output load. |
| 20 | Vbat | POWER | This pin is connected to the supply voltage and monitored by the NCN6000. The <br> operation is inhibited when Vbat is below the minimum 2.70 V value, followed by a <br> PWR_DOWN sequence and a Low STATUS state. |

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Battery Supply Voltage | Vbat | 7.0 | $\checkmark$ |
| Battery Supply Current (Note 2) | lbat | 300 | mA |
| Power Supply Voltage | Vcc | 6.0 | $\checkmark$ |
| Power Supply Current | Icc | $\pm 100$ | mA |
| Digital Input Pins | Vin | $\begin{gathered} -0.5 \mathrm{~V}<\mathrm{V}_{\text {in }}<\mathrm{V}_{\text {bat }}+0.5 \mathrm{~V}, \\ \text { but }<7.0 \mathrm{~V} \end{gathered}$ | V |
| Digital Input Pins | lin | $\pm 5.0$ | mA |
| Digital Output Pins | Vout | $\begin{gathered} -0.5 \mathrm{~V}<\mathrm{V}_{\text {in }}<\mathrm{V}_{\text {bat }}+0.5 \mathrm{~V}, \\ \text { but }<7.0 \mathrm{~V} \end{gathered}$ | V |
| Digital Output Pins | lout | $\pm 10$ | mA |
| Card Interface Pins | Vcard | $-0.5 \mathrm{~V}<\mathrm{V}_{\text {card }}<$ CRD_VCC +0.5 V | V |
| Card Interface Pins, except CRD_CLK | Icard | $\pm 15$ | mA |
| Inductor Current | ILout | 300 | mA |
| ESD Capability (Note 3) <br> Standard Pins <br> Card Interface Pins and CRD_DET | VESD | $\begin{aligned} & 2.0 \\ & 8.0 \end{aligned}$ | kV |
| TSSOP-20 Package <br> Power Dissipation @ Tamb $=+85^{\circ} \mathrm{C}$ <br> Thermal Resistance Junction to Air ( $\mathrm{R}_{\mathrm{\theta ja}}$ ) | $\begin{aligned} & \mathrm{P}_{\mathrm{DS}} \\ & \mathrm{R}_{\mathrm{\theta jj}} \end{aligned}$ | $\begin{aligned} & 320 \\ & 125 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Ambient Temperature Range | TA | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | TJ | -25 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature (Note 4) | TJmax | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | Tsg | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.
2. This current represents the maximum peak current the pin can sustain, not the NCN6000 consumption (see lbat ${ }_{\text {op }}$ ).
3. Human Body Model, $R=1500 \Omega, C=100 \mathrm{pF}$.
4. Absolute Maximum Rating beyond which damage to the device may occur.

POWER SUPPLY SECTION $\left(-25^{\circ} \mathrm{C}\right.$ to $+85^{\circ} \mathrm{C}$ ambient temperature, unless otherwise noted.)

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply | Vbat | 20 | 2.7 | - | 6.0 | V |
| Standby Supply Current Conditions: <br> PWR_ON = L, STATUS = H, CLOCK_IN = H, <br> $\overline{C S}=\mathrm{H}$. All other logic inputs and outputs are open: $\text { Vbat }=3.0 \mathrm{~V}$ $\text { Vbat }=5.0 \mathrm{~V}$ | $\mathrm{lbat}_{\text {sb }}$ | 20 | - |  | $\begin{aligned} & 8.0 \\ & 15 \end{aligned}$ | $\mu \mathrm{A}$ |
| DC Operating Current (Figure 19) <br> PWR_ON = H, CLOCK_IN = 0, CS = H, all CRD pins unloaded <br> $@$ Vbat $=6.0 \mathrm{~V}, \mathrm{CRD}_{2} \mathrm{VCC}=5.0 \mathrm{~V}$ <br> @ Vbat = 3.6 V, CRD_VCC $=5.0 \mathrm{~V}$ | $\mathrm{lbat}_{\text {op }}$ | 20 | - | $\begin{aligned} & 7.0 \\ & 2.0 \end{aligned}$ | $5.0$ | mA |
| Vbat Undervoltage Detection High Vbat Undervoltage Detection Low Vbat Undervoltage Detection Hysteresis | VbatLH <br> VbatLL <br> Vbat $_{\mathrm{HY}}$ | 20 | $\begin{aligned} & 2.1 \\ & 2.0 \\ & - \end{aligned}$ | $\begin{gathered} - \\ - \\ 100 \end{gathered}$ | $\begin{array}{r} 2.7 \\ 2.6 \\ \hline \end{array}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{mV} \end{gathered}$ |
| ```Output Card Supply Voltage @ Icc = 55 mA @ \(2.70 \mathrm{~V} \leq \mathrm{Vbat} \leq 6.0 \mathrm{~V}\) CRD_VCC \(=3.0 \mathrm{~V}\) CRD_VCC \(=5.0 \mathrm{~V}\) @ Vbat LL < Vbat < 2.70 V CRD_VCC \(=5.0 \mathrm{~V}\)``` | Vcc <br> $\mathrm{V}_{\mathrm{C} 3 \mathrm{H}}$ <br> $\mathrm{V}_{\mathrm{C} 5 \mathrm{H}}$ <br> $\mathrm{V}_{\mathrm{C} 5 \mathrm{H}}$ | 15 | $\begin{aligned} & 2.75 \\ & 4.75 \\ & 4.50 \end{aligned}$ |  | $\begin{aligned} & 3.25 \\ & 5.25 \end{aligned}$ | V |
| Output Card Supply Peak Current @ Vcc $=5.0 \mathrm{~V}$ <br> @ CRD_VCC = 5.0 V <br> @ CRD_VCC = 3.0 V <br> $@$ Vbat $=3.6 \mathrm{~V}, \mathrm{CRD} \_\mathrm{VCC}=5.0 \mathrm{~V}$, $\mathrm{Tamb}<65^{\circ} \mathrm{C}$ | Iccp | 15 | $\begin{aligned} & 55 \\ & 55 \\ & 65 \end{aligned}$ | - | - | mA |
| Output Current Limit Time Out | tdoff | 15 | - | 4.0 | - | ms |
| Output Over Current Limit | Iccov | 15 | - | - | 100 | mA |
| Output Dynamic Peak Current @ CRD_VCC = 3.0 V or 5.0 V , Cout $=10 \mu \mathrm{~F}$ Ceramic XR7, Pulse Width 400 ns (Notes 5 and 6) | Iccd | 15 | 100 | - | - | mA |
| Battery Start-Up Current <br> @ CRD_VCC $=3.0 \mathrm{~V},-25^{\circ} \mathrm{C} \leq T A \leq+85^{\circ} \mathrm{C}$ <br> @ CRD_VCC $=5.0 \mathrm{~V},-25^{\circ} \mathrm{C} \leq T A \leq+85^{\circ} \mathrm{C}$ | $\mathrm{lcc}_{\text {st }}$ | 20 |  | $\begin{aligned} & 140 \\ & 300 \end{aligned}$ |  | mA |
| ```Output Card Supply Voltage Ripple @ Lout = 22 \muH Cout 1 = 10 \muF, Cout 2 = 100 nF, Vbat = 3.6 V lout =55 mA CRD_VCC =5.0 V (Note 5) CRD_VCC = 3.0V``` | Vccrip | 15 |  |  | $\begin{aligned} & 50 \\ & 50 \end{aligned}$ | mV |
| Output Card Supply Turn On Time @ Lout = $22 \mu \mathrm{~F}$, Cout $1=10 \mu \mathrm{~F}$, Cout2 $=100 \mathrm{nF}$, Vbat $=2.7 \mathrm{~V}$, CRD_VCC $=5.0 \mathrm{~V}$ | $\mathrm{VcC}_{\text {ton }}$ | 15 | - | - | 2.0 | ms |
| Output Card Supply Shut Off Time @ Cout1 = $10 \mu \mathrm{~F}$, Ceramic, Vbat =2.7 V, CRD_VCC = 5.0 V, Vccoff $<0.4 \mathrm{~V}$ | $\mathrm{VcC}_{\text {TOFF }}$ | 15 | - | - | 250 | $\mu \mathrm{s}$ |
| DC/DC Converter Operating Frequency | Fsw | 18 | - | 600 | - | kHz |
| Power Switch Drain/Source Resistor | Rons | 18 | - | 1.9 | 2.2 | $\Omega$ |
| Output Rectifier ON Resistor | R ${ }_{\text {OND }}$ | 15 | - | 2.8 | 3.4 | $\Omega$ |

5. Ceramic X7R, SMD types capacitors are mandatory to achieve the CRD_VCC specifications. When electrolytic capacitor is used, the external filter must include a 100 nF , max $50 \mathrm{~m} \Omega$ ESR capacitor in parallel, to reduce both the high frequency noise and ripple to a minimum. Depending upon the PCB layout, it might be necessary is to use two $6.8 \mu \mathrm{~F} / 10 \mathrm{~V} /$ ceramic/X7R//SMD1206 in parallel, yielding an improved CRD_VCC ripple over the temperature range.
6. According to ISO7816-3, paragraph 4.3.2.

DIGITAL PARAMETERS SECTION @ 2.70 V $\leq$ Vbat $\leq 6.0$ V, NORMAL OPERATING MODE $\left(-25^{\circ} \mathrm{C}\right.$ to $+85^{\circ} \mathrm{C}$ ambient temperature, unless otherwise noted.) Note: Digital inputs undershoot $<-0.30 \mathrm{~V}$ to ground, Digital inputs overshoot $<0.30 \mathrm{~V}$ to Vbat

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Asynchronous Clock Duty Cycle = 50\% <br> @ Vbat = 3.0V over the temperature range | $F_{\text {CLKIN }}$ | 10 | - | - | 40 | MHz |
| Clock Rise Time Clock Fall Time | $\begin{aligned} & \hline F_{\mathrm{tr}} \\ & F_{\mathrm{tf}} \end{aligned}$ | 10 | - | - | $\begin{aligned} & 5.0 \\ & 5.0 \end{aligned}$ | ns |
| I/O Data Transfer Switching Time, Both Directions (I/O and CRD_IO), @ Cout = 30 pF I/O Rise Time* (Note 7) I/O Fall Time | $\begin{aligned} & \mathrm{T}_{\text {RIO }} \\ & \mathrm{T}_{\mathrm{FIO}} \end{aligned}$ | 8,14 | - | - | $\begin{aligned} & 0.8 \\ & 0.8 \end{aligned}$ | $\mu \mathrm{s}$ |
| Input/Output Data Transfer Time, Both Directions <br> @ $50 \%$ CRD_VCC, L to H and H to L | $\mathrm{T}_{\text {TIO }}$ | 8,14 | - | - | 150 | ns |
| Minimum PWR_ON Low Level Logic State Time to Power Down the DC/DC Converter | $\mathrm{T}_{\text {WON }}$ | 4 | 2.0 | - | - | $\mu \mathrm{s}$ |
| CRD_VCC Power Up/Down Sequence Interval | $\mathrm{T}_{\text {DSEQ }}$ |  | - | 0.5 | 2.0 | $\mu \mathrm{s}$ |
| STATUS Pull Up Resistance | $\mathrm{R}_{\text {STA }}$ | 5 | 20 | 50 | 80 | $\mathrm{k} \Omega$ |
| Chip Select CS Pull Up Resistance | $\mathrm{R}_{\text {CSPU }}$ | 6 | 20 | 50 | 80 | $\mathrm{k} \Omega$ |
| Interrupt INT Pull Up Resistance | R INTPU | 9 | 20 | 50 | 80 | $\mathrm{k} \Omega$ |
| Positive Going Input High Voltage Threshold (A0, <br> A1, PGM, PWR_ON, CS, RESET, CRD_DET) | $\mathrm{V}_{\mathrm{IH}}$ | $\begin{gathered} 1,2, \\ 3,4, \\ 6,7, \\ 11 \end{gathered}$ | 0.70 * Vbat | - | Vbat | V |
| Negative Going Input High Voltage Threshold (A0, A1, PGM, PWR_ON, CS, RESET, CRD_DET) | $\mathrm{V}_{\mathrm{IL}}$ | $\begin{gathered} 1,2, \\ 3,4, \\ 6,7, \\ 11 \end{gathered}$ | 0 | - | 0.30 * Vbat | V |
| Output High Voltage STATUS, INT @ $\mathrm{I}_{\mathrm{OH}}=-10 \mu \mathrm{~A}$ | $\mathrm{V}_{\mathrm{OH}}$ | 5, 9 | Vbat - 1.0 V | - | - | V |
| Output High Voltage STATUS, INT @ $\mathrm{I}_{\mathrm{OH}}=200 \mu \mathrm{~A}$ | $\mathrm{V}_{\text {OL }}$ | 5,9 | - | - | 0.40 | V |

7. Since a $20 \mathrm{k} \Omega$ pull up resistor is provided by the NCN6000, the external MPU can use an Open Drain connection.

DIGITAL PARAMETERS SECTION @ 2.70 V $\leq$ Vbat $\leq 6.0$ V, CHIP PROGRAMMING MODE $\left(-25^{\circ} \mathrm{C}\right.$ to $+85^{\circ} \mathrm{C}$ ambient temperature, unless otherwise noted.)

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A0, A1, PGM, PWR_ON, RESET and I/O | TSMOD | 1,2, | 2.0 | - | - |  |
| Data Set Up Time |  | 3,4, |  |  |  |  |
|  |  | 7,8 |  |  |  |  |
| A0, A1, PGM, PWR_ON, RESET and I/O | THMOD | 1,2, | 2.0 | - | - | $\mu \mathrm{s}$ |
| Data Set Up Time |  | 3,4, |  |  |  |  |
| Chip Select CS Low State Pulse Width | TWCS | 6 | 2.0 | - | - | $\mu \mathrm{s}$ |

SMART CARD SECTION $\left(-25^{\circ} \mathrm{C}\right.$ to $+85^{\circ} \mathrm{C}$ ambient temperature, unless otherwise noted.)

\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Rating \& Symbol \& Pin \& Min \& Typ \& Max \& Unit \\
\hline ```
CRD_RST @ CRD_VCC = +5.0 V
Output RESET \(\mathrm{V}_{\mathrm{OH}} @\) Icrd_rst \(=-20 \mu \mathrm{~A}\)
Output RESET \(\mathrm{V}_{\mathrm{OL}}\) @ Icrd_rst = \(200 \mu \mathrm{~A}\)
Output RESET Rise Time @ Cout = 30 pF
Output RESET Fall Time @ Cout = 30 pF
CRD_RST @ Vcc=+3.0 V
Output RESET \(\mathrm{V}_{\text {OH }} @\) Icrd_rst \(=-20 \mu \mathrm{~A}\)
Output RESET \(\mathrm{V}_{\mathrm{OL}}\) @ Icrd_rst = \(200 \mu \mathrm{~A}\)
Output RESET Rise Time @ Cout = 30 pF
Output RESET Fall Time @ Cout = 30 pF
``` \& \begin{tabular}{l}
\(\mathrm{V}_{\mathrm{OH}}\) \\
\(\mathrm{V}_{\mathrm{OL}}\) \\
\(t_{R}\) \\
\(t_{F}\) \\
\(\mathrm{V}_{\mathrm{OH}}\) \\
\(\mathrm{V}_{\mathrm{OL}}\) \\
\(t_{R}\) \\
\(t_{F}\)
\end{tabular} \& 12 \& \[
\begin{gathered}
\text { CRD_VCC }-0.9 \\
0 \\
\text { CRD_VCC }-0.9 \\
0
\end{gathered}
\] \& - \& \[
\begin{gathered}
\text { CRD_VCC } \\
0.4 \\
100 \\
100 \\
\\
\\
\text { CRD_VCC } \\
0.4 \\
100 \\
100
\end{gathered}
\] \& \begin{tabular}{l}
V \\
v \\
ns \\
V \\
V \\
ns \\
ns
\end{tabular} \\
\hline ```
CRD_CLK @ CRD_VCC = +3.0 V or +5.0 V
CRD_VCC \(=+5.0 \mathrm{~V}\)
Output Frequency (See Note 8)
Output Duty Cycle @ DC Fin = 50\% \(\pm 1 \%\)
Output CRD_CLK Rise Time @ Cout = 30 pF
Output CRD_CLK Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\mathrm{OH}} @\) Icrd_clk \(=-20 \mu \mathrm{~A}\)
Output V OL @ Icrd_clk \(=100 \mu \mathrm{~A}\)
CRD_VCC \(=+3.0 \mathrm{~V}\)
Output Frequency (See Note 8)
Output Duty Cycle @ DC Fin \(=50 \% \pm 1 \%\)
Output CRD_CLK Rise Time @ Cout = 30 pF
Output CRD_CLK Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\text {OH }} @\) Icrd_clk \(=-20 \mu \mathrm{~A} @\) Cout \(=30 \mathrm{pF}\)
Output \(\mathrm{V}_{\mathrm{OL}}\) @ Icrd_clk = \(100 \mu \mathrm{~A}\) @ Cout \(=30 \mathrm{pF}\)
``` \& \begin{tabular}{l}
FCRDCLK \\
\(F_{\text {CRDDC }}\) \(t_{R}\) \(t_{F}\) \(\mathrm{V}_{\mathrm{OH}}\) \(\mathrm{V}_{\mathrm{OL}}\) \\
FCRDCLK \(F_{\text {CRDDC }}\) \(t_{R}\) \(t_{F}\) \(V_{\mathrm{OH}}\) \(\mathrm{V}_{\mathrm{OL}}\)
\end{tabular} \& 13 \& \[
\begin{gathered}
45 \\
\\
3.15 \\
0 \\
\\
40 \\
\\
1.85 \\
0
\end{gathered}
\] \& - \& 5.0
55
18
18
CRD_VCC
+0.5

5.0
60
18
18
CRD_VCC

0.7 \& $$
\begin{gathered}
\mathrm{MHz} \\
\% \\
\mathrm{~ns} \\
\mathrm{~ns} \\
\mathrm{~V} \\
\mathrm{~V} \\
\\
\\
\mathrm{MHz} \\
\% \\
\mathrm{~ns} \\
\mathrm{~ns} \\
\mathrm{~V} \\
\mathrm{~V}
\end{gathered}
$$ <br>

\hline | CRD_I/O @ CRD_VCC = +5.0 V CRD_I/O Data Transfer Frequency CRD_I/O Rise Time @ Cout = 30 pF CRD_I/O Fall Time @ Cout = 30 pF Output $\mathrm{V}_{\mathrm{OH}} @$ Icrd_i/o = -20 $\mu \mathrm{A}$ Output $\mathrm{V}_{\mathrm{OL}} @$ Icrd_i/o $=500 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V}$ |
| :--- |
| CRD_I/O @ CRD_VCC = +3.0 V CRD_I/O Data Transfer Frequency CRD_I/O Rise Time @ Cout = 30 pF CRD_I/O Fall Time @ Cout = 30 pF Output $\mathrm{V}_{\mathrm{OH}} @$ Icrd_i/o $=-20 \mu \mathrm{~A}$ Output $\mathrm{V}_{\mathrm{OL}} @$ Icrd_i/o = $500 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V}$ | \& | $\mathrm{F}_{10}$ |
| :--- |
| $\mathrm{T}_{\text {RIO }}$ |
| $\mathrm{T}_{\text {FIO }}$ |
| $\mathrm{V}_{\mathrm{OH}}$ |
| $\mathrm{V}_{\mathrm{OL}}$ |
| $\mathrm{F}_{10}$ |
| $\mathrm{T}_{\mathrm{RIO}}$ |
| $\mathrm{T}_{\text {FIO }}$ |
| $\mathrm{V}_{\mathrm{OH}}$ |
| VOL | \& 14 \& \[

$$
\begin{gathered}
\text { CRD_VCC }-0.9 \\
0 \\
\\
\text { CRD_VCC }-0.9 \\
0
\end{gathered}
$$

\] \& \[

315
\]

$$
315
$$ \& \[

$$
\begin{gathered}
0.8 \\
0.8 \\
\text { CRD_VCC } \\
0.4 \\
\\
\\
0.8 \\
0.8 \\
\text { CRD_VCC } \\
0.4
\end{gathered}
$$

\] \& \[

$$
\begin{gathered}
\mathrm{kHz} \\
\mu \mathrm{~s} \\
\mu \mathrm{~s} \\
\mathrm{~V} \\
\mathrm{~V} \\
\\
\mathrm{kHz} \\
\mu \mathrm{~s} \\
\mu \mathrm{~s} \\
\mathrm{~V} \\
\mathrm{~V}
\end{gathered}
$$
\] <br>

\hline CRD_IO Pull Up Resistor @ PWR_ON = H \& R ${ }_{\text {CRDPU }}$ \& 14 \& 14 \& 20 \& 26 \& k $\Omega$ <br>

\hline Card Detection Debouncing Delay: Card Insertion Card Extraction \& | TCRDIN |
| :--- |
| TCRDOFF | \& 11 \& \[

$$
\begin{aligned}
& 50 \\
& 50
\end{aligned}
$$

\] \& - \& \[

$$
\begin{aligned}
& 150 \\
& 150
\end{aligned}
$$
\] \& $\mu \mathrm{S}$

$\mu \mathrm{s}$ <br>
\hline Card Insertion or Extraction Positive Going Input High Voltage \& $\mathrm{V}_{\text {IHDET }}$ \& 11 \& 0.70 * Vbat \& - \& Vbat \& V <br>
\hline Card Insertion or Extraction Negative Going Input Low Voltage \& $\mathrm{V}_{\text {ILDET }}$ \& 11 \& 0 \& - \& 0.30 * Vbat \& V <br>
\hline Card Detection Bias Pull Up Current @ Vbat $=5.0 \mathrm{~V}$ \& $\mathrm{I}_{\text {DET }}$ \& 11 \& - \& 10 \& - \& $\mu \mathrm{A}$ <br>
\hline Output Peak Max Current Under Card Static Operation Mode @ Vcc = 3.0 V or Vcc = 5.0 V \& Icrd_iorst \& 12, 14 \& - \& - \& 15 \& mA <br>
\hline Output Peak Max Current Under Card Static Operation Mode @ Vcc $=3.0 \mathrm{~V}$ or $\mathrm{Vcc}=5.0 \mathrm{~V}$ \& Icrd_clk \& 13 \& - \& - \& 70 \& mA <br>
\hline
\end{tabular}

8. The CRD_CLK clock can operate up to 20 MHz , but the rise and fall time are not guaranteed to be fully within the ISO7816 specification over the temperature range. Typically, tr and tf are $12 \mathrm{~ns} @$ CRD_CLK $=10 \mathrm{MHz}$.

## Programming and Status Functions

The NCN6000 features a programming interface and a status interface. Figure 4 illustrates the programming mode.
Table 1. Programming and Status Functions Pinout Logic

| Pins | Name | CRD_VCC <br> Prg. 3.0 V/5.0 V | CLOCK_IN <br> Divide Ratio | CRD_DET | CLOCK STOP <br> AND START | Poll Card <br> Status | DC/DC <br> Status | Vbat <br> Status | CRD_VCC <br> Status |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 5 | STATUS | Not Affected | Not Affected | Not Affected | Not Affected | READ | READ | READ | READ |
| 6 | $\overline{\text { CS }}$ | Latch On <br> Rising Edge | Latch On <br> Rising Edge | Latch On <br> Rising Edge | Latch On <br> Rising Edge | 0 | 0 | 0 | 0 |
| 3 | $\overline{\text { PGM }}$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | A0 | $0 / 1$ | $0 / 1$ | $0 / 1$ | $0 / 1$ | 0 | 1 | 0 | 1 |
| 2 | A1 | $0 / 1$ | $0 / 1$ | 1 | 0 | 0 | 0 | 1 | 1 |
| 7 | RESET | 0 | 0 | 1 | 1 | Z | Z | Z | Z |
| 8 | I/O (in) | $0 / 1$ | $0 / 1$ | $0 / 1$ | $0 / 1$ | Z | Z | Z | Z |

The $\overline{\text { PGM }}$ signal, pin 3, controls the mode of operation (chip programming or smart card transaction) and must be set up accordingly prior to pull Chip Select (pin 6) Low.

Table 2. Status Pin Logic Output

| Name | CS | PGM | A1 | A0 | Status Logic Level |
| :---: | :---: | :---: | :---: | :---: | :--- |
| None | H | X | X | X | No Chip Access |
| None | L | L | X | X | Programming Mode, No Read Available |
| CARD PRESENT | L | H | L | L | Low: No Card Inserted <br> High: Card inserted |
| DC/DC | L | H | L | H | Low: DC/DC Over Range <br> High: DC/DC Operates Normally |
| Vbat | L | H | H | L | Low: Vbat Within Range <br> High: Vbat Below Minimum range |
| CRD_VCC Overload | L | H | H | H | Low: CRD_VCC Voltage Below Minimum Range <br> High: CRD_VCC in Range |

## Card VCC, Card CLOCK and Card Detection Polarity Programming

The CRD_VCC and CLOCK_IN programming options allows matching the system frequency with the card clock frequency, and to select 3.0 V or 5.0 V CRD_VCC supply. The CRD_DET programming option allows the usage of either Normally Open or Normally Close detection switch. Table 3 highlights the A0, A1, $\overline{\mathrm{PGM}}$ and I/O logic states for the possible options. The default power up reset condition
is state 1: asynchronous clock, ratio $1 / 1$, CRD_CLK active, CRD_DET = Normally Open, CRD_VCC = 3.0 V. All states are latched for each output variable in programming mode at the positive going slope of Chip Select $[\overline{\mathrm{CS}}]$ signal. It is the system designer's responsibility to set up the options needed to match the chip with the peripherals. In particular, when using Normally Close switch, the CRD_DET polarity must be defined during the first cycles of the initialization.

Table 3. Card VCC, Card Clock and Card Detection Polarity Truth Table

| HEXA | CS | PWR_ON | PGM | RESET | A1 | A0 | I/O | CRD_VCC | CRD_CLK | CRD_DET | STATUS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| \$00 | L | - | L | L | L | L | L | 3.0 V | CLOCK_IN 1/1 | - | H (Note 13) |
| \$01 | L | - | L | L | L | L | H | 3.0 V | CLOCK_IN 1/2 | - | H (Note 13) |
| \$02 | L | - | L | L | L | H | L | 3.0 V | CLOCK_IN 1/4 | - | H (Note 13) |
| \$03 | L | - | L | L | L | H | H | 3.0 V | CLOCK_IN 1/8 | - | H (Note 13) |
| \$04 | L | - | L | L | H | L | L | 5.0 V | CLOCK_IN 1/1 | - | H (Note 13) |
| \$05 | L | - | L | L | H | L | H | 5.0 V | CLOCK_IN 1/2 | - | H (Note 13) |
| \$06 | L | - | L | L | H | H | L | 5.0 V | CLOCK_IN 1/4 | - | H (Note 13) |
| \$07 | L | - | L | L | H | H | H | 5.0 V | CLOCK_IN 1/8 | - | H (Note 13) |
| \$08 | L | - | L | H | L | L | L | - | START | - | H (Note 13) |
| \$09 | L | - | L | H | L | L | H | - | STOP Low | - | H (Note 13) |
| \$0A | L | - | L | H | L | H | L | - | STOP High | - | H (Note 13) |
| \$0B | L | - | L | H | L | H | H | - | Reserve | - | H (Note 13) |
| \$0C | L | - | L | H | H | L | L | - | - | Normally Open (Note 12) | H (Note 13) |
| \$OD | L | - | L | H | H | L | H | - | - | Normally Close (Note 12) | H (Note 13) |
| \$0E | L | - | L | H | H | H | L | - | - | Normally Close <br> (Note 12) | H (Note 13) |
| \$0F | L | - | L | H | H | H | H | - | - | Normally Close Note 12) | H (Note 13) |
| \$10 | L | - | H | Z | L | L | Z | - | - | - | Card Present |
| \$12 | L | 1 | H | Z | L | H | Z | - | - | - | DC/DC status |
| \$14 | L | - | H | Z | H | L | Z | - | - | - | Vbat |
| \$16 | L | 1 | H | Z | H | H | Z | - | - | - | CRD_VCC |

9. The programmed conditions are latched upon the Chip Select (CS, pin 6) positive going transient.
10. Card clock integrity is guaranteed no spikes whatever be the frequency switching.
11. The STATUS register is not affected when the NCN6000 operates in any of the programming functions.
12. The CRD_VCC and CRD_CLK are not affected when the NCN6000 operates outside their respective decoded logic address.
13. The High Level on STATUS in registors $\$ 00$ to $\$ 0 F$, inclusive, having being implemented to reduce current comsumption but have no other meanings.
14. At turn on, the NCN6000 is initialized with CRD_VCC $=3.0 \mathrm{~V}, \mathrm{CLOCK} \_$IN Ratio $=1 / 1$, CRD_CLK $=$ START, CRD_DET $=$ Normally Open.

## DC/DC Converter and Card Detector Status

The NCN6000 status can be polled when $\overline{\mathrm{CS}}=\mathrm{L}$. Please consult Figures 4 and 5 for a description of input and output signals. The status message is described in Table 4.

Note: in order to cope with a start up under low battery condition, the Vbat OK message uses a negative logic as depicted here below.

Table 4. Card and DC/DC Status Output

| PGM | A1 | A0 | STATUS | Message |
| :---: | :---: | :---: | :--- | :--- |
| HIGH | L | L | LOW | No Card |
| HIGH | L | L | HIGH | Card Present |
| HIGH | L | H | LOW | DC/DC Converter <br> Overloaded |
| HIGH | L | H | HIGH | DC/DC Converter OK |
| HIGH | H | L | LOW | Vbat OK |
| HIGH | H | L | HIGH | Vbat Undervoltage |
| HIGH | H | H | HIGH | CRD_VCC OK |
| HIGH | H | H | LOW | CRD_VCC Undervoltage |



The STATUS pin provides a feedback related to the detection of the card, the state of the DC/DC converter, the Vbat undervoltage and CRD_VCC undervoltage situations. When $\overline{\mathrm{PGM}}=\mathrm{H}$, the STATUS pin returns a High if a card is detected present, a Low being asserted if there is no card inserted. In any case, the external card is not automatically powered up. When the external MPU asserts $\mathrm{PWR} \_\mathrm{ON}=\mathrm{H}$, together with $\overline{\mathrm{CS}}=\mathrm{L}$, the CRD_VCC supply is provided to the card and the state of the DC/DC converter, the Vbat and the CRD_VCC can be polled through the STATUS pin.

## Card Power Supply Timing

At power up, the CRD_VCC power supply rise time depends upon the current capability of the DC/DC converter associated with the external inductor L1 and the reservoir capacitor connected across CRD_VCC and GROUND.

On the other hand, at turn off, the CRD_VCC fall time depends upon the external reservoir capacitor and the peak current absorbed by the internal CMOS transistor built across CRD_VCC and GROUND. These behaviors are depicted in Figure 6. Since these parameters have finite values, depending upon the external constraints, the designer must take care of these limits if the $t_{\mathrm{ON}}$ or the $\mathrm{t}_{\mathrm{OFF}}$ provided by the data sheets does not meet his requirements.

Figure 6. Card Power Supply Turn ON and OFF Timing

## Basic Operating Modes Flow Chart

The NCN6000 brings all the functions necessary to handle data communication between a host computer and the smart card. The built-in Chip Select pin provides a simple way to share the same MPU bus with several card interface. On top of that, the logic control are derived from specific pins, avoiding the risk of mixing up the operation when the interface is controlled by a low end microcontroller.

During the transaction operation, the external MPU takes care of whatever is necessary to he data on the single
bidirectional I/O line. Leaving aside the DC-DC control and associated failures, the NCN6000 does not take any further responsibility in the data transaction.
When the chip operates in the programming mode, the NCN6000 provide a flexible access to set up the CRD_VCC voltage, the CRD_CLK and the CRD_DET smart card signals.
The external micro controller takes care of the smart card transaction and shall handle the interface accordingly.


Figure 7. Operating Modes Flow Chart

## Standby Mode

The Standby Mode allows the NCN6000 to detect a card insertion, keeping the power consumption at a minimum. The power supply CRD_VCC is not applied to the card, until the external controllers set PWR_ON $=\mathrm{H}$ with $\overline{\mathrm{CS}}=\mathrm{L}$.

| Standby Mode <br> Logic Conditions: |  | Card Output: |
| :--- | :--- | :--- |
| $\overline{\text { CS }}$ | $=H$ | CRD_VCC $=0 \mathrm{~V}$ |
| PWR_ON | $=H$ | CRD_CLK $=$ L |
| A0 | $=Z$ | CRD_RST $=$ L |
| A1 | $=Z$ | CRD_IO $=$ L |
| PGM | $=Z$ |  |
| I/O | $=Z$ |  |
| RESET | $=Z$ |  |

When a card is inserted, the internal logic filters the signal present pin 11, then asserts the $\overline{\mathrm{INT}}$ pin to Low if the pulse applied to CRD_DET is longer than $150 \mu \mathrm{~s}$. The external MPU shall run whatever is necessary to handle the card.

The $\overline{\mathrm{INT}}$ is cleared (return to High) when a positive going transition is asserted to either the $\overline{\mathrm{CS}}$ or to the PWR_ON signal logically combined with Chip Select = Low.

## Programming Mode

The programming mode allows the configuration of the card power supply, card clock and Card Detection input logic polarity. These signals (CRD_VCC, CRD_CLK and CRD_DET) are described in the pin description paragraph associated with Tables 1 and 3 and Figures 4 and 8.

| Programming Mode <br> Logic Conditions: |  | Card Output: |
| :---: | :---: | :---: |
| CS | $=\mathrm{L}$ | CRD_VCC $=0 \mathrm{~V}$ |
| PWR_ON | $=\mathrm{L}$ | CRD_CLK $=$ L |
| A0 | = H/L | CRD_RST $=\mathrm{L}$ |
| A1 | = H/L | CRD_IO $=\mathrm{H} / \mathrm{L}$ depending upon |
| PGM | $=\mathrm{L}$ | the previous I/O pin |
| I/O | = L/ H | logic state |
| RESET | $=\mathrm{L} / \mathrm{H}$ |  |

The I/O and $\overline{\text { RESET }}$ pins are not connected to the smart card and become logic inputs to control the NCN6000 programming sequence. The programmed values are latched upon transition of $\overline{\mathrm{CS}}$ from Low to High, $\overline{\mathrm{PGM}}$ being Low during the transition.
When a programming mode is validated by a Chip Select negative going transient, the mode is latched and $\overline{\text { PGM }}$ can be released to High. This latch is automatically reset when $\overline{\mathrm{CS}}$ returns to High.

The logic input signals can be set simultaneously, or one bit a time (using either a STAA or a BSET function), the key point being the minimum delay between the shorter bit and the Chip Select pulse. The programmed value is latched into the NCN6000 register on the $\overline{\mathrm{CS}}$ positive going edge.


Figure 8. Minimum Programming Timings

## Active Mode

In the active mode, the NCN6000 is selected by the external MPU and the STATUS pin can be polled to get the status of either the DC/DC converter or the presence of the card (inserted or not valid). The power is not connected to the card: CRD_VCC $=0 \mathrm{~V}$.

| Active Mode |  |  |  |
| :---: | :---: | :---: | :---: |
| Logic Conditions: |  | Card Output: |  |
| CS | $=\mathrm{L}$ | CRD_VCC | $=0 \mathrm{~V}$ |
| PWR_ON | $=\mathrm{L}$ | CRD_CLK | $=\mathrm{L}$ |
| A0 | $=\mathrm{L}$ | CRD_RS | $=\mathrm{L}$ |
| A1 | $=\mathrm{L}$ | CRD_IO | $=\mathrm{H} / \mathrm{L}$ depending upon |
| PGM | $=\mathrm{H}$ |  | the previous I/O pin |
| I/O | = Z |  | logic state |
| RESET | = Z |  |  |
| STATUS | $=\underset{\text { Insert }}{ }$ |  |  |

The Chip Select pulse [ $\overline{\mathrm{CS}}$ ] will automatically clear the previously asserted $\overline{\mathrm{INT}}$ signal upon the positive going transition.
If a card is present, the MPU shall activate the DC/DC converter by asserting PWR_ON = H. The NCN6000 will automatically run a power up sequence when the CRD_VCC reaches the undervoltage level (either $\mathrm{V}_{\mathrm{C} 5 \mathrm{H}}$ or $\mathrm{V}_{\mathrm{C} 3 \mathrm{H}}$, depending upon the CRD_VCC voltage supply programmed). The CRD_IO, CRD_RST and CRD_CLK pins are validated, according to the ISO7816-3 sequence. The interface is now in transaction mode and the system is ready for data exchange through the I/O and $\overline{\text { RESET lines. }}$ At any time, the micro controller can change the CRD_CLK frequency and mode, or the CRD_VCC value as determined by the card being in use.

## Transaction Mode

During the transaction mode, the NCN6000 maintains power supply and clock signal to the card. All the signal levels related with the card are translated as necessary to cope with the MPU and the card.

The DC/DC converter status and the Vbat state can be monitored on the STATUS by using the A0 and A1 logic inputs as depicted Tables 3 and 4.

```
Transaction Mode
Logic Conditions: Card Output:
\begin{tabular}{lll}
\(\overline{\text { CS }}\) & \(=\) L & CRD_VCC \(=3.0\) or 5.0 V \\
PWR_ON & \(=\) H & CRD_CLK \(=\) CLOCK \\
A0 & \(=\) H & CRD_RST \(=\) H/L \\
A1 & \(=\) H & CRD_IO \(=\) DATA \\
\(\overline{\text { PGM }}\) & \(=\) H & \\
I/O & \(=\) DATA & \\
& TRANSFER & \\
\(\overline{\text { RESET }}\) & \(=\) H/L & \\
STATUS & \(=\) L/H DC/DC & \\
& & status: Fail/Pass?
\end{tabular}
```

To make sure the data are not polluted by power losses, it is recommended to check the state of CRD_VCC before launching a new data transaction. Since $\overline{\mathrm{CS}}=\mathrm{L}$, this is achieved by forcing bits A0 and A1 according to Table 4, and reading the STATUS pin 5.

## Idle Mode

The idle mode is used when a card is powered up ( CRD _VCC $=\mathrm{Vcc}$ ), without communication on going.

| Idle Mode |  |  |
| :---: | :---: | :---: |
| Logic Conditions: |  | Card Output: |
| $\overline{\mathrm{CS}}$ | $=\mathrm{L}$ | CRD_VCC $=3.0$ or 5.0 V |
| PWR_ON | $=\mathrm{H}$ | CRD_CLK = CLOCK active or |
| A0 | $=\mathrm{H}$ | L or H |
| A1 | $=\mathrm{H}$ | CRD_RST = H |
| PGM | $=\mathrm{H}$ | CRD_IO = Z |
| I/O | = Z |  |
| RESET | $=\mathrm{H}$ |  |
| STATUS | = L/H according to the internal register results |  |

## Logic Conditions: Card Output:

In addition, the CRD_CLK signal can be stopped, as depicted in Tables 3 and 4, to minimize the current consumption of the external smart card, leaving CRD_VCC active.

## Power Down Operation

The power down mode can be initiated by either the external MPU (pulling PWR_ON = L) or by one of the internal error condition (CRD_VCC overload or Vbat Low). The communication session is terminated immediately, according to the ISO7816-3 sequence. On the other hand, the MPU can run the Standby mode by forced $\overline{\mathrm{CS}}=\mathrm{H}$.

When the card is extracted, the interface shall detect the operation and run the Power Shut Off of the card as described by the ISO/CEI 7816-3 sequence depicted here after:

ISO7816-3 sequence:
$\Rightarrow$ Force RST to Low
$\Rightarrow$ Force CLK to Low, unless it is already in this state $\Rightarrow$ Force CRD_IO to Low
$\Rightarrow$ Shut Off the CRD_VCC supply
Since the internal digital filter is activated for any card insertion or extraction, the physical power sequence will be activated $150 \mu$ s maximum after the card has been extracted. Of course, such a delay does not exist when the MPU launch the power down intentionally.

The time delay between each negative going signal is 500 ns typical (Figure 10).


Figure 9. Typical Power Down Sequence in the NCN6000 Interface


Figure 10. Power Down Sequence Details

## Card Detection

The card detector circuit provides a $500 \mathrm{k} \Omega$ pull up resistor to bias the CRD_DET pin, yielding a logic High when the pin is left open (assuming a NO switch). The internal logic associated with pin 11 provides an automatic selection of the slope card detection, depending upon the polarity set by the external MPU. At start up, the CRD_DET is preset to cope with Normally Open switch. When a Normally Close switch is used in the card socket, it is mandatory to program the NCN6000 chip during the initialization sequence, otherwise the system will not start if a card was previously inserted. Table 3 gives the programming code for such a function. The next lines provide a typical assembler source to handle this CRD_DET Normally Close polarity:

```
Smart EQU $20 ; NCN6000 Physical CS Address
    LDX #$1000 ; Offset
    LDAA #$09 ; I/O = H, A0 = A1 = L, RESET = H
    STAA smart, X ; Set CRD_DET = Normally Closed
        Switch
```

The CRD_DET polarity can be updated at any time, during the Program Mode sequence ( $\overline{\mathrm{PGM}}=\mathrm{L}$ ), but, generally speaking, is useless since the switch does not change during the usage of the considered module. On the other hand, the card detection switch shall be connected across pin 11 and ground, for any polarity selected.

The transition presents pin 11, whatever be the polarity, is filtered out by the internal digital filter circuit, avoiding false interrupt. In addition to the minimum internal $50 \mu \mathrm{~s}$ timing, the MPU shall provide an additional delay to cope with the mechanical stabilization of the card interface (typically 3 ms ), prior to valid the CRD_VCC supply.
When a card is inserted, the detector circuit asserts $\mathrm{INT}=$ Low as depicted before. When the NCN6000 detects a card extraction, the power down sequence is activated, regardless of the PWR_ON state, and the $\overline{\mathrm{INT}}$ pin is asserted Low. It is up to the external MPU to clear this interrupt by forcing a chip select pulse as depicted in Figure 5.

The $75 \mu$ s delay represent the digital filter built-in the NCN6000 chip being used for the characterization. Any pulse shorter than this delay does not generate an interrupt. However, to guarantee an interrupt will be generated, the CRD_DET signal must be longer than $150 \mu$ s as defined by the specification.

The Chip Select pulse is generated by the external micro controller, the minimum pulse width being $2 \mu \mathrm{~s}$ to make sure the card is detected.

The oscillogram, Figure 11, depicts the behavior for a Normally Open switch, the delay existing between the interrupt negative going state and the $\overline{\mathrm{CS}}$ being Low comes from the particular software latency existing in this particular MPU.


Figure 11. Card Insertion Detection and Interrupt Signals


Figure 12. Card Extraction Detection and Interrupt Signals

When the card is extracted, the CRD_DET signal generates an interrupt, assuming the positive pulse width is longer than the digital filter. The oscillogram, Figure 12, depicts the behavior for a Normally Open switch.

Note: since the internal pull up resistor is relatively high ( $500 \mathrm{k} \Omega$ typical), one must use a $10 \mathrm{M} \Omega$ input impedance probe to read this signal.


Figure 13. Interrupt Acknowledgement During a Card Insertion Detection Sequence

The interrupt signal, provided pin 9, is cleared by a positive going Chip Select signal as depicted by the oscillogram, Figure 13. The $\overline{\mathrm{CS}}$ pulse width is irrelevant, as long as it is larger than $2.0 \mu \mathrm{~s}$, to activate a different sequence. Leaving the interrupt signal Low has no influence
on the internal behavior of the NCN6000, but will be automatically cleared when the DC/DC will be activated by the MPU ( $\overline{\mathrm{CS}}=\mathrm{L}, \mathrm{PWR} \_\mathrm{ON}=$ Positive High transition)

## Power Management

The purpose of the power management is to activate the circuit functions needed to run a given mode of operation, yielding a minimum current consumption on the Vbat supply. In the Standby mode ( $\mathrm{PWR} \_\mathrm{ON}=\mathrm{L}$ ), the power management provides energy to the card detection circuit only. All the card interface pins are forced to ground potential.

In the event of a power up request coming from the external MPU (PWR_ON $=\mathrm{H}, \overline{\mathrm{CS}}=\mathrm{L}$ ), the power manager starts the DC/DC converter.

When the CRD_VCC voltage reaches the programmed value ( 3.0 V or 5.0 V ), the circuit activates the card signals according to the following sequence:

$$
\begin{aligned}
& \text { CRD_VCC } \\
& \Rightarrow \text { CRD_IO } \\
& \quad \Rightarrow C R D \_C L K \\
& \quad \Rightarrow C R D \_R S T
\end{aligned}
$$

The logic level of the data lines are asserted High or Low, depending upon the state forced by the external MPU, when the start up sequence is completed. Under no situation the NCN6000 shall launch automatically a smart card ATR sequence. Assuming PWR_ON $=\mathrm{H}$, the CRD_VCC voltage
is maintained whatever be the logic level presents on Chip Select, pin 6.

At the end of the transaction, asserted by the MPU (PWR_ON $=\mathrm{L}, \overline{\mathrm{CS}}=\mathrm{L}$ ), or under a card extraction, the ISO7816-3 power down sequence takes place:

$$
\begin{aligned}
& \text { CRD_RST } \\
& \Rightarrow \text { CRD_CLK } \\
& \Rightarrow \text { CRD_IO } \\
& \quad \Rightarrow \text { CRD_VCC }
\end{aligned}
$$

When $\overline{\mathrm{CS}}=\mathrm{H}$, the bi-directional I/O line (pins 8 and 15) is forced into the High impedance mode to avoid signal collision with any data coming from the external MPU.

The CRD_VCC voltage is controlled by means of $\overline{\mathrm{CS}}$ and PWR_ON logic signal as depicted Figure 14. The PWR_ON logic level define the CRD_VCC voltage status, the amplitude being the one pre programmed into the chip.
In order to avoid uncontrolled command applied to the smart card, the NCN6000 internal logic circuit, together with the Vbat monitoring, clamps the card outputs until the CRD_VCC voltage reaches the minimum value. During the CRD_VCC slope, all the card outputs are kept Low and no spikes can be write to the smart card. The oscillogram on the right hand side is a magnification of the curves given on the opposite side.


Figure 14. Card Power Supply Control


Figure 15. Smart Card Signals Sequence at Power On

## Vbat Supply Voltage Monitoring

The built-in comparator, associated with the band gap reference, continuously monitors the + Vbat input. During the start up, all the NCN6000 functions are deactivated and no data transfer can take place. When the +Vbat voltage rises above 2.35 V (typical), the chip is activated and all the functions becomes available. The typical behavior is provided here after Figure 16. At this point, the internal Power On Reset signal is activated (not accessible externally) and all the logic signals are forced into the states as defined by Table 3 .

If the + Vbat voltage drops below 2.25 V (typical) during the operation, the NCN6000 generate a Power Down sequence and is forced in a no operation mode. The built-in 100 mV (typical) hysteresis avoids unstable operation when the battery voltage slowly varies around the 2.30 V .

On the other hand, the micro controller can read the STATUS signal, pin 5, to control the state of the battery prior to launch either a NCN6000 programming or an ATR sequence (Table 4).


Note: Drawing is not to scale and voltages are typical. See specifications data for details.
Figure 16. Typical Vbat Monitoring

## DC/DC Converter Operation

The built-in DC/DC converter is based on a modified boost structure to cover the full battery and card operating voltage range. The built-in battery voltage monitor provides an automatic system to accommodate the mode of operation whatever be the Vbat and CRD_VCC voltages. Comparator U3/Figure 17 tracks the two voltages and set up the operating mode accordingly.


Figure 17. Basic DC/DC Structure

When the input voltage Vbat is lower than the programmed CRD_VCC, the system operates under the boost mode, providing the voltage regulation and current limit to the smart card. In this mode, the external inductor, typically $22 \mu \mathrm{H}$, stores the energy to drive the +5.0 V card supply from the external low voltage battery. The
oscillogram, Figure 18, depicts the DC/DC behavior under these two modes of operation.

Beside the DC/DC converter, NMOS Q4 provides a low impedance to ground during the Power Down sequence, yielding the $250 \mu \mathrm{~s}$ maximum switch time depicted in the data sheet.


Figure 18. DC/DC Operating Modes

When the input voltage Vbat is higher than the programmed CRD_VCC, the system operates under a step down mode, yielding the voltage regulation and current limit identical to the boost mode. In this case, the built-in structure turns Off Q1 and inverts the Q2 substrate bias to control the current flowing to the load.These operations are fully automatic and transparent for the end user.

The High and Low limits of the current flowing into the external inductor L1 are sensed by the operational amplifier U1 associated with the internal shunt R1. Since this shunt resistor is located on the hot side of the inductor, the device reads both the charge and discharge of the inductor, providing a clean operation of the converter.

In order to optimize the DC/DC power conversion efficiency, it is recommended to use external inductor with $\mathrm{R}<2.0 \Omega$.

The output capacitor C 1 stores the energy coming from the converter and smooths the CRD_VCC voltage applied to the external card. At this point, care must be observed, beside the micro farad value, to select the right type of capacitor. According to the capacitor's manufacturers, the internal ESR can range from a low $10 \mathrm{~m} \Omega$ to more than $3.0 \Omega$, thus yielding high losses during the $\mathrm{DC} / \mathrm{DC}$ operation, depending upon the technology used to build the capacitor.


Figure 19. Typical DC Operating Current
The standard electrolytic capacitors have the low cost advantage for a relative high micro farad value, but have poor tolerance, high leakage current and high ESR.

The tantalum type brings much lower leakage current together with high capacity value per volume, but cost can be an issue and ESR is rarely better than $500 \mathrm{~m} \Omega$.
The new ceramic type have a very low leakage together with ESR in the $50 \mathrm{~m} \Omega$ range, but value above $10 \mu \mathrm{~F}$ are relatively rare. Moreover, depending upon the low cost ceramic material used to build these capacitors, the thermal coefficient can be very bad, as depicted in Figure 20. The X7R type is highly recommended to achieve low voltage ripple.


Figure 20. Typical Y7R Ceramic Type Value as a Function of the Temperature.

## NCN6000

Based on the experiments carried out during the NCN6000 characterization, the best comprise, at time of printing this document, is to use two $6.8 \mu \mathrm{~F} / 10 \mathrm{~V} /$ Ceramic/X7R capacitor in parallel to achieve the CRD_VCC filtering. The ESR will not extend $50 \mathrm{~m} \Omega$ over the temperature range and the combination of standard parts provide an acceptable $-20 \%$ to $+20 \%$ tolerance,
together with a low cost. Obviously, the capacitor must be SMD type to achieve the extremely low ESR and ESL necessary for this application. Figure 21 illustrates the CRD_VCC ripple observed in the NCN6000 demo board depending upon the type of capacitor used to filter the output voltage.

Table 5. Ceramic/Electrolytic Capacitors Comparison

| Manufacturers | Type/Series | Format | Max Value | Tolerance | Typ. Z @ 500 kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MURATA | CERAMIC/GRM225 | 0805 | $10 \mu \mathrm{~F} / 6.3 \mathrm{~V}$ | $+80 \% /-20 \%$ | $30 \mathrm{~m} \Omega$ |
| VISHAY | Tantalum/594C/593C |  | $10 \mu \mathrm{~F} / 16 \mathrm{~V}$ |  | $450 \mathrm{~m} \Omega$ |
| VISHAY | Electrolytic/94SV |  | $10 \mu \mathrm{~F} / 10 \mathrm{~V}$ | $-20 \% /+20 \%$ | $400 \mathrm{~m} \Omega$ |
|  | Electrolytic Low Cost |  | $10 \mu \mathrm{~F} / 10 \mathrm{~V}$ | $-35 \% /+50 \%$ | $2.0 \Omega$ |



Top Trace $=$ Electrolytic or Tantalum $10 \mu \mathrm{~F}$ Bottom Trace $=$ X7R $10 \mu \mathrm{~F}$ ceramic
The high ripple pulse across CRD_VCC is the consequence of the large ESR of the electrolytic capacitor.

Figure 21. CRD_VCC Ripple as a Function of the Capacitor Technology


Figure 22. External Capacitor Current Charge and CRD_VCC Voltage Ripple.


Figure 23. CRD_VCC Voltage Ripple

## Clock Divider

The main purpose of the built-in clock generator is threefold:

1. Adapts the voltage level shifter to cope with the different voltages that might exist between the MPU and the Smart Card.
2. Provides a frequency division to adapt the Smart Card operating frequency from the external clock source.
3. Controls the clock state according to the smart card specification.
In addition, the NCN6000 adjusts the signal coming from the microprocessor to get the Duty Cycle window as defined by the ISO7816-3 specification.

The logic input pins A0, A1, $\overline{\mathrm{PGM}}, \mathrm{I} / \mathrm{O}$ and $\overline{\mathrm{RESET}}$ fulfill the programming functions when both $\overline{\mathrm{PGM}}$ and $\overline{\mathrm{CS}}$ are

Low. The clock input stage (CLOCK_IN) can handle a 40 MHz frequency maximum, the divider being capable to provide a $1: 8$ ratio. Of course, the ratio must be defined by the engineer to cope with the Smart Card considered in a given application and, in any case, the output clock [CRD_CLK] shall be limited to 20 MHz maximum signal. In order to maximize the CLOCK_IN bandwidth, this pin has no Schmitt trigger input. The simple associated CMOS has a $\mathrm{Vbat} / 2$ threshold level. In order to minimize the $\mathrm{dI} / \mathrm{dt}$ and $\mathrm{dV} / \mathrm{dV}$ developed in the CRD_CLK line, the peak current as been internally limited to 30 mA peak (typical @ $C R D \_V C C=5.0 \mathrm{~V}$ ), hence limited the rise and fall time to 10 ns typical. Consequently, the NCN6000 fulfills the ISO7816 specification up to 10 MHz maximum, but can be used up to 20 MHz when the final application operates in a limited ambient temperature range.


Figure 24. Simplified Frequency Divider and Programming Functions

In order to avoid any duty cycle out of the frequency smart card ISO7816-3 specification, the divider is synchronized by the last flip flop, thus yielding a constant $50 \%$ duty cycle, whatever be the divider ratio. Consequently, the output

CRD_CLK frequency division can be delayed by eight CLOCK_IN pulses and the microcontroller software must take this delay into account prior to launch a new data transaction.


The example given by the oscillogram here above highlights the delay coming from the internal clock duty cycle resynchronization. In this example, the clock is internally divided by 2 prior to be applied to the CRD_CLK pin. Since the clock signal is asynchronous, it is up to the programmer to make sure the next card transaction is not
activated before the CRD_CLK signal has been updated. Generally speaking, such a delay can be derived from the maximum clock frequency provided to the interface, keeping in mind the maximum delay is eight incoming clock pulses.


Figure 25. Clock Programming Examples

The clock can be re-programmed without halting the rest of the circuit, whatever be the new clock divider ratio. In
particular, the CRD_VCC can be applied to the card while the clock is re-programmed.


Figure 26. Command Stop Clock HIGH

The CRD_CLK signal is halted in the High logic state, following the Chip Select positive going transition. Logic Input conditions:
$\begin{array}{ll}\overline{\text { PGM }} & =\text { Low } \\ \overline{\text { RESET }} & \text { Low } \\ \text { I/O } & \text { Low }\end{array}$

A0 = Low
A1 = Low
$\overline{\mathrm{CS}}=$ Low pulsed


Figure 27. Command Stop Clock LOW

The CRD_CLK signal is halted in the Low logic state, following the Chip Select positive going transition. Logic Input conditions:
$\overline{\text { PGM }}=$ Low
A0 = Low
$\overline{\text { RESET }}=$ Low
I/O = High

A1 = Low
$\overline{\mathrm{CS}}=$ Low, pulsed


Figure 28. Command Resume Clock Normal Operation

The CRD_CLK signal is resumed in the normal operation, following the Chip Select positive going transition. The previous halted state is irrelevant and the clock signal is synchronized with the internal clock divider to avoid non CRD_CLK 50\% duty cycle.
$\overline{\text { PGM }}=$ Low
A0 $=$ Low
$\overline{\text { RESET }}=$ High
A1 = Low
I/O = Low
$\overline{\mathrm{CS}}=$ Low, pulsed



回是 1.00 V

Figure 29. Card Clock Rise and Fall Time

Since the CRD_CLK signal can generate very fast transient (i.e. $\mathrm{tr}=2.5 \mathrm{~ns} @ \mathrm{Cp}=10 \mathrm{pF}$ ), adapting the design to cope with the EMV noise specification might be necessary at final check out. Using an external RC network is a way to reduce the dv/dt, hence the EMI noise.

Typically, the external series resistor is $10 \Omega$, the total capacitance being 30 pF to 50 pF

## Bidirectional Level Shifter

The NCN6000 carries out the voltage difference between the MPU and the Smart Card I/O signals. When the start sequence is completed, and if no failures have been detected, the device becomes essentially transparent for the data transferred on the I/O line. To fulfill the ISO7816-3 specification, both sides of the I/O line have built in pulsed circuitry to accelerate the signal rise transient. The I/O line is connected on both side of the interface by a NMOS switch which provide the level shifter and, thanks to its relative high internal impedance, protects the Smart Card in the event of data collision. Such a situation could occurs if either the MPU of the smart card forces a signal in the opposite logic level direction.

When the $\overline{\mathrm{CS}}$ signal goes High, or if the MPU is running any of the programming functions, the built in register holds the previous state presents on the input I/O pin. This


Figure 30. Basic Internal I/O Level Shifter
mechanism is useful to force the CRD_IO card pin in either a High or a Low pre-defined logic state. It is the responsibility of the programmer to set up the I/O line according to the system's activity
Device Q4 provides a low impedance to ground when the CRD_IO line is deactivated. This mechanism avoids noise presence on this line during any of the power operation.
When either side of this level shifter is forced to Low, the externally connected device will be forward biased by the DC current flowing through the pull up resistors as depicted in Figure 30. Since these two resistors will carry $350 \mu \mathrm{~A}$ max each under the worst case conditions, care must be observed to make sure the external device will be capable to handle this level of current. Note: the typical series impedance of the internal MOS device (Q3, Figure 30) is $400 \Omega$.

The oscillograms Figure 31 give the worst case operation when the stray capacitance is 15 pF .


Note: The I/O data depends solely upon the smart card ATR content, the NCN6000 being not involved in these data.

Figure 32. Typical I/O and RST Signals During an ATR Sequence.

## Input Schmitt Triggers

All the Logic Input pins have built-in Schmitt trigger circuits to prevent the NCN6000 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 33.

The output signal is guaranteed to go High when the input voltage is above $0.70 * \mathrm{Vbat}$, and will go Low when the input voltage is below $0.30^{*}$ Vbat.

The CLOCK_IN pin has been design to provide a 40 MHz bandwidth clock receiver input, capable to drive the internal clock divider. This front end circuit yields a constant Duty Cycle signal, according to the ISO specification, to the external smart card, even when the NCN6000 division ratio is $1: 1$.


Figure 33. Typical Schmitt Trigger Characteristic

## Interrupt Function

The NCN6000 flags the external microprocessor by pulling down the $\overline{\mathrm{INT}}$ signal provided in pin 9. This signal is activated by one of the here below referenced operations.

Table 6. Interrupt Functions

|  | Pin Related | Clear Function | STATUS Pin 5 |
| :--- | :---: | :--- | :--- |
| Card Insertion and <br> Extraction | 11 | Positive Going Chip Select, or logical <br> combination of Chip Select Low and <br> PWR_ON Positive Going | High = Card Presents <br> Low $=$ No Card Inserted |
| DC/DC Converter <br> Overloaded | 15 | Positive Going Chip Select, or logical <br> combination of Chip Select Low and <br> PWR_ON Positive Going | High = DC/DC Operates Normally <br> Low $=$ Output CRD_VCC Overloaded |

Leaving the $\overline{\mathrm{INT}}$ pin Low has no influence on the NCN6000 internal behavior. It is up to the engineering to decide when and how the interrupt will be cleared from this pin. As described before, this can be achieved by either
providing a Chip Select positive transient, or by starting the DC/DC converter with the standard command PWR_ON = H and $\overline{\mathrm{CS}}=\mathrm{L}$.

## Security Features

In order to protect both the interface and the external smart card, the NCN6000 provides security features to prevent catastrophic failures as depicted here after.

Pin Current Limitation: In the case of a short circuit to ground, the current forced by the device is limited to 15 mA for any pins, except CRD_CLK pin. No feedback is provided to the external MPU.

DC/DC Operation: The internal circuit continuously senses the CRD_VCC voltage and, in the case of either over or undervoltage situation, update the STATUS register accordingly. This register can be read out by the MPU.

Battery Voltage: Both the Over and Undervoltage are detected by the NCN6000, a POWER_DOWN sequence and the STATUS register being updated accordingly. The external MPU can read the STATUS pin to take whatever is appropriate to cope with the situation.

## ESD Protection

The NCN6000 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built-in structures have been designed to handle either 2.0 kV , when related to the microcontroller side, or 8.0 kV when connected with the external contacts. Practically, the CRD_RST, CRD_CLK, CRD_IO and CRD_DET pins can sustain 8 kV , the digital pins being capable to sustain 2 kV . The CRD_VCC pin has the same 8 kV ESD protection, but can source up to 55 mA continuously, the absolute maximum current being 100 mA .

To save as much battery current as possible when no card is inserted, one should use a Normally Open Card Detection switch connected pin 11. Since the internal card detection circuit source $10 \mu \mathrm{~A}$ (typical) to bias the switch, using a Normally Open avoid this direct sink to ground from the battery.

## Parallel Operation

When two or more NCN6000 operate in parallel on a common digital bus, the Chip Select pin allows the selection of one chip from the bank of the paralleled devices. Of course, the external MPU shall provide one unique $\overline{\mathrm{CS}}$ line for each of the NCN6000 considered interfaces. When a given interface is selected by $\overline{\mathrm{CS}}=\mathrm{L}$, all the logic inputs becomes active, the chip can be programmed or/and the external card can be accessed. When $\overline{\mathrm{CS}}=\mathrm{H}$, all the input logic pins are in the high impedance state, thus leaving the bus available for other purpose. On the other hand, when $\overline{\mathrm{CS}}=\mathrm{H}$, the CRD_IO and CRD_RST hold the previous I/O and $\overline{\text { RESET }}$ logic state, the CRD_CLK being either active or stopped, according to the programmed state forced by the MPU.

Since there is one single I/O line to communicate with the external microcontroller, one should provide a software routine to save the code when data exchanged are performed between the two cards. Generally speaking, the internal microcontroller RAM can be used to support such a transaction.

The CRD_VCC voltage and CRD_CLK signal of each NCN6000 can be operated simultaneously, these two pins being activated even when the related chip select is High. As depicted Figure 14, the DC/DC converter is not deactivated when PWR_ON goes to Low when $\overline{\mathrm{CS}}=$ High.

## Minimum Power Consumption

To achieve a minimum current consumption, the interface shall be programmed as follow:

1. Turn off the DCDC converter : this will disconnect the smart card if still inserted in the socket), reducing the power supply to the minimum needed to control the interface.
2. Force the input signals to a logic High to avoid current flowing through the pull up resistors. This applies to the here below table:

| $\overline{\mathbb{I N T}}$ | Pin 9 |
| :--- | :---: |
| $\overline{\text { CS }}$ | Pin 6 |
| STATUS | Pin 5 |
| I/O | Pin 8 |
| CRD_IO | Pin 14 |

To save as much battery current as possible when no card is inserted, one should use a Normally Open Card Detection switch connected pin 11 to ground. Since the internal card detection circuit source is $10 \mu \mathrm{~A}$ (typical), using such a NO switch saves the direct sink to ground current from the battery to ground.

During this mode of operation, the only active sub functions are the card detection and the battery monitoring. The activity resume immediately after either a card insertion, or a $\overline{\mathrm{CS}}=$ Low signal applied to pin 6 .

## Printed Circuit Board Layout

Since the NCN6000 carries high speed currents together with high frequency clock, the printed circuit board must be carefully designed to avoid the risk of uncontrolled operation of the interface.

A typical single-sided PCB layout is provided in Figure 34 highlighting the ground technique.

The card socket uses a low cost ISO only version, all the parts being located on the Component side. Connector J3 makes reference to the microcontroller used by the final application. Of course, the connector is not necessary and standard copper tracks might be used to connect the MPU to the NCN6000 interface chip.


Figure 34. Typical Single Sided Printed Circuit Board Layout

## Application Note

A partial schematic diagram of the demo board designed to support the NCN6000 applications is depicted Figure 35. This schematic diagram highlights the interface between the micro controller and the Smart Card, leaving aside the peripherals used to control the MPU.

## Conclusion

From a practical stand point, the CRD_VCC output capacitor has been split into two $6.8 \mu \mathrm{~F} / 10 \mathrm{~V} / \mathrm{X} 7 \mathrm{R}$, one being located as close as possible across pins 13 and 17 of the NCN6000, the second one being located close by the smart card physical connector. On the other hand, cares have
been observed to minimize the cross coupling between the clock signals (both Input and CRD_CLK) and the other signals presents on the board.
The micro controller holds the software necessary to program the NCN6000, together with the code handling the T0 operation. Provisions are made to provide a communication link with an external computer by using the RS232 standard port.
Thanks to the Chip Select signal, several NCN6000 can share a common data bus as depicted Figure 36. In this example, two interfaces are connected to a single MPU, the $\overline{\mathrm{CS}}$ pins being controlled by two different signals.


Figure 35. NCN6000 Single Interface Demo Board


Figure 36. NCN6000 Single Interface Demo Board

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## NCN6010

## SIM Card Supply and Level Shifter

The NCN6010 is a level shifter analog circuit designed to translate the voltages between a SIM Card and an external microcontroller. A built-in DC/DC converter makes the NCN6010 useable to drive any type of SIM card. The device fulfills the GSM 11.11 specification. The external MPU has an access to a dedicated input STOP pin, providing a way to switch off the power applied to the SIM card in case of failure or when the card is removed.

## Features

- Supports 3.0 V or 5.0 V Operating SIM Card
- Built-in Pull Up Resistor for I/O Pin in Both Directions
- All Pins are Fully ESD Protected, According to GSM Specification
- Supports 10 MHz Clock
- 6.0 kV ESD Proof on SIM Card Pins


## Typical Applications

- Cellular Phone SIM Interface
- Identification Module



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DIAGRAM

PIN CONNECTIONS


ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCN6010DTB | TSSOP-14 | 96 Units/Rail |
| NCN6010DTBR2 | TSSOP-14 | 2500 Tape \& Reel |

Figure 1. Typical Interface Application

NCN6010


Figure 2. NCN6010 Block Diagram

PIN DESCRIPTIONS

| Pin | Name | Type | Description |
| :---: | :---: | :---: | :---: |
| 1 | $V_{D D}$ | POWER | This pin is connected to the system controller power supply suitable to operate from a 3.6 V typical battery. A low ESR ceramic capacitor ( $4.7 \mu \mathrm{~F}$ typical) shall be used to bypass the power supply voltage. |
| 2 | STOP | INPUT | A Low level on this pin resets the SIM interface, switching off the SIM_VCC, according to the ISO7816-3 Power Down procedure (See Table 1 and Figure 3). |
| 3 | MOD_V ${ }_{\text {cc }}$ | INPUT | The signal present on this pin programs the SIM_VCC value (See Table 1): $\begin{aligned} & \text { MOD_VCC }=\mathrm{L} \rightarrow \text { SIM_VCC }=5.0 \mathrm{~V} \\ & \text { MOD_VCC }=\mathrm{H} \rightarrow \text { SIM_VCC }=3.0 \mathrm{~V} \end{aligned}$ |
| 4 | PWR_ON | INPUT | The signal present on this pin controls the SIM_VCC state (See Table 1): PWR_ON $=\mathrm{L} \rightarrow$ SIM_VCC $=$ Open, no supply connected to the SIM card. PWR_ON $=\mathrm{H} \rightarrow$ SIM_VCC = Active, the card is powered. |
| 5 | I/O | INPUT | This pin is connected to an external microcontroller or GSM management unit. A bi-directional level translator adapts the serial I/O signal between the smart card and the external controller. A built-in constant $20 \mathrm{k} \Omega$ (typical) resistor provides a high impedance state when not activated. |
| 6 | CLOCK | INPUT | The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max values defined by the specification (typically $50 \%$ ). The built-in level shifter translates the input signal to the external SIM card CLK input. |
| 7 | RESET | INPUT | The RESET signal present at this pin is connected to the SIM card. The internal level shifter translates the level according to the voltages present at pin 1 and the SIM_VCC programmed value. |
| 8 | SIM_RST | OUTPUT | This pin is connected to the RESET pin of the card connector. A level translator adapts the external RESET signal to the SIM card. A built-in active pull down connects this pin to ground when the device is in a nonoperating mode. |
| 9 | SIM_CLK | OUTPUT | This pin is connected to the CLK pin of the card connector. The CLOCK signal comes from the external clock generator, the internal level shifter being used to adapt the voltage defined for the SIM_VCC. A built-in active pull down connects this pin to ground when the device is in a nonoperating mode. |
| 10 | GND | GROUND | This pin is the GROUND reference for the integrated circuit and associated signals. Cares must be observed to avoid voltage spikes when the device operates in a normal operation. |
| 11 | SIM_I/O |  | This pin handles the connection to the serial I/O of the card connector. A bi-directional level translator adapts the serial I/O signal between the card and the microcontroller. A $20 \mathrm{k} \Omega$ (typical) pull up resistor provides a High impedance state for the SIM card I/O link. |
| 12 | Cta | POWER | This pin is connected to the external capacitor used by the internal Charge Pump converter. Using Low ESR ceramic type is recommended (X5R or X7R). |
| 13 | Ctb | POWER | This pin is connected to the external capacitor used by the internal Charge Pump converter. Using Low ESR ceramic type is recommended (X5R or X7R). |
| 14 | SIM_VCC | POWER | This pin is connected to the SIM card power supply pin. An internal Charge Pump converter is programmable by the external MPU to supply either 3.0 V or 5.0 V output voltage. An external $1.0 \mu \mathrm{~F}$ minimum ceramic capacitor (ESR $<100 \mathrm{~m} \Omega$, X5R or X7R recommended) must be connected across SIM_VCC and GND. <br> During a normal operation, the SIM_VCC voltage can be set to 3.0 V followed by a 5.0 V value, or can start directly to any of these two values. When the voltage is adjusted downward (from 5.0 V to 3.0 V ) cares must be observed as reverse peak current can flow from the external capacitors to the battery during a short amount of time (in the $1.0 \mu \mathrm{~s}$ range). When such a voltage adjustment is necessary, it is recommended to force SIM_VCC to zero, wait $350 \mu$ s minimum, then reprogram the chip to get SIM_VCC $=3.0 \mathrm{~V}$. |

MAXIMUM RATINGS (Note 1)

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply | $V_{D D}$ | 7.0 | V |
| External Card Power Supply and Level Shifter | SIM_VCC | 7.0 | V |
| Digital Input Voltage Digital Input Current | STOP | $-0.3 \leq \mathrm{V}_{1.0} \leq \mathrm{V}_{\mathrm{DD}}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Input Voltage Digital Input Current | RESET | $-0.3 \leq \mathrm{V}_{1.0} \leq \mathrm{V}_{\mathrm{DD}}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Input Voltage Digital Input Current | CLOCK | $-0.3 \leq \mathrm{V} \leq \mathrm{V}_{\mathrm{DD}}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Input Voltage Digital Input Current | 1/O | $-0.3 \leq \mathrm{V} \leq \mathrm{V}_{\mathrm{DD}}$ | $\begin{gathered} \hline \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Output Voltage Digital Output Current | SIM_RST | $\begin{gathered} -0.3 \leq \mathrm{V} \leq \text { SIM_VCC }_{25} \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Input/Output Voltage Digital Input/Output Current | SIM_I/O | $\begin{gathered} -0.3 \leq \mathrm{V} \leq \text { SIM_VCC } \\ 25 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Output Voltage Digital Output Current | SIM_CLK | $-0.3 \leq \mathrm{V} \leq \text { SIM_VCC }$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Human Body Model: $\mathrm{R}=1500 \Omega$, $\mathrm{C}=100 \mathrm{pF}$ SIM card side, pins 8, 9, 11 \& 14 All other pins | ESD | $\begin{aligned} & 6.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \mathrm{kV} \\ & \mathrm{kV} \end{aligned}$ |
| TSSOP-14 Package <br> Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ <br> Thermal Resistance Junction to Air | $P_{D}$ $R_{\text {THhja }}$ | $\begin{aligned} & 275 \\ & 145 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -25 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $\mathrm{T}_{\text {Jmax }}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$.

POWER SUPPLY SECTION $\left(-25^{\circ} \mathrm{C}\right.$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply | $V_{\text {DD }}$ | 1 | 2.7 | - | 3.6 | V |
| Standby Supply Current @ No Input Clock, All Input Logic to H, No Load Connected to the SIM Interface. | $I V_{D D}$ | 1 | - | 500 | - | nA |
| $\begin{aligned} & \text { Ground Current, @ } \mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V} \text {, Operating Conditions: } \\ & \text { PWR_ON }=0 \\ & \text { SIM_VCC }=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{CC}}=0 \mathrm{~mA} \\ & \text { SIM_VCC }=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{CC}}=10 \mathrm{~mA} \text { (Note 2) } \\ & \text { SIM_VCC }=3.0 \mathrm{~V}, \mathrm{I}_{\mathrm{CC}}=0 \mathrm{~mA} \\ & \text { SIM_VCC }=3.0 \mathrm{~V}, \mathrm{I}_{\mathrm{CC}}=6.0 \mathrm{~mA} \text { (Note 2) } \end{aligned}$ | $1 V_{\text {DD }}$ | 1 | - | $\begin{aligned} & 200 \\ & 40 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 125 \\ & \\ & 25 \end{aligned}$ | $\mu \mathrm{A}$ |
| External Card Power Supply at 5.0 V <br> @ $2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{DD}} \leq 3.6 \mathrm{~V}, \mathrm{I}_{\mathrm{CC}}=10 \mathrm{~mA}$ External Card Power Supply at 3.0 V <br> @ $2.7 \mathrm{~V} \leq \mathrm{V}_{\mathrm{DD}} \leq 3.6 \mathrm{~V}$, $\mathrm{I}_{\mathrm{CC}}=10 \mathrm{~mA}$ | SIM_VCC | 14 | $\begin{gathered} 4.5 \\ V_{D D}-50 \mathrm{mV} \end{gathered}$ | $V_{D D}-25 \mathrm{mV}$ | $\begin{gathered} 5.5 \\ V_{D D} \end{gathered}$ | V |
| Output SIM Card Supply Voltage Turn On Time $\begin{aligned} & \mathrm{Ct}=220 \mathrm{nF}, \text { Cout } 1=1.0 \mu \mathrm{~F} \pm 20 \% \\ & \mathrm{~V}_{\mathrm{DD}}=3.0 \mathrm{~V}, \mathrm{SIM} \text { VCC }=5.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{DD}}=3.0 \mathrm{~V}, \mathrm{SIM} \mathrm{VCCC}=3.0 \mathrm{~V} \end{aligned}$ | VCCTon | 14 | - | 0.5 | 1.0 | ms |
| Output SIM Card Supply Voltage Turn Off Time $\mathrm{Ct}=220 \mathrm{nF}$, Cout $1=1.0 \mu \mathrm{~F} \pm 20 \%$ (Note 3) $\mathrm{V}_{\mathrm{DD}}=2.7 \mathrm{~V}, \mathrm{SIM}_{2} \mathrm{VCC}=5.0 \mathrm{~V}$, @ $\mathrm{V}_{\text {LOW }}=0.4 \mathrm{~V}$ $\mathrm{V}_{\mathrm{DD}}=2.7 \mathrm{~V}$, SIM_VCC $=3.0 \mathrm{~V}$, @ $\mathrm{V}_{\text {LOW }}=0.4 \mathrm{~V}$ | VCC ${ }_{\text {TOFF }}$ | 14 | - | - | $\begin{aligned} & 300 \\ & 300 \end{aligned}$ | $\mu \mathrm{s}$ |
| $\begin{aligned} & \text { Output Voltage Ripple (Note 4) } \\ & \mathrm{Ct}=220 \mathrm{nF}, \mathrm{Cout} 1=1.0 \mu \mathrm{~F}, \mathrm{Cout} 2=100 \mathrm{nF} \\ & \mathrm{~V}_{\mathrm{DD}}=3.0 \mathrm{~V}, \mathrm{SIM} \mathrm{VCC}=5.0 \mathrm{~V}, \mathrm{I}_{\mathrm{CC}}=10 \mathrm{~mA} \\ & \text { (Not Relevant at } \mathrm{SIM} \mathrm{VCC}=3.0 \mathrm{~V} \text { ) } \end{aligned}$ | VCC ${ }_{\text {RIP }}$ | 14 | - | - | 200 | mV |
| Input Peak Current During DC/DC Startup <br> @ $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$, SIM_VCC $^{2} 5.0 \mathrm{~V}$ | $\mathrm{l}_{\text {DDpk }}$ | 1 | - | 300 | - | mA |
| Input Average Current During Normal Operation, @ $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$, SIM_VCC $^{2}=5.0 \mathrm{~V}$ | IdDavg | 1 | - | 20 | - | mA |
| DC/DC Internal Oscillator | Fosc | - | - | 800 | - | kHz |

2. The IDD current represents the absolute difference between the current absorbed by the load and the one absorbed by the chip.
3. A $350 \mu$ s delay must be observed by the external MPU prior to reactivate the SIM_VCC output.
4. Using low ESR capacitors type ( $\max 100 \mathrm{~m} \Omega$ ) is mandatory for Ct, Cout1 and Cout2 to reach the NCN6010 specifications. Ceramic type (X5R or X7R) are recommended.

DIGITAL INPUT SECTION CLOCK, RESET, I/O, STOP, MOD_VCC, PWR_ON

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| High Level Input Voltage | $\mathrm{V}_{\mathrm{IH}}$ | 2,3 | $0.7^{*} \mathrm{~V}_{\mathrm{DD}}$ | - | $\mathrm{V}_{\mathrm{DD}}$ | V |
| Low Level Input Voltage | $\mathrm{V}_{\mathrm{IL}}$ | 4,5 |  |  | $0.3^{*} \mathrm{~V}_{\mathrm{DD}}$ | V |
| Input Rise Time | tr | 6,7 |  |  | 50 | ns |
| Input Fall Time | tf |  |  |  | 50 | ns |
| Input Capacitance | Cin |  |  |  | 10 | pF |
| Input @ 45\% < Duty Cycle < 55\% | CLOCK | 6 | - | - | 5.0 | MHz |
| Clock Rise Time |  |  |  |  | 50 | ns |
| Clock Fall Time |  |  |  | 50 | ns |  |
| Input Clock Capacitance |  |  |  | 10 | pF |  |
| Input/Output Data Transfer Frequency | I/O | 5 | - | 15 | 160 | kHz |
| I/O Rise Time |  |  |  |  | 0.8 | $\mu \mathrm{~s}$ |
| I/O Fall Time |  |  |  | 0.8 | $\mu \mathrm{~s}$ |  |
| Input I/O Capacitance |  |  |  | 10 | pF |  |

SIM INTERFACE SECTION (Note 7)

\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Rating \& Symbol \& Pin \& Min \& Typ \& Max \& Unit \\
\hline ```
SIM_VCC \(=+5.0 \mathrm{~V}\)
Output RESET \(\mathrm{V}_{\mathrm{OH}} @\) Isim_rst \(=+200 \mu \mathrm{~A}\)
Output RESET V \({ }_{\text {OL }}\) @ Isim_rst = \(-200 \mu \mathrm{~A}\)
Output RESET Rise Time @ Cout = 50 pF
Output RESET Fall Time @ Cout = 50 pF
SIM_VCC = +3.0 V
Output RESET \(\mathrm{V}_{\text {OH }} @\) Isim_rst = +200 \(\mu \mathrm{A}\)
Output RESET VoL@ Isim_rst =-200 \(\mu \mathrm{A}\)
Output RESET Rise Time @ Cout = 50 pF
Output RESET Fall Time @ Cout = 50 pF
``` \& SIM_RST Note 5 \& 8 \& \[
\begin{gathered}
\text { SIM_VCC }-0.7 \\
0
\end{gathered}
\]
\[
0.8 \text { * } \underset{0}{\text { SIM_VCC }}
\] \& - \& SIM_VCC
0.6
400
400
SIM_VCC
0.2 * SIM_VCC
400
400 \& \[
\begin{gathered}
\mathrm{V} \\
\mathrm{~V} \\
\mathrm{~ns} \\
\mathrm{~ns}
\end{gathered}
\] \\
\hline ```
SIM_VCC \(=+5.0 \mathrm{~V}\)
Output Duty Cycle
Output Frequency
Output SIM_CLK Rise Time @ Cout = 50 pF
Output SIM_CLK Fall Time @ Cout = 50 pF
Output \(\mathrm{V}_{\text {OH }} @\) Isim_clk \(=+20 \mu \mathrm{~A}\)
Output \(\mathrm{V}_{\mathrm{OL}} @\) Isim_clk = \(-200 \mu \mathrm{~A}\)
SIM_VCC \(=+3.0 \mathrm{~V}\)
Output Duty Cycle
Output Frequency
Output SIM_CLK Rise Time @ Cout = 50 pF
Output SIM_CLK Fall Time @ Cout = 50 pF
Output \(\mathrm{V}_{\mathrm{OH}} @\) Isim_clk = +20 \(\mu \mathrm{A}\)
Output \(\mathrm{V}_{\text {OL }} @\) Isim_clk \(=-20 \mu \mathrm{~A}\)
``` \& \begin{tabular}{l}
SIM_CLK \\
Note 5 \\
Note 6
\end{tabular} \& 9 \& \[
\begin{gathered}
40 \\
0.7 \text { * } \begin{array}{c}
\text { SIM_VCC } \\
0
\end{array} \\
40 \\
\\
\begin{array}{c}
0.7 \\
\text { * } \\
0 \\
\text { SIM_VCC }
\end{array}
\end{gathered}
\] \& - \& 60
5.0
18
18
SIM_VCC
0.5
60
5.0
18
18
SIM_VCC
0.2 *SIM_VCC \& \[
\begin{gathered}
\text { \% } \\
\mathrm{MHz} \\
\mathrm{~ns} \\
\mathrm{~ns} \\
\mathrm{~V} \\
\mathrm{~V} \\
\\
\\
\% \\
\mathrm{MHz} \\
\mathrm{~ns} \\
\mathrm{~ns} \\
\mathrm{~V} \\
\mathrm{~V}
\end{gathered}
\] \\
\hline ```
SIM_VCC = +5.0 V
SIM_I/O Data Transfer Frequency
SIM_I/O Rise Time @ Cout = 50 pF
SIM_I/O Fall Time @ Cout = 50 pF
Output \(\mathrm{V}_{\mathrm{OH}} @ \mathrm{I}_{\mathrm{SIM} \_I O}=+20 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{V}_{\mathrm{DD}}\)
Output \(\mathrm{V}_{\mathrm{OL}} @ \mathrm{I}_{\text {SIM_IO }}=-1.0 \mathrm{~mA}\),
\(\mathrm{V}_{\mathrm{IL}} \mathrm{I} / \mathrm{O}=0 \mathrm{~V}\)
SIM_VCC \(=+3.0 \mathrm{~V}\)
SIM_I/O Data Transfer Frequency
SIM_I/O Rise Time @ Cout = 50 pF
SIM_I/O Fall Time @ Cout = 50 pF
Output \(\mathrm{V}_{\mathrm{OH}} @ \mathrm{I}_{\mathrm{SIM} \_I O}=+20 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{IH}}=\mathrm{V}_{\mathrm{DD}}\)
Output \(\mathrm{V}_{\text {OL }} @ \mathrm{I}_{\text {SIM } \_ \text {IO }}=-1.0 \mathrm{~mA}\),
\(\mathrm{V}_{\mathrm{IL}} \mathrm{I} / \mathrm{O}=0 \mathrm{~V}\)
``` \& SIM_I/O \& 11 \& \[
\underset{0}{0.7} \underset{0}{\text { * SIM_VCC }}
\]
\[
\frac{0.7}{\text { * }} \underset{0}{\text { SIM_VCC }}
\] \& 15

15 \& 160
0.8
0.8
SIM_VCC
0.4

160
0.8
0.8
SIM_VCC

0.4 \& | kHz |
| :--- |
| $\mu \mathrm{s}$ |
| $\mu \mathrm{s}$ |
| V |
| V |
| kHz |
| $\mu \mathrm{s}$ |
| $\mu \mathrm{s}$ |
| V |
| V | <br>

\hline I/O Pull Up Resistor \& I/O_RP \& 5 \& 13 \& 20 \& - \& k $\Omega$ <br>
\hline Card I/O Pull Up Resistor \& SIM_I/O_RP \& 11 \& 13 \& 20 \& - \& k $\Omega$ <br>
\hline
\end{tabular}

5. Internal NMOS device, biased to $V_{D D}$, provides low impedance when SIM_V $V_{C C}$ is disconnected to sustain GSM 11.11-200 $\mu \mathrm{A}$ input current test.
6. The SIM_CLK clock can operate up to 10 MHz , but the rise and fall time are not guaranteed to be fully within the ISO7816 specification over the temperature range. Typically, tr and tf are 12 ns @ CRD_CLK $=10 \mathrm{MHz}$.
7. Digital inputs undershoot $<-0.30 \mathrm{~V}$, Digital inputs overshoot $<0.30 \mathrm{~V}$.

## Card Supply Charge Pump Converter

The NCN6010 device provides three pins to control the operation of the interface as depicted in Table 1. The built-in charge pump converter circuit provides either a 3.0 V or a 5.0 V output voltage as defined by the programming mode. The external capacitor connected across pins 12 and 13 is used to generate the step up voltage. Since the device operates at 800 kHz typically, one must use high quality, Low ESR type, ceramic capacitor ( 220 nF recommended). The second external capacitor, connected across pin 14 and GND, smooths the output voltage coming from the Charge Pump. A high quality, Low ESR capacitor is necessary to achieve the SIM_VCC ripple voltage ( $1.0 \mu \mathrm{~F}$ Ceramic type is recommended).

The setting of the SIM_VCC voltage, using MOD_VCC $=0$ or 1 , can only be made when PWR_ON is Low. Consequently, a new supply voltage adjustment is performed by first deactivating the SIM card, followed by reactivating it with the new supply voltage. The SIM_VCC voltage can be reprogrammed straightforward when the output voltage increases from 3.0 V to 5.0 V . On the other
hand, although it is possible to change the SIM_VCC voltage from 5.0 V to 3.0 V , it is recommended to switch off the Charge Pump prior to reprogram the SIM_VCC voltage from the high 5.0 V to a low 3.0 V .
The DC/DC converter operates under two modes as defined by the logic level present at MOD_VCC/pin 3:
MOD_VCC $=0$ SIM_CC $=5.0 \mathrm{~V}, \pm 10 \%$. This is the default condition at start up.

MOD_VCC = 1 The Charge Pump is not activated and the SIM_VCC voltage is equal to the $\mathrm{V}_{\mathrm{DD}}$ supply minus the internal maximum 50 mV drop.

The NCN6010 provides a POWER DOWN sequence, according to the ISO7816-3 specification.

Since a built-in active pull down MOS pull the SIM_VCC pin to ground when the smart card is deactivated, a $350 \mu \mathrm{~s}$ minimum delay must be observed prior to reactivate the power supply. This timing assumes a $1.0 \mu \mathrm{~F}$ external reservoir capacitor connected across SIM_VCC and Ground.

Table 1. Programming Functions

| STOP | MOD_VCC | PWR_ON | Operation Mode |
| :---: | :---: | :---: | :--- |
| 0 | X | X | The SIM card supply is disabled, the SIM_VCC pin is Open, SIM_RST $=$ L, <br> SIM_I/O $=\mathrm{L}$, SIM_CLK $=\mathrm{L}$ |
| 1 | 0 | 0 | The NCN6010 is in the power down mode. The SIM card supply is disabled, <br> SIM_VCC = Open, SIM_RST $=$ L, SIM_CLK $=$ L, SIM_IO $=$ L. <br> The SIM_VCC voltage is programmed to 5.0 V. |
| 1 | 1 | 0 | The NCN6010 is in the power down mode. The SIM card supply is disabled, <br> SIM_VCC = Open, SIM_RST $=$ L, SIM_CLK $=$ L, SIM_IO $=$ L. <br> The SIM_VCC voltage is programmed to 3.0 V. |
| 1 | X | 1 | The NCN6010 is in normal operating mode. The SIM card supply is enabled, SIM_VCC <br> voltage is the one previously programmed, all the SIM interface pins are active. |

## Table 1: Programming Mode

When the card is removed, the STOP pin shall be asserted Low to disable the NCN6010. A mechanical switch, or equivalent, can be either sensed by the MPU, or directly connected to pin 2 , to handle the procedure.

## Power Up Sequence

When the charge pump is activated, MOD_VCC = Low, the SIM card related level shifter pins are biased to the 5.0 V
voltage. When the output voltage starts from zero, as depicted in Figure 3, a $50 \mu$ s stabilization delay (typical) is necessary to make sure all the output signals are biased at the nominal 5.0 V voltage. To avoid a card transaction error, the user must take this delay into account and program the chip accordingly.


Figure 3. Power On Sequence

## Power Down Operation

The power down mode can be initiated by either the PWR_ON or by the STOP pin condition. In both cases, the communication I/O session is terminated immediately, according to the ISO7816-3 sequence as depicted in Figure 4. When the PWR_ON signal is set Low, the NCN6010 goes to the power down mode. According to the ISO7816-3 procedure defined to deactivate the SIM contacts, the input pins I/O, CLOCK and RESET must be Low before the PWR_ON is taken Low. When the

PWR_ON is Low, the SIM_IO, SIM_CLK and SIM_RST pins are forced to Low and the SIM_VCC pin is left floating.
When the STOP signal is Low, the SIM_IO, SIM_CLK and SIM_RST are forced Low, the SIM_VCC being left floating, until the STOP pin is taken High again.

When the card is extracted, the external MPU shall detect the operation and run the Power Down of the card by forcing PWR_ON input to Low. The NCN6010 fulfills the power sequence as defined by the ISO/CEI 7816-3 norm (see oscillogram given in Figure 5).

Force SIM RST to Low
Force SIM_CLK to Low, unless it is already in this state
Force SIM IO to Low
Shut Off the SIM_V ${ }_{C C}$ supply


Figure 4. ISO7816-3 Power Down Sequence


Figure 5. Power Down Sequence Oscillogram

## Level Shifters

When the SIM card voltage is either higher or lower than the MPU $V_{D D}$ supply, the level shifters can be reprogrammed to cope with the expected output voltage. When the MPU and the SIM card operate under the same supply voltage, the DC/DC converter is not activated (SIM_VCC $=\mathrm{V}_{\mathrm{DD}}-50 \mathrm{mV}$ ) and the signals go directly through the level shifters.

The bi-directional I/O line provides a way to automatically adapt the voltage difference between the $\mu \mathrm{CU}$ and the SIM card. In addition with the pull up resistor, an active pull up circuit (Figure 6 Q1 and Q2) provides a fast charge of the stray capacitance, yielding a rise time fully within the ISO/EMV specifications.


Figure 6. Basic I/O Line Interface

The typical waveform provided in Figure 7 shows how the accelerator operates. During the first 200 ns (typical), the slope of the rise time is solely a function of the pull up resistor associated with the stray capacitance. During this period, the PMOS devices are not activated since the input voltage is below their Vgs threshold. When the input slope
crosses the Vgsth, the opposite one shot is activated, providing a low impedance to charge the capacitance, thus increasing the rise time as depicted in Figure 7. The same mechanism applies for the opposite side of the line to make sure the system is optimum.


Figure 7. SIM_IO Rise and Fall Time Oscillogram

## Input Schmitt Triggers

All the Logic Input pins have built-in Schmitt trigger circuits to prevent the NCN6010 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 8.

The output signal is guaranteed to go High when the input voltage is above $0.70^{*} \mathrm{Vbat}$, and will go Low when the input voltage is below $0.30 *$ Vbat.


Figure 8. Typical Schmitt Trigger Characteristic

## Charge Pump Converter

The converter uses a switched capacitor technique to increase the SIM_VCC voltage up to 5.0 V from a 3.3 V typical battery. The concept, depicted in Figure 9, charges the transfer capacitor C1 up to the Vcc value, then connects this capacitor is series with the input voltage-output
reservoir network. The voltage developed across the load is, theoretically, twice the battery voltage, but the system must takes into account the losses associated with the power switches and the internal ohmic drops.


Figure 9. Basic Charge Pump Converter

When the output voltage is programmed to 3.0 V , the clocks are inactive and the load is directly connected to the battery by means of switch S5. The SIM_VCC voltage follows the input value, minus the drop coming from the internal resistance. The current is limited by the Ron of the power device S 5 and t he output voltage will decrease as the load current increases above 20 mA (typical). Figure 10 illustrates the theoretical waveforms.


Figure 10. Basic Charge Pump Operating Timings

When the NCN6010 is programmed in the 5.0 V output voltage, the clocks are activated, switch S5 is disconnected and the output voltage is the result of the C 1 charge transfer into the output load. The current is limited by three mains parameters:

- the Ron of the switching MOS (S1 through S4)
- the operating frequency
- the C1/C2 ratio and their ESR

The first parameters are depending upon the internal structure and size of the NMOS/PMOS devices used to
design the chip. The third parameter is adjustable by the user and, beside the micro farad values, the type of capacitors plays a significant role. As a matter of fact, using a low cost electrolytic model will ruin the efficiency due to the high ESR of such a capacitor. It is highly recommended to use ceramic types, preferably from the X5R or X7R series, to achieve the efficiency and the SIM_VCC output voltage ripple. Table 2 summarizes the characteristics of the most common type of capacitors.

Table 2. Comparison of Capacitor Types

| Manufacturers | Type/Serie | Format | Max Value | Tolerance | Typ. Z @ 500 kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MURATA | CERAMIC/GRM225 | 0805 | $10 \mu \mathrm{~F} / 6.3 \mathrm{~V}$ | $+80 \% /-20 \%$ | $30 \mathrm{~m} \Omega$ |
| VISHAY | Tantalum/594C/593C | 1206 | $10 \mu \mathrm{~F} / 16 \mathrm{~V}$ | - | $450 \mathrm{~m} \Omega$ |
| VISHAY | Electrolytic/94SV | 1206 | $10 \mu \mathrm{~F} / 10 \mathrm{~V}$ | $-20 \% /+20 \%$ | $400 \mathrm{~m} \Omega$ |

It is clear that, with nearly half an ohm of resistance is series with the pure capacitor, the tantalum or the electrolytic type will generate high voltage spikes and poor regulation in the high frequency operating charge pump built into the NCN6010. Moreover, with ESR in the 3.0 Ohm range, low cost capacitors are not suitable for this application.

Figure 11 provides the schematic diagram of the simulated charge pump circuit. Although this schematic does not
represent the accurate internal structure of the NCN6010, it can be used for engineering purpose. The ABM devices S 1 , S2, S4 and S5 have been defined in the PSPICE model to represent the NMOS and PMOS used in the silicon. The ESR value of C2 and C3 can be adjusted, at PSPICE level, to cope with any type of external capacitors and are useful to double check the behavior of the system as a function of the external passives components.


Figure 11. Charge Pump Simulation Schematic Diagram

## NCN6010

The operating waveforms are given in Figure 12 to illustrate the high peak current flowing in the transfer
capacitor. The real ripple voltage, coming from the engineering board, is given in Figure 13.


Figure 12. Simulated Charge Pump Typical Waveforms


Figure 13. SIM_VCC Output Voltage Ripple @ lout = 10 mA


Figure 14. Engineering Test Board

The layout of the PCB is a key parameter to avoid the voltage spikes that could pollute the rest of the system. Figure 16 represents a typical printed circuit lay out, based on the schematic diagram given in Figure 14, highlighting the large ground plane used in this engineering tool.

Obviously, a GSM application will use much less area, but cares must be observed to locate the capacitors as close as possible to the integrated circuit associated pins.

Capacitors C1, C2, C3, C4 and C5 are ceramic, X7R, 10 V, surface mount.


Figure 15. Engineering Test Board Silk Layer


Figure 16. Engineering Test Board Top Layer

## NCN6011

## Low Power Level Shifter

The NCN6011 is a level shifter analog circuit designed to translate the voltages between a SIM Card and an external microcontroller. The device handles all the signals needed to control the data transaction between the external Card and the MPU.

## Features

- 2.7 to 6.0 V Input and/or Output Voltage Range
- 500 nA Quiescent Supply Current
- All Pins are Fully ESD Protected
- Supports 10 MHz Clock
- Provides a Logic I/O Enable Function
- Rx/Tx Communication Capability

Typical Applications

- SIM/GSM/SMARTCARD Interface


Figure 1. Typical Interface Application


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See detailed ordering and shipping information in the package dimensions section on page 3313 of this data sheet.


NOTES:

1. Numbers in parenthesis adjacent to the pins are related to the TSSOP-14 package.
2. TSSOP-14 package Pins 1, 7, 8 and 14 are not connected.

Figure 2. Block Diagram

## ABBREVIATIONS

| CLOCK | Input Logic Clock |
| :--- | :--- |
| RESET | Input Logic Reset |
| VDD | Interface Power Supply Input |
| SIM_VCC | Interface IC Card Power Supply Output |
| SIM_CLK | Interface IC Card Clock Output |
| SIM_RST | Interface IC Card Reset Output |
| SIM_IO | Interface IC Card I/O Signal Line |
| Class A | 5.0 V Smart Card |
| Class B | 3.0 V Smart Card |

PIN DESCRIPTIONS (Pin numbers in parenthesis are related to the TSSOP-14 package) (Pin numbers in bold are related to the MIcro-10 package)

| Pin | Name | Type | Description |
| :---: | :---: | :---: | :---: |
| (1) | - | NA | No Connection. (TSSOP-14 Only) |
| $\begin{gathered} 1 \\ (2) \end{gathered}$ | I/O | INPUT | This pin is connected to an external microcontroller. A bidirectional level translator adapts the serial I/O signal between the smart card and the external controller. A built-in constant $20 \mathrm{k} \Omega$ typical resistor provides a high impedance state when not activated. |
| $\begin{gathered} \mathbf{2} \\ (3) \end{gathered}$ | $V_{D D}$ | POWER | This pin is connected to the system controller power supply and the input voltage can range from 2.7 to 6.0 V . |
| $\begin{gathered} \hline 3 \\ (4) \end{gathered}$ | CLOCK | INPUT | The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max limits defined by the specification (typically $50 \%$ ). The built-in level shifter translates the input signal to the external SIM card voltage supply. |
| $\begin{gathered} \hline \mathbf{4} \\ (5) \end{gathered}$ | RESET | INPUT | The RESET signal present at this pin is provided by the MPU. The internal level shifter translates the level according to the voltages applied to pin 3 and pin 12. |
| $\begin{gathered} \mathbf{5} \\ (6) \end{gathered}$ | IO_ENABLE | INPUT | This logic input pin forces SIM_IO pin to Low when IO_ENABLE = Low, leaving this signal High when IO_ENABLE = High. The signal is not latched and the SIM_IO pin is released to a logic High when IO_ENABLE = High. When this condition is met, the SIM_IO logic status depends upon the signal presence pin I/O. When the MPU uses two different channels to exchange data with the SIM card, the IO_ENABLE pin can be used to as a Write line to the external card, the I/O pin being used to Read data from the SIM card. |
| (7) | - | NA | No Connection. (TSSOP-14 Only) |
| (8) | - | NA | No Connection. (TSSOP-14 Only) |
| $\begin{gathered} \hline \mathbf{6} \\ (9) \end{gathered}$ | GND | GROUND | This pin is the GROUND reference for the integrated circuit and associated signals. High frequency layout techniques are requested to connect the GND pin to the external functions. |
| $\begin{gathered} 7 \\ (10) \end{gathered}$ | SIM_RST | OUTPUT | This pin is connected to the RST pin of the card connector. A voltage level translator adapts the external RESET signal (coming from the MPU) to the smart card. |
| $\begin{gathered} \hline 8 \\ (11) \end{gathered}$ | SIM_CLK | OUTPUT | This pin is connected to the CLK pin of the card connector. The CLOCK signal comes from the external clock generator. The internal voltage level shifter adapts the clock signal flowing through this link. Care must be observed to prevent AC coupling with adjacent lines and signals PCB tracks. |
| $\begin{gathered} 9 \\ (12) \end{gathered}$ | SIM_VCC | POWER | This pin is connected to the smart card VCC power supply pin. The voltage, provided by an external power supply, can range from 2.7 V to 6.0 V. The NCN6011 does not regulate or protect the voltage supply applied to the external card. |
| $\begin{gathered} 10 \\ (13) \end{gathered}$ | SIM_I/O | OUTPUT | This pin handles the connection to the serial I/O of the card connector. A bidirectional voltage level translator adapts the serial I/O signal between the card and the microcontroller. A $20 \mathrm{k} \Omega$ typical pull up resistor provides a High impedance state for the SIM card I/O link. |
| (14) | - | NA | No Connection. (TSSOP-14 Only) |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Power Supply | $V_{\text {DD }}$ | 7.0 V | V |
| External Card and Level Shifter Power Supply | SIM_VCC | 7.0 V | V |
| Digital Input Voltage Digital Input Current | $\begin{gathered} \text { RESET, } \\ \text { IO_ENABLE } \end{gathered}$ | $-0.3 \leq \underset{1.0}{\mathrm{~V}} \leq \mathrm{V}_{\mathrm{DD}}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Input Voltage Digital Input Current | CLOCK | $-0.3 \leq \underset{1.0}{\mathrm{~V}} \leq \mathrm{V}_{\mathrm{DD}}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Input Voltage Digital Input Current | I/O | $-0.3 \leq \mathrm{V}_{1.0} \leq \mathrm{V}_{\mathrm{DD}}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Output Voltage Digital Output Current | SIM_RST | $-0.3 \leq \mathrm{V} \leq \text { SIM_VCC }$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Output/Input Voltage Digital Output/Input Current | SIM_I/O | $-0.3 \leq \mathrm{V} \leq \text { SIM_VCC }_{25}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Digital Output Voltage Digital Output Current | SIM_CLK | $\begin{gathered} -0.3 \leq \mathrm{V} \leq \text { SIM_VCC }_{50} \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~mA} \end{gathered}$ |
| Human Body Model: $\mathrm{R}=1500 \Omega, \mathrm{C}=100 \mathrm{pF}$ <br> SIM card side, pins 7, 8, 9,10 ( $10,11,12,13$ ) <br> All other pins | ESD | $\begin{aligned} & 4.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & \mathrm{kV} \\ & \mathrm{kV} \end{aligned}$ |
| Micro-10 Package <br> Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ <br> Thermal Resistance Junction to Air | $P_{D}$ $R_{\text {Thhja }}$ | $200$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| TSSOP-14 Package <br> Power Dissipation @ $\mathrm{T}_{\mathrm{A}}=+85^{\circ} \mathrm{C}$ <br> Thermal Resistance Junction to Air | $P_{D}$ $R_{\text {THhja }}$ | $\begin{aligned} & 320 \\ & 125 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Ambient Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}$ | -25 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $\mathrm{T}_{\text {Jmax }}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

Maximum electrical ratings define the values beyond which permanent damage(s) may occur internally to the chip regardless of the operating temperature. Pin numbers in parenthesis are related to the TSSOP-14 package.

POWER SUPPLY SECTION ( $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ ambient temperature, unless otherwise noted)
(Pin numbers in parenthesis are related to the TSSOP-14 package)
(Pin numbers in bold are related to the MIcro-10 package)

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Power Supply | $V_{D D}$ | $\begin{gathered} \hline \mathbf{2} \\ (3) \end{gathered}$ | 2.7 | - | 6.0 | V |
| Standby Supply Current, CLOCK = L, I/O = H, SIM_VCC = 3.0 V, No SIM Card Inserted | IVDD | $\begin{gathered} \mathbf{2} \\ (3) \end{gathered}$ | - | 0.5 | 2.0 | $\mu \mathrm{A}$ |
| Input External Power Supply | SIM_VCC | $\begin{gathered} 9 \\ (12) \end{gathered}$ | 2.7 | - | 6.0 | V |
| Standby Current, SIM_VCC = 3.0 V, I/O = H, No SIM Card Inserted, CLOCK = L | Ivcc | $\begin{gathered} 9 \\ (12) \end{gathered}$ | - | 0.2 | 0.5 | $\mu \mathrm{A}$ |
| Power Supply Normal Operating Current @ VDD $=+5.0 \mathrm{~V}$, SIM_VCC $=+5.0 \mathrm{~V}$, CLOCK $=5.0 \mathrm{MHz}$, RESET $=\mathrm{H}$, IO_ENABLE $=\mathrm{H}, \mathrm{I} / \mathrm{O}$ Data $=100 \mathrm{kHz}$ | IDD | $\begin{gathered} \hline \mathbf{2} \\ \text { (3) } \end{gathered}$ | - | 230 | - | $\mu \mathrm{A}$ |
| Power Supply Normal Operating Current @ VDD $=+5.0 \mathrm{~V}$, SIM $\mathrm{VCC}=+5.0 \mathrm{~V}$, CLOCK $=5.0 \mathrm{MHz}$, RESET $=\mathrm{H}$, IO_ENABLE $=\mathrm{H}, \mathrm{I} / \mathrm{O}$ Data $=\mathrm{H}$ | IDD | $\begin{gathered} \hline \mathbf{2} \\ \text { (3) } \end{gathered}$ | - | 80 | - | $\mu \mathrm{A}$ |
| $\begin{aligned} & \text { Card Level Shifter Operating Current } \\ & @ \text { VDD }=+5.0 \mathrm{~V}, \text { SIM VCC }=+5.0 \mathrm{~V}, \\ & \text { CLOCK }=5.0 \mathrm{MHz} \text {, RESET }=\mathrm{H}, \\ & \text { IO_ENABLE }=\mathrm{H}, \mathrm{I} / \mathrm{O} \text { Data }=100 \mathrm{kHz} \end{aligned}$ | Icc | $\begin{gathered} 9 \\ (12) \end{gathered}$ | - | 1.50 | - | mA |
| Card Level Shifter Operating Current $\begin{aligned} & @ \text { VDD }=+5.0 \mathrm{~V}, \text { SIM_VCC }=+5.0 \mathrm{~V}, \\ & \mathrm{CLOCK}=5.0 \mathrm{MHz}, \text { RESET }=\mathrm{H}, \\ & \text { IO_ENABLE }=\mathrm{H}, \mathrm{I} / \mathrm{O} \text { Data }=\mathrm{H} \end{aligned}$ | $I_{\text {cc }}$ | $\begin{gathered} \hline 9 \\ (12) \end{gathered}$ | - | 1.30 | - | mA |

DIGITAL INPUT SECTION: CLOCK, RESET, I/O, IO_ENABLE
( $-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ ambient temperature, unless otherwise noted) (Note 1)

| Rating | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLOCK, RESET, IO_ENABLE <br> High Level Input Voltage Low Level Input Voltage Input Rise Time Input Fall Time Input Capacitance | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \\ & \mathrm{tr} \\ & \mathrm{tf} \\ & \mathrm{Cin} \end{aligned}$ | $\begin{aligned} & 1,3, \\ & 4,5 \\ & (2,4, \\ & 5,6) \end{aligned}$ | $0.7{ }^{*} V_{\text {DD }}$ | - | $\begin{gathered} V_{C C} \\ 0.3 * V_{D D} \\ 50 \\ 50 \\ 10 \end{gathered}$ | $\begin{gathered} \mathrm{V} \\ \mathrm{~V} \\ \mathrm{~ns} \\ \mathrm{~ns} \\ \mathrm{pF} \end{gathered}$ |
| Input @ Duty Cycle = 50\% $\pm 1 \%$ (Note 2) <br> Clock Rise Time <br> Clock Fall Time <br> Input Clock Capacitance | CLOCK | $\begin{gathered} \hline 3 \\ (4) \end{gathered}$ | - | - | $\begin{aligned} & 5.0 \\ & 50 \\ & 50 \\ & 10 \end{aligned}$ | $\begin{gathered} \mathrm{MHz} \\ \mathrm{~ns} \\ \mathrm{~ns} \\ \mathrm{pF} \end{gathered}$ |
| Input/Output Data Transfer Frequency <br> I/O Rise Time <br> I/O Fall Time <br> Input I/O Capacitance | 1/O | $\begin{gathered} \hline \mathbf{1} \\ (2) \end{gathered}$ | - | - | $\begin{aligned} & 160 \\ & 0.8 \\ & 0.8 \\ & 10 \end{aligned}$ | $\begin{gathered} \hline \mathrm{kHz} \\ \mu \mathrm{~s} \\ \mu \mathrm{~s} \\ \mathrm{pF} \end{gathered}$ |

1. Digital inputs undershoot $<-0.30 \mathrm{~V}$, Digital inputs overshoot $<0.30 \mathrm{~V}$.
2. The SIM_CLK clock can operate up to 10 MHz , but, in this case, the rise and fall time are not guaranteed to be fully within the GSM specification over the temperature range.

SIM INTERFACE SECTION (Note 3)

\begin{tabular}{|c|c|c|c|c|c|c|}
\hline Rating \& Symbol \& Pin \& Min \& Typ \& Max \& Unit \\
\hline ```
SIM_VCC = +5.0 V
Output RESET \(\mathrm{V}_{\mathrm{OH}} @\) Irst \(=+200 \mu \mathrm{~A}\)
Output RESET \(\mathrm{V}_{\mathrm{OL}} @\) Irst \(=-200 \mu \mathrm{~A}\)
Output RESET Rise Time @ Cout = 30 pF
Output RESET Fall Time @ Cout = 30 pF
SIM_VCC = +3.0 V
Output RESET \(\mathrm{V}_{\mathrm{OH}} @\) Irst \(=+200 \mu \mathrm{~A}\)
Output RESET V \({ }_{\text {OL }}\) @ Irst \(=-200 \mu \mathrm{~A}\)
Output RESET Rise Time @ Cout = 30 pF
Output RESET Fall Time @ Cout = 30 pF
``` \& SIM_RST \& \[
\begin{gathered}
7 \\
(10)
\end{gathered}
\] \& \[
\underset{0}{\text { SIM_VCC }-0.7 \mathrm{~V}}
\]
\[
0.8 \underset{0}{\text { * SIM_VCC }}
\] \& \& SIM_VCC
0.6
100
100
SIM_VCC
0.2 * SIM_VCC
100
100 \& \[
\begin{gathered}
\mathrm{V} \\
\mathrm{~V} \\
\mathrm{~ns} \\
\mathrm{~ns} \\
\\
\mathrm{~V} \\
\mathrm{~V} \\
\mathrm{~ns} \\
\mathrm{~ns}
\end{gathered}
\] \\
\hline ```
SIM_VCC = +5.0 V
Output Duty Cycle @ Fin \(=5.0 \mathrm{MHz}\)
DC \(=50 \% \pm 1 \%\)
Output SIM_CLK Rise Time @ Cout = 30 pF
Output SIM_CLK Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\mathrm{OH}} @\) Iclk \(=+20 \mu \mathrm{~A}\)
Output \(\mathrm{V}_{\mathrm{OL}} @\) Iclk \(=-200 \mu \mathrm{~A}\)
SIM_VCC = +3.0 V
Output Duty Cycle @ Fin \(=5.0 \mathrm{MHz}\)
\(D C=50 \% \pm 1 \%\)
Output SIM_CLK Rise Time @ Cout = 30 pF
Output SIM_CLK Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\mathrm{OH}} @\) Iclk \(=+20 \mu \mathrm{~A}\)
Output \(\mathrm{V}_{\mathrm{OL}} @\) Iclk \(=-20 \mu \mathrm{~A}\)
``` \& SIM_CLK \& \[
\begin{gathered}
\hline 8 \\
(11)
\end{gathered}
\] \& \[
\begin{gathered}
40 \\
0.7 \text { * } \begin{array}{c}
\text { SIM_VCC } \\
0
\end{array} \\
40 \\
0.7{ }^{\text {* SIM_VCC }} \\
0
\end{gathered}
\] \& \& 60
18
18
SIM_VCC \(_{+0.5}^{+0.5}\)
60
18
18
SIM_VCC
0.2 *SIM_VCC \& \[
\begin{aligned}
\& \% \\
\& \mathrm{~ns} \\
\& \mathrm{~ns} \\
\& \mathrm{~V} \\
\& \mathrm{~V} \\
\& \\
\& \% \\
\& \% \\
\& \mathrm{~ns} \\
\& \mathrm{~ns} \\
\& \mathrm{~V} \\
\& \mathrm{~V}
\end{aligned}
\] \\
\hline ```
SIM_VCC = +5.0 V @ IO_ENABLE = H
SIM_I/O Data Transfer Frequency
SIM_I/O Rise Time @ Cout = 30 pF
SIM_I/O Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\mathrm{OH}} @\) ISIM_IO \(=+20 \mu \mathrm{~A}, \mathrm{~V}_{I H}=\mathrm{V}_{\mathrm{DD}}\)
Output \(\mathrm{V}_{\mathrm{OL}} @\) ISIM_IO \(=-1.0 \mathrm{~mA}, \mathrm{I} / \mathrm{O} \mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}\)
SIM_VCC = +3.0 V @ IO_ENABLE = H
SIM_I/O Data Transfer Frequency
SIM_I/O Rise Time @ Cout = 30 pF
SIM_I/O Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\mathrm{OH}} @ I S I M \_I O=+20 \mu \mathrm{~A}, \mathrm{~V}_{I H}=\mathrm{V}_{\mathrm{DD}}\)
Output \(\mathrm{V}_{\mathrm{OL}} @\) ISIM_IO \(=-1.0 \mathrm{~mA}, \mathrm{I} / \mathrm{O} \mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}\)
SIM_VCC = +5.0 V @ IO_ENABLE = L
SIM_I/O Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\mathrm{OL}}\) @ ISIM_IO = \(-1.0 \mathrm{~mA}, \mathrm{I} / \mathrm{O} \mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}\)
SIM_VCC = +3.0 V @ IO_ENABLE = L
SIM_I/O Fall Time @ Cout = 30 pF
Output \(\mathrm{V}_{\text {OL }} @\) ISIM_IO \(=-1.0 \mathrm{~mA}, \mathrm{I} / \mathrm{O} \mathrm{V}_{\mathrm{IL}}=0 \mathrm{~V}\)
SIM_VCC = +5.0 V @ I/O = H,
IO_ENABLE Returns to High
SIM_I/O Rise Time @ Cout = 30 pF
SIM_VCC = +3.0 V @ I/O = H,
IO_ENABLE Returns to High
SIM_I/O Rise Time @ Cout = 30 pF
``` \& SIM_I/O \& \[
\begin{gathered}
\mathbf{1 0} \\
(13)
\end{gathered}
\] \& \[
0.7{ }_{0}^{\text {* SIM_VCC }}
\]
\[
0.7 \underset{0}{\text { * SIM_VCC }}
\] \& \begin{tabular}{l}
150 \\
150 \\
2.0 \\
1.5
\end{tabular} \& 160
0.8
0.8
SIM_VCC
0.4

160
0.8
0.8
SIM_VCC
0.4
800
0.4

800

0.4 \& | kHz |
| :--- |
| $\mu \mathrm{s}$ |
| $\mu \mathrm{s}$ |
| V |
| V |
| kHz |
| $\mu \mathrm{s}$ |
| $\mu \mathrm{s}$ |
| V |
| V |
| ns |
| V |
| ns |
| V |
| $\mu \mathrm{s}$ |
| $\mu \mathrm{s}$ | <br>

\hline I/O Pull Up Resistor \& I/O_RPLD \& $$
\begin{gathered}
\hline \mathbf{1} \\
(2)
\end{gathered}
$$ \& 13 \& 20 \& \& k $\Omega$ <br>

\hline Card I/O Pull Up Resistor \& SIM_I/O_RPLD \& $$
\begin{gathered}
\mathbf{1 0} \\
(13)
\end{gathered}
$$ \& 13 \& 20 \& \& k $\Omega$ <br>

\hline
\end{tabular}

3. SIM logic input undershoot $<-0.30 \mathrm{~V}$, SIM logic input overshoot $<0.30 \mathrm{~V}$.


Figure 3. SIM Supply Current as a Function of the $\mathrm{V}_{\mathrm{DD}}$ Voltage, $\mathrm{I} / \mathrm{O}=\mathrm{High}$


Figure 5. Power Supply Current as Function of the $\mathrm{V}_{\mathrm{Cc}}$ Input Voltage, $\mathrm{I} / \mathrm{O}=\mathrm{High}$


Figure 4. SIM Supply Current as a Function of the $\mathrm{V}_{\mathrm{DD}}$ Voltage, $\mathrm{I} / \mathrm{O}=100 \mathrm{kHz}$ Data Transfer


Figure 6. Power Supply Current as Function of the $\mathrm{V}_{\mathrm{Cc}}$ Input Voltage, $\mathrm{I} / \mathrm{O}=100 \mathrm{kHz}$ Data Transfer

## Level Shifters

The built-in level shifters accommodate the differential voltage between the external MPU and the SIM card. Neither the logic nor the functions of the SIM signals are affected by the interface.

The NCN6011 does not regulate the SIM_VCC, nor does it detect the overload current.

## Bidirectional Level Shifter

The NCN6011 carries out the voltage difference between the MPU and the Smart Card I/O signals. When the start sequence is completed, and if no failures have been detected, the device becomes essentially transparent for the data transferred on the I/O line. To fulfill the ISO7816-3 specification, both sides of the I/O line have built-in pulsed circuitry to accelerate the signal rise transient. The I/O line is connected on both sides of the interface by a NMOS switch which provide the level shifter and, thanks to its relative high internal impedance, protects the Smart Card in the event of data collision. Such a situation could occur if either the MPU of the smart card forces a signal in the opposite logic level direction.


Figure 8. Typical I/O and SIM_IO Waveform, $\mathrm{V}_{\mathrm{DD}}=\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$, ENABLE $=$ LOw


Figure 7. Basic Internal I/O Level Shifter


Figure 9. Typical SIM_IO Activated by ENABLE Pin, I/O = High (open drain)

## Input Schmitt Triggers

All the Logic Input pins have built-in Schmitt trigger circuits to prevent the NCN6011 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 10.

The output signal is guaranteed to go High when the input voltage is above $0.70^{*} \mathrm{Vb}$ bat, and will go Low when the input voltage is below $0.30^{*} \mathrm{Vbat}$.


Figure 10. Typical Schmitt Trigger Characteristic

## ESD Protection

The NCN6011 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built-in structures have been designed to handle either 2.0 kV , when related to the microcontroller side, or 4.0 kV when connected with the external contacts. Practically, the SIM_RST, SIMD_CLK and SIM_IO pins can sustain 4.0 kV .

## Printed Circuit Board Layout

Since the NCN6011 carries high speed currents together with high frequency clock, the printed circuit board must be carefully designed to avoid the risk of uncontrolled operation of the interface.
Care must be observed to avoid common copper track sharing small signal and high power with a relative high impedance. On top of that, the clock signal (both input and output) shall be properly shielding to minimize the high frequency cross talk between this line and the rest of the circuit. In particular, the SIM_RST signal shall be protected from interference generated by the SIM_CLK line. Such protection can be achieved by surrounding the SIM_CLK track by a copper track connected to ground. Generally speaking, the ground plane shall be as large as possible for a given printed circuit board area.


Figure 11. Typical NCN6011/TSSOP-14 Application

NCN6011

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| NCN6011DTB | TSSOP-14 | 96 Units/Rail |
| NCN6011DTBR2 | TSSOP-14 | 2500 Tape \& Reel |
| NCN6011DMR2 | Micro-10 | 4000 Tape \& Reel |

## MC33170

## RF Amplifier Companion Chip for Dual-Band Cellular Subscriber Terminal

The MC33170 is a complete solution for drain modulated dual-band GSM 900MHz and DCS-1800MHz Power Amplifiers. Thanks to its internal decoder, the MC33170 drastically simplifies the interface between the PAs and the baseband logic section, providing an immediate gain in part count but also in occupied copper area. The device is also ready for 1 V platforms since it accepts logic high control signals down to $900 \mathrm{mV} @ 25^{\circ} \mathrm{C}$.

A priority management system ensures the negative is present before authorizing the power modulation, giving the necessary ruggedness to the final design. This function can easily be disabled for PAs not requiring a negative bias.

The device is able to directly drive an external P or N -channel with the possibility to linearize the overall response via the internal high-performance control amplifier and easily implement system gain.

Finally, an LDO delivers a stable voltage, usable for external biasing purposes.

- 1 V platform compatible: ON voltage $=900 \mathrm{mV}$, OFF voltage $=$ 300 mV max
- Priority management system prevents power modulation before negative bias establishes
- High performance 4.5 MHz gain-bandwidth product operational amplifier
- Drives N or P -channel MOSFET
- 2.5 V low-noise LDO
- Idle mode input for very low power consumption (standby mode)


## ON Semiconductor ${ }^{\text {w }}$

http://onsemi.com


TSSOP-14
DTB SUFFIX
CASE 948G
PIN CONNECTIONS

(Top View)

ORDERING INFORMATION

| Device | Package | Shipping |
| :--- | :---: | :---: |
| MC33170DTB | TSSOP-14 | 96 Units / Rail |
| MC33170DTBR2 | TSSOP-14 | 2500 / Tape \& Reel |



PIN DESCRIPTION

| Pin No. | Pin Name | Function | Description |
| :---: | :---: | :---: | :---: |
| 1 | Band Selection | Selects the transmit band | A level high on this input selects the DCS chain. A zero selects the GSM chain. |
| 2 | Tx Enable | Starts the power | A level high on this pin enables the DCS/GSM chain and establishes a low-resistance link between pin 5 and 7 |
| 3 | GSM-900 | Biases the 900MHz section | When pin 1 is at zero and pin 2 goes high, the LDO voltage appears on this pin (pin 14 is high) |
| 4 | DCS-1800 | Biases the 1.8 GHz section | When pin 1 is at one and pin 2 goes high, the LDO voltage appears on this pin (pin 14 is high) |
| 5 | PA Start-up | Enables the PA power section | When pin 2 goes high, the battery voltage appears on this pin with a 700 mA peak current capability (pin 14 is high) |
| 6 | Gnd | The IC ground | The IC ground |
| 7 | Vbat | The IC power supply | This pin is wired to the battery terminal. A 100 nF decoupling capacitor is recommended, depending on the supply impedance |
| 8 | LDO | Low DropOut regulator | This output requires a 100 nF decoupling and is able to deliver up to 10 mA continuous |
| 9 | NINV | Positive OPAMP input | The non-inverting OPAMP input |
| 10 | INV | Negative OPAMP input | The inverting OPAMP input |
| 11 | Vboost | Boost voltage from the PA | This pin connects to a boost voltage delivered by the RF PA. This boost is necessary when driving an N -channel |
| 12 | Out | The OPAMP output | The output of the OPAMP/MOSFET driver pin |
| 13 | Negative Reg. | The PA negative clip | This pin clips the PA negative bias to - 5 V and prevents/authorizes the modulation depending on its typical level : $\begin{aligned} & <5.5 \mathrm{~V}-2.5 \mathrm{~V}>\mathrm{OK} \\ & <1.3 \mathrm{~V}--3.5 \mathrm{~V}>\mathrm{NOTOK} \\ & <-4.2 \mathrm{~V}--5 \mathrm{~V}>\mathrm{OK} \end{aligned}$ <br> Max. clipping current is 5 mA |
| 14 | Common Enable | Enables the whole IC | When high, this pin puts the IC in on-mode |

MAXIMUM RATINGS

| Rating | Pin No. | Symbol | Value MIN | Value MAX | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Band selection | 1 | Vband | 0 | 5.5 | V |
| Tx Enable | 2 | TxEn | 0 | 5.5 | V |
| GSM-900 | 3 | VGSM | -5 | 5.5 | V |
| DCS-1800 | 4 | VDCS | -5 | 5.5 | V |
| PA Start-up | 5 | Vstartup | 0 | 5.5 | V |
| Vbat | 7 | Vbat | 0 | 5.5 | V |
| NINV | 9 | V+ | 0 | 5.5 | V |
| INV | 10 | V- | 0 | 5.5 | V |
| Boost voltage | 11 | Vboost | 0 | 12 | V |
| Negative regulation pin | 13 | VZ | -5.4 | 5.5 | V |
| Common Enable | 14 | CE | 0 | 5.5 | V |
| ESD capability, HBM model | All pins |  |  | 2 | kV |
| ESD capability, Machine model | All pins |  |  | 200 | V |
| Steering Switch, continuous output current Steering Switch, continuous output current Steering Switch, peak output current < $1 \mu \mathrm{~s}$ | $\begin{gathered} \hline 3-4 \\ 5 \\ 5 \end{gathered}$ | GSM/DCS <br> PA startup PA startup |  | $\begin{gathered} 1 \\ 50 \\ 700 \end{gathered}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \\ & \mathrm{~mA} \end{aligned}$ |
| Maximum power dissipation NW suffix, plastic package @Tj=25 ${ }^{\circ} \mathrm{C}$ NW suffix, plastic package @Tj=85 ${ }^{\circ} \mathrm{C}$ Thermal resistance Junction-to-Air |  | $\begin{gathered} \text { PD } \\ \text { PD } \\ \text { RJ-A } \end{gathered}$ |  | $\begin{aligned} & 500 \\ & 200 \\ & 200 \end{aligned}$ | $\begin{gathered} \mathrm{mW} \\ \mathrm{~mW} \\ { }^{\circ} \mathrm{C} / \mathrm{W} \end{gathered}$ |
| Operating Ambient Temperature Maximum Junction Temperature Maximum Operating Junction Temperature |  | $\begin{gathered} \hline \text { TA } \\ \text { Tjmax } \\ \mathrm{Tj}^{2} \end{gathered}$ |  | $\begin{gathered} -40 \text { to }+85 \\ 150 \\ 125 \end{gathered}$ | $\begin{aligned} & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \\ & { }^{\circ} \mathrm{C} \end{aligned}$ |
| Storage Temperature Range |  | TSTG |  | -60 to +150 | ${ }^{\circ} \mathrm{C}$ |

Note1: The control pins, CE, TxEn and Bands shall never exceed Vcc + 0.3V
Note2: A 100 nF decoupling capacitor is recommended between the IC Vcc and ground
Note3: To avoid any damage to the IC, the following sequence must be secured:
CE goes up then Tx goes up $\longrightarrow$ modulation startup
TX goes down then CE goes down $\longrightarrow$ modulation stop

ELECTRICAL CHARACTERISTICS

| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

INPUT SPECIFICATIONS
(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Max} \mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Input voltage range | 7 | $\mathrm{~V}_{\text {bat }}$ | 2.7 | 3.6 | 5.5 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Quiescent Current (ON mode) <br> 1 band operating, no load, Vneg. Reg. $=-4.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}}=900 \mathrm{mV}$ |  | $\mathrm{I}_{\mathrm{QON}}$ |  | 1.0 | 3.0 | mA |
| Standby current (OFF mode) <br> CE pin at low level, $\mathrm{V}_{\text {bat }}=5.5 \mathrm{~V}, \mathrm{~V}_{\text {NEG }}$ and $\mathrm{V}_{\text {boost }}$ open |  | $\mathrm{I}_{\text {QOFF }}$ |  | 1.0 | 10 | $\mu \mathrm{~A}$ |

## LOGIC CONTROL SPECIFICATIONS

Logic Levels (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Max} \mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Logic Level zero <br> Band Selection, Common Enable, TxEn | $1-2$ <br> 14 | OFF |  |  | 300 | mV |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Logic Level one <br> Band Selection, Common Enable, TxEn | $1-2$ <br> 14 | ON | 900 |  |  | mV |

Timings ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ )

| Transmission Enable, device already ON <br> $10 \%$ of TxEn to $90 \%$ of Vbat on PA start-up pin |  |  |  |  | 4.0 | $\mu \mathrm{~s}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :---: |

## VOLTAGE REGULATOR SPECIFICATIONS

Option section (For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min $/$ max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, Max $\mathrm{T}_{J}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Output voltage | 8 | VregOUT | 2.45 | 2.5 | 2.55 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Output current | 8 | IregOUT |  |  | 10 | mA |
| Short circuit current (Vout = Vnominal -300 mV ) | 8 | Iregshort | 20 |  |  | mA |
| Line regulation <br> Vin = Vout +1 V to 5.5 V, device is ON 10mA load on pin 8, 100nF | $7-8$ |  |  | 400 |  | $\mu \mathrm{~V}$ |
| Dropout voltage at lout $=10 \mathrm{~mA}$ | 8 | VregDROP |  |  | 150 | mV |
| Output capacitor | 8 | CregOUT |  |  | 100 | nF |

Dynamic parameters $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$

| Ripple rejection <br> $\mathrm{F}=1 \mathrm{kHz}$, Vin $=$ Vout +1 V, lout $=1 \mathrm{~mA}$, Cout $=100 \mathrm{nF}$ | 8 | PSRR |  | -70 |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
| RMS Noise voltage <br> lout $=1 \mathrm{~mA}$, Cout $=100 \mathrm{nF},<20 \mathrm{~Hz}-200 \mathrm{kHz}>$ | 8 |  |  | 100 |  |
| Noise density @ 1 kHz <br> lout $=1 \mathrm{~mA}$, Cout $=100 \mathrm{nF}$ | 8 | $\mathrm{e}_{\mathrm{n}}$ |  | 330 | dB |
| Rise time $: 10 \%$ of CE to $90 \%$ of Vregout | $14-8$ |  |  | 5.0 | $\mathrm{nV} / \mathrm{Hz}$ |

## CONTROL AMPLIFIER SPECIFICATIONS

(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Max} \mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Continuous current | 12 | $I_{\text {CONT }}$ |  |  | 2.0 | mA |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| Peak current (sink and source) | 12 | $\mathrm{I}_{\text {PEAK }}$ |  |  | 10 | mA |
| Quiescent current entering pin 11 at 8V <br> Device is in ON state and no load on pin 12 | 12 | $\mathrm{I}_{\mathrm{QON}}$ |  | 1.0 |  | mA |
| Input bias current, V+ = V- = 2V |  | $\mathrm{I}_{\mathrm{IB}}$ |  | 600 |  | nA |
| Open-loop voltage gain, TA = 25 ${ }^{\circ} \mathrm{C}$ |  | $\mathrm{A}_{\mathrm{VOL}}$ |  | 60 |  | dB |
| Gain Bandwidth Product measured at 100kHz |  | GBW |  | 5.5 |  | MHz |
| Output voltage levels, Vnegreg=-5V <br> Level high : Isource $=1 \mathrm{~mA}$ <br> Level low : Isink $=1 \mathrm{~mA}$ | 12 | $\mathrm{~V}_{\text {OH }}$ | 7.75 |  |  | V |
| Input offset voltage | $\mathrm{V}_{\text {OL }}$ |  |  | 0.25 |  |  |


| Characteristic | Pin \# | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |

PROTECTION AND STABILIZATION CIRCUIT
(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Max} \mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| Negative bias present | 12 |  |  |  | -4.2 | V |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
| No Negative protection disabled | 12 |  | 2.5 |  |  | V |
| Regulation level | 12 |  | -5.4 | -5.0 | -4.6 | V |
| Sink current | 12 |  |  |  | 5.0 | MA |

STEERING SWITCHES, SERIES RESISTANCE
(For typical values $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min/max values $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}, \mathrm{Max} \mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ unless otherwise noted)

| GSM-900 @ Id = 1mA, Vbat = 5.5V | 3 |  |  | 60 | 160 | $\Omega$ |
| :--- | :---: | :--- | :--- | :--- | :--- | :---: |
| DCS-1800 @ Id = 1mA, Vbat $=5.5 \mathrm{~V}$ | 4 |  |  | 60 | 160 | $\Omega$ |
| Power Amplifier Startup @ Id =50mA, Vbat = 5.5V | 5 |  |  | 1.0 | 2.0 | $\Omega$ |

## Lack of negative circuitry behavior:

The MC33170 hosts a circuitry that prevents the power modulation startup if the negative bias is not established. However, to accommodate with PAs that do make use of a
negative bias, it is possible to connect pin 13 to pin 7 and thus invalidate the protection circuitry. The below sketch details the available levels to fulfil this function


MC33170 operating truth table, pin levels:

| TxEN | Band Selection | Common Enable | GSM-900 | DCS-1800 | PA startup |
| :---: | :---: | :---: | :---: | :---: | :---: |
| X | X | 0 | High-impedance | High-impedance | High-impedance |
| 0 | X | 1 | High-impedance | High-impedance | High-impedance |
| 1 | 0 | 1 | $\mathrm{V}_{\text {LDO }}$-Io.RDS ${ }_{(0 \mathrm{ON})}$ | High-impedance |  |
| 1 | 1 | 1 | High-impedance | $\mathrm{V}_{\text {LDO-Io. }} \mathrm{RDS}_{(\mathrm{ON})}$ | $\mathrm{V}_{\mathrm{BAT}}$-Io.RDS ${ }_{(\mathrm{ON})}$ |

Io is the current delivered by the considered pin, $\operatorname{RDS}(\mathrm{ON})$ is the switch series resistance as defined in the section Steering Switches

TYPICAL OPERATING CHARACTERISTICS


Figure 1. TxEn, BAND, CE Logic Level with Temperature


Figure 3. LDO Output Voltage versus LDO Output Current @ $25^{\circ} \mathrm{C}$


Figure 5. Quiescent Current versus Temperature


Figure 2. LDO Voltage Output Variation with Temperature


Figure 4. LDO Dropout versus ILDOout Current @ $25^{\circ} \mathrm{C}$


Figure 6. Neg-Reg Thresholds versus Temperature

TYPICAL OPERATING CHARACTERISTICS (cont.)


Figure 7. Clamp Voltage vs INeg-Reg Current @ $25^{\circ} \mathrm{C}$

Figure 9. Transmission Enable Propagation Delay versus Temperature


Figure 11. Ground Current versus Temperature


Figure 8. NegReg Clamp @ 3mA versus Temperature


Figure 10. LDO Rise Time versus Load @ $25^{\circ} \mathrm{C}$


Figure 12. PA Start up Vdson @ Vbat 3.6V

## CHARACTERIZATION CURVES



LDO's output when banged from 0 to 10 mA


Audio susceptibility measurement fixture

## Measurement conditions:

$\mathrm{Tx}=\mathrm{CE}=1.0 \mathrm{~V}$, $\mathrm{Vcc}=3.6 \mathrm{~V}$, NegOut $=\mathrm{Vcc}, \mathrm{Cbyp}=100 \mathrm{nF}$

뭉


Input voltage rejection at lout $=1 \mathrm{~mA}$ and 10 mA
Input audio susceptibility at lout $=1 \mathrm{~mA} / 10 \mathrm{~mA}$

## GAIN / PHRSE MEASURE CIRCUIT



Gain/phase measurement fixture



Operational amplifier AC measurements with: $\mathrm{Vcc}=3.6 \mathrm{~V}$, $\mathrm{Tx}=\mathrm{CE}=1.0 \mathrm{~V}$, $\mathrm{Vboost}=8 \mathrm{~V}$, Pin 12 loaded not loaded


Spectral noise density at lout $=1 \mathrm{~mA}$

Operational amplifier AC measurements with:
$\mathrm{Vcc}=3.6 \mathrm{~V}$, $\mathrm{Tx}=\mathrm{CE}=1.0 \mathrm{~V}$, $\mathrm{Vboost}=8 \mathrm{~V}$, Pin 12 loaded by 1 nF

LDO output noise measurement with:
$\mathrm{Vcc}=3.6 \mathrm{~V}$, $\mathrm{Tx}=\mathrm{CE}=1.0 \mathrm{~V}$, Cout $=100 \mathrm{nF}$, lout $=1 \mathrm{~mA}$ Integrated noise: $\quad 20 \mathrm{~Hz}-200 \mathrm{kHz}=100 \mu \mathrm{Vrms}$ $20 \mathrm{~Hz}-1 \mathrm{MHz}=170 \mu \mathrm{Vrms}$

## MC33170 application hints

The MC33170 represents a major leap toward miniaturization and compactness of Power Amplifiers (PAs) systems. Prior to talk about the 33170 application circuits, let us review how a classical dual-band transmission chain is implemented. At the beginning of the chain, the power ramping signal is delivered by the Baseband's Digital to

Analog Converter (DAC). Because of the digitization, a natural discontinuity appears between the various steps the signal is made of. As a matter of fact, this sharp transitions create undesirable effects and need to be smoothed by an external circuitry (figure 13).


Figure 13. DAC's signal can be smoothed by an appropriate circuitry

The filtering action can be implemented in a various way, but usually a 3rd order Bessel filter represents a good choice. Actual solutions require the use of an external operational amplifier (OPAMP) dedicated to this function.

For drain-controlled PAs, the power is directly dependent upon the supply delivered to the device. Several methods exist but the preferred one stays the N or P channel modulation. In this application, the N -channel is wired in a source-follower configuration and therefore needs an external voltage to ensure its adequate enhancement. This upper voltage can be obtained from a step-up converter or directly from ON Semiconductor PAs, as with the MRFIC0919 or MRFIC1819. To quickly charge/discharge the MOSFET Ciss capacitor, a dedicated driver is needed, with a voltage swing high enough to bias the N -channel toward its specified RDSON.

Radio-Frequency PAs need stable bias levels to keep their operating point at the right place, despite supply variations. A Low DropOut (LDO) regulator is the obvious choice for
this purpose. Unfortunately, to keep the quiescent power at its minimum during the GSM/DCS time-frame pauses (e.g. no power delivered), it is important to quickly remove the bias from the PAs. Conversely, the LDO shall be fast enough to bias the PAs at anytime, without hampering the overall response time. Such a task is difficult for an off-the-shelf regulator: a specific component has to be found.
Thanks to their innovative designs, ON Semiconductor PAs, such as the aforementioned ones, do not require any external negative sources. However, some synchronization signals are needed to activate the internal circuitry and provide them with a stable operating point. This is usually done by using external low/high power switches.
Finally, a safety system needs to be implemented to prevent the modulation start in case the negative bias is not established.
Gathering all these information onto a final drawing gives birth to figure 14.


Figure 14. Actual solution to drive a two-PA configuration

## MC33170 as a Bessel filter

Thanks to its package, the MC33170 simplifies the implementation of any filtering/driving configuration, e.g. with either an N or P -channel MOSFET. Figure 15a details
the way to wire a 100 kHz filter while driving an N -channel MOSFET. In this application, a third order filter is achieved by combining a first pole passive RC-filter, followed by a second-order Sallen-Key complex pole-pair section.


Figure 15a. Using the MC33170's OPAMP to filter out the DAC discontinuities

As one can see, it is easy to select the desired gain value via the 100k feedback resistors and accordingly tailor it to the DAC output level. Figure 15a performs the filtering function but also delivers the adequate sink/source current to drive the MOSFET transistor. The two-component section of figure 2 is reduced into a single one, saving cost and PCB area. It also important to point out that the OPAMP section can be totally disabled by the Common Enable pin.

## Benefits of the closed loop configuration

One of the MC33170's key applications is to make the modulation section operating in a closed-loop configuration. That is to say, the power chain is closed
through the feedback resistor (the $100 \mathrm{k} \Omega$ network in figure 3) and forces the output to follow the input ramp. With N -channels, it brings several benefits:

1. The input ramp does no longer deals with the MOSFET threshold voltage which can introduce a certain amount of delay in the response time.
2. At low powers, the distributions between the $\mathrm{RDS}_{(\mathrm{ON})}$ is automatically compensated.

With P-channels, the application does not need an elevated voltage to ensure the channel enhancement but maximizes the presence of the OPAMP to ensure a fully linear chain.


Figure 15b. Going down with the 100 kHz filter

## The need of a fast regulator

Since the internal LDO controls the PA's bias points, it is important to quickly drive the regulator in order to ensure the minimum consumption during the non-modulation phases. A standard LDO has difficulties to react in less than $30 \mu \mathrm{~s}$.


Figure 15c. Going up with the 100 kHz filter
This delay would be unacceptable in a system operating with fast frames. The MC33170 internal LDO has be designed to react within less than $10 \mu \mathrm{~s}$, ensuring a prompt bias establishment. Figure 16 shows the way the bias voltage takes place, without any overshoot.


Figure 16. A fast LDO ensures an immediate bias availability

The LDO requires a standard 100 nF decoupling capacitor to keep its output stable. The typical output noise stays within $100 \mu \mathrm{~V}$ from 100 Hz to 100 kHz .

## High and low current switches

The MC33170 hosts two types of steering switch. The first one only deals with low currents since it delivers the
operating bias voltage to the PAs. With two distinct switches, the MC33170 low-current switches control the RF PA GSM 900 MHz or DCS 1.8 GHz . Once again, the reaction time of these elements is optimized to ensure a fast operation. Figure 17a depicts the typical signal variations. Please note that the Tx pin is controlled via a logic 01 of 1 V ensuring the compatibility with 1V platforms.


Figure 17a. Typical GSM/DCS pins response time


Figure 17b. Peak current capability of the power switch

## Complete dual-band application

Figure 18 shows how implementing the MC33170 in a complete dual-band application where a 100 kHz filter is combined with the MOSFET driver.


Figure 18. A complete dual-band application with the MC33170

## Application

The MC33170 has been designed to fulfill the requirements of the new ON Semiconductor dual-band RF amplifier, the MRFIC1859. For demonstration purposes, the
device was driven by the MC33170 in a simple gain two configuration. The below picture shows how the power signal drives the PA's drain.


Figure 19. The driving signal delivered by the MC33170 allows fully linear power modulation

## GSM specifications

In order to meet the GSM specifications, the modulation edges must be smoothed to fit into the spectral template. This can be accomplished by implementing figure 18 's

Bessel filter and adjusting the cutoff frequency. Once the edges are smoothed, the complete systems nicely fits into the GSM template, as depicted by figure 20.


Figure 20. Thanks to its flexibility, the MC33170 helps reaching the GSM specs

## NCS5000

## Integrated RF Schottky Detector

The NCS5000 is an integrated schottky detector intended for use as a level detector in RF measurement/power control applications such as those found in GSM handsets. The detector converts the peak RF voltage applied to a DC level. The circuit consists of an RF schottky detector, a reference schottky diode, as well as biasing and control circuitry. There is an enable input that allows the part to be placed in a low power state when not in use.

The detector is designed for operation up to 2.0 GHz and can operate with input power levels up to +25 dBm . There is a fixed offset of 10 mV (nominal) between the Reference Detector and the RF Detector under no applied RF. The two detectors are monolithically integrated so that they closely track over temperature, voltage and process.

The NCS5000 is housed in a very small TSOP-6 package ideal for portable applications. The TSOP-6 package is a lower profile, footprint compatible package to the SOT23-6.

## Features

- Wide Operating Frequency Range to 2.0 GHz
- 2.7-5.5 V Operating Voltage
- Very Low Operating Current of $300 \mu \mathrm{~A}$
- Enable Control to Place the Part in a Low Current Standby Mode
- Typical Standby Current of $<1.0 \mu \mathrm{~A}$
- -40 to $85^{\circ} \mathrm{C}$ Operating Temperature Range
- Very Small TSOP-6 Package


## Typical Applications

- Cellular Handsets (GSM and DCS1800/PCS1900)
- Wireless Data Modems
- Transmitter Power Measurement and Control
- Test Equipment

ORDERING INFORMATION

| Device | Package | Shipping |
| :---: | :---: | :---: |
| NCS5000SNT1 | TSOP-6 | 3000/Tape \& Reel |



This circuit has 28 active transistors

Figure 1.

PIN DESCRIPTION

| Pin | Name | Description |
| :---: | :---: | :--- |
| 1 | DET_OUT | This is the RF Detector Output. This signal is proportional to the peak RF voltage applied at the RF_In pin. |
| 2 | V $_{\text {CC }}$ | Input power supply. |
| 3 | Enable | Control signal to turn on and off the device. If this signal is not used, this pin should be connected directly <br> to VCc. $^{\prime}$ A logic high on this input turns on the device. |
| 4 | RF_In | This is the input to the RF detector. The signal must be AC-coupled into this input with a good quality RF capacitor. |
| 5 | GND | Ground. |
| 6 | REF | This is the reference detector output. Nominal this signal is 10 mV higher than DET_OUT when no RF signal is <br> applied at RF_In. |

MAXIMUM RATINGS $\left(T_{A}=25^{\circ} \mathrm{C}\right.$, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Maximum Input Power on RF Pin | PMAX | 28 | dBm |
| Maximum Power Supply | VCCMAX | 6.0 | V |
| ESD Rating for RF_In (HBM) All Other Pins are $2.5 \mathrm{kV}(\mathrm{HBM})$ | - | 500 | V |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -40 to +125 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | +150 | ${ }^{\circ} \mathrm{C}$ |
| Maximum Input Voltage on Pins | VIMAX | $\mathrm{V}_{\mathrm{CC}}+0.3 \mathrm{~V}$ | - |
| Minimum Input Voltage on Pins | VIMIN | -0.3 V | - |

## RECOMMENDED OPERATING CONDITIONS

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| RF Input (50 $\Omega$ Equivalent) | $\mathrm{RF}_{\text {in }}$ | - | - | 25 | dBm |
| Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 2.7 | - | 5.5 | V |
| Operating Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 | - | 85 | ${ }^{\circ} \mathrm{C}$ |

## ELECTRICAL CHARACTERISTICS

( $\mathrm{V}_{\mathrm{CC}}=2.8 \mathrm{~V}$, for typical values; $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, for min and max values; $\mathrm{T}_{A}=-40$ to $85^{\circ} \mathrm{C}$ unless otherwise noted.)

| Characteristic | Symbol | Pin | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RF Operating Frequency | - | 4 | 100 | - | 2000 | MHz |
| Operating Current Consumption ( $\mathrm{V}_{\text {enable }}=2.4 \mathrm{~V}$, No RF Applied) | Icc(op) | 2 | - | - | 500 | $\mu \mathrm{A}$ |
| Standby Current Consumption ( $\mathrm{V}_{\text {enable }}=0.4 \mathrm{~V}$, No RF Applied) | Icc(stby) | 2 | - | 1 | 10 | $\mu \mathrm{A}$ |
| Power Supply Ripple Rejection $\left(\mathrm{V}_{\mathrm{CC}}=3.6 \mathrm{~V}, \mathrm{~V}_{\text {ripple }}=0.5 \mathrm{~V} \text { PP, No RF) } \begin{array}{r} 1 \mathrm{kHz} \\ 10 \mathrm{kHz} \end{array}\right.$ | RR | 2 | - | $\begin{aligned} & 56 \\ & 41 \end{aligned}$ | - | dB |
| Detector Output (No RF Applied) | DET_OUT | 1 | 40 | 45 | 50 | mV |
| Reference Output (No RF Applied) | REF | 6 | 50 | 55 | 60 | mV |
| Reference - Detector Output Differential Voltage (No RF Applied) | REFDET_OUT | 1,6 | 5 | 10 | 15 | mV |
| $\begin{aligned} & \text { Detector Output } \\ & \mathrm{F}_{\text {in }}=1.0 \mathrm{GHz}, \mathrm{RF}_{\text {in }}=-5.0 \mathrm{dBm}(50 \Omega) \\ & \mathrm{F}_{\text {in }}=1.0 \mathrm{GHz}, \mathrm{RF}_{\text {in }}=5.0 \mathrm{dBm}(50 \Omega) \\ & \mathrm{F}_{\text {in }}=1.0 \mathrm{GHz}, \mathrm{RF}_{\text {in }}=15 \mathrm{dBm}(50 \Omega) \end{aligned}$ | - | - | - | $\begin{gathered} 100 \\ 335 \\ 1285 \end{gathered}$ | - | mV |
| Enable Logic High | Vih | 3 | 2.4 | - | - | V |
| Enable Logic Low | Vil | 3 | 0 | - | 0.4 | V |
| Enable Input Current, $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$, $\mathrm{V}_{\text {enable }}=2.4 \mathrm{~V}$ | lin | 3 | 0 | - | 30 | $\mu \mathrm{A}$ |



Figure 2. Typical Application Block Diagram

## APPLICATION INFORMATION

The NCS5000 is an integrated RF schottky detector designed for use in level detector and power amplifier control circuits. The device is optimized for large signal applications (Pin $>-20 \mathrm{dBm}$ ) such as those found in GSM handsets and data modems. This device has been designed for applications that require operation from a single $\mathrm{Li}-\mathrm{Ion}$ or multi- $\mathrm{Ni}-\mathrm{MH}$ battery pack. The operating range is $2.7-5.5 \mathrm{~V}$ so the device can be powered directly from the battery or a low drop out regulator. To support power sequencing, an Enable circuitry is included which allows the
device to be placed into a very low power state $(<3.0 \mu \mathrm{~W})$ when not in use.

In addition to the RF detector, a reference detector is included so the NCS5000 can be used to implement a differential detector. Since the RF and reference detectors are integrated on the same silicon, they track each other tightly over temperature, bias voltage, and process. Each detector is biased with approximately $45 \mu \mathrm{~A}$ of current and there is a built-in offset of 10 mV (nom) between the RF and the Reference Detector.


Figure 3. Detector Output Voltage vs. RF Input Power ( $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$ )


Figure 5. Offset Between RF Detector and Reference Detector Output Voltage Over Temperature ( $\mathrm{V}_{\mathrm{CC}}=\mathbf{2 . 7} \mathrm{V}$, No RF Applied)


Figure 7. Current Consumption vs. Input Power
$\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}, \mathrm{F}_{\text {in }}=100 \mathrm{MHz}$


Figure 4. Detector and Reference Output Variation Over Temperature ( $\mathrm{V}_{\mathrm{CC}}=2.7 \mathrm{~V}$, No RF Applied)


Figure 6. Detector and Reference Output Variation Over $\mathrm{V}_{\mathrm{Cc}}$ Bias ( $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, No RF Applied)


Figure 8. Icc Variation Over Temperature $\mathrm{V}_{\mathrm{Cc}}=5.5 \mathrm{~V}$, No RF Applied

## INFORMATION FOR USING THE TSOP-6 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.


The power dissipation of the TSOP-6 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $\mathrm{T}_{\mathrm{J}(\max )}$, the maximum rated junction temperature of the die, $\mathrm{R}_{\theta \mathrm{JA}}$, the thermal resistance from the device junction to ambient, and the operating temperature, $\mathrm{T}_{\mathrm{A}}$. Using the values provided on the data sheet for the TSOP-6 package, $\mathrm{P}_{\mathrm{D}}$ can be calculated as follows:

$$
P_{D}=\frac{T_{J(\text { max })}-T_{A}}{R_{\theta J A}}
$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $\mathrm{T}_{\mathrm{A}}$ of $25^{\circ} \mathrm{C}$, one can calculate the power dissipation of the device which in this case is 400 milliwatts.

$$
\mathrm{P}_{\mathrm{D}}=\frac{150^{\circ} \mathrm{C}-25^{\circ} \mathrm{C}}{300^{\circ} \mathrm{C} / \mathrm{W}}=417 \text { milliwatts }
$$

The $300^{\circ} \mathrm{C} / \mathrm{W}$ for the TSOP-6 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 417 milliwatts.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be $100^{\circ} \mathrm{C}$ or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of $10^{\circ} \mathrm{C}$.
- The soldering temperature and time should not exceed $260^{\circ} \mathrm{C}$ for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be $5^{\circ} \mathrm{C}$ or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.
*Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.


## Advance Information

## Antenna Switch Controller

The MDC5100 is designed to control GaAs RF switches which require positive and negative going control voltages to select the switch path. All input control signals are 3 V CMOS-logic compatible to allow for direct interface to a microcontroller. The device also has an accessory detect pin for use in applications where there is a portable handset to mobile adapter. The device is designed to interface directly with Double Pull-Double Throw (DPDT) switches such as the M/A-Com SW 363.

This device in combination with a GaAs RF switch can be used to achieve duplex isolation in many Time Division Duplex Radios like DECT or in Frequency Division Duplex Radios employing time division multiple access with staggered Transit/Receive time slots such as GSM. It can also be used to control an RF switch in dual band radio applications. The device is housed in a miniature Micro-8 for minimum space utilization.

## Features

- Micro-miniature Low Profile Micro 8 Package
- 3 V CMOS Logic Control Inputs
- Ultra-low Quiescent Current of $400 \mu \mathrm{~A}$ Typical
- Wide Operating Temperature Range of -40 to $85^{\circ} \mathrm{C}$


## Applications

- GSM and PCS Portable Phones
- Mobile to Portable Accessories
- Wireless LAN Modems
- Specialized TDD and TDMA Radios
- Dual Band Phones


Functional Block Diagram
This document contains information on a new product. Specifications and information herein are subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Positive Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 6 | V |
| Negative Supply Voltage | $\mid \mathrm{V}_{\mathrm{EE}}$ | 12 | V |
| Differential Supply Voltage | $\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}$ | 15 | V |
| Voltage Range at Any Input Pin (TxE, RxE, Acc) | $\mathrm{V}_{\text {in }}$ | -1 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Total Power Dissipation <br> Derate above $25^{\circ} \mathrm{C}$ | $\mathrm{PD}_{\mathrm{D}}$ | 510 <br> 4 | mW <br> $\mathrm{mW} /{ }^{\circ} \mathrm{C}$ <br> Thermal Resistance, Junction to Ambient $\mathrm{R}_{\theta J \mathrm{~A}}$ |

## DEVICE MARKING

5100
ORDERING INFORMATION

## MDC5100R2

13 inch Reel, 4000 units

TRUTH TABLE

| Input Logic |  |  | Output Logic |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RxE | TxE | ACC | V1 ${ }_{\text {out }}$ | V2 ${ }_{\text {out }}$ |  |
| 0 | 0 | 0 | GND | GND |  |
| 0 | 0 | 1 | GND | GND |  |
| 0 | 1 | 0 | V- | V+ |  |
| 0 | 1 | 1 | V+ | V- |  |
| 1 | 0 | 0 | V+ | V- |  |
| 1 | 0 | 1 | V- | V+ |  |
| 1 | 1 | 0 | V+ | $V_{+}$ | Invalid state, should be |
| 1 | 1 | 1 | V+ | V+ |  |

Note 1: ACC " 0 " = Open, ACC " 1 " = $10 \mathrm{k} \Omega$ to GND
Note 2: $\mathrm{V}_{+}$is nominally $\mathrm{V}_{\mathrm{IH}}-0.1$
Note 3: V - is nominally $\mathrm{V}_{\mathrm{EE}}-1 \mathrm{~V}$

PIN DESCRIPTION

| Pin | Name | Functional Description |
| :---: | :--- | :--- |
| 1 | $\mathrm{~V}_{\mathrm{CC}}$ | Positive Supply |
| 2 | $\mathrm{~V}_{\text {out }}$ | Antenna Control Output 1, $\mathrm{V}+$ is referenced to the $\mathrm{V}_{\mathrm{IH}}$ of TxE, RxE and V - is referenced to the $\mathrm{V}_{\text {EE }}$ Voltage |
| 3 | $\mathrm{~V}_{\text {out }}$ | Antenna Control Output 2, $\mathrm{V}+$ is referenced to the $\mathrm{V}_{\mathrm{IH}}$ of TxE, RxE and V - is referenced to the $\mathrm{V}_{\text {EE }}$ Voltage |
| 4 | TxE | Transmit Enable Input |
| 5 | RxE | Receive Enable Input |
| 6 | $\mathrm{~V}_{\text {EE }}$ | Negative Supply |
| 7 | GND | Ground |
| 8 | Acc | Accessory Present Input |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=2.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-10 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RECOMMENDED OPERATING CONDITIONS |  |  |  |  |  |
| Positive Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 1.8 |  | 5.0 | V |
| Negative Supply Voltage | $\mathrm{V}_{\mathrm{EE}}$ | -10 |  | -5.0 | V |
| Voltage Range at Any Input Pin (TxE, RxE, Acc) | $\mathrm{V}_{\text {in }}$ | 0 |  | $\mathrm{V}_{\text {CC }}$ | V |
| Ambient Operating Temperature Range | $\mathrm{T}_{\text {A }}$ | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |

## DC ELECTRICAL CHARACTERISTICS

| Positive Supply Current (Acc connected to GND) Negative Supply Current (Acc, V1, V2 unterminated) | $\begin{aligned} & \mathrm{I}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{EE}} \end{aligned}$ | 100 | 400 | $\begin{gathered} 500 \\ -200 \end{gathered}$ | $\mu \mathrm{A}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RxE or TxE Input High State for V1 or $\mathrm{V} 2=\mathrm{V}_{+}$ RxE or TxE Input Low State for V1 or V2 = V- | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IL}} \end{aligned}$ | 2.65 |  | 0.4 | V |
| V1, V2 Output High State - TxE or RxE $=\mathrm{V}_{\mathrm{IH}}, \mathrm{I}_{\mathrm{OH}}=-25 \mu \mathrm{~A}{ }^{(1)}$ <br> V1, V2 Output Low State - TxE or RxE $=\mathrm{V}_{\mathrm{IL}}, \mathrm{I}_{\mathrm{OL}}=25 \mu \mathrm{~A}{ }^{(1)}$ | $\begin{aligned} & \mathrm{V}_{+} \\ & \mathrm{V}_{-} \end{aligned}$ | 2.50 |  | -5.75 | V |
| Accessory Resistance for $\mathrm{V} 1=\mathrm{V}-, \mathrm{V} 2=\mathrm{V}+\left(\mathrm{TxE}=\mathrm{V}_{\mathrm{IH}}, \mathrm{RxE}=\mathrm{V}_{\mathrm{VL}}\right)$ <br> Accessory Resistance for $\mathrm{V} 1=\mathrm{V}+\mathrm{V} 2=\mathrm{V}-\left(\mathrm{TxE}=\mathrm{V}_{\mathrm{IH}}, \mathrm{RxE}=\mathrm{V}_{\mathrm{IL}}\right)$ | Racc Racc | 800 |  | 12 | $\mathrm{k} \Omega$ |

AC ELECTRICAL CHARACTERISTICS

| Propagation Delay - RxE/TxE to V1/V2 (Racc = $800 \mathrm{k} \Omega$ to GND) | $\begin{aligned} & \hline \mathrm{T}_{\mathrm{PLH}}{ }^{(2)} \\ & \mathrm{T}_{\mathrm{PH}}{ }^{(2)} \end{aligned}$ | $\begin{aligned} & 0.016 \\ & 0.004 \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 1.4 \end{aligned}$ | usec $\mu \mathrm{sec}$ |
| :---: | :---: | :---: | :---: | :---: |
| Propagation Delay - RxE/TxE to V1/V2 (Racc = $12 \mathrm{k} \Omega$ to GND) | $\begin{aligned} & \mathrm{T}_{\mathrm{PLH}} \\ & \mathrm{~T}_{\mathrm{PHL}} \end{aligned}$ | $\begin{gathered} 0.35 \\ 0.005 \end{gathered}$ | $\begin{aligned} & 4.0 \\ & 1.4 \end{aligned}$ | usec $\mu \mathrm{sec}$ |
| Propagation Delay - Acc to V1/V2 through $12 \mathrm{k} \Omega$ | $\begin{aligned} & \hline \mathrm{T}_{\mathrm{PLH}} \\ & \mathrm{~T}_{\mathrm{PHL}} \end{aligned}$ | $\begin{aligned} & \hline 0.4 \\ & 0.1 \end{aligned}$ | $\begin{aligned} & 7.5 \\ & 5.0 \end{aligned}$ | usec <br> $\mu \mathrm{sec}$ |
| Transition Time of V1/V2 from RxE or TxE (Racc $=800 \mathrm{k}$ to GND) | $\begin{aligned} & \mathrm{T}_{\text {rise }}{ }^{(3)} \\ & \mathrm{T}_{\text {fall }}{ }^{(3)} \end{aligned}$ | $\begin{aligned} & \hline 0.3 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 7.4 \\ & 4.4 \end{aligned}$ | $\mu \mathrm{sec}$ <br> $\mu \mathrm{sec}$ |
| Transition Time of V1/V2 from RxE or TxE (Racc $=12 \mathrm{k}$ to GND) | $\begin{aligned} & \mathrm{T}_{\text {rise }} \\ & \mathrm{T}_{\text {fall }} \end{aligned}$ | $\begin{aligned} & 0.3 \\ & 0.2 \end{aligned}$ | $\begin{aligned} & 16 \\ & 4.0 \end{aligned}$ | $\begin{aligned} & \mu \mathrm{sec} \\ & \mu \mathrm{sec} \end{aligned}$ |
| Transition Time of V1/V2 from Acc Input | $\begin{aligned} & \hline \mathrm{T}_{\text {rise }} \\ & \mathrm{T}_{\text {fall }} \end{aligned}$ | $\begin{aligned} & 0.3 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 4.1 \\ & 4.1 \end{aligned}$ | $\mu \mathrm{sec}$ <br> $\mu \mathrm{sec}$ |

NOTES: 1 Refer to truth table for input test states
2. $T_{P L H}$ and $T_{P H L}$ are measured from the $50 \%$ point of input waveform to $50 \%$ of the output waveform
3. $T_{\text {rise }}$ and $T_{\text {fall }}$ are measured from the $10 \%$ point to the $90 \%$ point of the output

## MDC5100



Figure 1.


Figure 2. AC Test Load

MDC5100


Figure 3. Diversity Antenna Application


Figure 4. TDD or Half-Duplex Handie-Talkie Application

## Antenna Switch Control

The MDC5101 inputs TxE and RxE Logic Signals with an accessory input termination option and, allows positive and negative control voltages in accordance with the enclosed truth table. This device is primarily intended to control GaAs RF switches. It is also designed to interface with most HCMOS MCUs such as the ON Semiconductor MC68338.

The MDC5101 is intended to replace a circuit of up to 18 discrete components and is available in a Micro- 8 package. This device, in combination with a compatible RF switch, can be used to achieve duplex isolation in any Time Division Duplex Radio like GSM and DCS1800 with staggered Transmit Receive Time Slots. It can also be used to control an RF switch in dual band radio applications.

This integrated solution in a Micro-8 package compared with a discrete solution will add a great value in performance with less board space consumption.

## Features

- Miniature Micro-8 Surface Mount Package Saves Board Space
- Logic Level Control
- Designed to Interface with Microcontrollers


## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Positive Power Supply Voltage ${ }^{(1)}$ | $\mathrm{V}_{\mathrm{CC}}$ | 15 | Vdc |
| Negative Power Supply Voltage ${ }^{(2)}$ | $\mathrm{V}_{\mathrm{EE}}$ | -12 | Vdc |
| Differential Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}$ | 15 | Vdc |
| Input Voltage ${ }^{(3)}$ | $\mathrm{V}_{\text {in }}$ | $\mathrm{V}_{\mathrm{CC}}$ | Vdc |
| Output Current ${ }^{(4)}$ | $\mathrm{I}_{1}, \mathrm{I}_{2}$ | 5.0 | mAdc |
| Operating Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Total Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ | 510 | mW |
| Derate above $25^{\circ} \mathrm{C}$ |  | 4.0 | $\mathrm{~mW} /{ }^{\circ} \mathrm{C}$ |
| Thermal Resistance, Junction to Ambient | $\mathrm{R}_{\text {日JA }}$ | 245 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

Note 1: Pin 1 Referenced to Ground
Note 2: Pin 6 Referenced to Ground
Note 3: Pin 3, 4 Referenced to Ground
Note 4: Pin 5, 7 Referenced to Ground

## DEVICE MARKING

## 5101

## ORDERING INFORMATION

MDC5101R2 13 inch Reel, 4000 units

## ESD Rating

ESD protection on each pin to $\pm 2500 \mathrm{~V}$ per MIL-STD6883 method 3015 , using human body model of $100 \mathrm{pF}, 1500$ Ohms and using the machine model to $\pm 200 \mathrm{~V}$ at 100 pF and 0 Ohms. Parts must meet electrical requirement after testing.

ELECTRICAL CHARACTERISTICS $\left(\mathrm{V}_{\mathrm{CC}}=2.75 \mathrm{~V}, \mathrm{~V}_{\mathrm{EE}}=-5.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathrm{T}_{\text {low }}\right.$ to $\mathrm{T}_{\text {high }}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |

DC PARAMETERS

| Positive Power Supply Current V1, V2, ACC $10 \mathrm{k} \Omega$ to $\mathrm{GND}, \mathrm{RxE}=\mathrm{V}_{\mathrm{IH}}, \mathrm{TxE}=\mathrm{V}_{\mathrm{IL}}$ | ICC | - | - | 1.0 | mA |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Negative Power Supply Current $\mathrm{V} 1, \mathrm{~V} 2, \mathrm{ACC} \text { Open, } \mathrm{RxE}=\mathrm{V}_{\mathrm{IL}}, \mathrm{TxE}=\mathrm{V}_{\mathrm{IH}}$ | $\mathrm{I}_{\text {EE }}$ | - | -50 | - | $\mu \mathrm{A}$ |
| Negative Power Supply Current <br> V1, V2, ACC $10 \mathrm{k} \Omega$ to GND, RxE $=\mathrm{V}_{\mathrm{IL}}, \mathrm{TxE}=\mathrm{V}_{\mathrm{IH}}$ | $l_{\text {EE }}$ | -1.5 | - | - | mA |
| $\begin{aligned} & \text { High Level Output Voltage } \\ & I_{1}=I_{2}=250 \mu A, A C C \text { Open } \\ & R \times E=V_{I L}, T \times E=V_{I H} \\ & R \times E=V_{I H}, T x E=V_{I L} \\ & I_{1}=I_{2}=250 \mu A, A C C 10 \mathrm{k} \Omega \text { to GND } \\ & R \times E=V_{I L}, T \times E=V_{I H} \\ & R \times E=V_{\text {IH }}, T x E=V_{I L} \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}(\mathrm{V} 1)}$ <br> $\mathrm{VOH}_{\mathrm{O}}$ (V) <br> $\mathrm{V}_{\mathrm{OH}(\mathrm{V} 2)}$ <br> $\mathrm{V}_{\mathrm{OH}(\mathrm{V} 1)}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}^{-}-0.25} \\ & \mathrm{~V}_{\mathrm{IH}^{-}-25} \\ & \\ & \mathrm{~V}_{\mathrm{IH}^{-}-0.25} \\ & \mathrm{~V}_{\mathrm{IH}^{-}}-0.25 \end{aligned}$ |  |  | Vdc |
| Low Level Output Voltage $\begin{aligned} & I_{1}=I_{2}=250 \mu \mathrm{~A}, \mathrm{ACC} \text { Open } \\ & \mathrm{RxE}=\mathrm{TxE}=\mathrm{V}_{\mathrm{IL}} \\ & \mathrm{RxE}=\mathrm{V}_{\mathrm{IH}}, \mathrm{TxE}=\mathrm{V}_{\mathrm{IL}} \\ & \mathrm{I}_{1}=\mathrm{I}_{2}=250 \mu \mathrm{~A}, \mathrm{ACC} 10 \mathrm{k} \Omega \text { to GND } \\ & \mathrm{RxE}=\mathrm{TxE}=\mathrm{V}_{\mathrm{IL}} \\ & \mathrm{RxE}=\mathrm{V}_{\mathrm{IH}}, \mathrm{TxE}=\mathrm{V}_{\mathrm{IL}} \\ & \hline \end{aligned}$ | $\begin{gathered} \mathrm{V}_{\mathrm{OL}(\mathrm{~V} 1, \mathrm{~V} 2)} \\ \mathrm{V}_{\mathrm{OL}(\mathrm{~V} 1)} \\ \\ \mathrm{V}_{\mathrm{OL}(\mathrm{~V} 1, \mathrm{~V} 2)} \\ \mathrm{V}_{\mathrm{OL}(\mathrm{~V} 2)} \end{gathered}$ | $\begin{aligned} & -0.5 \\ & -0.5 \\ & \\ & -0.5 \\ & -0.5 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 0.5 \\ & \\ & 0.5 \\ & 0.5 \end{aligned}$ | Vdc |
| Low Level Output Voltage $\begin{aligned} & \mathrm{I}_{1}=\mathrm{I}_{2}=250 \mu \mathrm{~A}, \mathrm{TxE}=\mathrm{V}_{\mathrm{IH}}, \mathrm{RxE}=\mathrm{V}_{\mathrm{IL}} \\ & \text { ACC Open } \\ & \text { ACC } 10 \mathrm{k} \Omega \text { to GND } \end{aligned}$ | $\mathrm{V}_{\mathrm{OL}(\mathrm{V} 2)}$ <br> VoL(V1) |  |  | $\begin{aligned} & -4.5 \\ & -4.5 \\ & \hline \end{aligned}$ | Vdc |

AC PARAMETERS

| Propagation Delay RxE, TxE to V1, V2 ACC Open |  |  |  |  | $\mu \mathrm{S}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $t_{\text {PLH }}$ | - | - | 1.5 |  |
|  | $t_{\text {PHL }}$ | - | - | 1.5 |  |
| RxE, TxE to V1, V2 | $t_{\text {PLH }}$ | - | - | 1.5 |  |
| ACC $10 \mathrm{k} \Omega$ to GND | $t_{\text {PHL }}$ | - | - | 1.5 |  |
| ACC to V1, V2 | $t_{\text {PLH }}$ $t_{\text {PHL }}$ | - | - | 5.0 5.0 |  |

## TRUTH TABLE

| Input Logic |  |  | Output Logic |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{R x E}$ | TxE | ACC | V2 | V1 |  |
| 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | -5.0 | 2.7 |  |
| 0 | 1 | 1 | 2.7 | -5.0 |  |
| 1 | 0 | 0 | 2.7 | 0 |  |
| 1 | 0 | 1 | 0 | 2.7 |  |
| 1 | 1 | 0 | 2.7 | 2.7 |  |

Note: ACC Logic Low $=$ Open, ACC Logic High $=10 \mathrm{k} \Omega$

| Low Level Input Voltage | $\mathrm{V}_{\mathrm{IL}}$ |  |  |  | Vdc |
| :--- | :---: | :---: | :---: | :---: | :---: |
| RxE, TxE | $\mathrm{V}_{\mathrm{IH}}$ | - | - | 0.4 |  |
| High Level Input Voltage <br> RxE, TxE <br> Maximum Voltage Differential | $\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{IH}}$ | -2.5 | - | - |  |



Figure 1. $\mathrm{V}_{\text {out (high) }}$ versus Temperature


Figure 3. ICc versus Temperature


Figure 5. IEE versus Temperature


Figure 2. $\mathrm{V}_{\text {out (low) }}$ versus Temperature


Figure 4. $\mathrm{I}_{\mathrm{EE}}$ versus Temperature


Figure 6. $\mathrm{I}_{\mathrm{EE}}$ versus $\mathrm{V}_{\mathrm{EE}}$


Figure 7. $\mathrm{I}_{\mathrm{cc}}$ versus $\mathrm{V}_{\mathrm{Cc}}$


Figure 8. $\mathrm{V}_{\text {out }}$ versus $\mathrm{V}_{\mathrm{EE}}$


Figure 9. $\mathrm{V}_{\text {out }}$ versus $\mathrm{V}_{\mathrm{IH}} / \mathrm{V}_{\mathrm{CC}}$

MDC5101


Figure 10. Antenna Switch Controller Block Diagram


Figure 11. Temperature Measurement Schematic

MDC5101


Figure 12. Measurement Schematic $\mathrm{V}_{\text {out }}$ vs $\mathrm{V}_{\mathrm{EE}}$ \& $\mathrm{I}_{\mathrm{EE}}$ vs $\mathrm{V}_{\mathrm{EE}}$


Figure 13. Measurement Schematic
$\mathrm{V}_{\text {out }}$ vs $\mathrm{V}_{\mathrm{CC}}$

## Low Voltage Bias Stabilizer with Enable

- Maintains Stable Bias Current in N-Type Discrete Bipolar Junction and Field Effect Transistors
- Provides Stable Bias Using a Single Component Without Use of Emitter Ballast and Bypass Components
- Operates Over a Wide Range of Supply Voltages Down to 1.8 Vdc
- Reduces Bias Current Variation Due to Temperature and Unit-to-Unit Parametric Changes
- Consumes $<0.5 \mathrm{~mW}$ at $\mathrm{V}_{\mathrm{CC}}=2.75 \mathrm{~V}$
- Active High Enable is CMOS Compatible

This device provides a reference voltage and acts as a DC feedback element around an external discrete, NPN BJT or N-Channel FET. It allows the external transistor to have its emitter/source directly grounded and still operate with a stable collector/drain DC current. It is primarily intended to stabilize the bias of discrete RF stages operating from a low voltage regulated supply, but can also be used to stabilize the bias current of any linear stage in order to eliminate emitter/source bypassing and achieve tighter bias regulation over temperature and unit variations. The "ENABLE" polarity nulls internal current, Enable current, and RF transistor current in "STANDBY." This device is intended to replace a circuit of three to six discrete components.

The combination of low supply voltage, low quiescent current drain, and small package make the MDC5001T1 ideal for portable communications applications such as:

- Cellular Telephones
- Pagers
- PCN/PCS Portables
- GPS Receivers
- PCMCIA RF Modems
- Cordless Phones
- Broadband and Multiband Transceivers and Other Portable Wireless Products


## MDC5001T1



MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 15 | Vdc |
| Ambient Operating Temperature Range | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $\mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ}{ }^{\circ} \mathrm{C}$ |
| Junction Temperature | $\mathrm{T}_{\mathrm{J}}$ | 150 | ${ }^{\circ} \mathrm{C}$ |
| Collector Emitter Voltage (Q2) | $\mathrm{V}_{\mathrm{CEO}}$ | -15 | V |
| Enable Voltage (Pin 5) | $\mathrm{V}_{\text {ENBL }}$ | $\mathrm{V}_{\mathrm{CC}}$ | V |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
| :--- | :---: | :---: | :---: |
| Total Device Power Dissipation | $\mathrm{P}_{\mathrm{D}}$ |  | mW |
| (FR-5 PCB of $1^{\prime \prime} \times 0.75^{\prime \prime} \times 0.062^{\prime \prime}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ ) |  | 150 | 1.2 |
| Derate above $25^{\circ} \mathrm{C}$ |  | $\mathrm{mW} /{ }^{\circ} \mathrm{C}$ |  |
| Thermal Resistance, Junction to Ambient | $\mathrm{R}_{\text {өJA }}$ | 833 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

ELECTRICAL CHARACTERISTICS $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right.$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Recommended Operating Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 1.8 | 2.75 | 10 | Volts |
| Power Supply Current ( $\mathrm{V}_{\mathrm{CC}}=2.75 \mathrm{~V}$ ) <br> $V_{\text {ref }}$, $\mathrm{l}_{\text {out }}$ are unterminated See Figure 8 | Icc | - | 130 | 200 | $\mu \mathrm{A}$ |
| Q2 Collector Emitter Breakdown Voltage $\left(\mathrm{I}_{\mathrm{C} 2}=10 \mu \mathrm{~A}, \mathrm{I}_{\mathrm{B} 2}=0\right)$ | $\mathrm{V}_{\text {(BR)CEO2 }}$ | 15 |  |  | Volts |
| $\begin{aligned} & \text { Reference Voltage }\left(\mathrm{V}_{\text {ENBL }}=\mathrm{V}_{\mathrm{CC}}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {out }}=0.7 \mathrm{~V}\right) \\ & (\text { l out }=30 \mu \mathrm{~A}) \\ & (\text { lout }=150 \mu \mathrm{~A}) \\ & \text { See Figure } 1 \end{aligned}$ | $\mathrm{V}_{\text {ref }}$ | $\begin{aligned} & 2.050 \\ & 2.110 \end{aligned}$ | $\begin{aligned} & 2.075 \\ & 2.135 \end{aligned}$ | $\begin{aligned} & 2.100 \\ & 2.160 \end{aligned}$ | Volts |
| $\begin{aligned} & \text { Reference Voltage }\left(\mathrm{V}_{\text {ENBL }}=\mathrm{V}_{\mathrm{CC}}=2.75 \mathrm{~V}, \mathrm{~V}_{\text {out }}=0.7 \mathrm{~V},\right. \\ & \left.-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}\right) \\ & \mathrm{V}_{\mathrm{CC}} \text { Pulse Width }=10 \mathrm{mS} \text {, Duty Cycle }=1 \% \\ & \text { (lout }=10 \mu \mathrm{~A}) \\ & \text { (lout }=30 \mu \mathrm{~A} \text { ) } \\ & \text { (lout }=100 \mu \mathrm{~A} \text { ) } \\ & \text { See Figures } 2 \text { and } 11 \end{aligned}$ | $\Delta \mathrm{V}_{\text {ref }}$ |  | $\begin{aligned} & \pm 5.0 \\ & \pm 15 \\ & \pm 25 \end{aligned}$ | $\begin{aligned} & \pm 10 \\ & \pm 30 \\ & \pm 50 \end{aligned}$ | mV |

## MDC5001T1

The following SPICE models are provided as a convenience to the user and every effort has been made to insure their accuracy. However, no responsibility for their accuracy is assumed by ON Semiconductor.

| .MODEL Q4 NPN |  | .MODEL Q1, Q2 PNP |  |
| :---: | :---: | :---: | :---: |
| $B F=136$ | $\mathrm{NE}=1.6$ | $\mathrm{BF}=87$ | NK $=0.5$ |
| $\mathrm{BR}=0.2$ | $\mathrm{NF}=1.005$ | $\mathrm{BR}=0.6$ | NR $=1.0$ |
| CJC $=318.6 \mathrm{f}$ | $\mathrm{RB}=140$ | CJC $=800 \mathrm{E}-15$ | $\mathrm{RB}=720$ |
| $\mathrm{CJE}=569.2 \mathrm{f}$ | $\mathrm{RBM}=70$ | CJE $=46 \mathrm{E}-15$ | RBM $=470$ |
| CJS $=1.9 \mathrm{p}$ | $\mathrm{RC}=180$ | $E G=1.215$ | $\mathrm{RC}=180$ |
| $E G=1.215$ | $\mathrm{RE}=1.6$ | $\mathrm{FC}=0.5$ | RE $=26$ |
| $\mathrm{FC}=0.5$ | TF $=553.6 \mathrm{p}$ | IKF $=3.8 \mathrm{E}-04$ | TF = 15E-9 |
| IKF $=24.41 \mathrm{~m}$ | TR = 10 n | IKR $=2.0$ | TR $=50 \mathrm{E}-09$ |
| IKR $=0.25$ | VAF $=267.6$ | $1 \mathrm{RB}=0.9 \mathrm{E}-3$ | $\mathrm{VAF}=54.93$ |
| $\mathrm{IRB}=0.0004$ | $V A R=12$ | $\mathrm{IS}=1.027 \mathrm{E}-15$ | $V A R=20$ |
| IS $=256 \mathrm{E}-18$ | VJC $=0.4172$ | ISC $=10 \mathrm{E}-18$ | VAR $=20$ |
| ISC $=1 \mathrm{f}$ | $\mathrm{VJE}=0.7245$ | ISE $=1.8 \mathrm{E}-15$ | VJC $=0.4172$ |
| ISE $=500 \mathrm{E}-18$ | VJS $=0.39$ | ITF $=2 \mathrm{E}-3$ | $\mathrm{VJE}=0.4172$ |
| ITF $=0.9018$ | VTF $=10$ | MJC $=0.2161$ | VTF $=10$ |
| MJC $=0.2161$ | XTB $=1.5$ | MJE $=0.2161$ | XTB $=1.5$ |
| $\mathrm{MJE}=0.3373$ | XTF $=2.077$ | $N C=0.8$ | XTF $=2.0$ |
| $\mathrm{MJS}=0.13$ | $\mathrm{XTI}=3$ | $\mathrm{NE}=1.38$ | $\mathrm{XTI}=3$ |
| NC $=1.09$ |  | $N F=1.015$ |  |


| RESISTOR VALUES |
| :---: |
|  |
| $R 1=12 \mathrm{~K}$ |
| $R 2=6 \mathrm{~K}$ |
| $\mathrm{R} 3=3.4 \mathrm{~K}$ |
| $\mathrm{R} 4=12 \mathrm{~K}$ |
| $\mathrm{R} 5=20 \mathrm{~K}$ |
| $\mathrm{R} 6=40 \mathrm{~K}$ |
|  |
|  |
| These models can be retrieved |
| electronically by accessing the ON |
| Semiconductor Web page at |
| http://design-net.sps.mot.com/models |
| and searching the section on |
| SMALLBLOCKTM models |

MDC5001T1
TYPICAL OPEN LOOP CHARACTERISTICS


Figure 1. $\mathrm{V}_{\text {ref }}$ versus $\mathrm{V}_{\mathrm{Cc}} @ \mathrm{I}_{\text {out }}$

## TYPICAL OPEN LOOP CHARACTERISTICS

(Refer to Circuits of Figures 10 through 15)


Figure 2. $\Delta \mathrm{V}_{\text {ref }}$ versus $\mathrm{T}_{\mathbf{J}} @ \mathrm{I}_{\text {out }}$


Figure 4. Q2 Current Gain versus Output Current @ $\mathrm{T}_{\mathbf{J}}$


Figure 3. Icc versus $\mathrm{V}_{\mathrm{cc}} @ \mathrm{~T}_{\mathrm{J}}$


Figure 5. $\mathrm{I}_{\text {enable }}$ versus $\mathrm{V}_{\text {enable }}$


Figure 6. $\mathrm{V}_{\text {ref }}$ versus $\mathrm{V}_{\text {enable }} @ \mathrm{~V}_{\mathrm{Cc}}$ and $\mathrm{I}_{\mathrm{out}}$

## MDC5001T1

TYPICAL CLOSED LOOP PERFORMANCE
(Refer to Circuits of Figures 16 \& 17)


Figure 7. $\Delta \mathbf{I}_{\mathbf{C} 3}$ versus $\mathrm{T}_{\mathbf{A}} @ \mathrm{I}_{\mathbf{C} 3}$


Figure 8. $\Delta \mathrm{V}_{\text {ref }}$ versus External Transistor DC Beta @ $\mathrm{I}_{\mathrm{C}}$


Figure 9. $\Delta \mathrm{I}_{\mathrm{C} 3}$ versus External Transistor DC Beta @ $\mathrm{I}_{\mathrm{C}}$

## OPEN LOOP TEST CIRCUITS



Figure 10. ICc versus $V_{C C}$ Test Circuit


Figure 12. $\mathrm{V}_{\text {ref }}$ versus $\mathrm{T}_{\mathrm{J}}$ Test Circuit


Figure 14. IENBL versus VENBL Test Circuit


Figure 11. $\mathbf{V}_{\text {ref }}$ versus $\mathrm{V}_{\mathrm{Cc}}$ Test Circuit


Figure 13. $\mathrm{H}_{\text {FE }}$ versus $\mathrm{I}_{\text {out }}$ Test Circuit


Figure 15. $\mathrm{V}_{\text {ref }}$ versus $\mathrm{V}_{\text {ENBL }}$ Test Circuit

NOTE 1: $\mathrm{V}_{\mathrm{BE} 3}$ is used to simulate actual operating conditions that reduce $\mathrm{V}_{\mathrm{CE} 2}$ \& $\mathrm{H}_{\mathrm{FE} 2}$, and increase $\mathrm{I}_{\mathrm{B} 2}$ \& $\mathrm{V}_{\text {ref }}$.

## CLOSED LOOP TEST CIRCUITS



Figure 17. RF Stage $\mathrm{I}_{\mathrm{C} 3}$ versus $\mathrm{T}_{\mathrm{A}}$ Test Circuit

## MDC5001T1

## APPLICATION CIRCUITS



Step 1: Choose $\mathrm{V}_{\mathrm{CC}}$ (1.8 V Min to 10 V Max)
Step 2: Insure that Min $\mathrm{V}_{\mathrm{ENBL}}$ is $\geq$ minimum indicated in Figures 5 and 6.
Step 3: Choose bias current, $\mathrm{I}_{\mathrm{C} 3}$, and calculate needed $\mathrm{I}_{\text {out }}$ from typ $\mathrm{H}_{\text {FE3 }}$
Step 4: From Figure 1, read $\mathrm{V}_{\text {ref }}$ for $\mathrm{V}_{\mathrm{CC}}$ and $\mathrm{I}_{\text {out }}$ calculated.
Step 5: Calculate Nominal $\mathrm{R} 5=\left(\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\text {ref }}\right) \div\left(\mathrm{I}_{\mathrm{C} 3}+\mathrm{I}_{\mathrm{out}}\right)$. Tweak as desired.
Figure 18. Class A Biasing of a Typical 900 MHz BJT Amplifier Application

## MDC5001T1



Step 1: Choose $V_{C C}$ (1.8 V Min to 10 V Max)
Step 2: Insure that Min $V_{\text {ENBL }}$ is $\geq$ minimum indicated in Figures 5 and 6.
Step 3: Choose bias current, $\mathrm{I}_{\mathrm{D}}$, and determine needed gate-source voltage, $\mathrm{V}_{\mathrm{GS}}$.
Step 4: Choose $I_{\text {out }}$ keeping in mind that too large an $I_{\text {out }}$ can impair MDC5000 $\Delta \mathrm{V}_{\text {ref }} / \Delta T_{J}$ performance (Figure 2) but too large an R6 can cause $l_{\text {DGO }} \& I_{G S O}$ to bias on the FET.
Step 5: Calculate $\mathrm{R} 6=\left(\mathrm{V}_{\mathrm{GS}}+\mathrm{E}_{\mathrm{GS}}\right) \div \mathrm{I}_{\text {out }}$
Step 6: From Figure 1, read $V_{\text {ref }}$ for $V_{C C} \& I_{\text {out }}$ chosen
Step 7: Calculate Nominal $R 5=\left(V_{C C}-V_{\text {ref }}\right) \div\left(I_{D}+I_{\text {out }}\right.$. Tweak as desired.
Figure 19. Class A Biasing of a Typical 890 MHz Depletion Mode GaAs FET Amplifier
http://onsemi.com

CHAPTER 3
Case Outlines and Package Dimensions

## CASE OUTLINES AND PACKAGE DIMENSIONS

TO-92 (TO-226)
CASE 29-11
ISSUE AL


TO-220
CASE 221A-09
ISSUE AA


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: INCH.
2. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

|  | INCHES |  | MILLIMETERS |  |
| :---: | ---: | ---: | ---: | ---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | --- | 1.15 | --- |
| $\mathbf{Z}$ | --- | 0.080 | --- | 2.04 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

5 LEAD TO-220 (THA5)
CASE 314A-03
ISSUE E


TO-220
CASE 314B-05
ISSUE J

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI
Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE
INTERCONNECT BAR (DAMBAR) PROTRUSION.
DIMENSION D INCLUDING PROTRUSION SHALL
NOT EXCEED 0.043 (1.092) MAXIMUM.

|  | INCHES |  |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |
| A | 0.572 | 0.613 | 14.529 | 15.570 |  |
| B | 0.390 | 0.415 | 9.906 | 10.541 |  |
| C | 0.170 | 0.180 | 4.318 | 4.572 |  |
| D | 0.025 | 0.038 | 0.635 | 0.965 |  |
| E | 0.048 | 0.055 | 1.219 | 1.397 |  |
| F | 0.850 | 0.935 | 21.590 | 23.749 |  |
| G | 0.067 | BSC | 1.702 | BSC |  |
| H | 0.166 | BSC | 4.216 | BSC |  |
| J | 0.015 | 0.025 | 0.381 | 0.635 |  |
| K | 0.900 | 1.100 | 22.860 | 27.940 |  |
| L | 0.320 | 0.365 | 8.128 | 9.271 |  |
| N | 0.320 | BSC | 8.128 | BSC |  |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |  |
| S | --- | 0.620 | --- | 15.748 |  |
| U | 0.468 | 0.505 | 11.888 | 12.827 |  |
| V | --- | 0.735 | --- | 18.669 |  |
| W | 0.090 | 0.110 | 2.286 | 2.794 |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

TO-220
CASE 314D-04
ISSUE E


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE

INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 0.572 | 0.613 | 14.529 | 15.570 |
| B | 0.390 | 0.415 | 9.906 | 10.541 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.025 | 0.038 | 0.635 | 0.965 |
| E | 0.048 | 0.055 | 1.219 | 1.397 |
| G | 0.067 BSC |  | 1.702 BSC |  |
| H | 0.087 | 0.112 | 2.210 | 2.845 |
| J | 0.015 | 0.025 | 0.381 | 0.635 |
| K | 0.990 | 1.045 | 25.146 | 26.543 |
| L | 0.320 | 0.365 | 8.128 | 9.271 |
| Q | 0.140 | 0.153 | 3.556 | 3.886 |
| U | 0.105 | 0.117 | 2.667 | 2.972 |

## 5 LEAD TO-220 (THE5) <br> CASE 314J-01 <br> ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION D DOES NOT INCLUDE

INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. DIMENSIONS EXCLUSIVE OF MOLD FLASH AND METAL BURRS.
5. FOOTPAD LENGTH MEASURED FROM LEAD TIP WITH REFERENCE TO DATUM -M-.
6. COPLANARITY 0.004" MAX. REFERENCE TO DATUM -N STANDOFF HEIGHT $0.00-0.010$ ".

|  | INCHES |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |
| A | 0.568 | 0.583 | 14.43 | 14.81 |  |
| B | 0.395 | 0.405 | 10.03 | 10.29 |  |
| C | 0.170 | 0.180 | 4.32 | 4.57 |  |
| D | 0.028 | 0.036 | 0.71 | 0.91 |  |
| E | 0.045 | 0.055 | 1.14 | 1.40 |  |
| F | 0.543 | 0.558 | 13.79 | 14.17 |  |
| G | 0.067 BSC |  | 1.70 BSC |  |  |
| J | 0.014 | 0.022 | 0.36 | 0.56 |  |
| K | 0.073 | 0.088 | 1.85 | 2.24 |  |
| L | 0.324 | 0.339 | 8.23 | 8.61 |  |
| Q | 0.146 | 0.156 | 3.71 | 3.96 |  |
| S | 0.000 | 0.010 | 0.00 | 0.25 |  |
| U | 0.460 | 0.475 | 11.68 | 12.07 |  |
| W | $5^{\circ}$ |  | $5^{\circ}$ |  |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

## 5 LEAD (TVA5) <br> CASE 314K-01 ISSUE O



NOTES
. DIMENSION
CONTROLLING DIMENSION: INCH
DIMENSION D DOES NOT INCLUDE
INTERCONNECT BAR (DAMBAR) PROTRUSION INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSIO
NOT EXCEED $10.92(0.043)$ MAXIMUM.

|  | INCHES |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | ---: | ---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |
| A | 0.560 | 0.590 | 14.22 | 14.99 |  |
| B | 0.385 | 0.415 | 9.78 | 10.54 |  |
| C | 0.160 | 0.190 | 4.06 | 4.83 |  |
| D | 0.027 | 0.037 | 0.69 | 0.94 |  |
| E | 0.045 | 0.055 | 1.14 | 1.40 |  |
| F | 0.530 | 0.545 | 13.46 | 13.84 |  |
| G | 0.067 BSC |  | 1.70 BSC |  |  |
| J | 0.014 | 0.022 | 0.36 | 0.56 |  |
| K | 0.785 | 0.800 | 19.94 | 20.32 |  |
| L | 0.321 | 0.337 | 8.15 | 8.56 |  |
| M | 0.063 | 0.078 | 1.60 | 1.98 |  |
| Q | 0.146 | 0.156 | 3.71 | 3.96 |  |
| R | 0.271 | 0.321 | 6.88 | 8.15 |  |
| S | 0.146 | 0.196 | 3.71 | 4.98 |  |
| U | 0.460 | 0.475 | 11.68 | 12.07 |  |
| W | $5^{\circ}$ |  |  | $5^{\circ}$ |  |

## 5 LEAD TO-220 (TFVA5) <br> CASE 314N-01 <br> ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION. INCH.
3. DIMENSION D DOES NOT INCLUDE

INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. LEADS MAINTAIN A RIGHT ANGLE WITH

RESPECT TO THE PACKAGE BODY TO WITHIN $\pm 0.015$ "

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 0.604 | 0.614 | 15.34 | 15.60 |
| B | 0.395 | 0.405 | 10.03 | 10.29 |
| C | 0.175 | 0.185 | 4.44 | 4.70 |
| D | 0.027 | 0.037 | 0.69 | 0.94 |
| E | 0.100 | 0.110 | 2.54 | 2.79 |
| F | 0.712 | 0.727 | 18.08 | 18.47 |
| G | 0.067 BSC |  | 1.70 BSC |  |
| H | 0.020 | 0.030 | 0.51 | 0.76 |
| J | 0.014 | 0.022 | 0.36 | 0.56 |
| K | 0.889 | 0.904 | 22.58 | 22.96 |
| L | 0.324 | 0.339 | 8.23 | 8.61 |
| M | 0.115 | 0.130 | 2.92 | 3.30 |
| N | 0.115 | 0.125 | 2.92 | 3.17 |
| Q | 0.120 | 0.130 | 3.05 | 3.30 |
| R | 0.292 | 0.342 | 7.42 | 8.69 |
| S | 0.133 | 0.183 | 3.38 | 4.65 |
| U | 0.480 | 0.495 | 12.19 | 12.57 |
| W | $5^{\circ}$ |  | $5^{\circ}$ |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AH


SOT-223 (TO-261)
CASE 318E-04
ISSUE K


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

|  | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 0.249 | 0.263 | 6.30 | 6.70 |
| B | 0.130 | 0.145 | 3.30 | 3.70 |
| C | 0.060 | 0.068 | 1.50 | 1.75 |
| D | 0.024 | 0.035 | 0.60 | 0.89 |
| F | 0.115 | 0.126 | 2.90 | 3.20 |
| G | 0.087 | 0.094 | 2.20 | 2.40 |
| H | 0.0008 | 0.0040 | 0.020 | 0.100 |
| J | 0.009 | 0.014 | 0.24 | 0.35 |
| K | 0.060 | 0.078 | 1.50 | 2.00 |
| L | 0.033 | 0.041 | 0.85 | 1.05 |
| M | $0^{\circ}$ | $10^{\circ}$ | $00^{\circ}$ | $10^{\circ}$ |
| S | 0.264 | 0.287 | 6.70 | 7.30 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

TSOP-6
CASE 318G-02
ISSUE H



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD

FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

|  | MILLIMETERS |  | INCHES |  |
| :---: | ---: | ---: | ---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.1142 | 0.1220 |
| B | 1.30 | 1.70 | 0.0512 | 0.0669 |
| C | 0.90 | 1.10 | 0.0354 | 0.0433 |
| D | 0.25 | 0.50 | 0.0098 | 0.0197 |
| G | 0.85 | 1.05 | 0.0335 | 0.0413 |
| H | 0.013 | 0.100 | 0.0005 | 0.0040 |
| J | 0.10 | 0.26 | 0.0040 | 0.0102 |
| K | 0.20 | 0.60 | 0.0079 | 0.0236 |
| L | 1.25 | 1.55 | 0.0493 | 0.0610 |
| M | $0^{\circ}$ | $10^{\circ}$ | 0 | 0 |
| S | 2.50 | 3.00 | 0.0985 | 0.1181 |

SOT-23L
CASE 318J-01
ISSUE B


## CASE OUTLINES AND PACKAGE DIMENSIONS

DPAK
CASE 369-07
ISSUE M


DPAK
CASE 369A-13
ISSUE AB

notes

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

|  | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.250 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.033 | 0.040 | 0.84 | 1.01 |
| F | 0.037 | 0.047 | 0.94 | 1.19 |
| G | 0.090 BSC |  | 2.29 BSC |  |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.175 | 0.215 | 4.45 | 5.46 |
| S | 0.050 | 0.090 | 1.27 | 2.28 |
| V | 0.030 | 0.050 | 0.77 | 1.27 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

|  | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.250 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.033 | 0.040 | 0.84 | 1.01 |
| F | 0.037 | 0.047 | 0.94 | 1.19 |
| G | 0.180 BSC |  | 4.58 BSC |  |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.090 BSC |  | 2.29 |  |
| BSC |  |  |  |  |
| R | 0.175 | 0.215 | 4.45 | 5.46 |
| S | 0.020 | 0.050 | 0.51 | 1.27 |
| U | 0.020 | --- | 0.51 | --- |
| V | 0.030 |  | 0.050 | 0.77 |
| Z | 0.138 | --- | 1.27 |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

3 LEAD D²PAK CASE 418E-01
ISSUE O

NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

|  | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 0.326 | 0.336 | 8.28 | 8.53 |
| B | 0.396 | 0.406 | 10.05 | 10.31 |
| C | 0.170 | 0.180 | 4.31 | 4.57 |
| D | 0.026 | 0.036 | 0.66 | 0.91 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.090 | 0.110 | 2.29 | 2.79 |
| G | 0.100 BSC | 2.54 BSC |  |  |
| H | 0.098 | 0.108 | 2.49 | 2.74 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.204 | 0.214 | 5.18 | 5.44 |
| L | 0.045 | 0.055 | 1.14 | 1.40 |
| M | 0.055 | 0.066 | 1.40 | 1.68 |
| N | 0.000 | 0.004 | 0.00 | 0.10 |

## 3 LEAD D²PAK <br> CASE 418F-01 ISSUE O



NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES |  | MILLIMETERS |  |  |
| :---: | :---: | ---: | ---: | ---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | 0.326 | 0.336 | 8.28 | 8.53 |  |
| B | 0.396 | 0.406 | 10.05 | 10.31 |  |
| C | 0.170 | 0.180 | 4.31 | 4.57 |  |
| D | 0.026 | 0.036 | 0.66 | 0.91 |  |
| E | 0.045 | 0.055 | 1.14 | 1.40 |  |
| F | 0.058 | 0.078 | 1.47 |  |  |
|  | 1.98 |  |  |  |  |
| G | 0.100 |  | BSC | 2.54 BSC |  |
| H | 0.098 | 0.108 | 2.49 | 2.74 |  |
| J | 0.018 | 0.025 | 0.46 | 0.64 |  |
| K | 0.163 | 0.173 | 4.14 | 4.39 |  |
| L | 0.045 | 0.055 | 1.14 | 1.40 |  |
| M | 0.055 | 0.066 | 1.40 | 1.68 |  |
| N | 0.000 | 0.004 | 0.00 | 0.10 |  |

N

## CASE OUTLINES AND PACKAGE DIMENSIONS

SC-88A (SOT-323)
CASE 419A-02
ISSUE F


SC-88 (SOT-363) CASE 419B-02 ISSUE J


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.

| DIM | INCHES |  | MILLIMETERS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |  |
| A | 0.071 | 0.087 | 1.80 | 2.20 |  |  |
| B | 0.045 | 0.053 | 1.15 | 1.35 |  |  |
| C | 0.031 | 0.043 | 0.80 | 1.10 |  |  |
| D | 0.004 | 0.012 | 0.10 |  |  |  |
| G | 0.026 |  | BSC | 0.65 BSC |  |  |
| H | --- | 0.004 | --- |  |  |  |
| J | 0.004 | 0.010 | 0.10 |  |  |  |
| K | 0.004 | 0.012 | 0.25 |  |  |  |
| N | 0.008 |  | REF | 0.20 |  | REF |
| S | 0.079 |  | 0.087 | 2.00 |  | 2.20 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

|  | INCHES |  | MILLIMETERS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |  |
| A | 0.071 | 0.087 | 1.80 | 2.20 |  |  |
| B | 0.045 | 0.053 | 1.15 | 1.35 |  |  |
| C | 0.031 | 0.043 | 0.80 | 1.10 |  |  |
| D | 0.004 | 0.012 | 0.10 |  |  |  |
| G | 0.026 |  | BSC | 0.65 BSC |  |  |
| H | --- | 0.004 | -- |  |  |  |
| J | 0.004 | 0.010 | 0.10 | 0.25 |  |  |
| K | 0.004 | 0.012 | 0.10 |  |  |  |
| N | 0.008 |  | REF | 0.20 |  | REF |
| S | 0.079 | 0.087 | 2.00 |  |  |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

SC-82
CASE 419C-01
ISSUE A


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

|  | MILLIMETERS |  | INCHES |  |
| :---: | ---: | ---: | ---: | ---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 1.8 | 2.2 | 0.071 | 0.087 |
| B | 1.15 | 1.45 | 0.045 | 0.057 |
| C | 0.8 | 1.1 | 0.031 | 0.043 |
| D | 0.2 | 0.4 | 0.008 | 0.016 |
| F | 0.3 | 0.5 | 0.012 | 0.020 |
| G | 1.1 | 1.5 | 0.043 | 0.059 |
| H | 0.0 | 0.1 | 0.000 | 0.004 |
| J | 0.10 | 0.26 | 0.004 | 0.010 |
| K | 0.1 | --- | 0.004 | --- |
| L | 0.05 | BSC | 0.002 BSC |  |
| N | 0.7 | REF | 0.028 |  |
| REF |  |  |  |  |
| S | 1.8 | 2.4 | 0.07 |  |

TSOP-5
CASE 483-01
ISSUE B


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETER
2. MAXIMUM LEAD THICKNESS INCLUDES LEAD MAXIMUM LEAD THICKNESS INCLUDES LEAD
FINISH THICKNESS. MINIMUM LEAD THICKNESS FINISH THICKNESS. MINIMUM LEAD THICK
IS THE MINIMUM THICKNESS OF BASE IS THE MINI
MATERIAL.

|  | MILLIMETERS |  | INCHES |  |
| :---: | ---: | ---: | ---: | ---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.1142 | 0.1220 |
| B | 1.30 | 1.70 | 0.0512 | 0.0669 |
| C | 0.90 | 1.10 | 0.0354 | 0.0433 |
| D | 0.25 | 0.50 | 0.0098 | 0.0197 |
| G | 0.85 | 1.05 | 0.0335 | 0.0413 |
| H | 0.013 | 0.100 | 0.0005 | 0.0040 |
| J | 0.10 | 0.26 | 0.0040 | 0.0102 |
| K | 0.20 | 0.60 | 0.0079 | 0.0236 |
| L | 1.25 | 1.55 | 0.0493 | 0.0610 |
| M | $0^{\circ}$ | $10^{\circ}$ | $0^{\circ}$ | $10^{\circ}$ |
| S | 2.50 | 3.00 | 0.0985 | 0.1181 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

QFN 2x2
CASE 488-02
ISSUE B

notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
. CONTROLLING DIMENSION: MILLIMETERS.
2. 488-01 OBSOLETE. NEW STANDARD IS 488-02

\left.|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 2.18 | 2.23 | 0.086 | 0.088 |
| B | 1.98 | 2.03 | 0.078 | 0.080 |
| C | 0.88 | 0.93 | 0.035 | 0.037 |
| D | 0.23 | 0.28 | 0.009 |  |$\right) 0.011 ~\left[\right.$| G | 0.650 BSC |  | 0.026 BSC |  |
| :---: | :---: | :---: | :---: | :---: |
| H | 0.35 | 0.40 | 0.014 |  |
| J | 0.05 | 0.10 | 0.002 |  |
| L | 1.28 | 1.33 | 0.050 |  |
| S | 0.33 | 0.38 | 0.004 |  |

8 LEAD PDIP<br>CASE 626-05<br>ISSUE L



NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | ---: | ---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 | BSC | 0.100 |  |
| BSC |  |  |  |  |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 |  |
| K | 2.92 | 3.43 | 0.115 |  |
| L | 7.62 | BSC | 0.300 |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE M


## CASE OUTLINES AND PACKAGE DIMENSIONS

PDIP-16
CASE 648C-04
ISSUE D


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION L TO CENTER OF LEADS WHEN

FORMED PARALIEL
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH

|  | INCHES |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |
| A | 0.744 | 0.783 | 18.90 | 19.90 |  |
| B | 0.240 | 0.260 | 6.10 | 6.60 |  |
| C | 0.145 | 0.185 | 3.69 | 4.69 |  |
| D | 0.015 |  | 0.021 | 0.38 |  |
| E | 0.050 |  | BSC | 1.27 |  |
| BSC |  |  |  |  |  |
| F | 0.040 | 0.70 | 1.02 |  | 1.78 |
| G | 0.100 BSC |  | 2.54 |  | BSC |
| J | 0.008 |  | 0.015 | 0.20 |  |
| K | 0.115 |  | 0.135 | 2.92 |  |
| L | 0.300 |  | BSC | 7.62 |  |
| M | $0^{\circ}$ |  | $10^{\circ}$ | $0^{\circ}$ |  |
| N | 0.015 | 0.040 | $10^{\circ}$ |  |  |

PDIP-16
CASE 648E-01
ISSUE O


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
6. ROUNDED CORNER OPTIONAL

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.760 | 18.80 | 19.30 |
| B | 0.245 | 0.260 | 6.23 | 6.60 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC |  | 2.54 BSC |  |
| H | 0.050 BSC |  | 1.27 BSC |  |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.120 | 0.140 | 3.05 | 3.55 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | $0^{\circ}$ | $10^{\circ}$ | $0^{\circ}$ | $10^{\circ}$ |
| P | 0.200 BSC |  | 5.08 BSC |  |
| R | 0.300 BSC |  | 7.62 BSC |  |
| S | 0.015 | 0.035 | 0.39 | 0.88 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

## 18 LEAD PDIP <br> CASE 707-02 <br> ISSUE D



NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN $0.25 \mathrm{~mm}(0.010)$ AT MAXIMUM
MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 0.875 | 0.915 | 22.22 | 23.24 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.140 | 0.180 | 3.56 | 4.57 |
| D | 0.014 | 0.022 | 0.36 | 0.56 |
| F | 0.050 | 0.070 | 1.27 | 1.78 |
| G | 0.100 BSC |  | 2.54 BSC |  |
| H | 0.040 | 0.060 | 1.02 | 1.52 |
| J | 0.008 | 0.012 | 0.20 | 0.30 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC |  | 7.62 BSC |  |
| M | $0^{\circ}$ | $15^{\circ}$ | $0^{\circ}$ | $15^{\circ}$ |
| N | 0.020 | 0.040 | 0.51 | 1.02 |

40 LEAD PDIP
CASE 711-03
ISSUE D


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN $0.25 \mathrm{~mm}(0.010)$ AT MAXIMUM
MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER
2. DIMENSION LTO CENTER OF LEADS WHEN

FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH. 4. CONTROLLING DIMENSION: INCH.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 51.69 | 52.45 | 2.035 | 2.065 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC |  | 0.100 BSC |  |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC |  | 0.600 BSC |  |
| M | $0^{\circ}$ | $15^{\circ}$ | $0^{\circ}$ | $15^{\circ}$ |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

PDIP-24
CASE 724-03
ISSUE D


NOTES:

1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 1.230 | 1.265 | 31.25 | 32.13 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.020 | 0.38 | 0.51 |
| E | 0.050 BSC |  | 1.27 BSC |  |
| F | 0.040 | 0.060 | 1.02 | 1.52 |
| G | 0.100 BSC |  | 2.54 BSC |  |
| J | 0.007 | 0.012 | 0.18 | 0.30 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC |  | 7.62 BSC |  |
| M | $0^{\circ}$ | $15^{\circ}$ | $0^{\circ}$ | $15^{\circ}$ |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

PDIP-20
CASE 738-03
ISSUE E


## CASE OUTLINES AND PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE W


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
. MAXIMUM MOLD PROTRUSION $0.15(0.006)$ PER SIDE. DIMENSION D DOES NOT INCLUDE DAMBA PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G |  | BSC |  | BSC |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | $0^{\circ}$ | $8{ }^{\circ}$ | $0{ }^{\circ}$ | $8{ }^{\circ}$ |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOIC-14
CASE 751A-03
ISSUE F


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 ( 0.006 ) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE 0.127 ( 0.005 ) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

|  | MILLIMETERS |  | INCHES |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |  |
| A | 8.55 | 8.75 | 0.337 | 0.344 |  |  |
| B | 3.80 | 4.00 | 0.150 | 0.157 |  |  |
| C | 1.35 | 1.75 | 0.054 | 0.068 |  |  |
| D | 0.35 | 0.49 | 0.014 | 0.019 |  |  |
| F | 0.40 | 1.25 | 0.016 | 0.049 |  |  |
| G | 1.27 |  | BSC | 0.050 |  | BSC |
| J | 0.19 | 0.25 | 0.008 | 0.009 |  |  |
| K | 0.10 | 0.25 | 0.004 | 0.009 |  |  |
| M | 0 | $7^{\circ}$ | $0^{\circ}$ | $7^{\circ}$ |  |  |
| P | 5.80 | 6.20 | 0.228 | 0.244 |  |  |
| R | 0.25 | 0.50 | 0.010 | 0.019 |  |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE J


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) MAXIMUM M
PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

|  | MILLIMETERS |  | INCHES |  |
| :---: | ---: | ---: | ---: | ---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC |  | 0.050 |  |
| BSC |  |  |  |  |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | $0^{\circ}$ | $7^{\circ}$ | $0^{\circ}$ | $7^{\circ}$ |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOIC-20
CASE 751D-05 ISSUE F


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS

INTERPRET DIMENSIONS AND TOLERANCES
INTERPRET DIMENSIONS AND TOLERANCES
PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION

|  | MILLIMETERS |  |
| :---: | ---: | ---: |
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 |  |
| BSC |  |  |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| $\boldsymbol{\theta}$ | $0^{\circ}$ | $7^{\circ}$ |

## CASE OUTLINES AND PACKAGE DIMENSIONS

SOIC-24
CASE 751E-04
ISSUE E


28 LEAD SOIC WB
CASE 751F-05
ISSUE G


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR

PROTRUSION. ALLOWABLE DAMBER
PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN
EXCESS OF B DIMENSION AT MAXIMUM
MATERIAL CONDITION.

|  | MILLIMETERS |  |
| :---: | :---: | :---: |
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.13 | 0.29 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 17.80 | 18.05 |
| E | 7.40 | 7.60 |
| G | 1.27 | BSC |
| H | 10.05 | 10.55 |
| L | 0.41 | 0.90 |
| M | $0^{\circ}$ | $8^{\circ}$ |

## CASE OUTLINES AND PACKAGE DIMENSIONS

SOIC-16 WB
CASE 751G-03
ISSUE B


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS
2. INTERPRET DIMENSIONS AND TOLERANCES

INTERPRET DIMENSIONS AND TOLERANCES
PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |  |
| :---: | :---: | :---: |
|  | MIN | MAX |
| A | 2.35 | 2.65 |
| A | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 | BSC |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| $\boldsymbol{\theta}$ | $0{ }^{\circ}$ | $7^{\circ}$ |

## SOIC-16 WB <br> CASE 751K-01 ISSUE O



NOTES:
. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETER
DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE 0.127 ( 0.005 ) TOTALIN PROTRUSION SHALL BE 0.127 (0.005) TOTAL I EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.368 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 | BSC | 0.050 |  |
| BSC |  |  |  |  |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | $0^{\circ}$ | $7^{\circ}$ | $0^{\circ}$ | $7^{\circ}$ |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

SOIC-16 WB
CASE 751N-01
ISSUE O


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI YIMENSIONING
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 ( 0.006 ) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | ---: | ---: | ---: | ---: |
|  | MIN | MAX | MIN | MAX |
| A | 10.15 | 10.45 | 0.400 | 0.411 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | 0.050 |  | BSC |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | $0^{\circ}$ | $7^{\circ}$ | 0 | $0^{\circ}$ |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |
| S | 2.54 BSC | 0.100 BSC |  |  |
| T | 3.81 BSC | 0.150 BSC |  |  |

SO-32, WB
CASE 751P-01
ISSUE O


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE
5. DIMENSION B DOES NOT INCLUDE DAMBAR

PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS
OF B DIMENSION AT MAXIMUM MATERIAL
CONDITION.

|  | MILLIMETERS |  |
| :---: | :---: | :---: |
| DIM | MIN | MAX |
| A | 2.29 | 2.54 |
| A1 | 0.10 | 0.25 |
| B | 0.36 | 0.51 |
| C | 0.15 | 0.32 |
| D | 20.57 | 20.88 |
| E | 7.42 | 7.60 |
| G | 1.27 | BSC |
| H | 10.29 | 10.64 |
| L | 0.53 | 1.04 |
| M | $0{ }^{\circ}$ | $8^{\circ}$ |

## CASE OUTLINES AND PACKAGE DIMENSIONS



## CASE OUTLINES AND PACKAGE DIMENSIONS

7 LEAD TO-220 (T7)
CASE 821E-04
ISSUE C


M,

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 0.600 | 0.610 | 15.24 | 15.49 |
| B | 0.386 | 0.403 | 9.80 | 10.23 |
| C | 0.170 | 0.180 | 4.32 | 4.56 |
| D | 0.028 | 0.037 | 0.71 | 0.94 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.088 | 0.102 | 2.24 | 2.59 |
| J | 0.018 | 0.026 | 0.46 | 0.66 |
| K | 1.028 | 1.042 | 26.11 | 26.47 |
| L | 0.355 | 0.365 | 9.02 |  |
| M | $5^{\circ}$ |  | NOM | 9.27 |
| Q | 0.142 | 0.148 | 3.61 | NOM |
| U | 0.490 | 0.501 | 12.45 | 12.72 |
| V | 0.045 | 0.055 | 1.15 | 1.39 |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
. DIMENSION D DOES NOT INCLUDE
INTERCONNECT BAR (DAMBAR) PROTRUSION. INTERCONNECT BAR (DAMBAR) PROTRUSION.
DIMENSION D INCLUDING PROTRUSION SHALL DIMENSION D INCLUDING PROTRUSIO
NOT EXCEED 10.92 (0.043) MAXIMUM.
3. LEADS MAINTAIN A RIGHT ANGLE WITH
4. LEADS MAINTAIN A RIGHT ANGLE WITH
RESPECT TO THE PACKAGE BODY TO WITH RESPECT
$\pm 0.020^{\prime \prime}$.

| DIM | INCHES |  | MILLIMETERS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |  |
| A | 0.560 | 0.590 | 14.22 | 14.99 |  |  |
| B | 0.385 | 0.415 | 9.77 | 10.54 |  |  |
| C | 0.160 | 0.190 | 4.06 | 4.82 |  |  |
| D | 0.023 | 0.037 | 0.58 | 0.94 |  |  |
| E | 0.045 | 0.055 | 1.14 | 1.40 |  |  |
| F | 0.568 | 0.583 | 14.43 | 14.81 |  |  |
| G | 0.050 |  | BSC | 1.27 |  |  |
| BSC |  |  |  |  |  |  |
| J | 0.015 | 0.022 | 0.38 | 0.56 |  |  |
| K | 0.728 | 0.743 | 18.49 | 18.87 |  |  |
| L | 0.322 | 0.337 | 8.18 | 8.56 |  |  |
| M | 0.101 | 0.116 | 2.57 | 2.95 |  |  |
| N | 0.090 | 0.115 | 2.28 | 2.91 |  |  |
| Q | 0.146 | 0.156 | 3.70 | 3.95 |  |  |
| S | 0.150 | 0.200 | 3.81 | 5.08 |  |  |
| U | 0.460 | 0.475 | 11.68 | 12.07 |  |  |
| W | $3^{\circ}$ |  |  | $3^{\circ}$ |  |  |



## CASE OUTLINES AND PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE

INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

| DIM | INCHES |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | 0.560 | 0.590 | 14.22 | 14.99 |  |
| B | 0.385 | 0.415 | 9.77 | 10.54 |  |
| C | 0.160 | 0.190 | 4.06 | 4.82 |  |
| D | 0.023 | 0.037 | 0.58 | 0.94 |  |
| E | 0.045 | 0.055 | 1.14 | 1.40 |  |
| F | 0.540 | 0.555 | 13.72 | 14.10 |  |
| G | 0.050 BSC |  | 1.27 BSC |  |  |
| H | 0.570 | 0.595 | 14.48 | 15.11 |  |
| J | 0.014 | 0.022 | 0.36 | 0.56 |  |
| K | 0.785 | 0.800 | 19.94 | 20.32 |  |
| L | 0.322 | 0.337 | 8.18 | 8.56 |  |
| M | 0.073 | 0.088 | 1.85 | 2.24 |  |
| N | 0.090 | 0.115 | 2.28 | 2.91 |  |
| Q | 0.146 | 0.156 | 3.70 | 3.95 |  |
| R | 0.289 | 0.304 | 7.34 | 7.72 |  |
| S | 0.164 | 0.179 | 4.17 | 4.55 |  |
| U | 0.460 | 0.475 | 11.68 | 12.07 |  |
| W | $3^{\circ}$ |  |  | $3^{\circ}$ |  |



Micro8
CASE 846A-02
ISSUE E

## CASE OUTLINES AND PACKAGE DIMENSIONS

MICRO-10
CASE 846B-02
ISSUE B


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B-01 OBSOLETE. NEW STANDARD 846B-02

|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | 0.95 | 1.10 | 0.037 | 0.043 |
| D | 0.20 | 0.35 | 0.008 | 0.014 |
| G | 0.50 BSC |  | 0.020 |  |
| HSC |  |  |  |  |
| H | 0.05 | 0.15 | 0.002 | 0.006 |
| J | 0.10 | 0.21 | 0.004 | 0.008 |
| K | 4.75 | 5.05 | 0.187 | 0.199 |
| L | 0.40 | 0.70 | 0.016 | 0.028 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

TQFP-32
CASE 873-01
ISSUE A



DETAIL C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE - H -.
5. DIMENSIONS S AND $V$ TO BE DETERMINED AT SEATING PLANE -C-
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 ( 0.010 ) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 ( 0.003 ) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 6.95 | 7.10 | 0.274 | 0.280 |
| B | 6.95 | 7.10 | 0.274 | 0.28 |
| C | 1.40 | 1.60 | 0.055 | 0.06 |
| D | 0.273 | 0.373 | 0.010 | 0.015 |
| E | 1.30 | 1.50 | 0.051 | 0.059 |
| F | 0.273 | -- | 0.010 |  |
| G | 0.80 BSC |  | 0.031 BSC |  |
| H | --- | 0.20 | --- | 0.008 |
| J | 0.119 | 0.197 | 0.005 | 0.008 |
| K | 0.33 | 0.57 | 0.013 | 0.022 |
| L | 5.6 REF |  | 0.220 REF |  |
| M | $6^{\circ}$ | $8^{\circ}$ | $6^{\circ}$ | $8^{\circ}$ |
| N | 0.119 | 0.135 | 0.005 | 0.005 |
| P | 0.40 BSC |  | 0.016 BSC |  |
| Q | $5^{\circ}$ | $10^{\circ}$ | $5^{\circ}$ | $10^{\circ}$ |
| R | 0.15 | 0.25 | 0.006 | 0.010 |
| S | 8.85 | 9.15 | 0.348 | 0.360 |
| T | 0.15 | 0.25 | 0.006 | 0.010 |
| U | $5^{\circ}$ | $11^{\circ}$ | $5^{\circ}$ | $11^{\circ}$ |
| V | 8.85 | 9.15 | 0.348 | 0.360 |
| X | 1.00 REF |  | 0.039 REF |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

LQFP
CASE 873A-02
ISSUE A

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-,- -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 7.000 BSC |  | 0.276 BSC |  |
| A1 | 3.500 BSC |  | 0.138 BSC |  |
| B | 7.000 BSC |  | 0.276 BSC |  |
| B1 | 3.500 BSC |  | 0.138 BSC |  |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC |  | 0.031 BSC |  |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.500 | 0.700 | 0.020 | 0.028 |
| M | $12^{\circ} \mathrm{REF}$ |  | $12^{\circ} \mathrm{REF}$ |  |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC |  | 0.016 BSC |  |
| Q | $1^{\circ}$ | $5^{\circ}$ | $1^{\circ}$ | $5{ }^{\circ}$ |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC |  | 0.354 BSC |  |
| S1 | 4.500 BSC |  | 0.177 BSC |  |
| V | 9.000 BSC |  | 0.354 BSC |  |
| V1 | 4.500 BSC |  | 0.177 BSC |  |
| W | 0.200 REF |  | 0.008 REF |  |
| X | 1.000 REF |  | 0.039 REF |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.
3. CONTROLLING DIMENSION: INCH.
4. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS

A AND K.
DIMENSIONS U AND V ESTABLISH A MINIMUM
4. DIMENSIONS U AND V ESTABLISH A MINIM
MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E | 0.045 | 0.055 | 1.143 | 1.397 |
| F | 0.051 REF |  | 1.295 REF |  |
| G | 0.100 BSC |  | 2.540 BSC |  |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| J | 0.125 MAX |  | 3.175 MAX |  |
| K | 0.050 REF |  | 1.270 REF |  |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | $5^{\circ} \mathrm{REF}$ |  | $5^{\circ} \mathrm{REF}$ |  |
| S | 0.116 REF |  | 2.946 REF |  |
| U | 0.200 MIN |  | 5.080 MIN |  |
| V | 0.250 MIN |  | 6.350 MIN |  |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS TAB CONT
A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E | 0.045 | 0.055 | 1.143 | 1.397 |
| G | 0.067 BSC |  | 1.702 BSC |  |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| K | 0.050 REF |  | 1.270 REF |  |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | $5^{\circ} \mathrm{REF}$ |  | $5^{\circ} \mathrm{REF}$ |  |
| S | 0.116 REF |  | 2.946 REF |  |
| U | 0.200 MIN |  | 5.080 MIN |  |
| V | 0.250 MIN |  | 6.350 MIN |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS



## CASE OUTLINES AND PACKAGE DIMENSIONS

## 24 LEAD SSOP <br> CASE 940D-03 <br> ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED $0.15(0.006)$ PROTRUSION
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 ( 0.005 ) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
|  | 8.07 | 8.33 | 0.317 | 0.328 |
| B | 5.20 | 5.38 | 0.205 | 0.212 |
| C | 1.73 | 1.99 | 0.068 | 0.078 |
| D | 0.05 | 0.21 | 0.002 | 0.008 |
| F | 0.63 | 0.95 | 0.024 | 0.037 |
| G | 0.65 BSC |  | 0.026 BSC |  |
| H | 0.44 | 0.60 | 0.017 | 0.024 |
| J | 0.09 | 0.20 | 0.003 | 0.008 |
| J1 | 0.09 | 0.16 | 0.003 | 0.006 |
| K | 0.25 | 0.38 | 0.010 | 0.015 |
| K1 | 0.25 | 0.33 | 0.010 | 0.013 |
| L | 7.65 | 7.90 | 0.301 | 0.311 |
| M | $0 \circ$ | $8{ }^{\circ}$ | $0{ }^{\circ}$ | $8{ }^{\circ}$ |

TSSOP-20
CASE 948E-02
ISSUE A


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSI
PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | 0.026 BSC |  |  |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | 0.252 BSC |  |  |
| M | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |
|  |  |  |  |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

TSSOP-16
CASE 948F-01
ISSUE O


TSSOP-14
CASE 948G-01
ISSUE O


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM EXCESS OF THE K DIME
MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR TERMINAL NUMBER
REFERENCE ONLY.
REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

|  | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | 0.026 |  | BSC |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | 0.252 BSC |  |  |
| M | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |

## CASE OUTLINES AND PACKAGE DIMENSIONS

TSSOP-8
CASE 948J-01
ISSUE O


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE $0.08(0.003)$ TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM EXCESS OF THE K DIME
MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

|  | MILLIMETERS |  | INCHES |  |  |  |
| :---: | :---: | ---: | ---: | ---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |  |
| A | 2.90 | 3.10 | 0.114 | 0.122 |  |  |
| B | 4.30 | 4.50 | 0.169 | 0.177 |  |  |
| C | --- | 1.20 | --- | 0.047 |  |  |
| D | 0.05 | 0.15 | 0.002 | 0.006 |  |  |
| F | 0.50 | 0.75 | 0.020 | 0.030 |  |  |
| G | 0.65 |  | BSC | 0.026 |  | BSC |
| H | 0.50 | 0.60 | 0.020 | 0.024 |  |  |
| J | 0.09 | 0.20 | 0.004 | 0.008 |  |  |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |  |  |
| K | 0.19 | 0.30 | 0.007 | 0.012 |  |  |
| K1 | 0.19 | 0.25 | 0.007 |  |  |  |
| L | 6.40 |  | 0.010 |  |  |  |
| M | 0.0 | 0.252 |  | BSC |  |  |

## CASE OUTLINES AND PACKAGE DIMENSIONS

TSSOP-24
CASE 948K-01
ISSUE O


NOTES:

1. Dimensioning and tolerancing per ansi Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR protrusion shal not exceed 0.25 (0.010) PER SIDE
5. DIMENSION K DOES NOT INCLUDE DAMBAR DIMENSION KDOESNOA INCLUDE DA
PROTRUSION. ALIOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTALIN EXCESS OF THE KDIMENSION AT MAXIMUM MATERIAL CONDITIN.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED at datum PLANE -W-.

|  | MILLIMETERS |  | INCHES |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |  |  |
| A | 7.70 | 7.90 | 0.303 | 0.311 |  |  |  |
| B | 5.50 | 5.70 | 0.216 | 0.224 |  |  |  |
| C | --- | 1.20 | --- | 0.047 |  |  |  |
| D | 0.05 | 0.15 | 0.002 | 0.006 |  |  |  |
| F | 0.50 | 0.75 | 0.020 | 0.030 |  |  |  |
| G | 0.65 BSC |  | 0.026 BSC |  |  |  |  |
| H | 0.27 | 0.37 | 0.011 | 0.015 |  |  |  |
| J | 0.09 | 0.20 | 0.004 | 0.008 |  |  |  |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |  |  |  |
| K | 0.19 | 0.30 | 0.007 | 0.012 |  |  |  |
| K1 | 0.19 | 0.25 | 0.007 |  |  |  |  |
| L | 7.60 |  | 0.010 |  |  |  |  |
| M | $0^{\circ}$ |  | $8^{\circ}$ | 0.299 |  | $0^{\circ}$ | BSC |

SO-14
CASE 965-01
ISSUE O


DETAIL P


NOTES: Y DIMENSIONIN
2. CONTROLING DIMENSION: ML HMETER
2. CIMENSIONS D AND EDO NOT INCLUDE
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE RADIUS OR THE FOOT. MINIMUM SPACE
BETWEEN PROTRUSIONS AND ADJACENT LEAD BETWEEN PROTRUS
TO BE 0.46 ( 0.018 ).

| DIM | MILLIMETERS |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |
|  | --- | 2.05 | --- | 0.081 |
| $\mathrm{~A}_{1}$ | 0.05 | 0.20 | 0.002 | 0.008 |
| $\mathbf{b}$ | 0.35 | 0.50 | 0.014 | 0.020 |
| $\mathbf{c}$ | 0.18 | 0.27 | 0.007 | 0.011 |
| $\mathbf{D}$ | 9.90 | 10.50 | 0.390 | 0.413 |
| $\mathbf{E}$ | 5.10 | 5.45 | 0.201 | 0.215 |
| $\mathbf{e}$ | 1.27 | BSC | 0.050 |  |
| $\mathrm{H}_{\mathbf{E}}$ | 7.40 | 8.20 | 0.291 | 0.323 |
| $\mathbf{0 . 5 0}$ | 0.50 | 0.85 | 0.020 | 0.033 |
| $\mathrm{~L}_{\mathbf{E}}$ | 1.10 | 1.50 | 0.043 | 0.059 |
| $\mathbf{M}$ | $0^{\circ}$ | $10^{\circ}$ | 0 | 0 |
| $\mathbf{Q}_{1}$ | 0.70 | 0.90 | 0.028 | $10^{\circ}$ |
| $\mathbf{Z}$ | --- | 1.42 | --- | 0.035 |

## CASE OUTLINES AND PACKAGE DIMENSIONS



NOTES

1. DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS D AND E DO NOT INCLUDE MOID FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION DAMBAR CANNOT BE LOCATED ON THE LOWER DAMBAR CANNOT BE LOCATED ON THE RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRU
TO BE 0.46 ( 0.018).

|  | MILLIMETERS |  | INCHES |  |
| :--- | ---: | ---: | ---: | ---: |
| DIM | MIN | MAX | MIN | MAX |
| $\mathbf{A}$ | --- | 2.05 | --- | 0.081 |
| $\mathbf{A}_{\mathbf{1}}$ | 0.05 | 0.20 | 0.002 | 0.008 |
| $\mathbf{b}$ | 0.35 | 0.50 | 0.014 | 0.020 |
| $\mathbf{c}$ | 0.18 | 0.27 | 0.007 | 0.011 |
| $\mathbf{D}$ | 9.90 | 10.50 | 0.390 | 0.413 |
| $\mathbf{E}$ | 5.10 | 5.45 | 0.201 | 0.215 |
| $\mathbf{e}$ | 1.27 BSC |  | 0.050 |  |
| $\mathrm{H}_{\mathbf{E}}$ | 7.40 | 8.20 | 0.291 | 0.323 |
| $\mathbf{L}$ | 0.50 | 0.85 | 0.020 | 0.033 |
| $\mathrm{~L}_{\mathbf{E}}$ | 1.10 | 1.50 | 0.043 | 0.059 |
| $\mathbf{M}$ | $0{ }^{\circ}$ | $10^{\circ}$ | $0^{\circ}$ | $10^{\circ}$ |
| $\mathbf{Q}_{\mathbf{1}}$ | 0.70 | 0.90 | 0.028 | 0.035 |
| $\mathbf{Z}$ | --- | 0.78 | --- | 0.031 |

SOT-23
CASE 1212-01
ISSUE O

otes:

1. DIMENSIONS ARE IN MILLIMETERS
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
3. DATUM C IS A SEATING PLANE.

|  | MILLIMETERS |  |
| :---: | :---: | :---: |
| DIM | MIN | MAX |
| A1 | 0.00 | 0.10 |
| A2 | 1.00 | 1.30 |
| B | 0.30 | 0.50 |
| C | 0.10 | 0.25 |
| D | 2.80 | 3.00 |
| E | 2.50 | 3.10 |
| E1 | 1.50 | 1.80 |
| e | 0.95 BSC |  |
| e1 | 1.90 BSC |  |
| L | 0.20 | --- |
| L1 | 0.45 | 0.75 |

## CASE OUTLINES AND PACKAGE DIMENSIONS

```
SOT-89 (3-LEAD)
    CASE 1213-02
        ISSUE C
```


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI
Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 1213-01 OBSOLETE, NEW STANDARD $1213-02$.

|  | MILLIMETERS |  |  |  |  | INCHES |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |  |  |  |
| A | 4.40 | 4.60 | 0.173 | 0.181 |  |  |  |
| B | 2.40 | 2.60 | 0.094 | 0.102 |  |  |  |
| C | 1.40 | 1.60 | 0.055 | 0.063 |  |  |  |
| D | 0.37 | 0.57 | 0.015 | 0.022 |  |  |  |
| E | 0.32 | 0.52 | 0.013 | 0.020 |  |  |  |
| F | 1.50 | 1.83 | 0.059 | 0.072 |  |  |  |
| G | 1.50 | BSC | 0.059 | BSC |  |  |  |
| H | 3.00 | BSC | 0.118 | BSC |  |  |  |
| J | 0.30 | 0.50 | 0.012 | 0.020 |  |  |  |
| K | 0.80 | --- | 0.031 | --- |  |  |  |
| L | --- | 4.25 | --- | 0.167 |  |  |  |

SOT-23
CASE 1262-01
ISSUE A


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS

INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
3. DIMENSION D DOES NOT INCLUDE FLASH OR PROTRUSIONS. FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.23 PER SIDE.
4HALL NOT EXCEED 0.23 PER SIDE.
4. TERMINAL NUMBER
5. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

| DIM | MILLIMETERS |  |
| :---: | :---: | :---: |
|  | MIN | MAX |
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| b | 0.35 | 0.50 |
| b1 | 0.35 | 0.45 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.15 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| e | 0.95 |  |
| e1 | 1.90 |  |
| L | 0.25 | 0.55 |
| $\boldsymbol{\theta}$ | $0{ }^{\circ}$ |  |

SECTION A-A
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## ON SEMICONDUCTOR STANDARD DOCUMENT TYPE DEFINITIONS

## DATA SHEET CLASSIFICATIONS

A Data Sheet is the fundamental publication for each individual product/device, or series of products/devices, containing detailed parametric information and any other key information needed in using, designing-in or purchasing of the product(s)/device(s) it describes. Below are the three classifications of Data Sheet: Product Preview; Advance Information; and Fully Released Technical Data

## PRODUCT PREVIEW

A Product Preview is a summary document for a product/device under consideration or in the early stages of development. The Product Preview exists only until an "Advance Information" document is published that replaces it. The Product Preview is often used as the first section or chapter in a corresponding reference manual. The Product Preview displays the following disclaimer at the bottom of the first page: "This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice."

## ADVANCE INFORMATION

The Advance Information document is for a device that is NOT fully qualified, but is in the final stages of the release process, and for which production is eminent. While the commitment has been made to produce the device, final characterization and qualification may not be complete. The Advance Information document is replaced with the "Fully Released Technical Data" document once the device/part becomes fully qualified. The Advance Information document displays the following disclaimer at the bottom of the first page: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

## FULLY RELEASED TECHNICAL DATA

The Fully Released Technical Data document is for a product/device that is in full production (i.e., fully released). It replaces the Advance Information document and represents a part that is fully qualified. The Fully Released Technical Data document is virtually the same document as the Product Preview and the Advance Information document with the exception that it provides information that is unavailable for a product in the early phases of development, such as complete parametric characterization data. The Fully Released Technical Data document is also a more comprehensive document than either of its earlier incarnations. This document displays no disclaimer, and while it may be informally referred to as a "data sheet," it is not labeled as such.

## DATA BOOK

A Data Book is a publication that contains primarily a collection of Data Sheets, general family and/or parametric information, Application Notes and any other information needed as reference or support material for the Data Sheets. It may also contain cross reference or selector guide information, detailed quality and reliability information, packaging and case outline information, etc.

## APPLICATION NOTE

An Application Note is a document that contains real-world application information about how a specific ON Semiconductor device/product is used, or information that is pertinent to its use. It is designed to address a particular technical issue. Parts and/or software must already exist and be available.

## SELECTOR GUIDE

A Selector Guide is a document published, generally at set intervals, that contains key line-item, device-specific information for particular products or families. The Selector Guide is designed to be a quick reference tool that will assist a customer in determining the availability of a particular device, along with its key parameters and available packaging options. In essence, it allows a customer to quickly "select" a device. For detailed design and parametric information, the customer would then refer to the device's Data Sheet. The Master Components Selector Guide (SG388/D) is a listing of ALL currently available ON Semiconductor devices.

## REFERENCE MANUAL

A Reference Manual is a publication that contains a comprehensive system or device-specific descriptions of the structure and function (operation) of a particular part/system; used overwhelmingly to describe the functionality or application of a device, series of devices or device category. Procedural information in a Reference Manual is limited to less than 40 percent (usually much less).

## HANDBOOK

A Handbook is a publication that contains a collection of information on almost any give subject which does not fall into the Reference Manual definition. The subject matter can consist of information ranging from a device specific design information, to system design, to quality and reliability information.

## ADDENDUM

A documentation Addendum is a supplemental publication that contains missing information or replaces preliminary information in the primary publication it supports. Individual addendum items are published cumulatively. The Addendum is destroyed upon the next revision of the primary document.


#### Abstract

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## PUBLICATION ORDERING INFORMATION

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[^0]:    6. Output voltages from 2.0 V to 6.0 V , in 0.1 V increments, are available on request
[^1]:    . Output voltages from 2.0 V to 6.0 V , in 0.1 V increments, are available on request
    *Q2, 2001

[^2]:    10. Output voltages from 2.0 V to 6.0 V , in 0.1 V increments, are available on request.
    *Q2, 2001
[^3]:    ${ }^{*} \mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter.
    ${ }^{* *} C_{O}$ is not needed for stability; however, it does improve transient response.

[^4]:    $z z=05,08,09,12,15,18$ or 24
    A = Assembly Location
    L = Wafer Lot
    Y = Year
    WW = Work Week

[^5]:    ${ }^{*} \mathrm{C}_{\text {in }}$ is required if regulator is located an appreciable distance from power supply filter. (See Applications Informationfor details.)
    ${ }^{* *} \mathrm{C}_{o}$ is not needed for stability; however, it does improve transient response.

[^6]:    xx = Nominal Voltage
    A = Assembly Location
    WL = Wafer Lot
    Y = Year
    WW = Work Week

[^7]:    *Contact your ON Semiconductor sales representative for other output voltage values.

[^8]:    *Pin 6 GND is not directly shorted to the fused paddle GND. The fused paddle GND (pins 4, 5, 12, 13) is connected through the substrate. Pin 6 must be electrically connected to at least one of the fused paddle GND's on the PC board.

[^9]:    1. $\mathrm{I}_{\text {out }}$ (Output Current) is the measured current when the output voltage drops below 0.3 V with respect to $\mathrm{V}_{\text {out }}$ at $\mathrm{I}_{\text {out }}=30 \mathrm{~mA}$.
[^10]:    ${ }^{*} \mathrm{C}_{1}$ is required if the regulator is far from the power source filter.
    ${ }^{* *} \mathrm{C}_{2}$ is required for stability.

[^11]:    1. 10 second maximum.
[^12]:    This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

[^13]:    *Additional ordering information can be found on page 727 of this data sheet.
    $\dagger$ TO-220 is 3 -pin, straight leaded. $D^{2}$ PAK are all 3 -pin.

[^14]:    ${ }^{*} \mathrm{C}_{1}$ is required if the regulator is far from the power source filter.
    ${ }^{* *} \mathrm{C}_{2}$ is required for stability.

[^15]:    ${ }^{*} \mathrm{C}_{1}$ required if regulator is located far from power supply filter.
    ${ }^{* *} \mathrm{C}_{2}$ and $\mathrm{C}_{3}$ required for stability. Capacitor must operate at minimum temperature expected during system operations.

[^16]:    ${ }^{*} \mathrm{C}_{1}$ required if regulator is located far from power supply filter.
    ${ }^{* *} \mathrm{C}_{2}$ and $\mathrm{C}_{3}$ required for stability. Capacitor must operate at minimum temperature expected during system operations.

[^17]:    ${ }^{*} \mathrm{C}_{1}$ required if regulator is located far from power supply filter.
    ${ }^{* *} \mathrm{C}_{2}$ and $\mathrm{C}_{3}$ required for stability. Capacitor must operate at minimum temperature expected during system operations.

[^18]:    This document contains information on a new product. Specifications and information herein are subject to change without notice.

[^19]:    2. For $\mathrm{V}_{\mathrm{IN}} \leq 4.5 \mathrm{~V}$, a RESET = Low may occur with the output in regulation.
[^20]:    This document contains information on a new product. Specifications and information
    herein are subject to change without notice.

[^21]:    2. For $\mathrm{VIN} \leq 4.5 \mathrm{~V}$, a RESET = Low may occur with the output in regulation.
[^22]:    This document contains information on a new product. Specifications and information

[^23]:    * Add Q1, C13, and R7-R10, and Change R4 to 2.0 k $\Omega$ for Charger Output

[^24]:    *Measurements performed using Voltech PM1200 ac power analysis.

[^25]:    Control Logic Inputs from Microcontroller Output Ports

[^26]:    NOTE: 2 Refer to "Voltage Sensing" text of Operating Description. Guaranteed by Design Only; NOT TESTED.

[^27]:    This document contains information on a new product. Specifications and information herein are subject to change without notice.

[^28]:    $x x x=3.3,5.0,12,15$, or ADJ
    A = Assembly Location
    WL = Wafer Lot
    Y = Year
    WW = Work Week

[^29]:    Vout $=15 \mathrm{~V}$
    A: Output Pin Voltage, 10 V/DIV
    B: Inductor Current, 2.0 A/DIV
    C: Inductor Current, 2.0 A/DIV, AC-Coupled
    D: Output Ripple Voltage, $50 \mathrm{mV} / \mathrm{dDIV}$, AC-Coupled
    Horizontal Time Base: $5.0 \mu \mathrm{~s} / \mathrm{DIV}$

[^30]:    2. Guaranteed by design, not $100 \%$ tested in productions.
[^31]:    6. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
[^32]:    3. Guaranteed by design, not $100 \%$ tested in production.
[^33]:    2. Not tested in production. Specification is guaranteed by design.
[^34]:    * Consult your local sales representative for other package options.

[^35]:    Trace 1- Regulator Output Voltage ( $100 \mathrm{mV} / \mathrm{div}$.)
    Trace 2- Regulator Output Voltage (10 A/div.)

[^36]:    Trace 1- Regulator Output Voltage (1.0 V/div.)
    Trace 2- Regulator Output Voltage (20 V/div.)

[^37]:    1. Split Power Supplies.
[^38]:    This document contains information on a new product. Specifications and information

[^39]:    2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
    3. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC34064
    $-40^{\circ} \mathrm{C}$ for MC33064
    $\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC34064
    $+85^{\circ} \mathrm{C}$ for MC33064
[^40]:    2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
    $\mathrm{T}_{\text {low }}=-40^{\circ} \mathrm{C}$ for MC33153 $\quad \mathrm{T}_{\text {high }}=+105^{\circ} \mathrm{C}$ for MC33153
[^41]:    X = Don't Care; MSB is Transferred first.

[^42]:    * $\mathrm{V}_{\mathrm{CC}}=6.0 \mathrm{~V}$ TO 26 V

[^43]:    ${ }^{*} \mathrm{~V}_{\text {in }}$ switched from 0.8 to 2.0 V .
    Typical values determined at $25^{\circ} \mathrm{C}$ ambient and 5.0 V supply.

[^44]:    1. $\mathrm{T}_{\text {low }}=0^{\circ} \mathrm{C}$ for MC1496
    $=-40^{\circ} \mathrm{C}$ for MC1496B
    $\mathrm{T}_{\text {high }}=+70^{\circ} \mathrm{C}$ for MC1496

    $$
    =+125^{\circ} \mathrm{C} \text { for MC1496B }
    $$

